High Performance Digital Fractional-N Frequency Synthesizers

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October 16, 2008

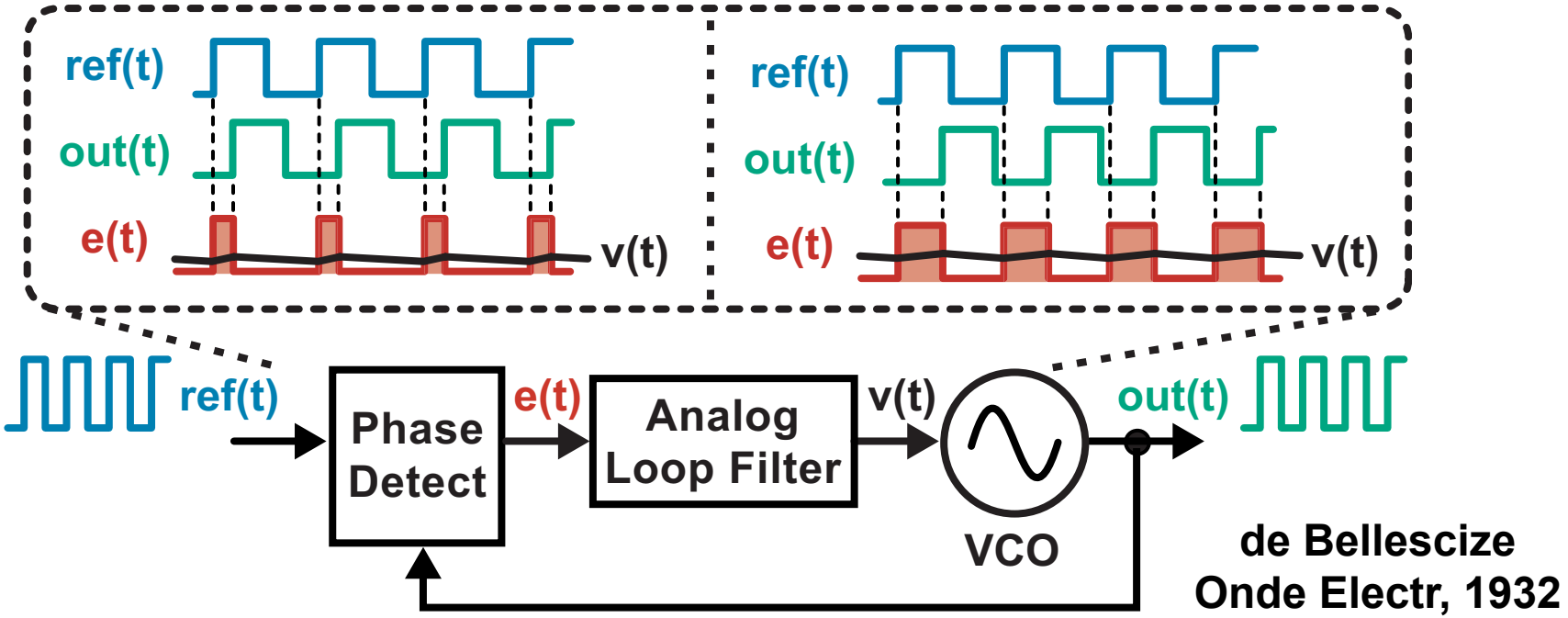
Why Are Digital Phase-Locked Loops Interesting?

- PLLs are needed for a wide range of applications
  - Communication systems (both wireless and wireline)
  - Digital processors (to achieve GHz clocks)
- Performance is important
  - Phase noise can limit wireless transceiver performance
  - Jitter can be a problem for digital processors
- The standard analog PLL implementation is problematic in many applications
  - Analog building blocks on a mostly digital chip pose design and verification challenges
  - The cost of implementation is becoming too high …

Can digital phase-locked loops offer excellent performance with a lower cost of implementation?

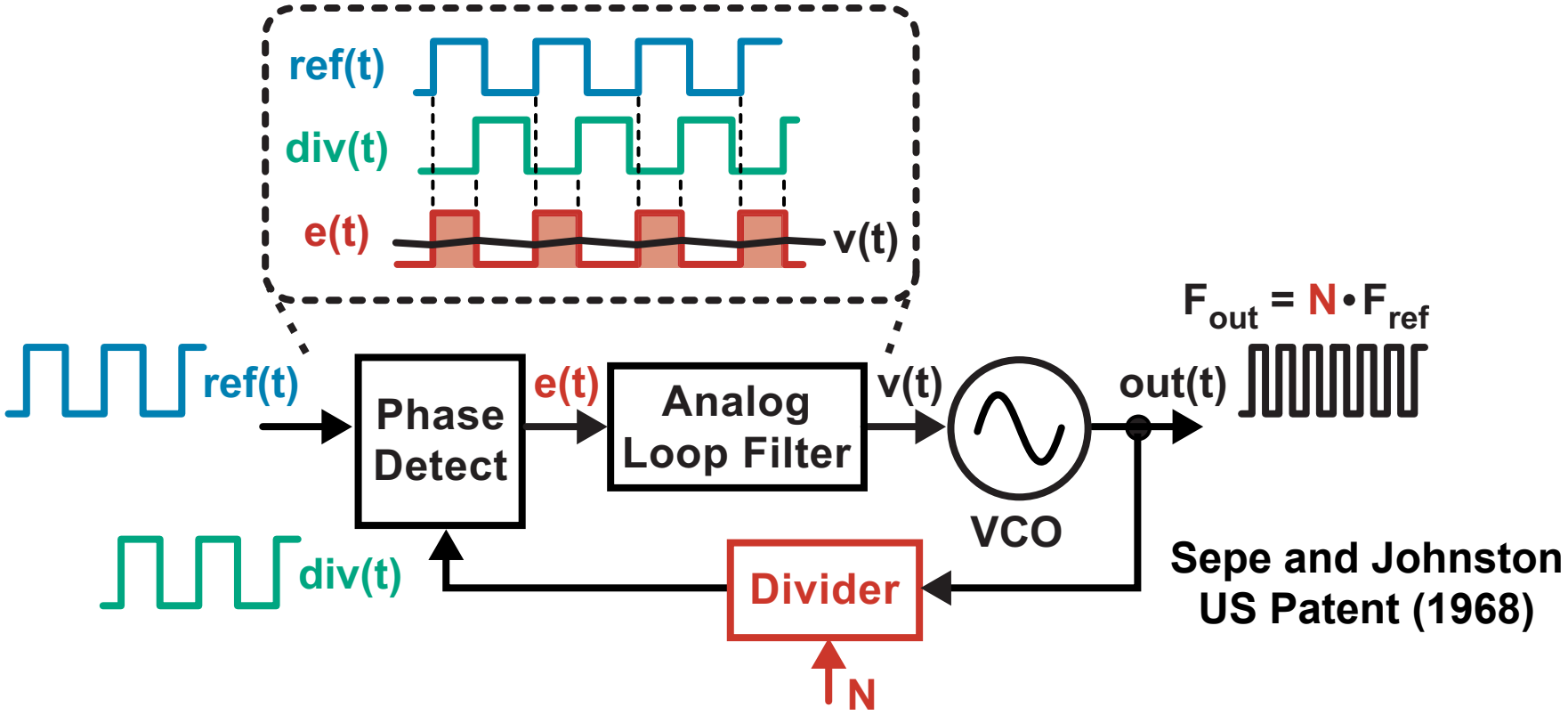
Just Enough PLL Background …

What is a Phase-Locked Loop (PLL)?



- **VCO efficiently provides oscillating waveform with variable frequency**
- **PLL synchronizes VCO frequency to input reference frequency through feedback**
  - **Key block is phase detector**
    - Realized as *digital gates* that create pulsed signals

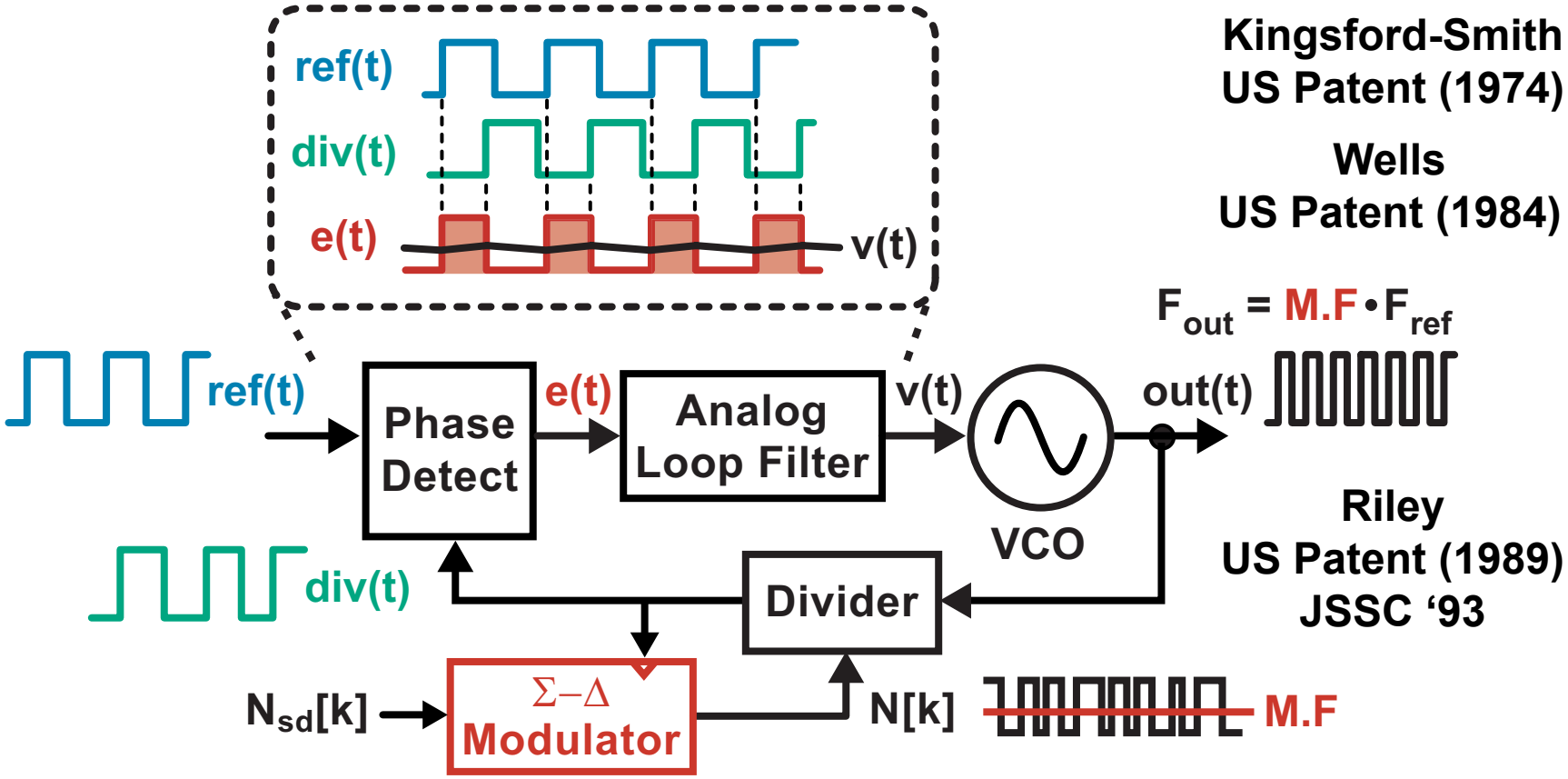
Integer-N Frequency Synthesizers



- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Output frequency is digitally controlled

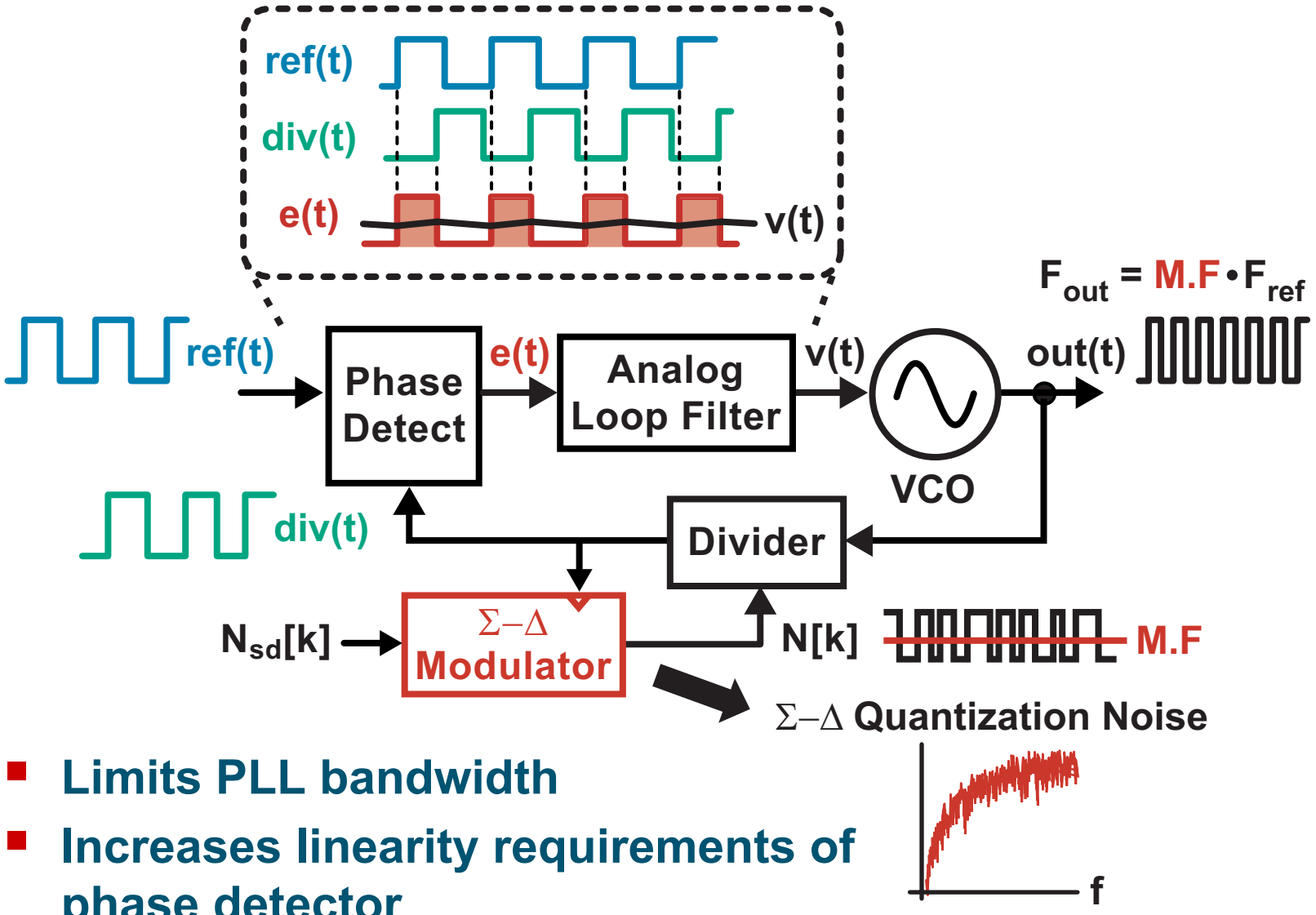
Fractional-N Frequency Synthesizers



- Dither divide value to achieve fractional divide values
  - PLL loop filter smooths the resulting variations

Very high frequency resolution is achieved

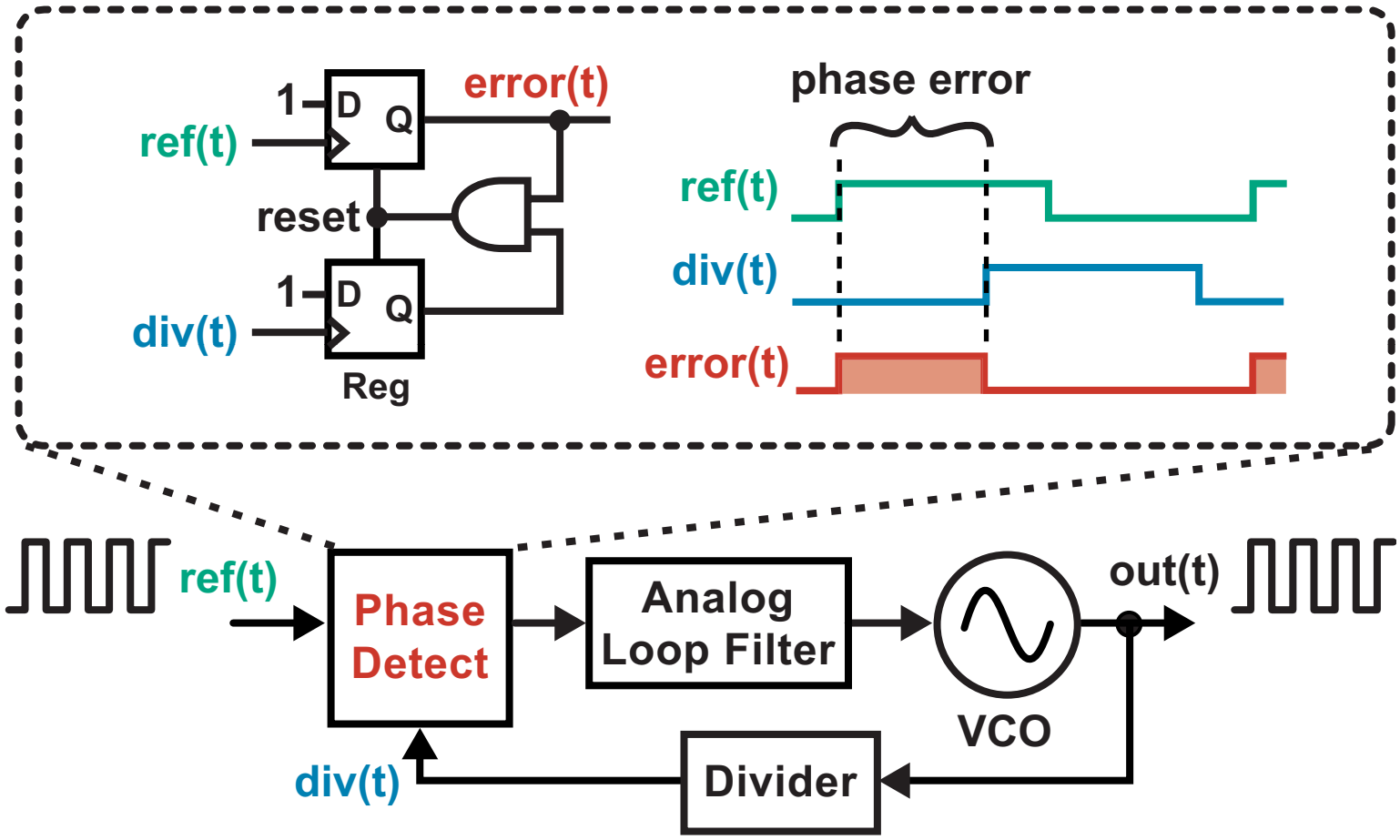
The Issue of Quantization Noise



- Limits PLL bandwidth
- Increases linearity requirements of phase detector

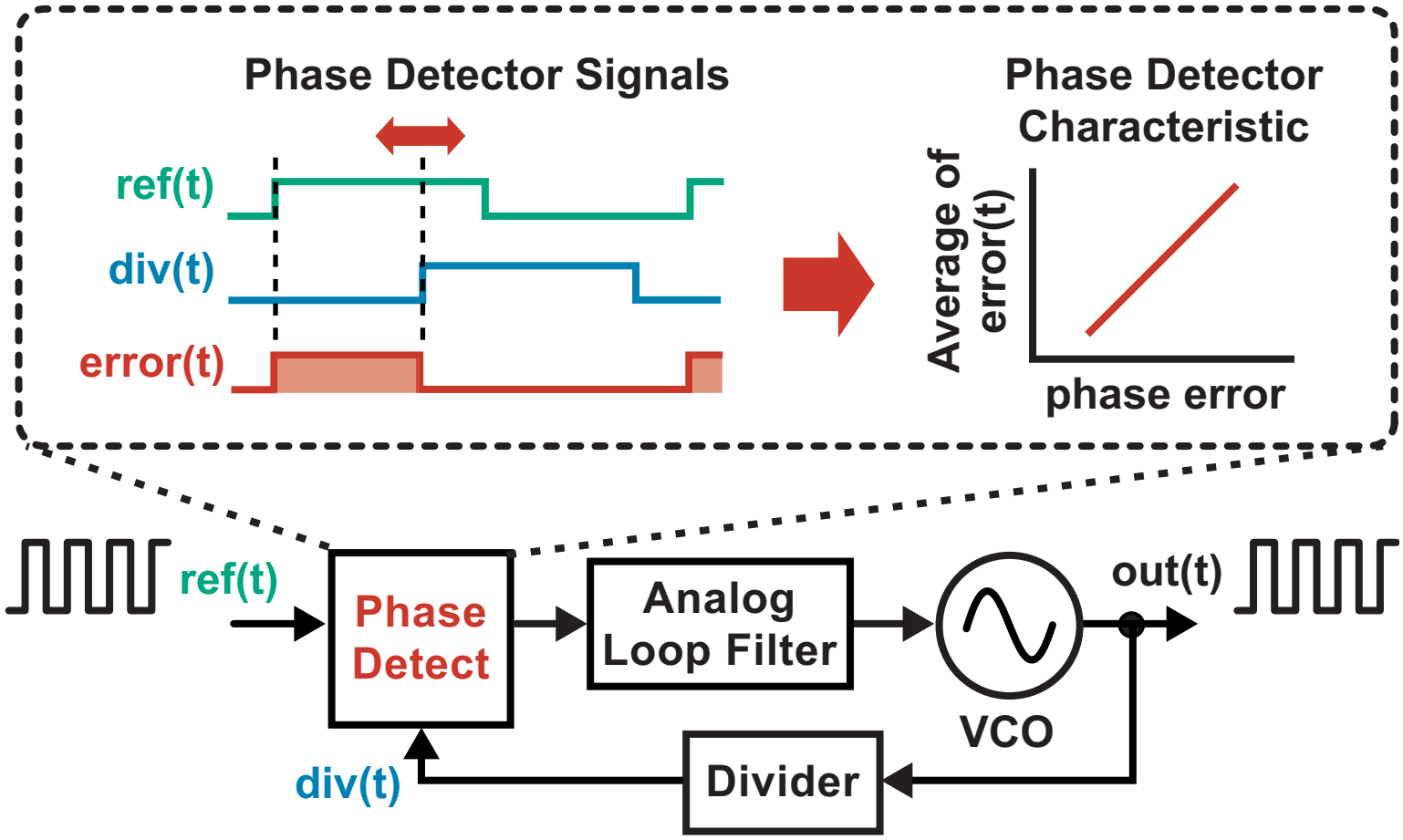
Striving for a Better PLL Implementation

Analog Phase Detection



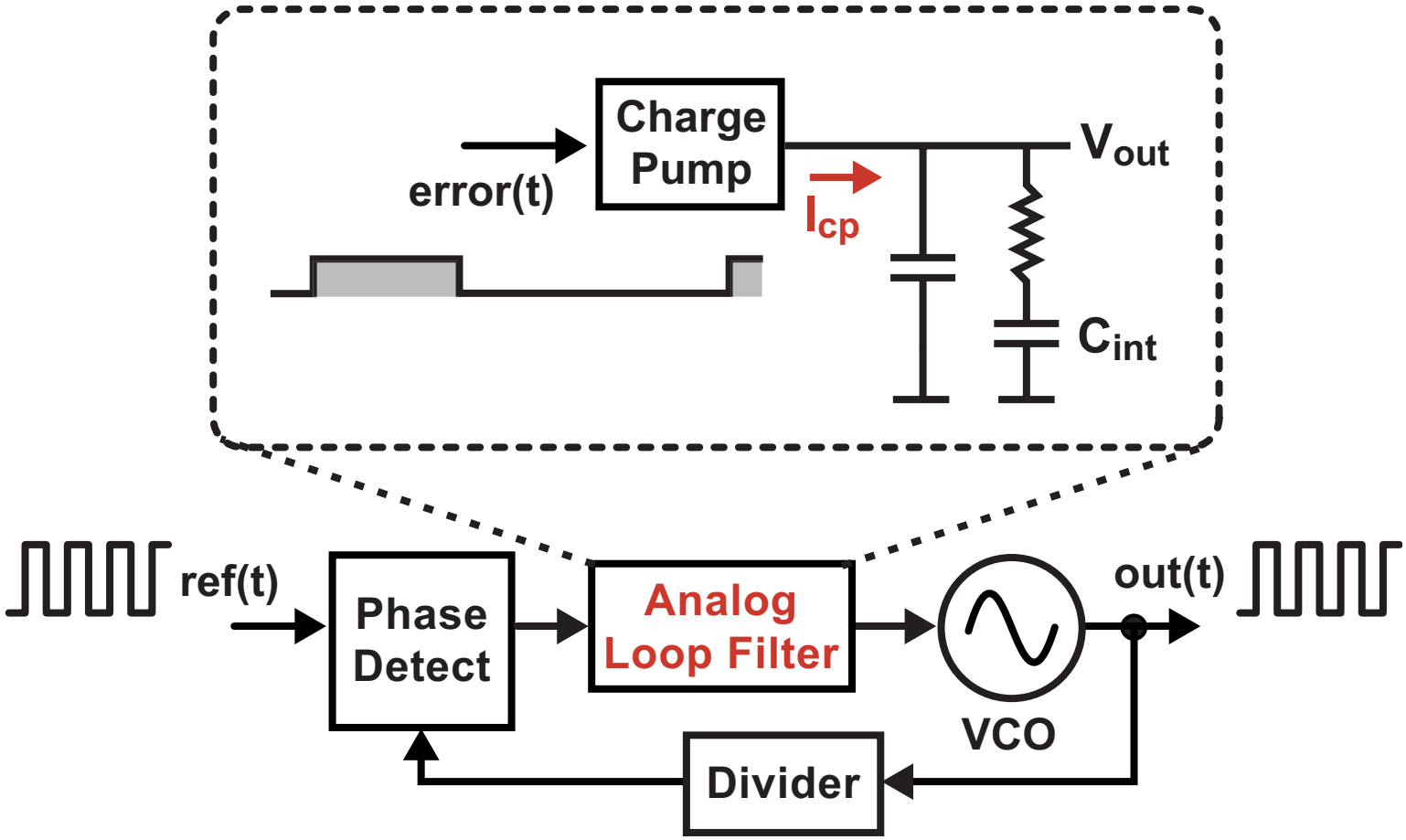
- Pulse width is formed according to phase difference between two signals
- Average of pulsed waveform is applied to VCO input

Tradeoffs of Analog Approach



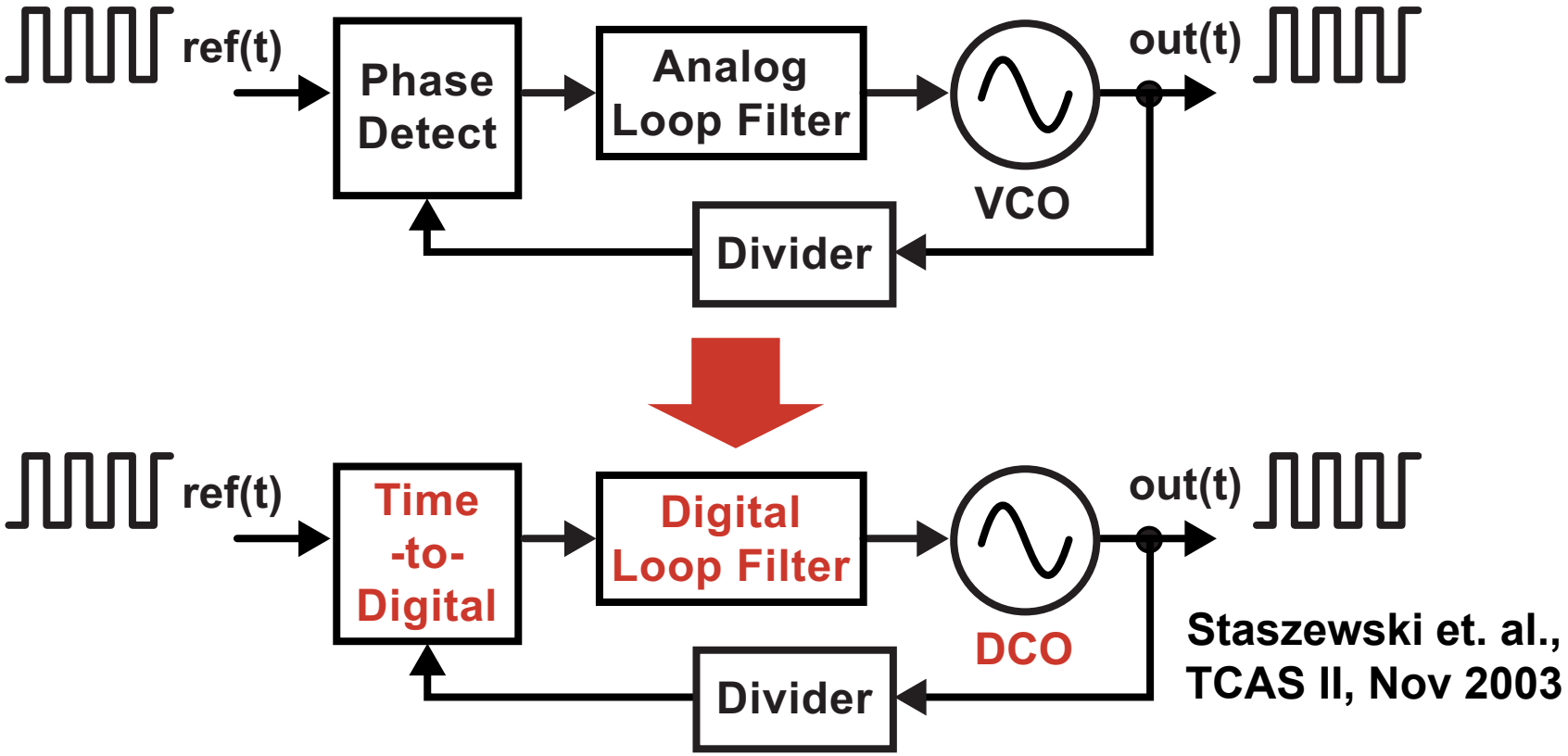
- **Benefit: average of pulsed output is a continuous, linear function of phase error**
- **Issue: analog loop filter implementation is undesirable**

Issues with Analog Loop Filter



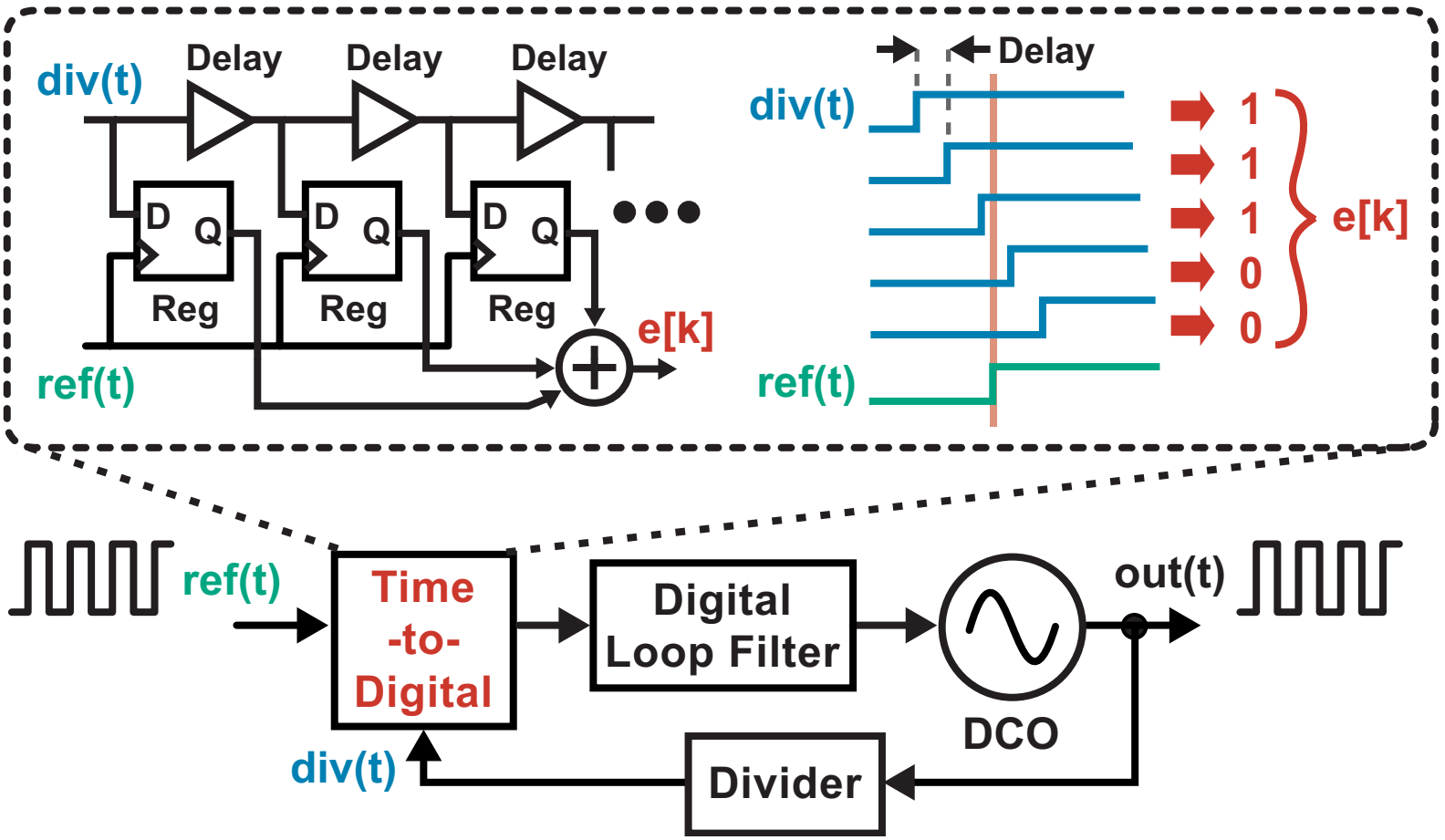
- Charge pump: output resistance, mismatch
- Filter caps: leakage current, *large area*

Going Digital …



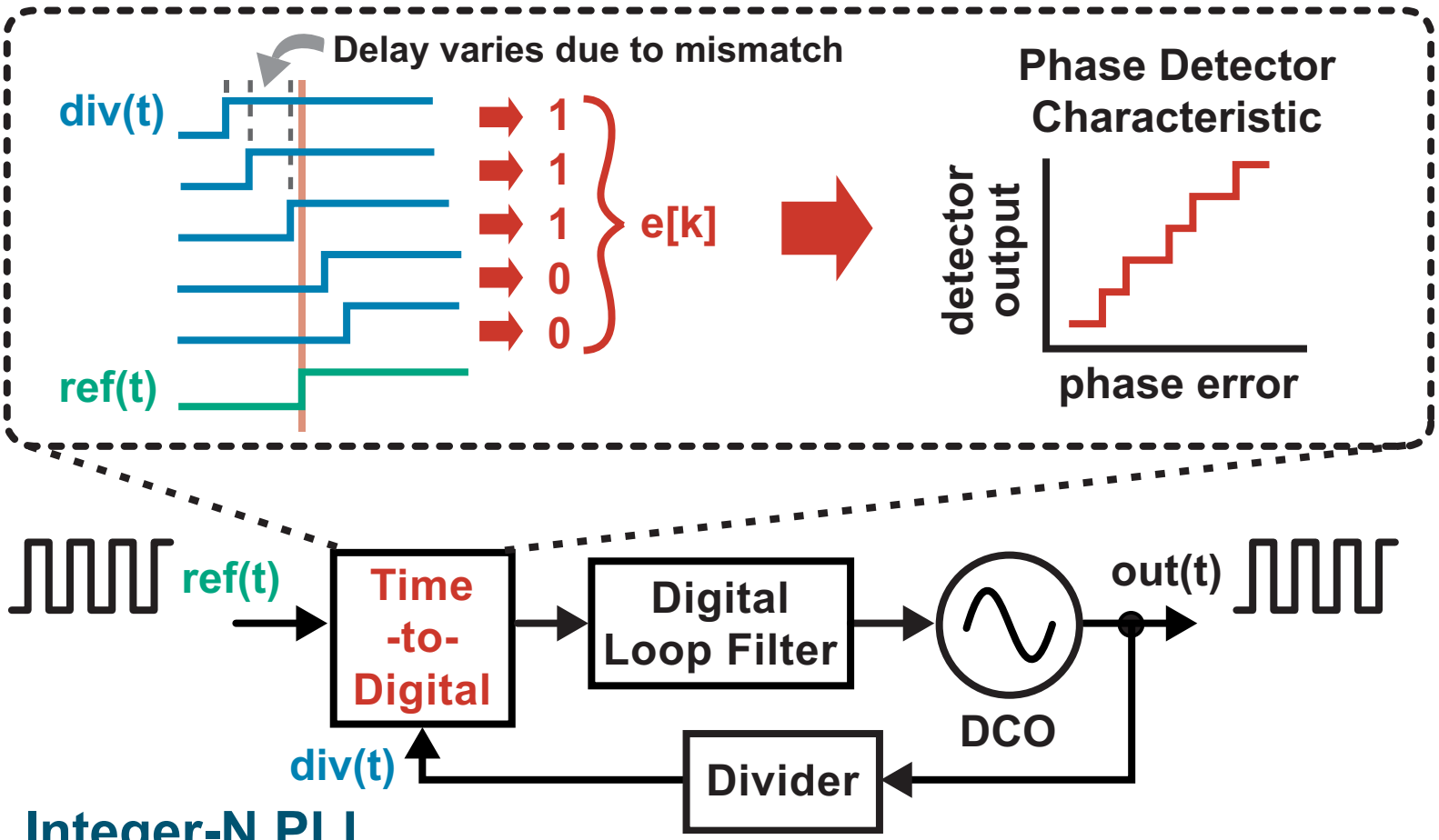
- Digital loop filter: compact area, insensitive to leakage
- Challenges:
  - Time-to-Digital Converter (TDC)
  - Digitally-Controlled Oscillator (DCO)

Classical Time-to-Digital Converter



- Resolution set by a "Single Delay Chain" structure
  - Phase error is measured with delays and registers
- Corresponds to a flash architecture

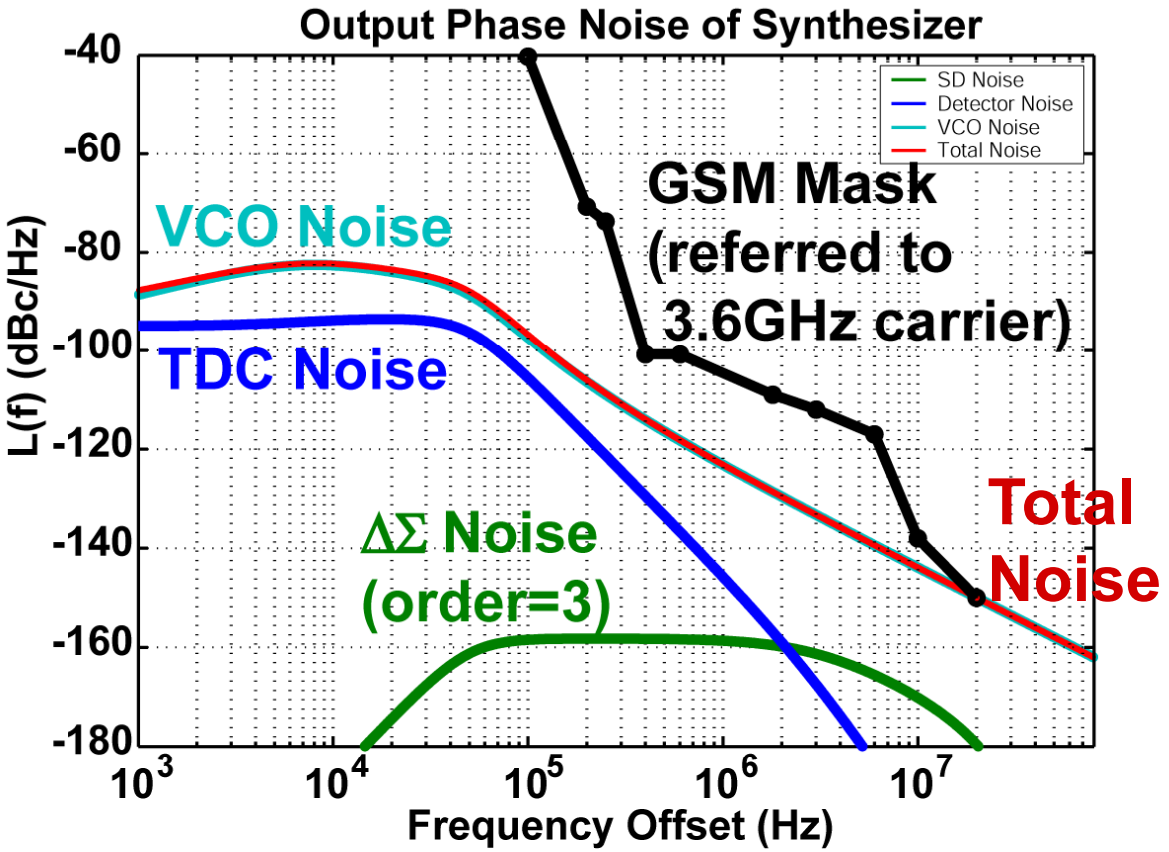
Impact of Limited Resolution and Delay Mismatch



- **Integer-N PLL**
  - Limit cycles due to limited resolution (unless high ref noise)
- **Fractional-N PLL**
  - Fractional spurs due to non-linearity from delay mismatch

Examine Noise Performance: Narrow-Bandwidth Case

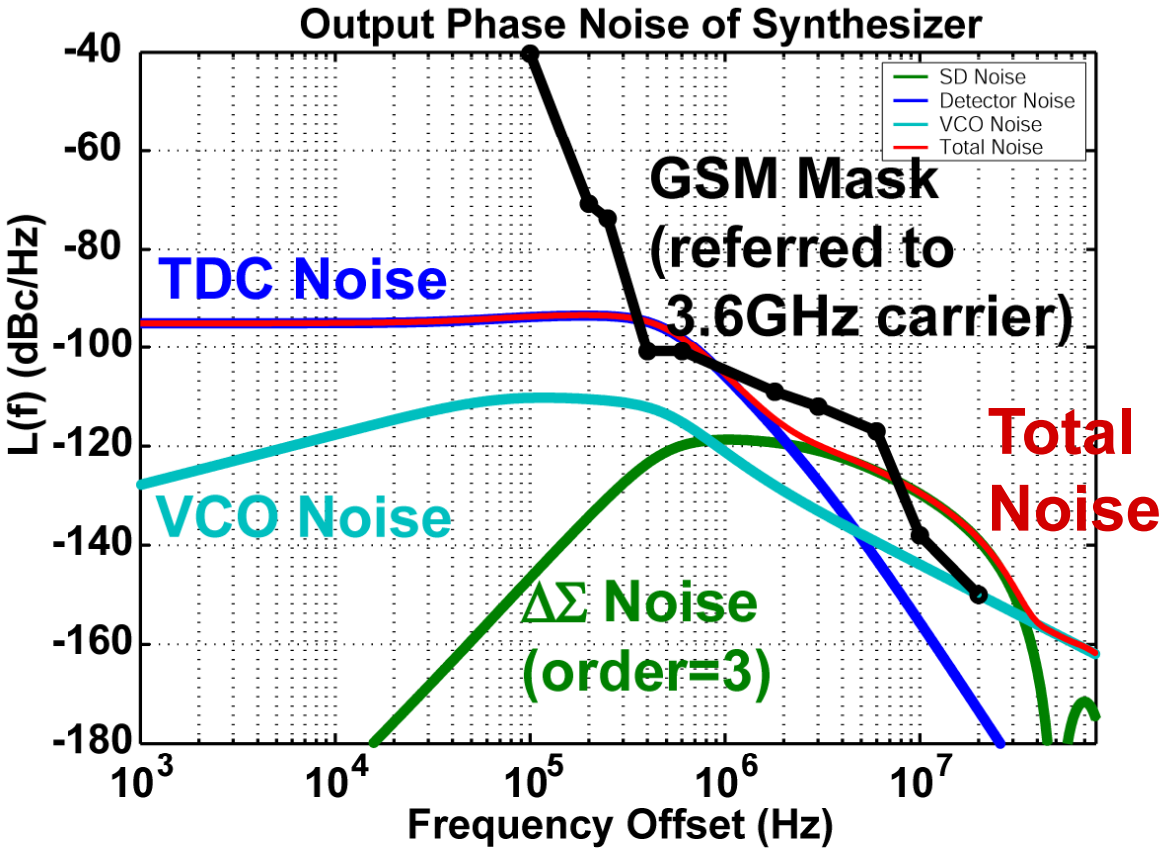
- **Assumptions:**
  - **TDC ΔT= 20ps**
  - **carrier freq. = 3.6GHz**
  - **reference freq. = 50MHz**
  - **PLL BW = 50kHz**
  - **3rd order ΔΣ**



- **VCO noise dominates performance everywhere …**
- **Don't need very high TDC resolution**
- **Δ–Σ fractional-N quantization noise is not an issue**

Examine Noise Performance: Wide-Bandwidth Case

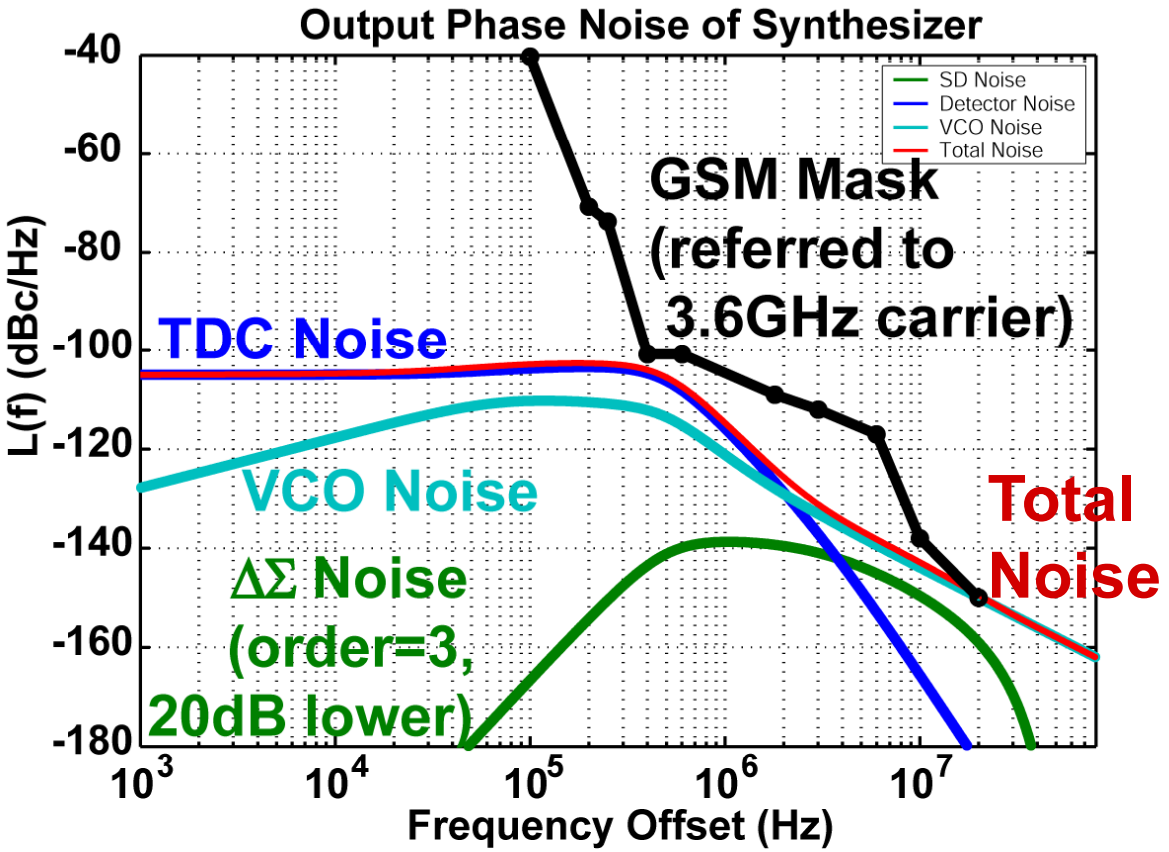
- **Assumptions:**
  - TDC ΔT= 20ps
  - carrier freq. = 3.6GHz
  - reference freq. = 50MHz
  - PLL BW = 500kHz
  - 3rd order $\Delta\Sigma$



- **Noise dominated by TDC at low frequencies**
- **Noise dominated by $\Delta\Sigma$ fractional-N noise at high frequencies**

To Meet High Performance Applications like GSM….

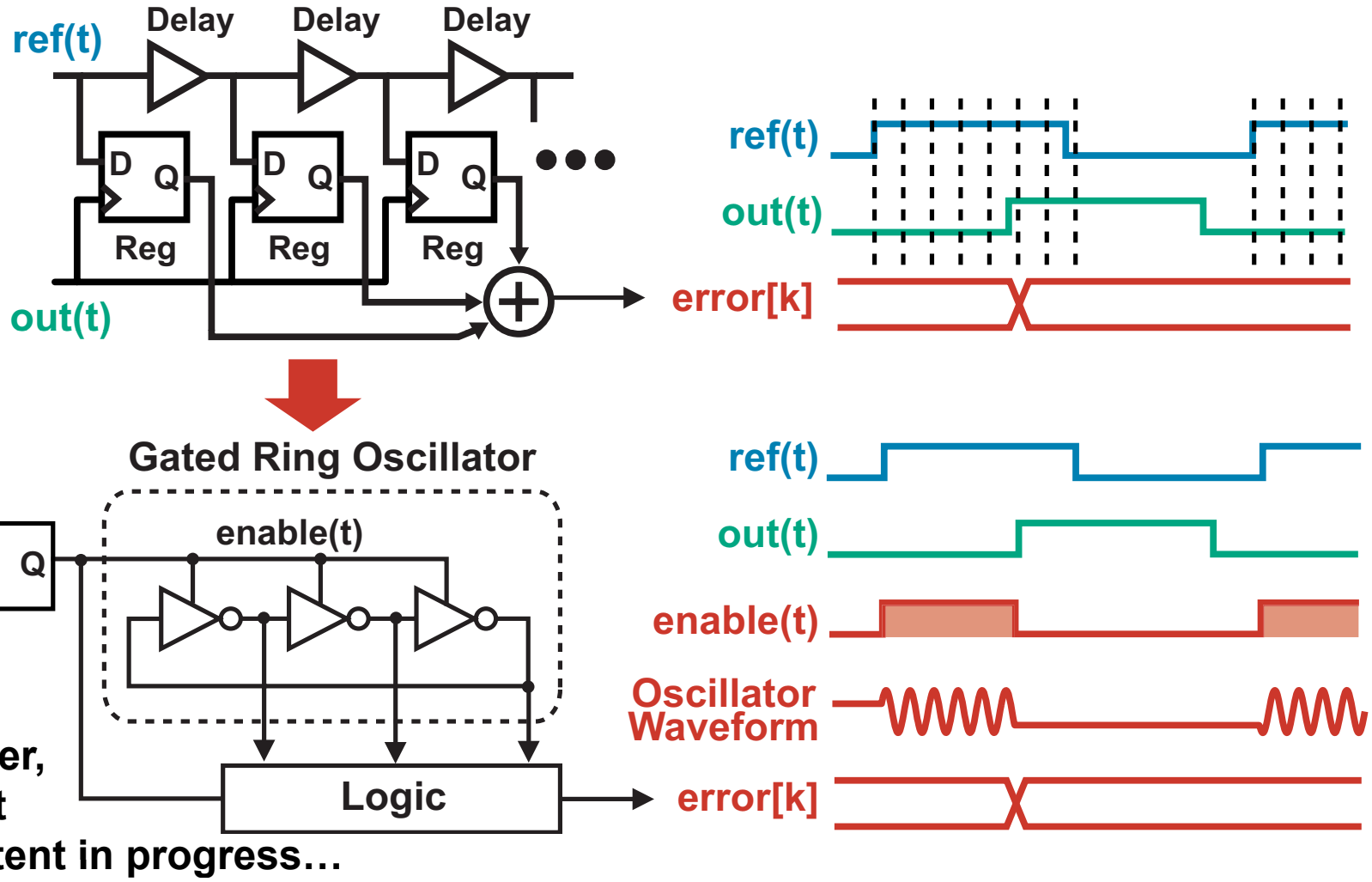
- **Assumptions:**
  - **TDC ΔT = 6ps**
  - **carrier freq. = 3.6GHz**
  - **reference freq. = 50MHz**
  - **PLL BW = 500kHz**
  - **3rd order ΔΣ (20dB lower)**



Need *6-ps* TDC resolution and *20dB* cancellation of Δ–Σ fractional-N noise to achieve 500kHz bandwidth

Can We Improve the Effective Resolution of Time-to-Digital Conversion?

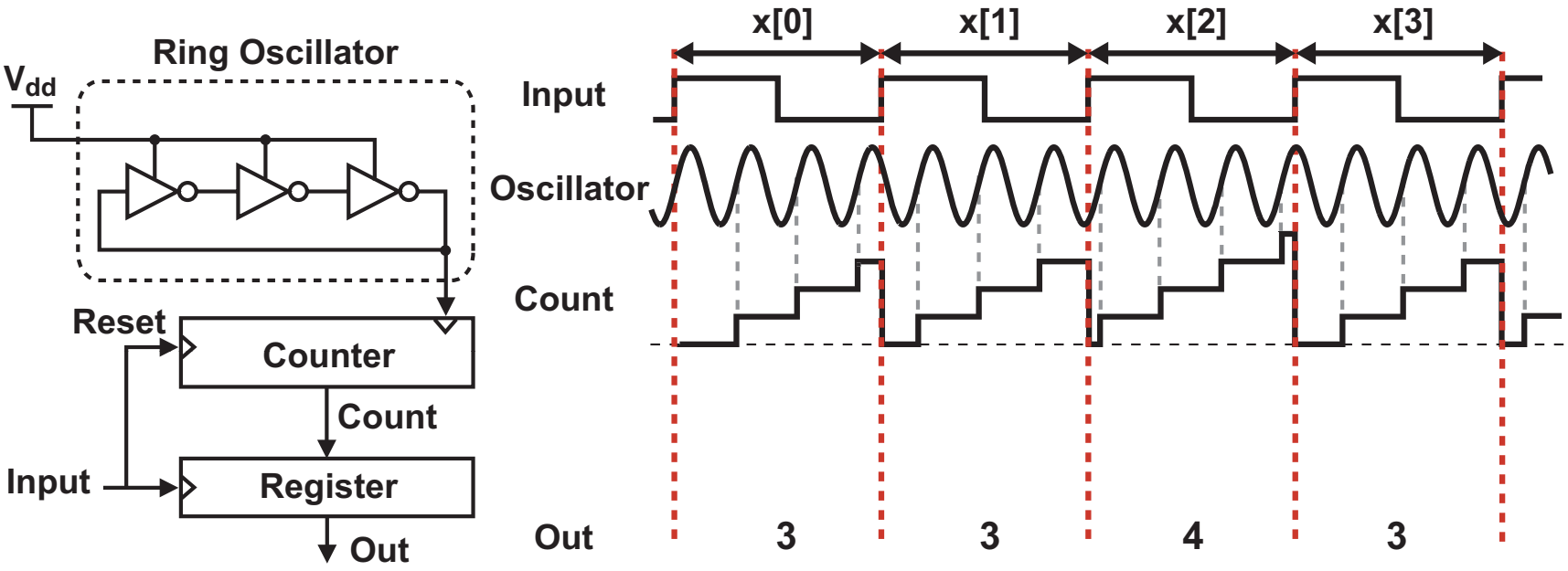
Proposed Approach: A Better Time-to-Digital Converter



Straayer, Perrott US Patent in progress…

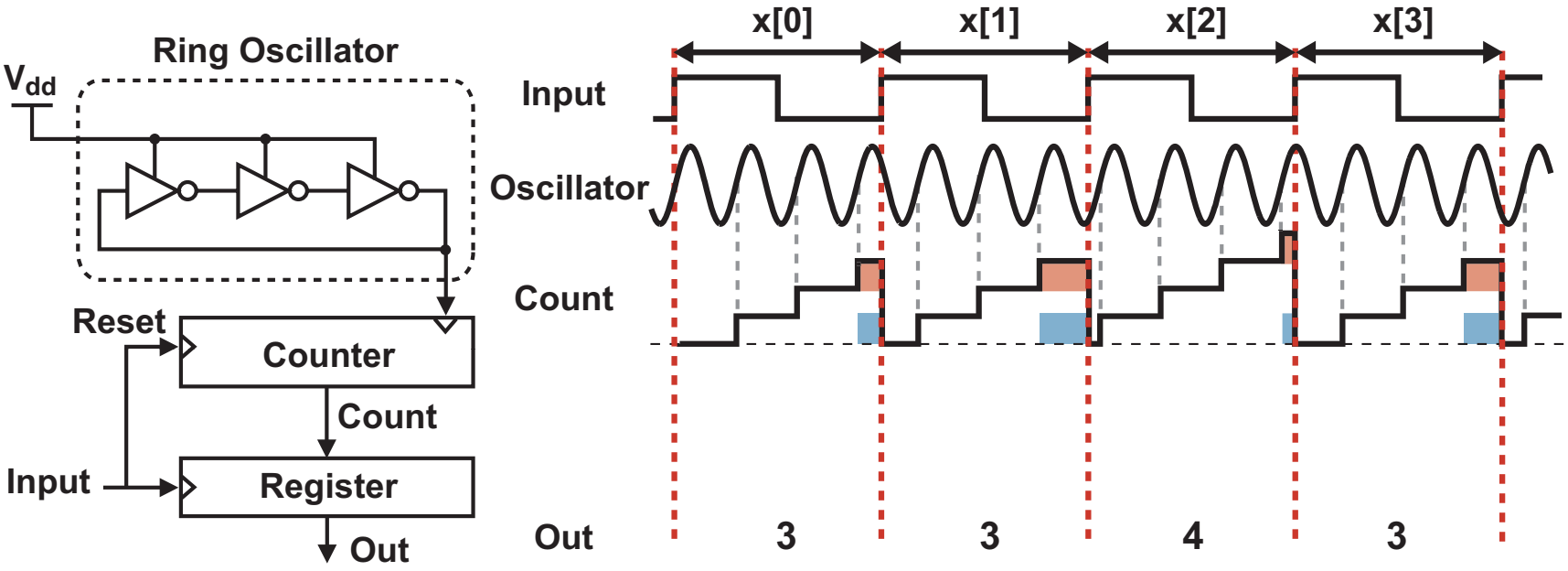
- This is a simplified view
  - We will need a few slides to properly explain this …

Consider Measurement of the Period of a Signal



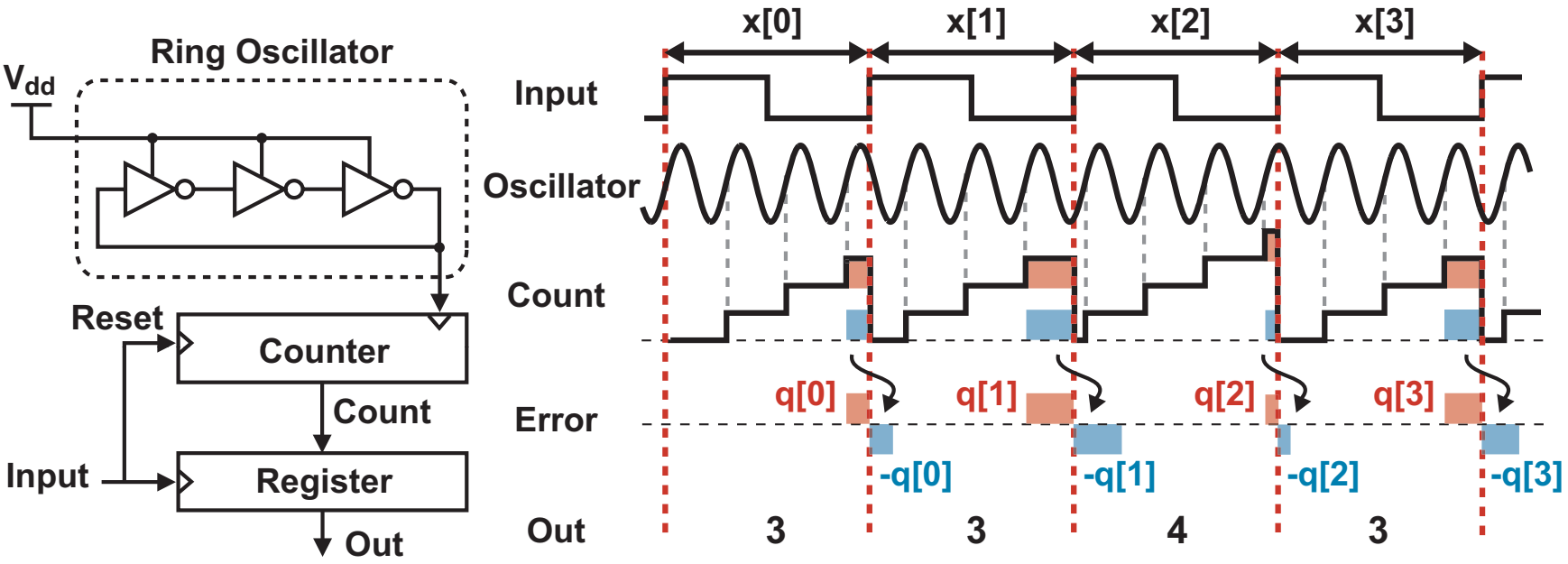
- Use digital logic to count number of oscillator cycles during each input period
  - Assume that oscillator period is much smaller than that of the input
- Note: output count per period is not consistent
  - Depends on starting phase of oscillator within a given measurement period

Examine Quantization Error in Measurements



- Quantization error varies according to starting phase of the oscillator within a given measurement period
  - Leads to *scrambling* of the quantization noise
- But there is something rather special about the scrambling action …

A Closer Examination of Quantization Noise



- **Calculate impact of quantization noise in time:**

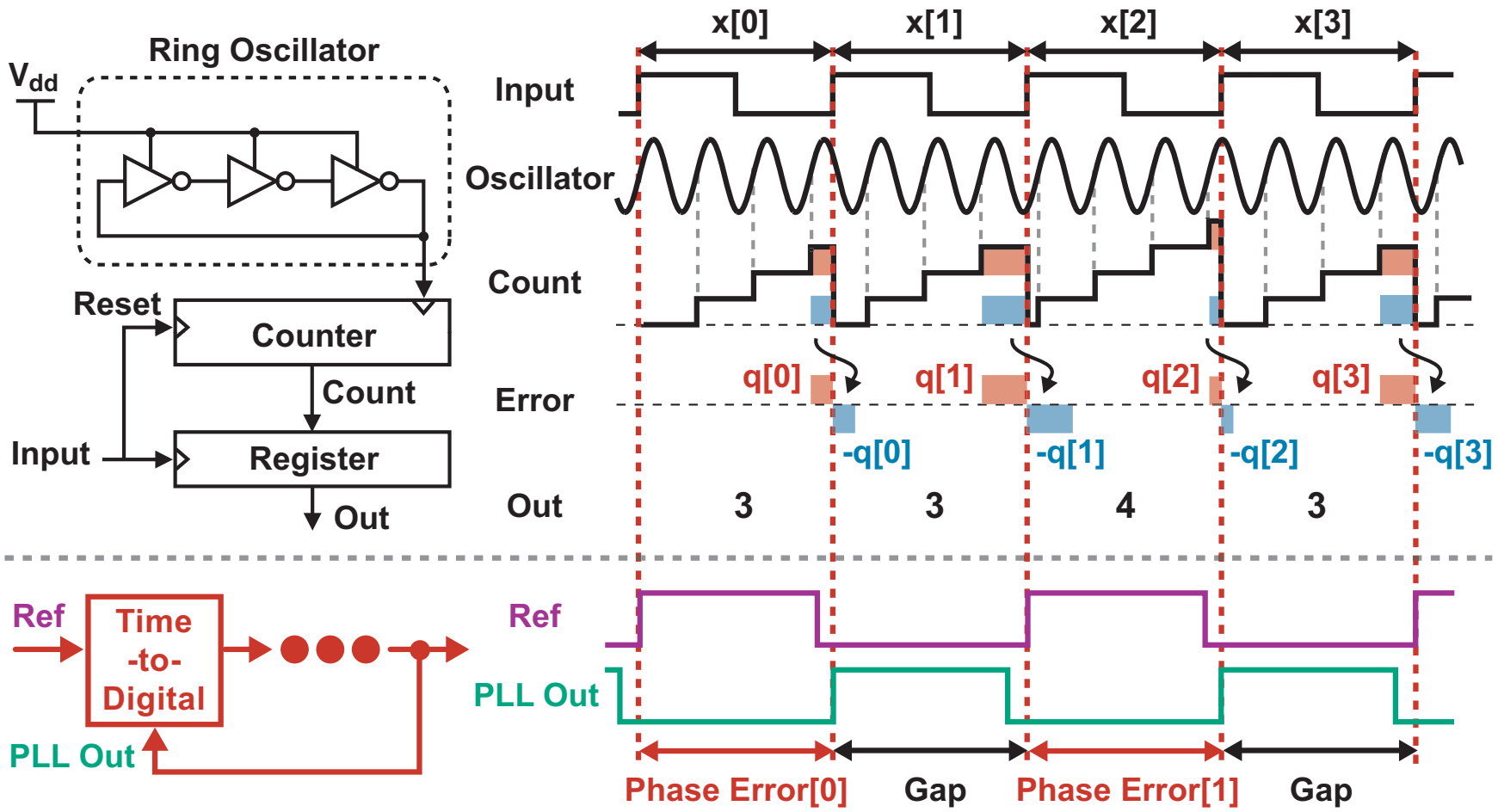
$$\begin{aligned} out[k] &= x[k] + error[k] \\ &= x[k] + q[k] - q[k-1] \end{aligned}$$

- **Take Z-transform:**

$$Out(z) = X(z) + (1 - z^{-1})Q(z)$$

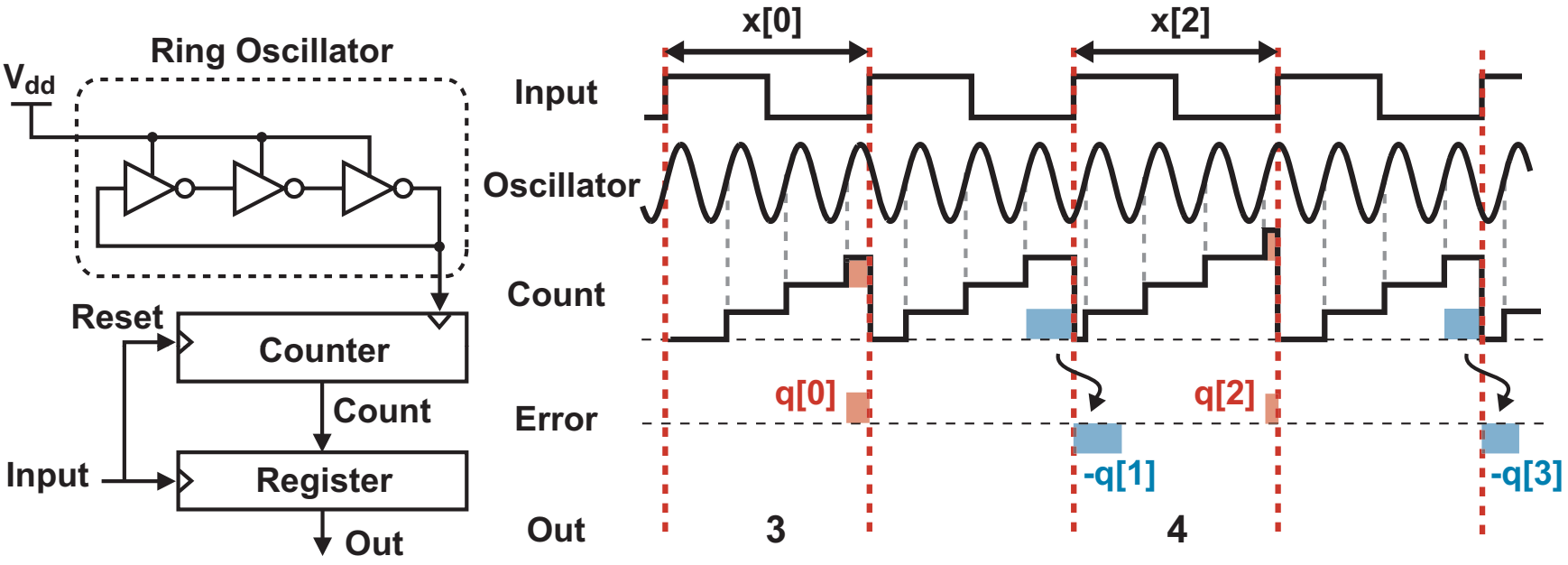
Quantization noise is first order noise shaped!

Relating to Phase Error Between Two Signals



- **Measurement of phase error *between two signals* requires *gaps* between measurements**
  - **What is the implication of such gaps?**

The Impact of Non-Consecutive Measurements

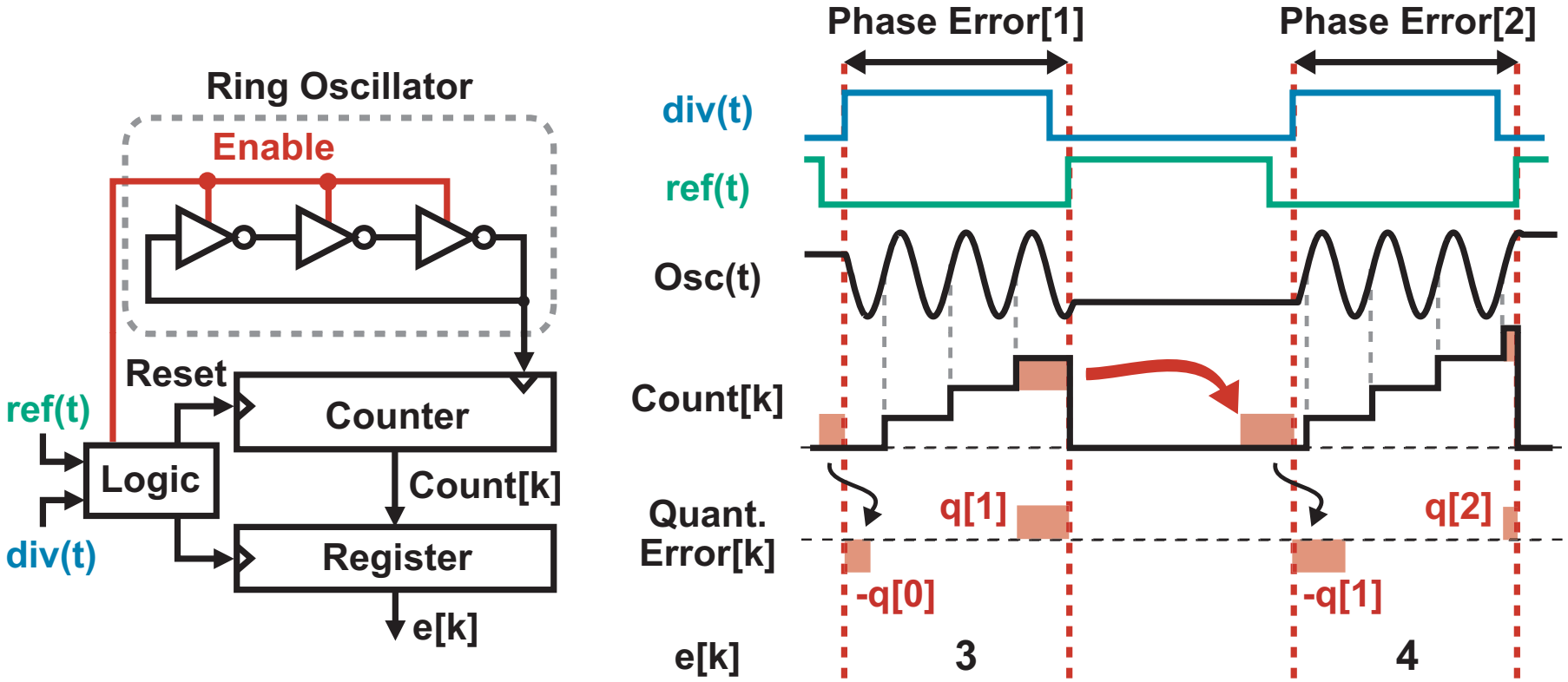


- Consider measuring input period every *other* cycle
  - Analogous to phase measurement *between* two signals
- Key observation:
  - Quantization noise is no longer first order noise shaped!

Is there a way to restore noise shaping?

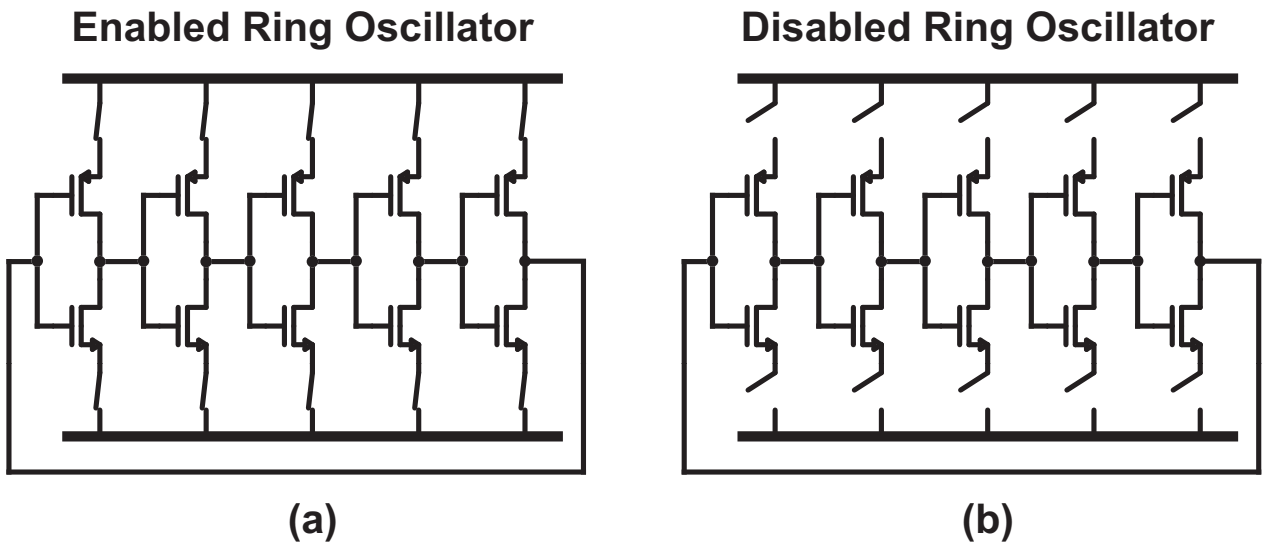
Proposed GRO TDC Structure

A Gated Ring Oscillator (GRO) TDC

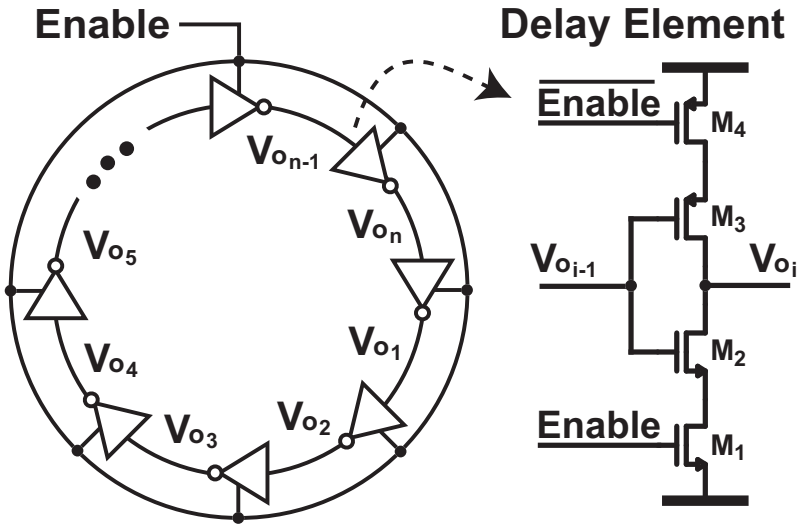


- Enable ring oscillator only during measurement intervals
  - Hold the state of the oscillator between measurements
- Quantization error becomes first order noise shaped!
  - *e[k] = Phase Error[k] + q[k] – q[k-1]*
  - Averaging dramatically improves resolution!

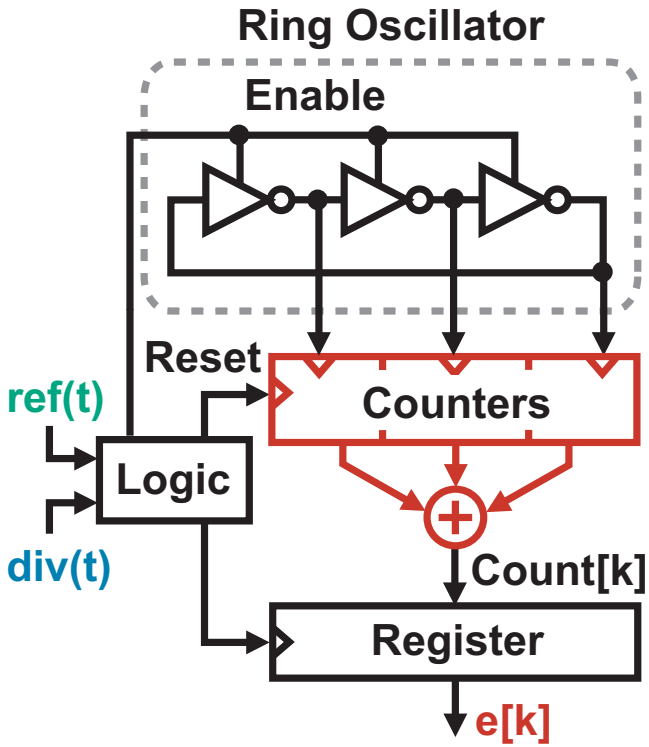
Simple gated ring oscillator inverter-based core



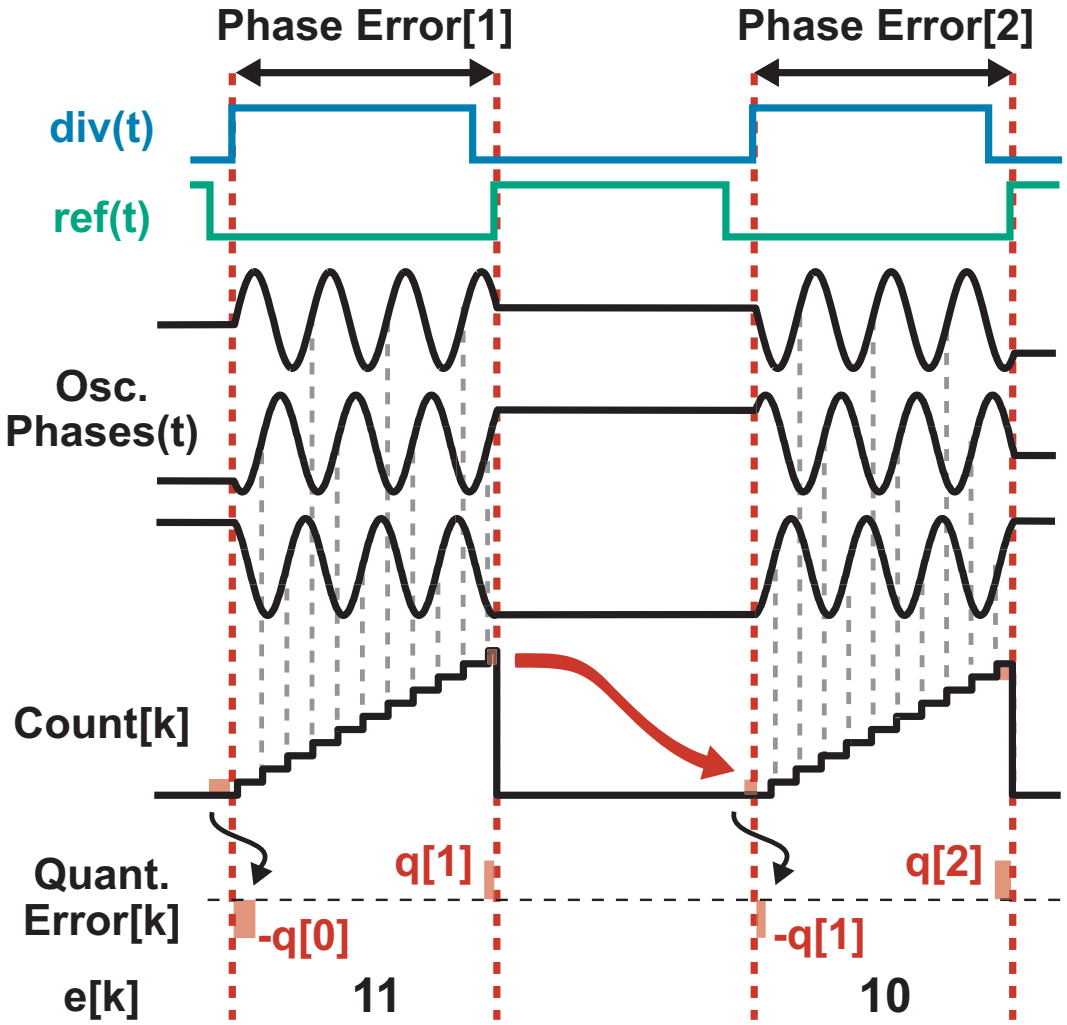
Gate the oscillator by switching the inverter cores to the power supply



Improve Resolution By Using All Oscillator Phases

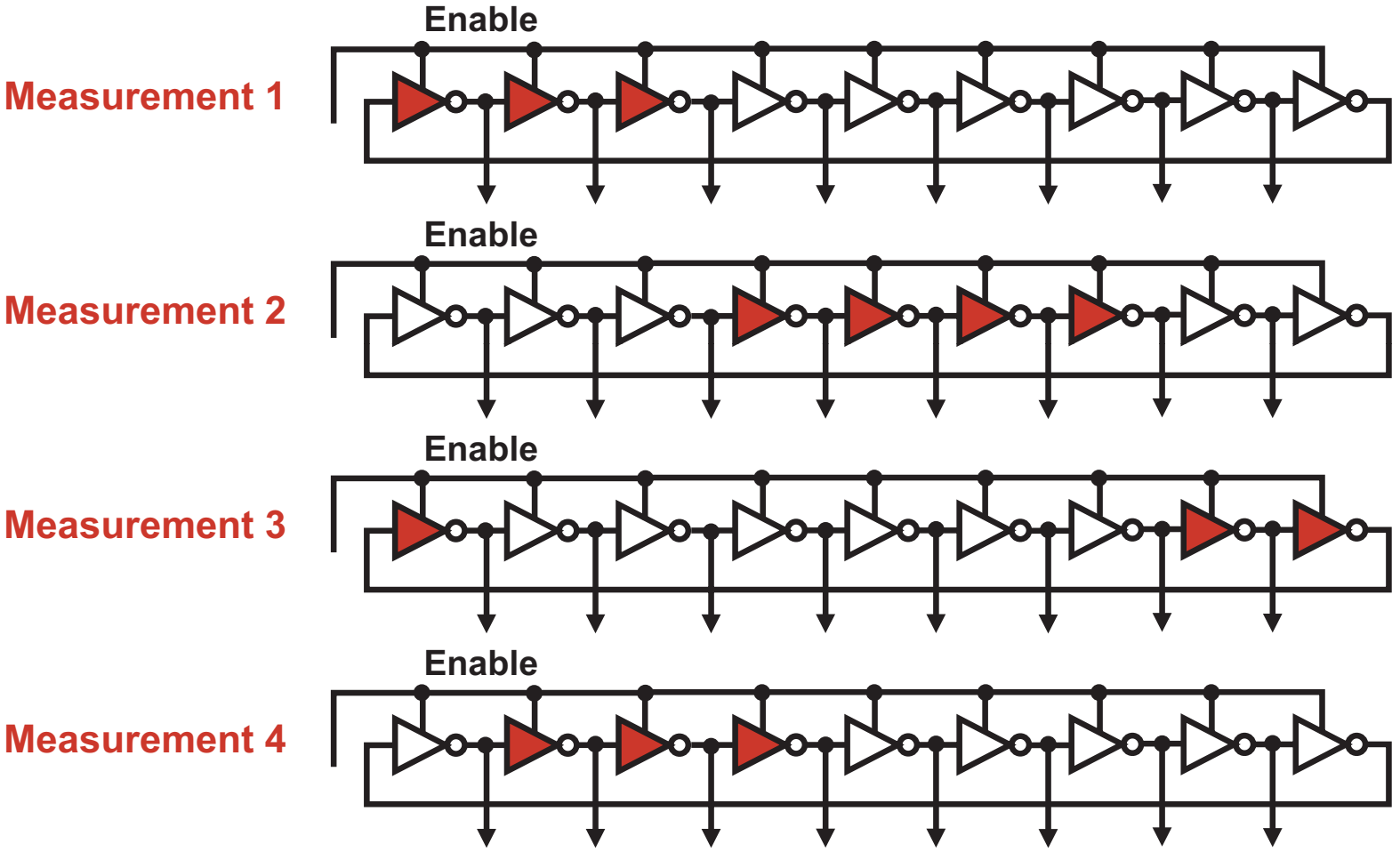


Helal, Straayer, Wei,
Perrott VLSI 2007



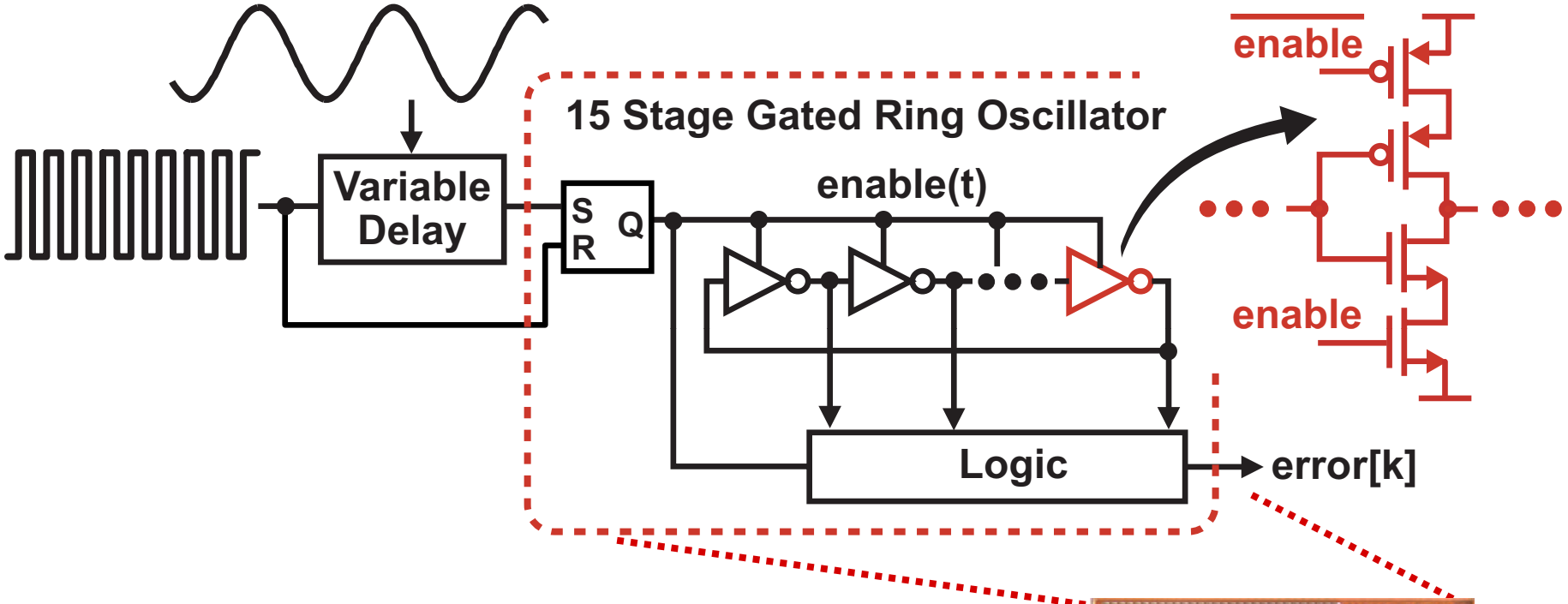
- Raw resolution is set by inverter delay
- Effective resolution is dramatically improved by averaging

GRO TDC Also Shapes Delay Mismatch

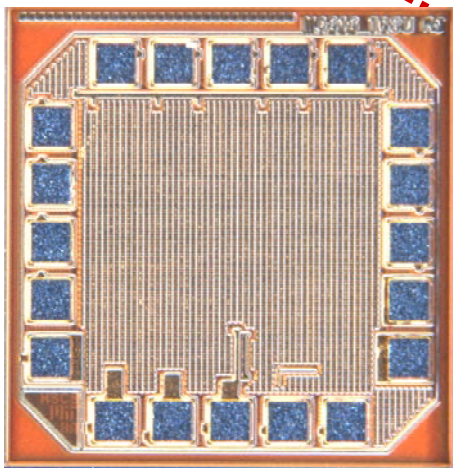


- Barrel shifting occurs through delay elements across different measurements
  - Mismatch between delay elements is first order shaped!

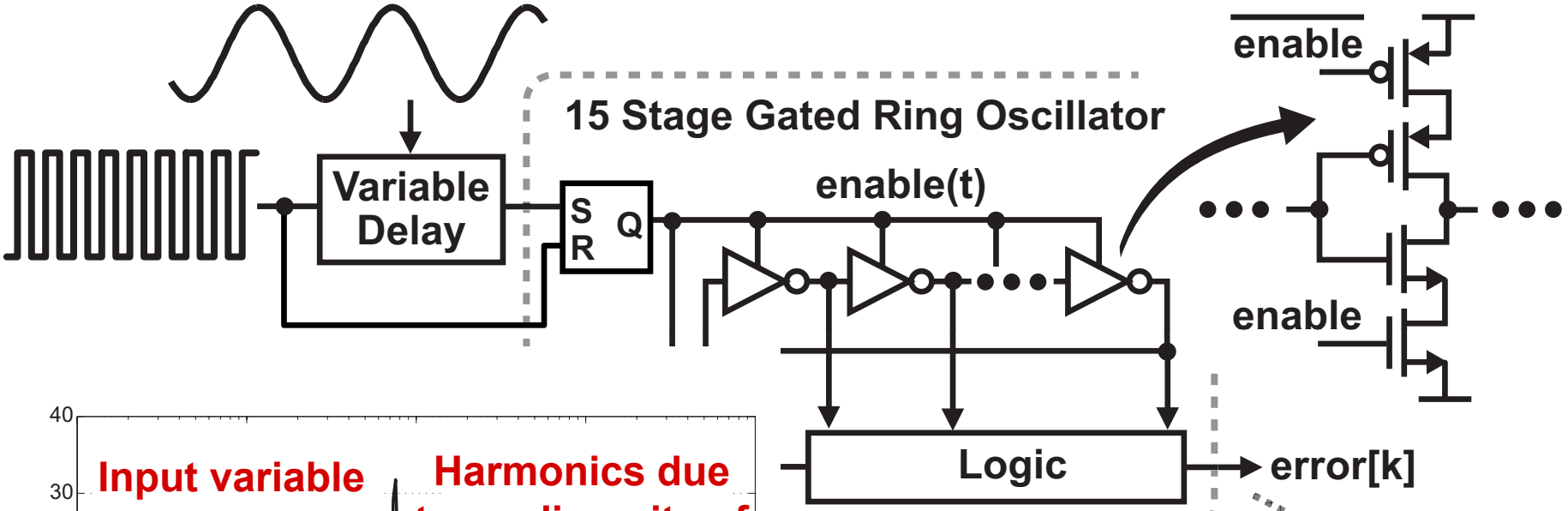
First Generation GRO Prototype

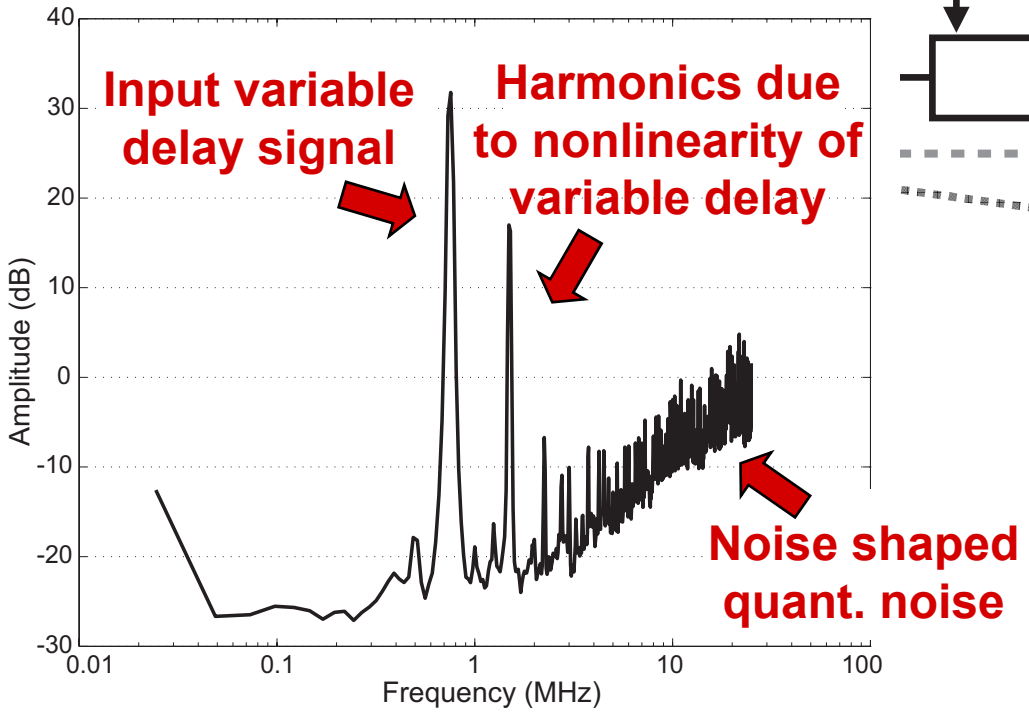


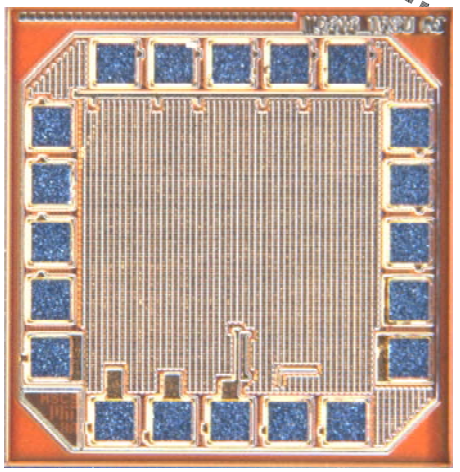
- GRO implemented as a custom 0.13u CMOS IC
- External setup consists of signal source and variable delay
  - Test issue: variable delay is nonlinear



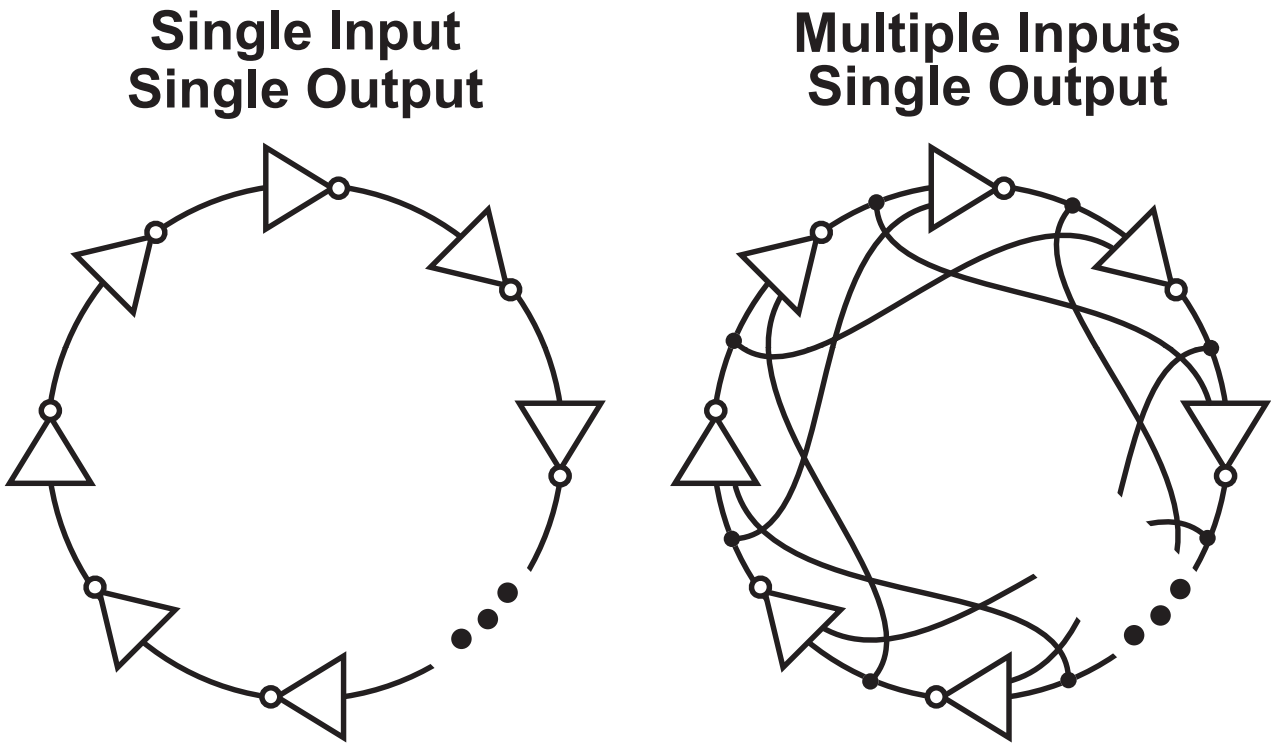
Measured GRO Results Confirm Noise Shaping





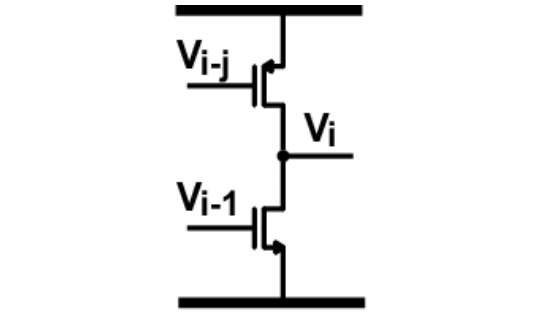


Next Generation GRO: Multi-path oscillator concept



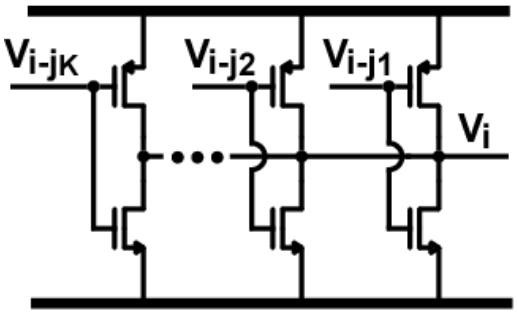
- Use multiple inputs for each delay element instead of one
- Allow each stage to optimally begin its transition based on information from the entire GRO phase state
- Key design issue is to ensure primary mode of oscillation

Multi-path inverter core



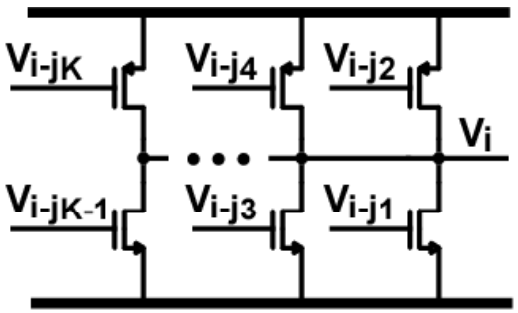
(a) Asymmetrically skewed inverter

Lee, Kim, Lee
JSSC 1997

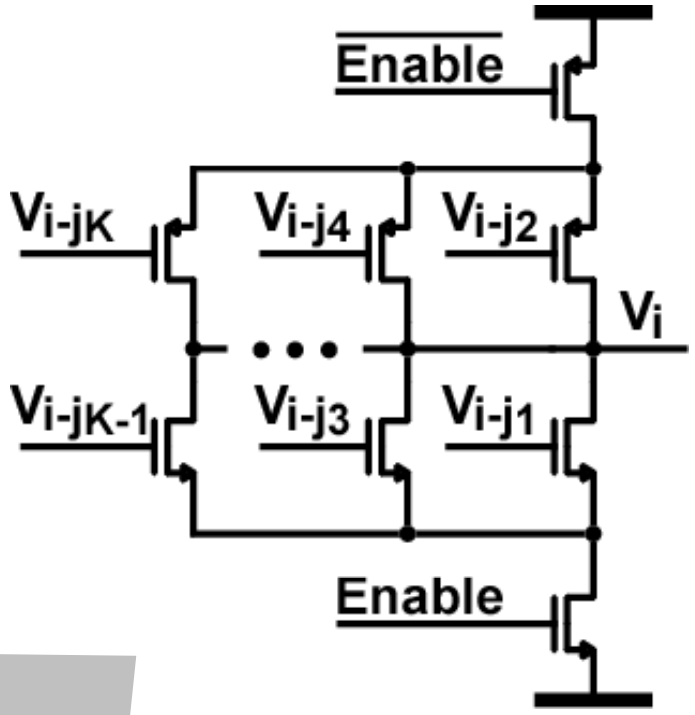


(b) Multiple skewed inverters

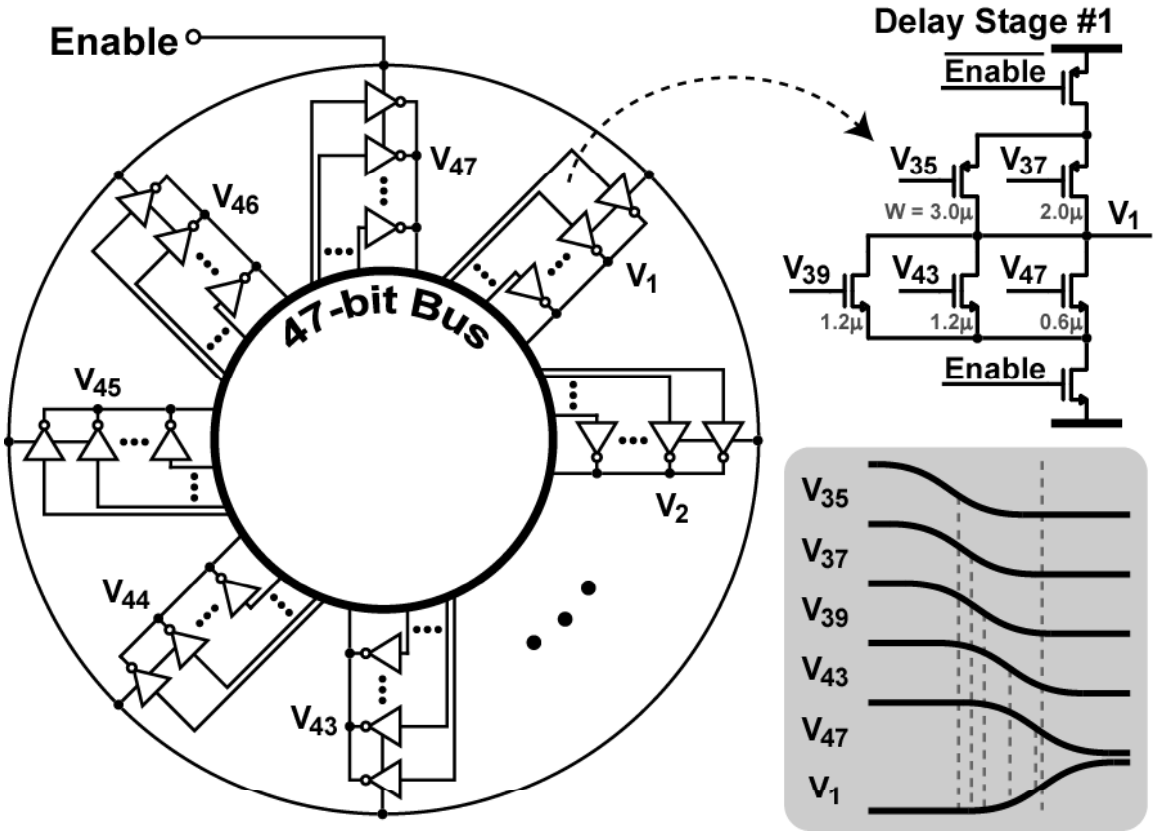
Mohan, et. al.,
CICC 2005



(c) Unrestricted connections



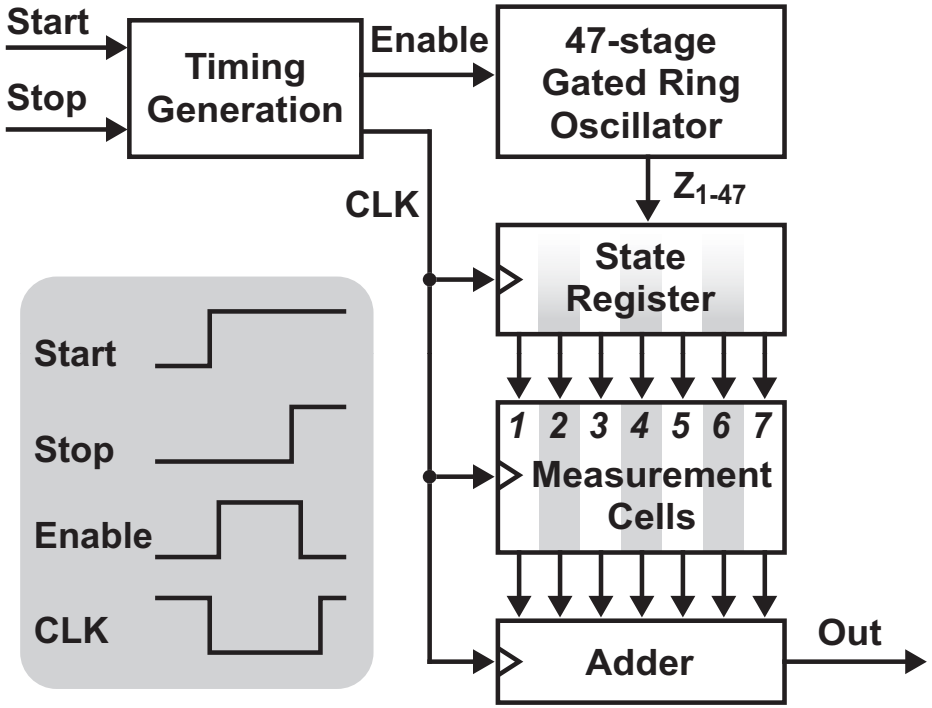
Proposed Multi-Path Gated Ring Oscillator TDC

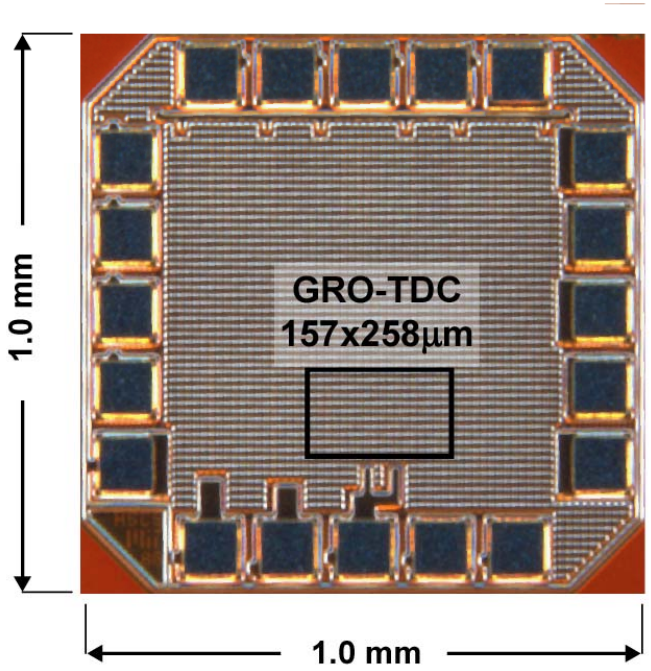


Hsu, Straayer, Perrott
ISSCC 2008

- Oscillation frequency near 2GHz with 47 stages…
- Reduces effective delay per stage by a factor of 5-6!
- Represents a factor of 2-3 improvement compared to previous multi-path oscillators

Prototype 0.13μm CMOS Multi-Path GRO-TDC

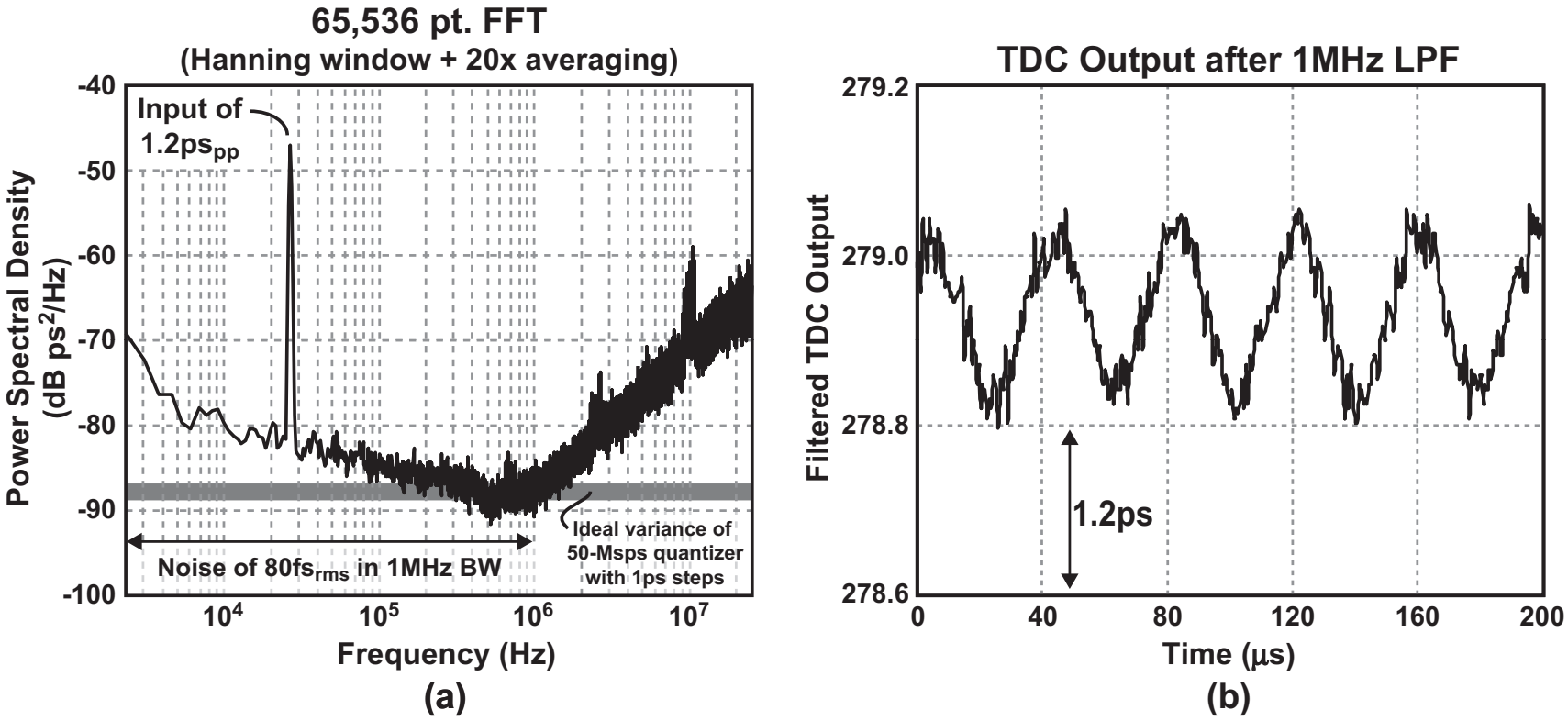




Straayer, Perrott
VLSI 2008

- **Two implemented versions:**
  - **8-bit, 500Msps**
  - **11-bit, 100Msps version**
- **2-21mW power consumption depending on input duty cycle**

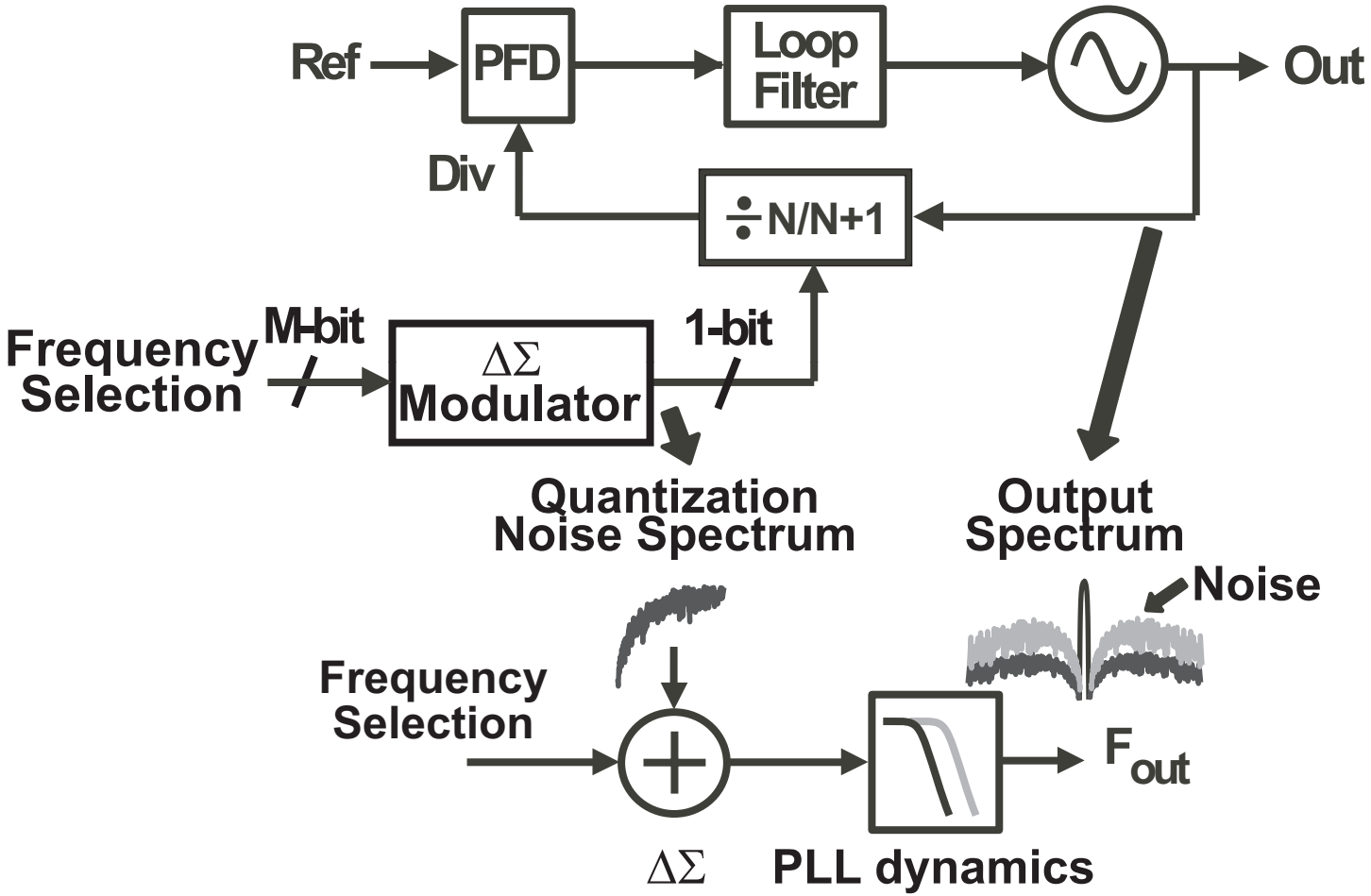
Measured noise-shaping of multi-path GRO



- Data collected at 50Msps
- More than 20dB of noise-shaping benefit
- 80fs$_{rms}$ integrated error from 2kHz-1MHz
- Floor primarily limited by 1/f noise (up to 0.5-1MHz)

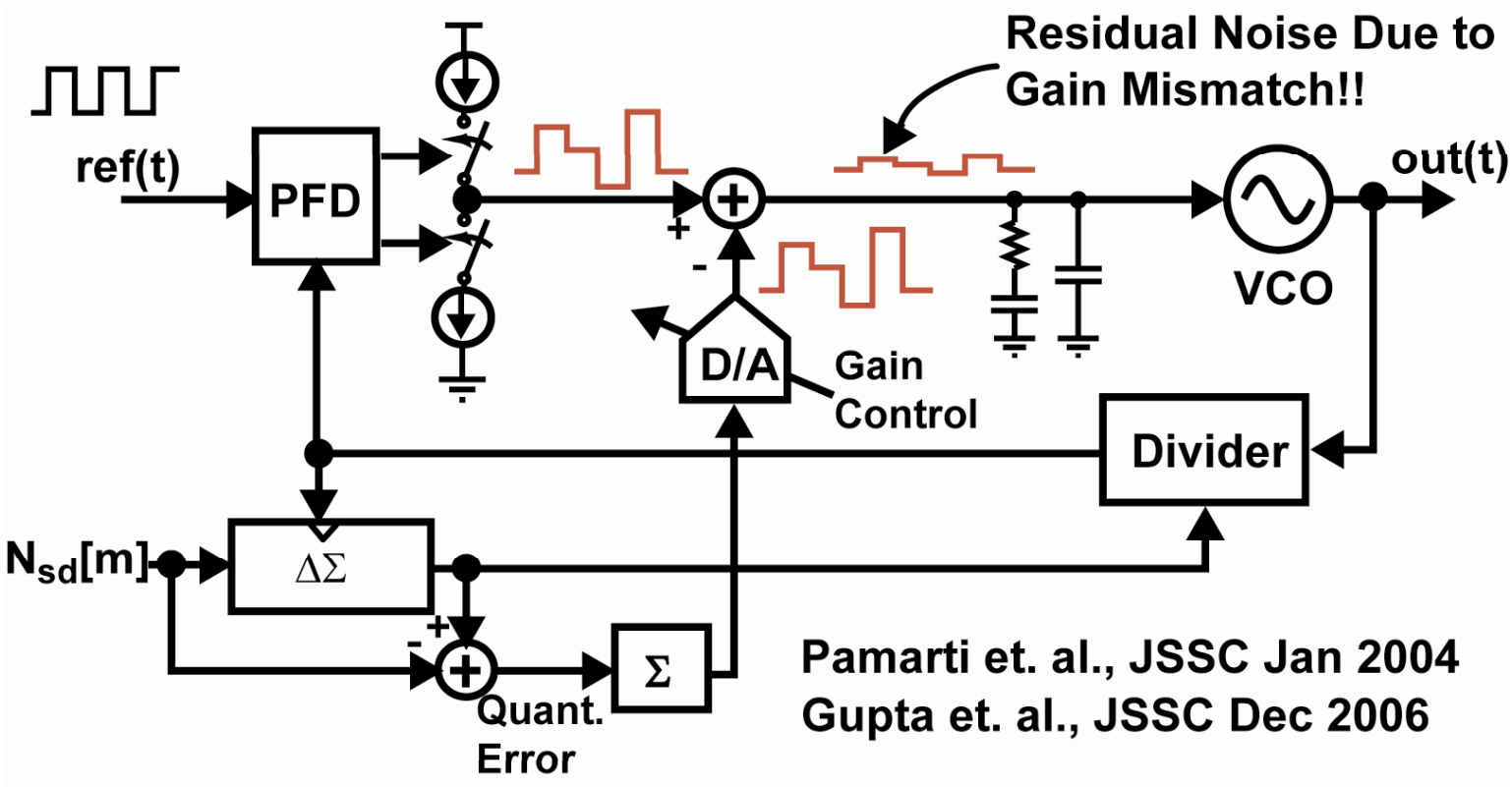
Can We Reduce Sigma-Delta Quantization Noise Caused by Divider Dithering?

The Nature of the Quantization Noise Problem



- Increasing PLL bandwidth increases impact of ΔΣ fractional-N noise
  - Cancellation offers a way out!

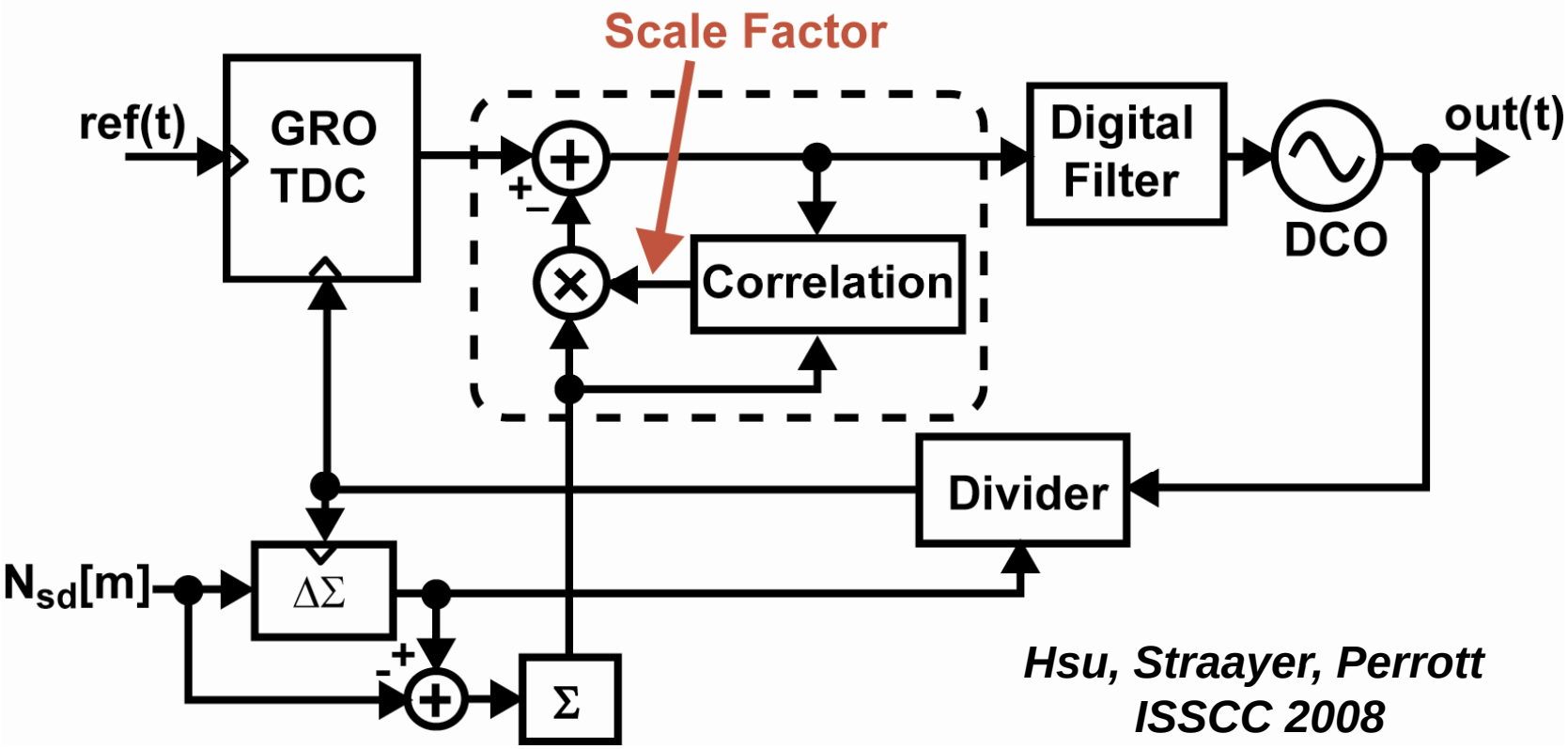
Previous Analog Quantization Noise Cancellation



- Phase error due to ΔΣ is predicted by accumulating ΔΣ quantization error
- Gain matching between PFD and D/A must be precise

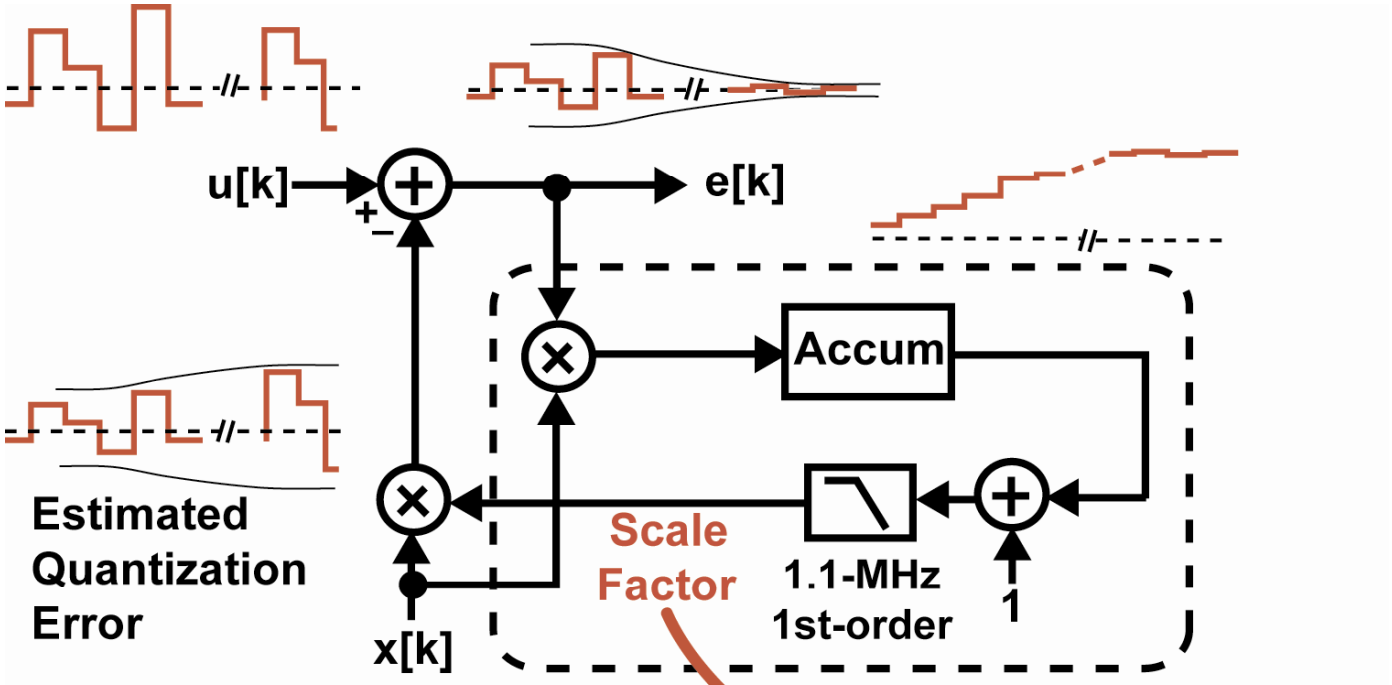
Matching in *analog* domain limits performance

Proposed All-digital Quantization Noise Cancellation

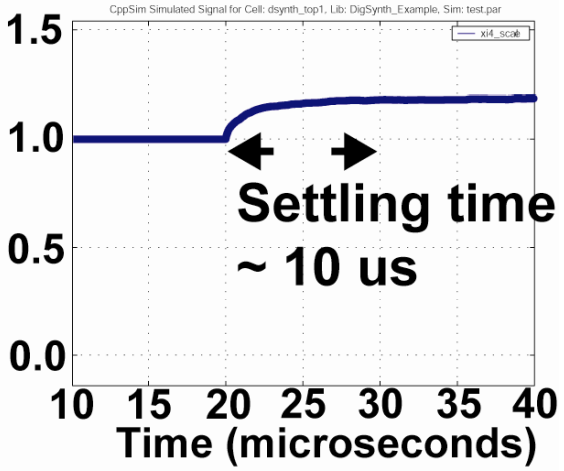


- **Scale factor determined by simple digital correlation**
- **Analog non-idealities such as DC offset are completely eliminated**

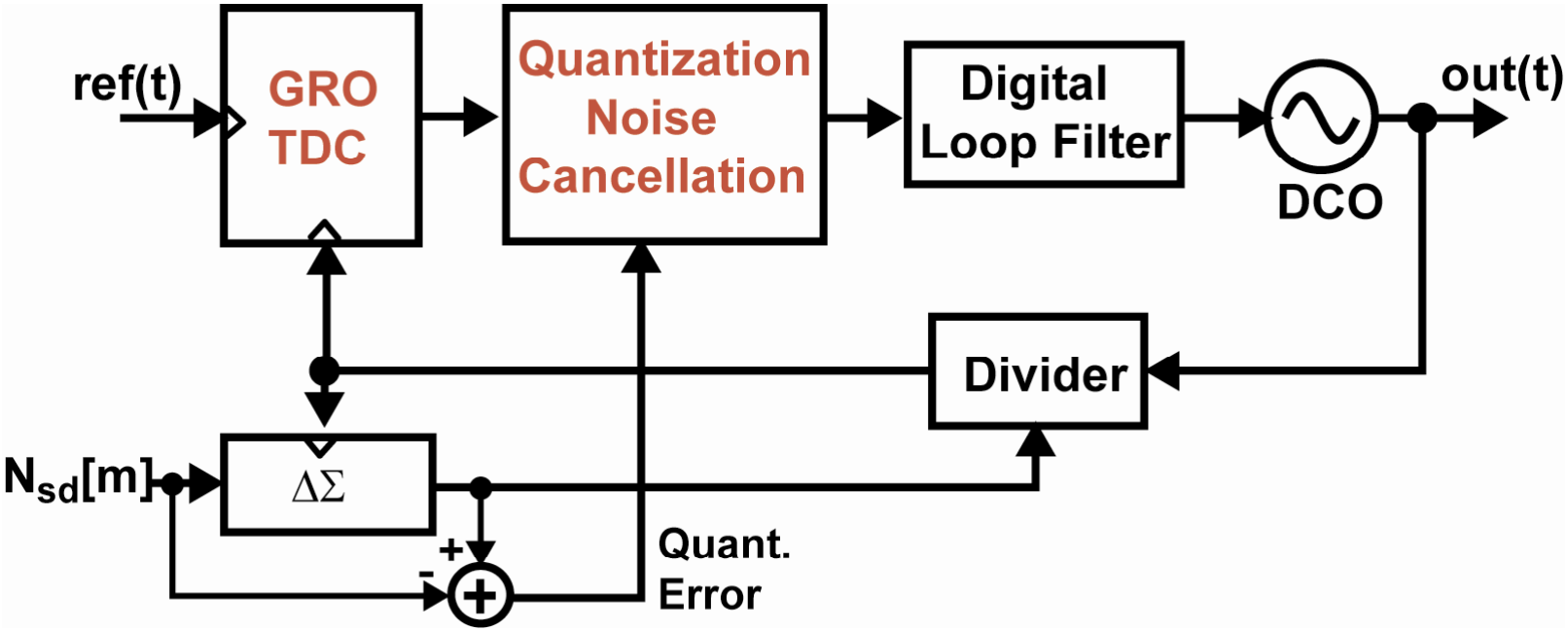
Details of Proposed Quantization Noise Cancellation



- Correlator out is accumulated and filtered to achieve scale factor
  - Settling time chosen to be around 10 us
- See *analog* version of this technique in *Swaminathan et.al., ISSCC 2007*

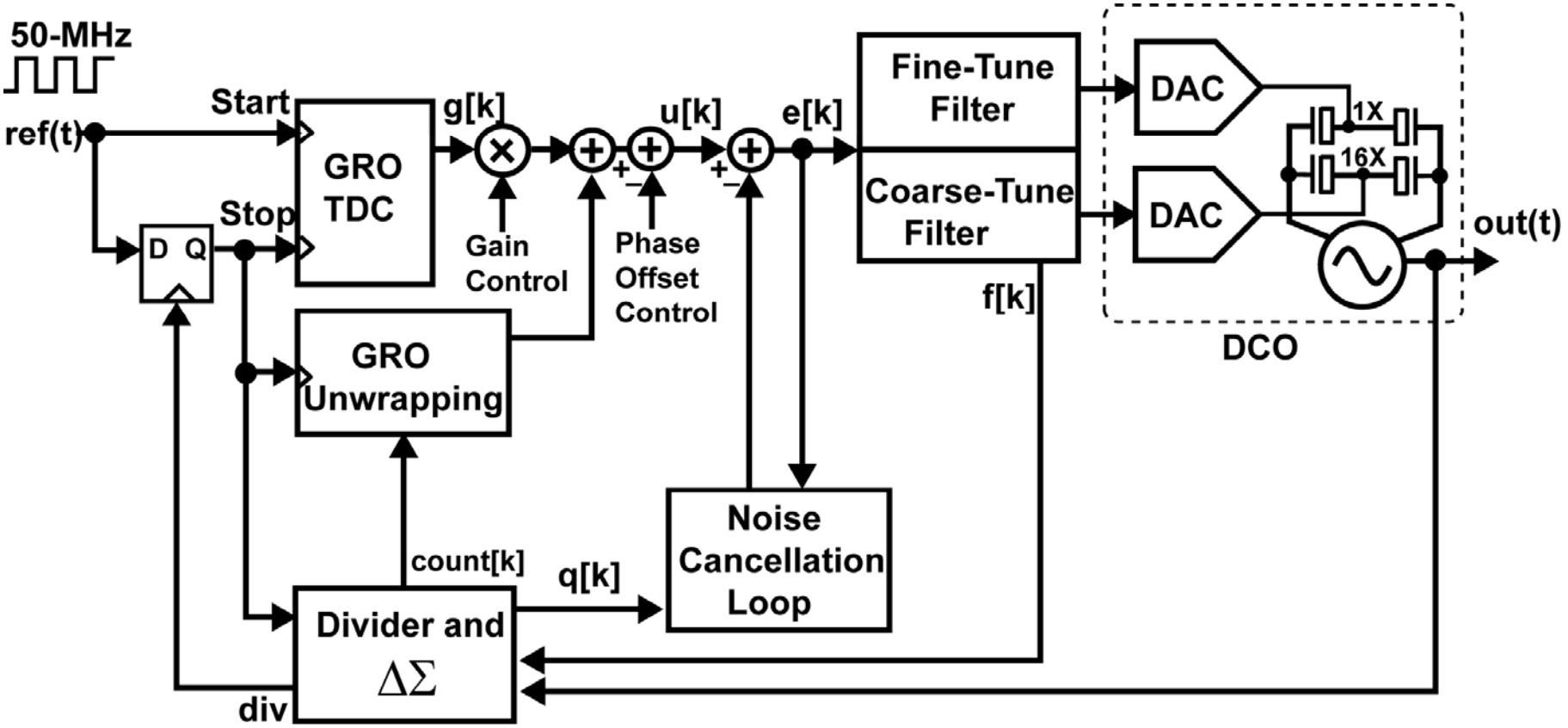


Proposed Digital Wide BW Synthesizer



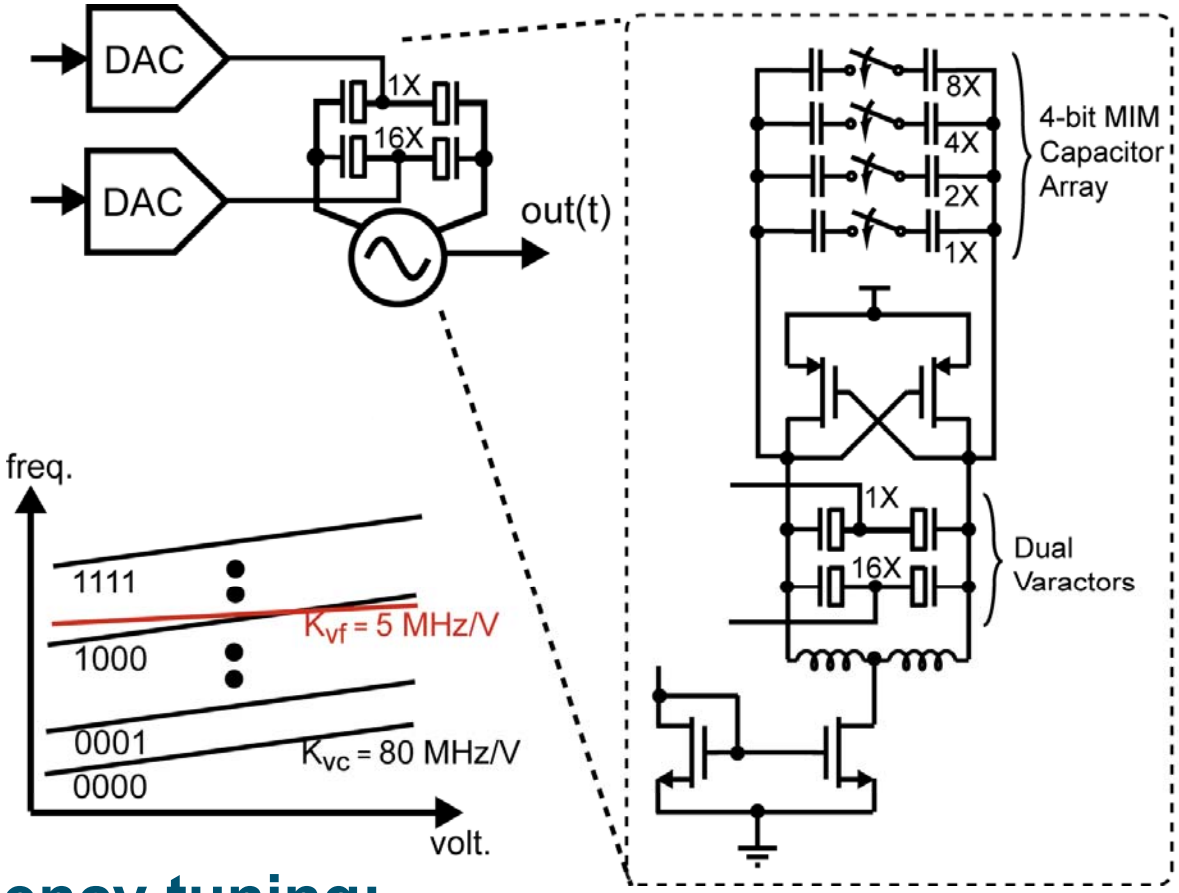
- *Gated-ring-oscillator (GRO) TDC* achieves low in-band noise
- *All-digital quantization noise cancellation* achieves low out-of-band noise
- Design goals:
  - 3.6-GHz carrier, 500-kHz bandwidth
  - <-100dBc/Hz in-band, <-150 dBc/Hz at 20 MHz offset

Overall Synthesizer Architecture



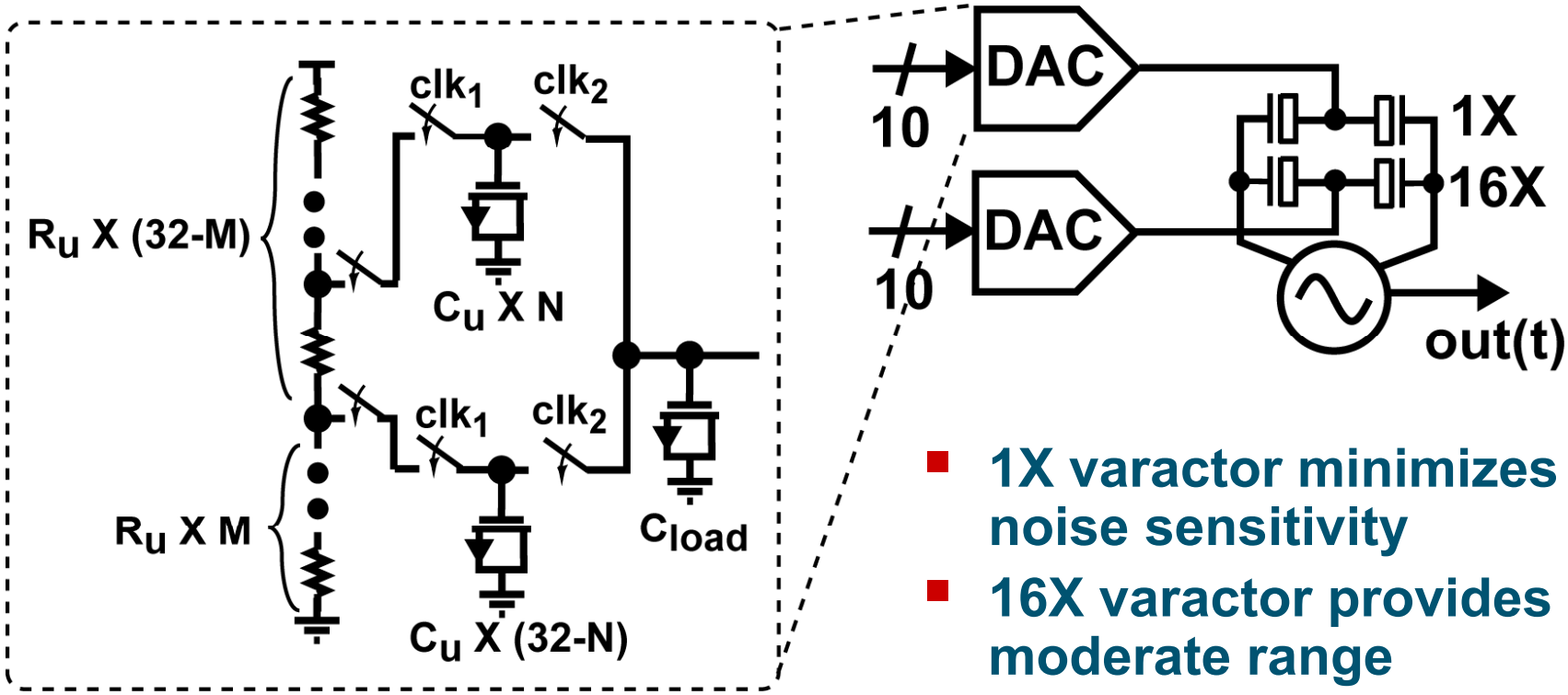
Note: Detailed behavioral simulation model available at http://www.cppsim.com

Dual-Port LC VCO



- **Frequency tuning:**
  - **Use a small 1X varactor to minimize noise sensitivity**
  - **Use another 16X varactor to provide moderate range**
  - **Use a four-bit capacitor array to achieve 3.3-4.1 GHz range**

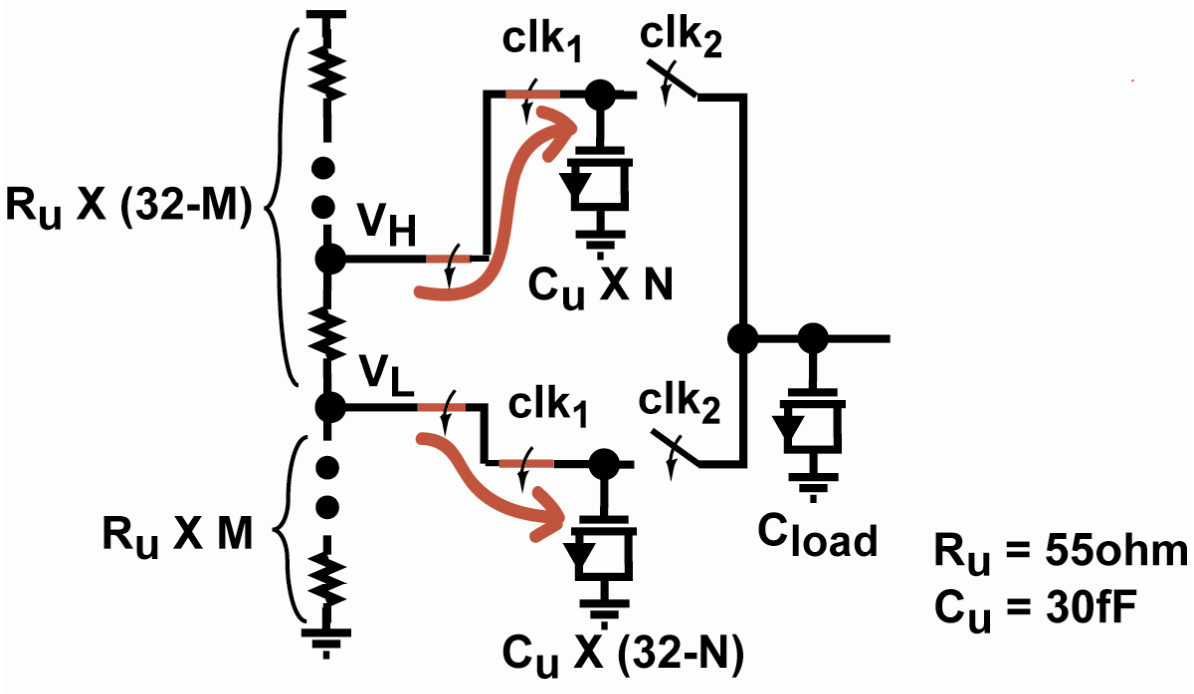
Digitally-Controlled Oscillator with Passive DAC



- 1X varactor minimizes noise sensitivity
- 16X varactor provides moderate range
- A four-bit capacitor array covers 3.3-4.1GHz

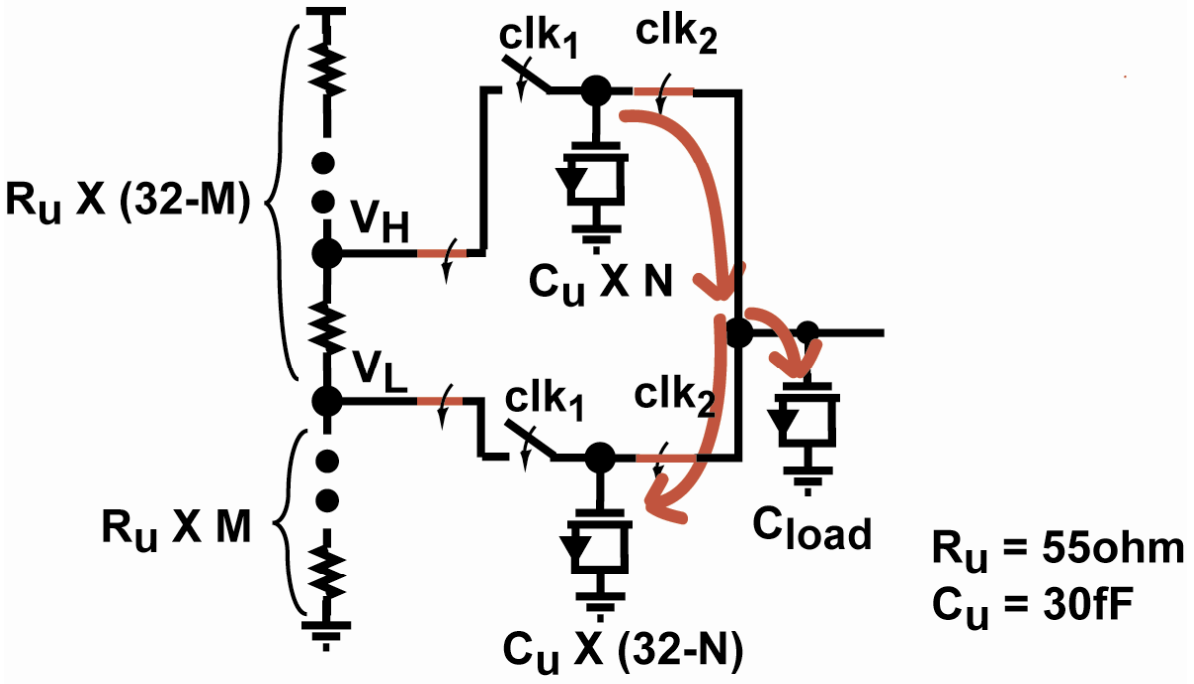
- Goals of 10-bit DAC
  - Monotonic
  - Minimal active circuitry and no transistor bias currents
  - Full-supply output range

Operation of 10-bit Passive DAC (Step 1)



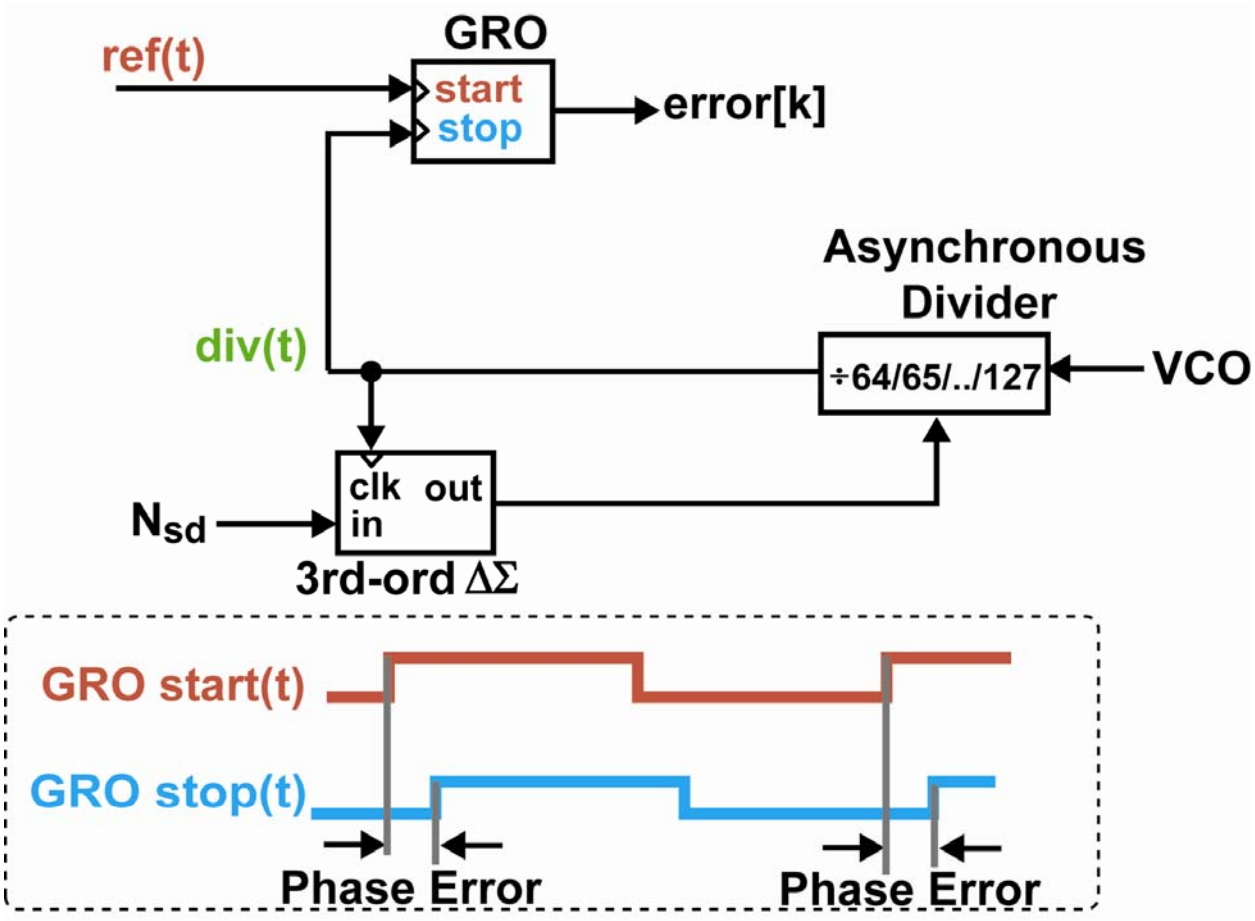
- **5-bit resistor ladder; 5-bit switch-capacitor array**
- **Step 1: *Capacitors Charged***
  - **Resistor ladder forms $V_L = M/32 \cdot V_{DD}$ and $V_H = (M+1)/32 \cdot V_{DD}$, where M ranges from 0 to 31**
  - **N unit capacitors charged to V_H, and (32-N) unit capacitors charged to V_L**

Operation of 10-bit Passive DAC (Step 2)



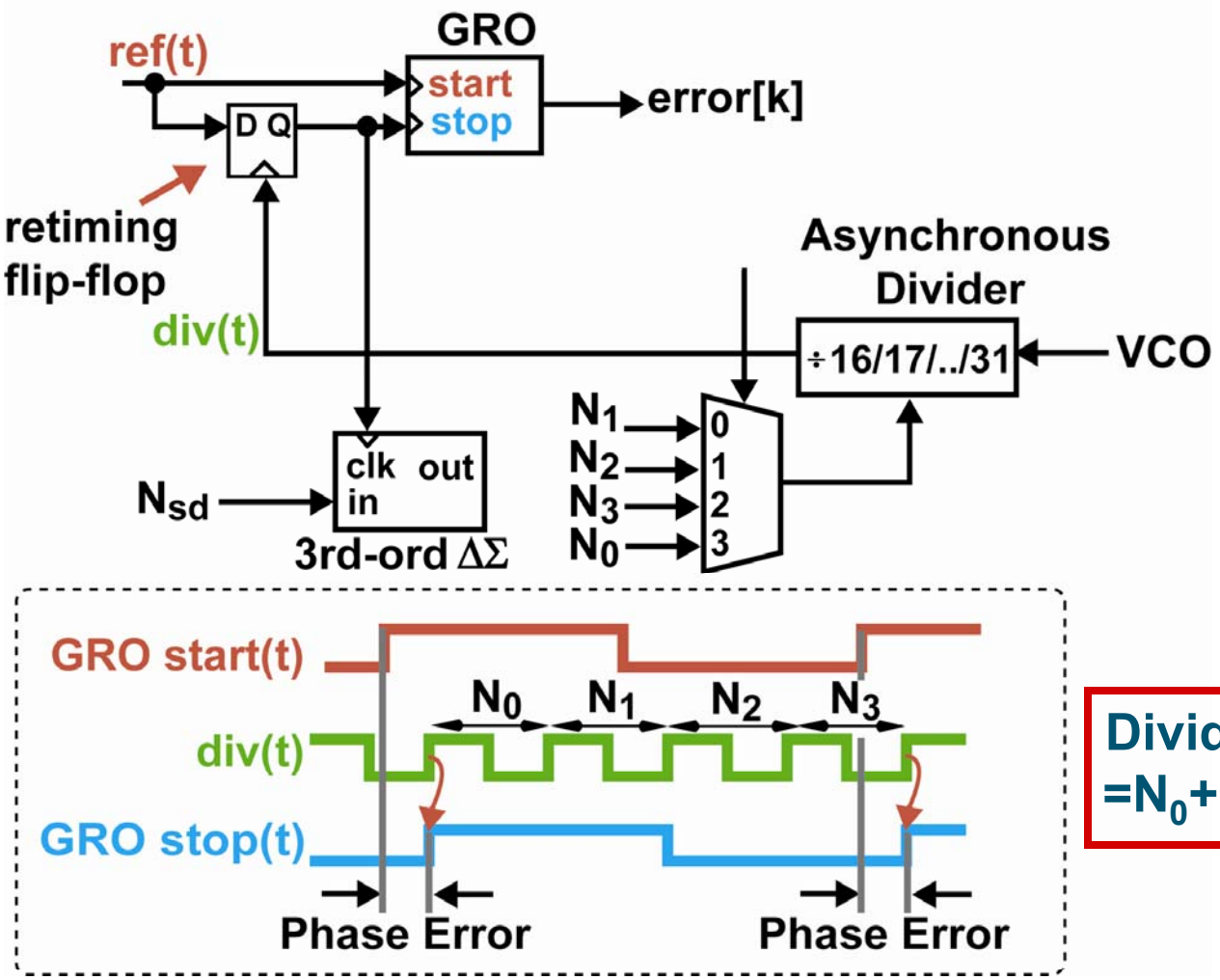
- **Step 2:** ***Disconnect Capacitors from Resistors, Then Connect Together***
  - **Achieves DAC output with first-order filtering**
  - **Bandwidth = 32• C_u/(2π•C_{load})•50MHz**
    - Determined by capacitor ratio
    - Easily changed by using different C_{load}

Now Let's Examine Divider …



- **Issues:**
  - **GRO range must span entire reference period during initial lock-in**

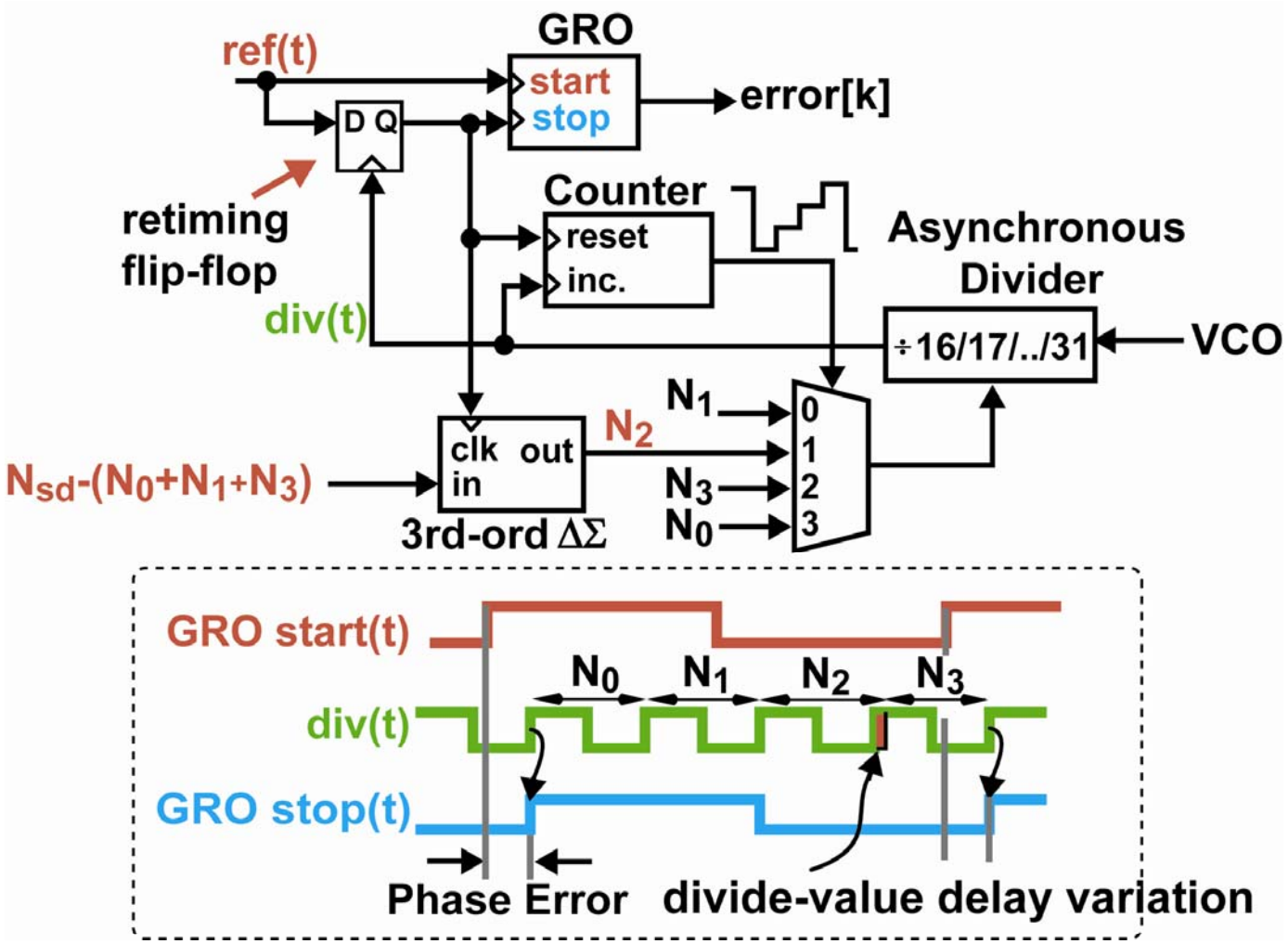
Proposed Divider Structure



Divide value
$=N_0+N_1+N_2+N_3$

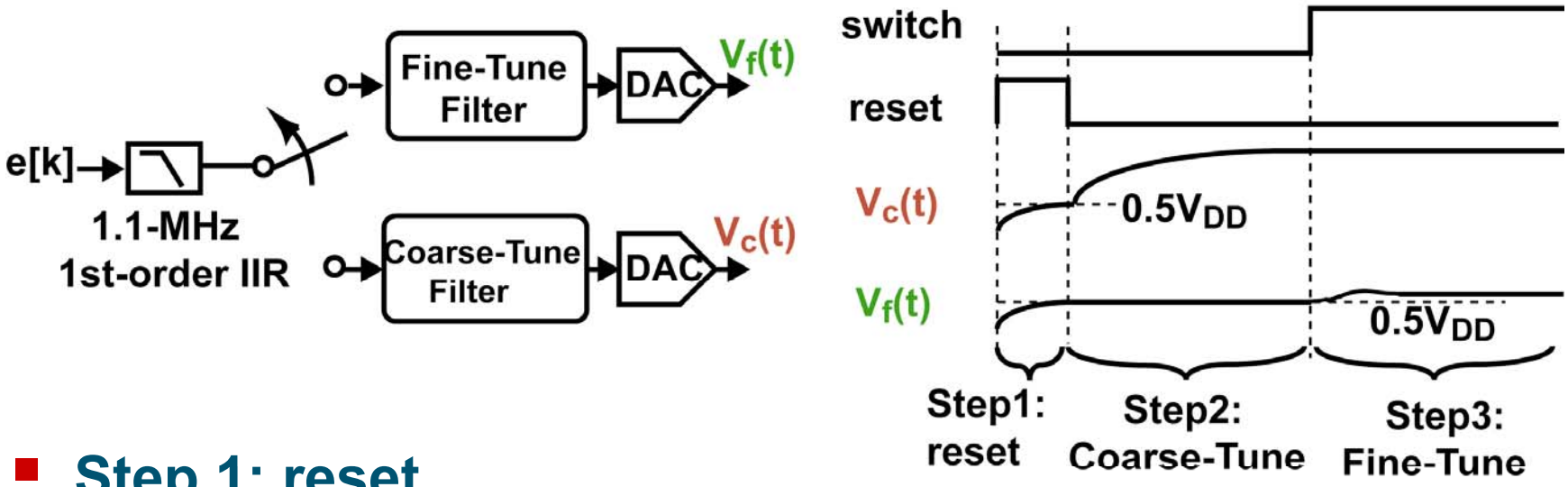
- **Resample reference with 4x division frequency**
  - **Lowers GRO range to one fourth of the reference period**

Proposed Divider Structure (cont'd)



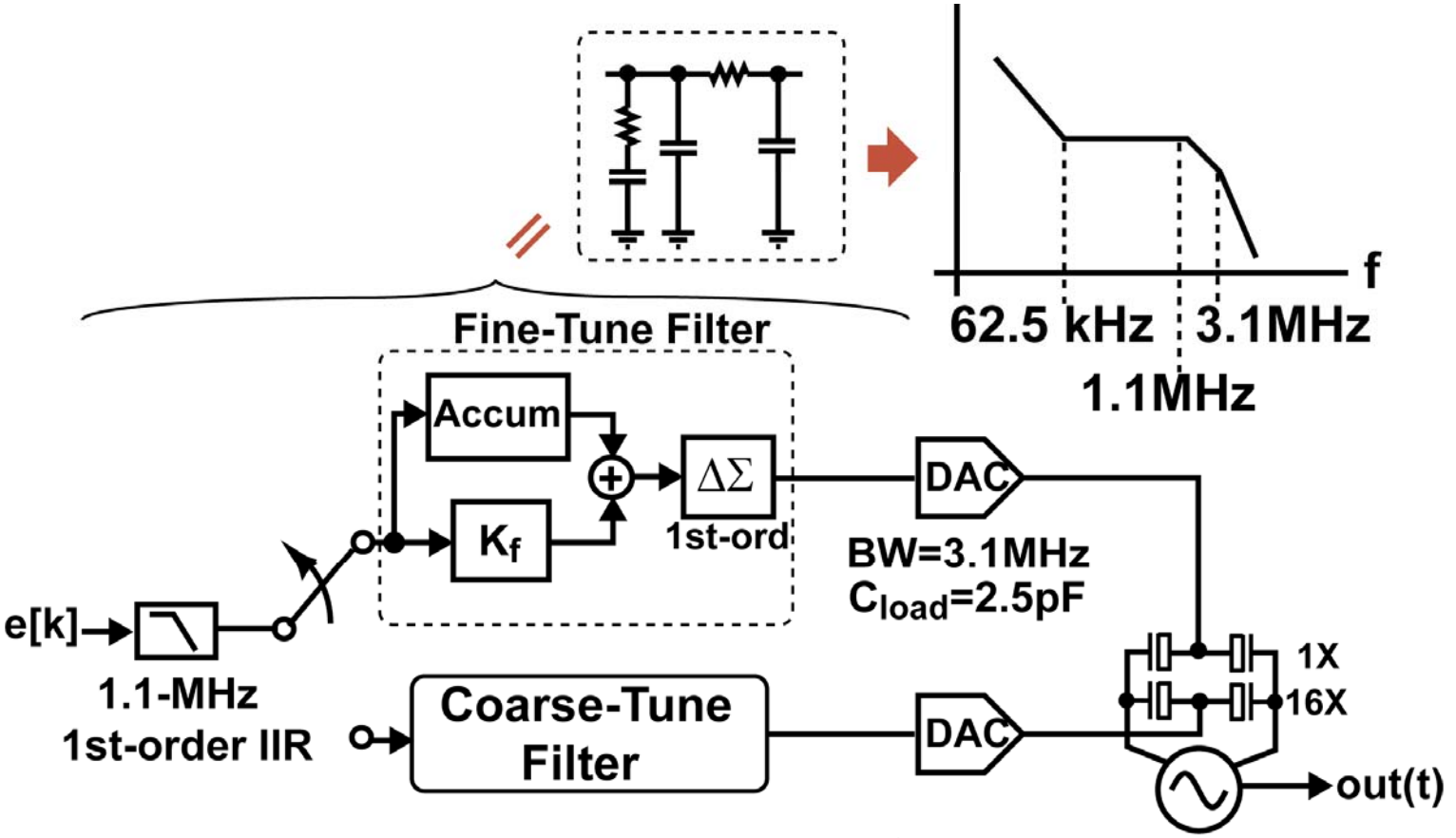
- Place ΔΣ dithered edge away from GRO edge
  - Prevents extra jitter due to divide-value dependent delay

Dual-Path Loop Filter



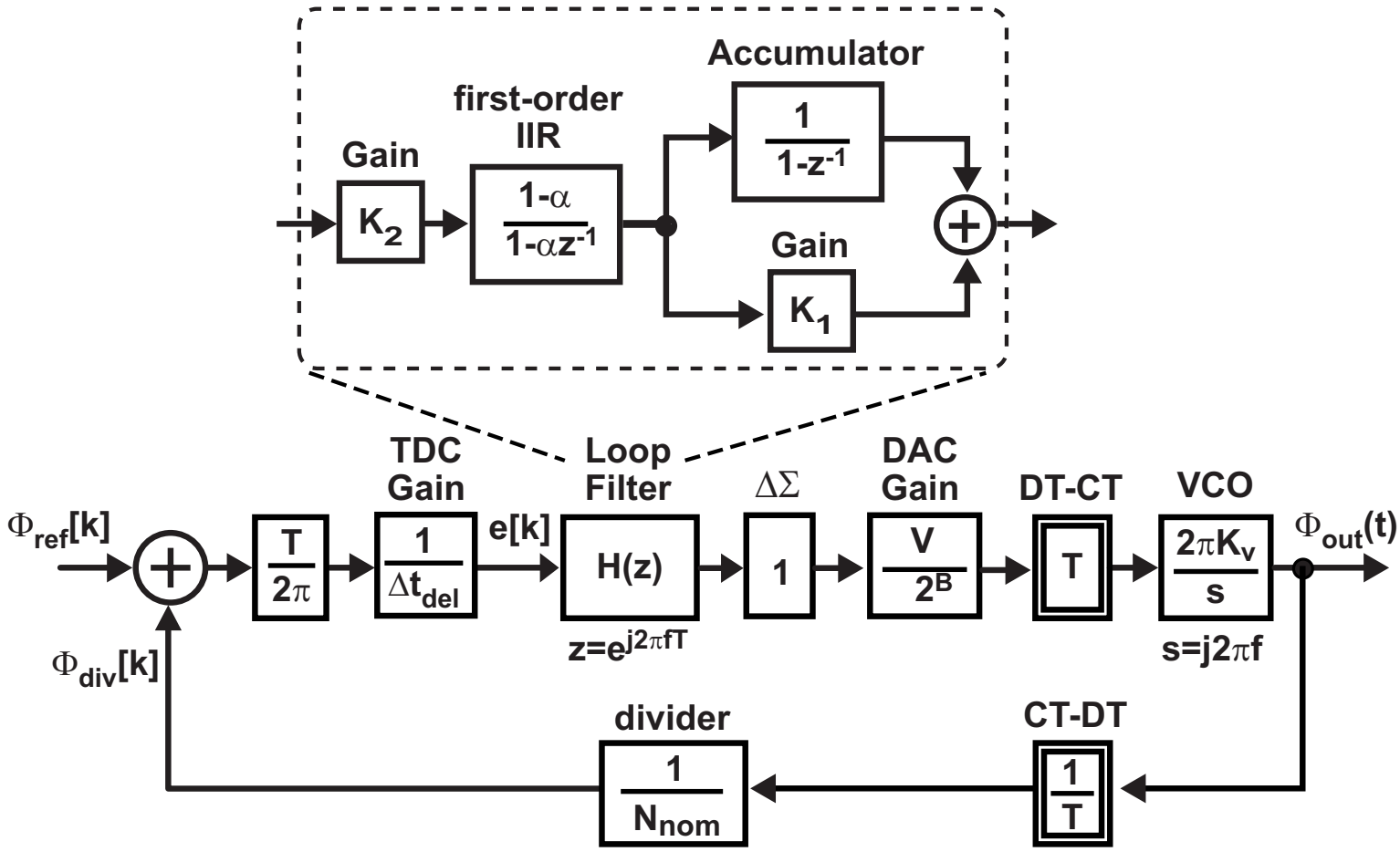
- **Step 1: reset**
- **Step 2: frequency acquisition**
  - **$V_c(t)$ varies**
  - **$V_f(t)$ is held at midpoint**
- **Step 3: steady-state lock conditions**
  - **$V_c(t)$ is frozen to take quantization noise away**
  - **ΔΣ quantization noise cancellation is enabled**

Fine-Path Loop Filter



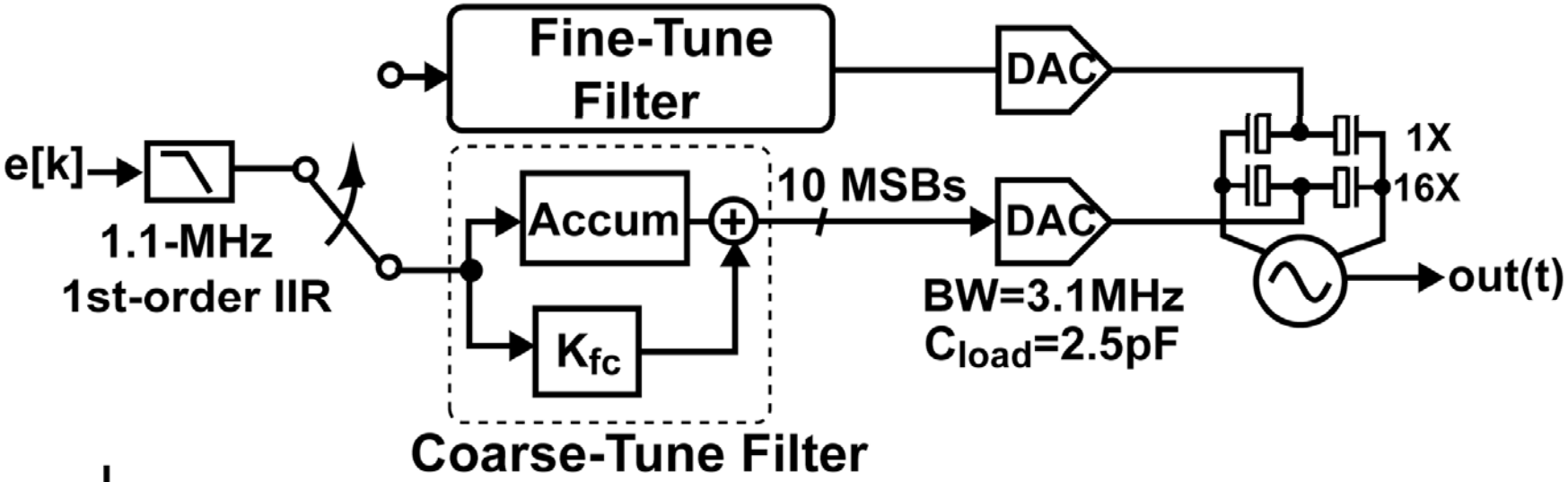
- Equivalent to an analog lead-lag filter
  - Set zero (62.5kHz) and first pole (1.1MHz) digitally
  - Set second pole (3.1MHz) by capacitor ratio
- First-order ΔΣ reduces in-band quantization noise

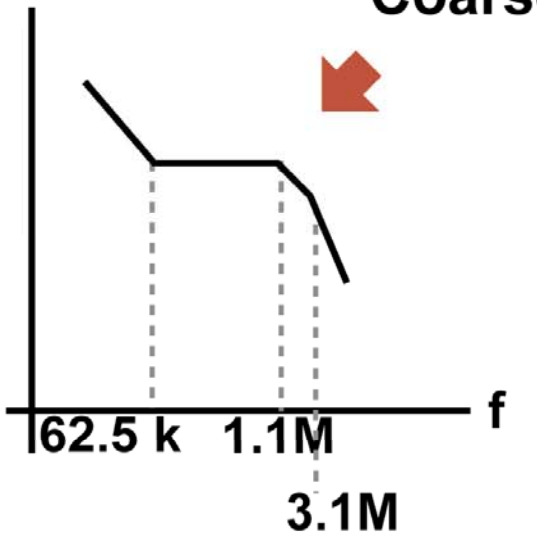
Linearized Model of PLL Under Fine-Tune Operation



- Standard lead-lag filter topology but implemented in digital domain
  - Consists of accumulator plus feedforward path

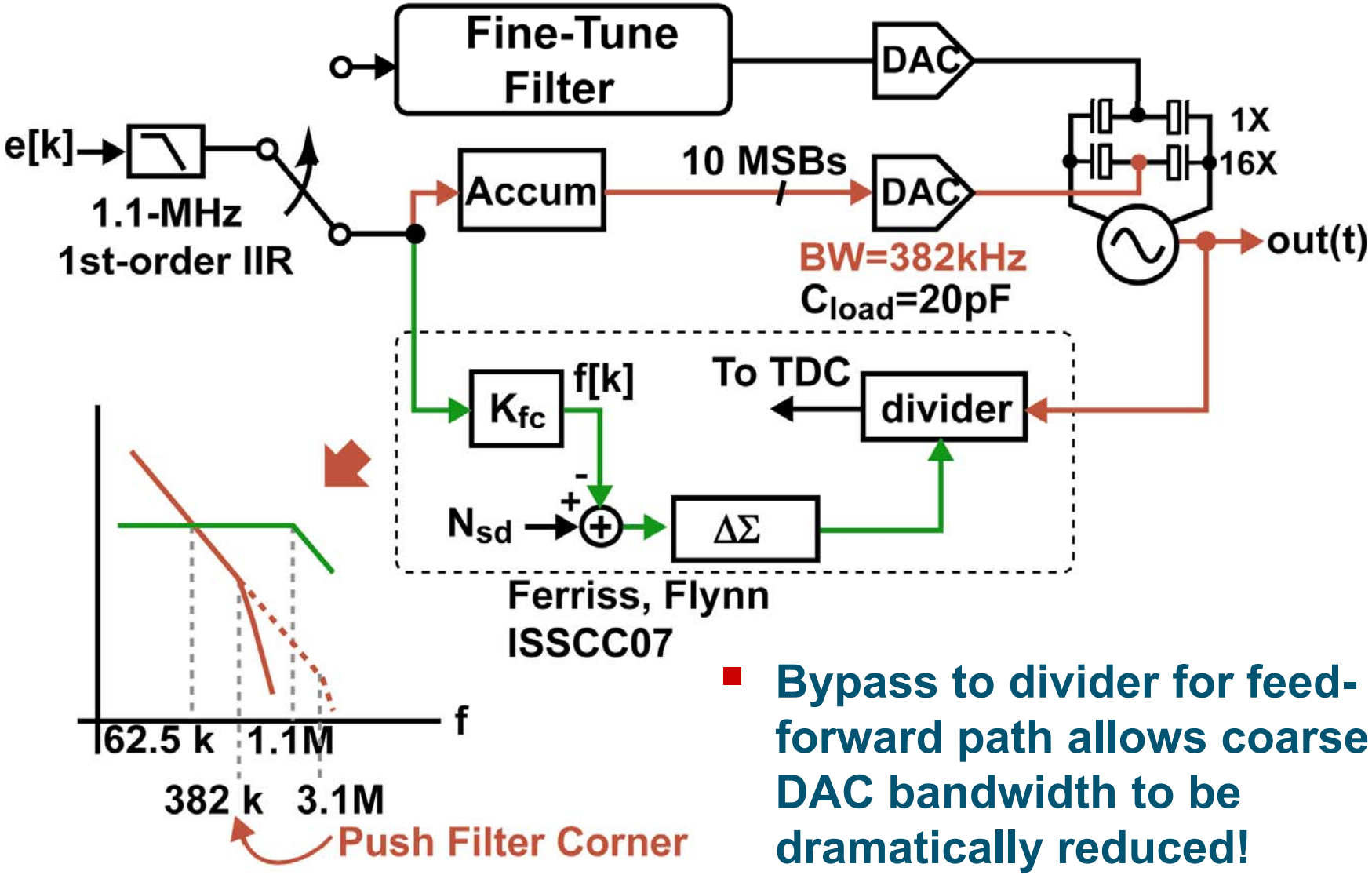
Same Technique Poses Problems for Coarse-Tune





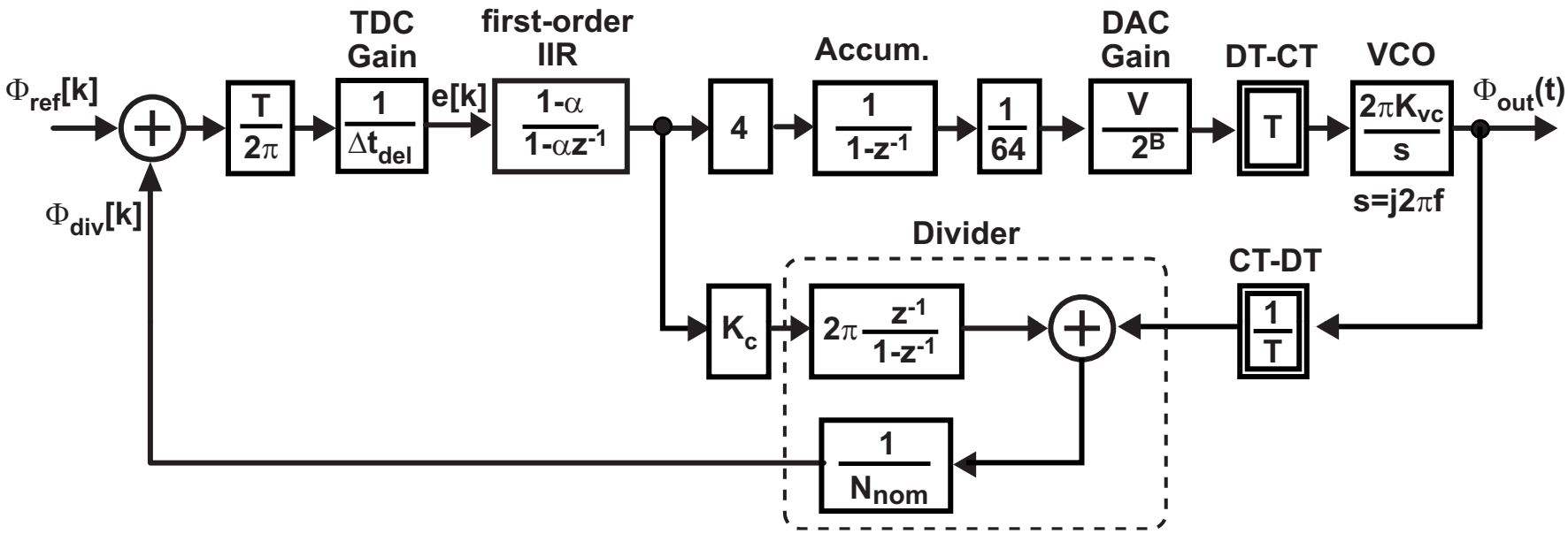
- DAC thermal noise impacts performance due to the higher coarse VCO gain
  - Can we somehow lower the DAC bandwidth?

Fix: Leverage the Divider as a Signal Path



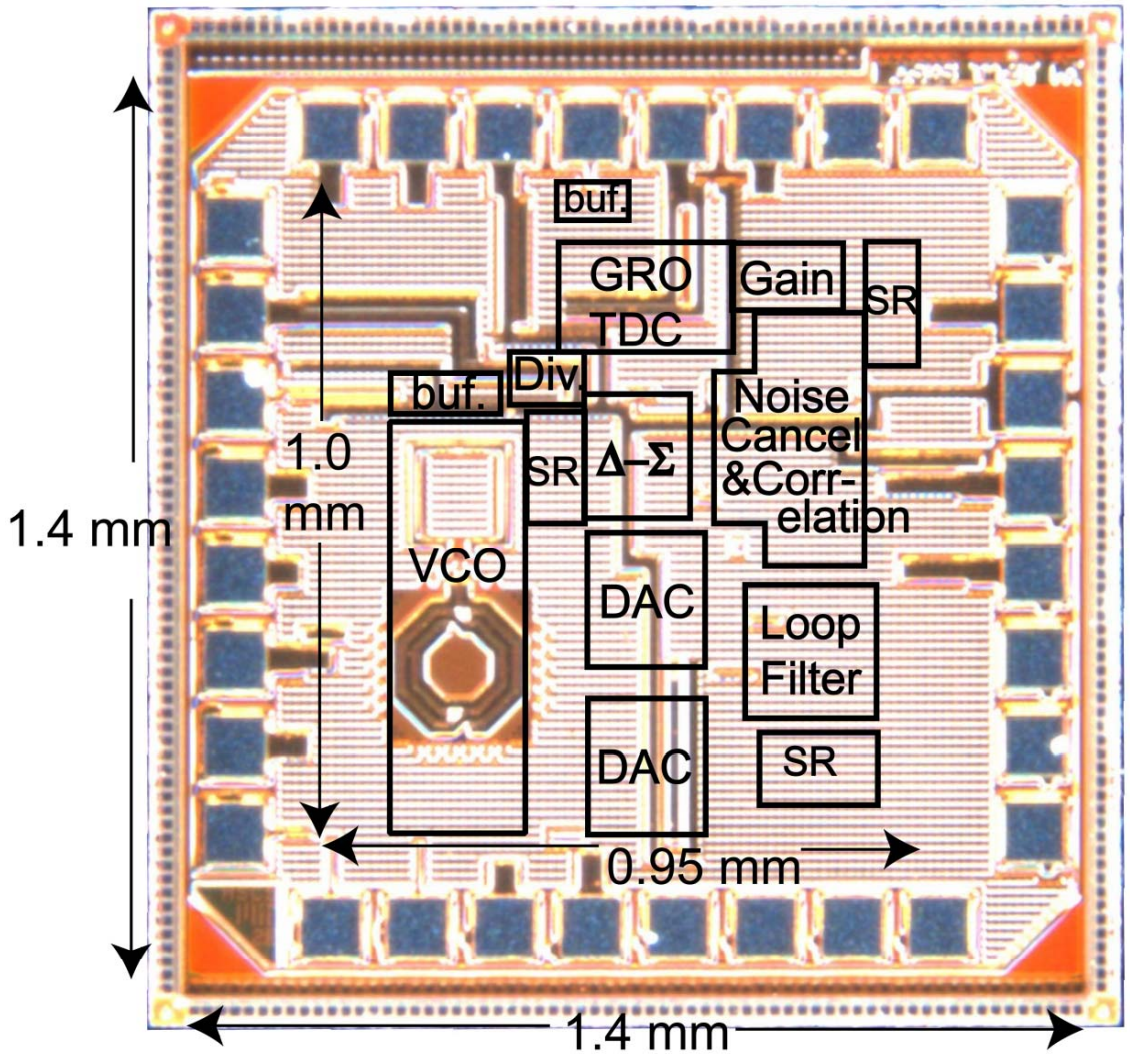
- Bypass to divider for feed-forward path allows coarse DAC bandwidth to be dramatically reduced!

Linearized Model of PLL Under Coarse-Tune Operation



- **Routing of signal path into Sigma-Delta controlling the divider yields a feedforward path**
  - **Adds to accumulator path as both signals pass back through the divider**
  - **Allows reduction of coarse DAC bandwidth**
    - Noise impact of coarse DAC on VCO is substantially lowered

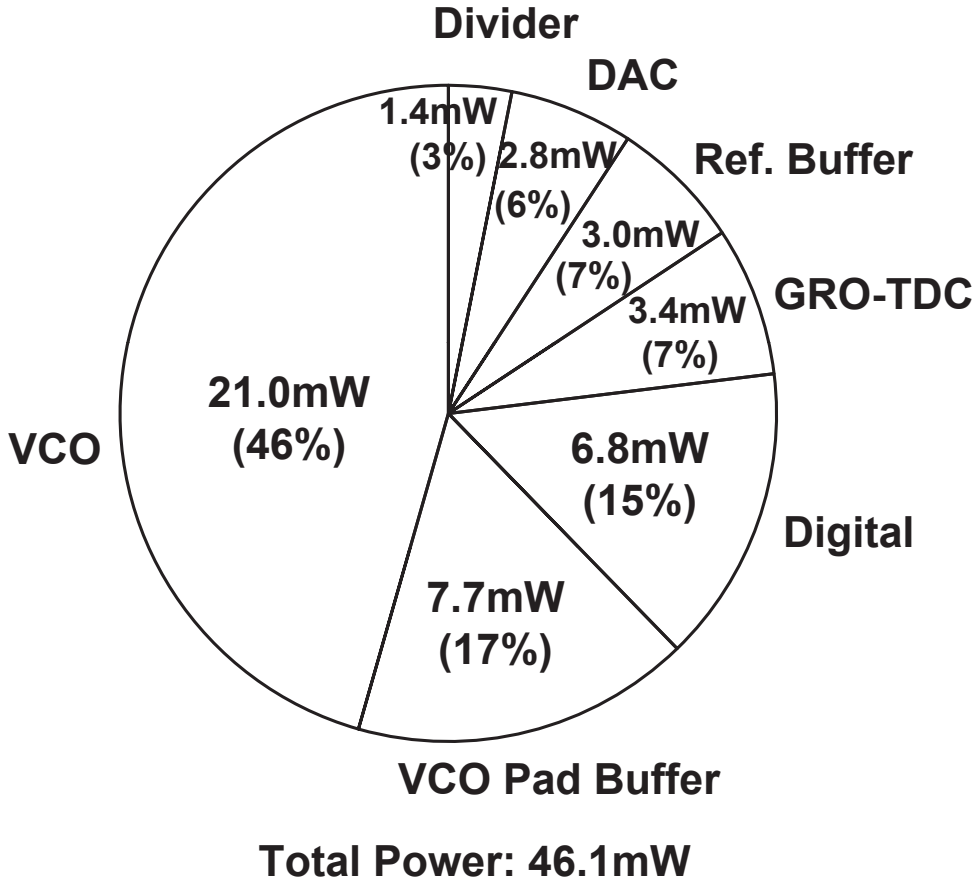
Die Photo



- 0.13-μm CMOS
- Active area: 0.95 mm^2
- Chip area: 1.96 mm^2
- V_{DD}: 1.5V
- Current:
  - 26mA (Core)
  - 7mA (VCO output buffer at 1.1V)

GRO-TDC:
- 2.3mA
- 157X252 um^2

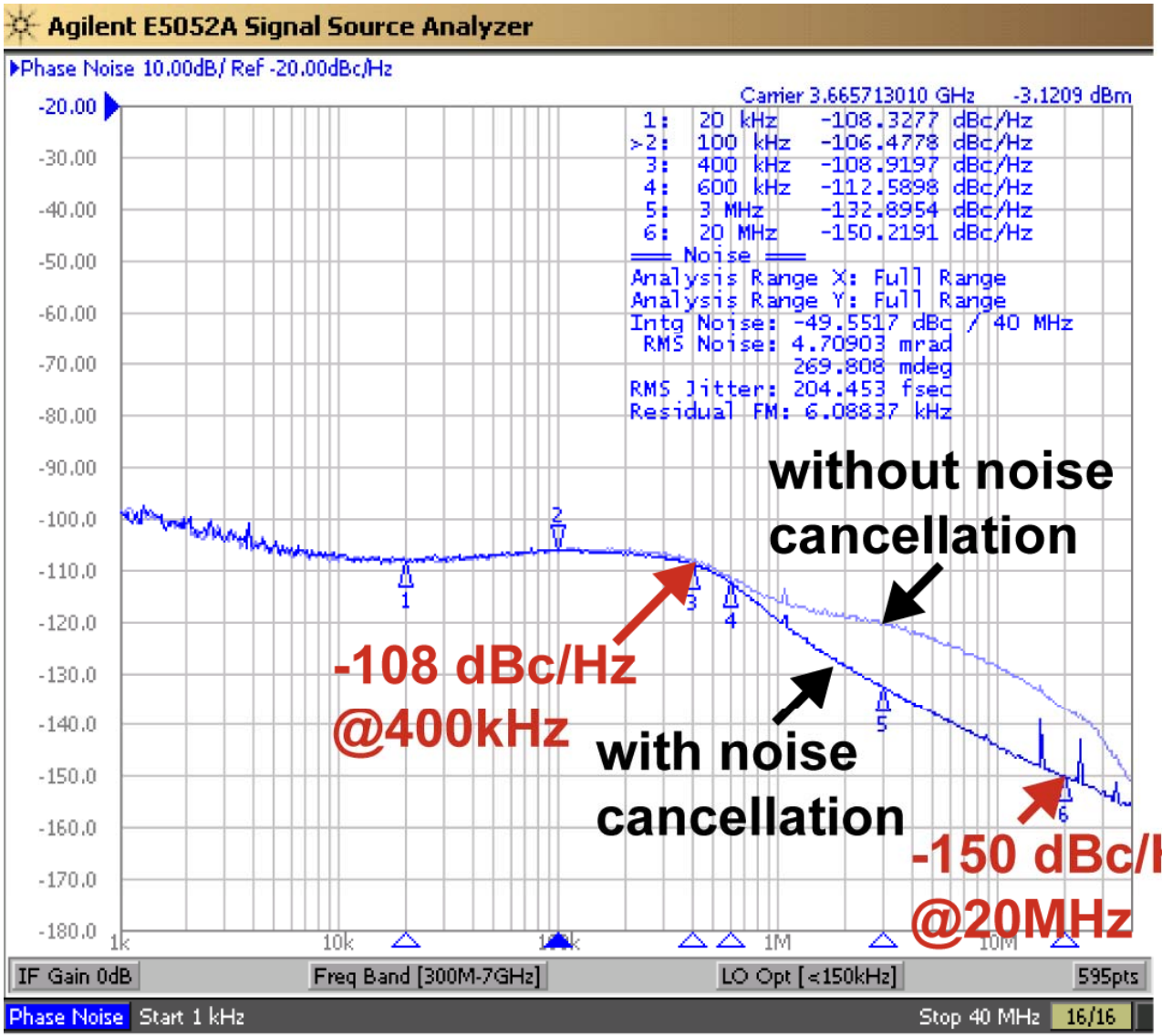
Power Distribution of Prototype IC



Total Power: 46.1mW

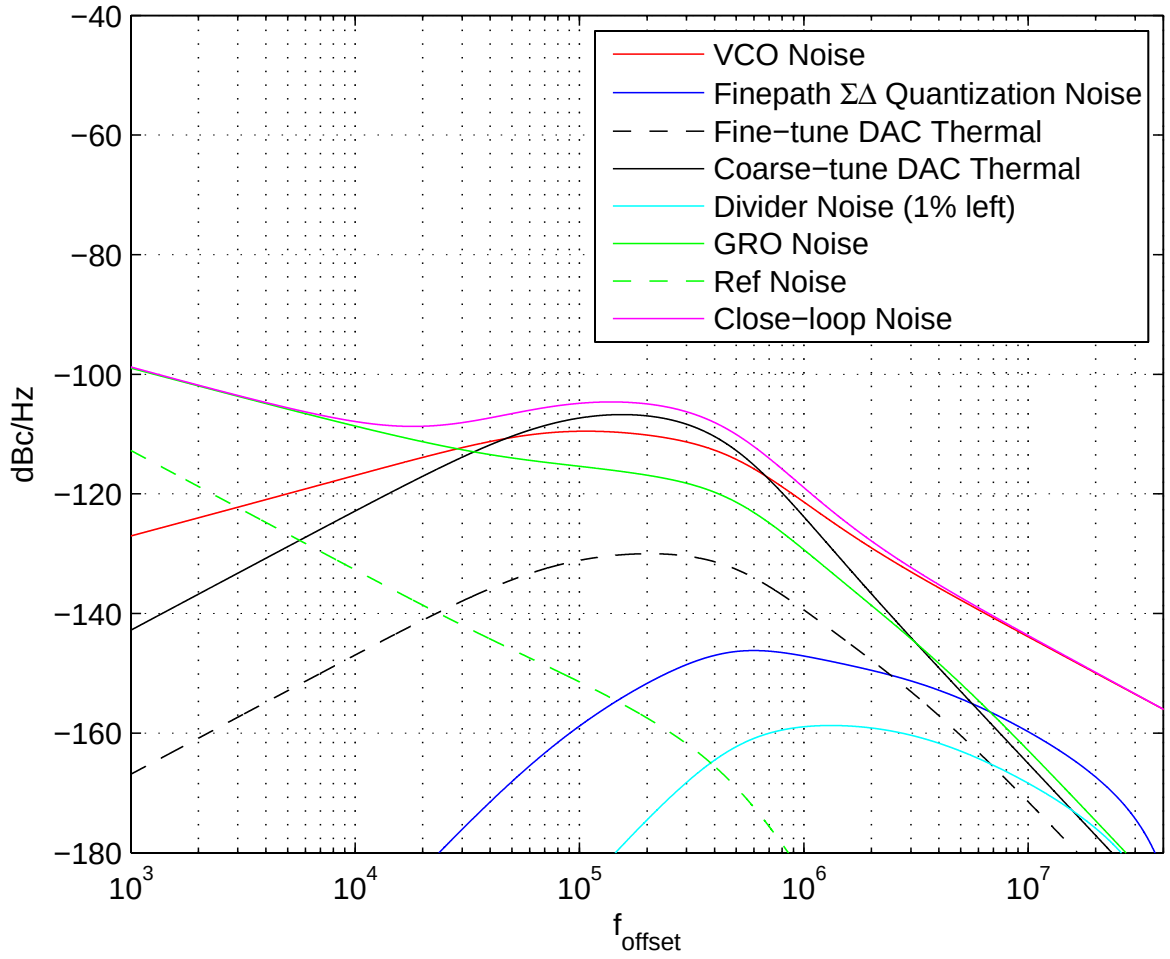
- **Notice GRO and digital quantization noise cancellation have only minor impact on power (and area)**

Measured Phase Noise at 3.67GHz



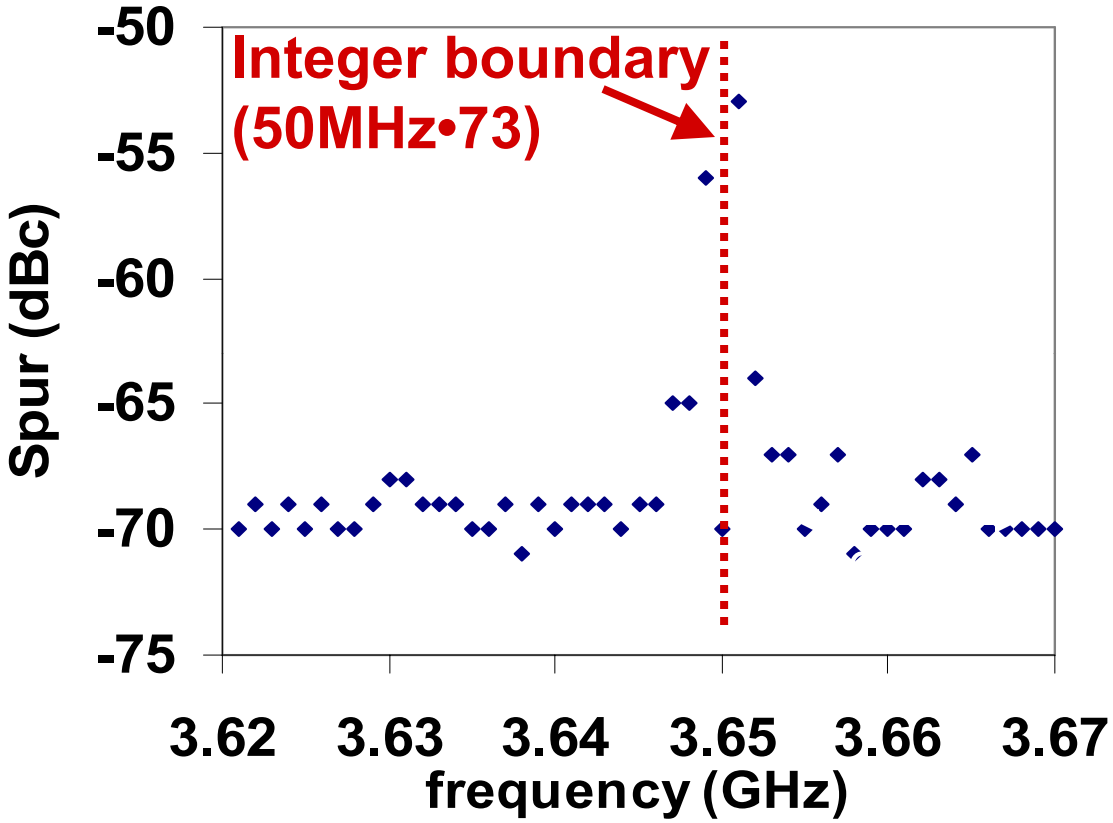
- **Suppresses quantization noise by more than 15 dB**
- **Achieves 204 fs (0.27 degree) integrated noise (jitter)**
- **Reference spur: -65dBc**

Calculation of Phase Noise Components



- **See wideband digital synthesizer tutorial available at http://www.cppsim.com**

Measured Worst Spurs over Fifty Channels



- Tested from 3.620 GHz to 3.670 GHz at intervals of 1 MHz
  - Worst spurs observed close to integer-N boundary (multiples of 50 MHz)
- -42dBc worst spur observed at 400kHz offset from boundary

Conclusions

- **Digital Phase-Locked Loops look extremely promising for future applications**
  - **Very amenable to future CMOS processes**
  - **Excellent performance can be achieved**

- **A low-noise, wide-bandwidth digital ΔΣ fractional-N frequency synthesizer is achieved with**
  - **High performance *noise-shaping* GRO TDC**
  - **Quantization noise cancellation in *digital* domain**

- **Key result: < *250 fs* integrated noise with 500 kHz bandwidth**

Innovation of future digital PLLs will involve joint circuit/algorithm development