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Cascaded Noise Shaping for Oversampling A/D and D/A Conversion

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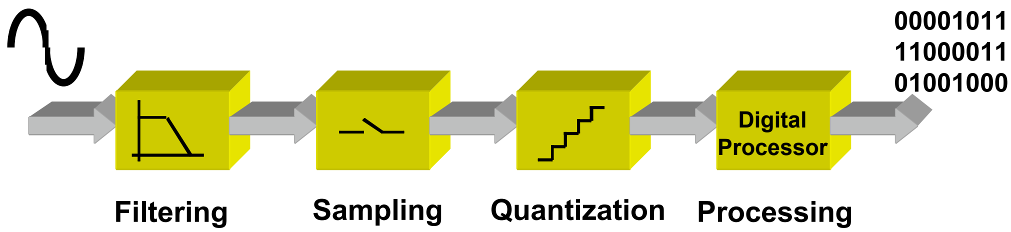
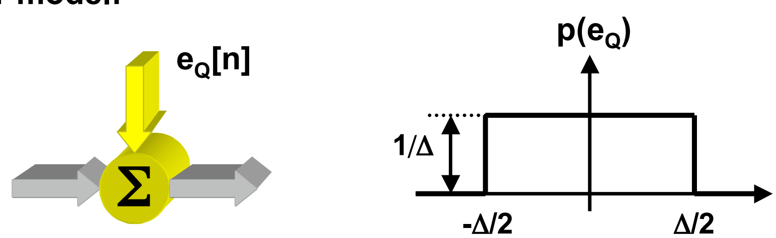
Outline

- **Oversampling modulators for A-to-D conversion**
- **Cascaded ΣΔ modulators**
- **Low-voltage ΣΔ modulator design for MHz-bandwidth signals**
- **Cascaded noise shaping for bandpass oversampling D-to-A conversion**

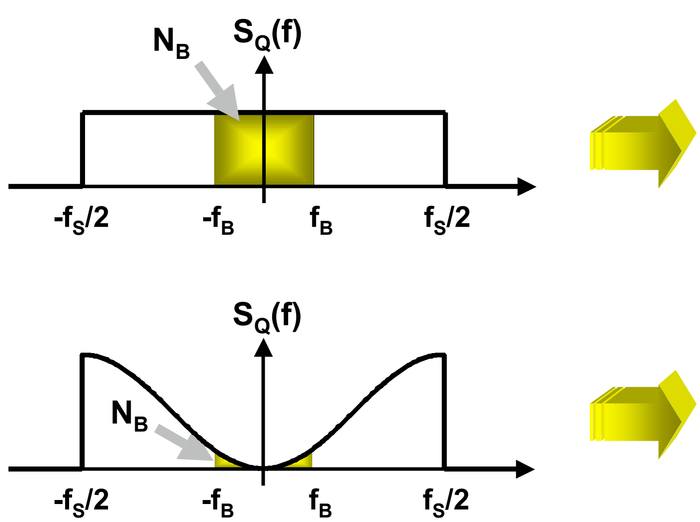
Analog-to-Digital Conversion



Quantizer model:



Quantization Noise Shaping



Quantizer resolution increased by 3 dB per octave of OVERSAMPLING

Quantizer resolution increased through NOISE SHAPING

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Oversampling Modulators

- **Embed quantizer in a feedback loop to achieve larger improvement in resolution with increasing oversampling**
- **Feedback can be used for PREDICTION (Δ modulation) or NOISE SHAPING (ΣΔ modulation)**
- **Noise shaping modulators are more robust and easier to implement than predictive modulators**

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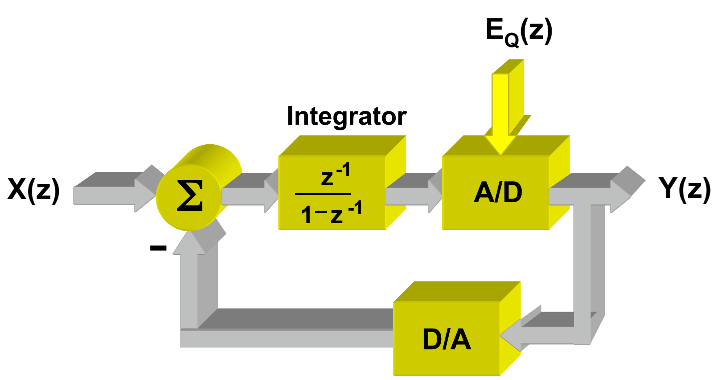
Sigma-Delta (or Delta-Sigma) Modulation



$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E_Q(z)$$

$$N_E(f) = \left[2\sin\left(\pi f / f_S\right)\right]^2 N_Q(f)$$

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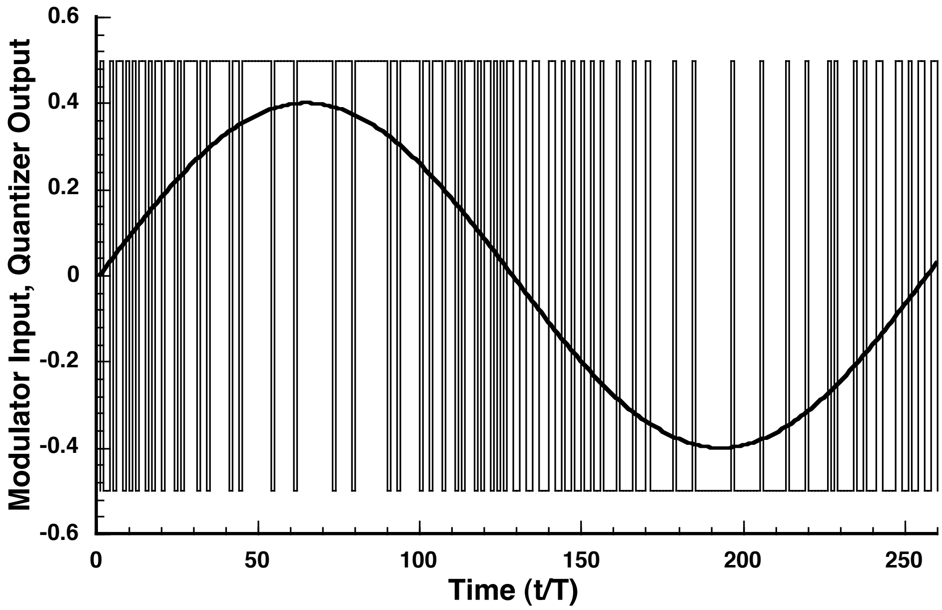
ΣΔ Modulator Response



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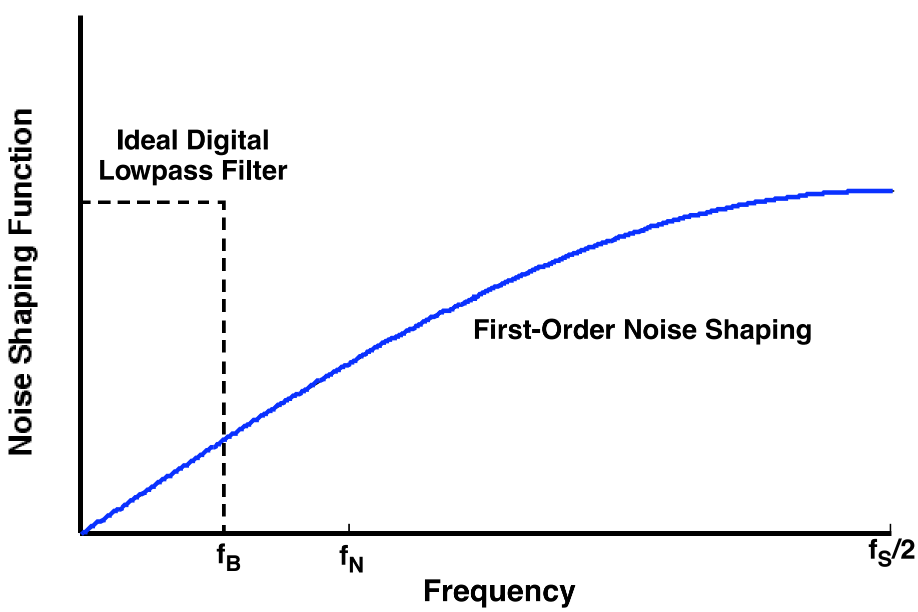
Noise Shaping



Higher-Order Noise-Shaping Modulators

The order of the noise shaping can be increased using either

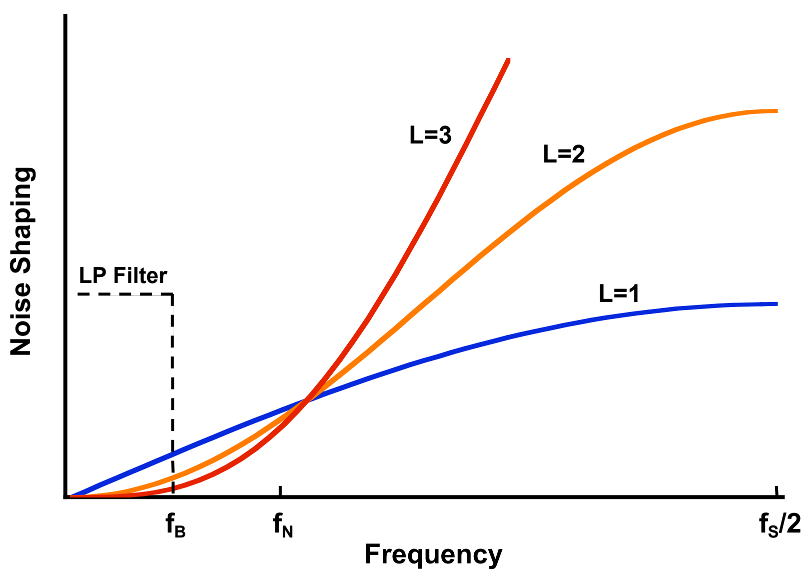
- Single quantizer modulators
  - Multi-loop noise differencing
  - Single loop with multi-order filtering

or

- Cascaded (multistage) modulators

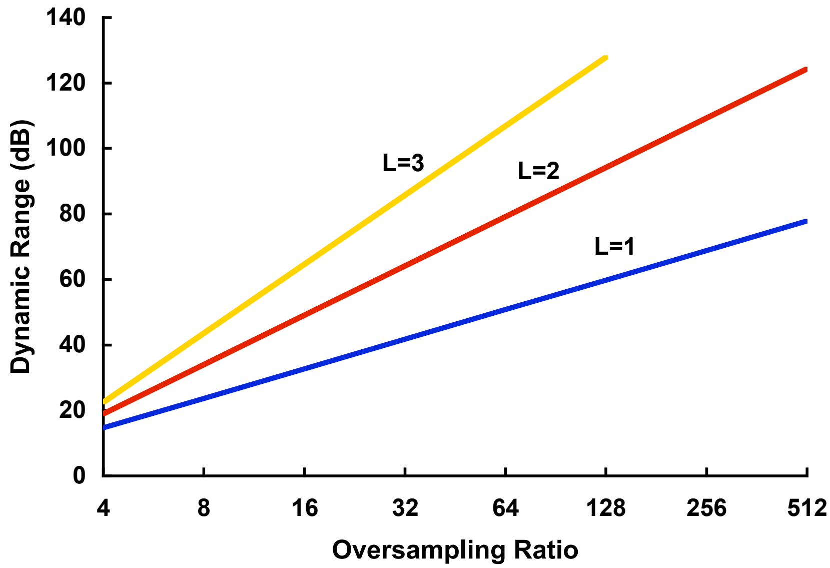
Noise-Differencing ΣΔ Modulators

$$Y(z) = z^{-1}X(z) + (1-z^{-1})^L E(z)$$

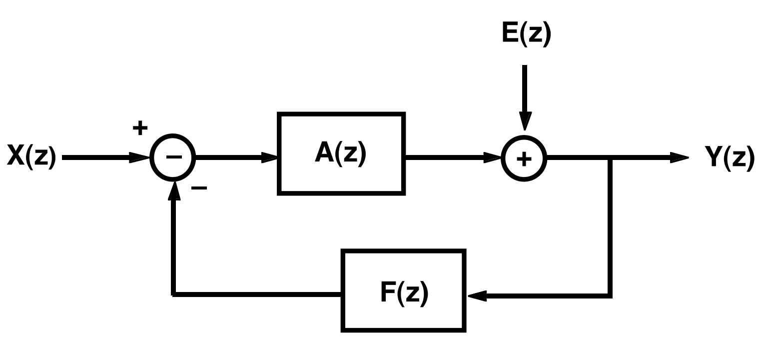


ΣΔ Modulator Dynamic Range

(with 1-bit quantization)



Single-Quantizer ΣΔ Modulator



$$Y(z) = H_X(z)X(z) + H_E(z)E(z)$$

where

$$H_X(z) = \frac{A(z)}{1 + A(z)F(z)}, \quad H_E(z) = \frac{1}{1 + A(z)F(z)}$$

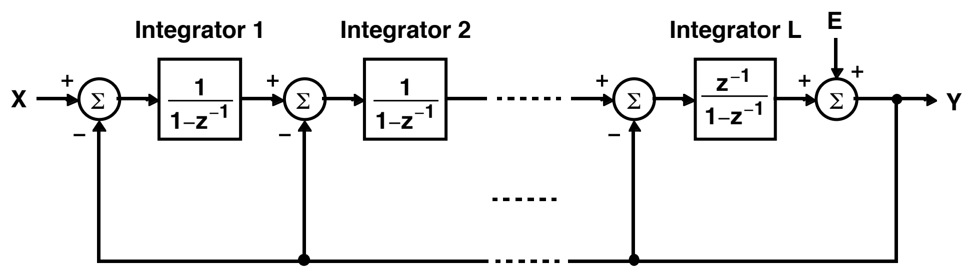
and

$$A(z) = \frac{H_X(z)}{H_E(z)}, \quad F(z) = \frac{1 - H_E(z)}{H_X(z)}$$

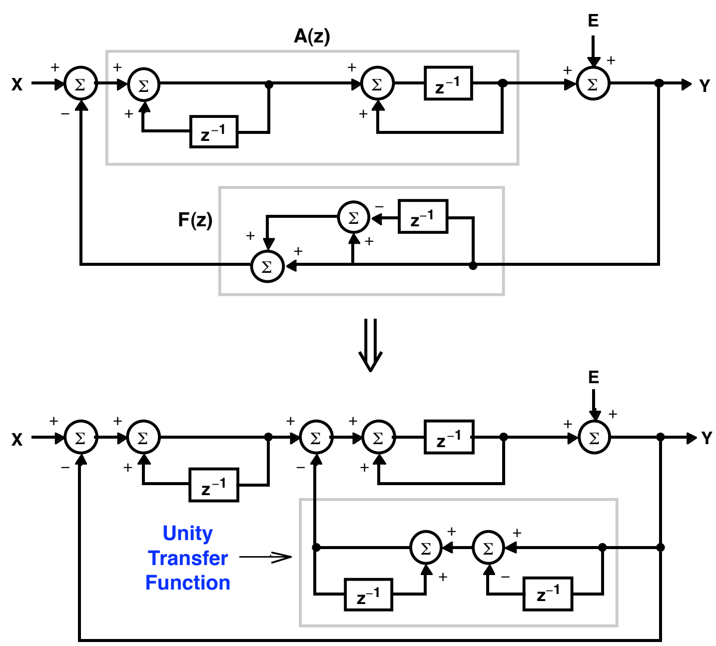
Noise Differencing Modulators

- $Y(z) = z^{-1}X(z) + (1-z^{-1})^L E(z)$
- Can implement with a single quantizer and L nested loops
- Limit cycle instability for L > 2
- For L = 2

$$A(z) = \frac{z^{-1}}{(1-z^{-1})^2} \quad \text{and} \quad F(z) = 2 - z^{-1}$$



2nd-Order Modulator Implementation



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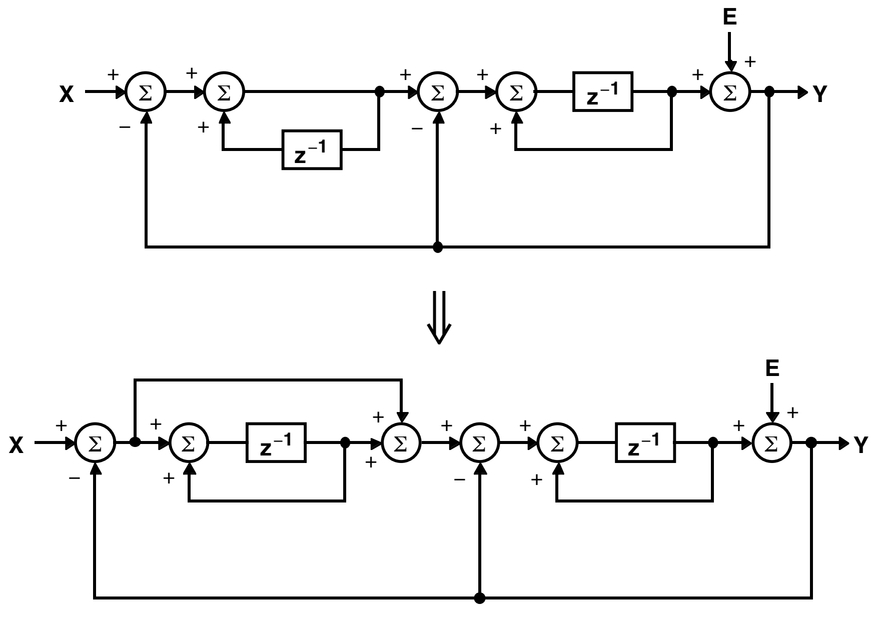
2nd-Order ΣΔ Modulator



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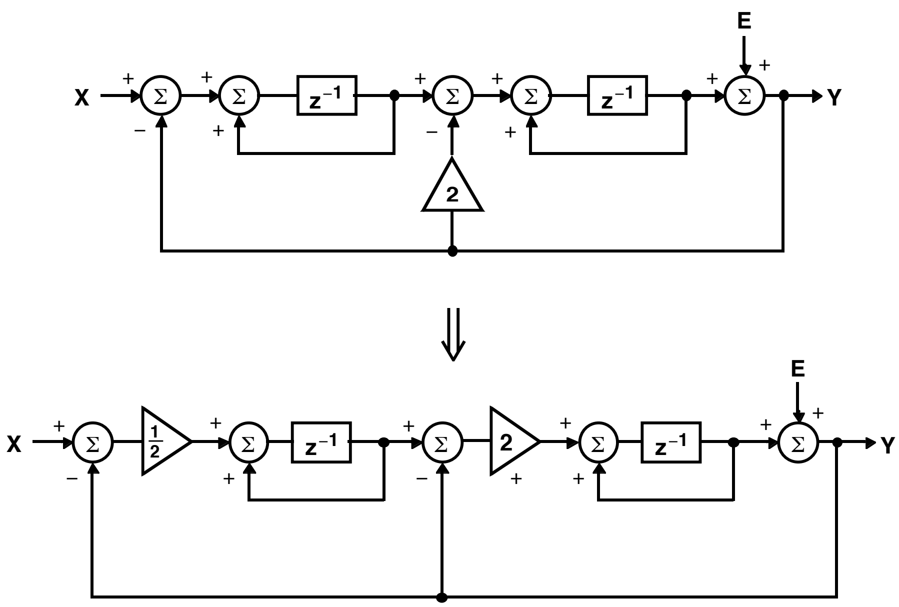
2nd-Order ΣΔ Modulator



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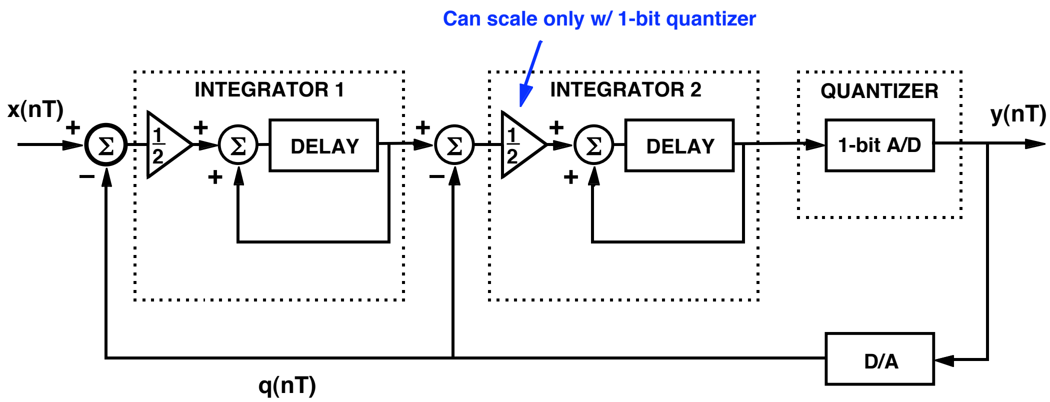
2nd-Order Noise-Differencing ΣΔ Modulator *

(with 1-bit quantization)



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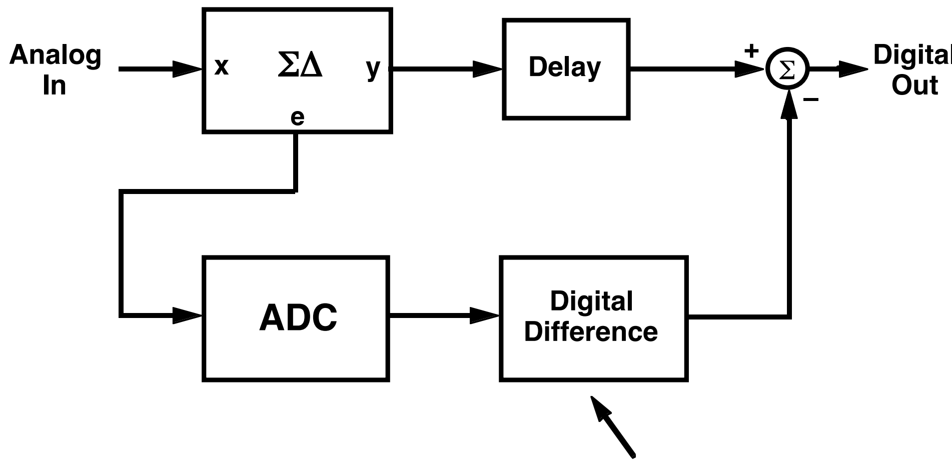
Cascaded ΣΔ Modulators

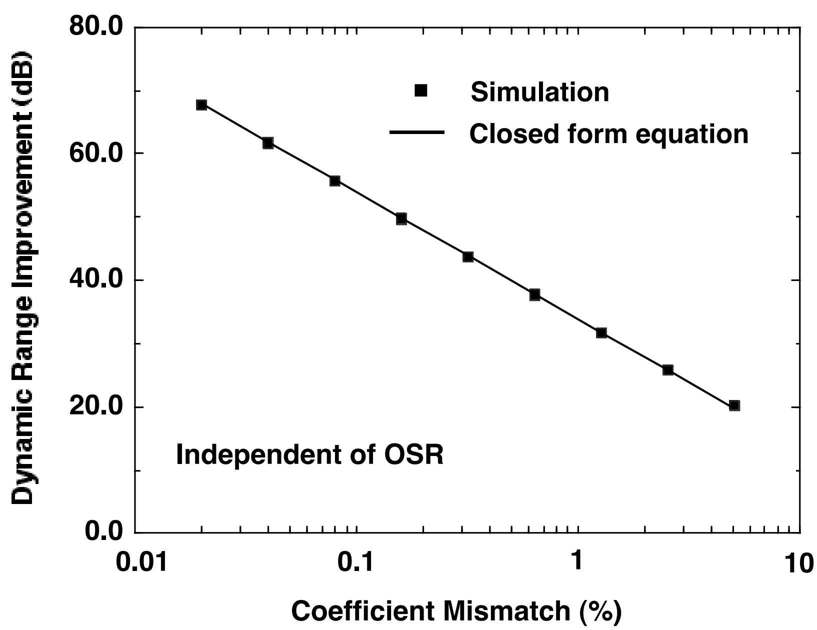
- Quantizer error quantized by subsequent stage and then digitally filtered and subtracted from output of preceding stage
- Cancellation of lower-order noise-shaping terms depends on matching of analog and digital paths
- No potential instability if use first- and second-order stages

Cascaded Noise-Shaping Modulator

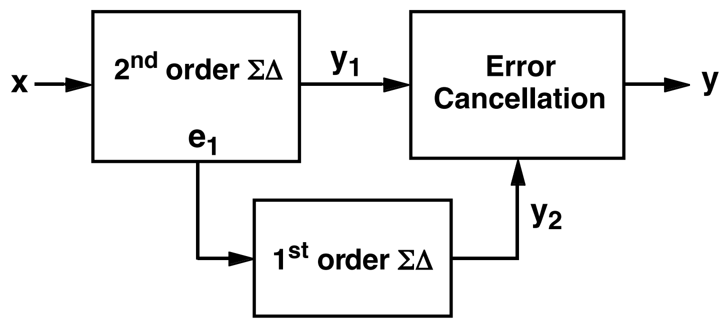


Matches noise shaping of
quantization error in first-stage

Maximum Improvement in Dynamic Range



Third-Order (2-1) Cascaded Modulator

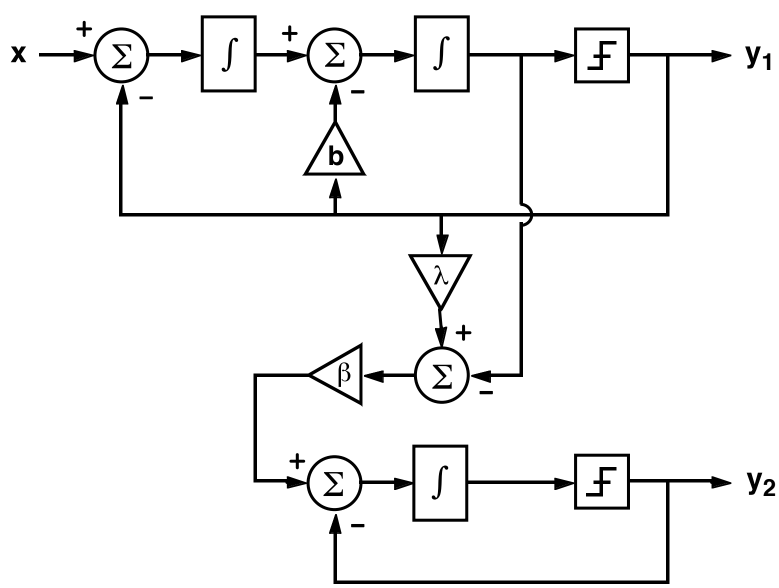


$$Y_1(z) = z^{-2}X(z) + (1 - z^{-1})^2 E_1(z)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z)$$

$$Y(z) = z^{-1}Y_1(z) - (1 - z^{-1})^2 Y_2(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_2(z)$$

2-1 Cascaded ΣΔ Modulator



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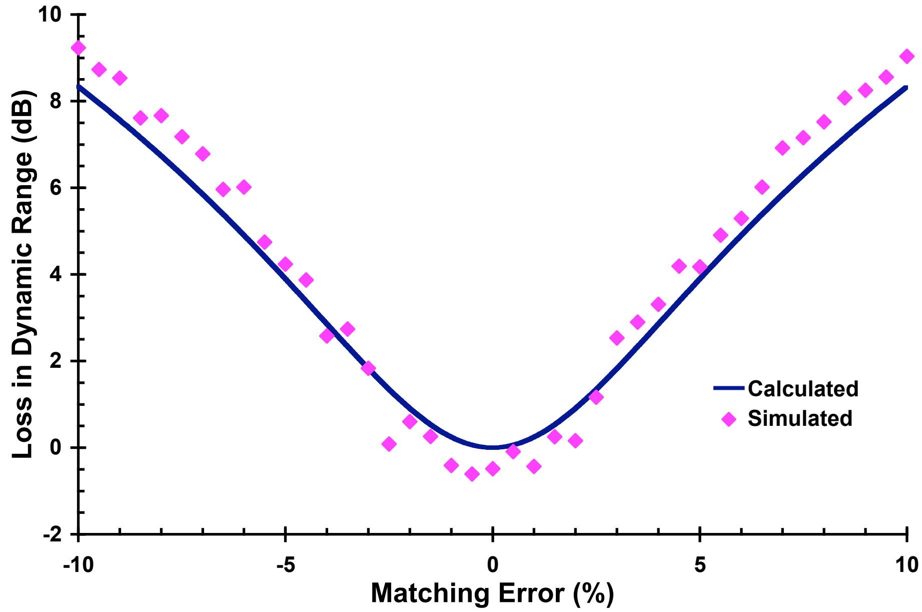
Matching Error in 2-1 Cascade



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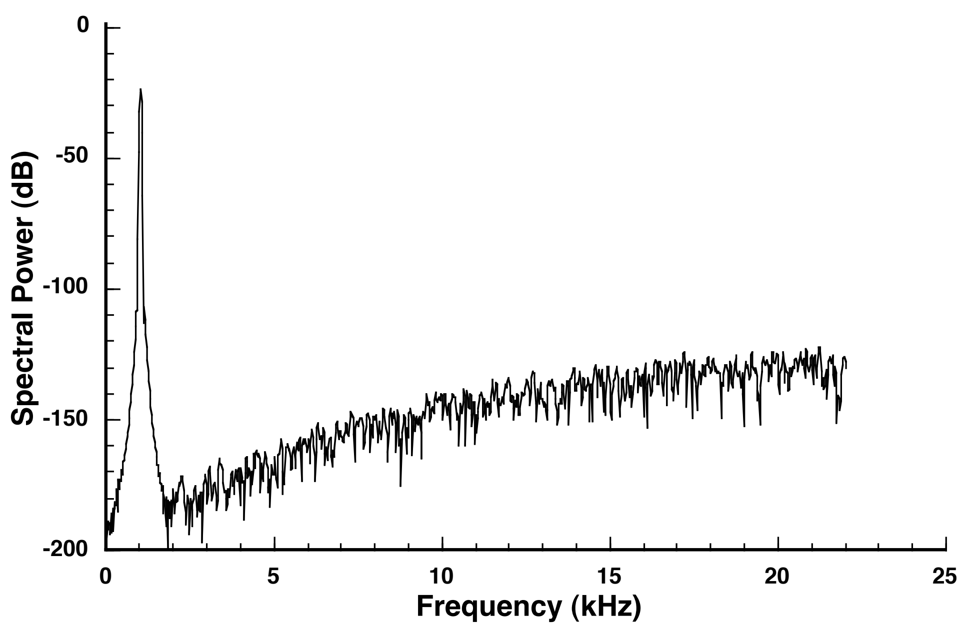
Spectrum of 2-1 Cascade w/ Mismatch



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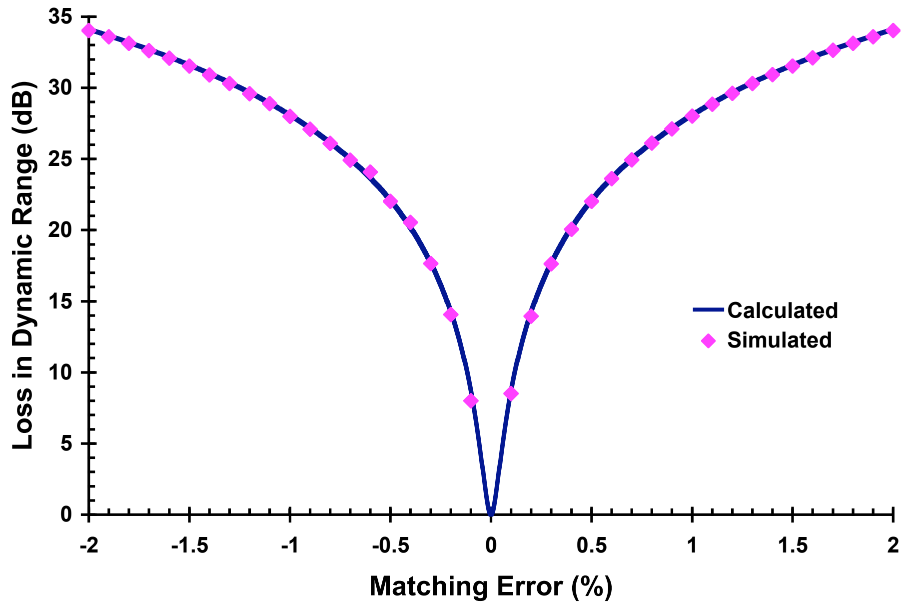
Matching Error in 1-1-1 Cascade



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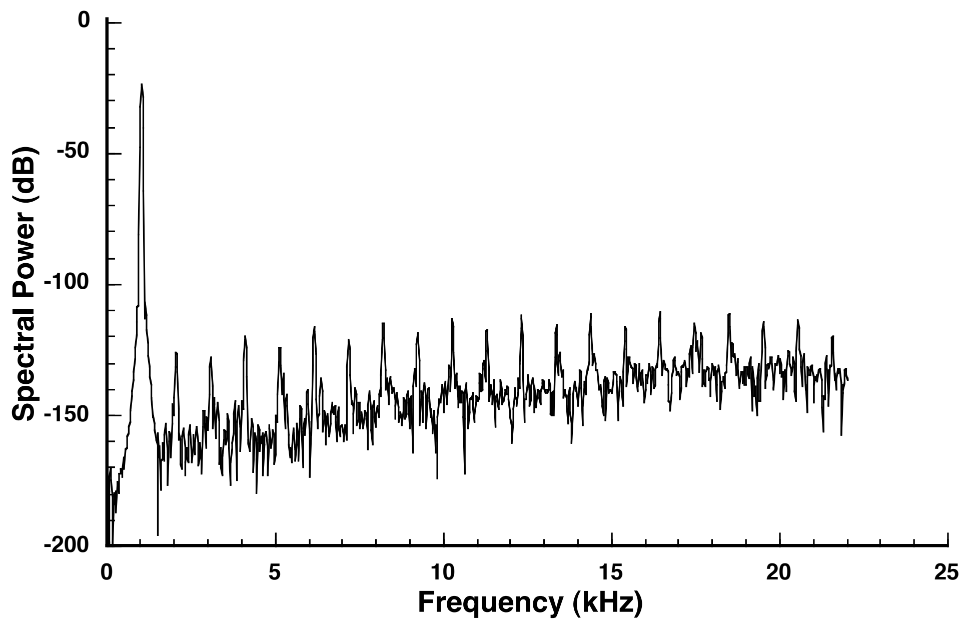
Spectrum of 1-1-1 Cascade w/ Mismatch



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Advantages of 2-1 Cascade

- Low sensitivity to precision of analog circuits
- Suppression of spurious noise tones resulting for correlation of quantization noise with input
- Considerable design flexibility
- No potential instability

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Analog Integration in CMOS

- Continuous Time (tune g_m or MOS-R)
  - g_m-C
  - MOSFET-C
- Sampled Data
  - Switched current
  - Switched capacitor

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Analog Integration in CMOS

- Continuous-time (g_m-C or MOSFET)
  - Tune g_m or MOS resistor
  - Performance limited by timing jitter, waveform asymmetry and integrator linearity
- Switched-current
  - Limitations:
    - current sources must be cascoded to increase output resistance ⇨ high supply voltage
    - large $V_{GS} - V_T$ needed to reduce sensitivity to V_T mismatch ⇨ high power dissipation
    - sensitive to switch parasitics and charge injection
    - noise introduced into “compressed” signal

⇨ Switched-capacitor approach preferable for obtaining high resolution at low supply voltage and low power dissipation

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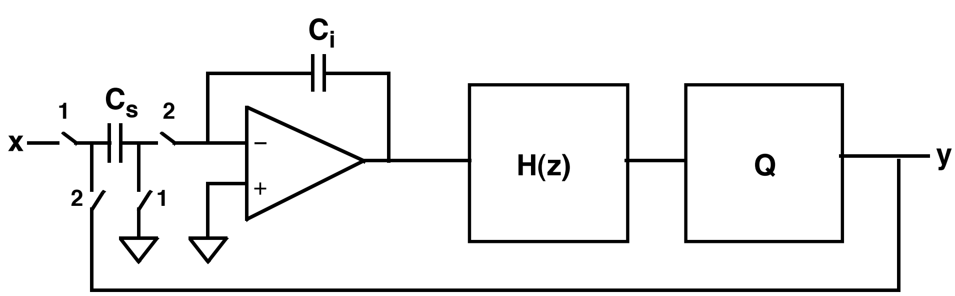
Low-Power ΣΔ Modulator Design *



- High-resolution converters should by limited by thermal noise
  - kT/C noise in switched-capacitor circuits
- First stage limit performance and therefore dissipates a large fraction of power
- Minimize power by minimizing capacitor size in switched-C implementations

* S. Rabii, JSSC, June 1997

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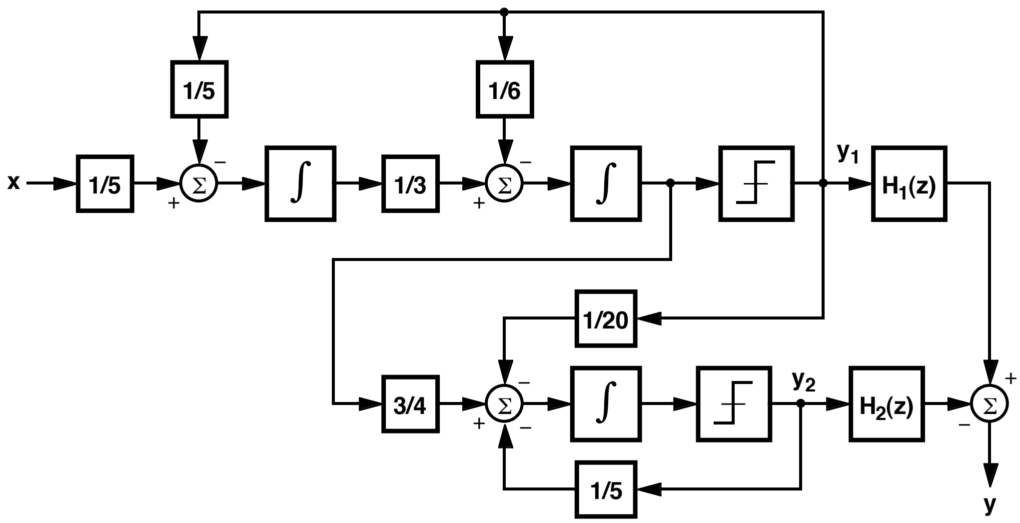
ΣΔ Modulator Implementation



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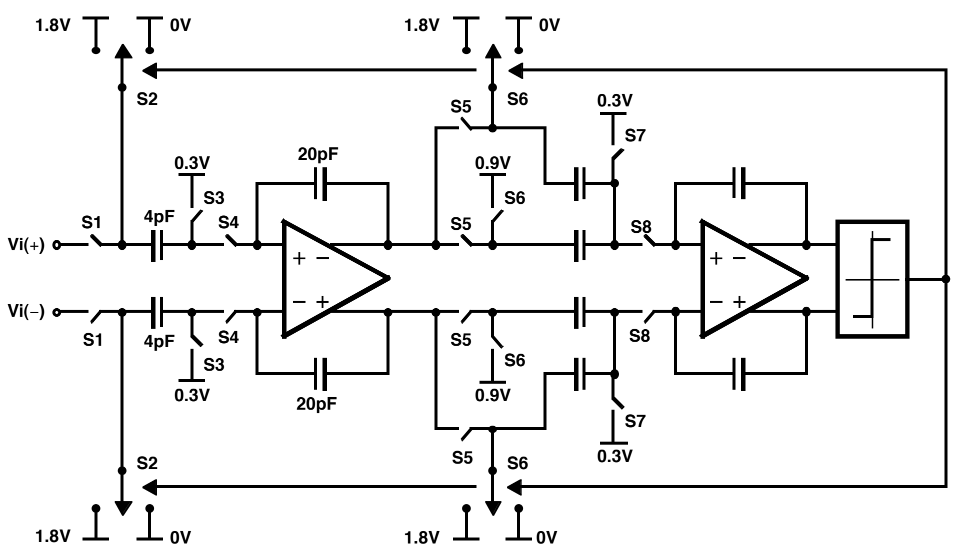
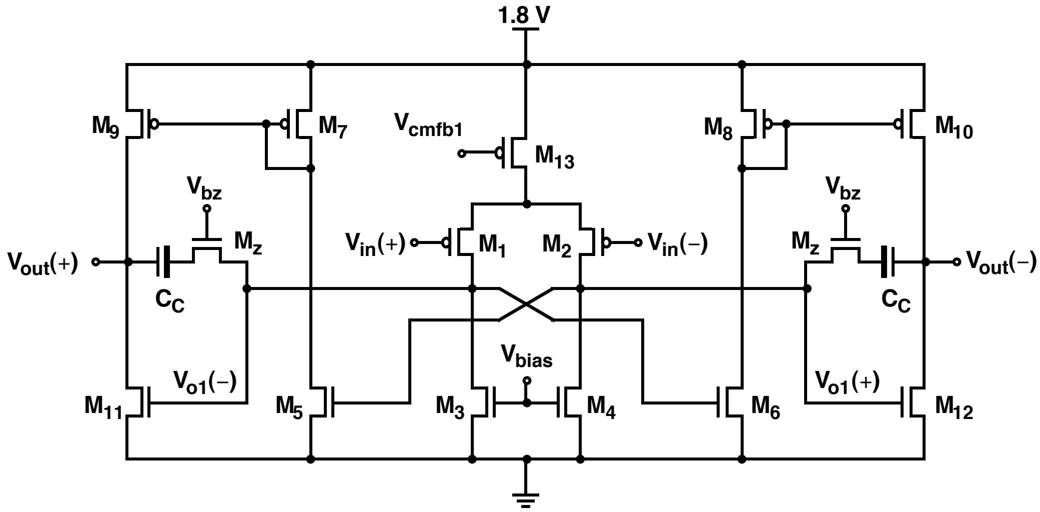
First Stage of Modulator



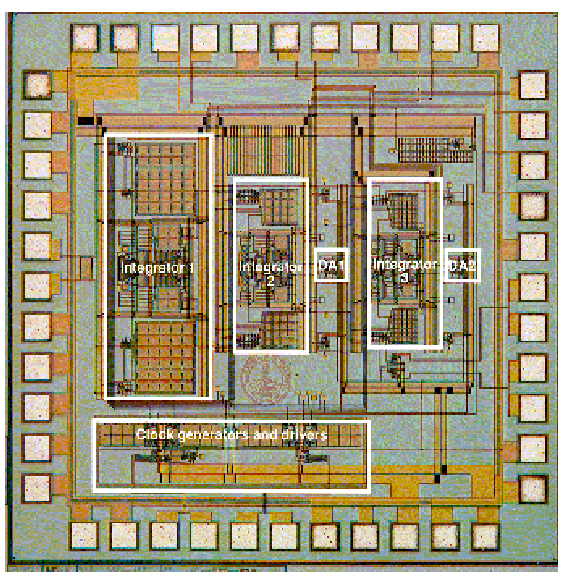
S1, S5: $\Phi1_{delayed}$, CMOS S3, S7: $\Phi1$, NMOS

S2, S6: $\Phi2_{delayed}$, CMOS S4, S8: $\Phi2$, NMOS

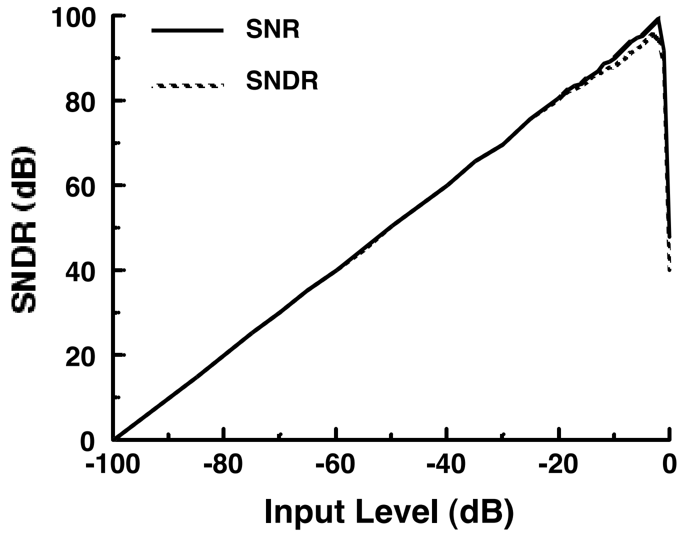
2-Stage Class A/AB Amplifier



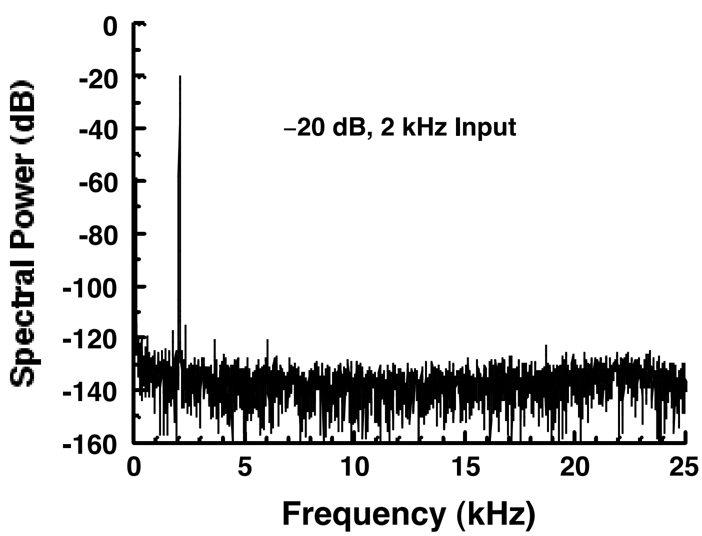
Die Photo of 1.8-V CMOS ΣΔ Modulator



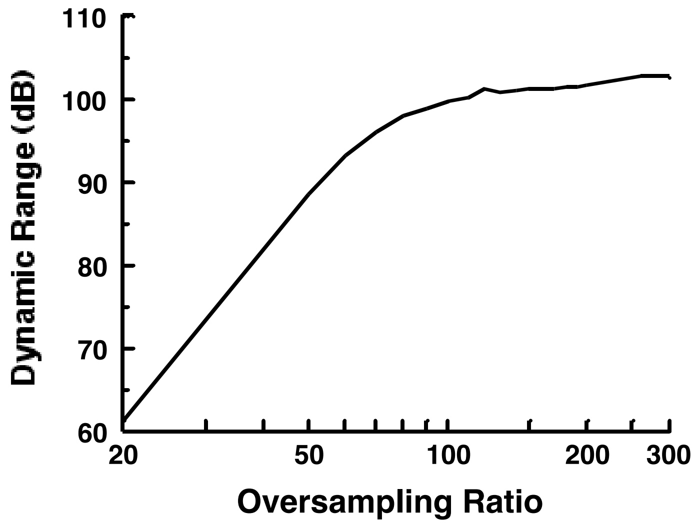
Measured SNR and SNDR



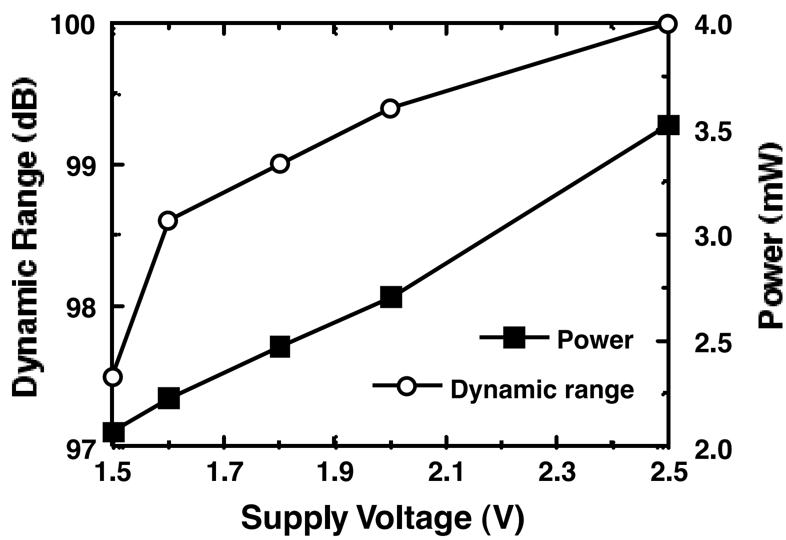
Measured Baseband Output Spectrum



Dynamic Range vs. Oversampling Ratio



Dynamic Range & Power vs. Supply Voltage



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1.8-V CMOS ΣΔ Modulator Performance

Dynamic range	99 dB
Peak SNR	99 dB
Peak SNDR	95 dB
Bandwidth	25 kHz
Oversampling ratio	80
Power dissipation	2.5 mW
Active area	1.5 mm^2
Technology	0.8-μm CMOS
Threshold voltages	+0.65 V, –0.75 V

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Power Efficiency Figure of Merit

- Power efficiency as a Figure of Merit:

$$\text{FoM} = \frac{\text{Dynamic Range} \times \text{Bandwidth}}{\text{Power}}$$

$$= \frac{2^{2N} \times \text{BW}}{\text{Power}} \quad (\text{MHz}/\text{mW})$$

where Dynamic Range is a POWER, not voltage, ratio
N = effective # of bits of resolution

- For circuits in which the dynamic range is limited by thermal noise and the bandwidth is not limited by technology:
  - Quadratic dependence on voltage dynamic range
  - Linear dependence on bandwidth

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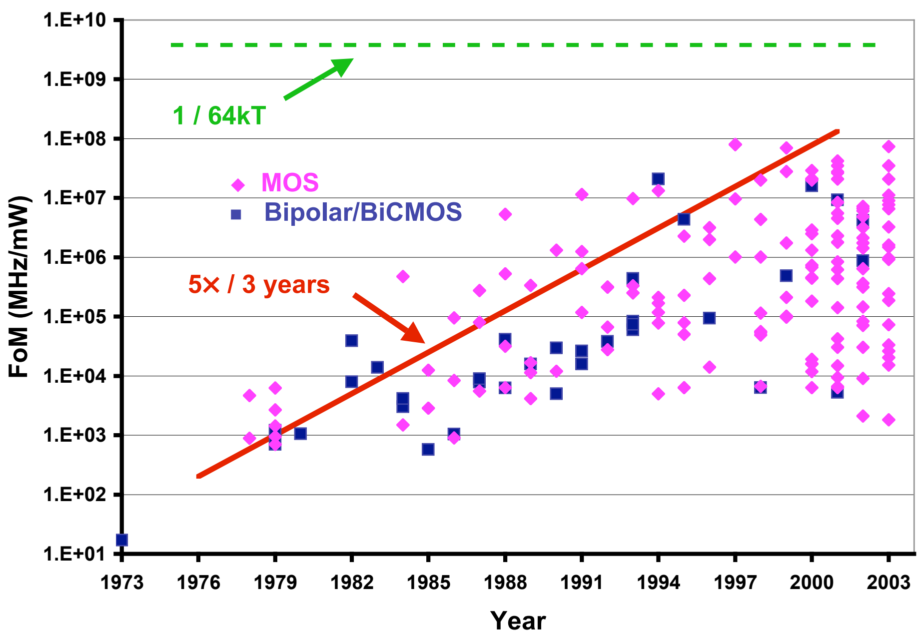
ADC Power Efficiency



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Low-Voltage Broadband ΣΔ Modulation *

- **Target objective is low-voltage, high-resolution broadband A/D conversion for applications such as ADSL, CDMA 2000, IS-95, and GSM**

- **Objectives**
  - **Conversion rate** — **2.5 MSample/s**
  - **Dynamic range** — **92 dB (15 bits)**
  - **Power supply** — **1.2V**
  - **Power dissipation** — **~ 80 mW**
  - **Technology** — **0.25-μm CMOS**

*** K. Nam, 2004 CICC**

Analog Challenges @ Low V_{DD}

- Reduced voltage headroom
- Limited choice of op amp topologies
- Dynamic range decreases unless noise floor is reduced
  - ∴ Low-voltage analog ⇨ high power
- In this work consider architecture and circuits needed to achieve low voltage and low power

Low-Voltage, Low-Power Strategies

- Low oversampling ratio & high-order modulator
- Maximize the full-scale input amplitude for a given V_{DD}
- Multi-bit quantization
- Single-stage op amps
- Linear integrator settling
  - allows use of slower op amps

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Architectural Decisions

- **Single-bit or multi-bit quantization ⇨ multi-bit**
  - single-bit feedback causes op amp slew ⇨ need fast op amp
  - single-bit quantization results in larger quantization noise leakage into the output in cascaded modulators
- **Single-quantizer or cascade ⇨ cascade**
  - Even with multi-bit quantization op amp slewing can limit performance of a high-order single-quantizer modulator ⇨ use 2nd-order modulator for first stage
  - 2-2 cascade with 5-bit and 3-bit quantizers

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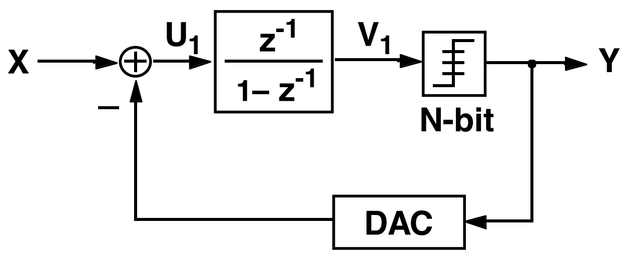
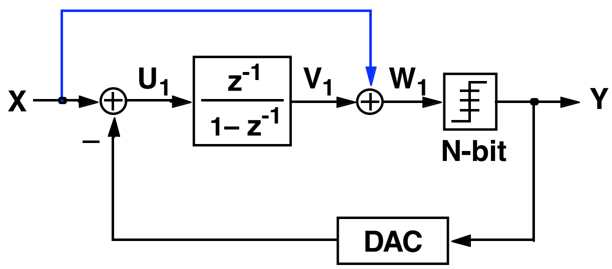
Conventional First-Order ΣΔ Modulator



$$Y = z^{-1}X + (1 - z^{-1})E$$

- $U_1 = (1 - z^{-1})X - (1 - z^{-1})E$ ⇨ magnitude depends on input amplitude and frequency
- $V_1 = z^{-1}X - z^{-1}E$ ⇨ magnitude depends on input
- Op amps designed to ensure minimum SNDR degradation for large signals ⇨ inefficient power allocation

Reduced Integrator Swing-Range ΣΔ Modulator



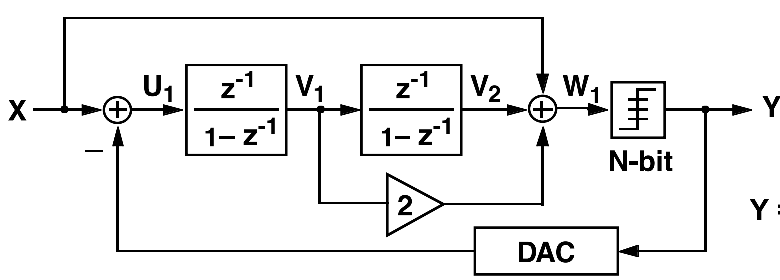
$Y = X + (1 - z^{-1})E$

- $U_1 = -(1 - z^{-1})E$ ⇨ $|U_1| \le$ LSB

  $V_1 = -z^{-1}E$ ⇨ $|V_1| \le 0.5$ LSB

  U_1 & V_1 are DECOUPLED from the input X ⇨ attractive at low V_{DD}
- $W_1 = X - z^{-1}E$ ⇨ swing-range burden is moved to W_1
- Approach can be extended to higher-order modulators

Second-Order RISR ΣΔ Modulator

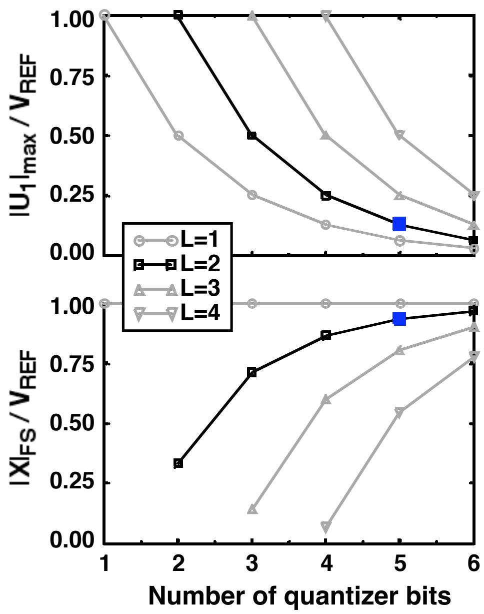


$Y = X + (1 - z^{-1})^2E$

- $U_1 = -(1 - z^{-1})^2E$ ⇨ $|U_1| \le 2$ LSB
- $V_1 = -z^{-1}(1 - z^{-1})E$ ⇨ $|V_1| \le$ LSB
- $V_2 = -z^{-2}E$ ⇨ $|V_2| \le 0.5$ LSB
- $W_1 = X + z^{-1}(z^{-1} - 2)E$

* J. Silva, Elec Letters, June 2001

Trade-Offs in RISR ΣΔ Modulators



$$U_1 = -(1 - z^{-1})^L E$$

L = 2 & N = 5 for first stage

For $V_{REF} = 1.2V$,
$|X|_{FS} = 1.1V$
$|U_1|_{max} = 150mV$
$|V_1|_{max} = 75mV$
$|V_2|_{max} = 37.5mV$

$$|X|_{FS} = \left(\frac{2^N - (2^L - 1)}{2^N - 1}\right) V_{REF}$$

Implementation Issues

- **Integrator op amp:** requirements are greatly relaxed
  - small input signal range
    - linear settling dominates
    - slow op amp can be used ⇨ power saving
  - relaxed dc gain requirement
  - small output range
- **Quantizer:** more stringent requirements
  - multiple signals summed at quantizer input
  - offset
    - increases swing ranges
    - need offset cancellation
  - very fast regeneration needed since latch must be strobed after sampling of the input is complete

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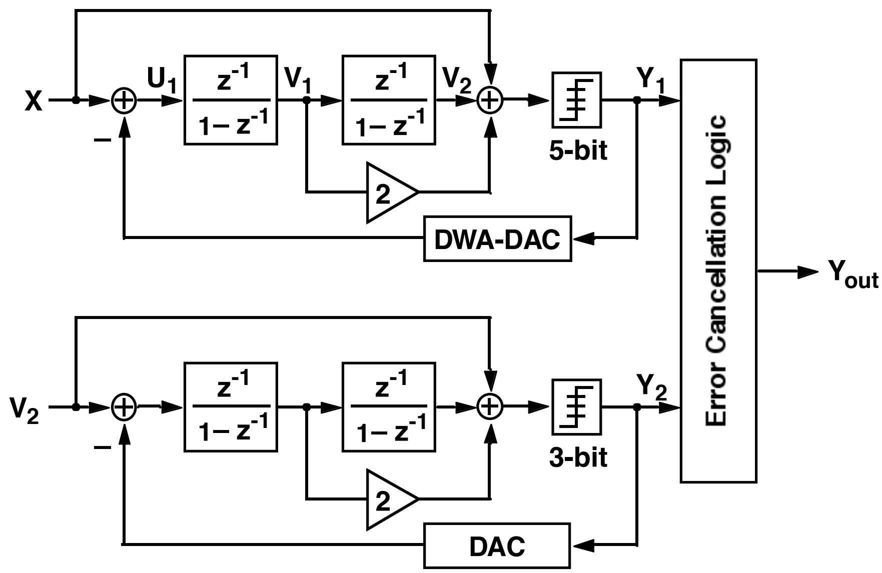
Experimental Prototype



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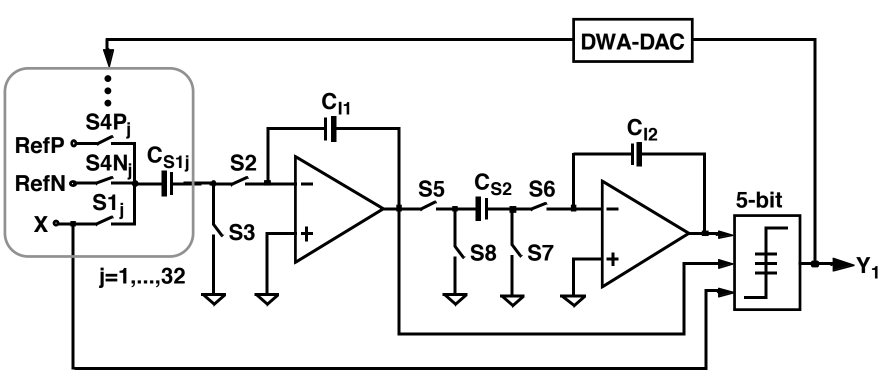
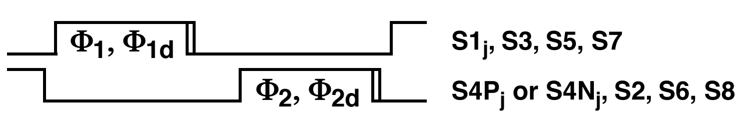
First-Stage Implementation *





* actual implementation is fully differential

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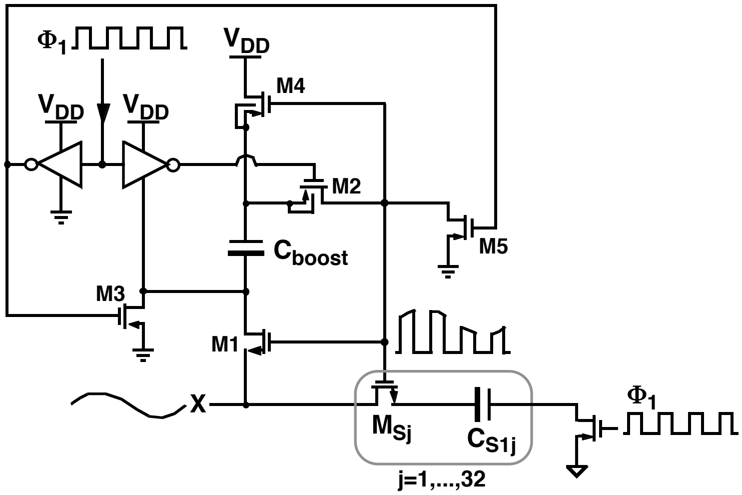
Low Distortion Input Sampling *



* M. Dessouky, JSSC, March 2001

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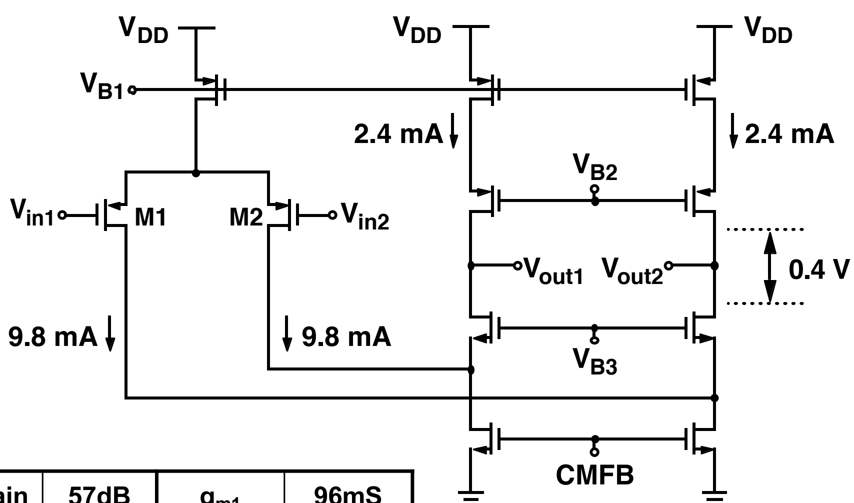
First Op Amp



Dc gain	57dB	g_{m1}	96mS
Power	29mW	BW_{CL}	122MHz
V_{CM}(in)	0.15mV	V_{CM}(out)	0.65V

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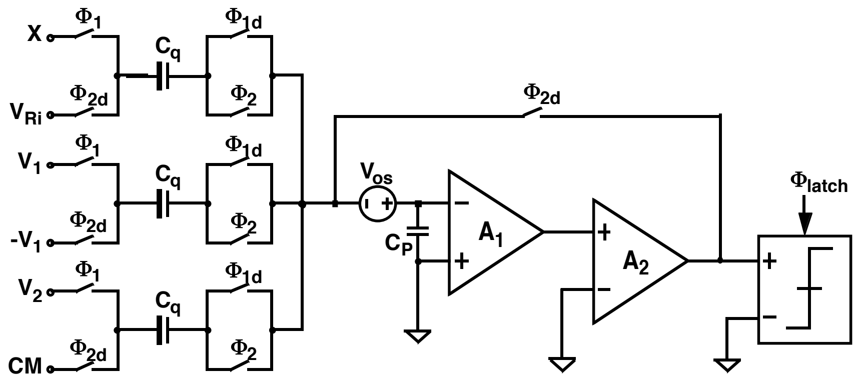
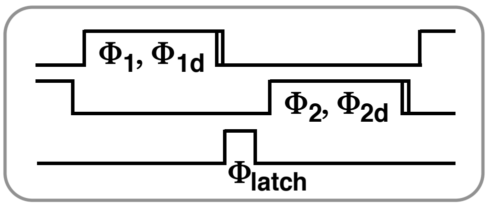
Quantizer Comparator (1 of 32)





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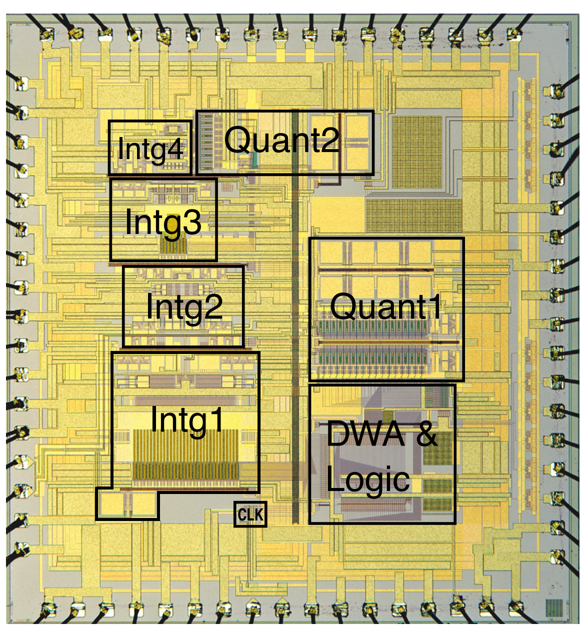
Prototype Die Photo



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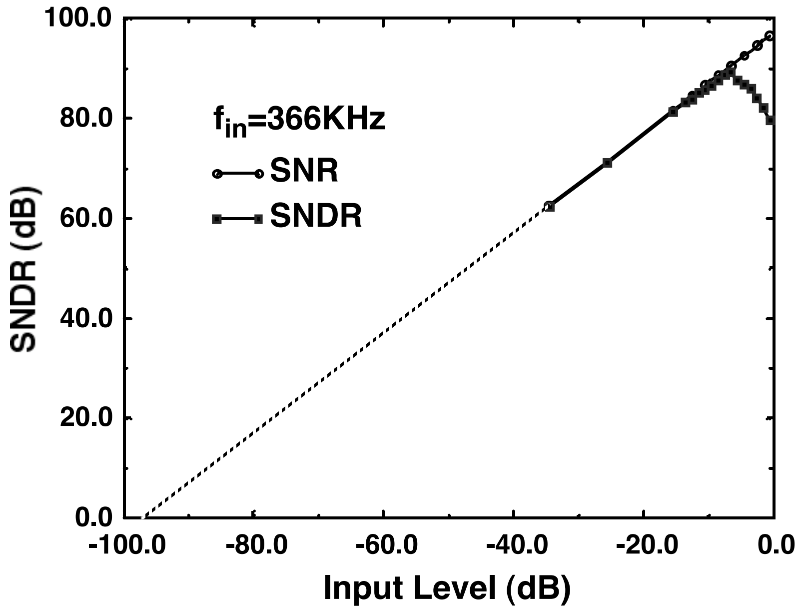
Measured SNR and SNDR



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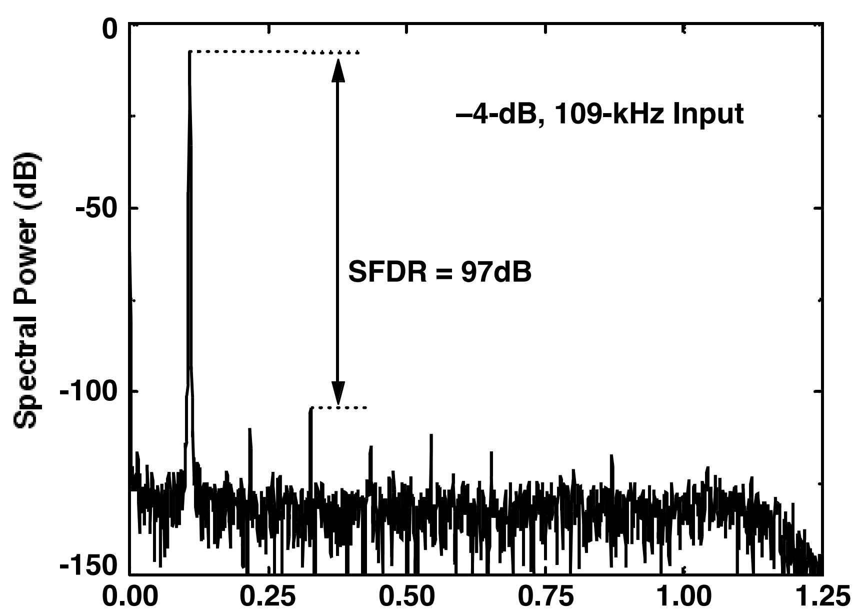
Measured Output Spectrum



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Performance Summary

Analog Supply Voltage	1.2 V
Sampling Rate	40 MHz
Signal Bandwidth	1.25 MHz
Dynamic Range	96 dB
Peak SNDR @ 366-kHz input	89 dB
Analog Power	44 mW
Digital Power	43 mW *
Active Area	8.6 mm^2
Technology	0.25-μm CMOS

* Estimate 10 mW digital power in 0.13-μm CMOS

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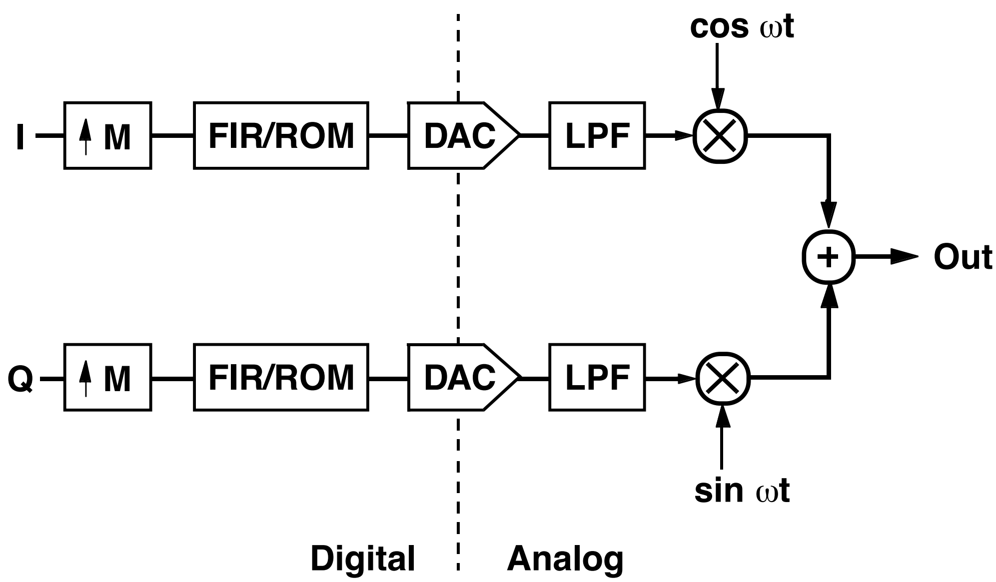
Bandpass Oversampling D/A Conversion *

- Consider the use of cascaded noise shaping for bandpass D/A conversion in RF transmitters
- Move IF into the digital domain to eliminate
  - dc offset
  - I & Q mismatch
- Merge D/A conversion, noise shaping, reconstruction and mixing to IF
- Explore the use of cascaded noise shaping with semi-digital filtering

* D. Barkin, 2003 VLSI Ckts Symp

Traditional Wireless Transmitter Architecture



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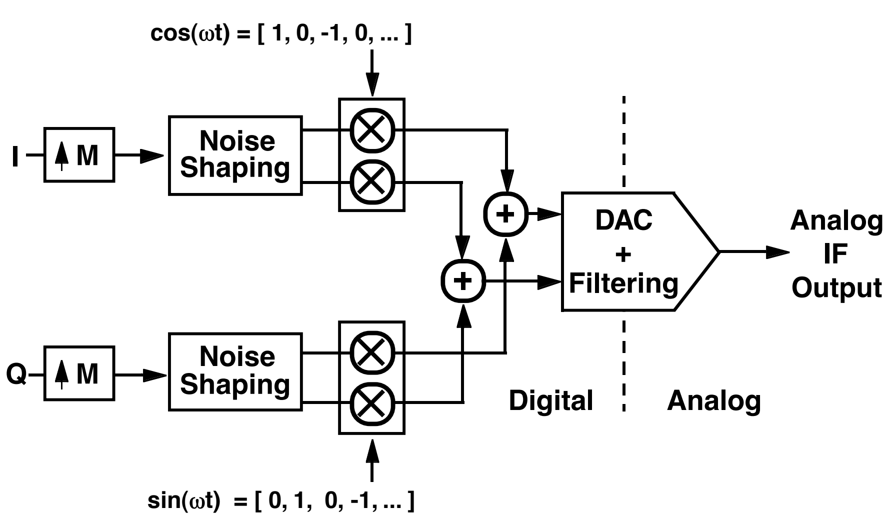
Bandpass Oversampling DAC



- Mix to IF (at $f_S/4$) following cascaded noise shaping
- Error cancellation performed at IF

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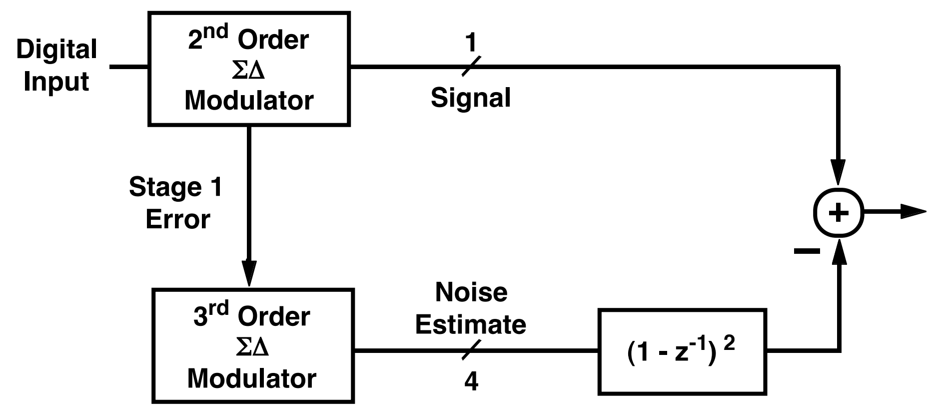
Lowpass Cascaded Noise Shaping



- 2nd-order differentiator matches noise shaping in first stage

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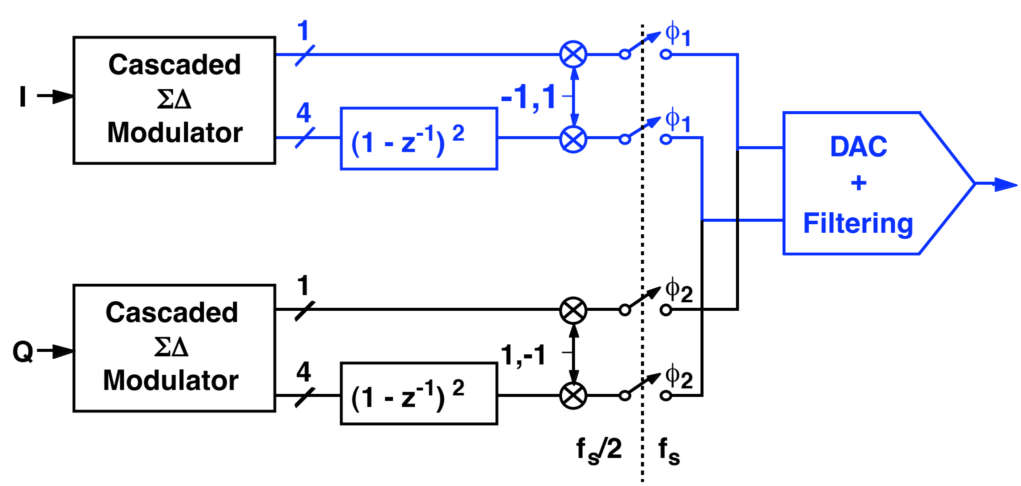
Bandpass DAC Architecture



- I and Q modulators operate at $f_S/2$, saving power

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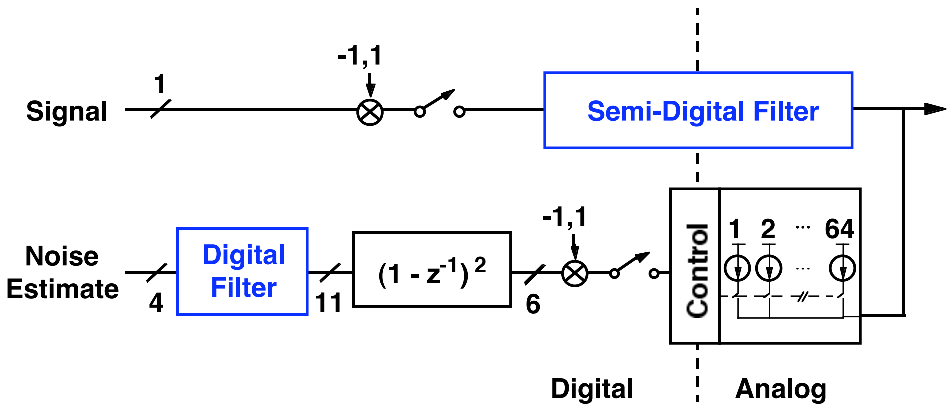
Discrete Time - Continuous Time Interface



- Semi-digital filtering for reconstruction of signal
  - Good for 1-bit signal path, but not multi-bit noise estimation path
- Digital filter reduces out-of-band quantization noise
- Digital filter transfer function matches that of semi-digital filter

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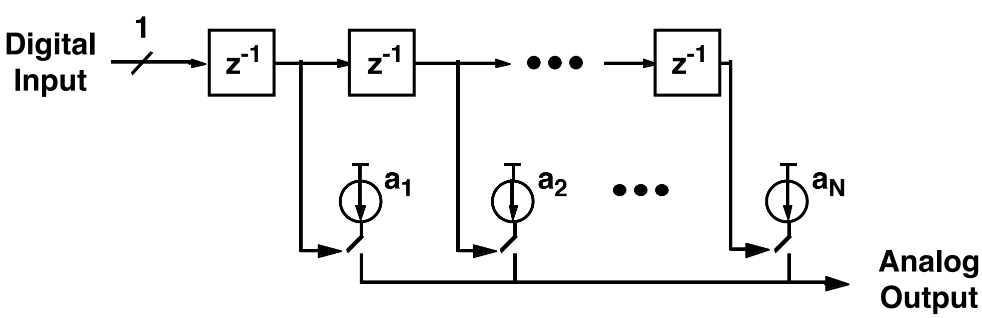
Semi-Digital Filter *



- Mismatch among current sources alters the transfer function but doesn't introduce nonlinearity
- Area limits number of taps and precision of coefficients
- Good for 1-bit signal path but not multi-bit noise estimation path

* D. Su, et al., JSSC, Dec. 1993

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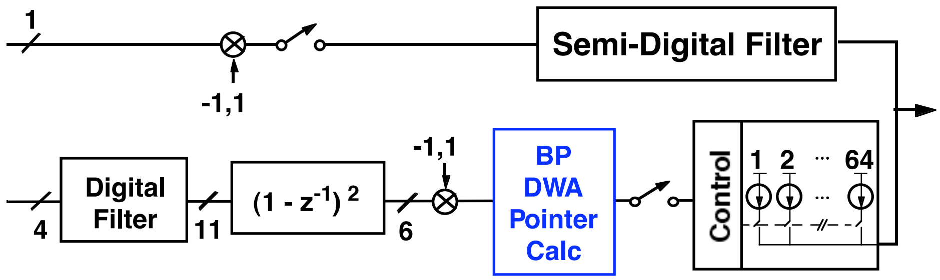
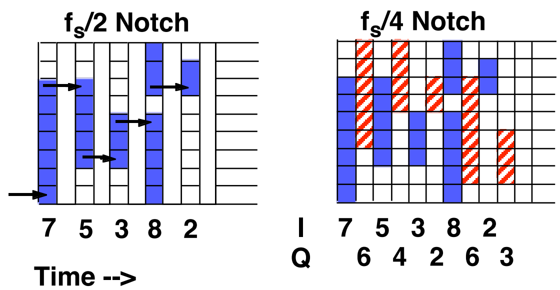
Bandpass Data Weighted Averaging *





I & Q pointer calculations are independent

* T. Shui, et al., ISCAS, 1998

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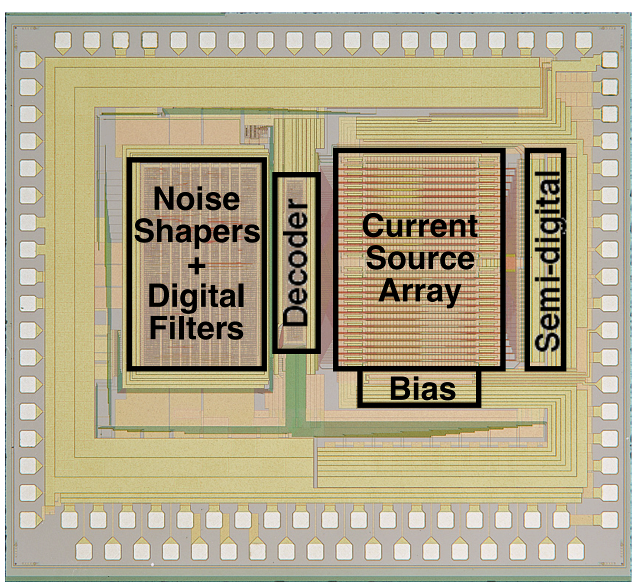
Bandpass DAC Die Photo



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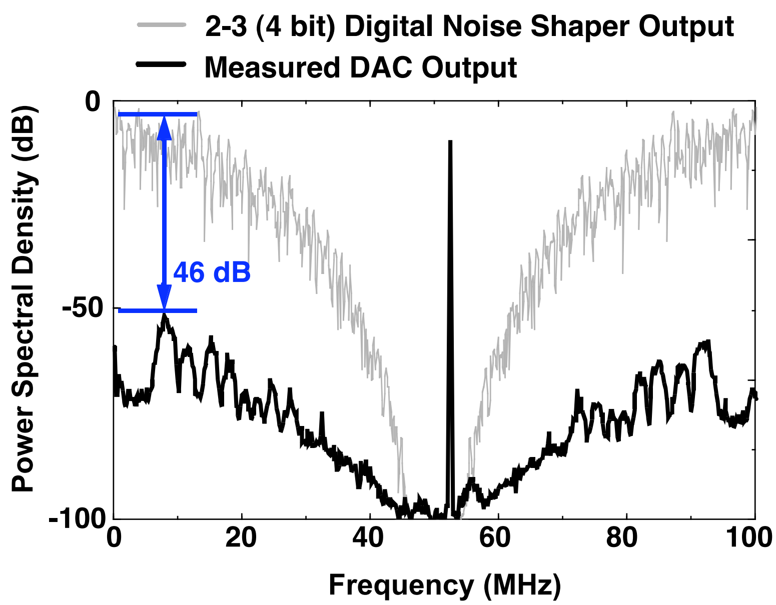
DAC Output Spectrum



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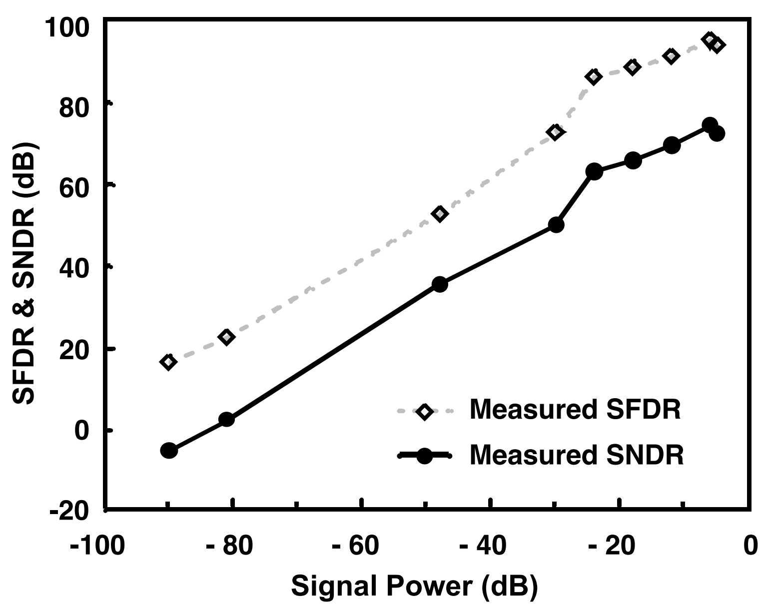
SNR and SNDR



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Bandpass DAC Performance

Technology	0.25-μm CMOS
Center frequency	50 MHz
Bandwidth	6.25 MHz
Peak SNDR	76 dB
Dynamic range	85 dB
Minimum out-of-band suppression	80 dB
Mirror for –6 dB Input	–90 dB
Active area	2.1 mm^2
Power (except for current sources)	100 mW

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Summary

- **Cascades of first- and second-order noise-shaping modulator stages can be used for**
  - A/D and D/A conversion
  - lowpass and bandpass data conversion
- **If properly designed, advantages include**
  - no potential instability
  - decorrelation of quantization noise and input
  - low sensitivity to analog precision
- **Still room for architectural and circuit innovation to meet the challenges presented by**
  - technology scaling to sub-100nm dimensions
  - performance demands of new applications

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