# Digitally Assisted A/D Conversion-Trading off Analog Precision for Computing Power

SCV SSC Chapter Meeting

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# Outline

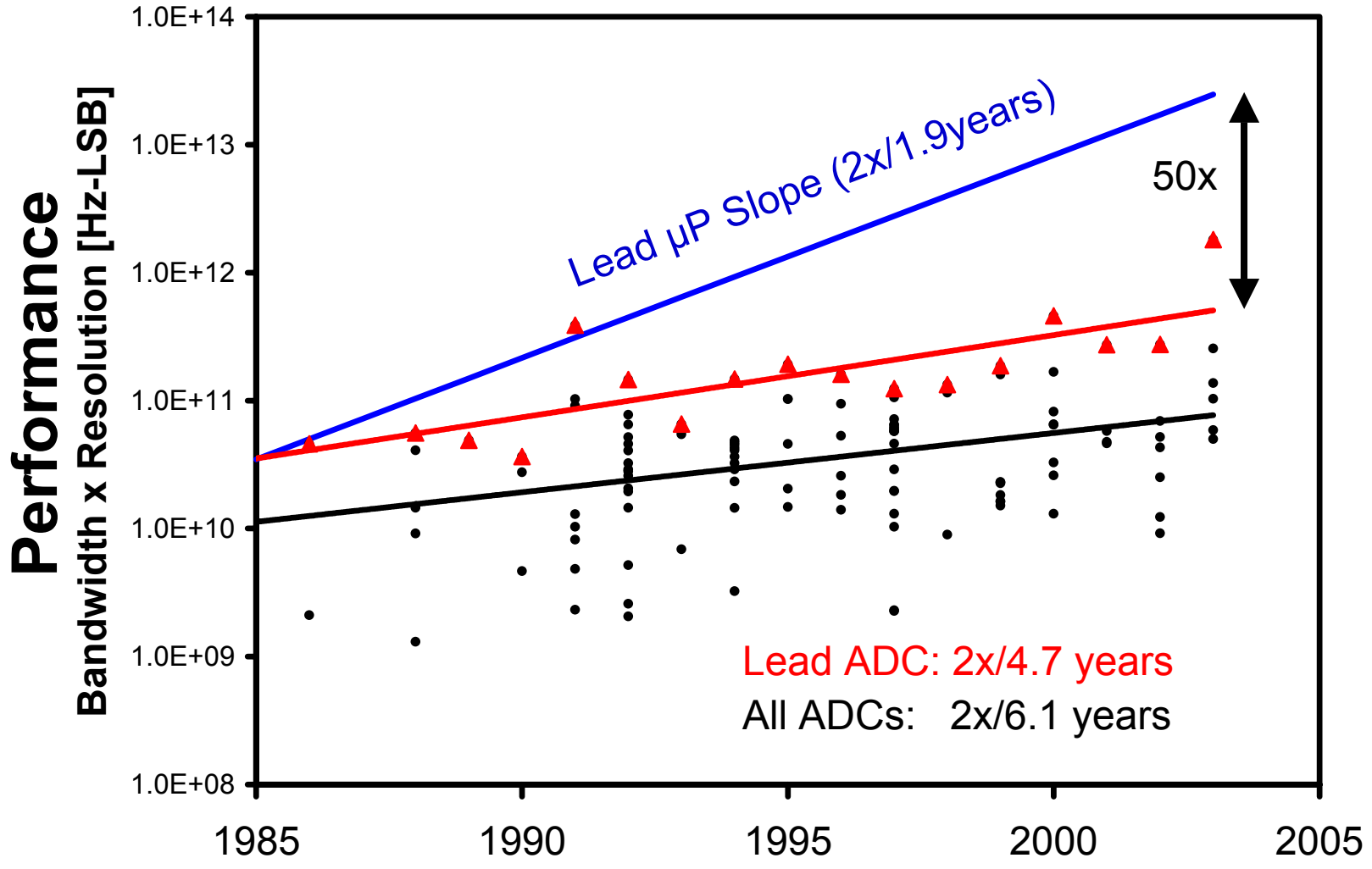
- Motivation
- Digitally Assisted Pipelined ADC
  - Circuit Concepts
  - Experimental Results
- Other Work & Future Opportunities
- Conclusion

# “The Digital Revolution“

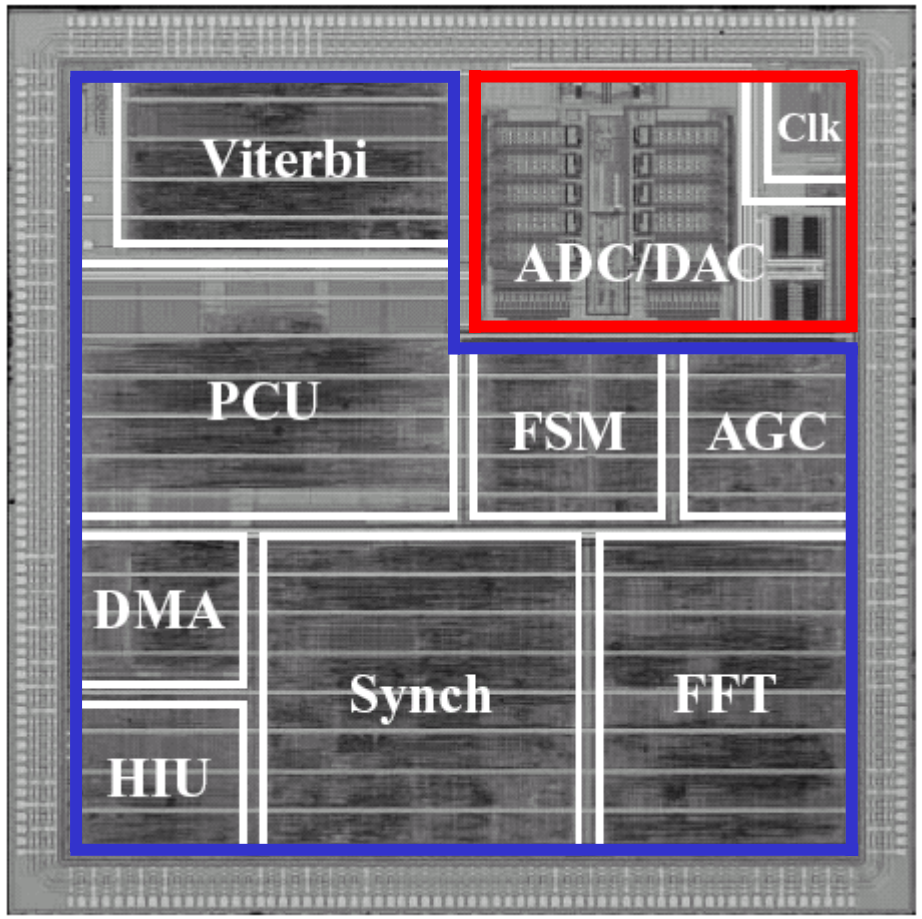
| | 1974 | 2002 | Rate of Change |
|---|---|---|---|
| Transistor Feature Size | 6μm | 0.13μm | 0.7x every 2-3 years |
| Lead μP Transistors/die | 5000 | ≈200,000,000 | 2x every 1.8 years |
| Lead μP Peformance | 0.3 MIPS | ≈10,000 MIPS | 2x every 1.9 years |

[Moore, ISSCC 2003]

# ADC vs. µP Performance



# Modern Application

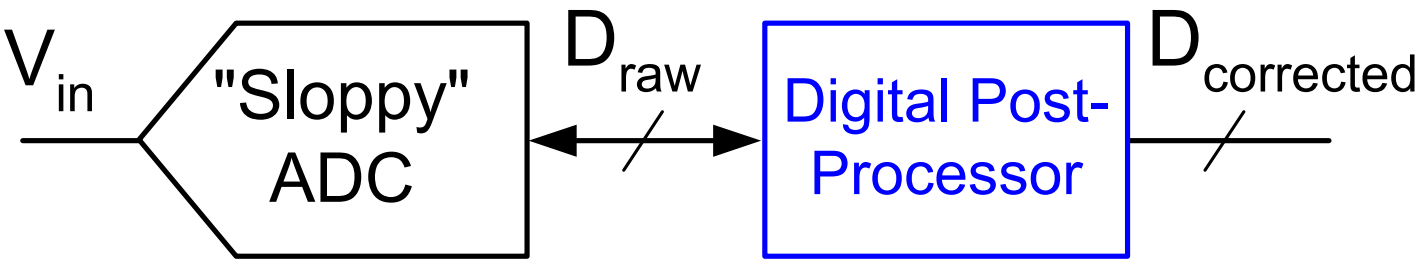



50% $P_{tot}$ (ADC only)

4 Million Transistors

802.11 Baseband Processor
[Thomson et. al., ISSCC 2002]

# Proposed Approach




- Relax analog domain precision & complexity
  - ⇒ Reduced power consumption
  - ⇒ Improved deep sub-μm compatibility
  - ⇒ Higher speed (?)
- Recover conversion accuracy in digital domain
- “Digitally Assisted A/D Conversion”

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    - Analog Errors & Digital Compenstion
    - Correction Parameter Estimation & Tracking
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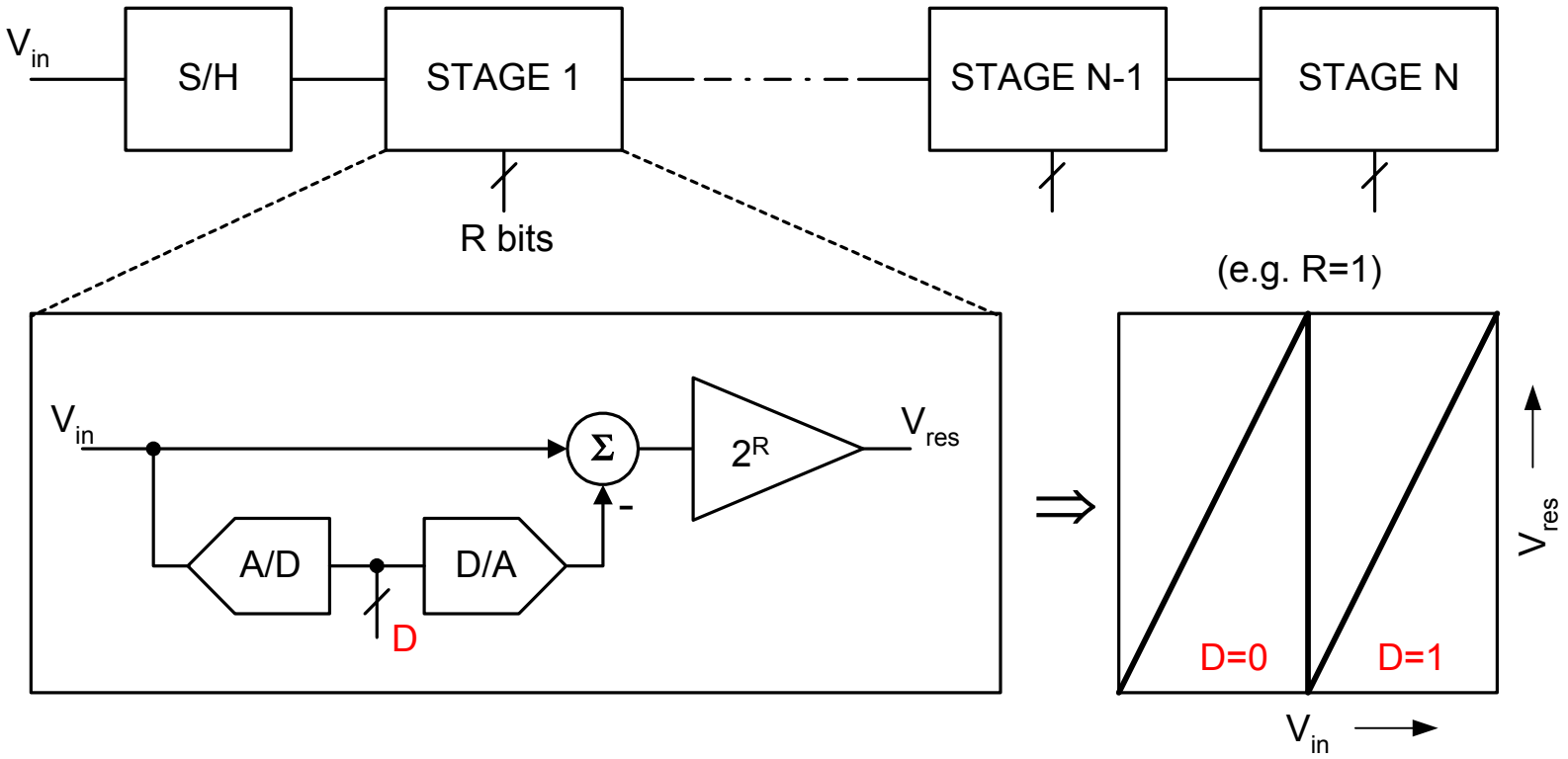
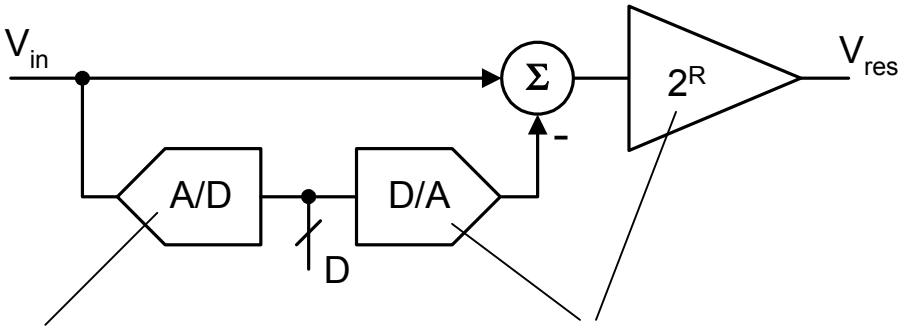
# Generic Pipelined ADC




- Predominant topology for wide performance range: 10-14 bits, 10-200MHz

# Relax Analog Precision?




"Digital correction" helps tolerate large sub A/D errors [Lewis, 1987]

"Digital calibration" removes D/A and linear gain error by adjusting digital weights [Karanicolas, 1993]

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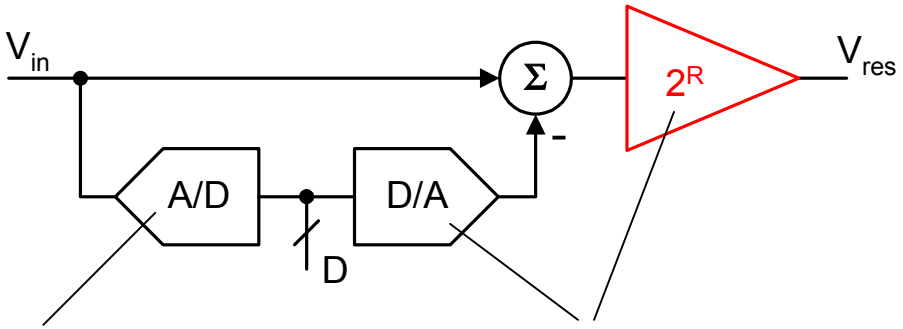
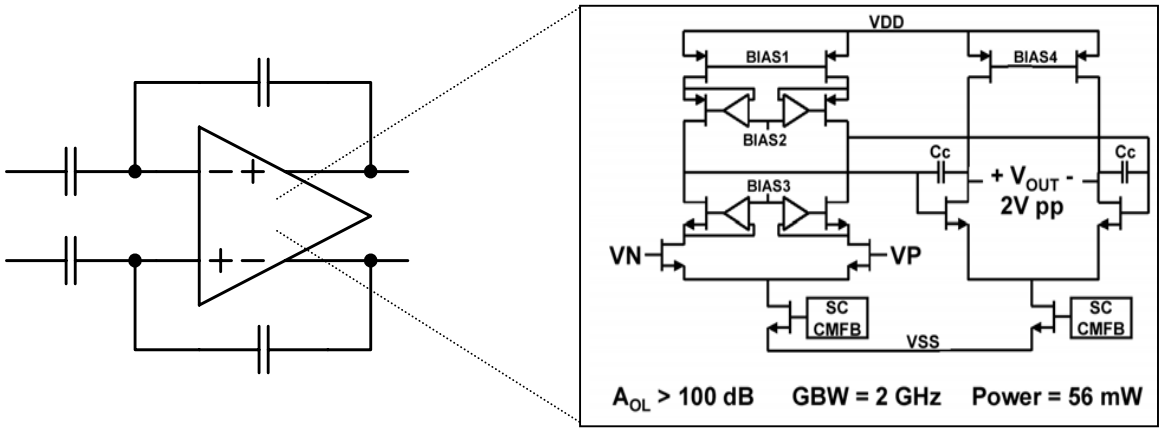



"Digital correction" helps tolerate large sub A/D errors [Lewis, 1987]

"Digital calibration" removes D/A and linear gain error by adjusting digital weights [Karanicolas, 1993]

- Remaining burden: Fast, highly linear gain element
- 50-70% of total pipeline ADC power is consumed by interstage amplifiers

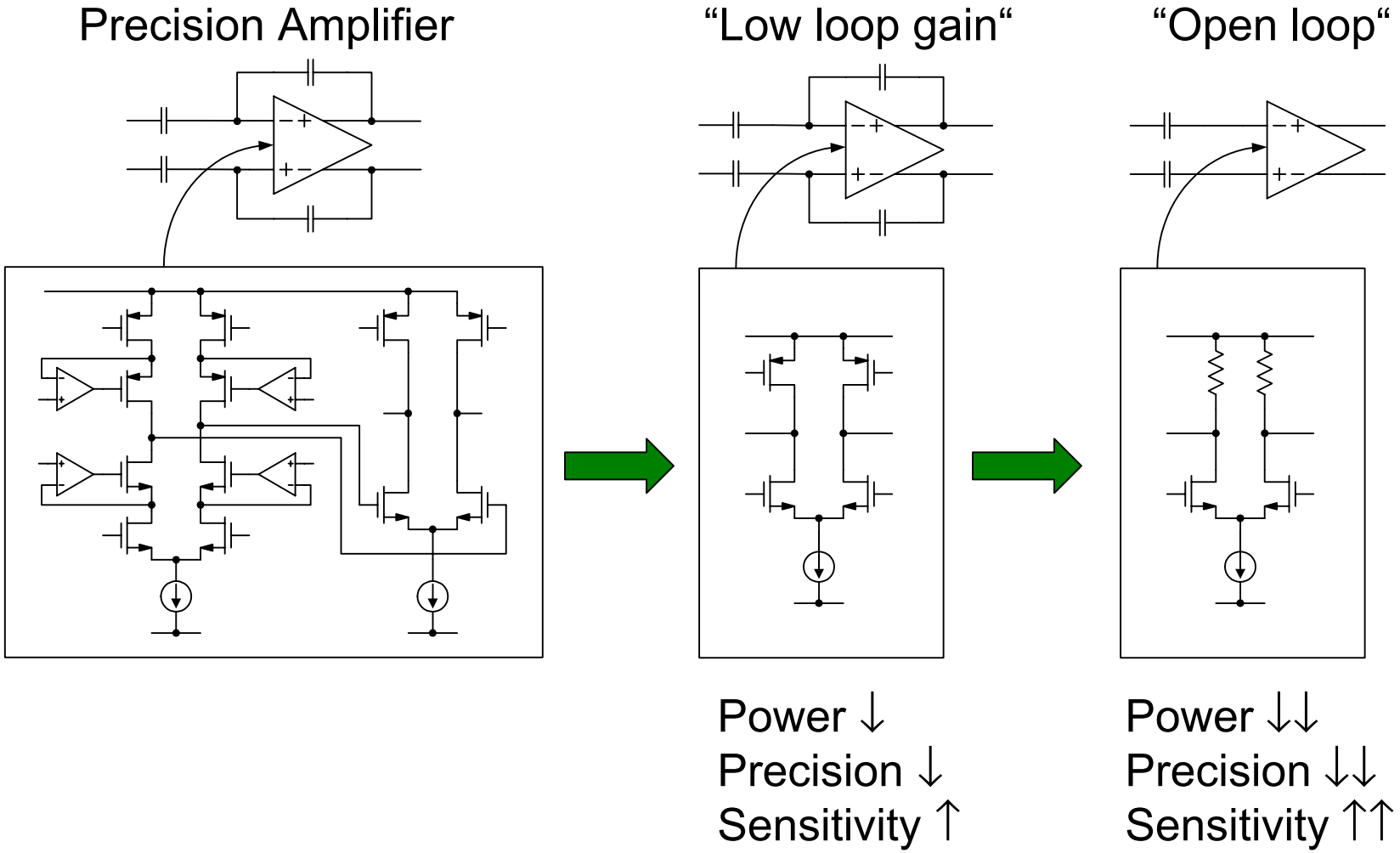
# Conventional Gain Element



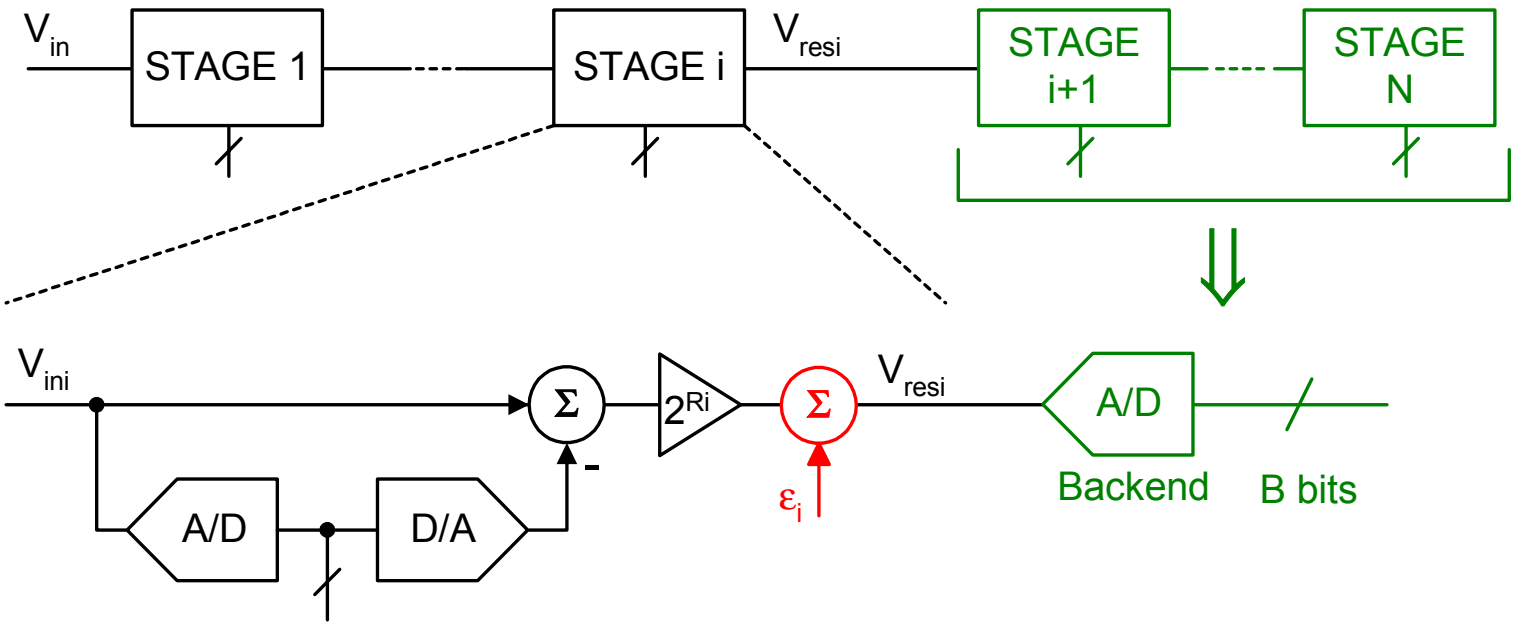

E.g. [Kelly, ISSCC 2001]

- Electronic feedback linearizes, desensitizes
- High gain requirement costs headroom and/or additional stages $\Rightarrow$ power penalty
- Semiconductor technology trend: Decreasing VDD and low intrinsic device gain!

# Alternatives

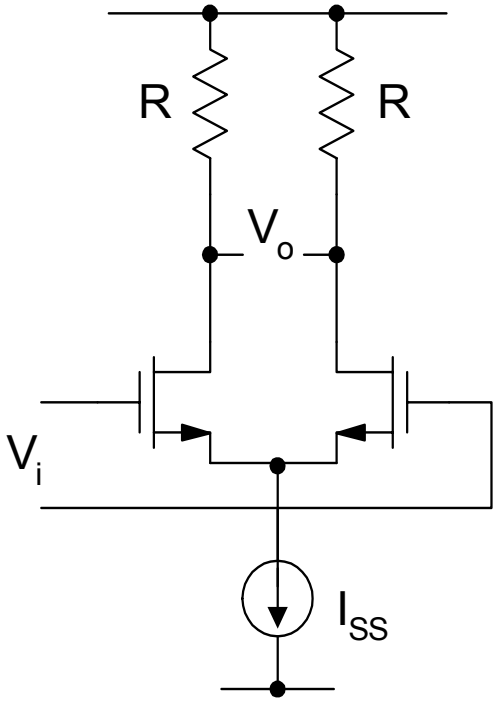


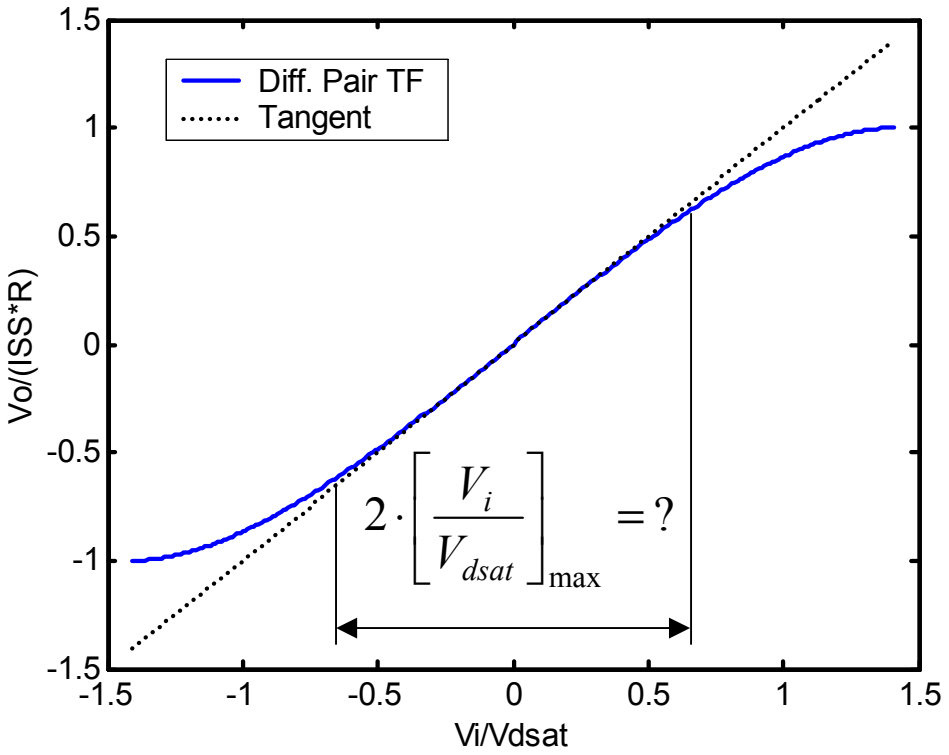
# Precision Requirements




- Residue errors must be < ½ LSB of "backend converter"
- E.g. 3-bit Stage1 in 12-bit converter $\Rightarrow$ 9-bit backend
  $\Rightarrow \varepsilon_1 < 0.1\%$

# Basic Amplifier Considerations



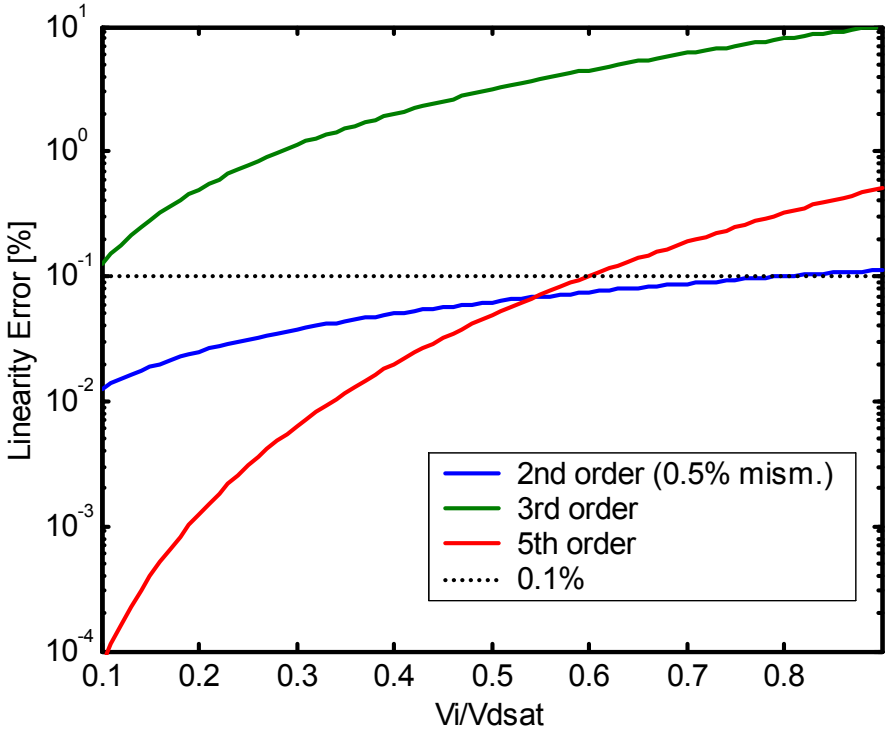




- Example: Simplest possible topology
- What fraction of transfer function should be used?

# Transfer Function Nonlinearity

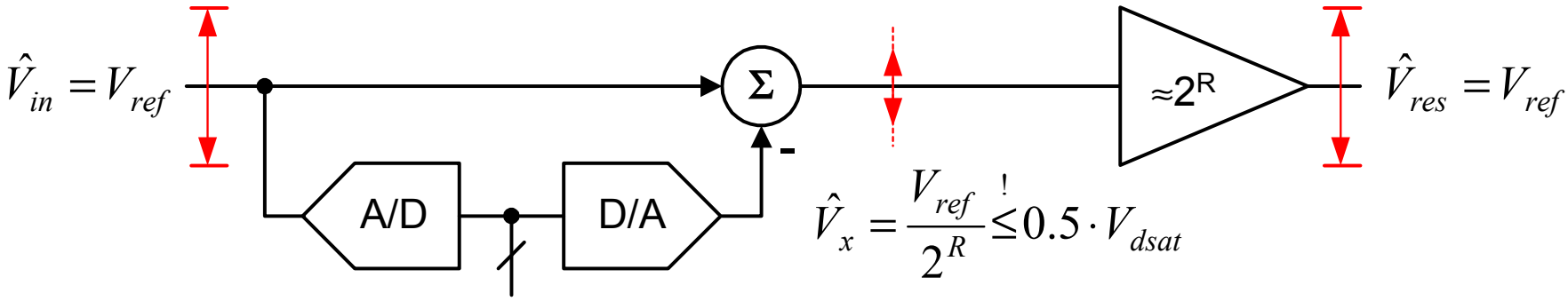
$$\frac{V_0}{I_{SS}R} = \left(\frac{V_i}{V_{dsat}}\right) + \frac{1}{4}\frac{\Delta\beta}{\beta}\left(\frac{V_i}{V_{dsat}}\right)^2 - \frac{1}{8}\left(\frac{V_i}{V_{dsat}}\right)^3 - \frac{1}{128}\left(\frac{V_i}{V_{dsat}}\right)^5 - \ldots$$

2nd order (Device Mismatch) 3rd order 5th order (Gain Compression)




- 3rd order error unavoidable
- 5th and higher order error small for $|V_{imax}| \leq 0.5V_{dsat}$
- Desirable to neglect high order terms
- Design implications?

# Design Example

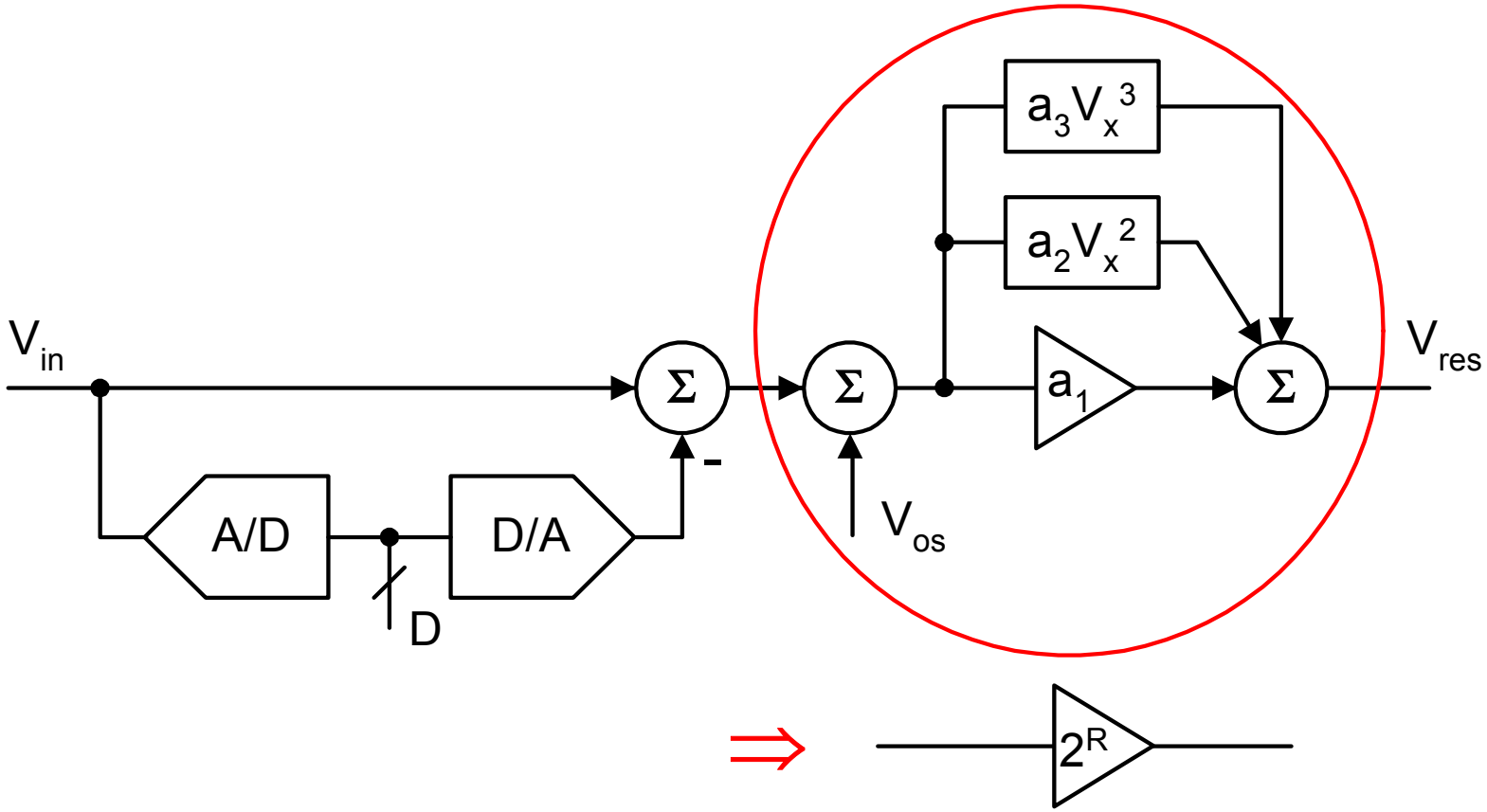



| $V_{ref}$ | R | $\hat{V}_x$ | $V_{dsat}$ | |
|---|---|---|---|---|
| 1V | 1 | 500 mV | ≥ 1V | ✗ |
| | 2 | 250 mV | ≥ 500 mV | ✗ |
| | 3 | 125 mV | ≥ 250 mV | ✓ |
| | 4 | 62.5 mV | ≥ 125 mV | ✓ |

(headroom, $g_m/I_D$)

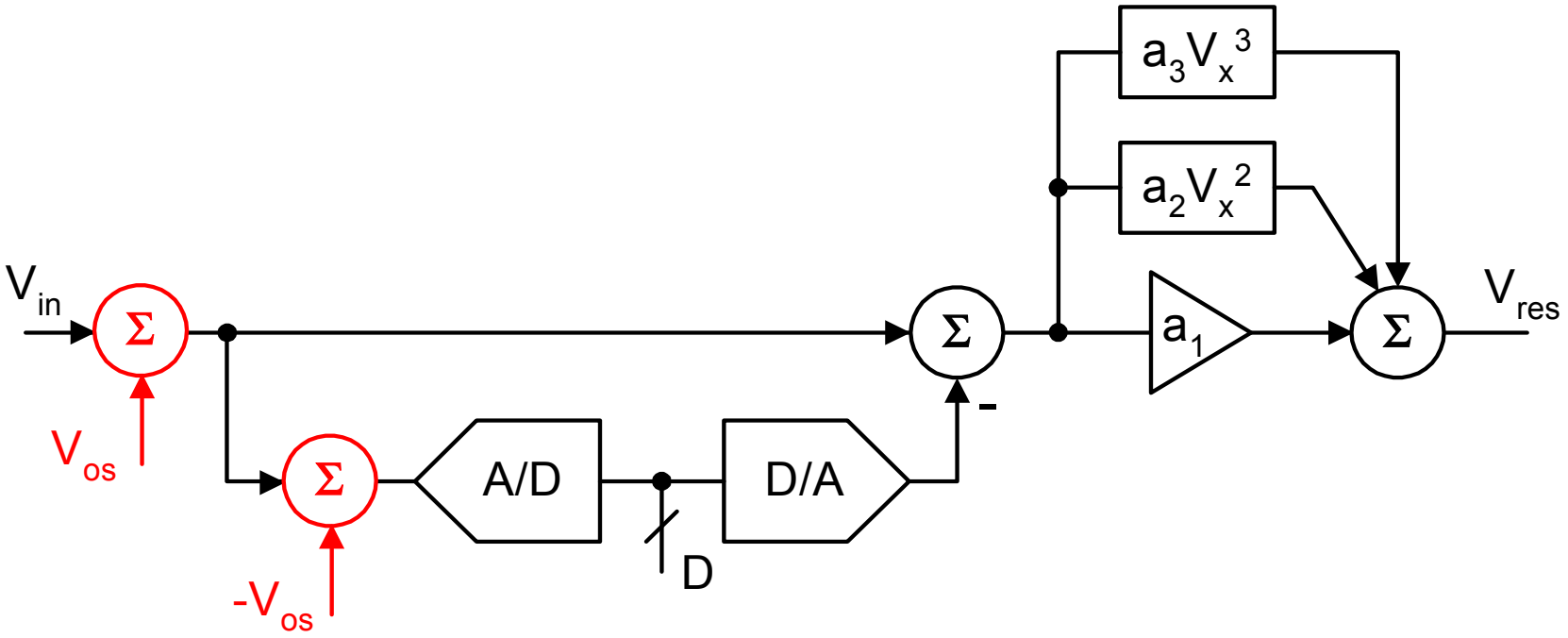
- Simple diff. pair “practical“ for stage resolution R>2
- Third order error model sufficient in this case

# Pipeline Stage Model



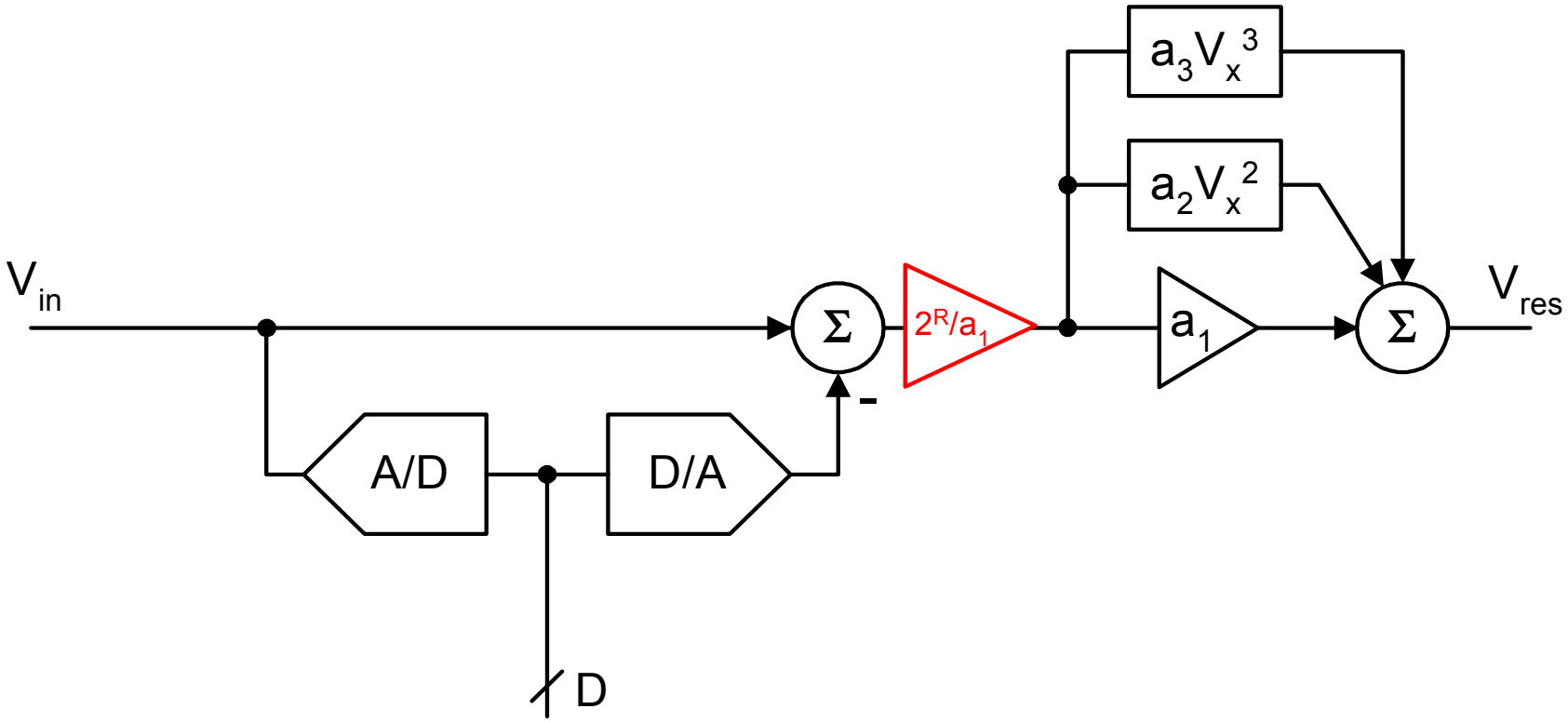

- How can we correct errors digitally ?

# Offset Pushthrough

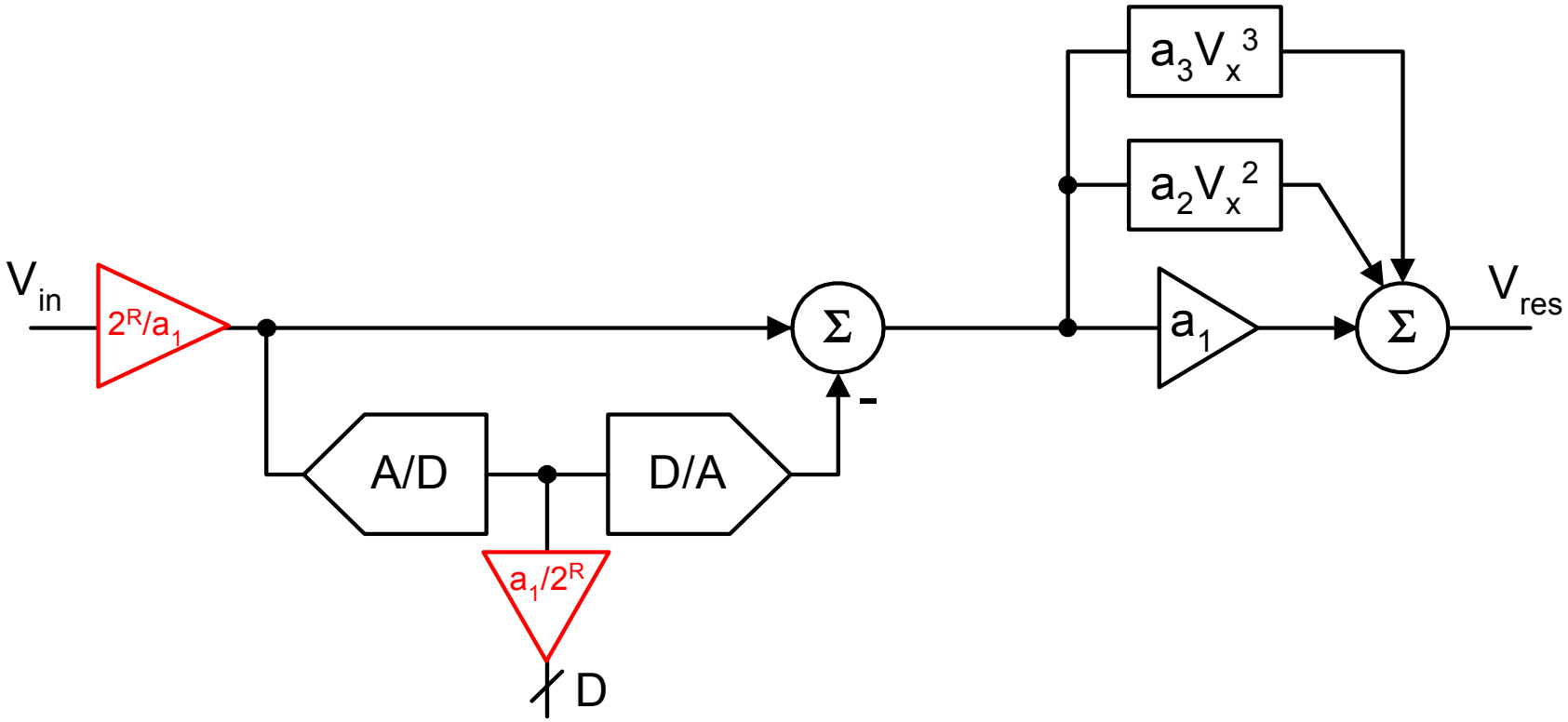



- Input referred converter offset, does not harm linearity
- Equivalent sub-A/D offset can be addressed with digital RSD arithmetic [Lewis, 1987]

# Gain Error Pushthrough

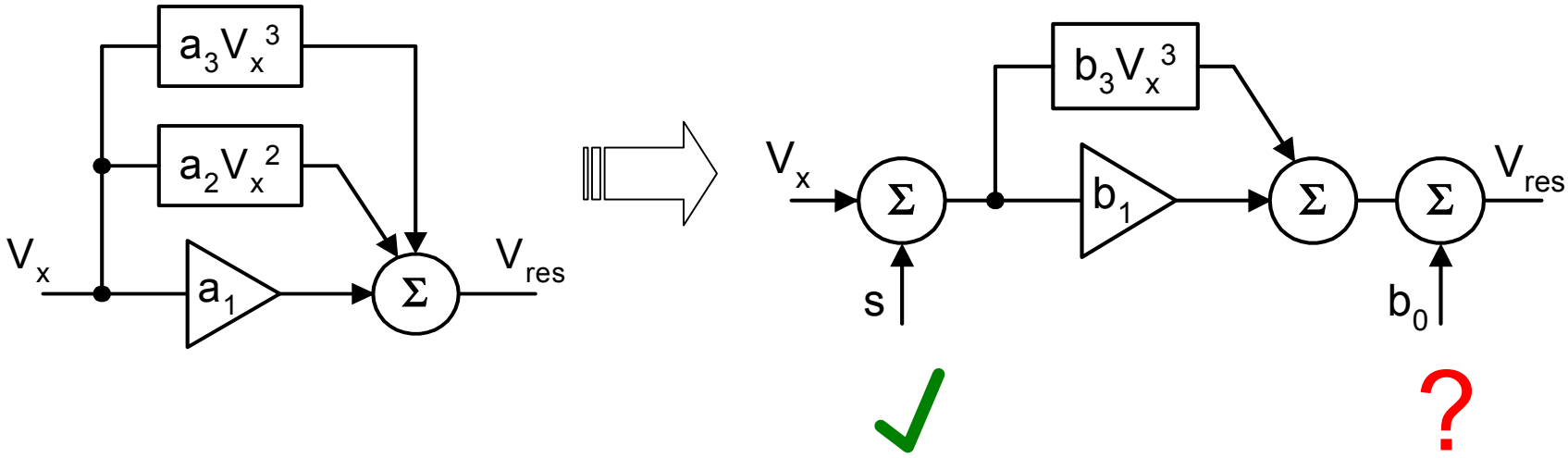


# Gain Error Pushthrough




- Correct digital weight of sub-conversion [Karanicolas, 1993]
- Results in (often) tolerable input referred gain error

# Second Order Cancellation

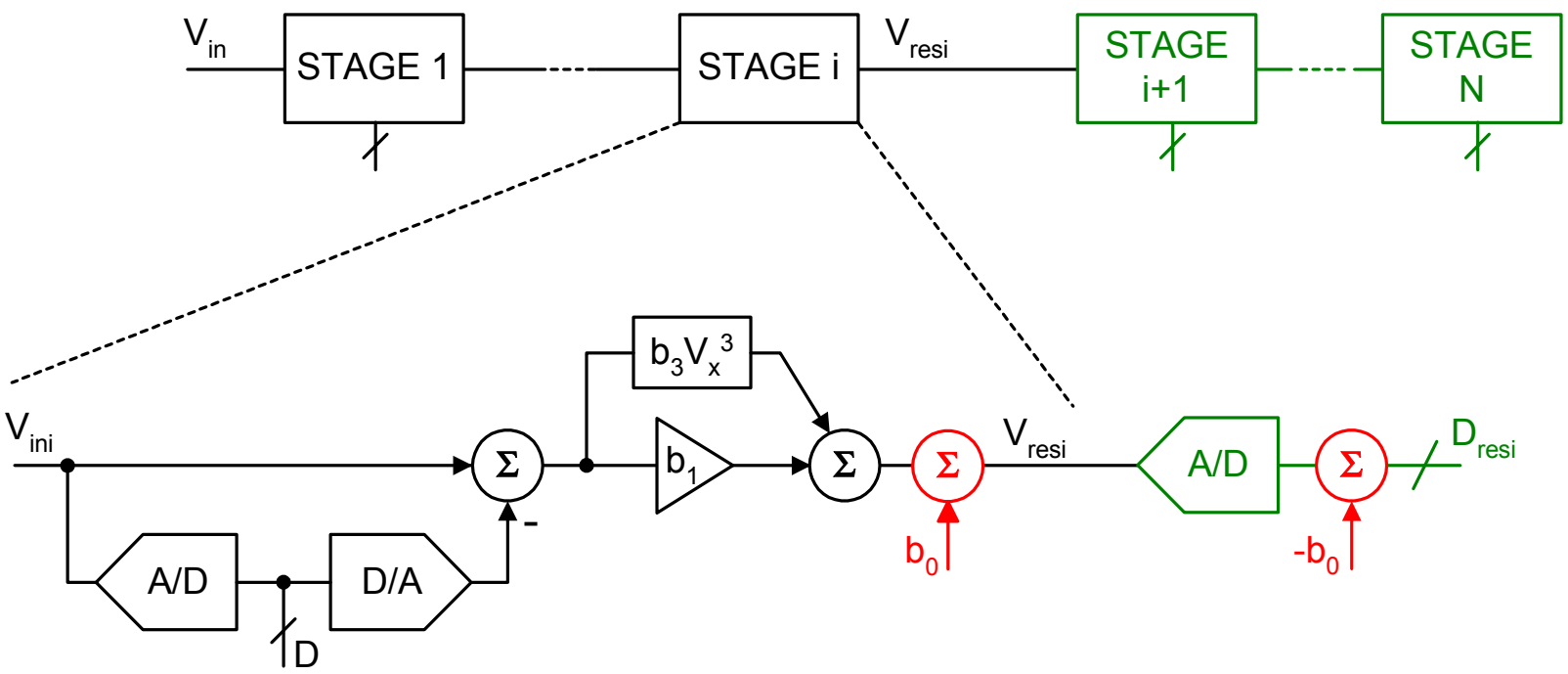



If $a_3 \neq 0$:

$$a_1 x + a_2 x^2 + a_3 x^3 = b_0 + b_1 (x - s) + b_3 (x - s)^3$$

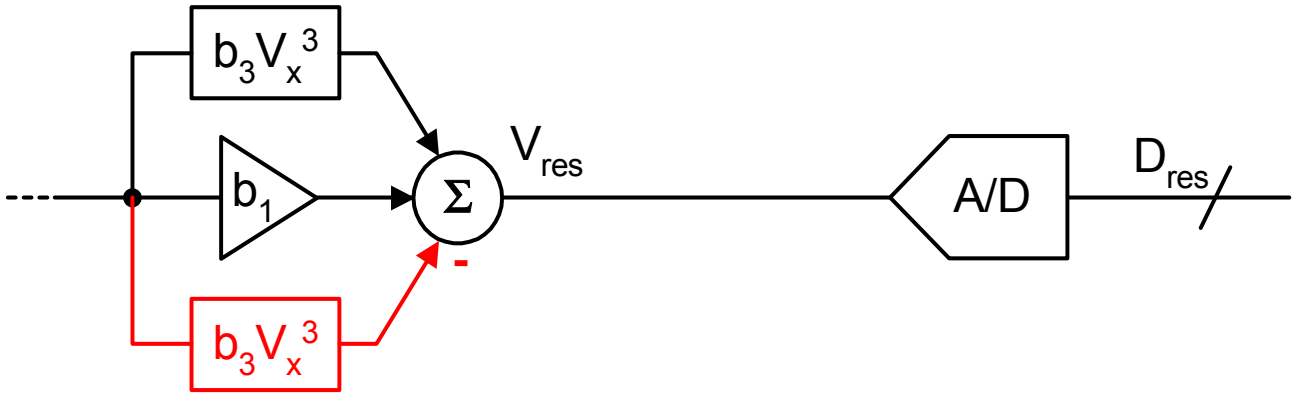
$$\left[ With: \quad b_3 = a_3 \quad b_1 = a_1 - \frac{a_2^2}{3a_3} \quad b_0 = \frac{2a_2^3}{27a_3^2} - \frac{a_1 a_2}{3a_3} \quad s = \frac{a_2}{3a_3} \right]$$

# Use of Digitized Residue




- Compensate error using digital backend representation of residue
- Add 1-2 bits to backend to reduce quantization error

# Third Order Correction



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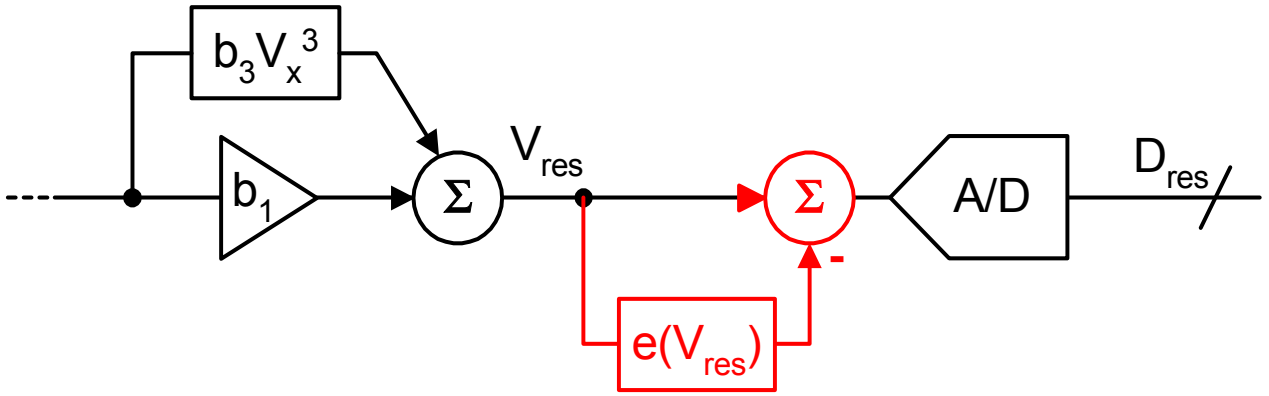
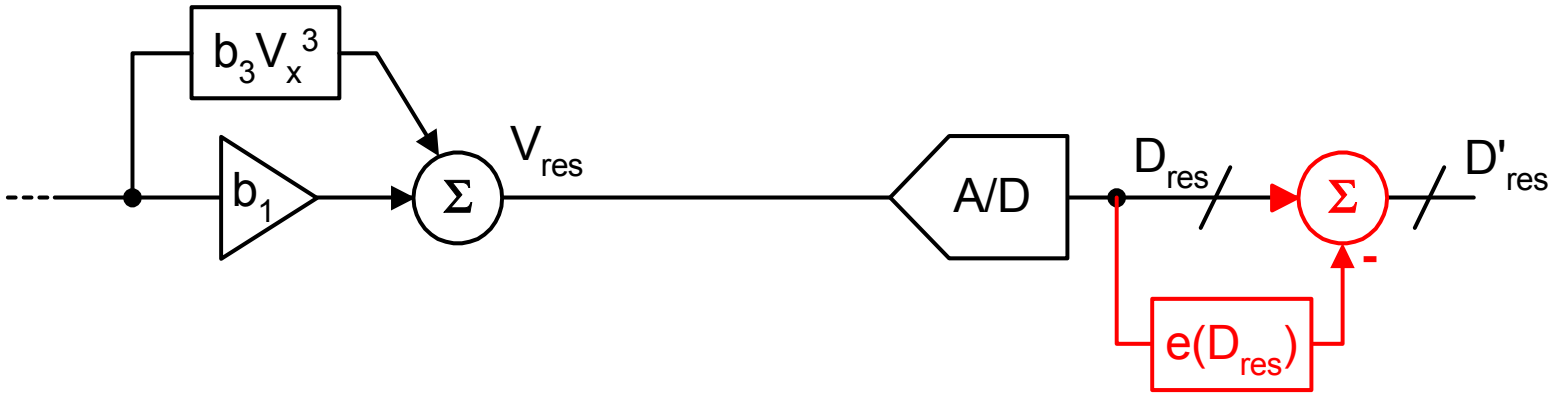


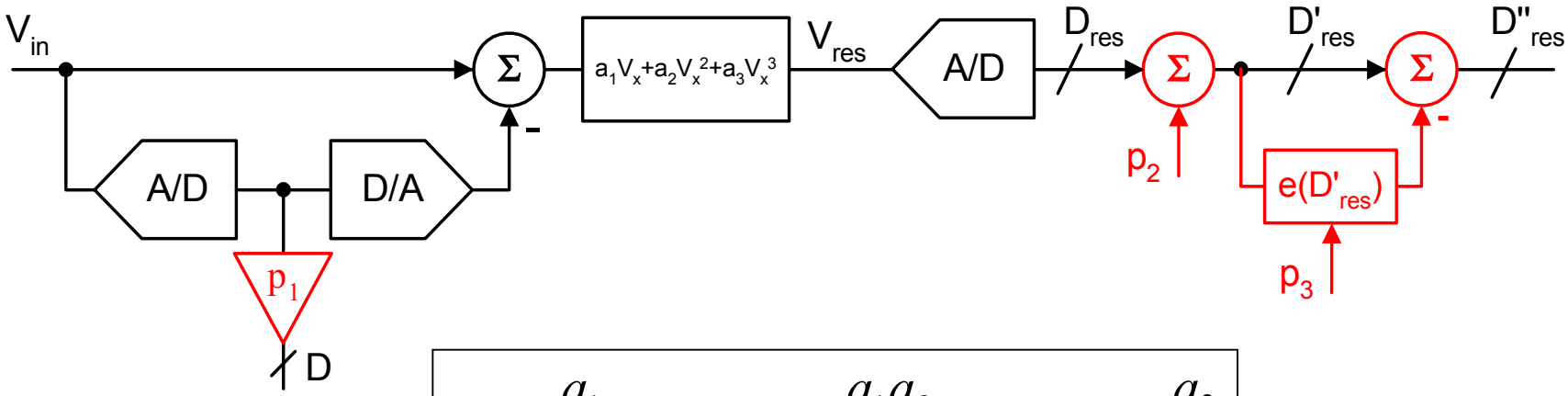

$$e(V_{res}) = V_{res} - 2\sqrt{-\frac{1}{3p_3}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{V_{res}}{2\cdot\sqrt{-\frac{1}{27p_3}}}\right)\right] \qquad with: p_3 = \frac{b_3}{b_1^3} < 0$$

# Third Order Correction




- Single-parameter correction function can be pre-computed and stored in look-up table (ROM)
- Small ROM size achievable through continuous data compression methods

# Complete Digital Correction




$$p_1 \cong \frac{a_1}{2^R} \qquad p_2 \cong \frac{a_1 a_2}{3a_3} \qquad p_3 \cong \frac{a_3}{a_1^3}$$

- How can we measure/calibrate parameters in digital domain?

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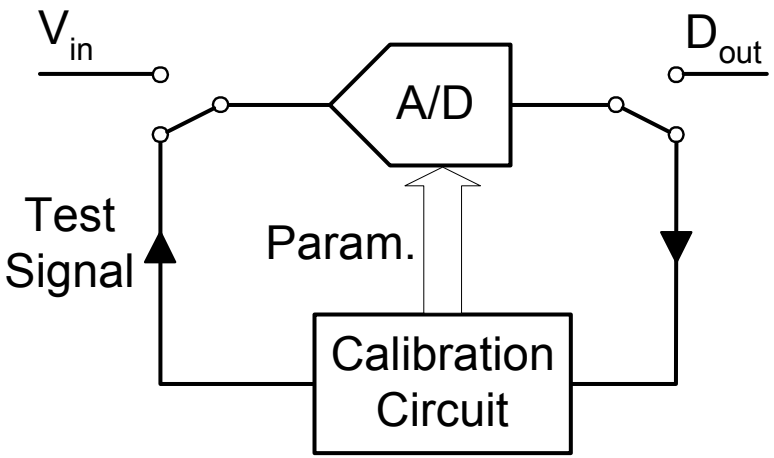
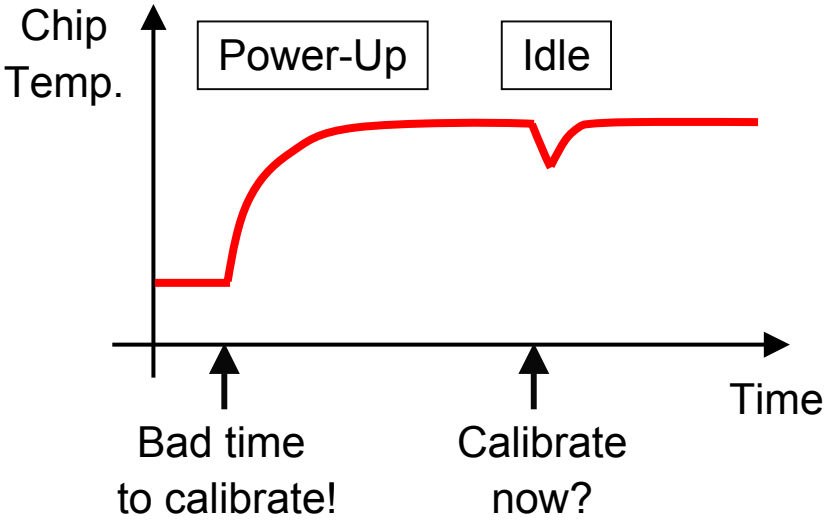
# Calibration Concept

## Classical Approach:

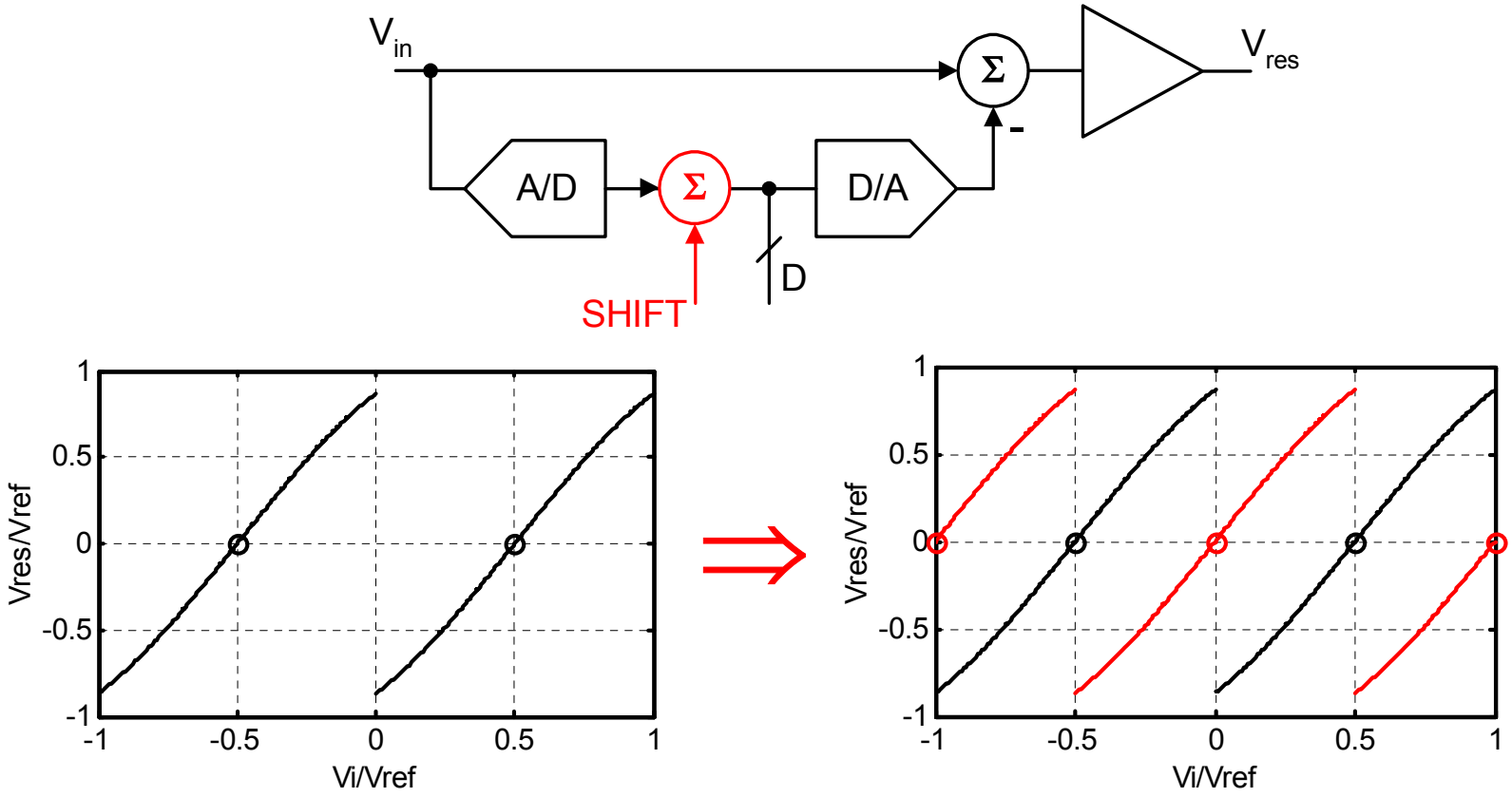



## Problem:




- Correction parameters depend on temperature, etc.
- Classical “foreground calibration“ unfeasible
- Need continuous “background calibration“ during normal A/D operation

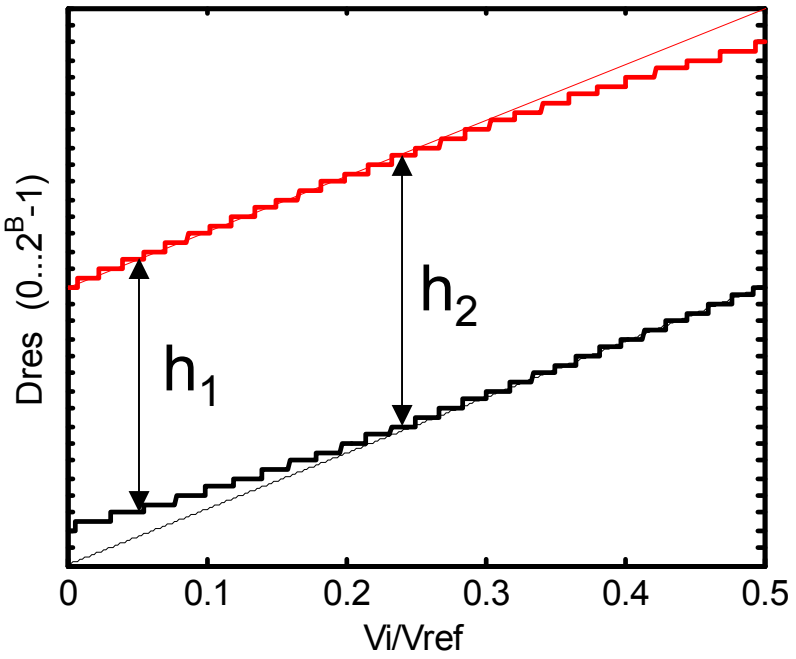
# Key: Two-Residue Pipeline Stage



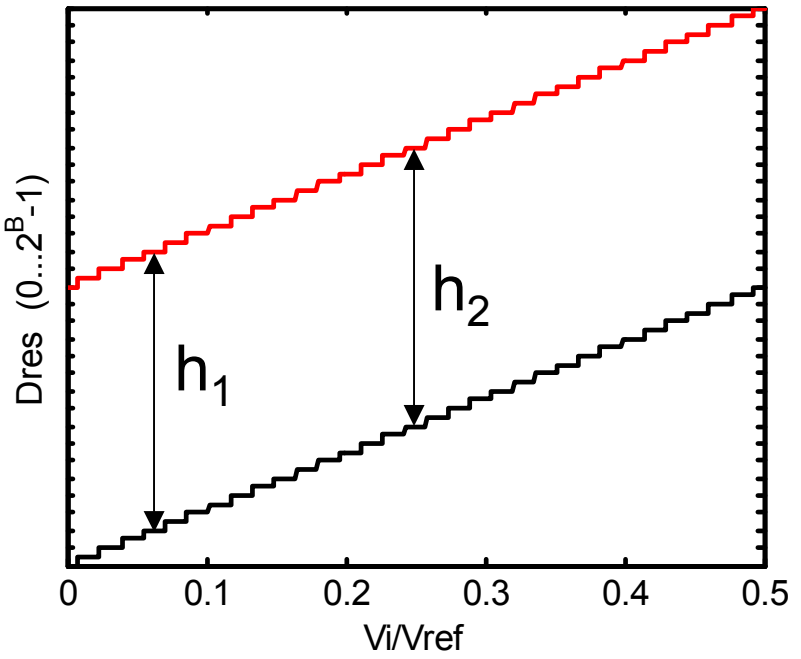

- Add: Digital SHIFT signal, redundant A/D and D/A states
- Can carry out conversion on “red“ or “black“ segments

# Digitized Segment ($a_2$=0)

<u>no calibration:</u> $h_1 < h_2$

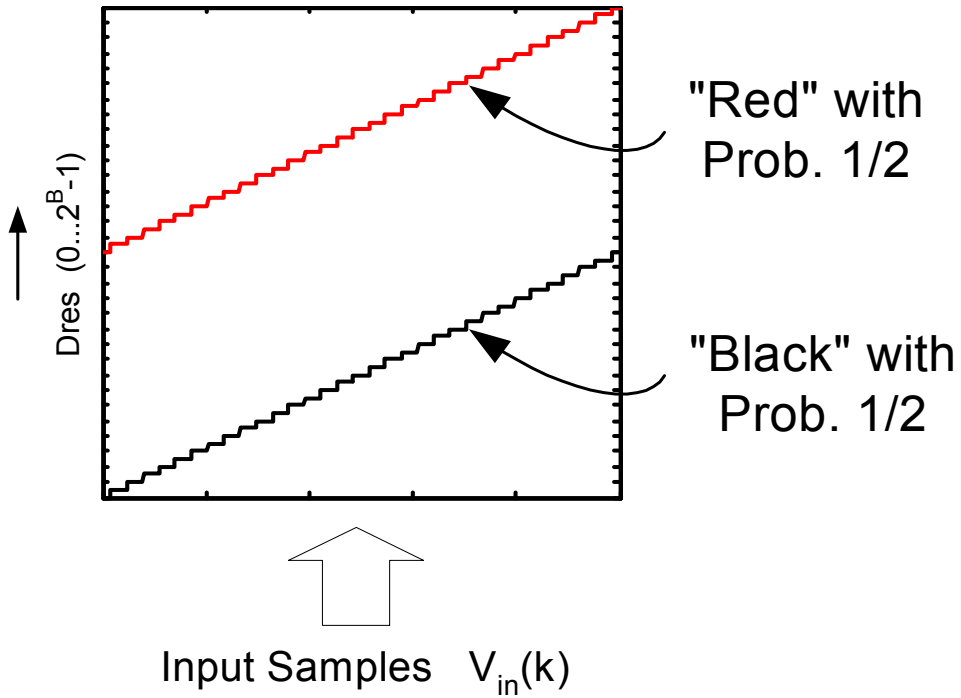



<u>perfect calibration:</u> $h_1 = h_2$



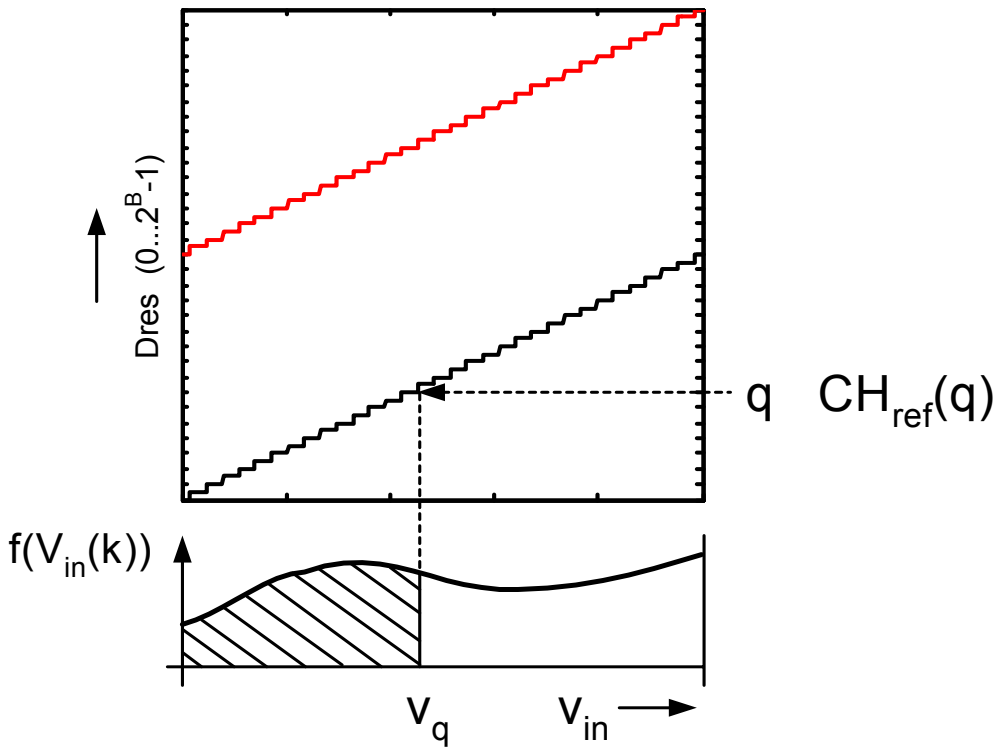

- Idea: Measure $h_1$, $h_2$ and force difference to 0
- How to measure without interrupting A/D operation?
- Solution: Statistics based measurement

# Distance Estimation (1)



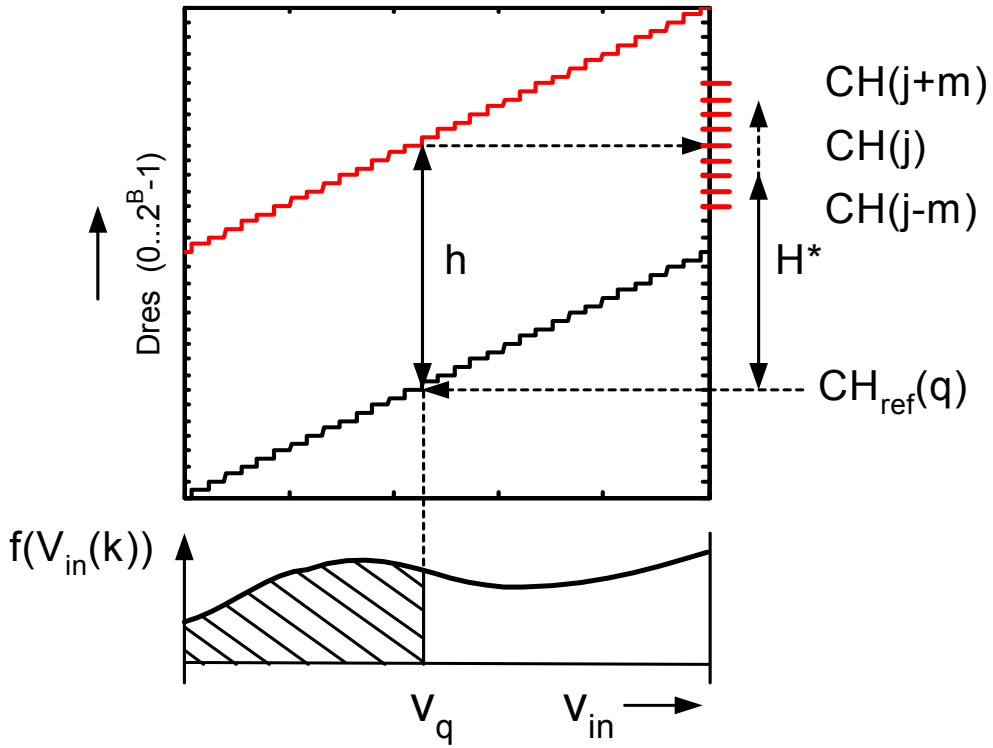

- For each input sample “fair coin toss“ [independent of $V_{in}(k)$] decides red/black

# Distance Estimation (2)



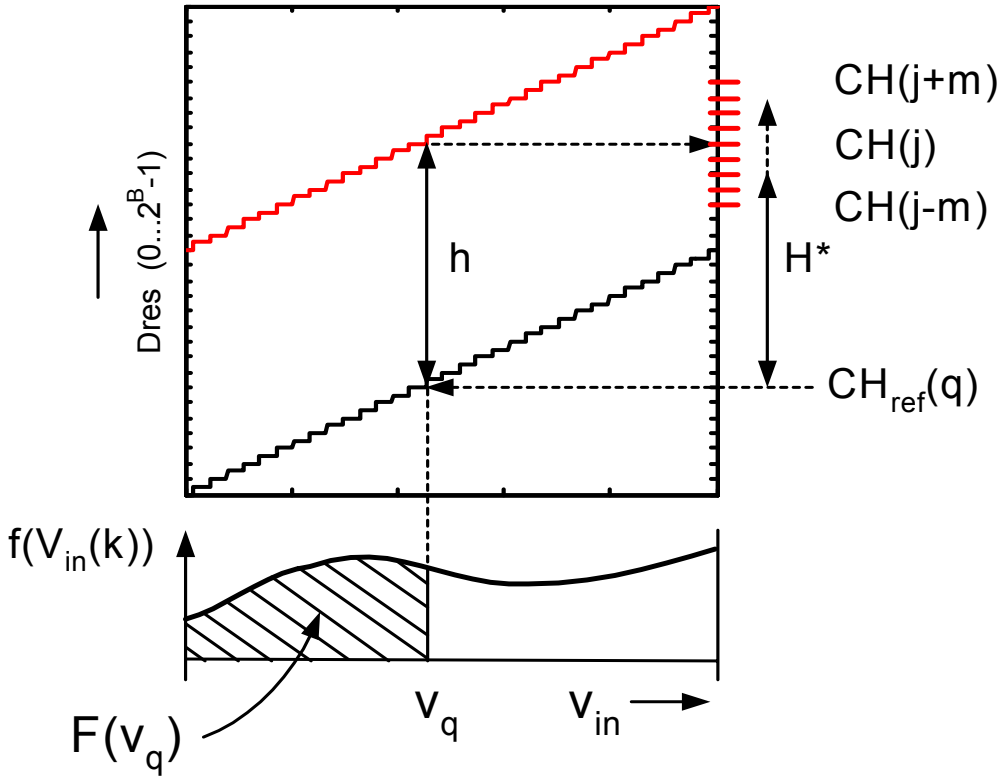

- Simple input model: *stationary* random process
- Count # of codes ≤ q in "black channel" → cumulative histogram $CH_{ref}(q)$

# Distance Estimation (3)




- Place counter array in “red channel“
- After n samples, find “red“ count that is closest to $CH_{ref}$ (q) $\Rightarrow$ Distance Estimator H*

# Distance Estimation (4)



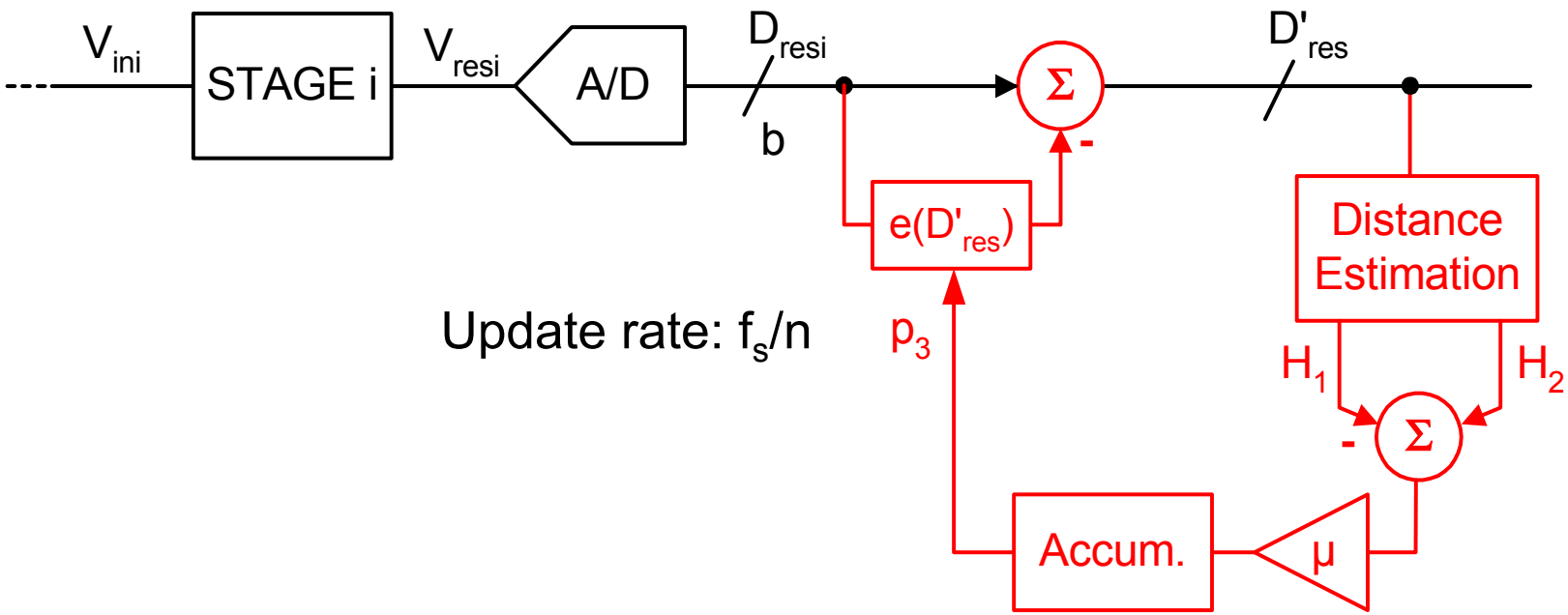

## Can show:

$$\lim_{n\to\infty} E(H^*) \to h$$

$$\mathrm{var}(H^*) \cong \frac{F(v_q)\cdot 2^{2B}}{n\cdot f(v_q)^2}$$

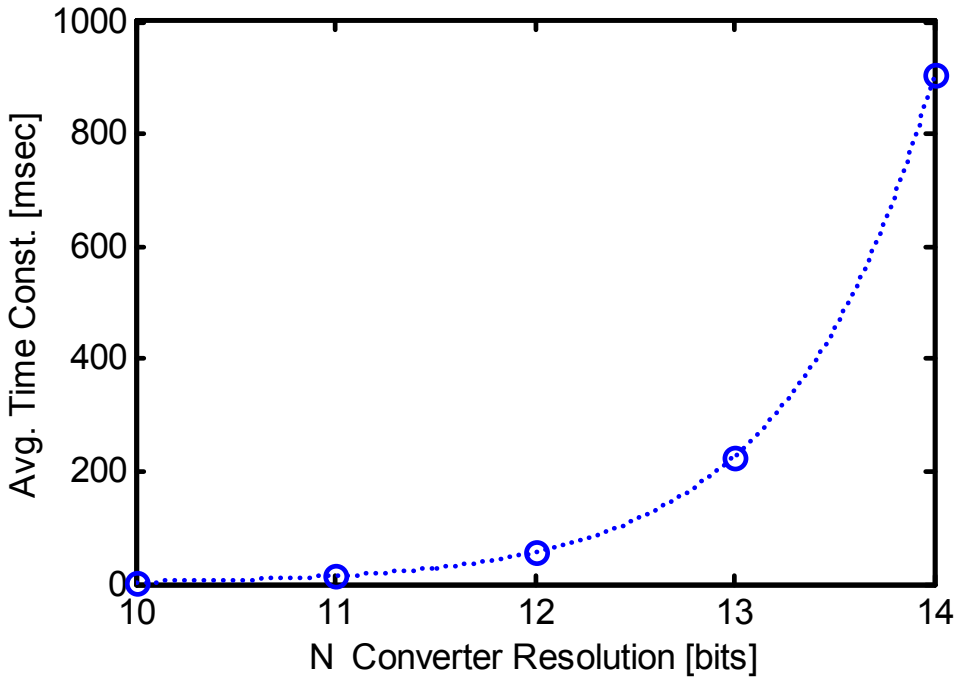
- Estimation fails if signal not “busy“ around $v_q$
- Detectable!

# LMS Loop




- Accumulator forces average $H_2$-$H_1$ to zero
- Tradeoff: Residual variance of $p_3$ vs. tracking time constant
- Straightforward extension to track $p_1$, $p_2$

# Tracking Time Constant




$$\tau_{AVG} \cong \frac{0.6 \cdot k^2 \cdot 2^{2B}}{f_s \cdot \varepsilon^2}$$

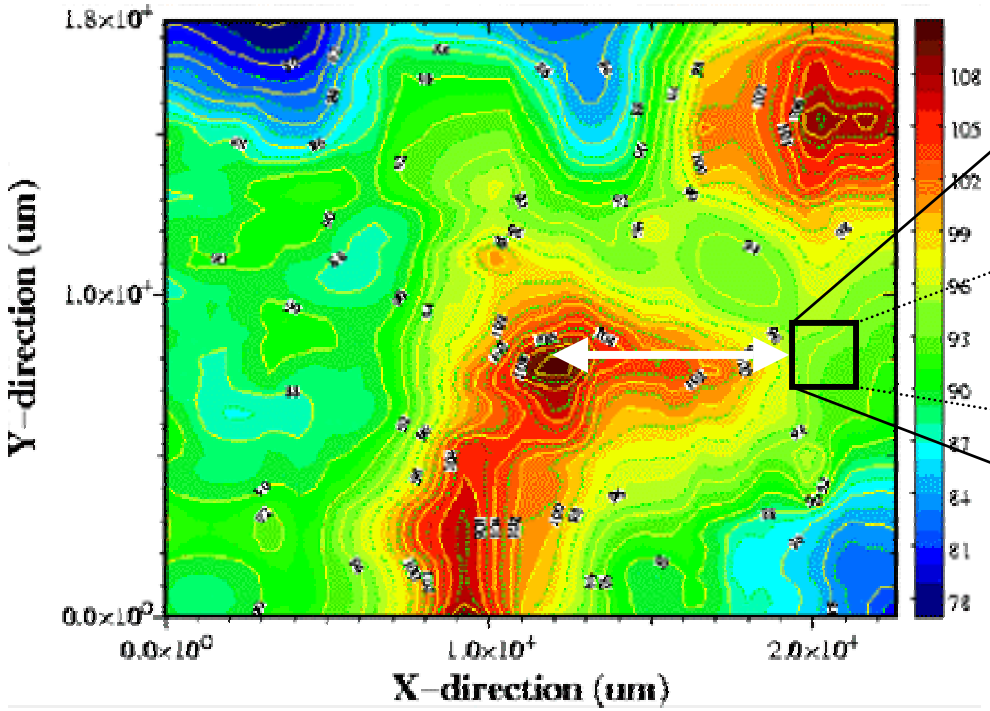
*Example* :

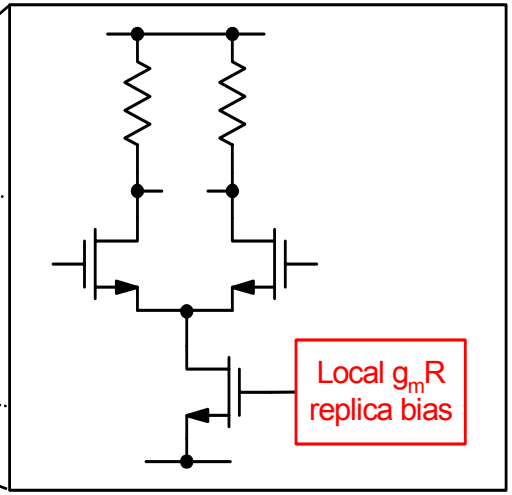
| | |
|---|---|
| $k = 3$ | Confidence |
| $B = N - 3$ | Backend res. [bits] |
| $f_s = 100 MHz$ | Sampling rate |
| $\varepsilon = 0.5$ | LSB precision |

- Example: N bit converter with 3-bit Stage1, uniform input distribution
- Must address/attenuate potentially faster variations in analog domain

# On-Chip Temperature Variations

μP Temperature Map [Najm, EEdesign 01/09/01]




Rule of thumb, d=200μm:

$\Delta T_{remote} / \Delta T_{local} > 10$, $\tau = 100\mu s$

Solutions:

- Local replica biasing
- Keep distance to “hot spots“, common centroid layout

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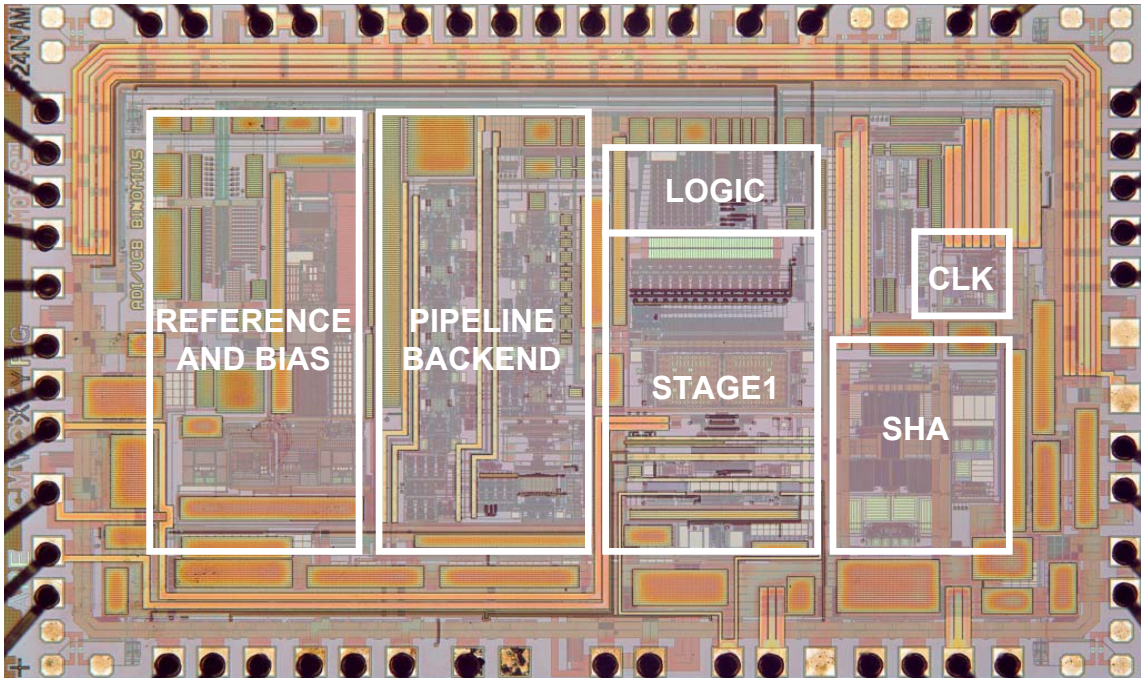
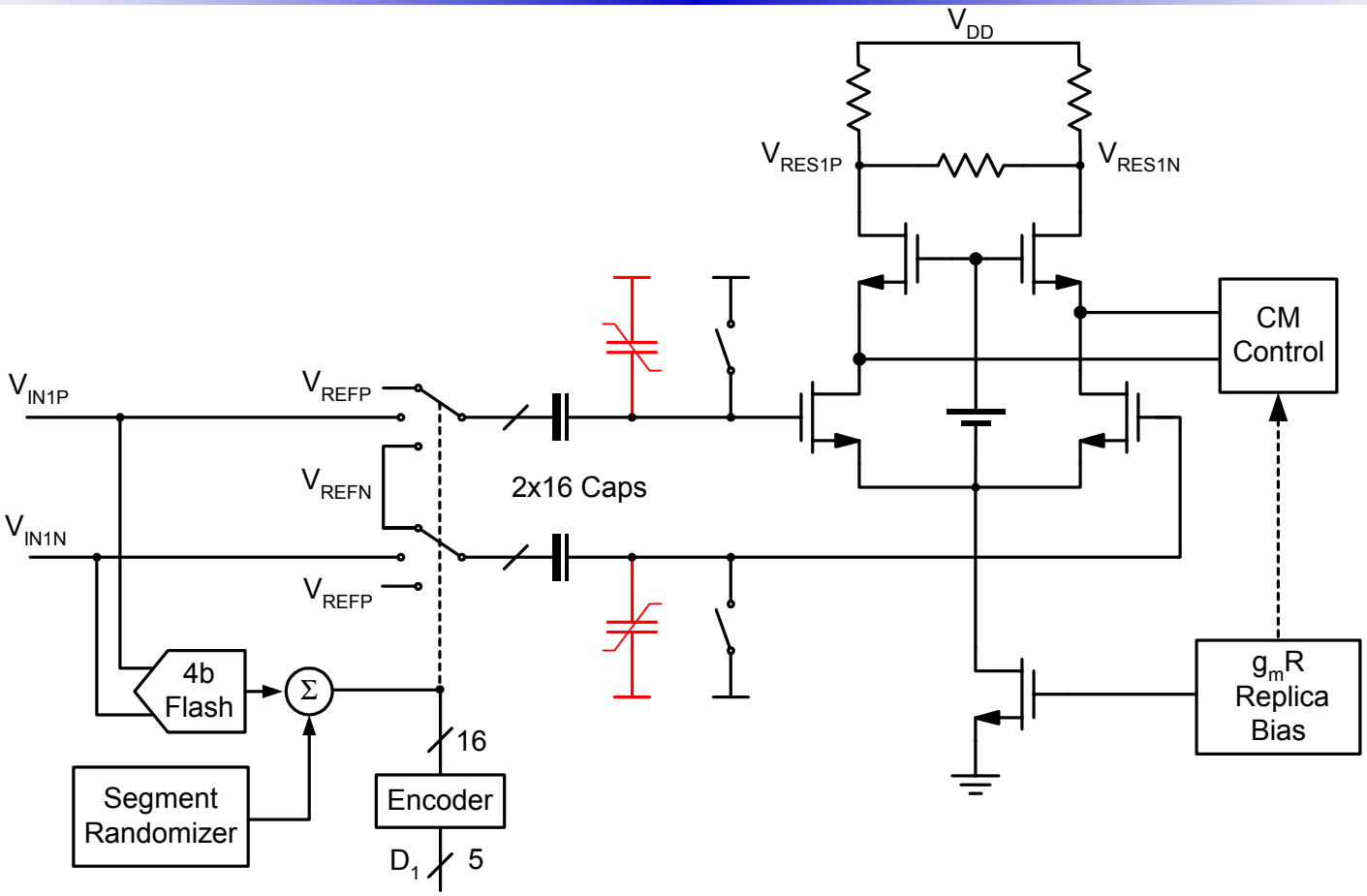
# Die Photograph



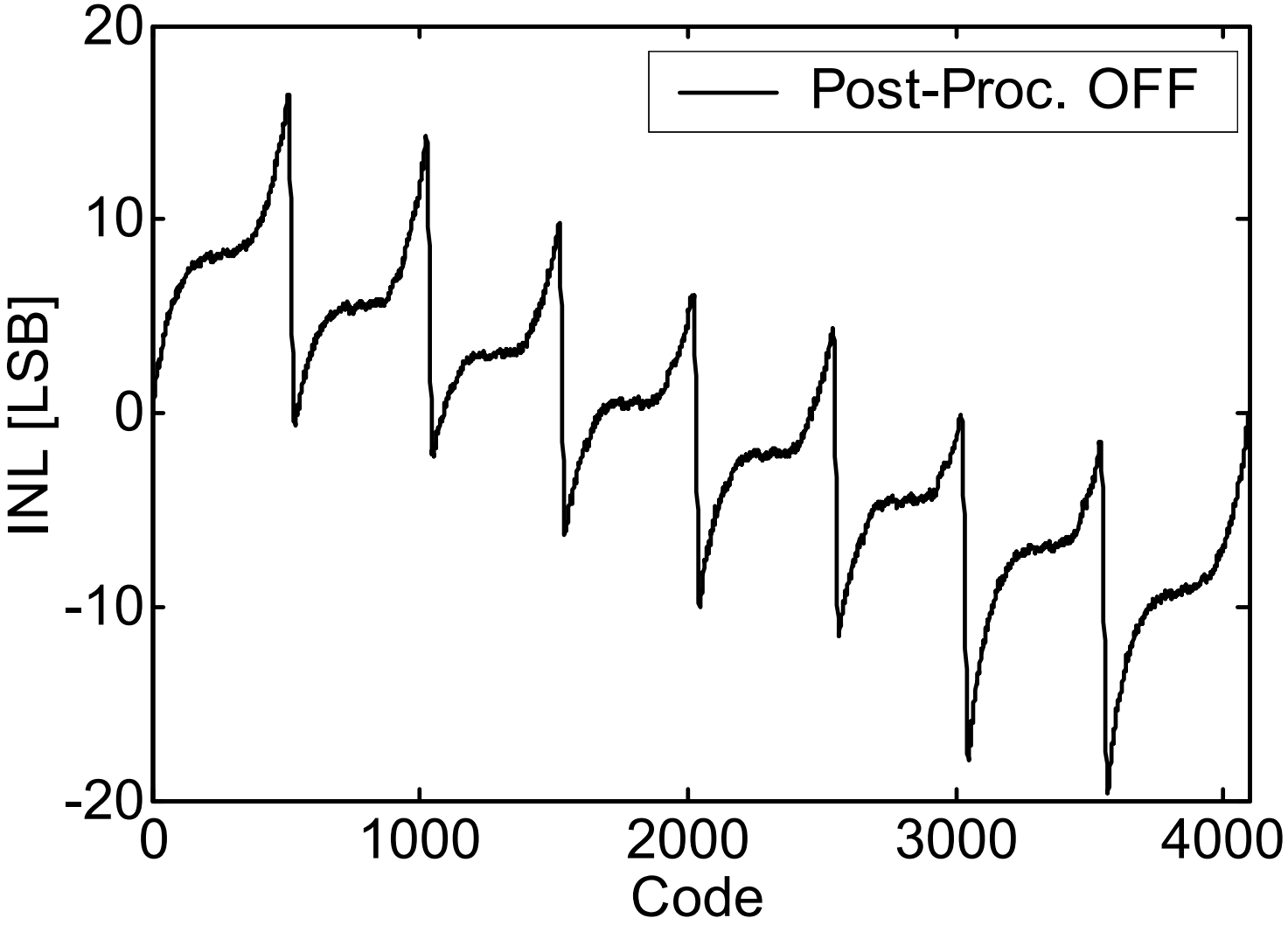

- "Proof of concept": 12bit, 75MHz ADC, 0.35µm
- Re-used commercial part (Analog Devices AD9235)
- Modified only 3-bit Stage1 → Open-loop
- Digital post-processor off-chip (FPGA)

# Open Loop Pipeline Stage

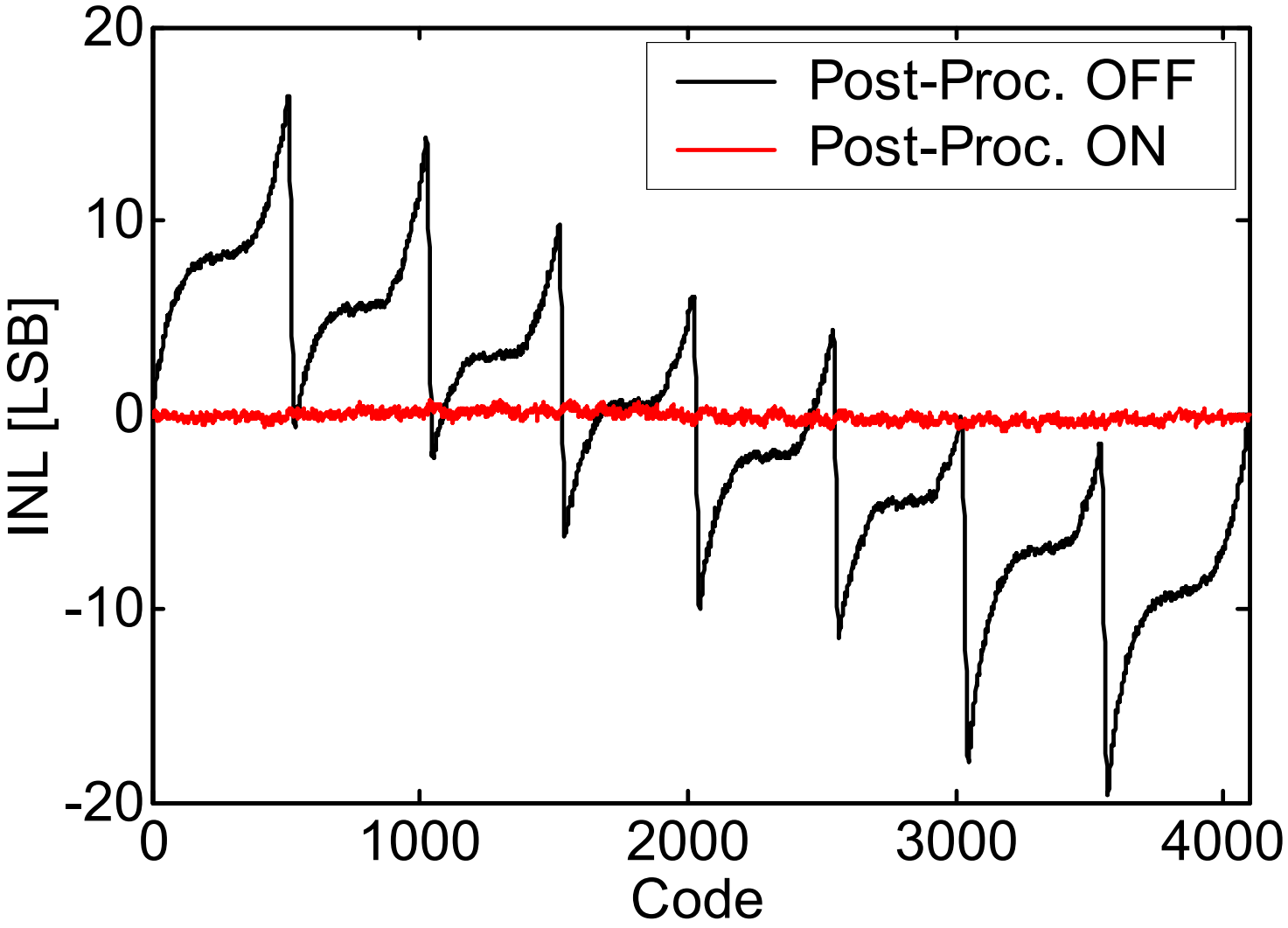



- Open-loop ⇒ “New“ second order circuit effects

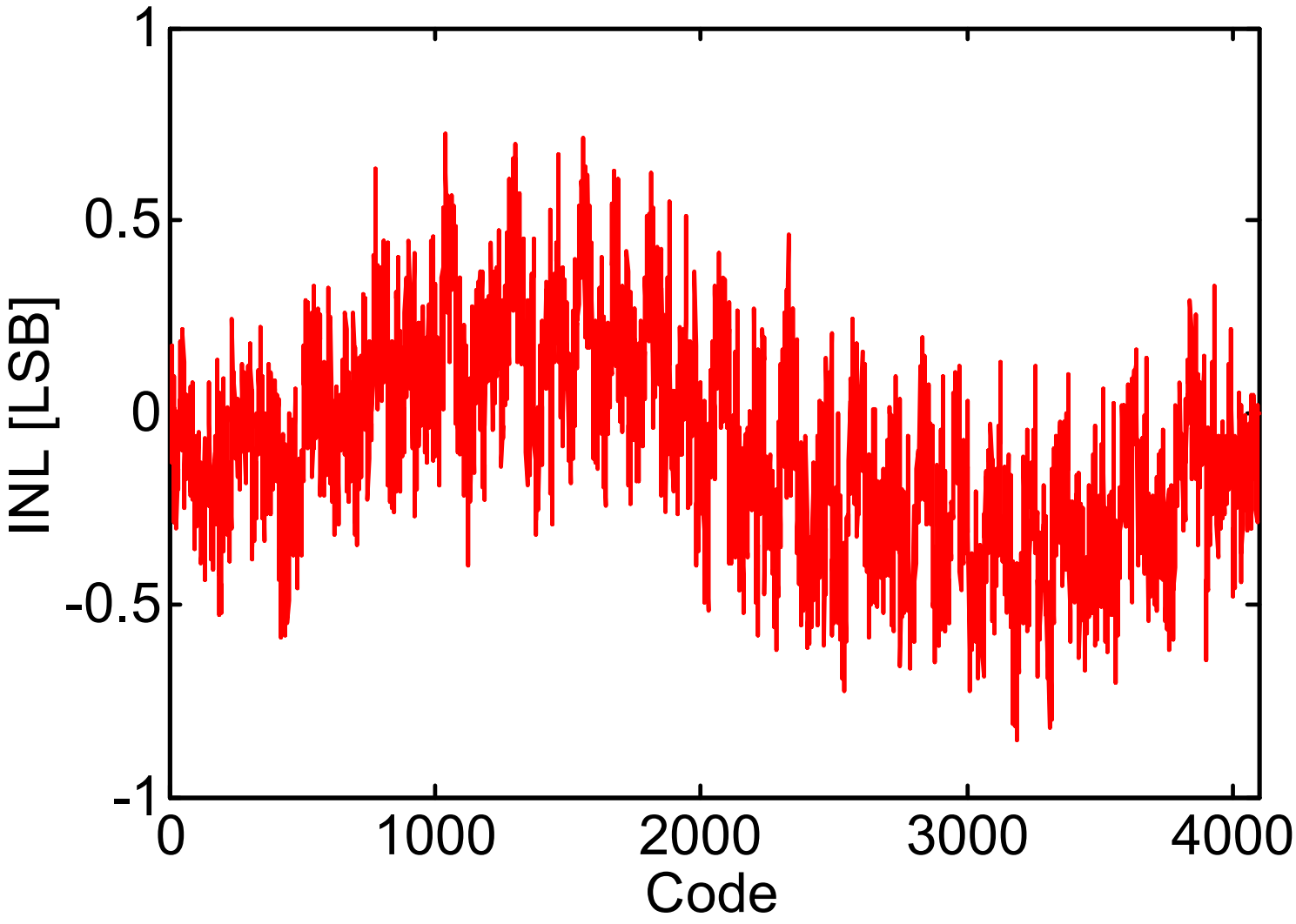
# Measured INL



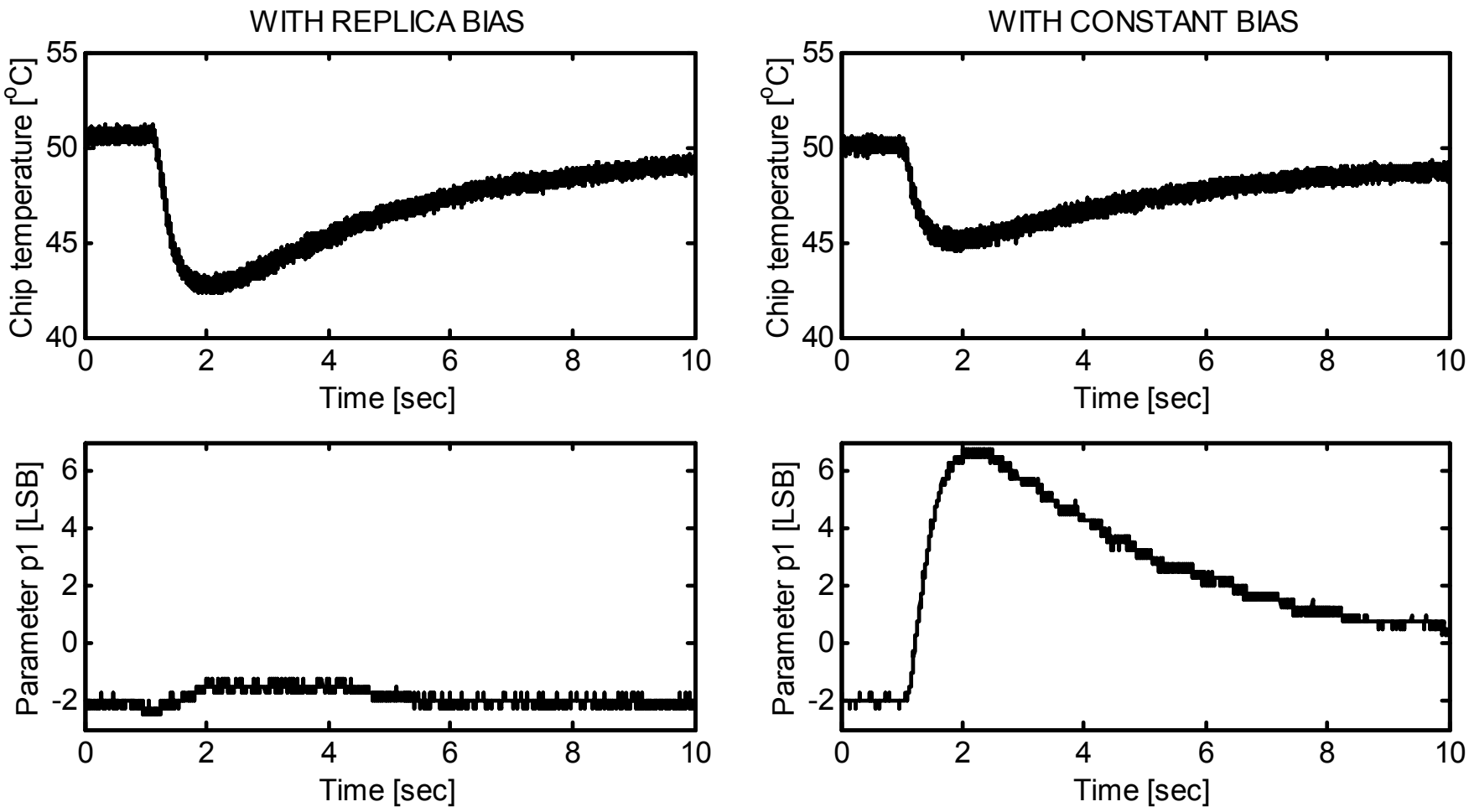
# Measured INL



# INL Zoom (Post-Proc. ON)



# Measurement Results: Tracking



# Performance Summary

| | | | |
|---|---|---|---|
| Technology | | 0.35µm CMOS | |
| Supply Voltage | | 3V | |
| Resolution | | 12b | |
| Conversion Rate | | 75 MSamples/sec | |
| | | With Calibration | Without Calibration |
| SNR | $f_{in}$=1MHz<br>$f_{in}$=40MHz | 68.2 dB<br>67 dB | 48 dB |
| THD | $f_{in}$=1MHz<br>$f_{in}$=40MHz | -76 dB<br>-74 dB | -50 dB |
| SFDR | $f_{in}$=1MHz<br>$f_{in}$=40MHz | 80 dB<br>76 dB | 52 dB |
| DNL | | -0.5, +0.5 LSB | -1, 0.6 LSB |
| INL | | -0.9, +0.6 LSB | -19, +16 LSB |
| Power Dissipation<br><br>ADC Core<br>Output Drivers | | 290 mW<br>24 mW | |

- With calibration: Within data sheet of commercial part (AD9235)!

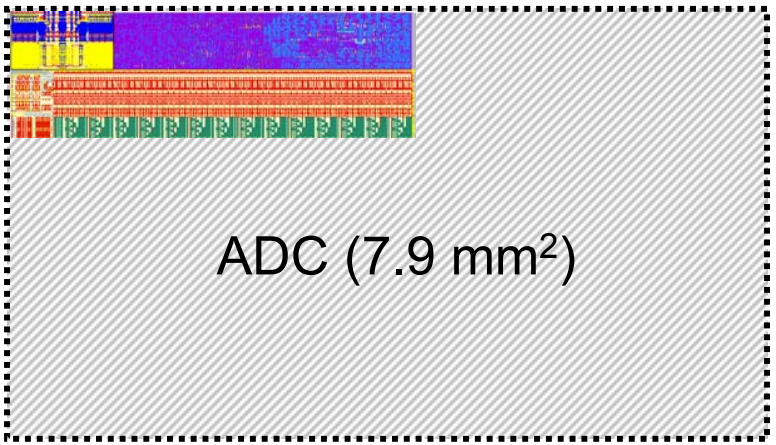
# Digital Post-Processor

- Only 1st and 3rd order correction ($p_1$ and $p_3$)
- Synthesis & Place/Route results using 0.35µm CMOS library:

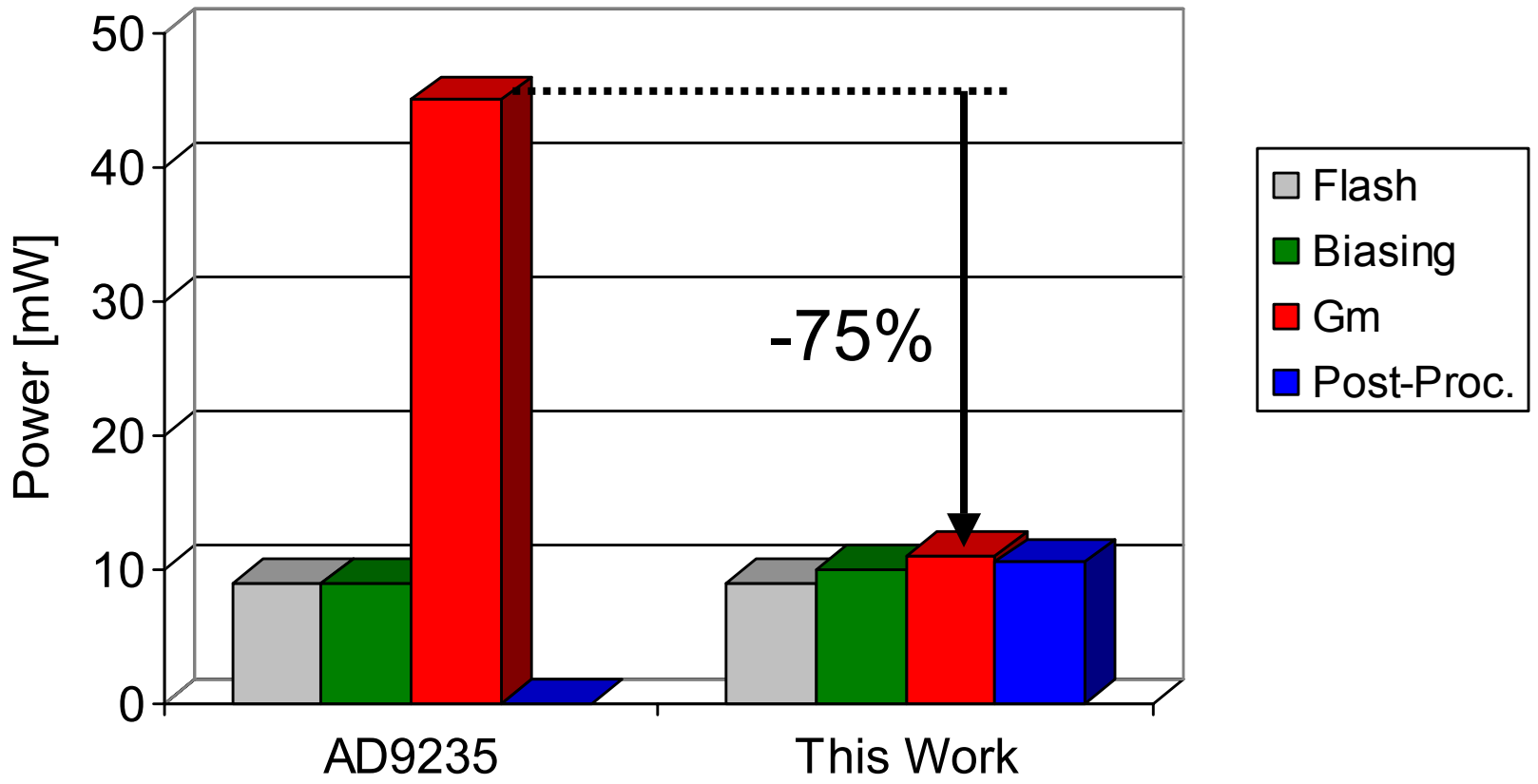
Post-Processor

8400 gates
64kBit ROM
64 Bytes RAM

∑ 1.4 mm²



# Stage1 Power Breakdown



# Prototype Summary

- Open-loop residue amplification
  - Reduces ADC power consumption
  - Improves deep sub-µm compatibility
  - May help in pushing attainable speed
- Resulting analog errors
  - “Slow“ $\rightarrow$ statistics based digital calibration
  - “Fast“ $\rightarrow$ analog domain techniques
- Judicious combination of digital and analog techniques $\Rightarrow$ feasible, low overhead solution

# Continuation Work

- Optimized deep sub-μm design
- Multi-stage calibration
- Cash in on simplified circuits
  - Push conversion speed
  - Explore architectural simplifications to lower power
- Work in progress at Berkeley: 12b, 200MS/s, 200mW, power 4x below state-of-the art!
- At Analog Devices: Commercial implementation for embedded applications in fine line technology

# Outline

- Motivation
- Digitally Assisted Pipelined ADC
  - Circuit Concepts
  - Experimental Results
- Other Work & Future Opportunities
- Conclusion

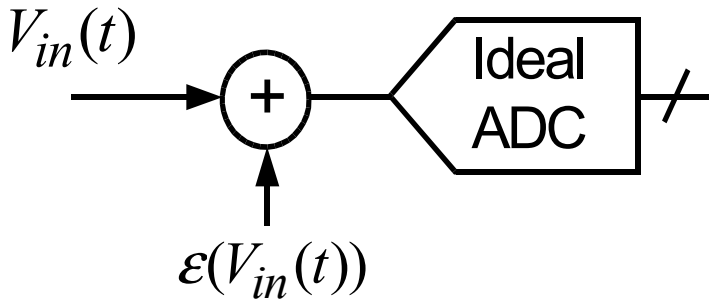
# Recent Digitally Assisted ADCs

| Work | Target | | Issues adressed | | | |
|---|---|---|---|---|---|---|
| | Perfor-mance | Low power | Amplifier Errors | | Matching, Offset | Deep sub-µm compatib. |
| | | | Lin. | Nonlin. | | |
| Murmann, ISSCC 2003 Pipeline | | √ | √ | √ | | √ |
| Jamal, ISSCC 2002 Time Interleaved | √ | | | | √ | |
| Yu, ISSCC 2001 Pipeline | √ | | √ | | √ | |
| Ming, ISSCC 2001 Pipeline | | | √ | | √ | |

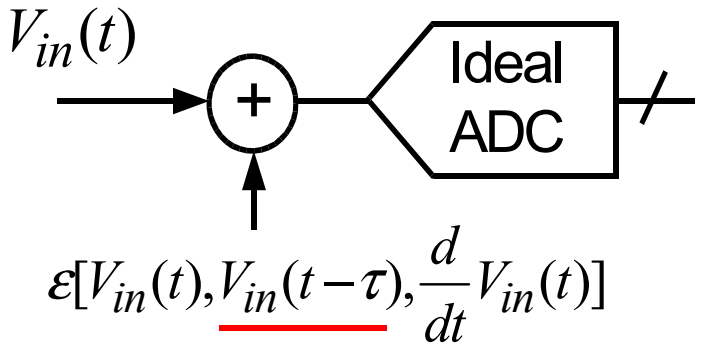
- So far: initial attempts, proof of concept studies
- Expected breakthrough: new, tailored ADC architectures

# Dynamic Error Compensation

Static Error Model



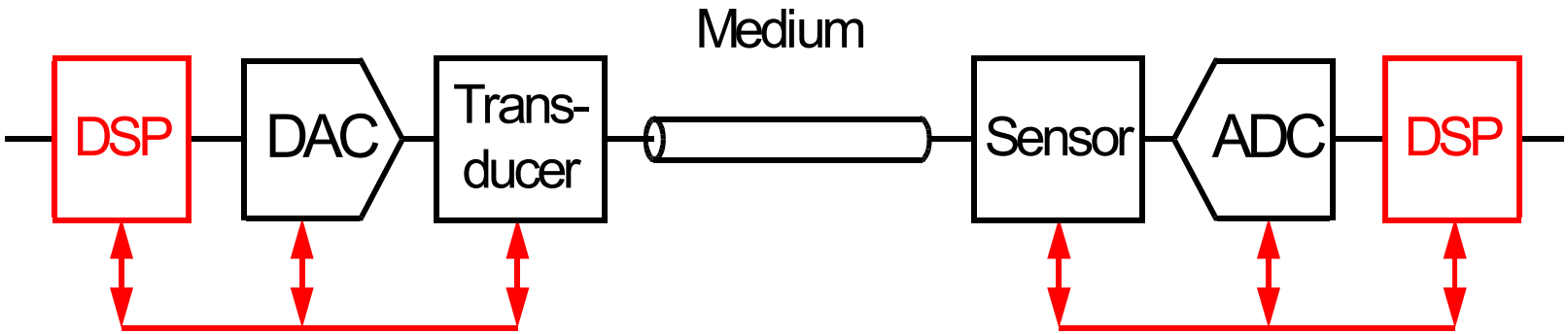

Dynamic Error Model




- Dynamic errors limit spurious & distortion performance many ADCs
- Today: Lots of effort to mitigate dynamic errors through analog domain design techniques
- Future opportunity: Digital compensation!
- Feasible solution to be demonstrated

# Need More “Digitally Assisted Analog“

- Don't care only about ADC!
- Broad, multidisciplinary, system oriented approach to address showstoppers in entire analog signal chain:
  - Transducers, sensors
  - Transmission media
  - A/D and D/A conversion interfaces



# Conclusion

- Demonstrated feasible concept for digitally assisted pipelined ADC
- Lots of room to explore digital post-processing techniques beyond recent efforts
- Visions:
  - New ADC topologies that are tailored to maximally benefit from digital assistance
  - System level: Expand on compensation of analog signal path nonidealities