20.5: A Single-chip CMOS Radio SoC for v2.1 Bluetooth Applications

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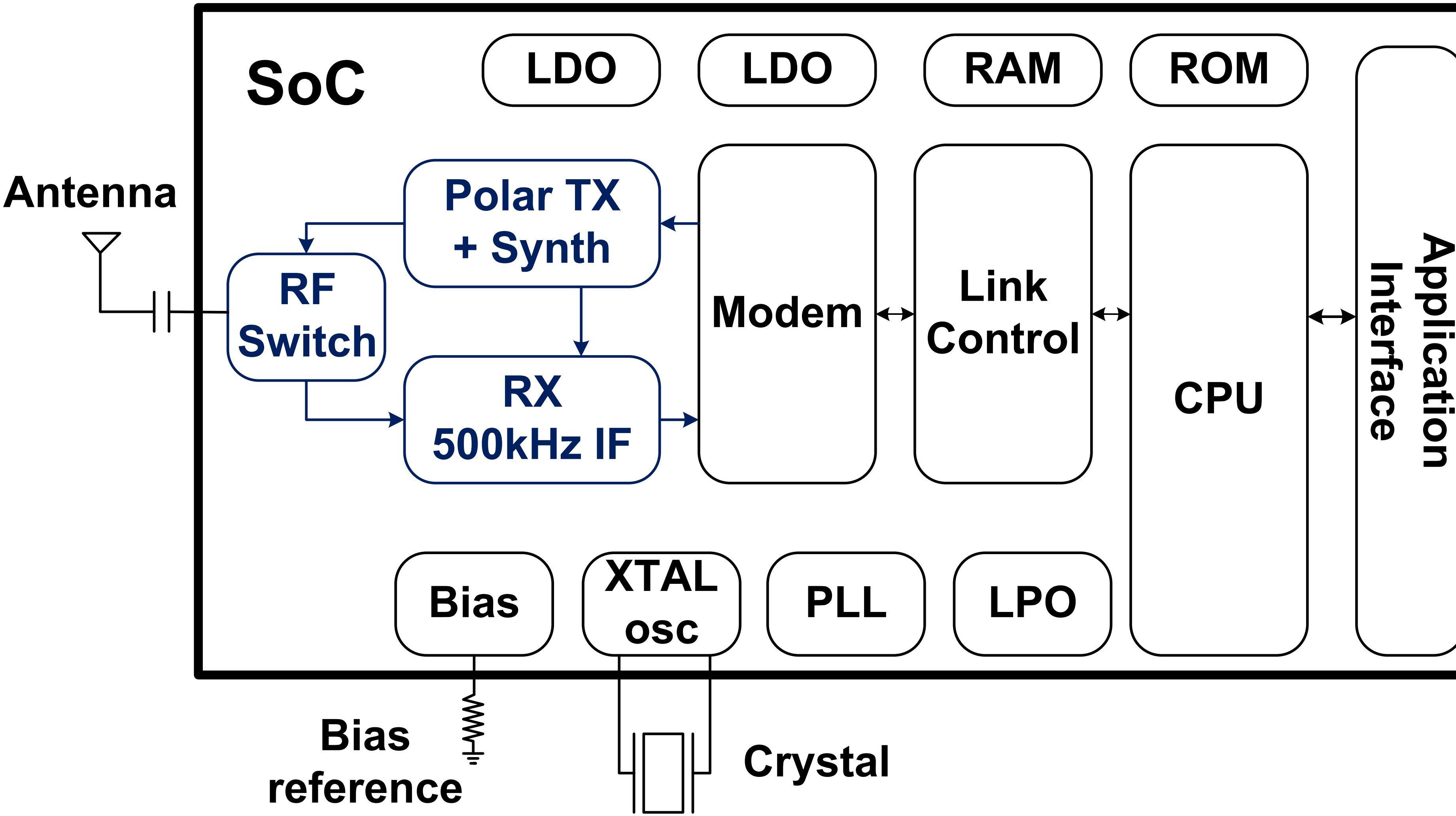
Outline

- Bluetooth Requirements
- SoC block diagram
- Frequency Plan
- Polar Transmitter and Synthesizer
- 500kHz low-IF Receiver
- Summary

Bluetooth Requirements

- Operates in ISM band (2.402 – 2.480GHz)
- Hops through 79 channels, each 1MHz bandwidth
- There are now three data rates
  - Original 1Mbps rate uses GFSK modulation
  - EDR (2 & 3Mbps) uses π/4-DPSK and 8-PSK modulation
- Primarily for short range communication
- Goal is to reduce power consumption and cost

SoC Block diagram



Frequency Plan

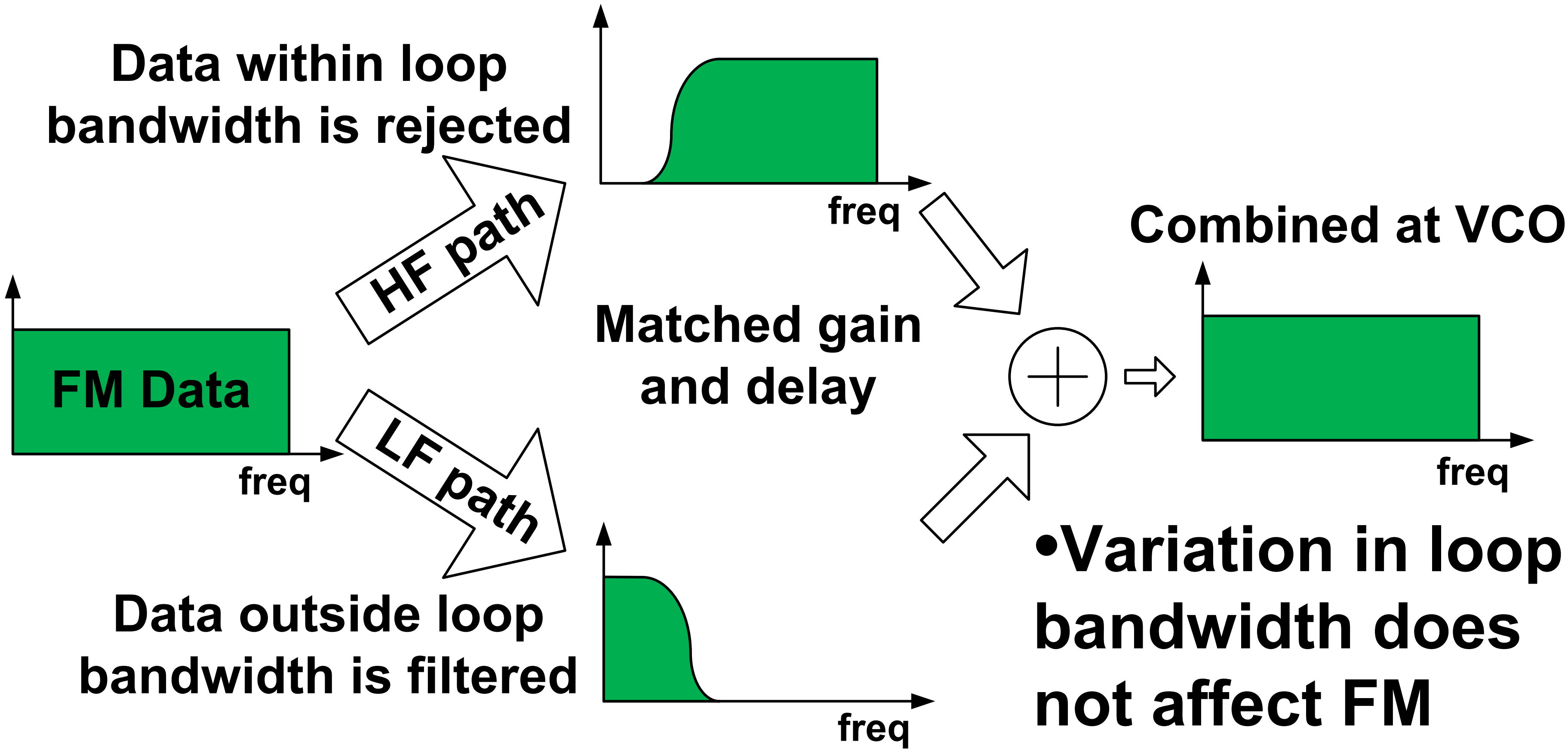
- **VCO operates between 4.8 and 5 GHz**
  - **LO signals generated efficiently with divide-by-2**
- **For transmit, VCO operates at 2x channel frequency**
  - **Divide-by-two block drives power amplifier**
- **For receive, VCO is shifted by 1MHz relative to 2x channel frequency**
  - **Creates 500kHz low-IF receive topology**

TX Architecture

- **Polar architecture**
  - ➢ **Modem divides signal into AM and FM paths**
  - ➢ **Minimizes silicon area**
  - ➢ **Particularly efficient for 1Mbps rate when only FM data is needed (amplitude is constant)**
- **AM data is added at power amplifier**
  - ➢ **Required for 2Mbps and 3Mbps rates**
- **2-point modulation for FM data**
  - ➢ **FM data is subdivided into High Frequency (HF) and Low Frequency (LF) paths**

Two-point modulation

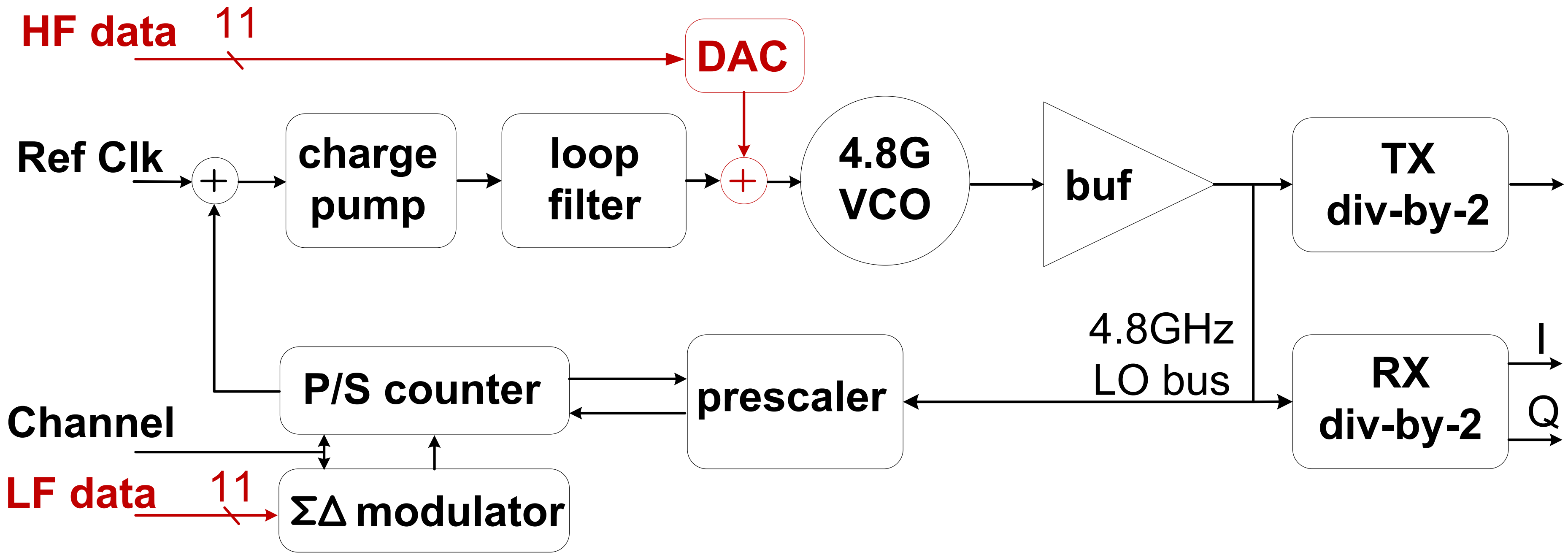
- **Allows FM path bandwidth to be wider than synthesizer loop bandwidth**



•Variation in loop bandwidth does not affect FM

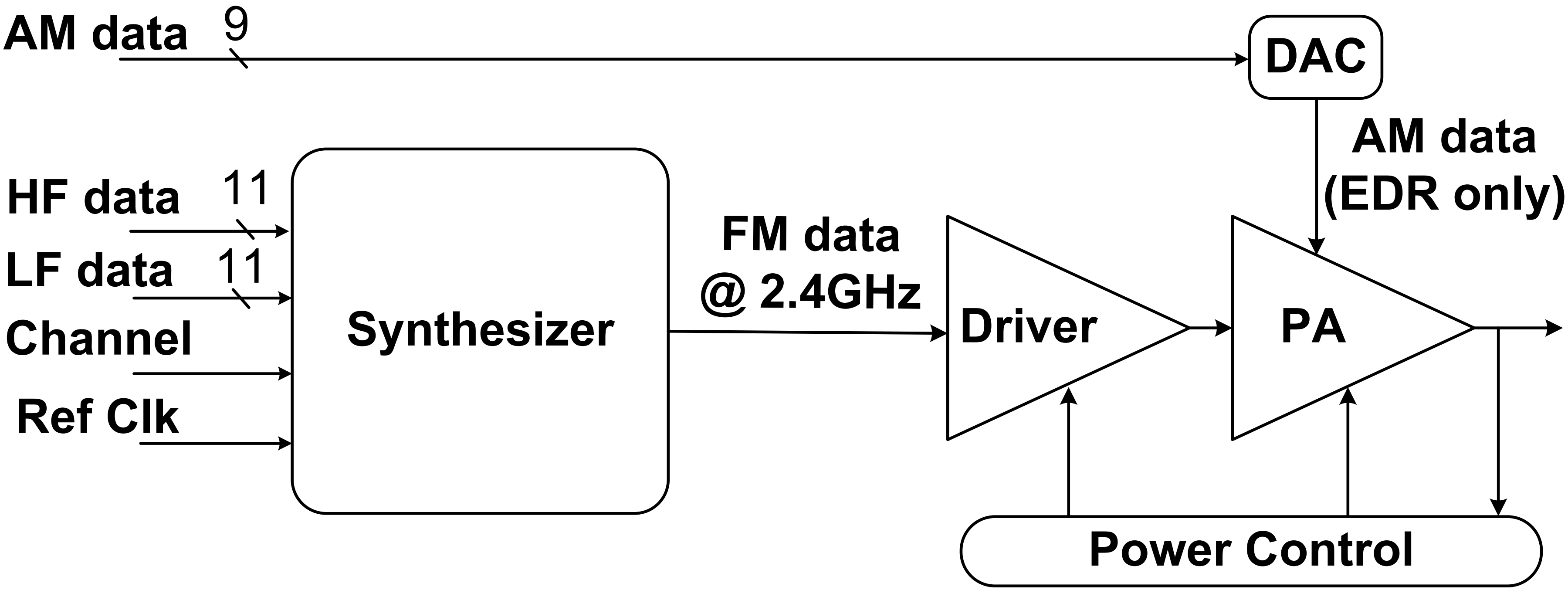
Ref: R. Meyers, P. Waters, Colloquium on VLSI implementations, 1990

Synthesizer and FM modulation



- Elements in Red add frequency modulation path

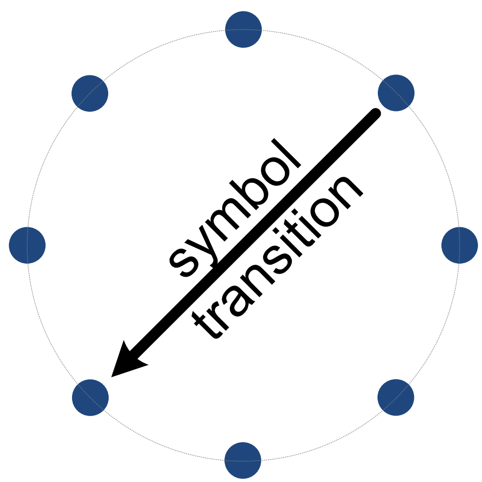
TX Block Diagram



- For 1Mb rate, PA simply amplifies Synth output
- For 2Mb and 3Mb rates, AM signal is added at PA

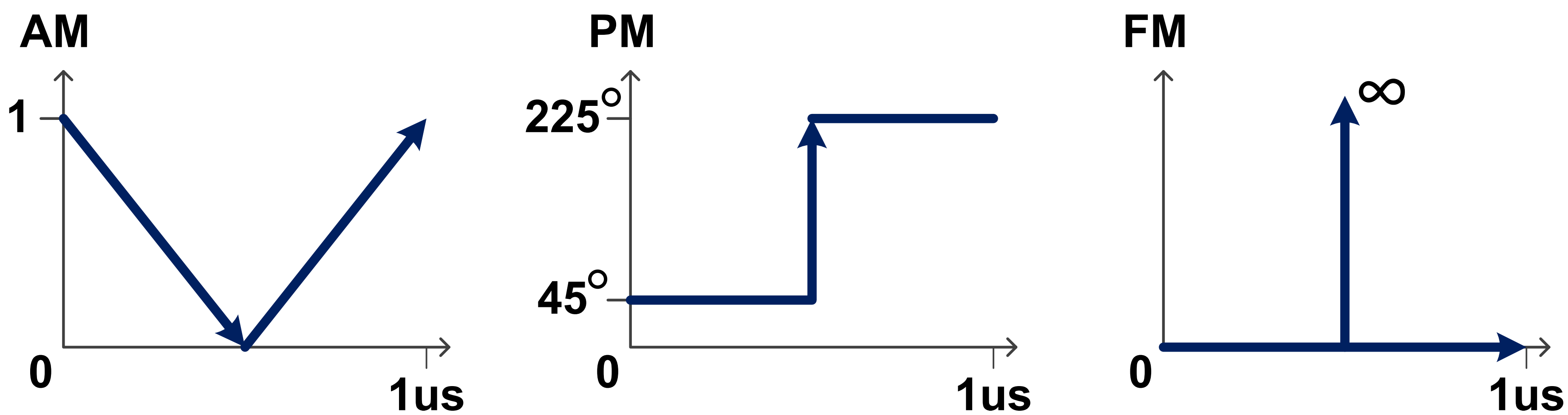
EDR Signals

3Mbps rate uses 8-PSK constellation

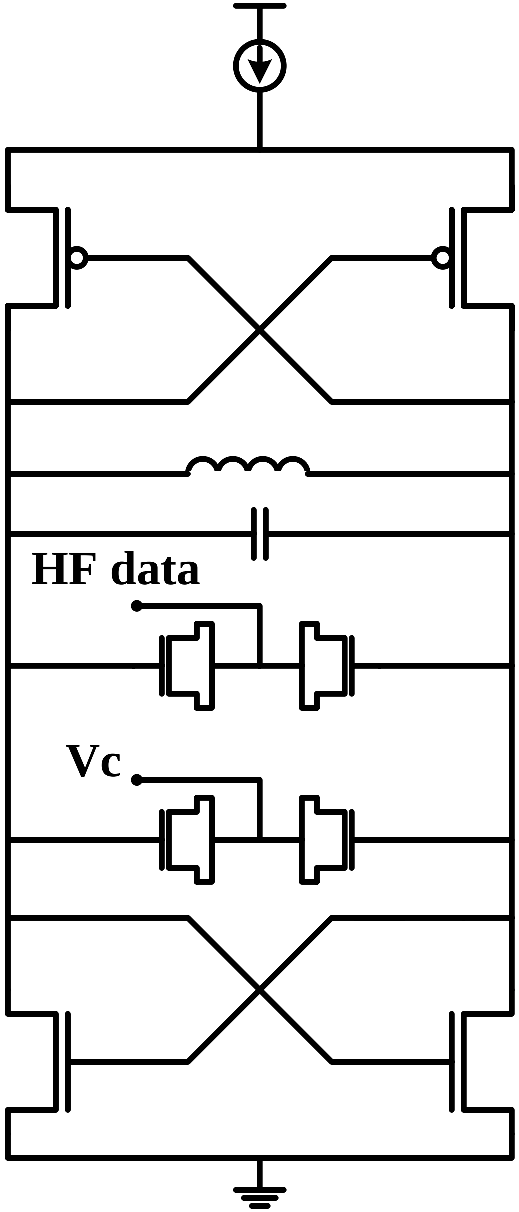


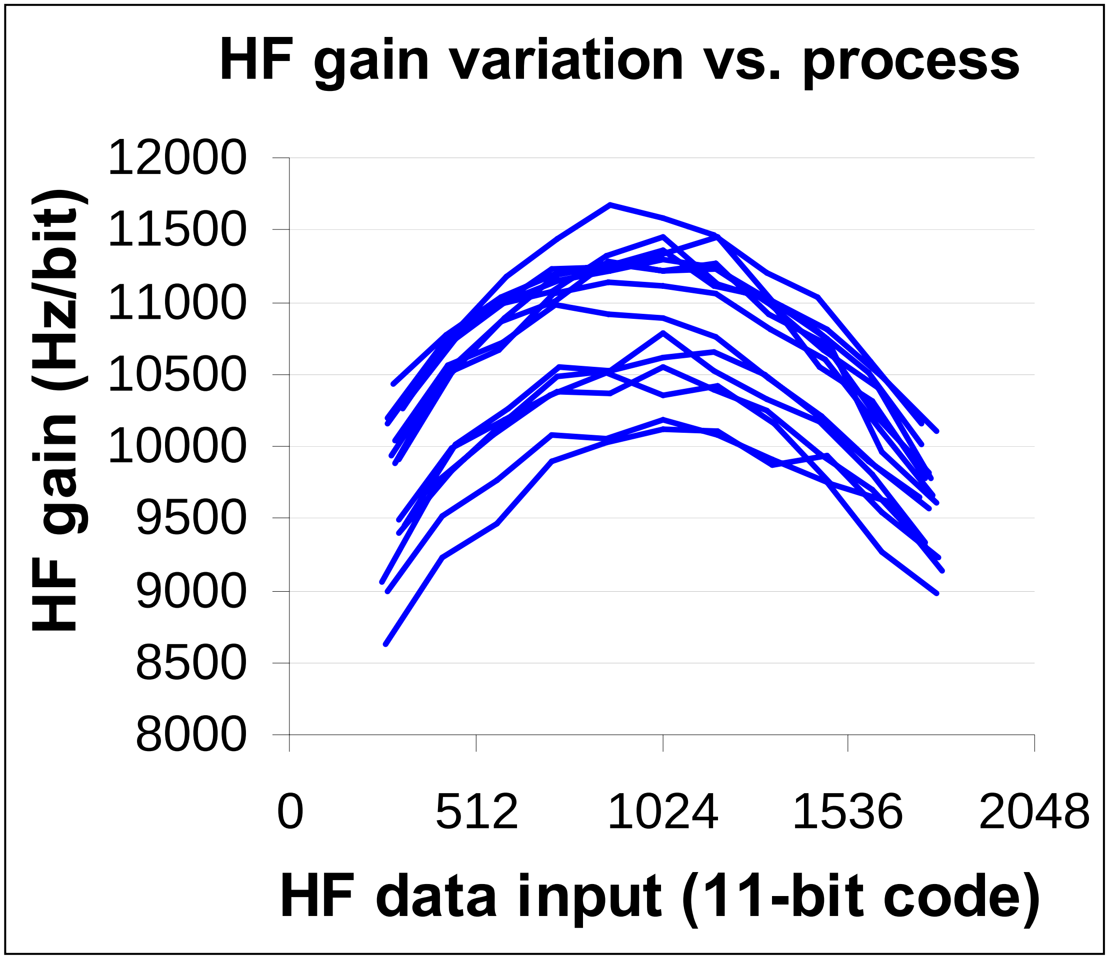
•**AM dynamic range:**
need 26dB min → Spectral mask

•**FM bandwidth:**
need 6.5MHz min → EVM



VCO design





- HF modulation gain must be calibrated

PA design

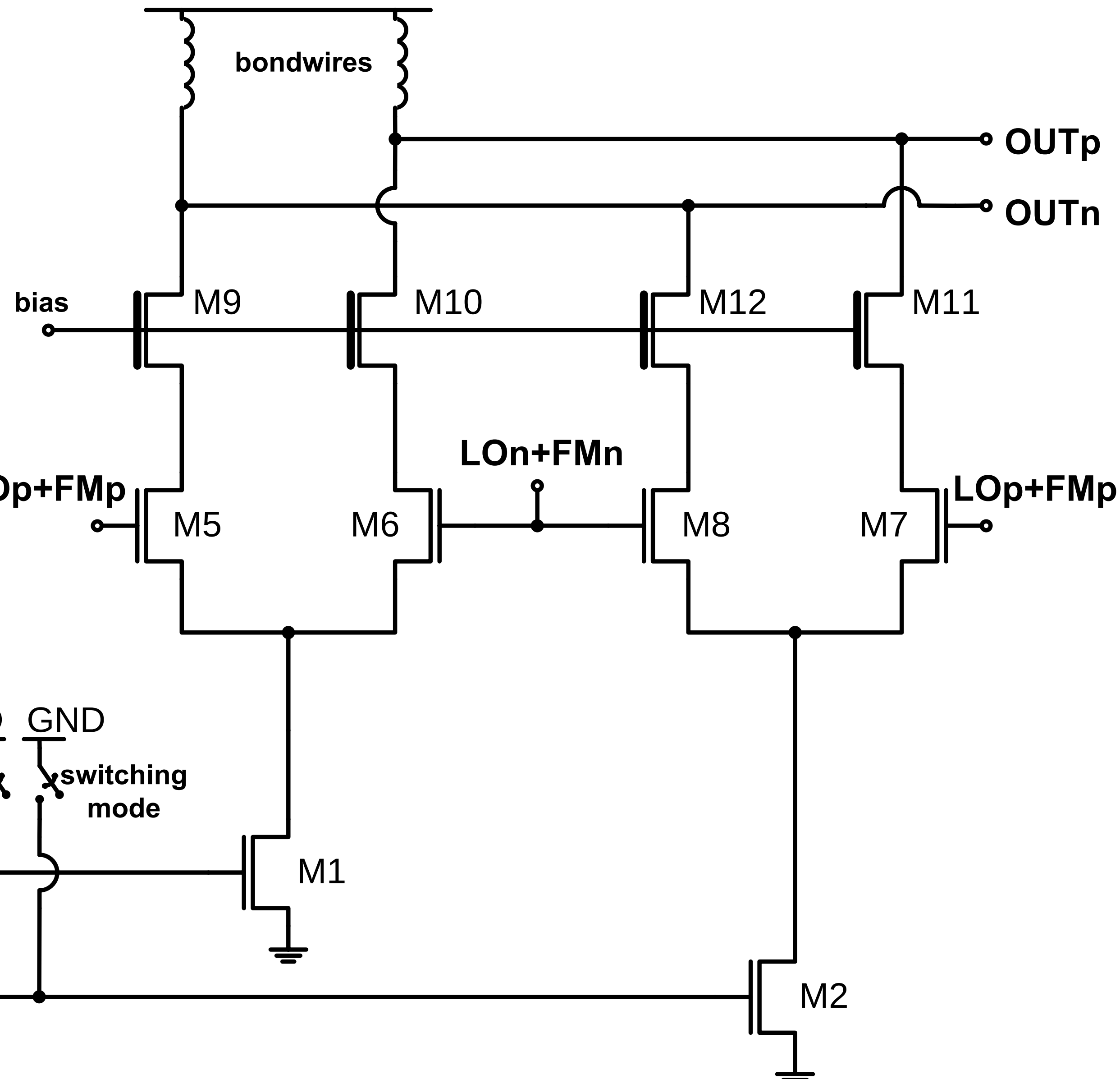
<u>DC current@2dBm</u>

Switching mode:

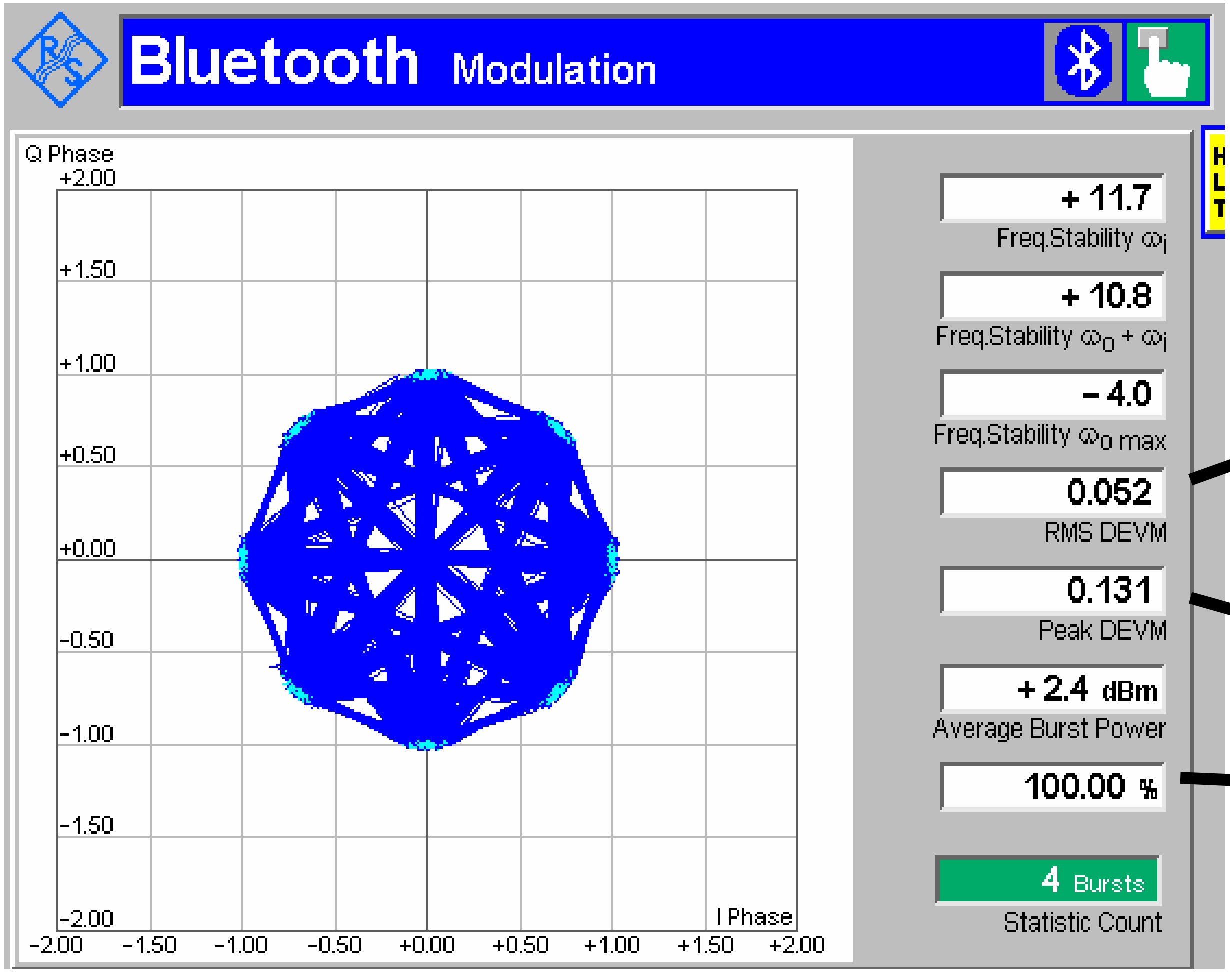
10.1mA

Linear mode:

20mA



EVM measurement



3Mb specification

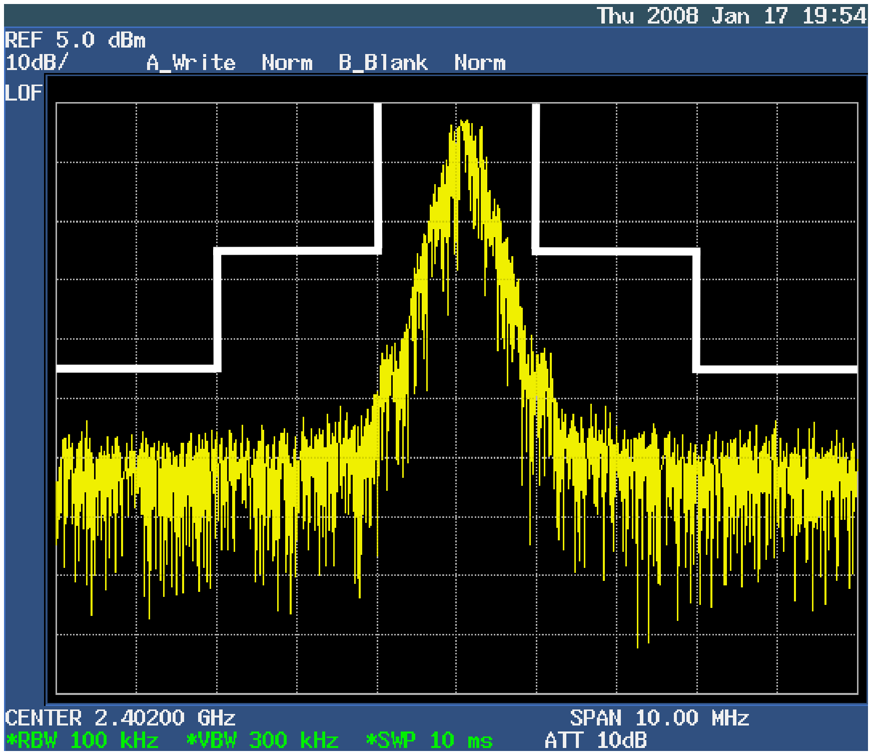
< 13% RMS DEVM

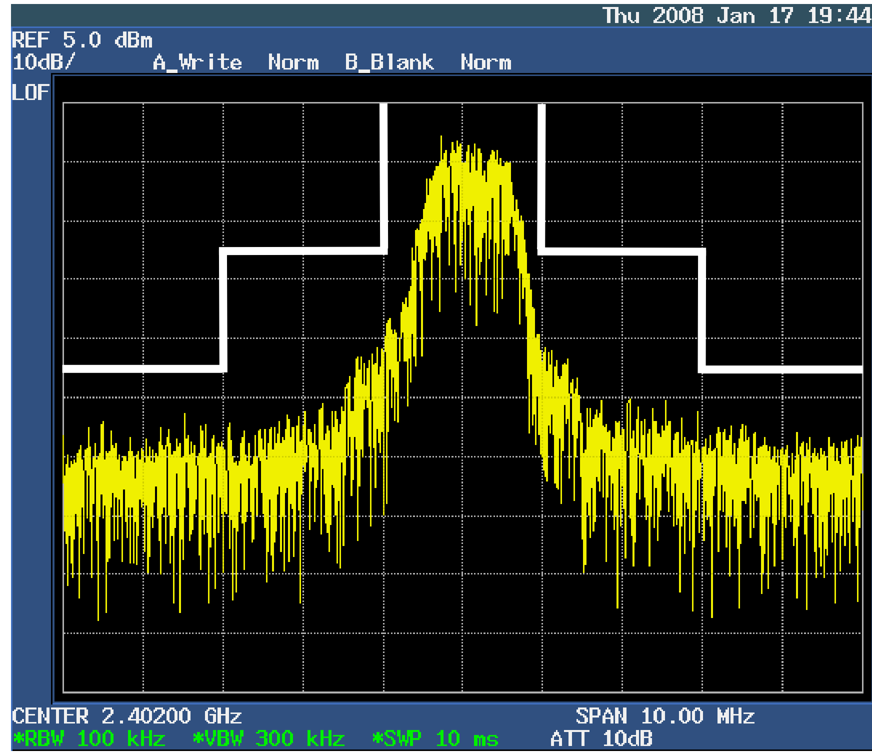
< 25% peak DEVM

99% symbols
< 20% DEVM

- Transmitting 3Mbps packet (8psk) at 2dBm

TX Spectrum measurements





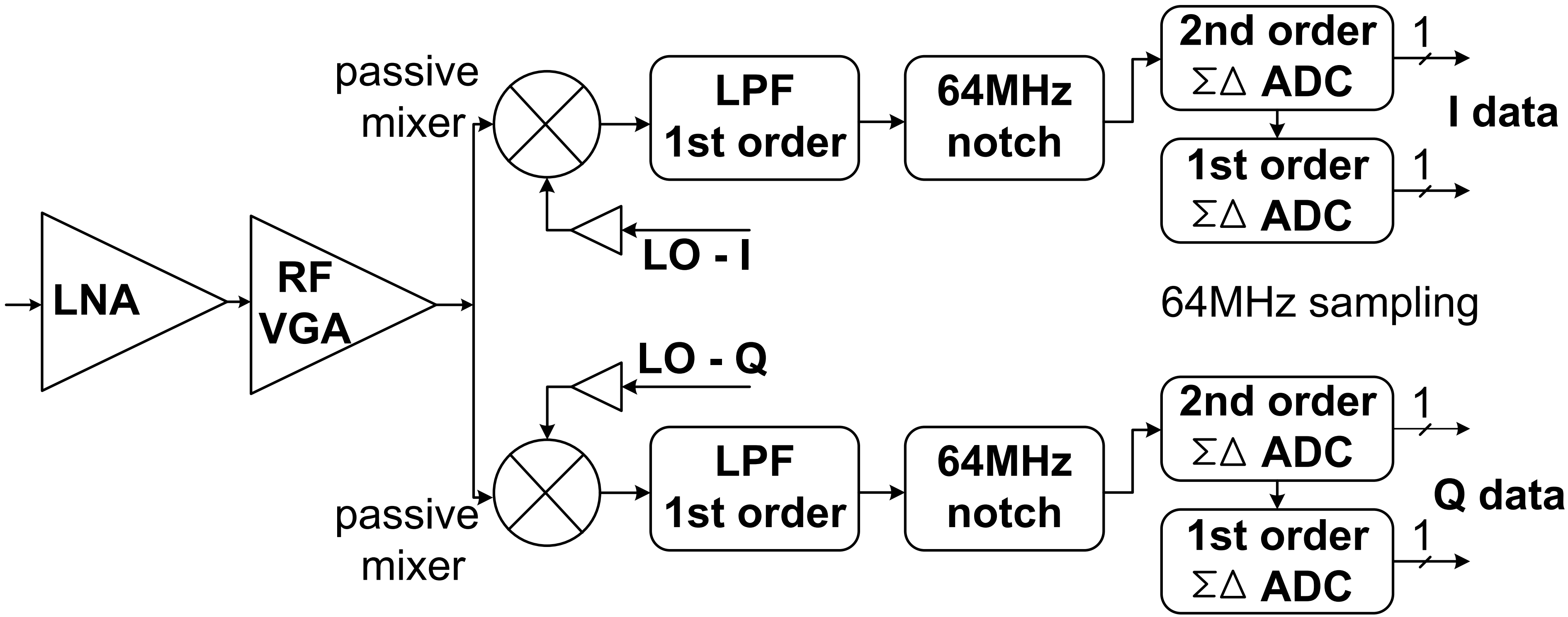
1Mb GFSK Spectrum (2dBm channel power)

3Mb 8PSK Spectrum (2dBm channel power)

RX architecture

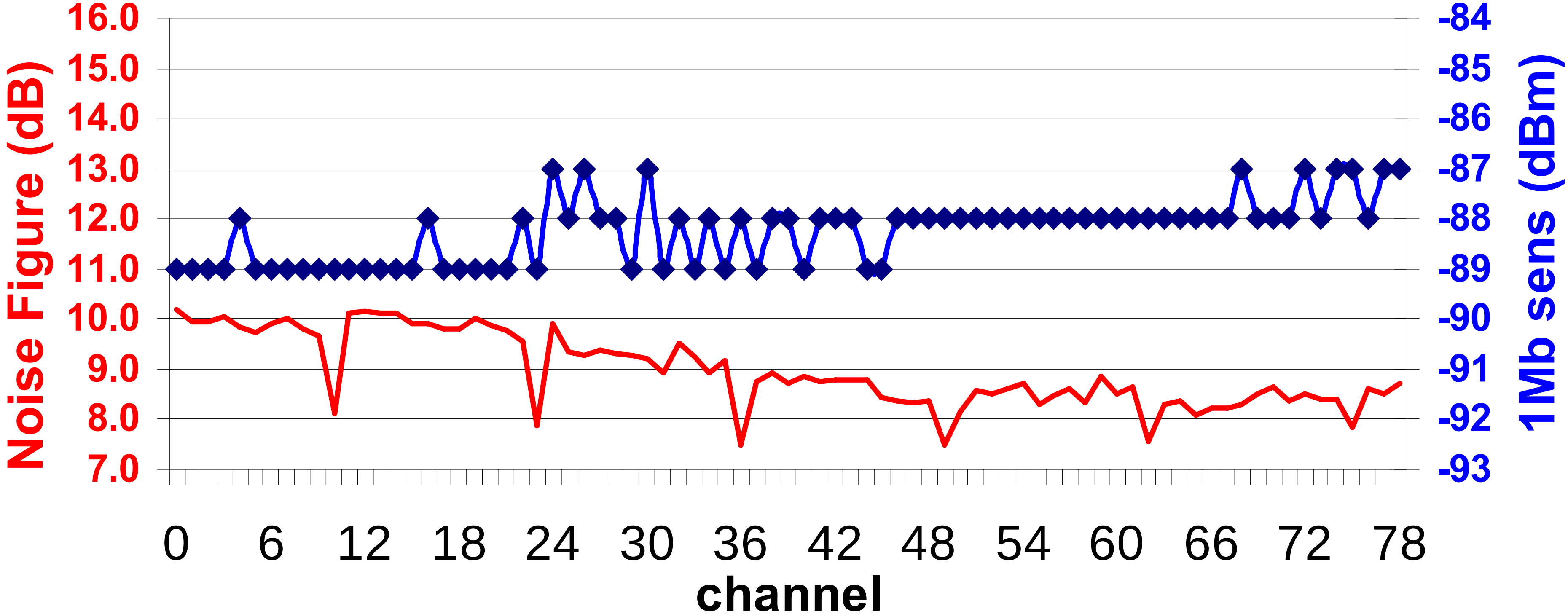
- **500kHz IF optimizes area and power**
  - ➢ Traditional low-IF uses analog BPF → more area
  - ➢ Direct conversion overlaps signal and DC offset → signal detection challenge
  - ➢ 500kHz IF analog components similar to zero-IF → both area efficient and robust
- **Minimal analog filtering**
  - ➢ ΔΣ ADC has 74dB dynamic range
  - ➢ Modem removes DC offset and close-in blockers
  - ➢ LPF and notch prevent ADC saturation and aliasing

RX block diagram



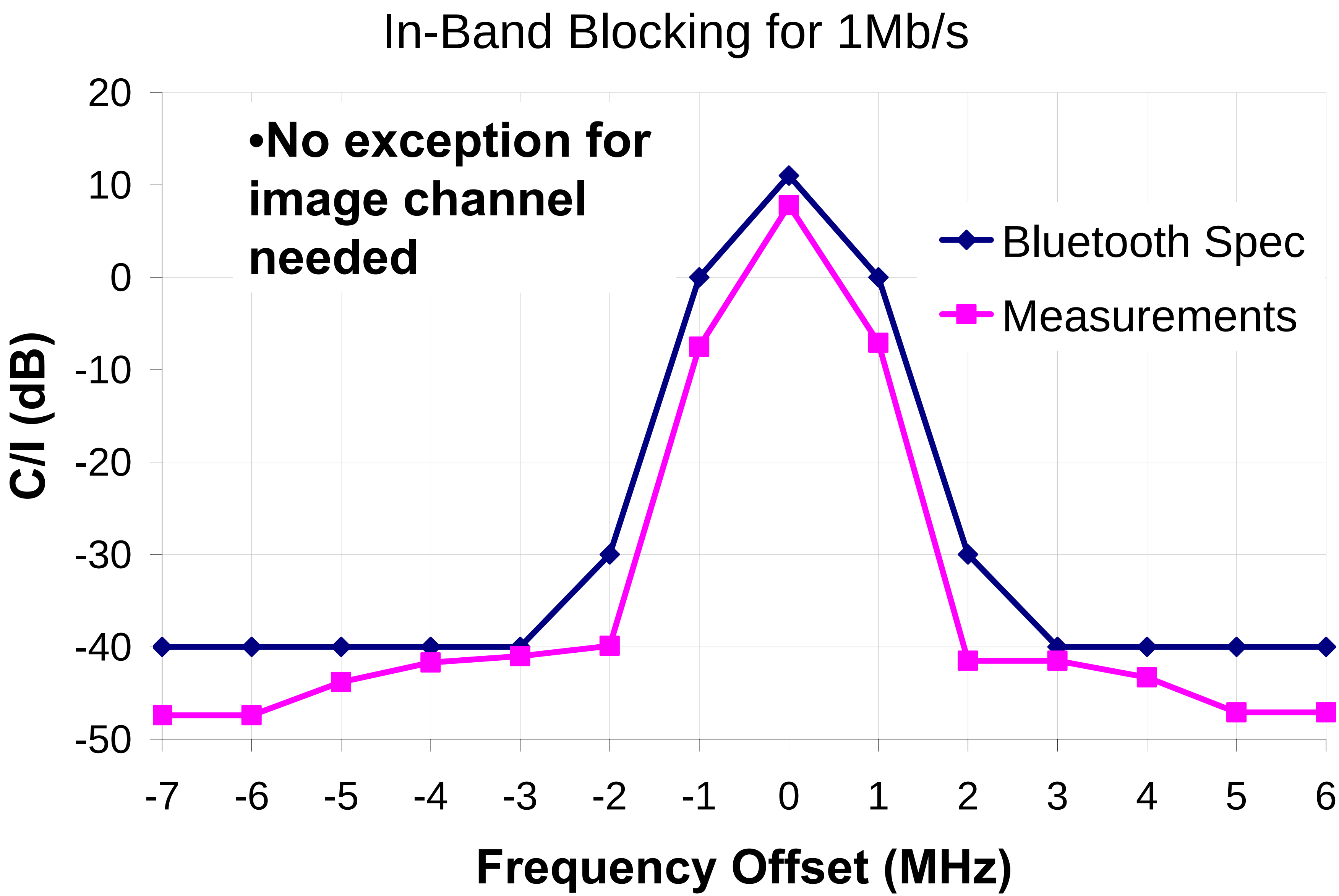
- Similar to zero-IF

RX performance

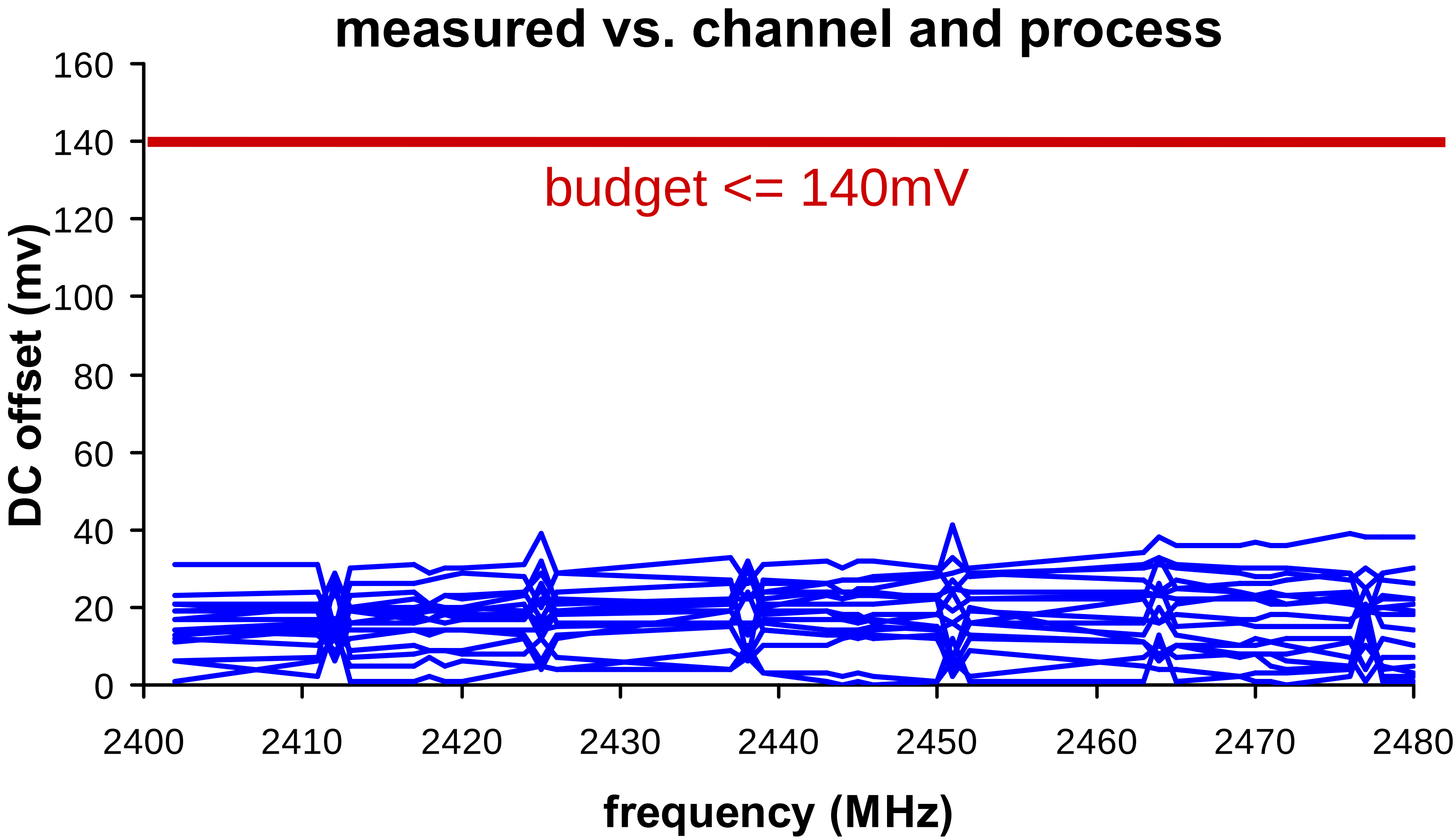


- **Battery life is more important than range!**
  - **-88dBm sensitivity @ 1Mb requires 12dB NF**
  - **RX signal path consumes 18.5mW**

RX blocker rejection

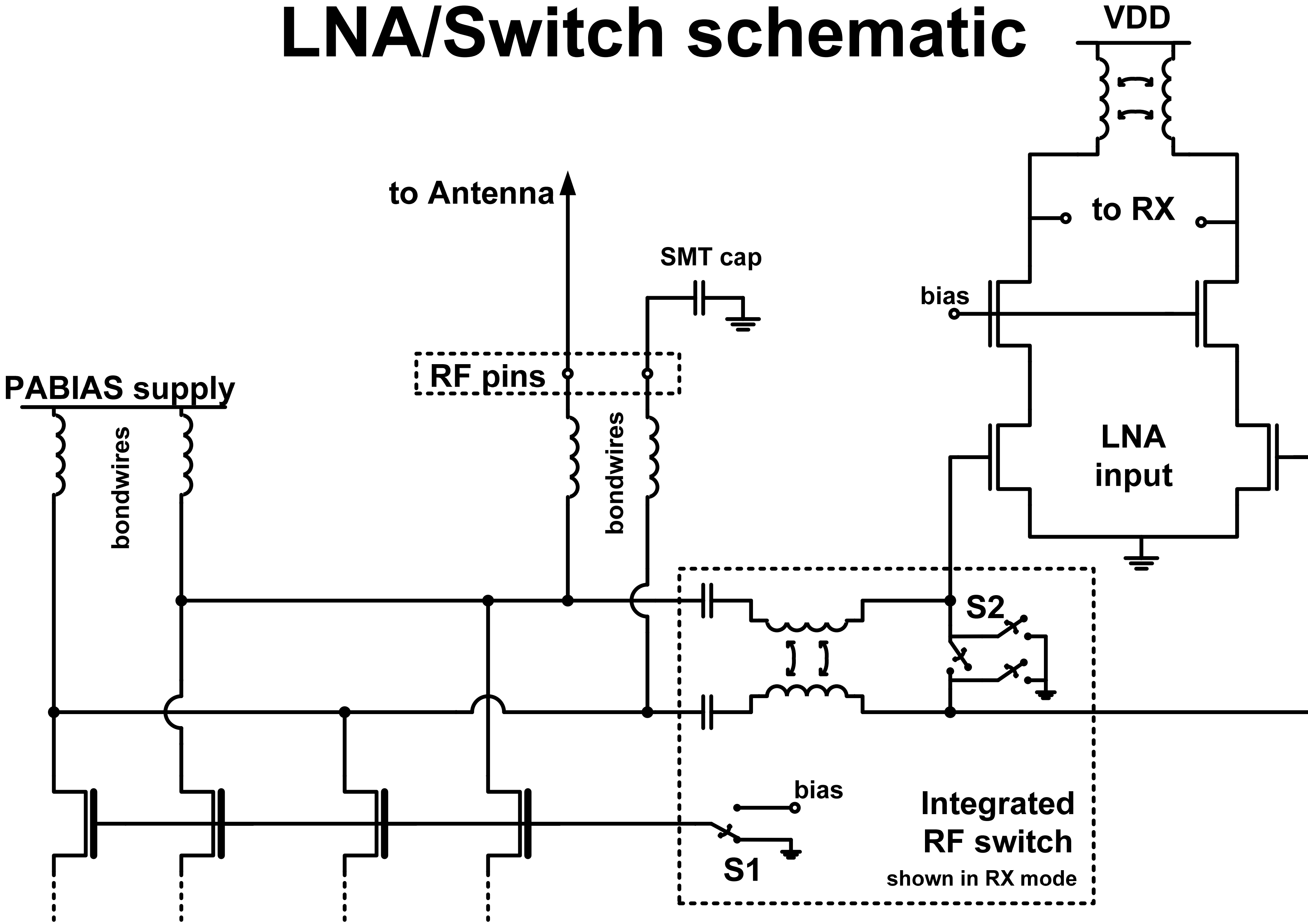


DC Offset



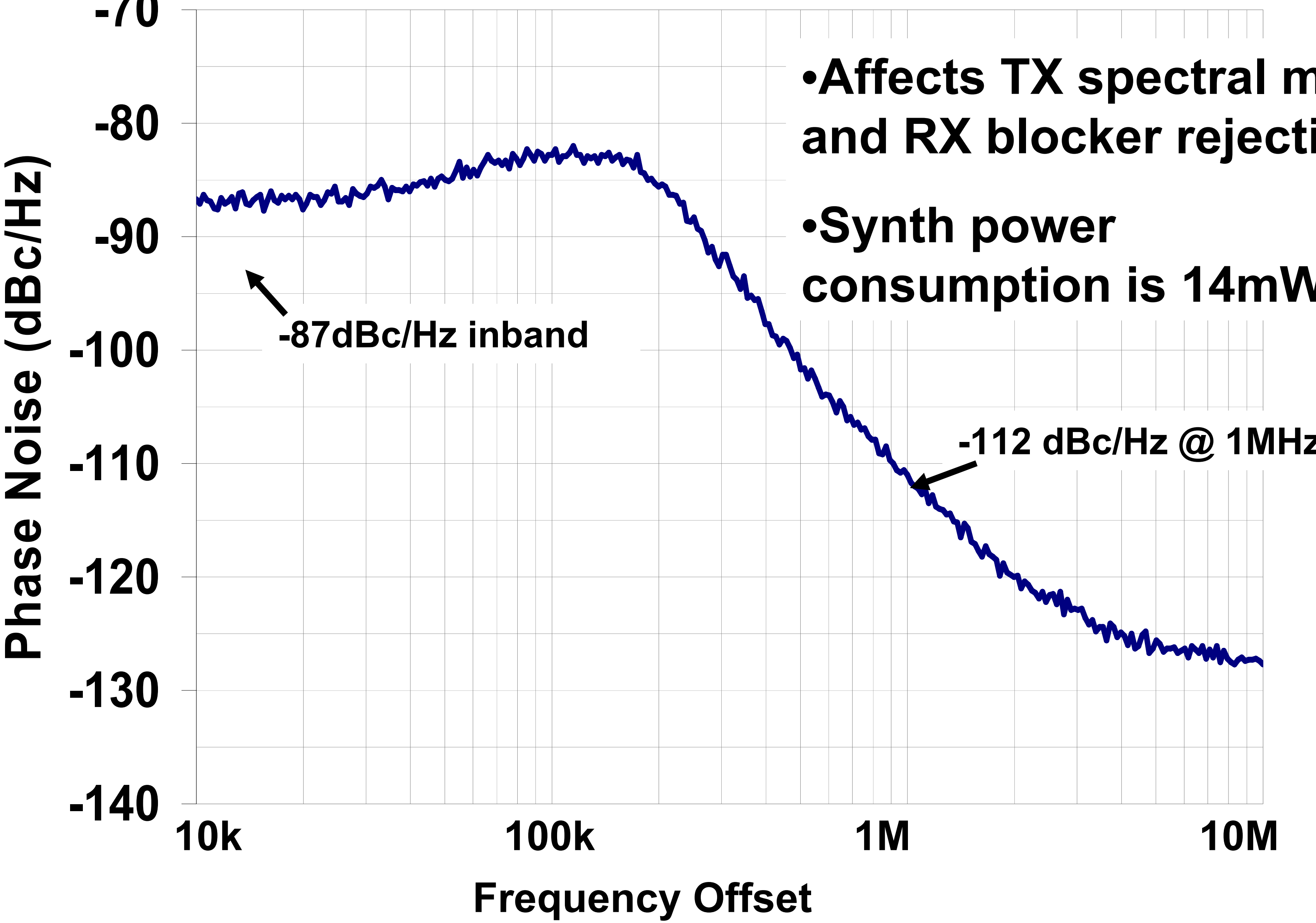
•**Offset is quantized by ADC and removed by modem**

LNA/Switch schematic



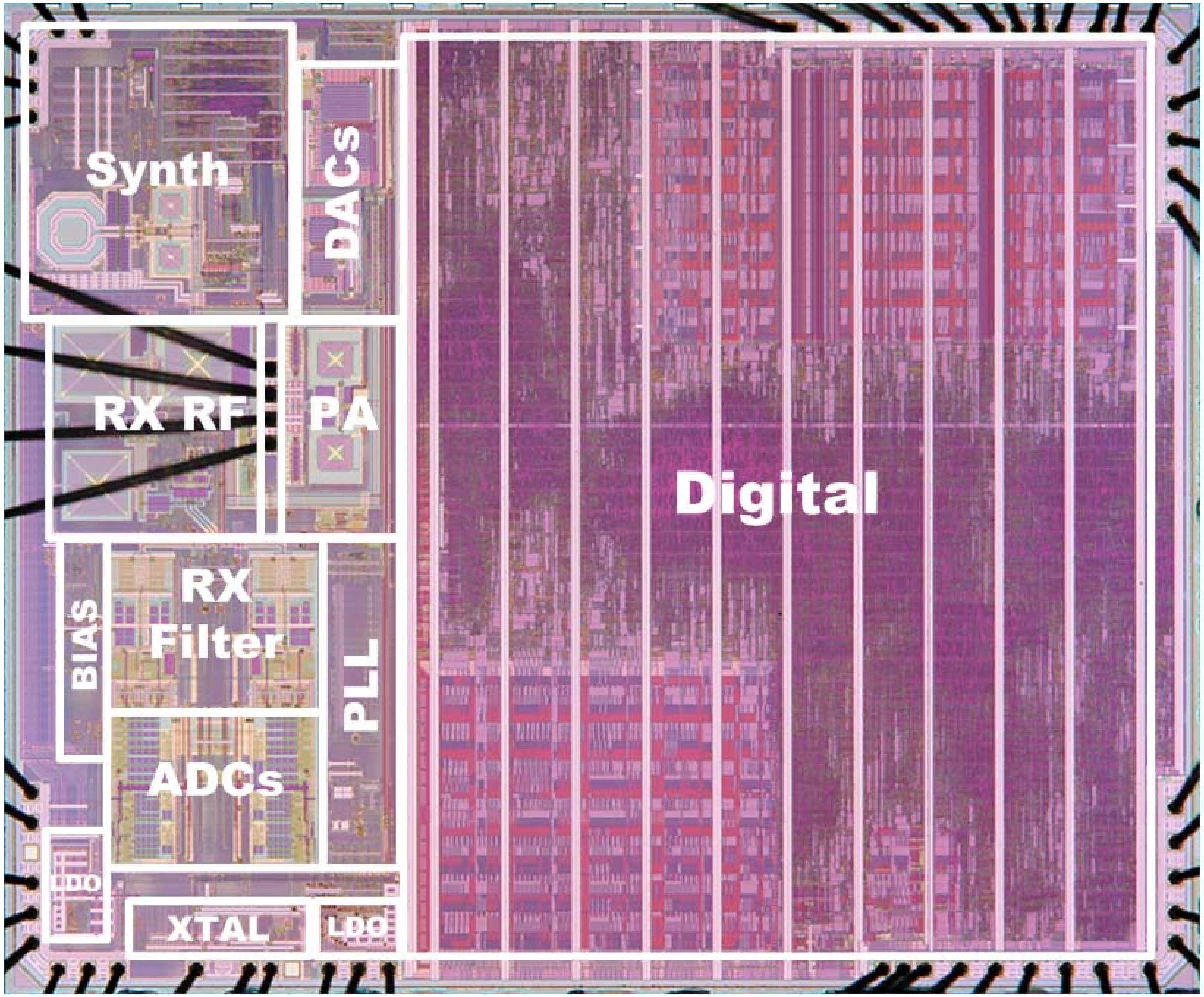
Ref: R. Chang, ISSCC 2007

Phase Noise



- Affects TX spectral mask and RX blocker rejection
- Synth power consumption is 14mW

Die Photo



- 0.13um CMOS
- Standard digital process
- Analog area: $3mm^2$
- Total die size: $9.2mm^2$
- QFN 40pin package

Performance Summary

	This work	
TX output power	2dBm	Class 2 operation
3Mbps Transmit DEVM rms peak	<6% <18%	<13% spec <25% spec
Continuous TX power consumption (All analog/RF functions excluding PA)	19.3mA	1.2V supply
PA power consumption – basic rate EDR	10.1mA 20mA	tested with 3.3V supply voltage
RX sensitivity – 1Mb (GFSK) 2Mb (π/4 DPSK) 3Mb (8PSK)	-88 dBm -90 dBm -84 dBm	-70dBm spec for all rates
RX noise figure	<12dB	
Continuous RX power consumption (All analog/RF functions)	29.7mA	1.2V supply
Die Area SoC including Analog/RF Analog/RF portion only	$9.2mm^2$ $3.0mm^2$	
Technology	0.13um standard CMOS	
Package	5x5 QFN	

Conclusions

- **Demonstrated a single-chip Bluetooth v2.1 SoC supporting EDR**
- **Polar transmitter architecture reduces area**
- **500kHz IF Receiver minimizes analog filtering**
- **Smallest published Bluetooth SoC to date in 0.13um CMOS**

Acknowledgements

An SoC requires more than a radio to succeed.

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