Highly re-configurable RF receivers and challenges towards a true SDR receiver

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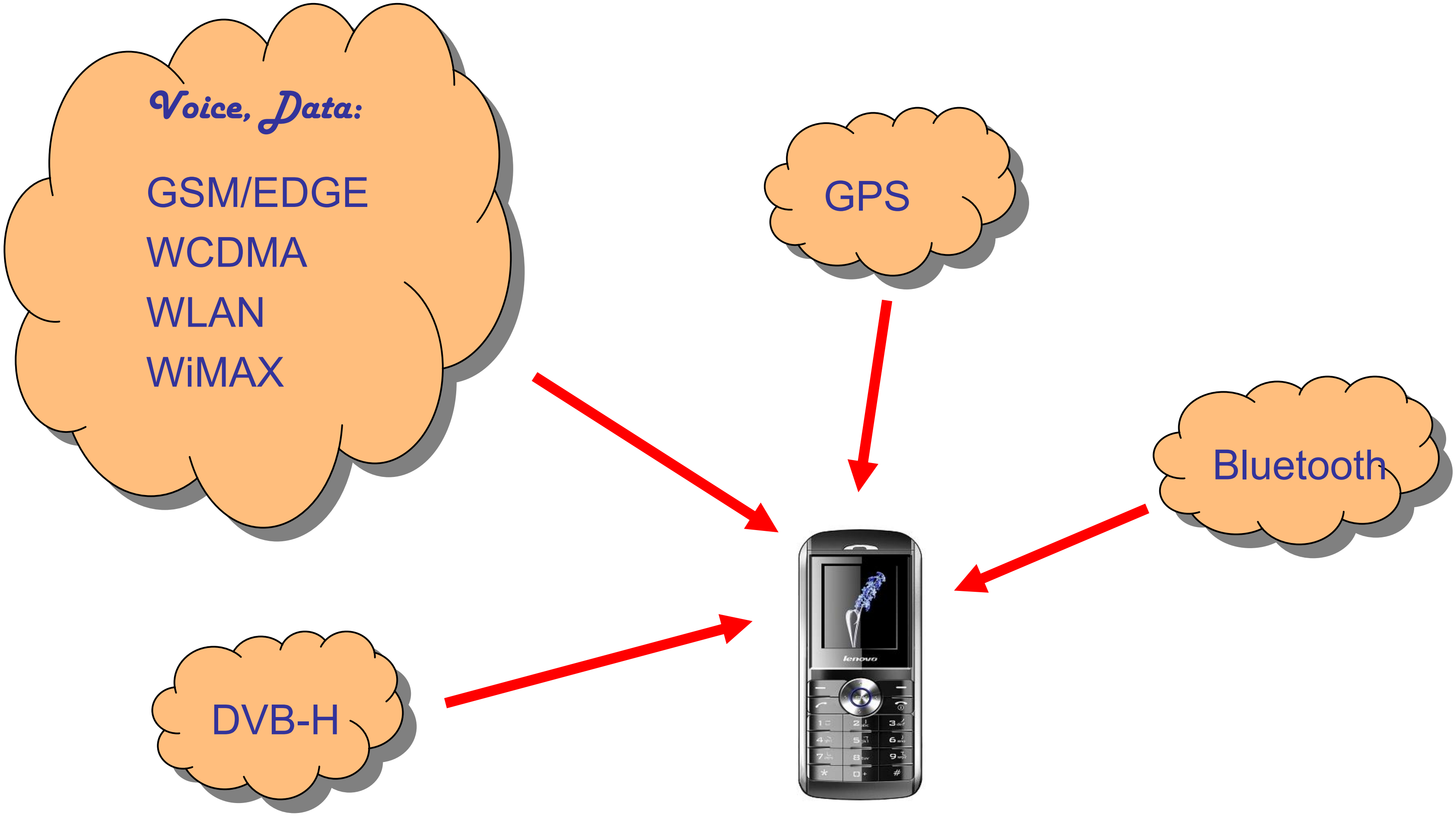
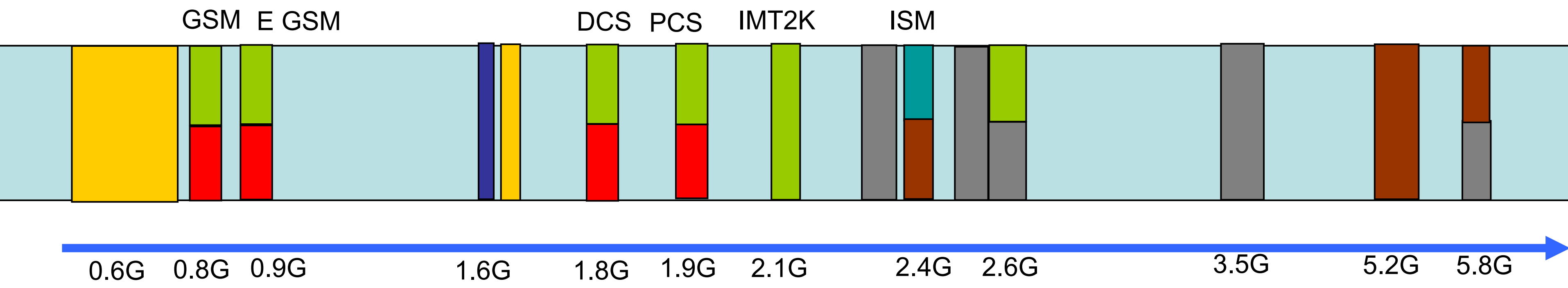
Outline

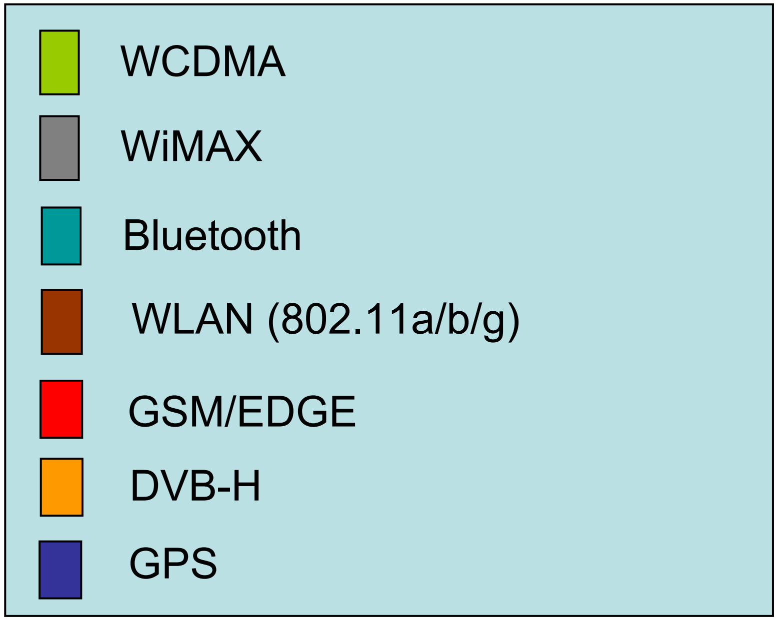
- The need for highly reconfigurable “multi-band, multi-mode” SDR receiver.
- Multi-band receiver: Design directions and challenges.
- Multi-mode receiver: Architecture and design strategy for a re-configurable receiver.
- A WCDMA, GSM/EDGE “multi-mode” RF receiver front-end in 90nm CMOS.
- Conclusion.

Plethora of wireless applications for the mobile terminal



Multiple bands across the frequency spectrum





Multiple receiver bands,

Mobile standards

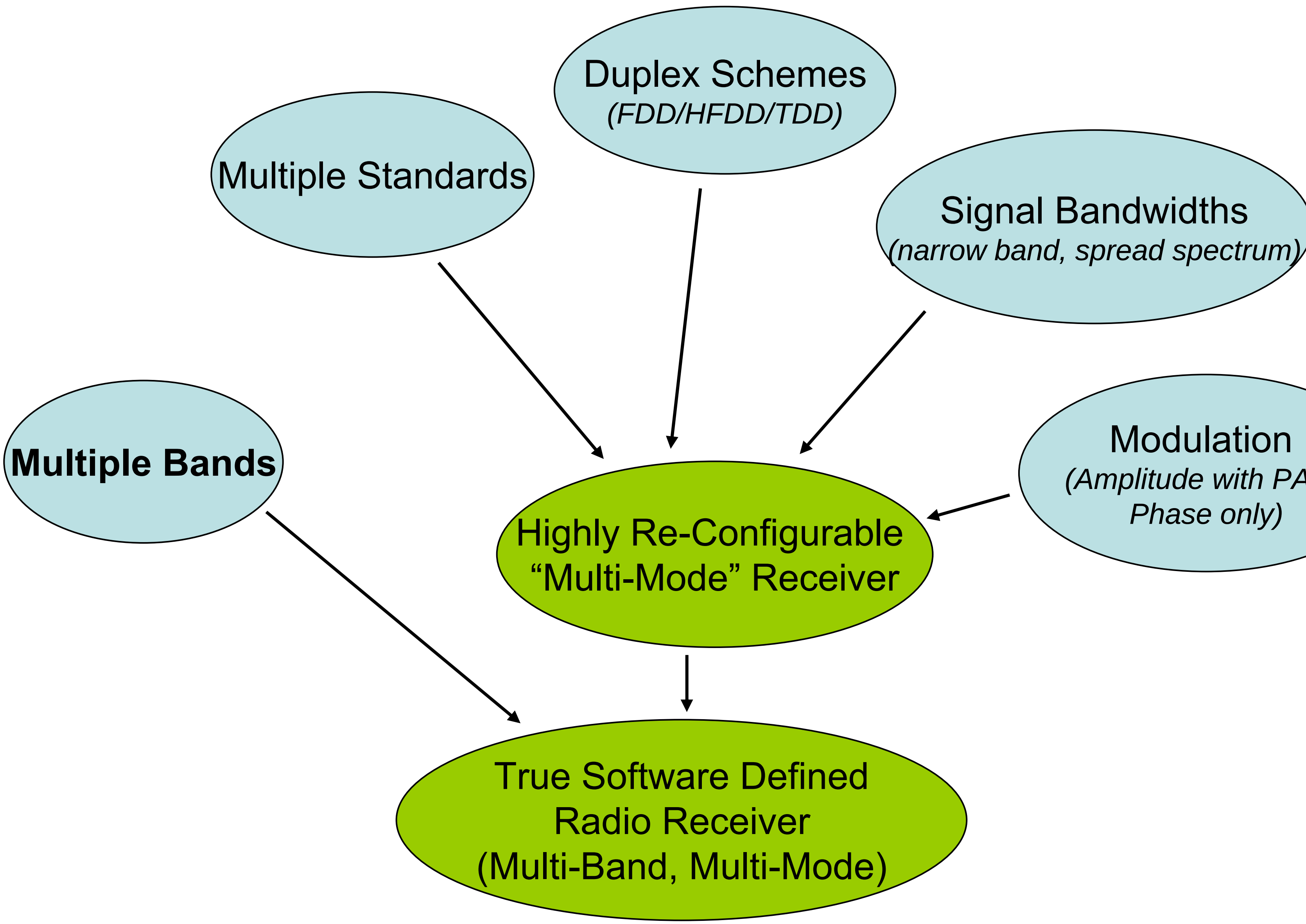
MIMO/Diversity

Co-existence

↓

Need for efficient receiver hardware re-use

Need for receiver hardware re-configurability



Need an agile "multi-band, multi-mode" receiver with programmable performance combinations

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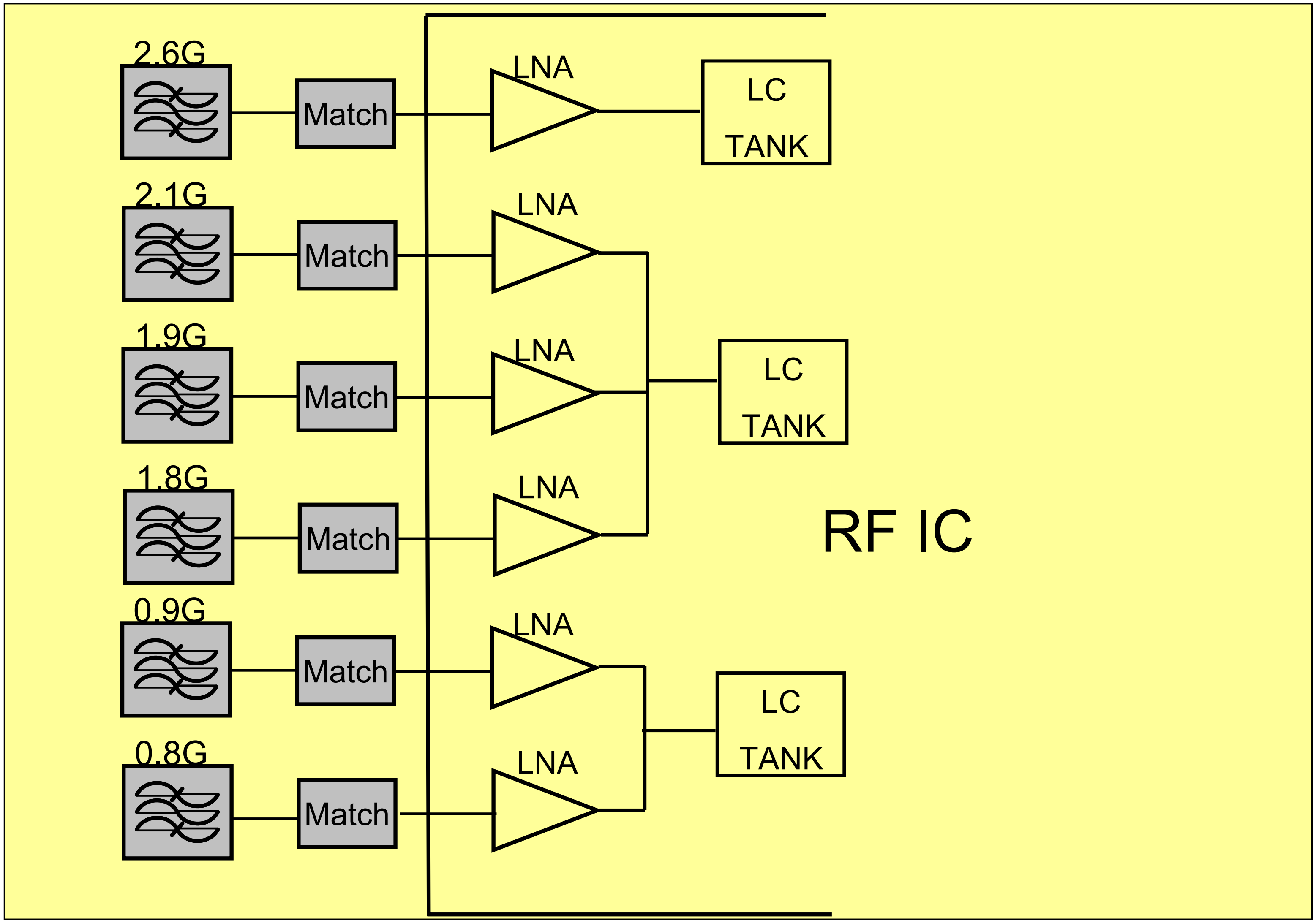
Pre-Select Filter Bottleneck

- Pre-Select Filters (Duplexer/SAW/BAW) are band specific.



- **Dedicated RX input pins, Matching Networks, LNA input stages are required.**

Can we overcome this bottleneck?

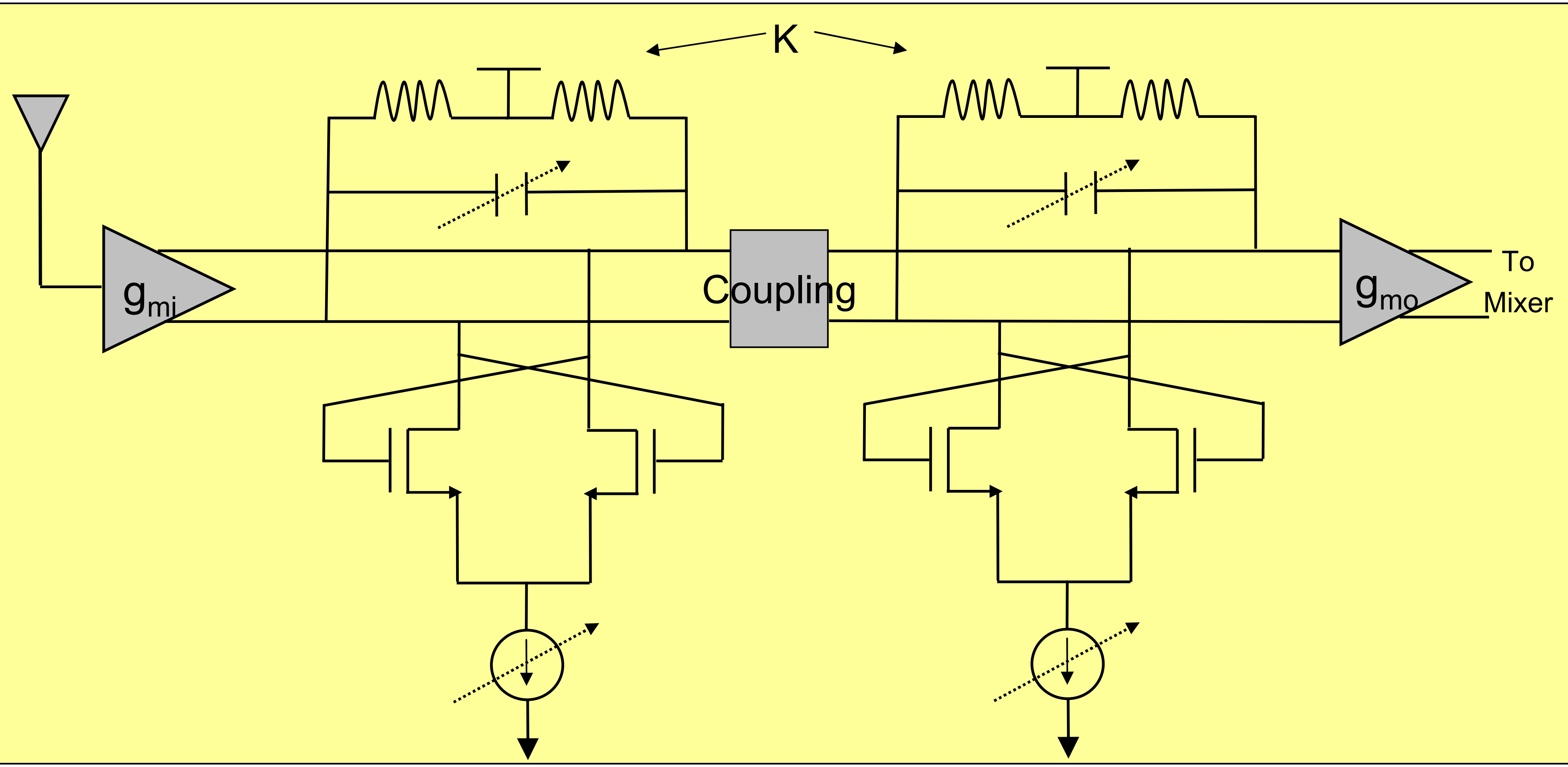
High dynamic range RF ADC

- Nyquist rate as high as 10GHz.
- Dynamic range requirement of 100dB or more.

- Complete spectrum is converted to digital.
- A very powerful receiver!

- State of the art ADCs are not able to meet this required performance.

Integrated Tunable RF Bandpass Filters

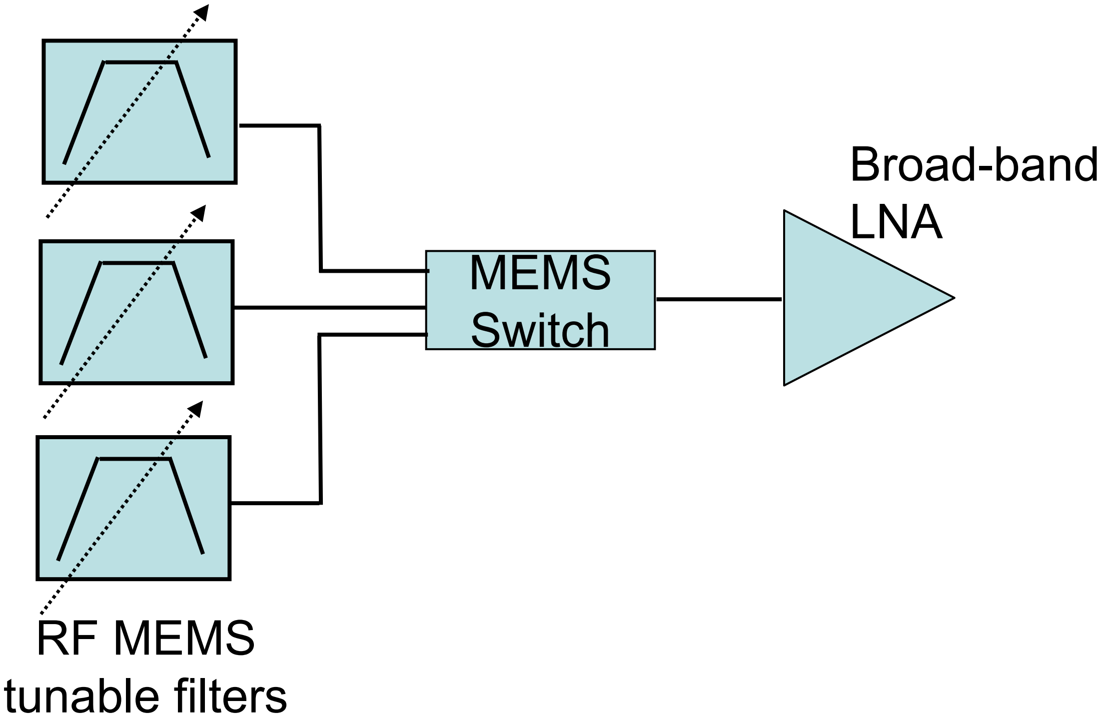


- Dynamic range issues based on low Q of on-chip inductors.
- Issues with channel based tuning and tuning range.
- Input g_m linearity is still an issue.

[Ref] Kuhn, W.B.; Yanduru, N.K.; Wyszynski, A.S., "Q-enhanced LC bandpass filters for integrated wireless applications", IEEE-MTT Dec. 1998.

RF filtering using MEMS

- MEMS based RF filters using switchable capacitors for tuning have been shown.
- Low loss switches using MEMS can be used to switch between various RF filters.

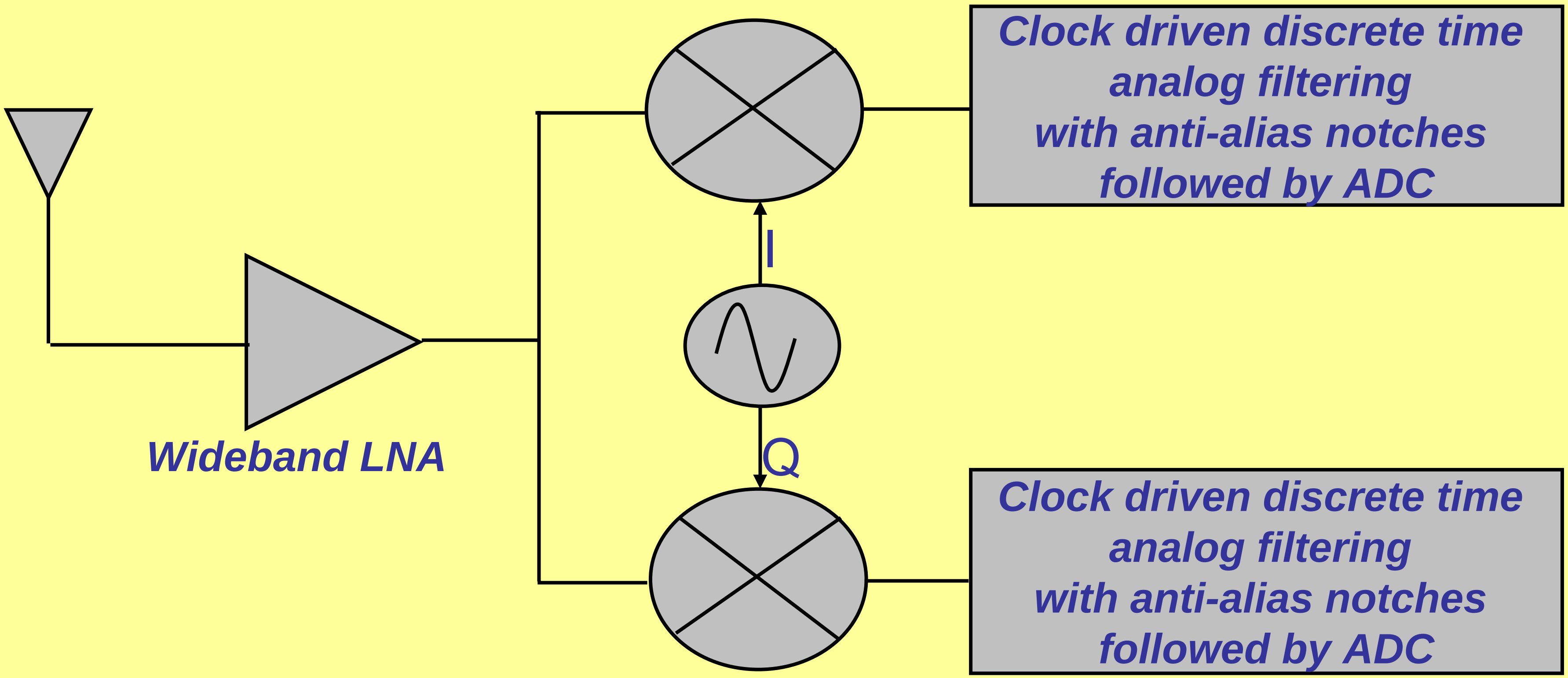


- Issues such as reliability, yield and complexities in integrating mechanical structures with transistors need to be considered.

[Ref] Nguyen C. T –C, "RF MEMS in wireless Architectures", DAC 2005.

[Ref] S.-J Park, K.-Y Lee, G.M. Rebeiz, "Low-Loss 5.15 to 5.70-GHz RF MEMS Switchable Filter for Wireless LAN Applications" IEEE-MTT, Nov. 2006.

Clock driven discrete time filtering after RF down conversion

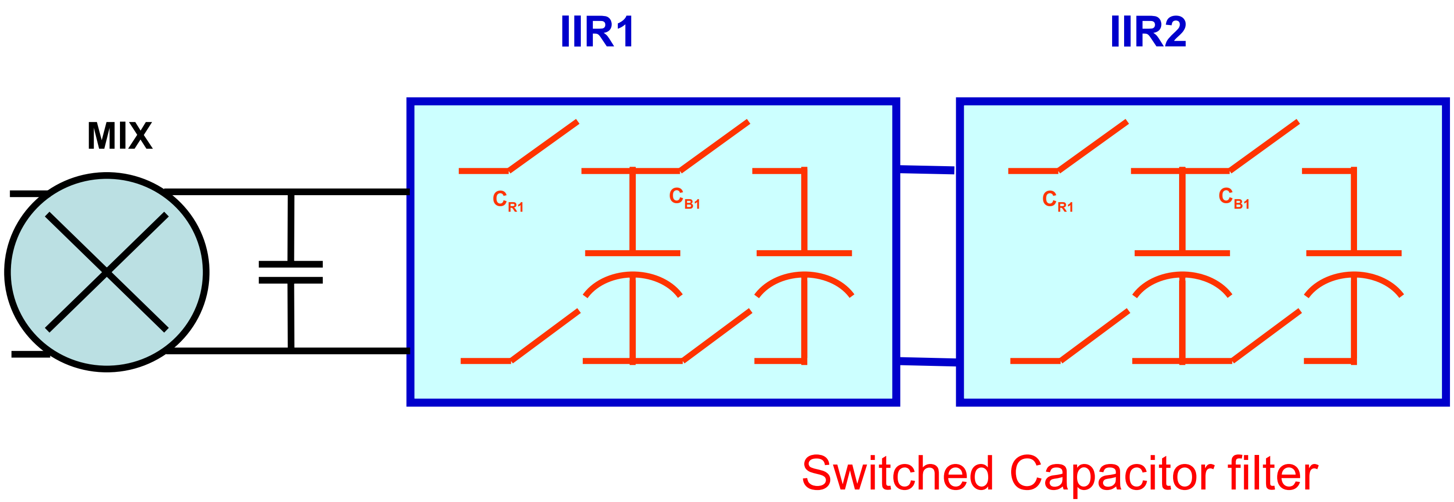


- **Input linearity of the LNA and Mixer in the absence of any RF filtering needs to be addressed.**

[Ref] Abidi, A. A., "Evolution of a Software-Defined Radio Receiver's RF Front End," IEEE *RFIC Symposium 2006.*

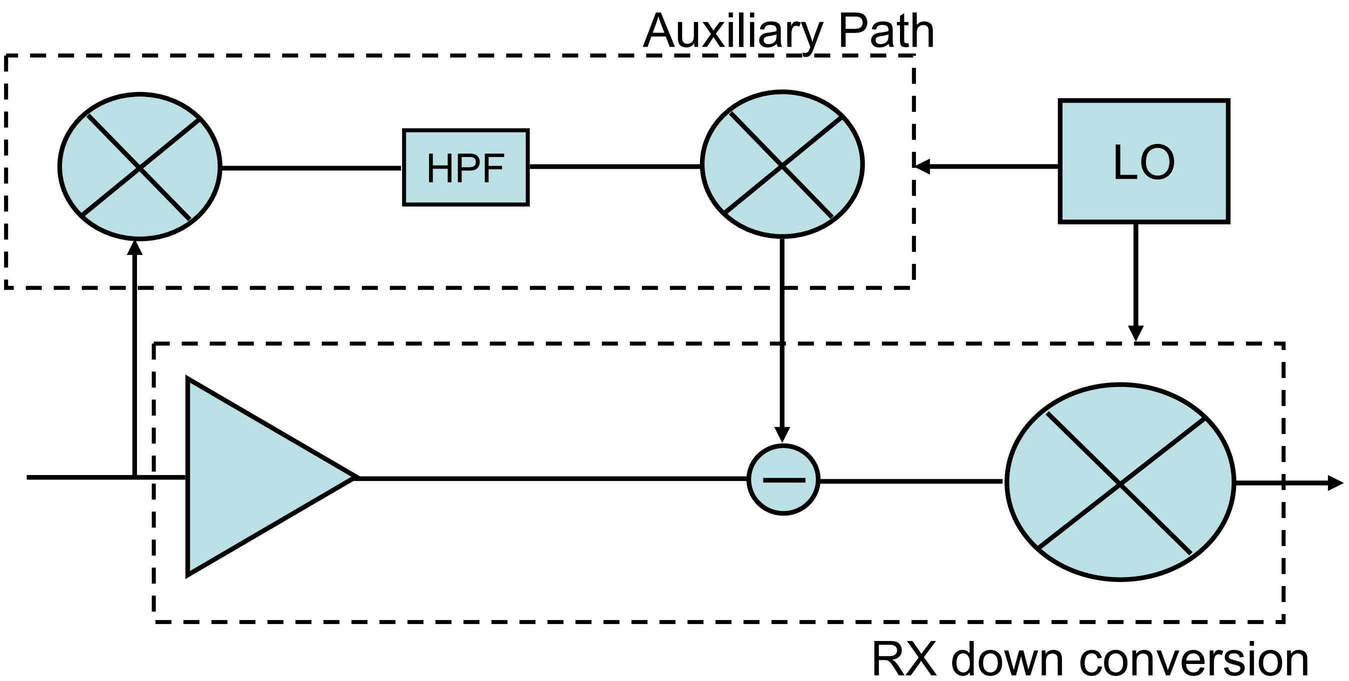
[Ref] Muhammad, K., et al, "The First Fully Integrated Quad-Band GSM/GPRS Receiver in a 90-nm Digital CMOS Process" IEEE JSSC, Aug. 2006.

Discrete time analog filtering (cont.)



- Advantages
  - Digital process friendly base-band filtering.
  - Easy programmability of base-band filtering between modes and for notches.
- Disadvantages
  - **Main issue of linearity of LNA, mixer needs to be addressed.**

Feed forward cancellation of blockers



- Advantages
  - Removes in-band and out-of-band blockers.
  - Relaxes linearity for the Mixer.
- Disadvantages
  - Mismatch issues with gain and phase inversion between the main and aux. path.
  - LNA linearity still a challenge,
  - Phase noise requirement is shifted to up-conversion mixer of Aux. path.

[Ref] R. Gharpurey, S. Ayazian, “Feedforward Interference Cancellation in Narrow-Band Receivers” 2006 IEEE Dallas/CAS Workshop, Oct. 2006.

[Ref] H. Darabi, “A Blocker Filtering Technique for Wireless Receivers”, ISSCC 2007.

Some other approaches including blocker detection using fast RSSI and subsequent reduction in RF gain have been investigated.

But these schemes along with other schemes discussed are not able to match the RF performance of a receiver with pre-select filter.

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Direct Conversion as Receiver Architecture

Advantages:

- Reduced hardware (Image rejection/filtering, Signal processing, Synthesizer)

Issues:

- Second order inter-modulation/“self-mixing” issues with modulated blockers.
- Flicker noise.
- LO leakage and dc offsets.

A “Near-Zero or Low-IF” architecture can be used if image rejection requirements are not too difficult.

2^{nd} order inter-modulation distortion in direct conversion receiver

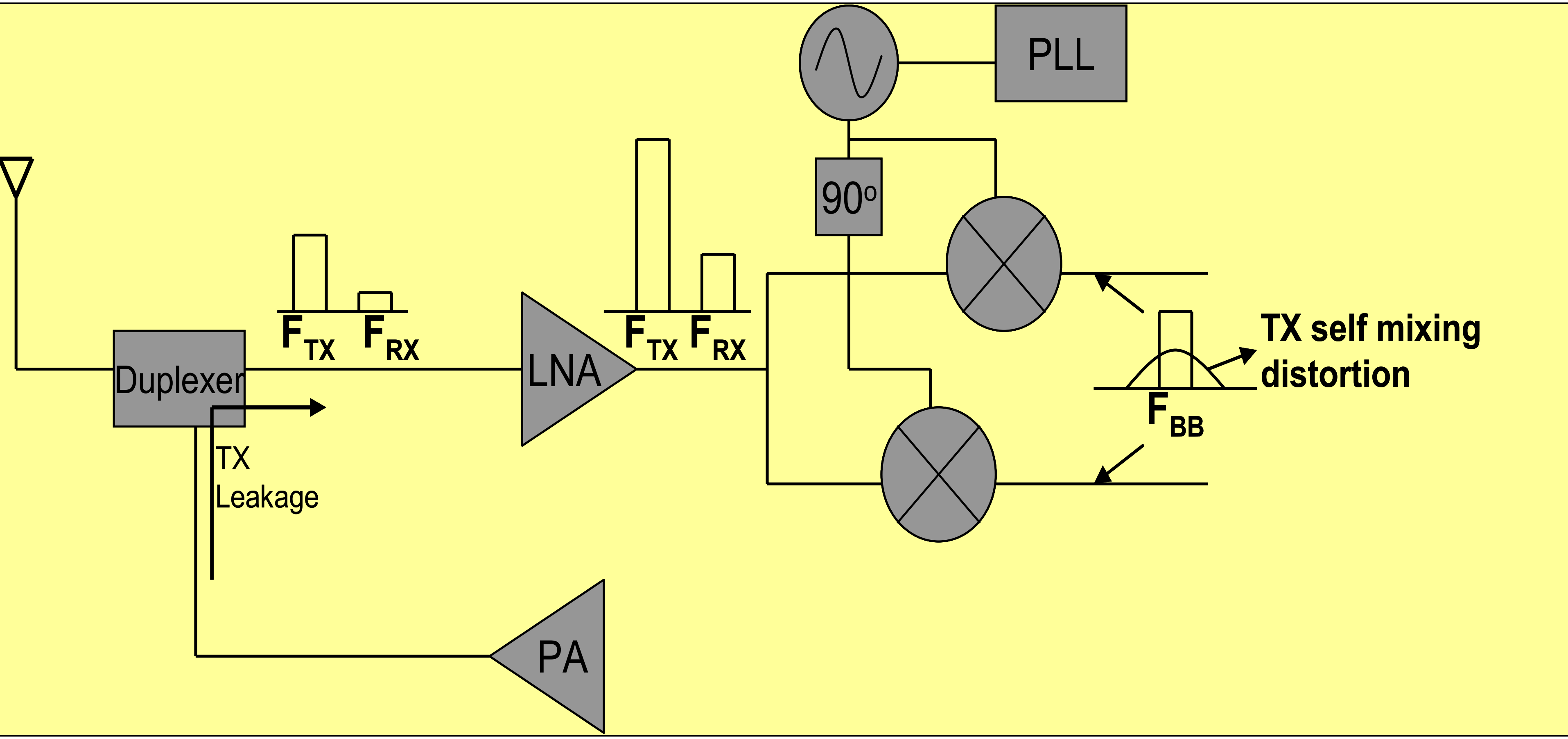
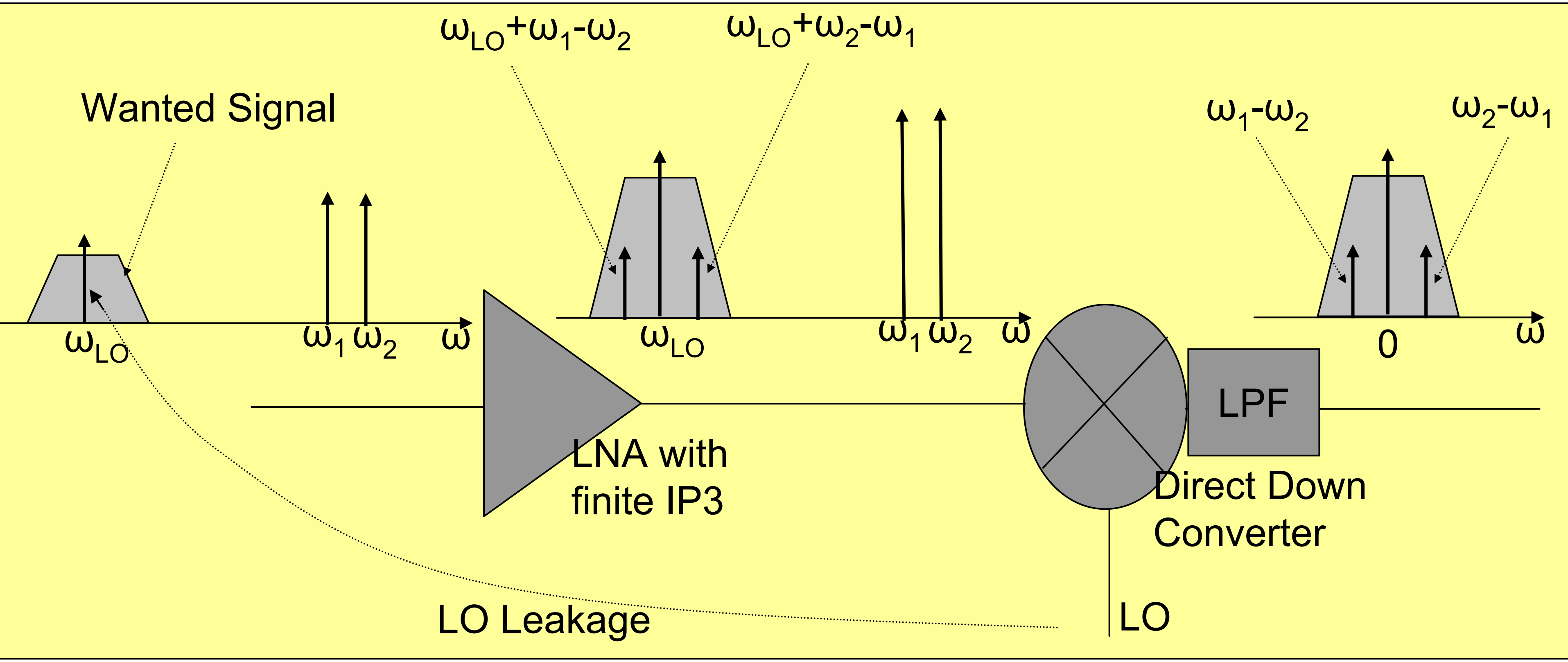


Figure showing IM2 distortion from modulated TX blocker in FDD mode.

Any modulated blocker with non-constant envelope (AM) causes this distortion.

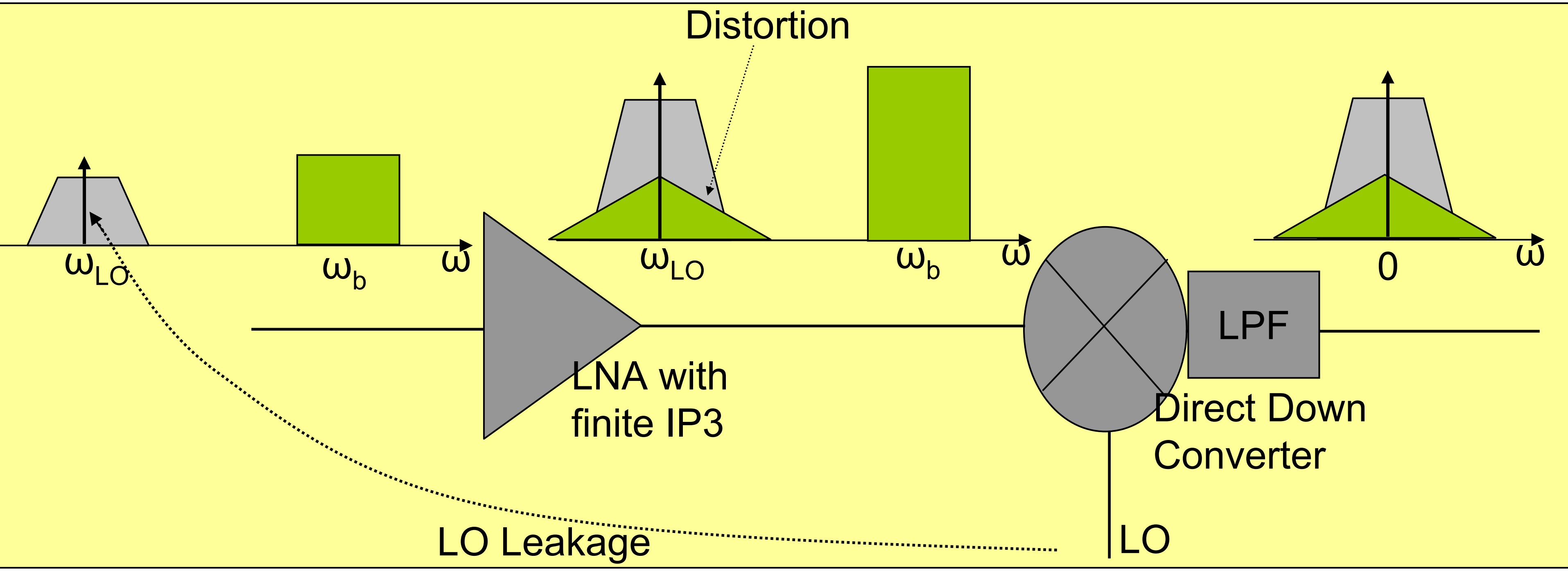
Distortion in the presence of LO leakage in Direct Conversion Receivers (1)



ω_1-ω_2 , ω_2-ω_1 at the output of the mixer looks like an IM2 component.
(Can misleadingly imply an IP2 issue!)

But really it is the LO leakage and IP3 that is the problem!

Distortion in the presence of LO leakage in Direct Conversion Receivers (2)



Distortion caused by an AM blocker will have similar issue like the two tone case shown earlier.

Performance re-configurability in RF front end

- A high dynamic range RF Front End design is the starting point.
- Need to be able to program this front end for various combinations of noise/linearity/power.
- Need to have little degradation in overall performance between various programming modes.

Linearity/(Noise*Power) ~ Constant

- High Linearity mode – FDD mode, higher input signal conditions.
- Low Noise mode – TDD mode, sensitivity conditions.
- Low Power mode – high input signal, low level of blockers.

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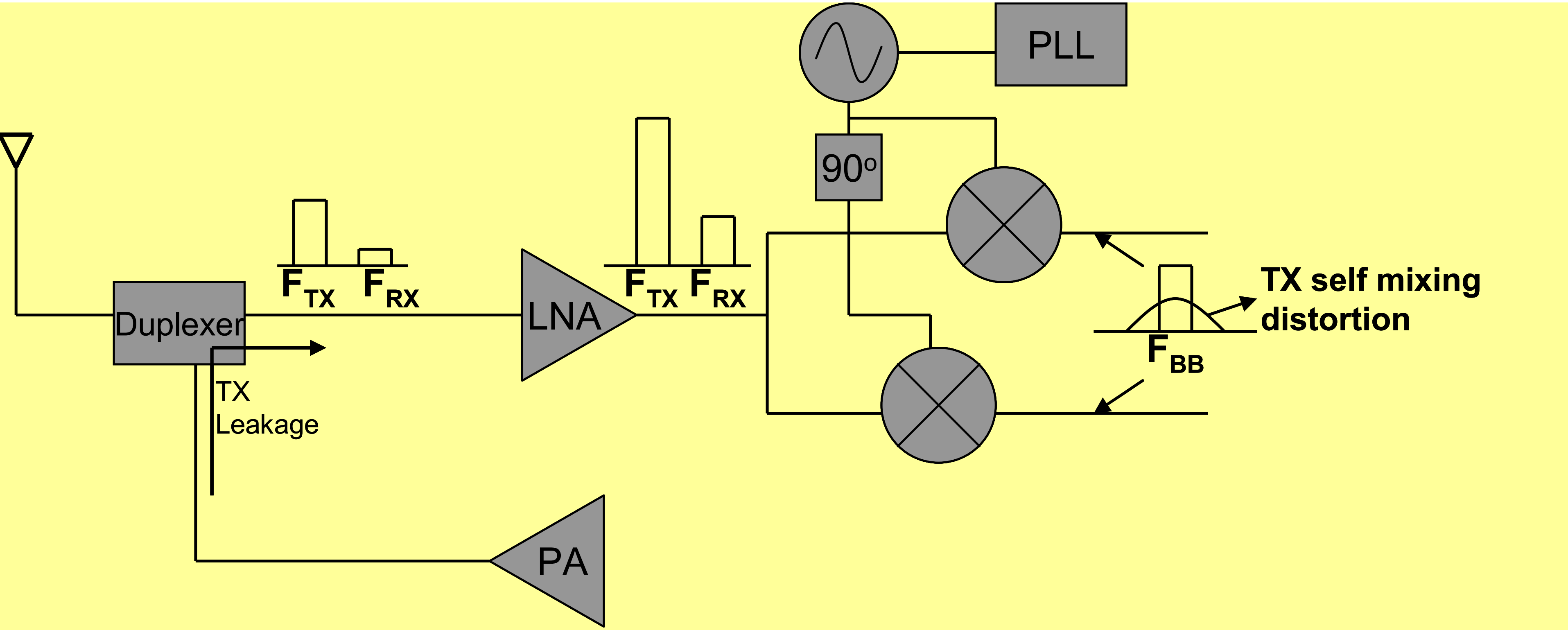
A WCDMA, GSM/GPRS/EDGE “multi-mode” RF Receiver Front End in 90nm CMOS

Linearity bottleneck in WCDMA receiver - IIP2 based on TX leakage



Input IP2 = $2P_{TX} - P_{IM2}$ – "Adj_N"

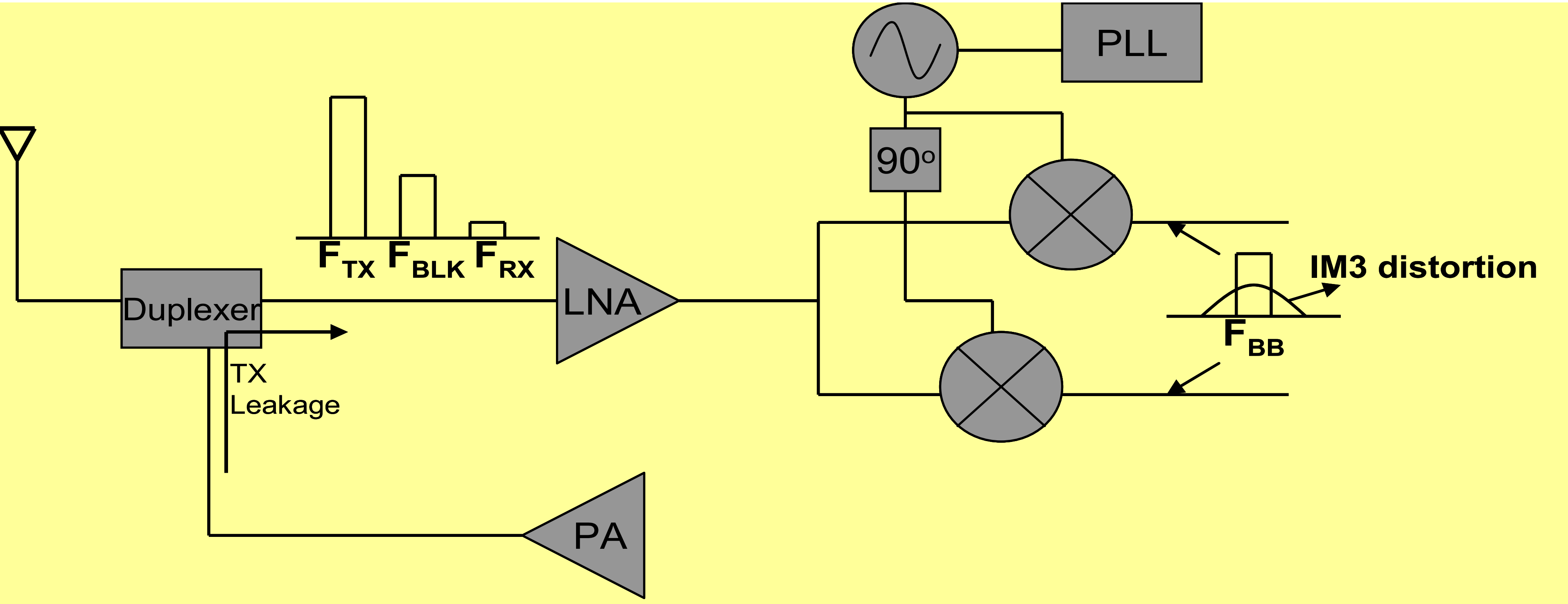
Where,

P_{IM2} is the input referred IM product;

"Adj_N" is the adjustment factor which depends on no. of channels in the TX leakage

[Ref] Khan, M.S.; Yanduru, N., "Analysis and Measurement of Self Mixing of Transmitter Leakage in WCDMA Receivers," *IEEE-RWS 2007.*

Linearity bottleneck in WCDMA receiver - IIP3 from TX leakage, blocker



Input IP3 = $(2P_{BLK}+P_{TX}-P_{IM3}+$ "Adj_N"$) / 2$

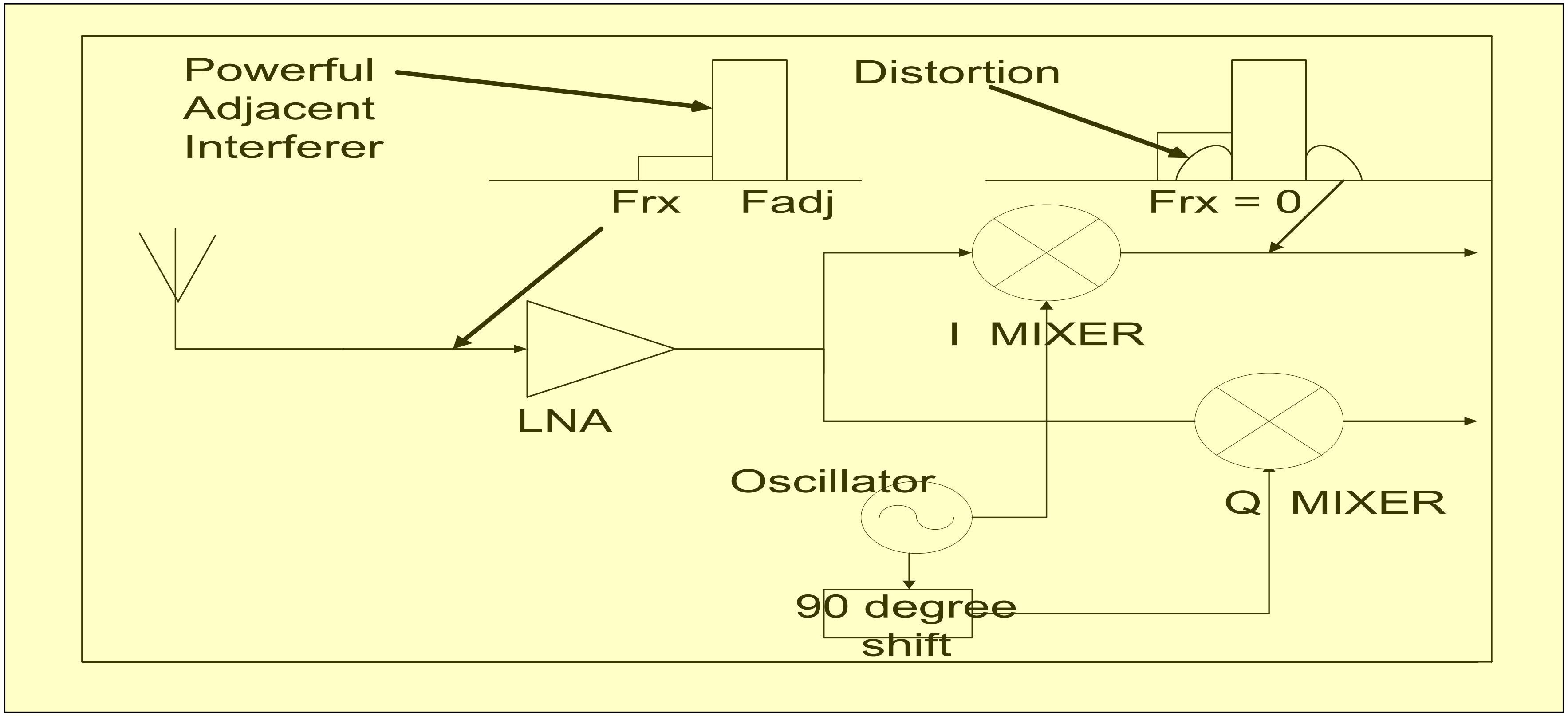
Where,

P_{IM3} is the input referred IM product;

"Adj_N" is the adjustment factor which depends on no. of channels in the AM blocker.

[Ref] Khan, M.S.; Yanduru, N., "Analysis of Signal Distortion due to Third Order Non-Linearity in WCDMA Receivers," *IEEE ISCAS 2006.*

Spectral re-growth of WCDMA adjacent channel



Input IP3 = $(3P_{ADJ} – P_{IM} + \text{“Adj\_N”}) / 2$

Where,

P_{IM} is the input referred Spectral re-growth product;

“Adj_N” is the adjustment factor which depends on no. of channels in the AM blocker.

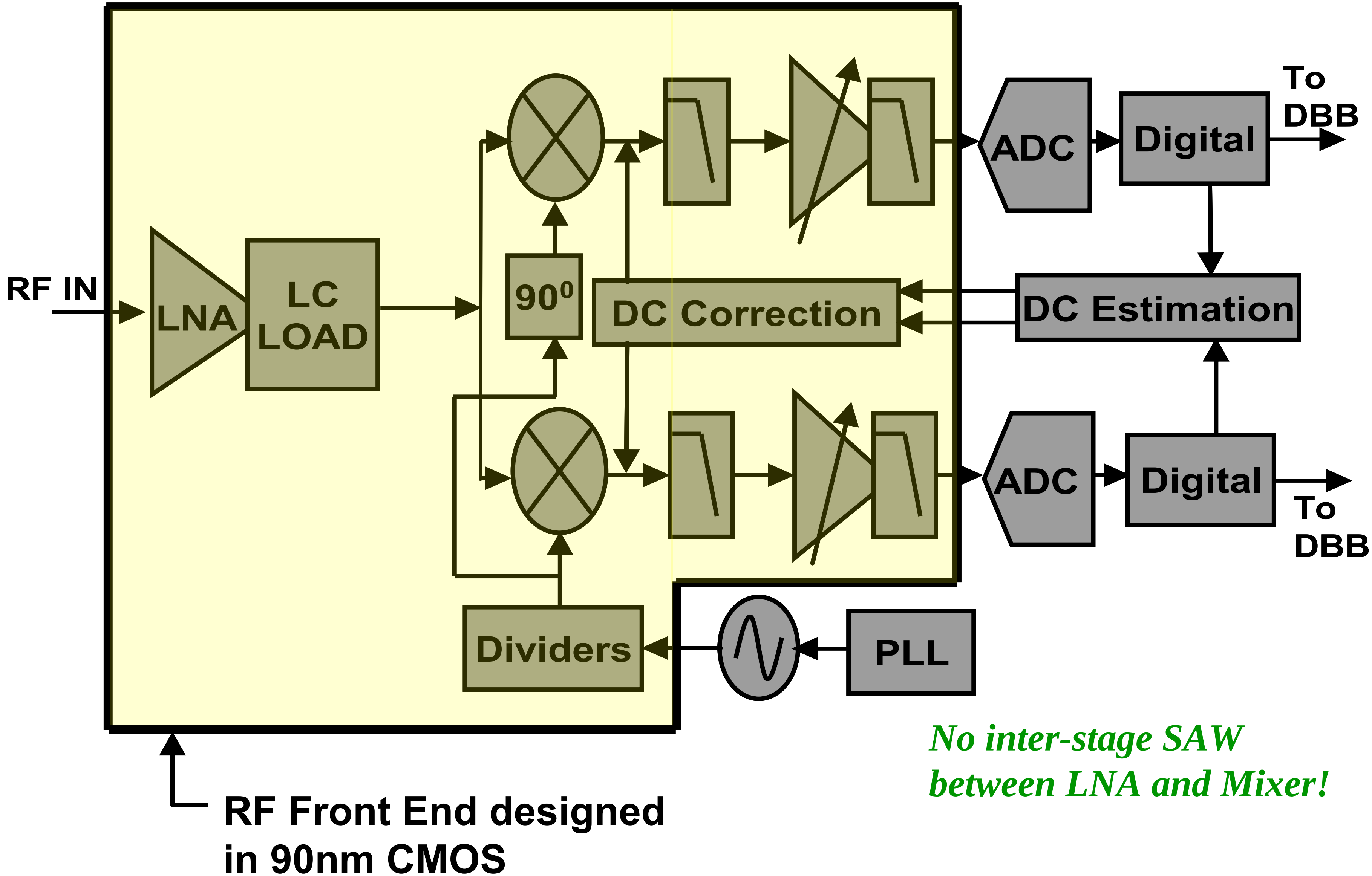
Khan, M.S.; Yanduru, N., “Signal Distortion Due To Spectral Re-Growth of Adjacent Channel Interferers in WCDMA Receivers,” *IEEE-RWS 2007.*

Key RF Performance Specifications

RF Parameter	GGE Mode (GSM/GPRS/EDGE)	WCDMA Mode	Units
NF	2.5	3.0	dB
IIP3	-18	-7	dBm
IIP2	40	44	dBm
Signal Bandwidth	0.2	3.84	MHz

- Higher LNA gain in GSM mode
- Adjust base band filter corner based on signal bandwidth
- Trade IP3 with current in GSM mode.

Receiver Block Diagram



No inter-stage SAW between LNA and Mixer!

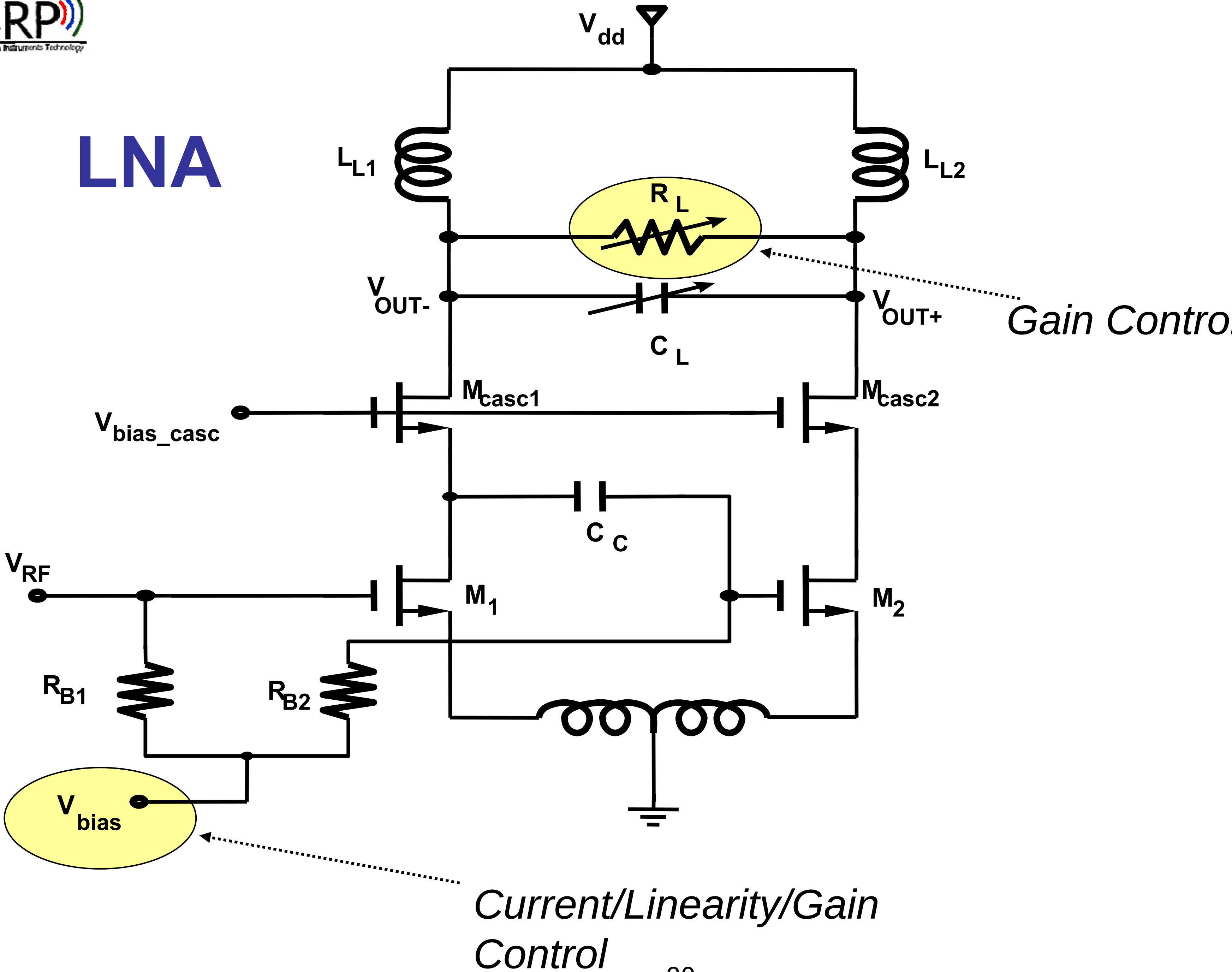
[Ref] Yanduru, N. K, et al, “A WCDMA, GSM/GPRS/EDGE Receiver Front End without Interstage SAW Filter,” IEEE *RFIC Symposium 2006*,

Pros & Cons

- Pros
  - + Design in 90nm CMOS
  - + Highly integrated receiver

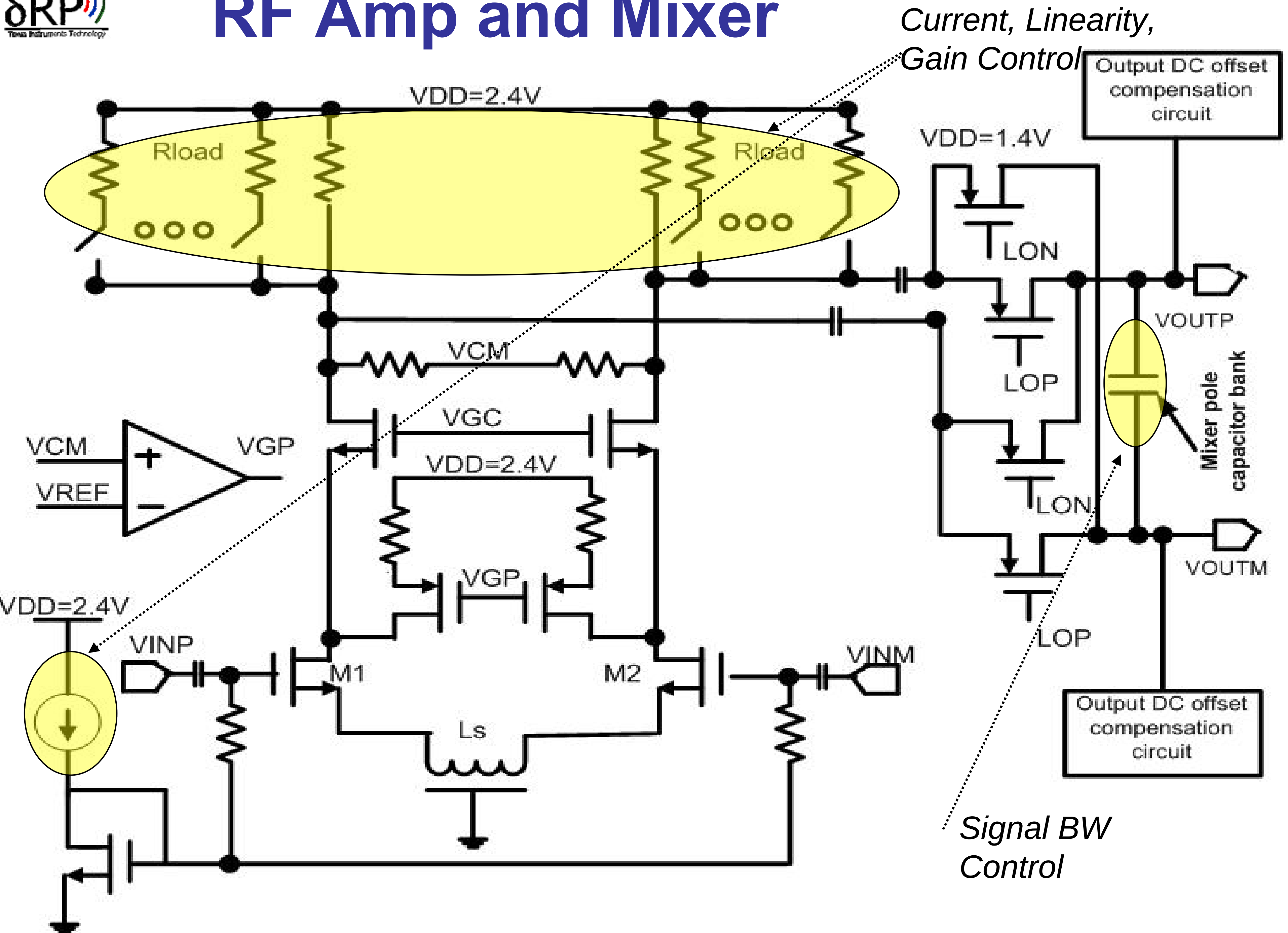
- Cons
  - – Uses 2.4V supply for the mixer (rest of the chip uses 1.4V)
  - – Use of bond-wire inductor for the tuned LC LNA load

LNA

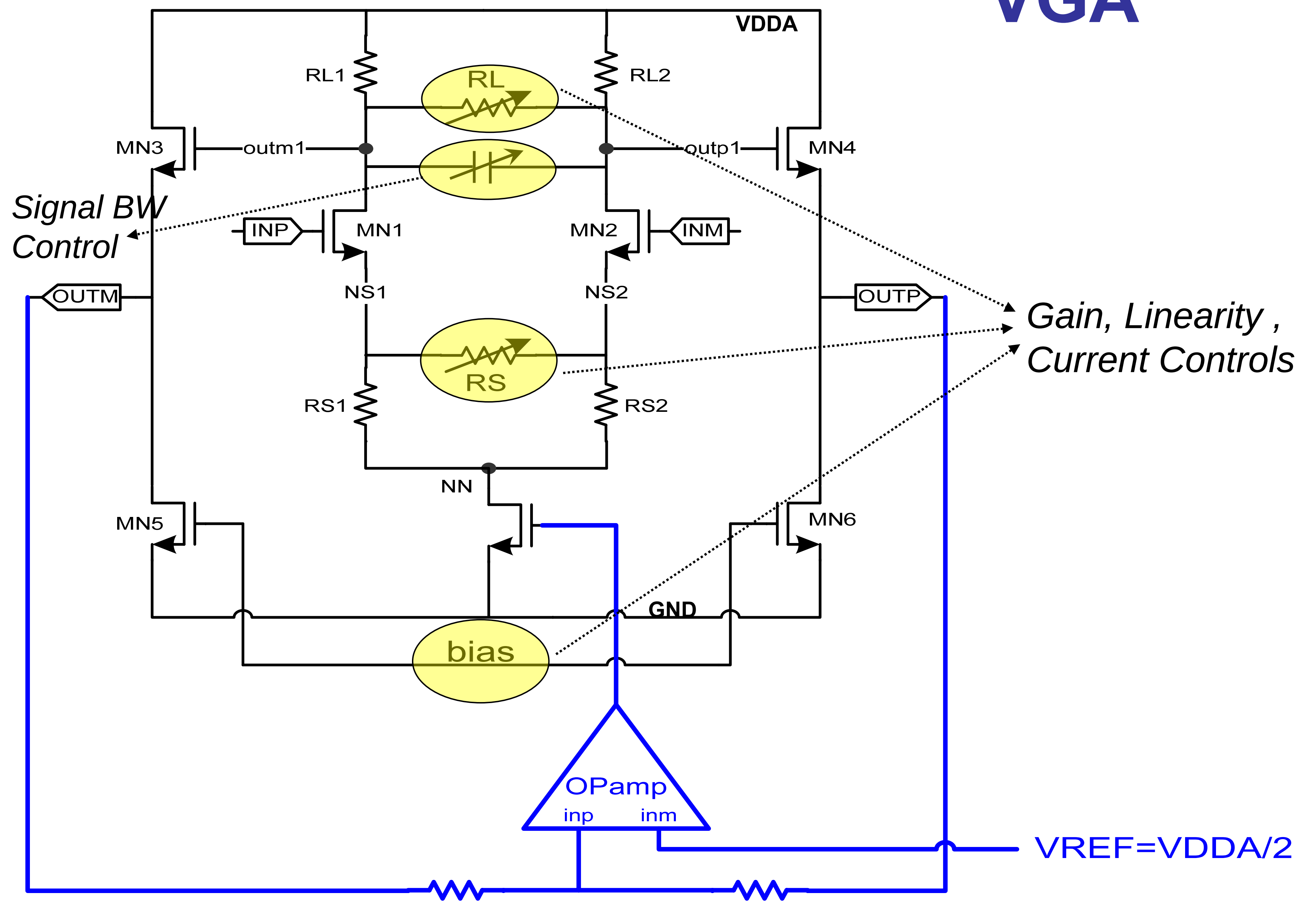


Vdd
LL1
LL2
R L
VOUT-
VOUT+
C L
Gain Control
Mcasc1
Mcasc2
Vbias_casc
C C
VRF
M1
M2
RB1
RB2
V bias
Current/Linearity/Gain Control

RF Amp and Mixer



VGA


VDDA
RL1
RL2
RL
MN3
outm1
outp1
MN4
Signal BW
Control
INP
MN1
MN2
INM
OUTM
NS1
NS2
OUTP
Gain, Linearity ,
Current Controls
RS
RS1
RS2
NN
MN5
MN6
GND
bias
OPamp
inp
inm
VREF=VDDA/2

WCDMA measured performance - Band III

Parameter	Measured performance
Voltage gain	37.3 dB
NF	2.90 dB
In band IIP3	-10.8 dBm
Out of band IIP3 (CW blockers at TX and TX+47.5MHz)	-7.3 dBm
Out of band IIP3 (CW blockers at TX and TX-95MHz)	-3.75 dBm
Out of band IIP2 (2 CW blockers at TX freq.)	47.0 dBm

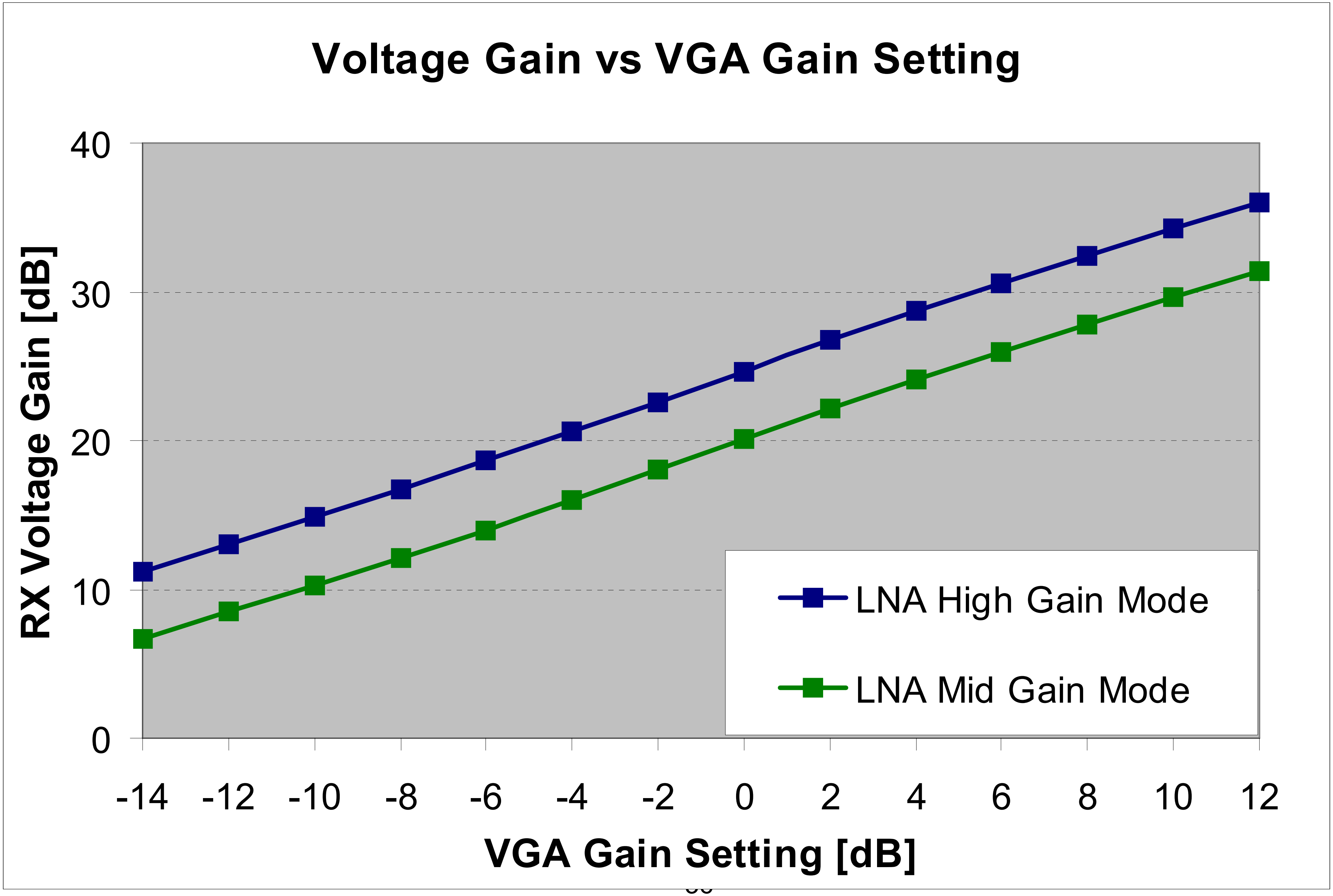
GGE measured performance – DCS band

Parameter	Measured performance
Voltage gain	37.3 dB
NF	2.90 dB
NF under blocking (3MHz blocker at -23dBm), includes reciprocal mixing	8.64dB
IIP3 (blockers at 800kHz and 1600kHz offset)	-10.8 dBm
IIP2 (self-mixing of blockers at 6MHz offset)	44.0 dBm

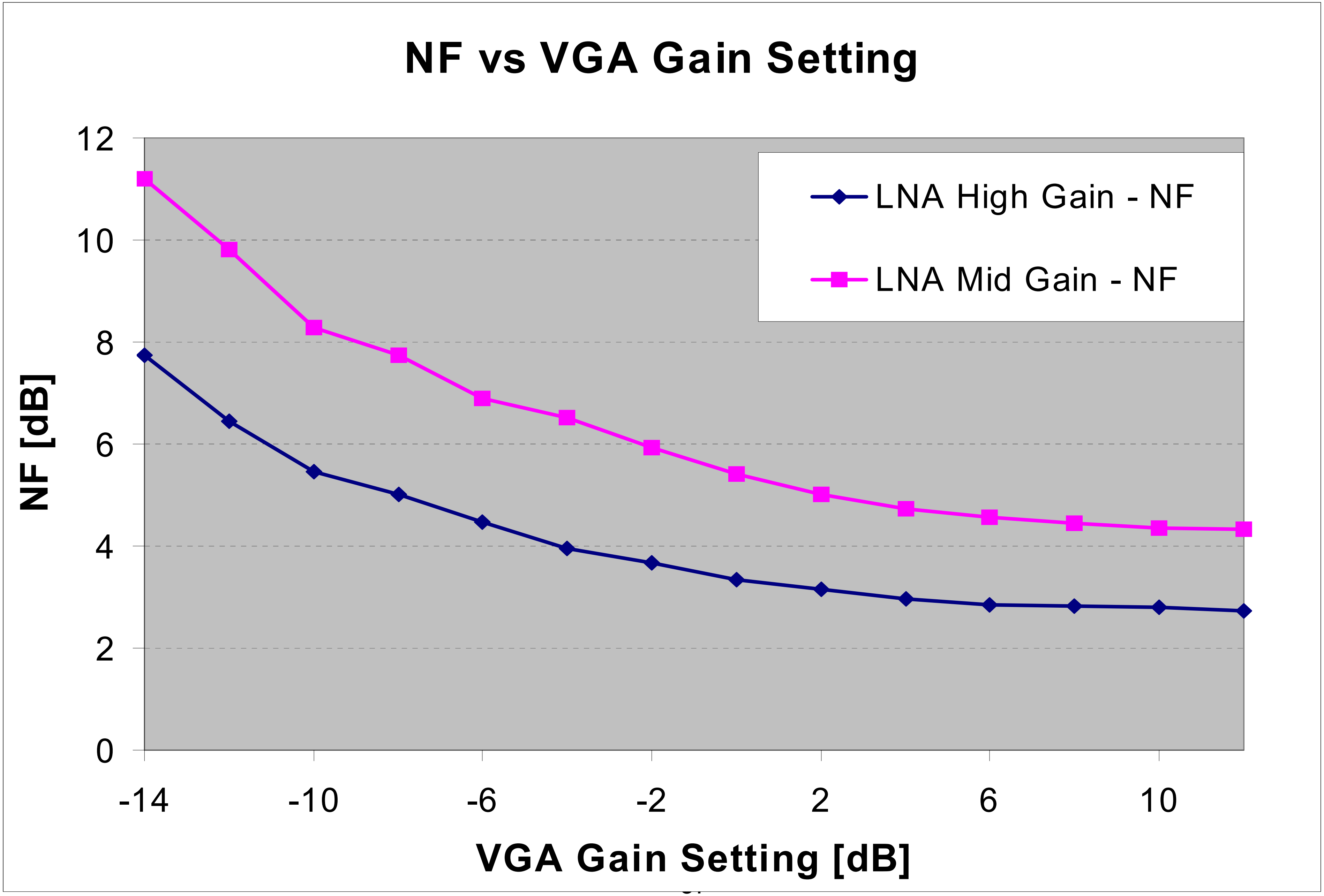
More Measured performance

Parameter	Measured performance
S11	-14 dB
Output DC offset (after correction)	50 uV
Gain imbalance (WCDMA)	0.4 dB
Gain Imbalance (GGE)	0.3 dB
Phase imbalance (WCDMA)	4^{o}
Phase Imbalance (GGE)	1^{o}
Out of Band IIP2 (WCDMA) (CW blockers at RX+TX and TX)	34.7 dBm

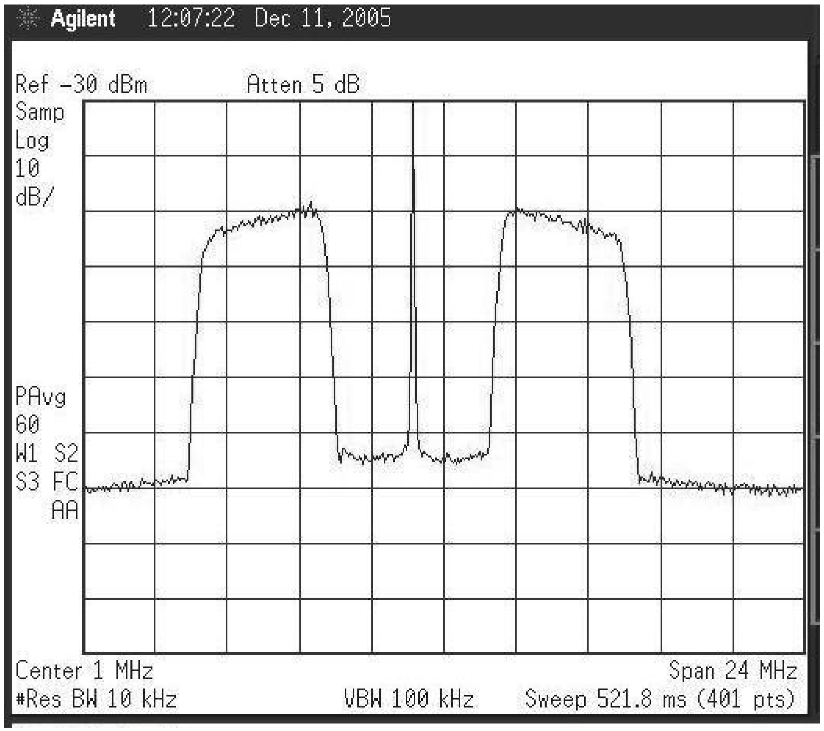
VGA voltage gain curve



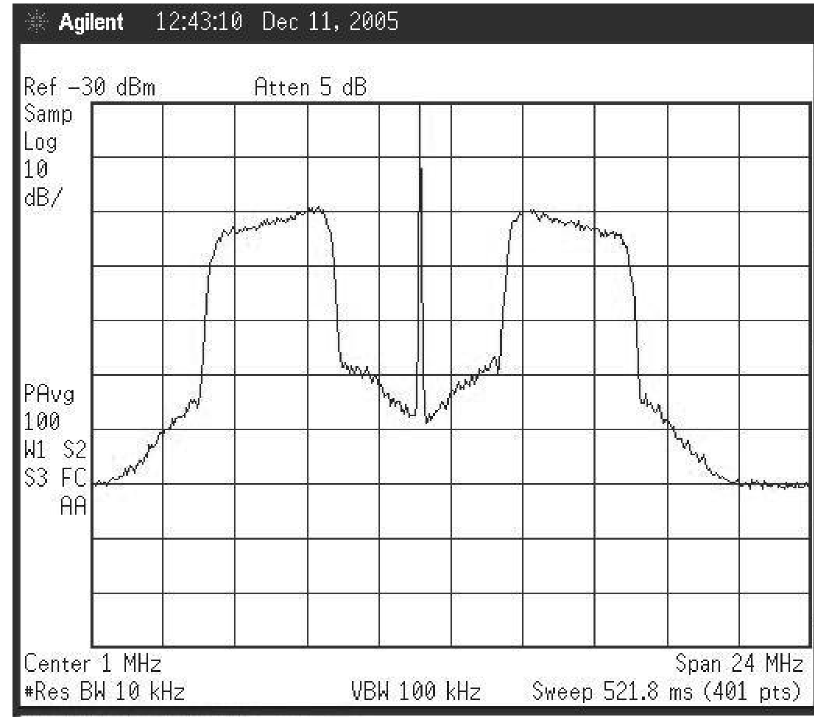
NF vs. VGA Gain Setting



Measured spectral re-growth based on number of channels in adjacent channel



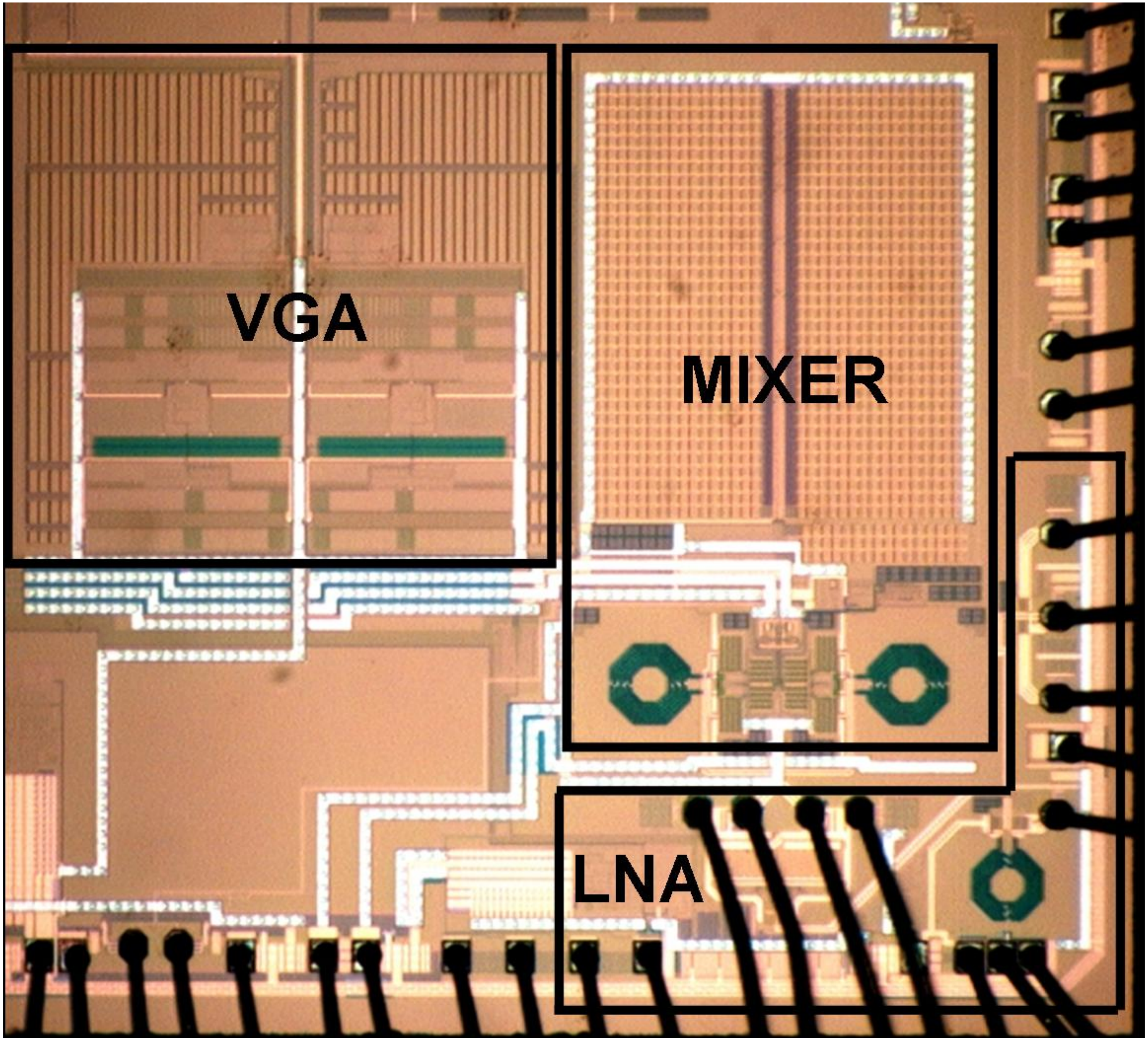
Re-growth of a 1 DPCH WCDMA ACI



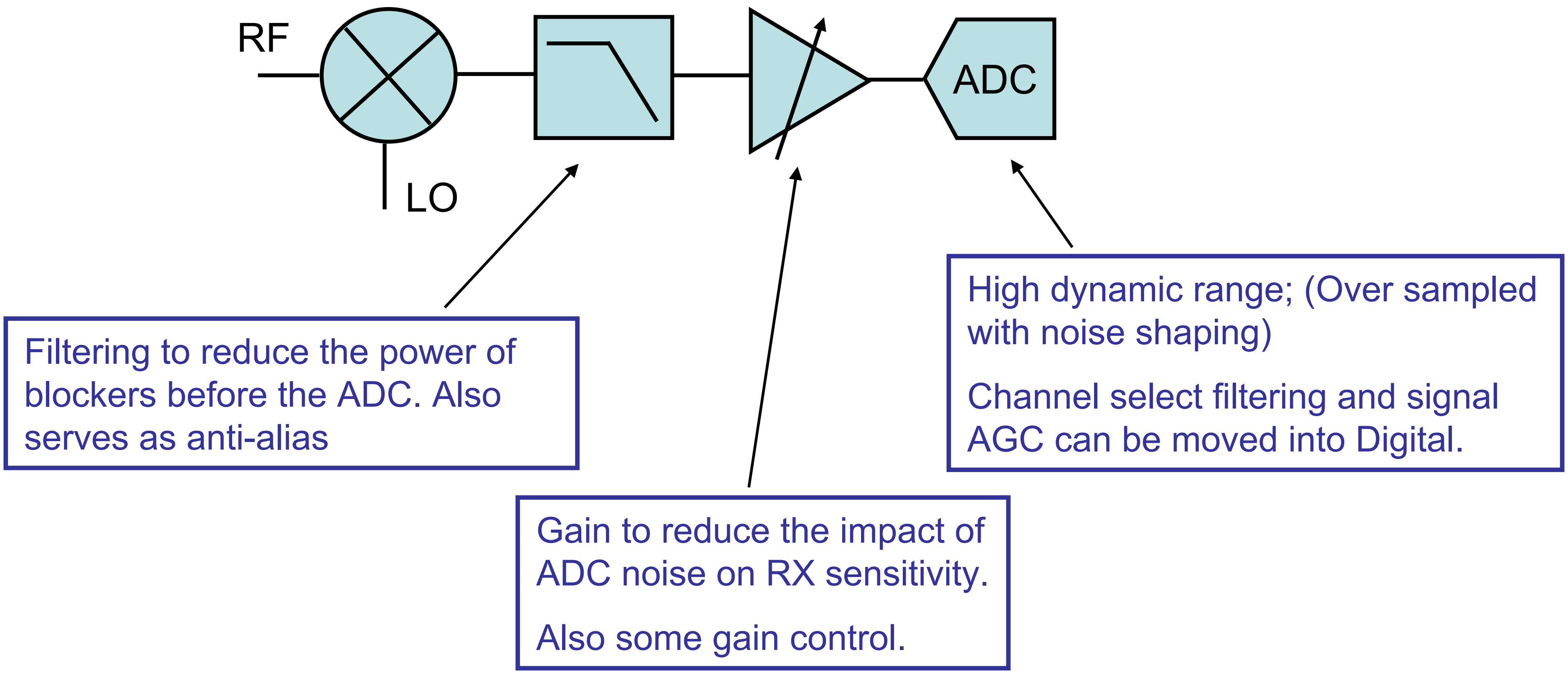
Re-growth of a 16 DPCH WCDMA ACI

- High PAR/increase in channels in adjacent channel will cause increased spectral re-growth.

Die Photo

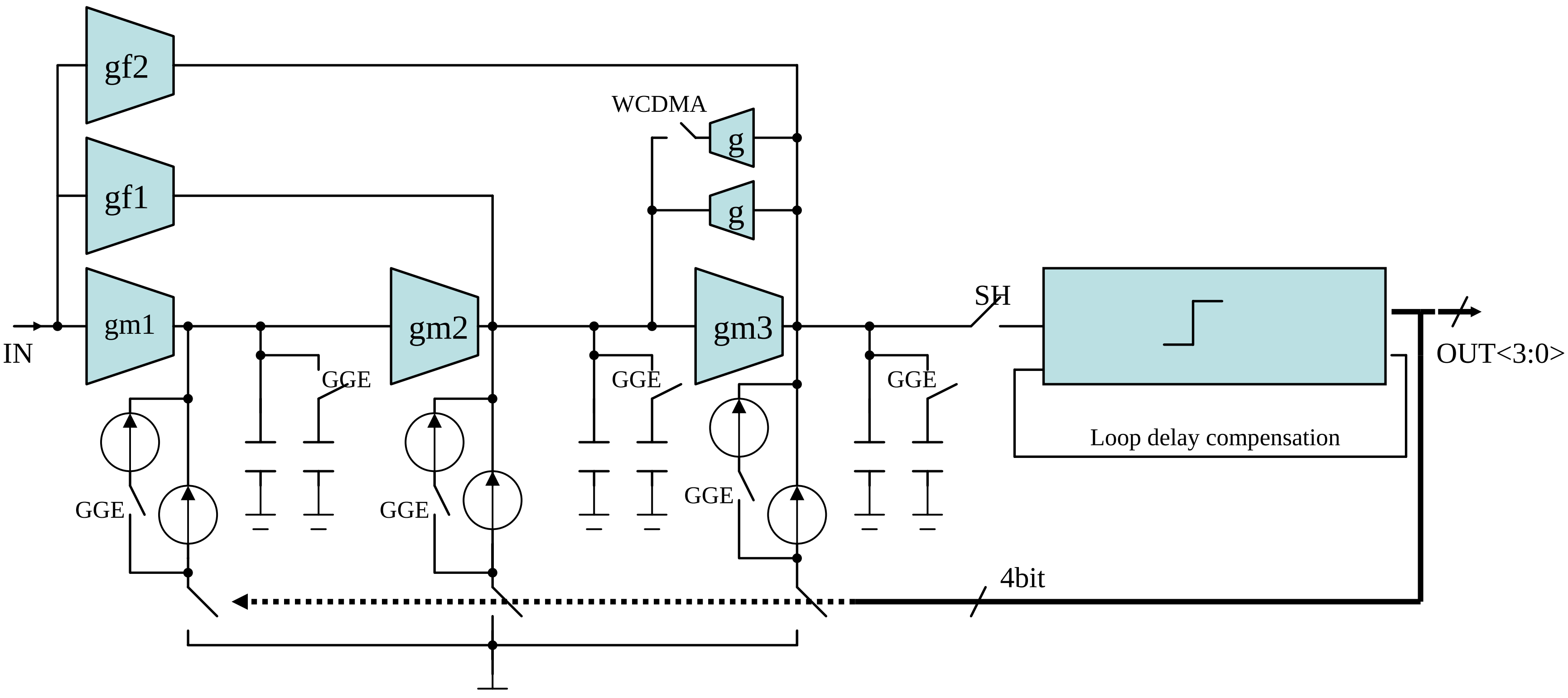


High Dynamic range ADCs



- High dynamic range in the ADC reduces the filtering and gain required in the analog (lower analog signal processing).

3rd Order continuous time ΣΔ ADC



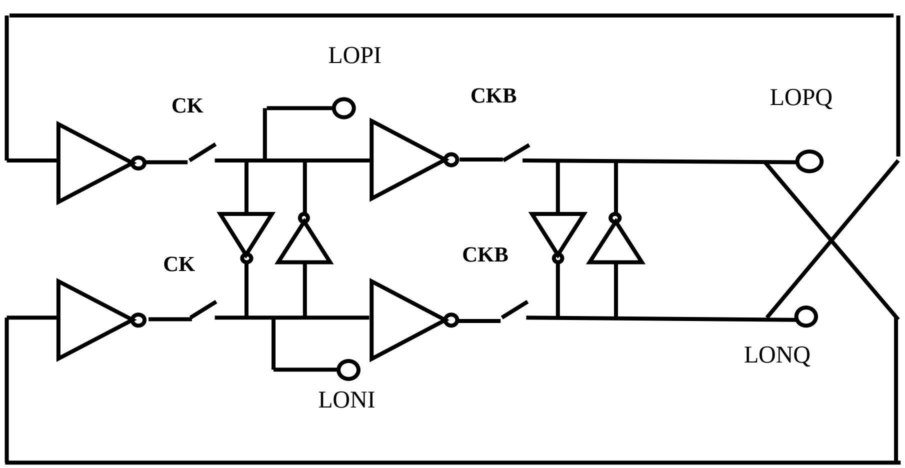
- Digital programmability for STF, NTF control.
- Gms, capacitors, clock rate, reference level, feedback currents are digitally programmable.

ADC simulated performance

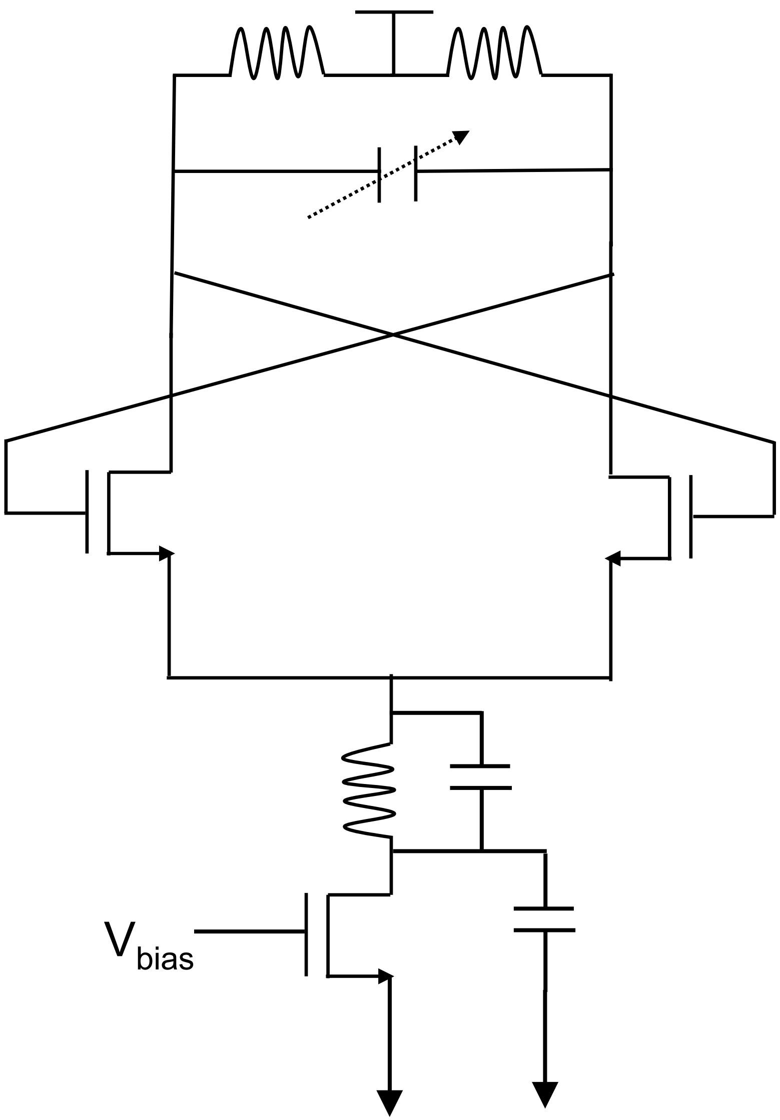
	Simulation results in WCDMA mode	Simulation results in GGE mode	Units
Signal Bandwidth	1.92	0.2	MHz
Sampling Frequency	120MHz	56MHz	MHz
Quantizer levels	9	9	MHz
Peak Signal	75	150	mVpk
Noise	5.83	8.0	nVrms/sqrt(Hz)
Dynamic Range	76.2	89.5	dB
IIP3	-0.5 (3.5MHz, 5.9MHz blockers)	2.1 (0.8MHz, 0.16MHz blockers)	dBVrms
Supply	1.4V	1.4V	V
Current consumption (I&Q)	8.0	9.0	mA

LO Generation

- Key Considerations
  - Tuning Range for desired band coverage (consider switchable inductor)
  - Phase noise requirement based on reciprocal mixing.
  - Dividers for quadrature generation and low-band coverage.



Quadrature Divider



VCO

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Conclusion

- The need for SDR style “multi-band, multi-mode” receivers is highlighted.
- Multi-band receiver: Various approaches and directions in trying to achieve this goal are presented.
- Multi-mode receiver: A multi-mode receiver in 90nm CMOS is presented illustrating the multi-mode concepts.
- Once a clear winner showing the performance and requirements for multi-band receiver emerges, we will have the much needed SDR receiver.

Acknowledgements

- Fikret Dulger
- Danielle Griffith
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- CC Chen
- Shanthi Bhagavatheeswaran

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