Analog Circuit Design with Submicron Transistors

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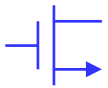
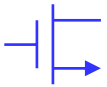


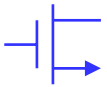
Analog Circuit Design

- Objective:
  Translate circuit specifications
  (gain, bandwidth, dynamic range, …)
  into transistor sizes and bias currents
- Challenge:
  Accurate device models for deep submicron transistors
  - "Square-law model"
  - Simulation models (BSIM, EVK, …)
  - "Model" for analog design



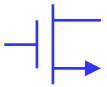
Device Model Objectives

- Device Physics
- Simulation / Verification
  - Accuracy, efficiency
- (Analog) Circuit Design
  - Relate device characteristics to circuit specifications
  - E.g.
    - Bandwidth
    - Gain
    - Power dissipation
    - Dynamic range (noise)
  - Accurate, simple



Device Parameters for Analog Design

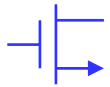
- Large signal
  - Current I_D → power dissipation
  - Minimum V_{DS} → available signal swing
- Small signal
  - Transconductance g_m → speed / voltage gain
  - Capacitances C_{GS}, C_{GD}, … → speed
  - Output impedance r_o → voltage gain



Metrics for Design

- Transistor Objectives: High transconductance
  - Without large I_D
  - Without large C_{GS}

- Figures of Merit
  - Current efficiency $\frac{g_m}{I_D}$
  - Transit frequency $\frac{g_m}{C_{gs}}$



Current Efficiency

- "Square-law transistor":

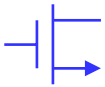
$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

$$g_m = \frac{2I_D}{V_{GS} - V_{TH}}$$

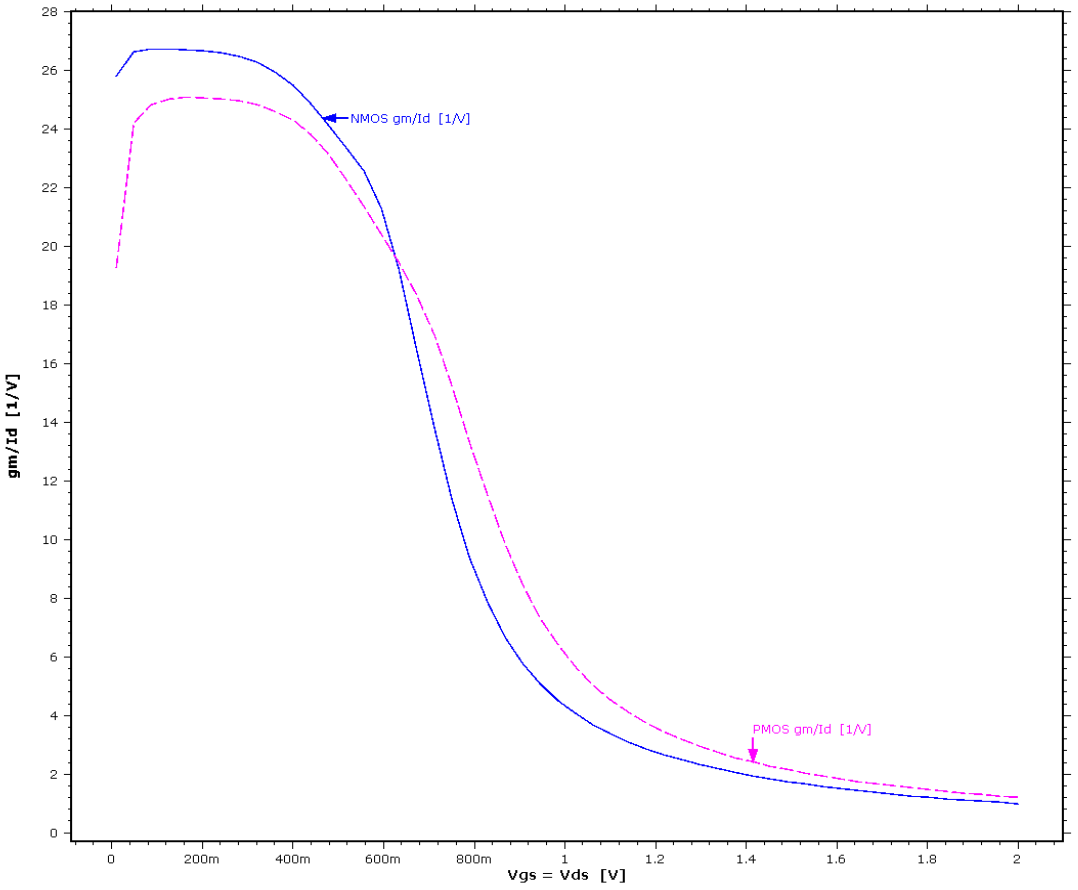
$$= \frac{2I_D}{V_d^{sat}}$$

← Overdrive voltage

- High efficiency → low overdrive voltage



Current Efficiency g_m/I_D



- High efficiency is good for low power
- Higher g_m/I_D at low V_{GS}
- Approaches BJT for $V_{GS} < V_{TH}$

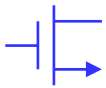
  $g_m/I_C = 1/V_t \sim 40\ V^{-1}$
- Weak dependence on transistor type and process

Transit Frequency ω_T

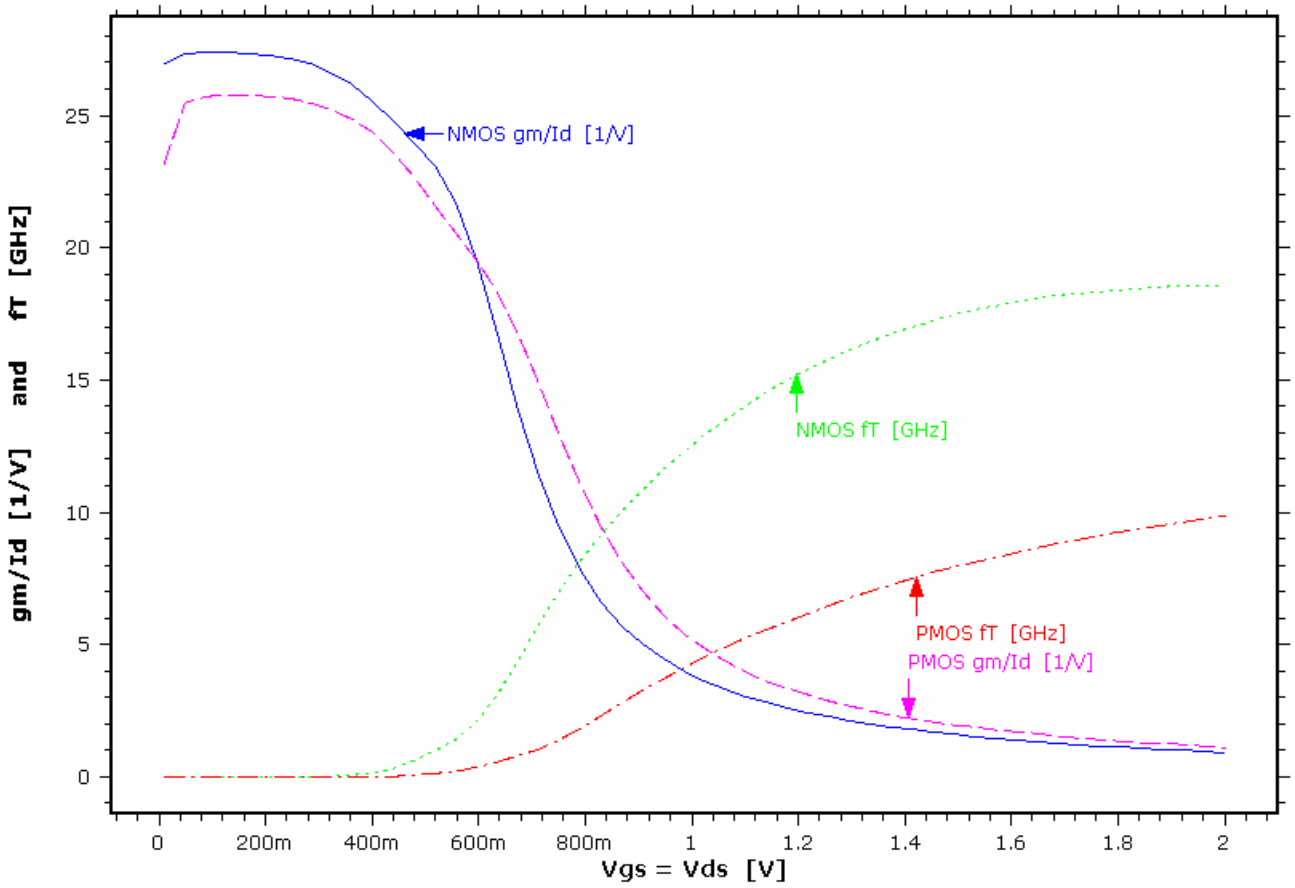
- Unity current-gain bandwidth

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}$$

$$\approx \frac{\mu V_d^{sat}}{L^2} \qquad \text{(square-law model)}$$



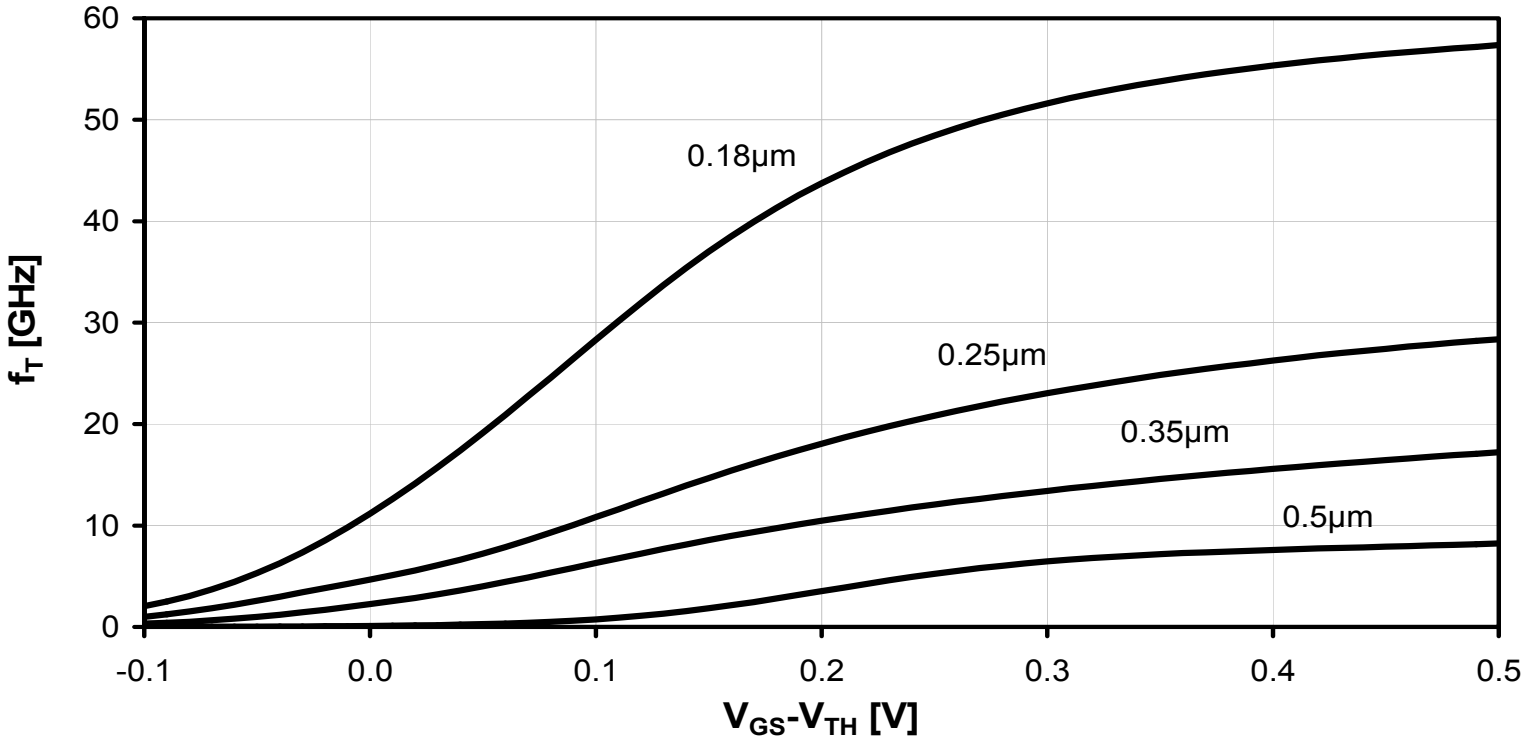
Efficiency g_m/I_D versus f_T



Speed-Efficiency Tradeoff

NMOS faster than PMOS

Device Scaling



Short channel devices are significantly faster!

Current Efficiency vs Transient frequency

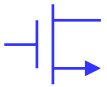
- Tradeoff:

$$\frac{g_m}{I_D} \propto \frac{1}{V_d^{sat}}$$

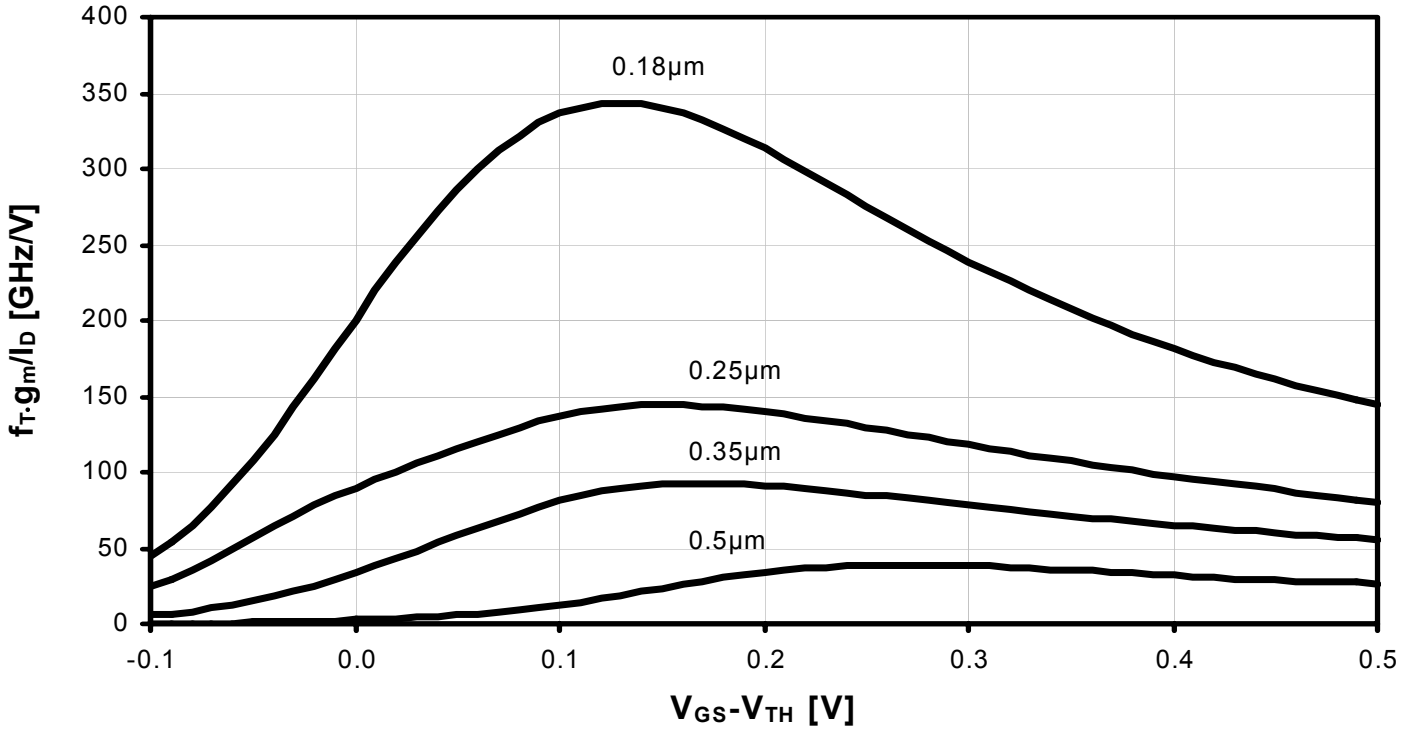
$$\omega_T \propto V_d^{sat}$$

- What about:

$$\frac{g_m}{I_D} \times \omega_T \propto \frac{\mu}{L^2}$$



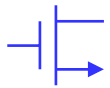
Device Figure-of-Merit



Peak performance for low $V_{GS}-V_{TH}$

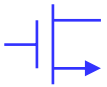
Device Scaling for Analog Circuits

- "Moore's Law"
  - L_{min} decreases ~ 2x every 5 years
  - L_{min} = 10μm in 1970, 90nm in 2004
- Benefits (for analog circuits):
  - Higher speed: increase g_m/C_{gs} while keeping g_m/I_D constant
  - Lower power: increase g_m/I_D while keeping bandwidth (g_m/C_{gs}) constant
- In both cases, reducing L is advantageous!



Short Channel Devices

- Short channel effects
  - Velocity saturation
  - Mobility degradation (thin oxide)
- Prior considerations assume “square law” models and ignore these effects
  → Significant discrepancies
- Let’s fix this …



Efficiency g_m/I_D

- Important design parameter … but a little unusual: units 1/V
- Let's define

$$V^* = \frac{2I_D}{g_m} \quad \Leftrightarrow \quad \frac{g_m}{I_D} = \frac{2}{V^*}$$

e.g. V* = 200mV → g_m/I_D = 10 V^{-1}

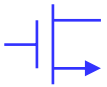
- Square-law devices *only*: V* = V_{GS}-V_{TH} = V_{dsat}

$$\text{Square law :} \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}} = \frac{2I_D}{V^*}$$

Saturation Voltage versus V*

- Saturation voltage
  - Minimum V_{DS} for "high" output resistance
  - Poorly defined: transition is smooth in practical devices

- "Long channel" (square law) devices:
  - $V_{GS} - V_{TH} = V_{dsat} = V_{ov} = V^*$
  - Significance:
    - Channel pinch-off
    - $I_D \sim V_{dsat}^2$
    - Boundary between triode and saturation



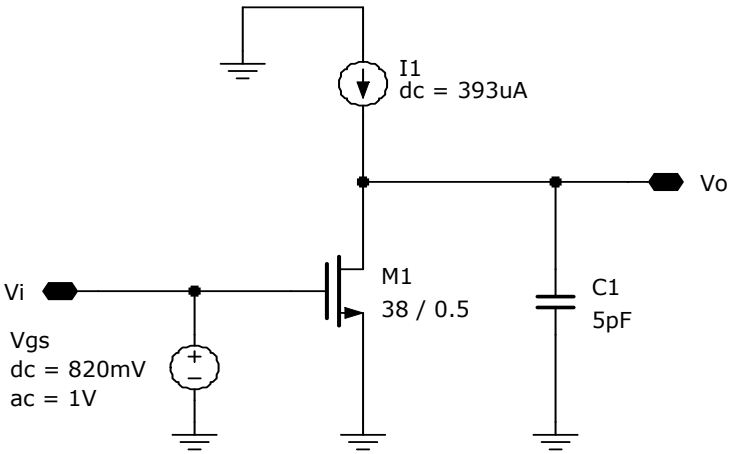
Design Example

Example: Common-source amp

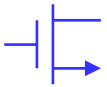
$a_{v0} > 100$, $f_u = 100\text{MHz}$ for $C_L = 5\text{pF}$

DC Analysis DC1
Device Vgs
sweep from 800m to 900m (1001 steps)

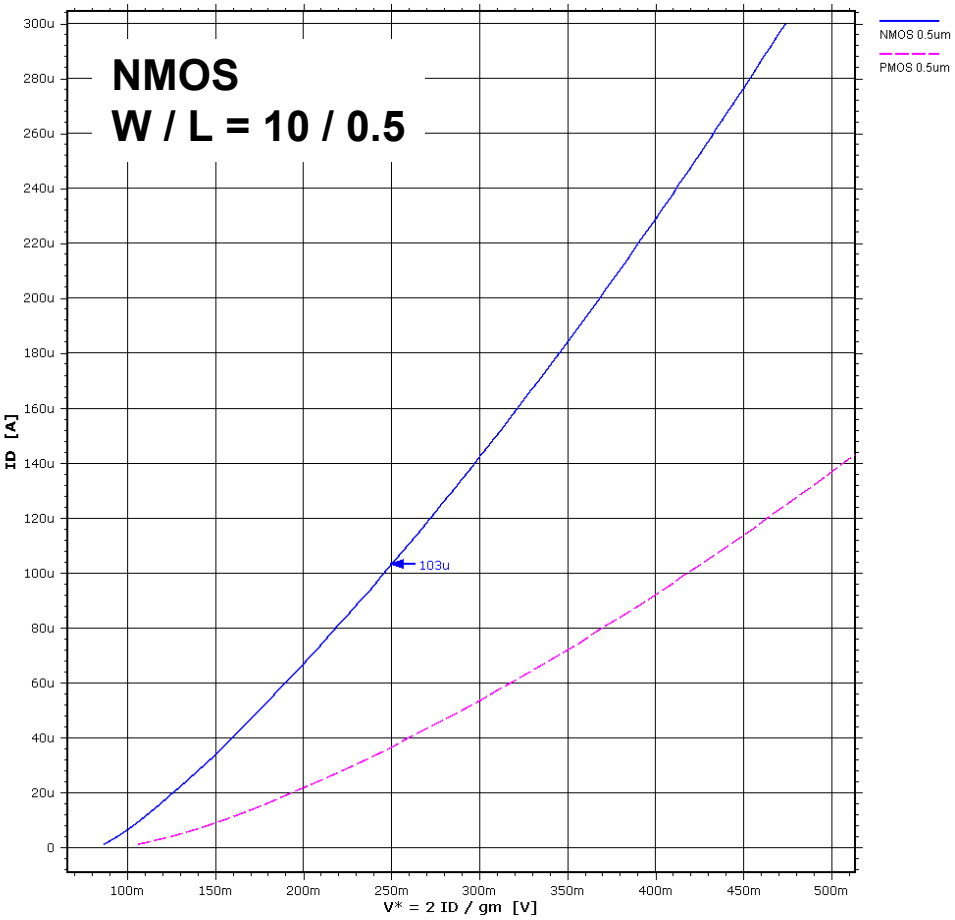
AC Analysis AC1
log sweep from 1k to 10G (101 steps)



- $a_{v0} > 100 \rightarrow L = 0.5\mu\text{m}$
- $g_m \approx 2\pi f_u C_L = 3.14\text{mS}$
- High f_T (small C_{GS}): $V^* = 250\text{mV}$
- $I_D = \frac{g_m V^*}{2} = 393\mu\text{A}$



Device Sizing

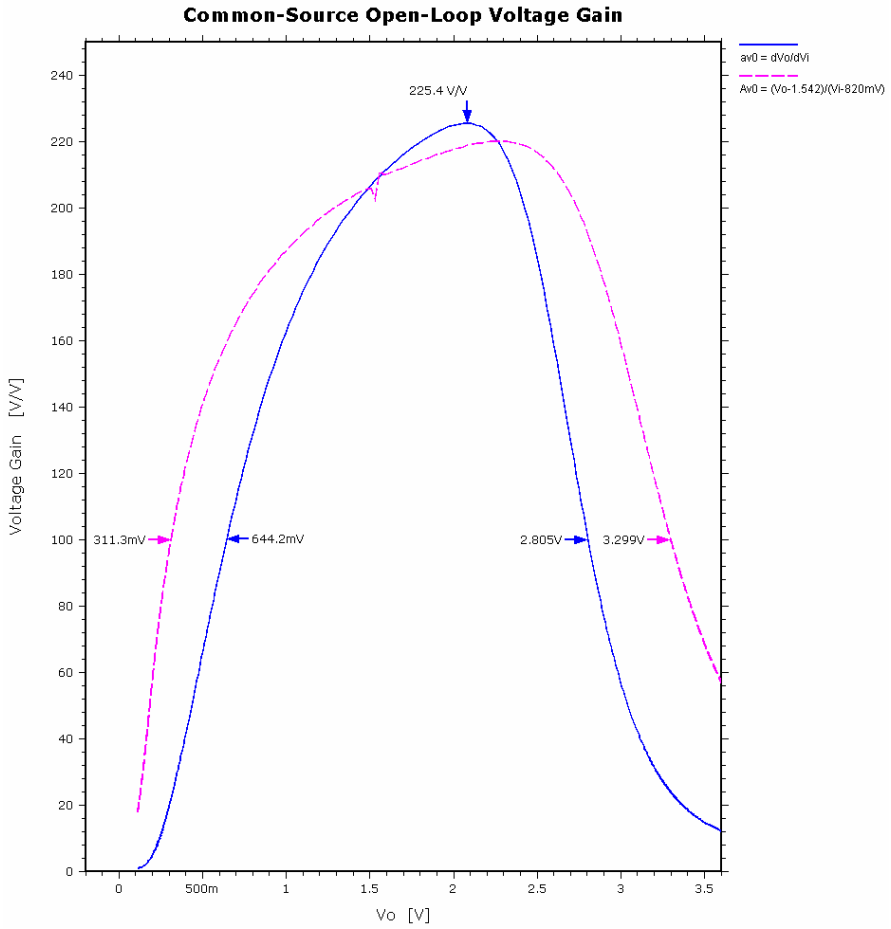


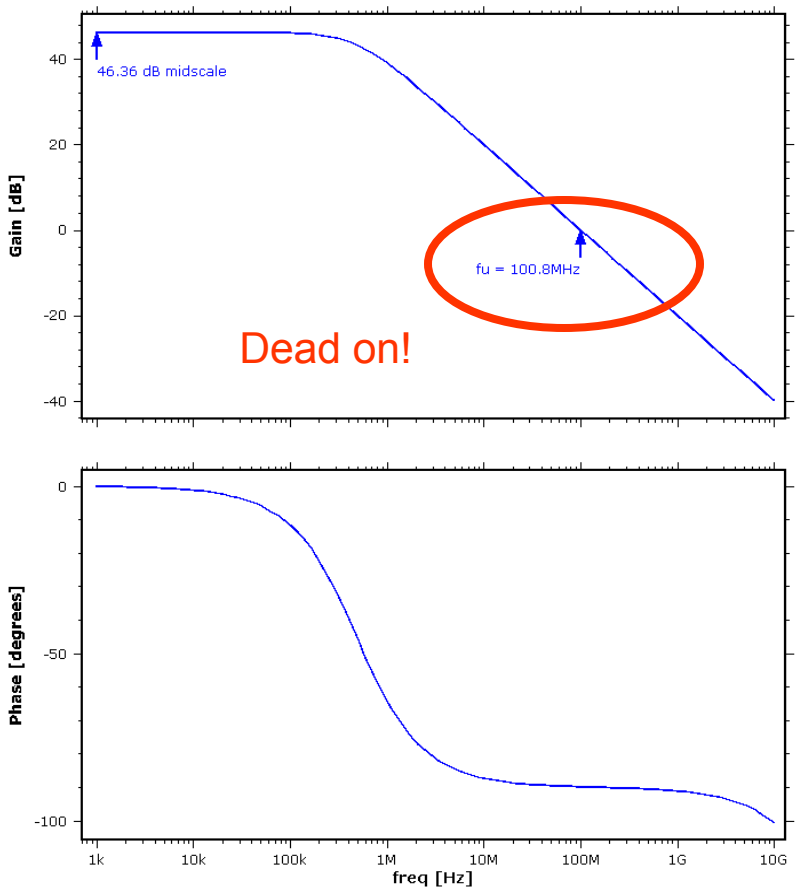
- Pick L 0.5μm
- Pick V* 250mV
- Determine g_m 3.14mS
- $I_D = 0.5\ g_m\ V^*$ 393μA
- W from graph (generate with SPICE)

  → W = 10μm (393μA /103μA)
  = 38μm

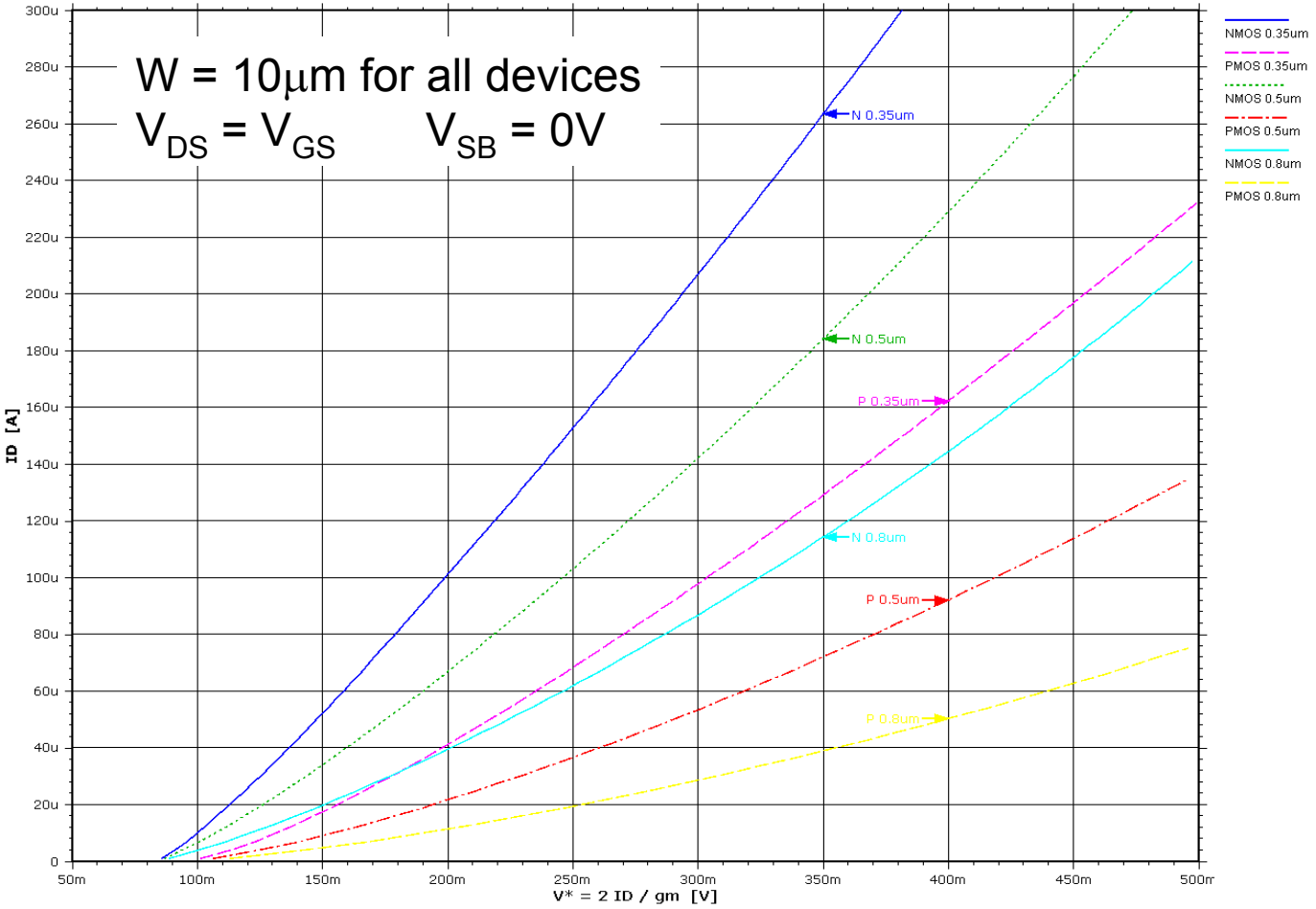
- ***Create such graphs for several device length' for design reference***

Common Source Example





Device Sizing Chart



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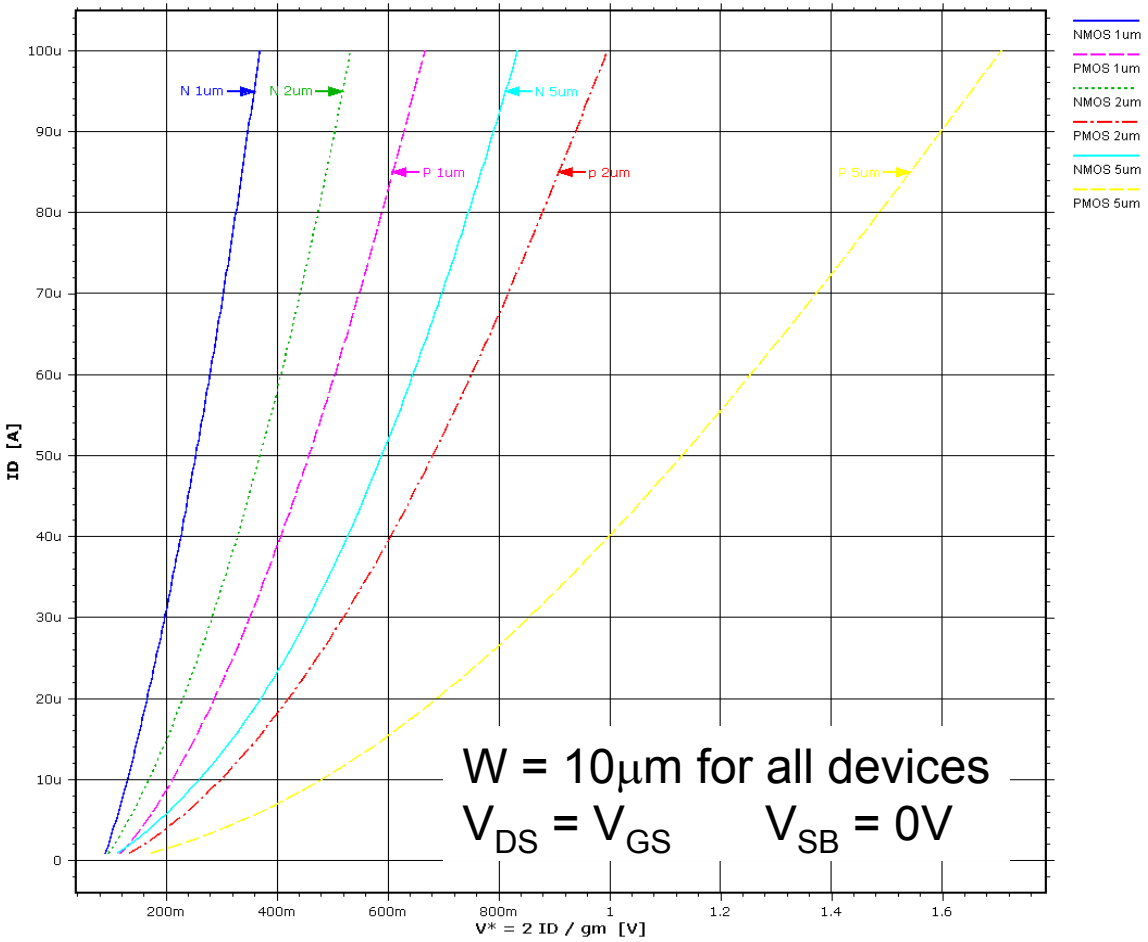

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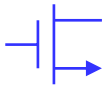
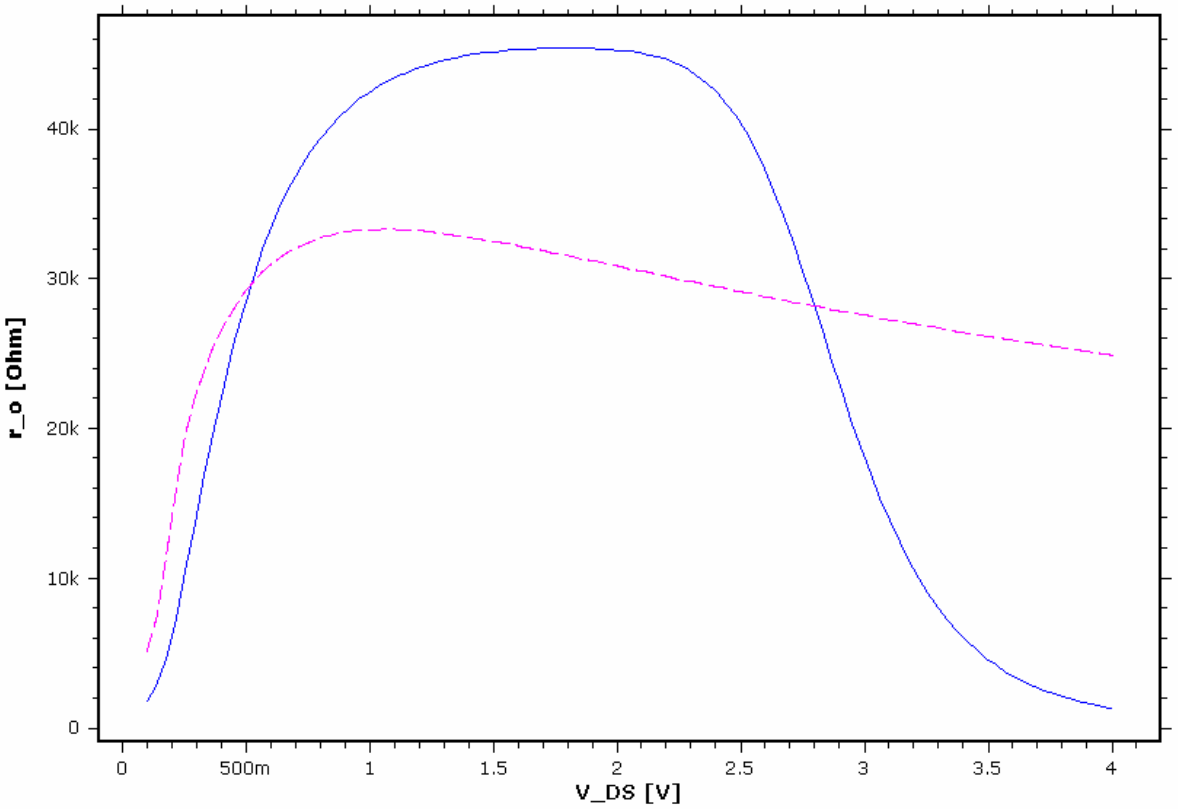
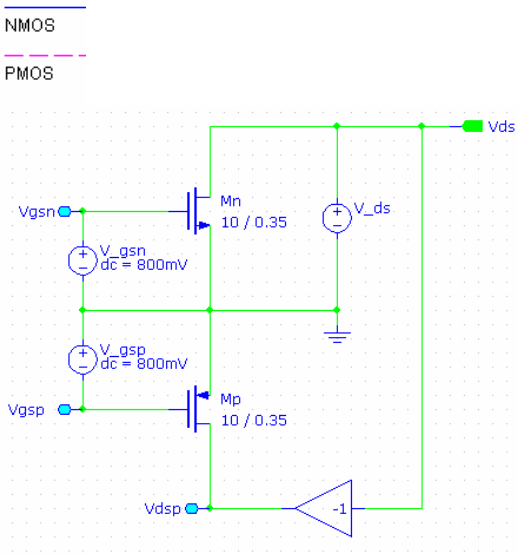
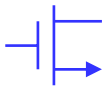


Output Resistance r_o

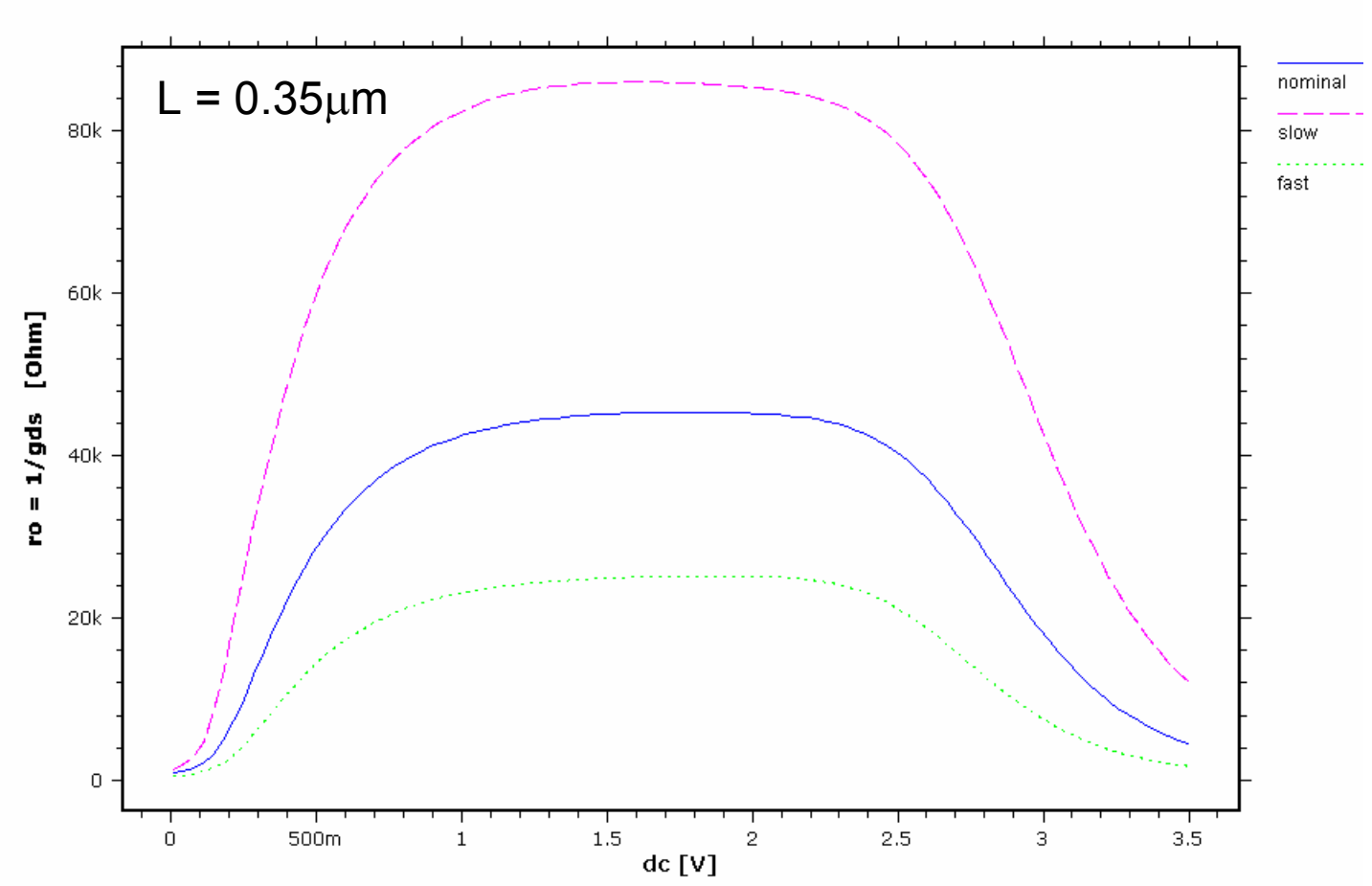




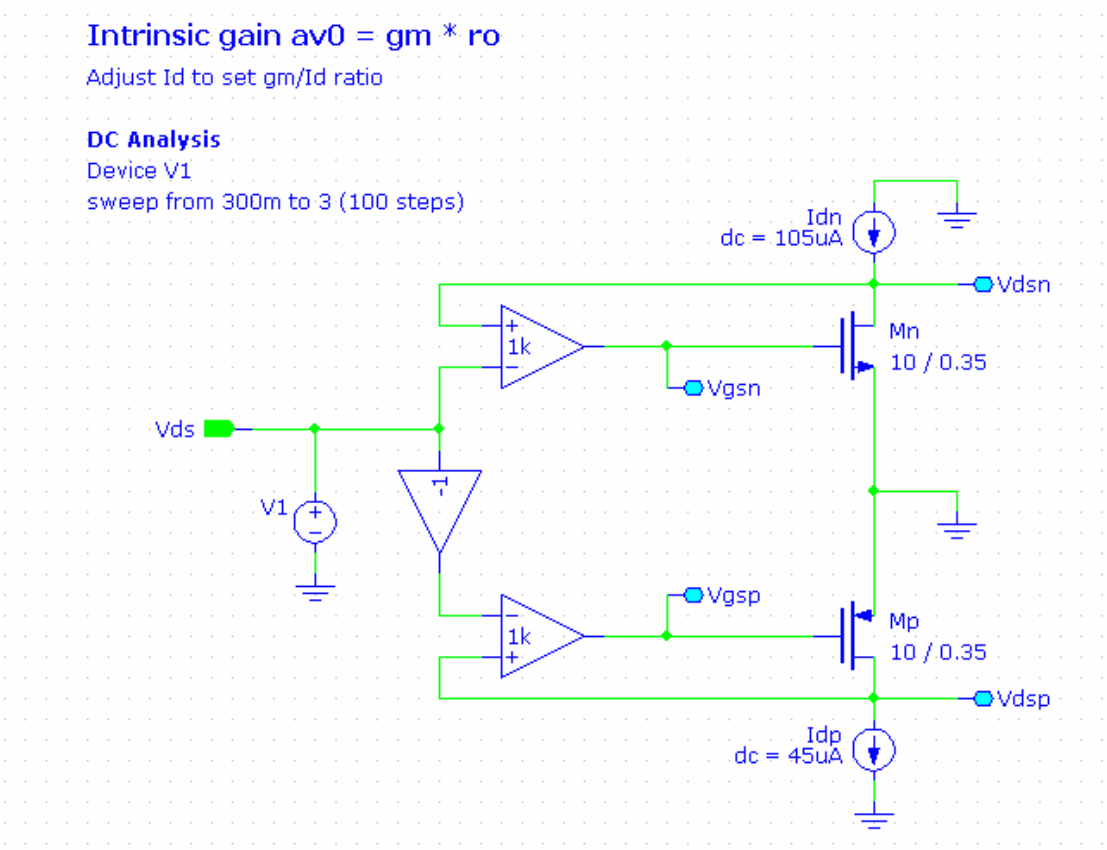
Hopeless to model this with a simple equation (e.g. $g_{ds} = \lambda I_D$)



Process Variations for r_o

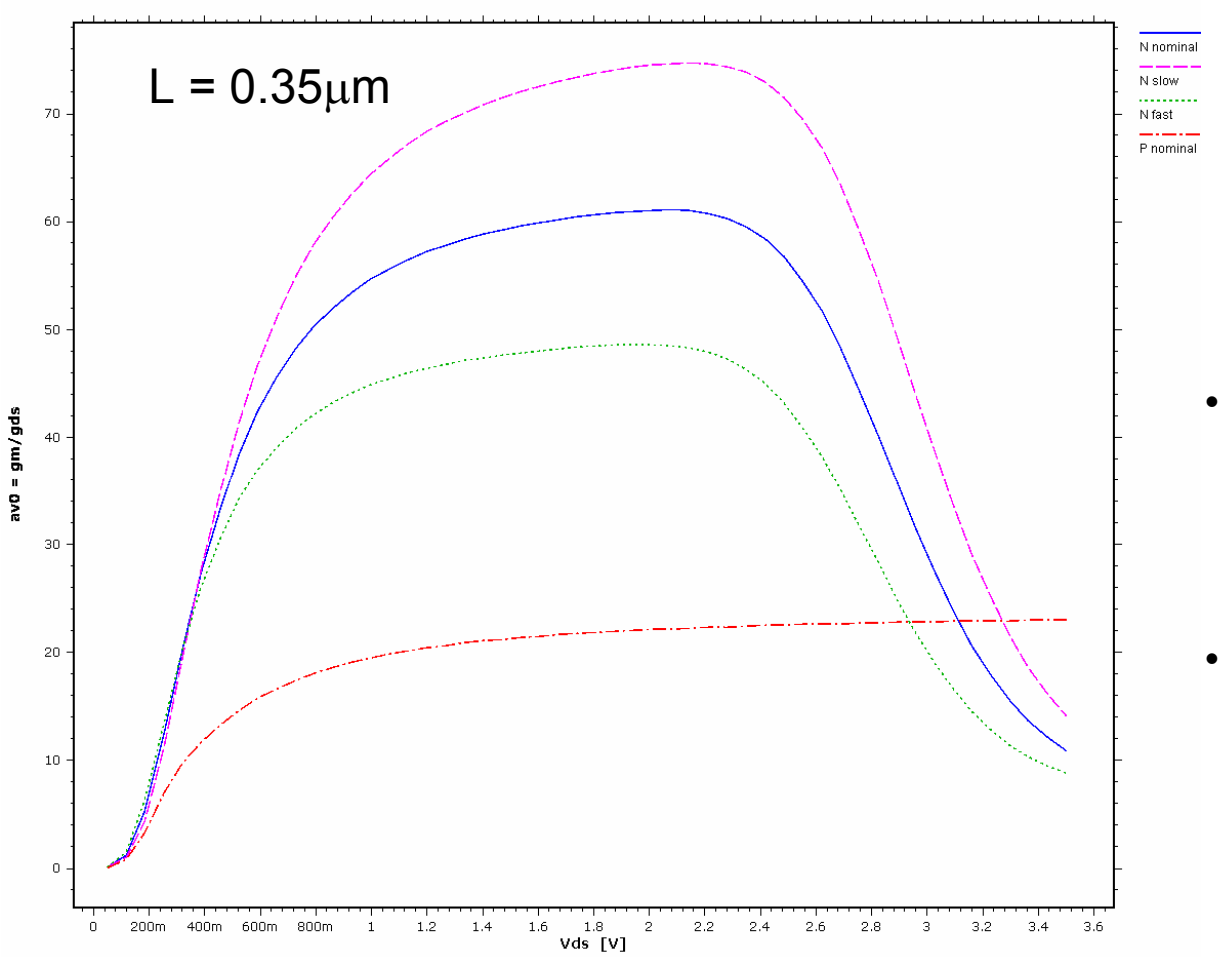


Open-loop Gain a_{v0}



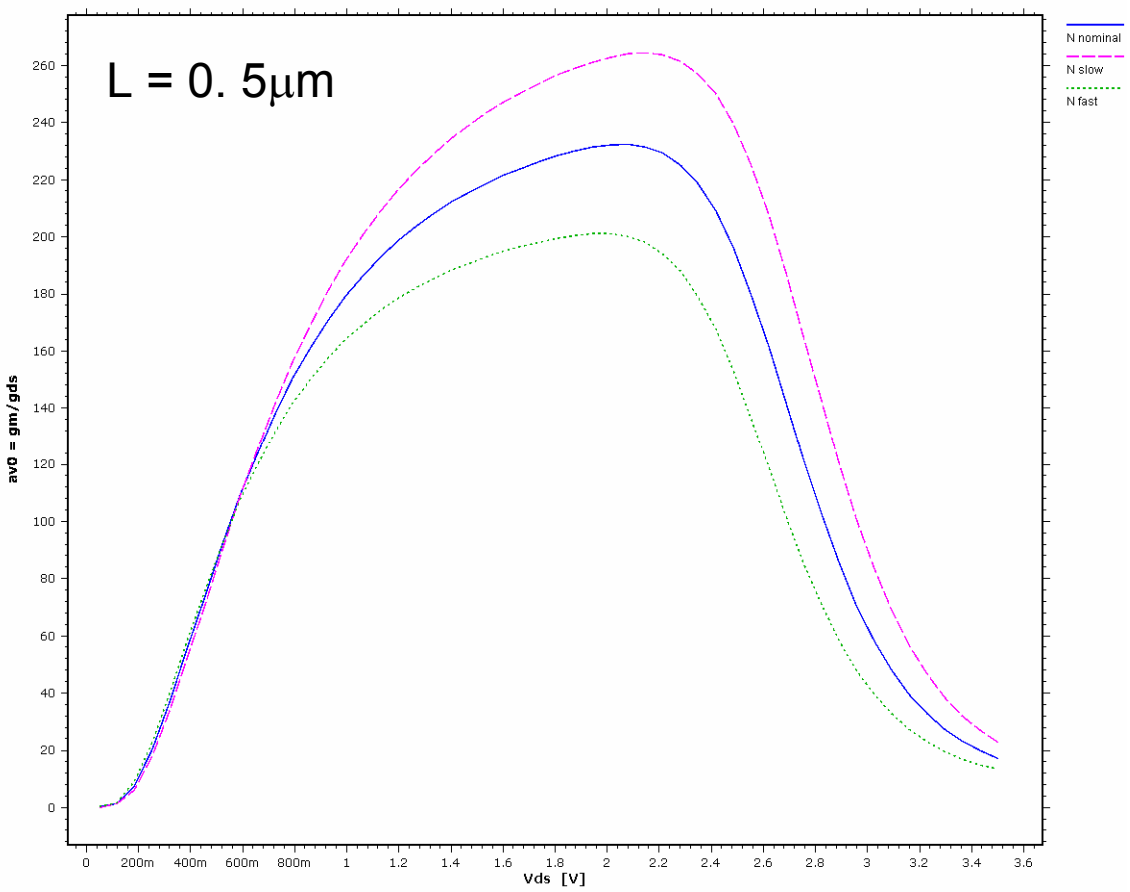
More useful than r_o

Gain, $a_{v0} = g_m r_o (g_m/I_D = 10/V)$



- Strong tradeoff: a_{v0} versus V_{DS} range
- ***Create such plots for several device length' for design reference***

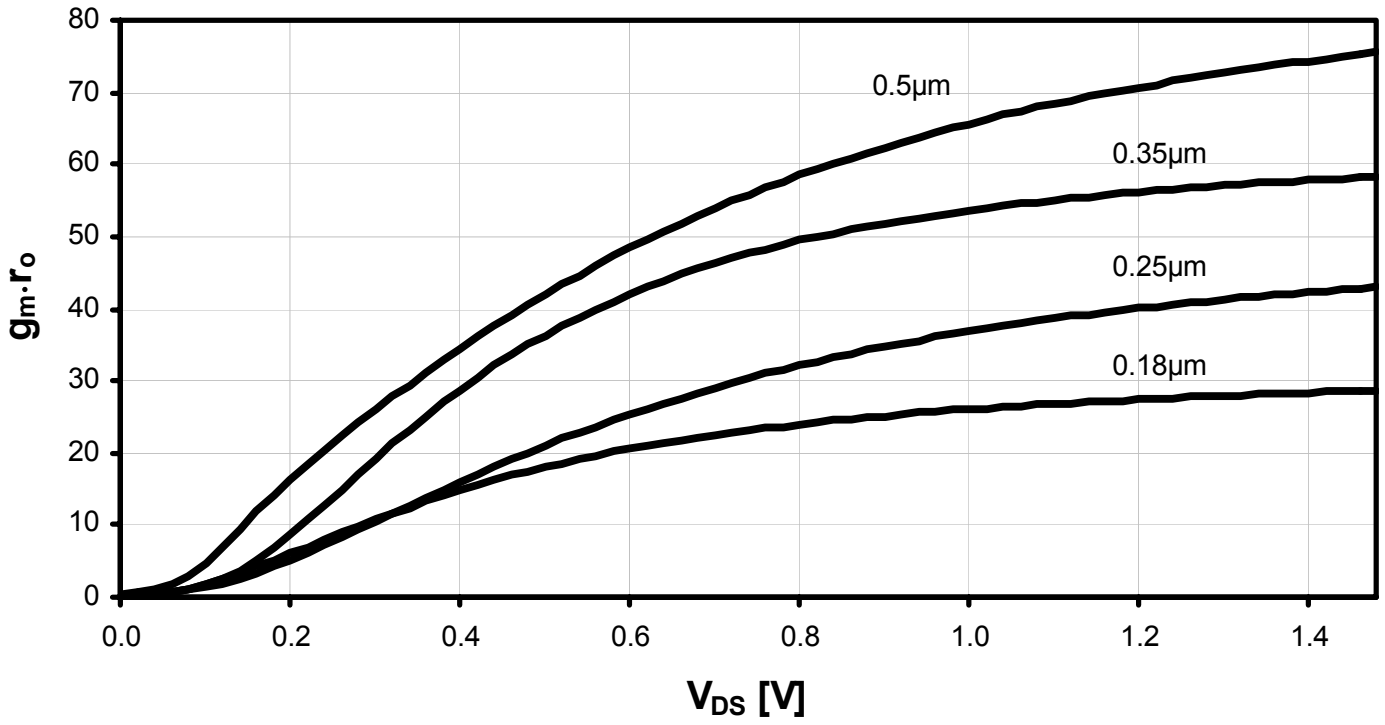
Gain, $a_{v0} = g_m r_o (g_m/I_D = 10/V)$



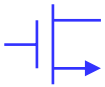
$L \uparrow \rightarrow a_{v0} \uparrow$

like long channel device

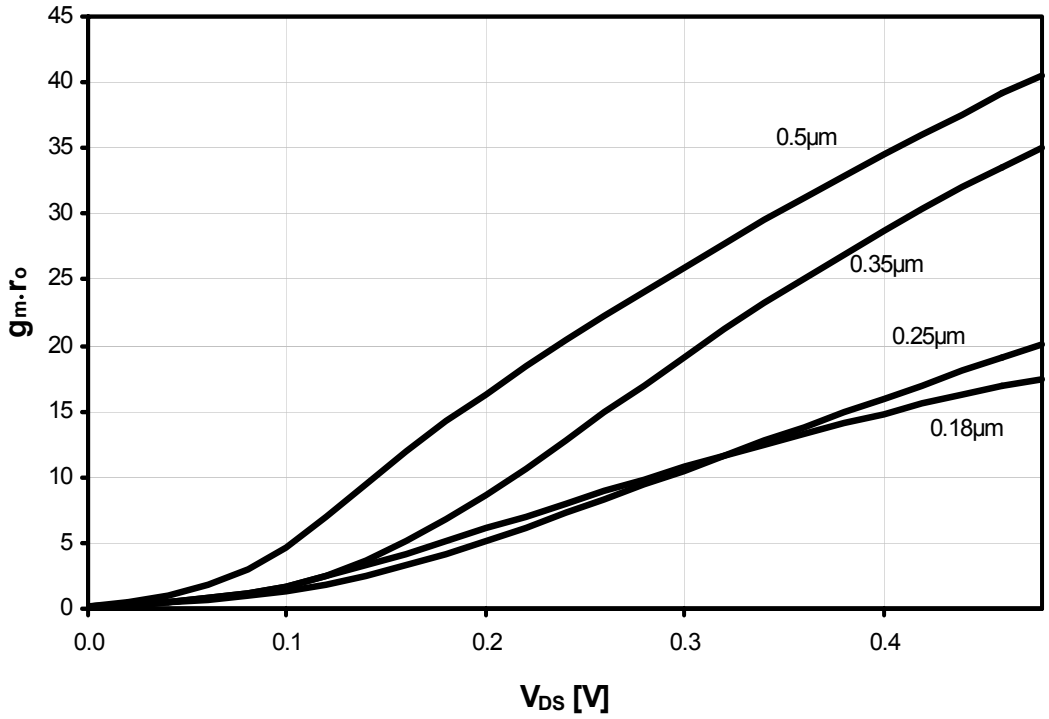
Technology Trend



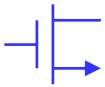
Short channel devices suffer from reduced per transistor gain



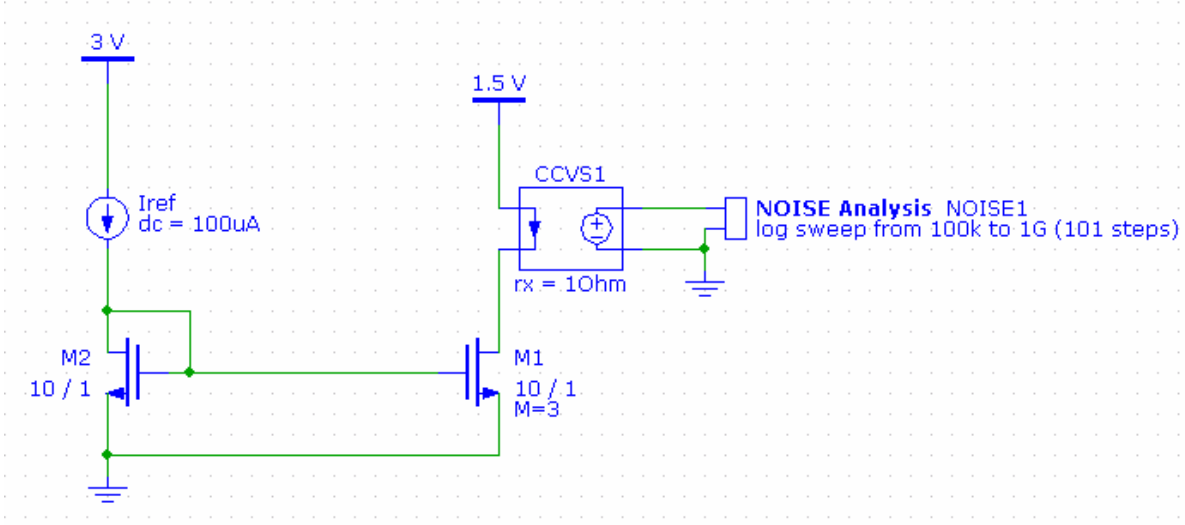
Transistor Gain Detail



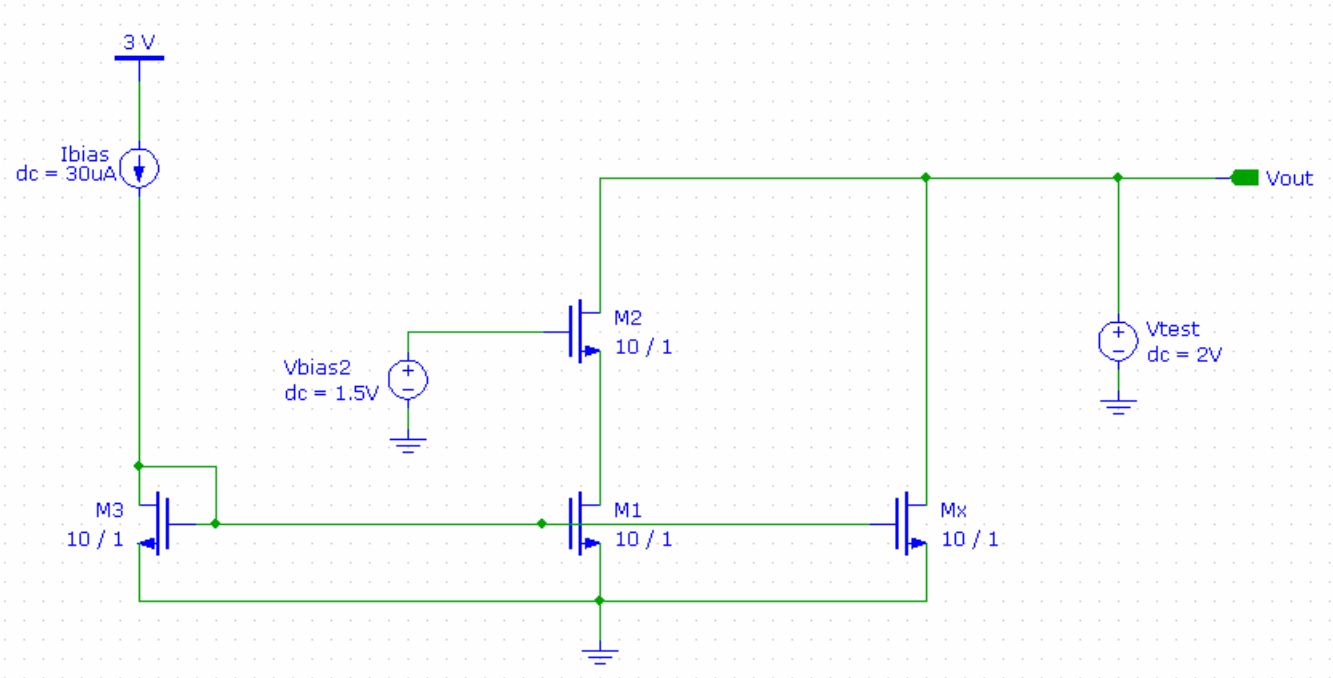
For practical V_{DS} the effect the “short-channel” gain penalty is less severe (remember: worst case V_{DS} is what matters!)



Current Sources (Biasing)

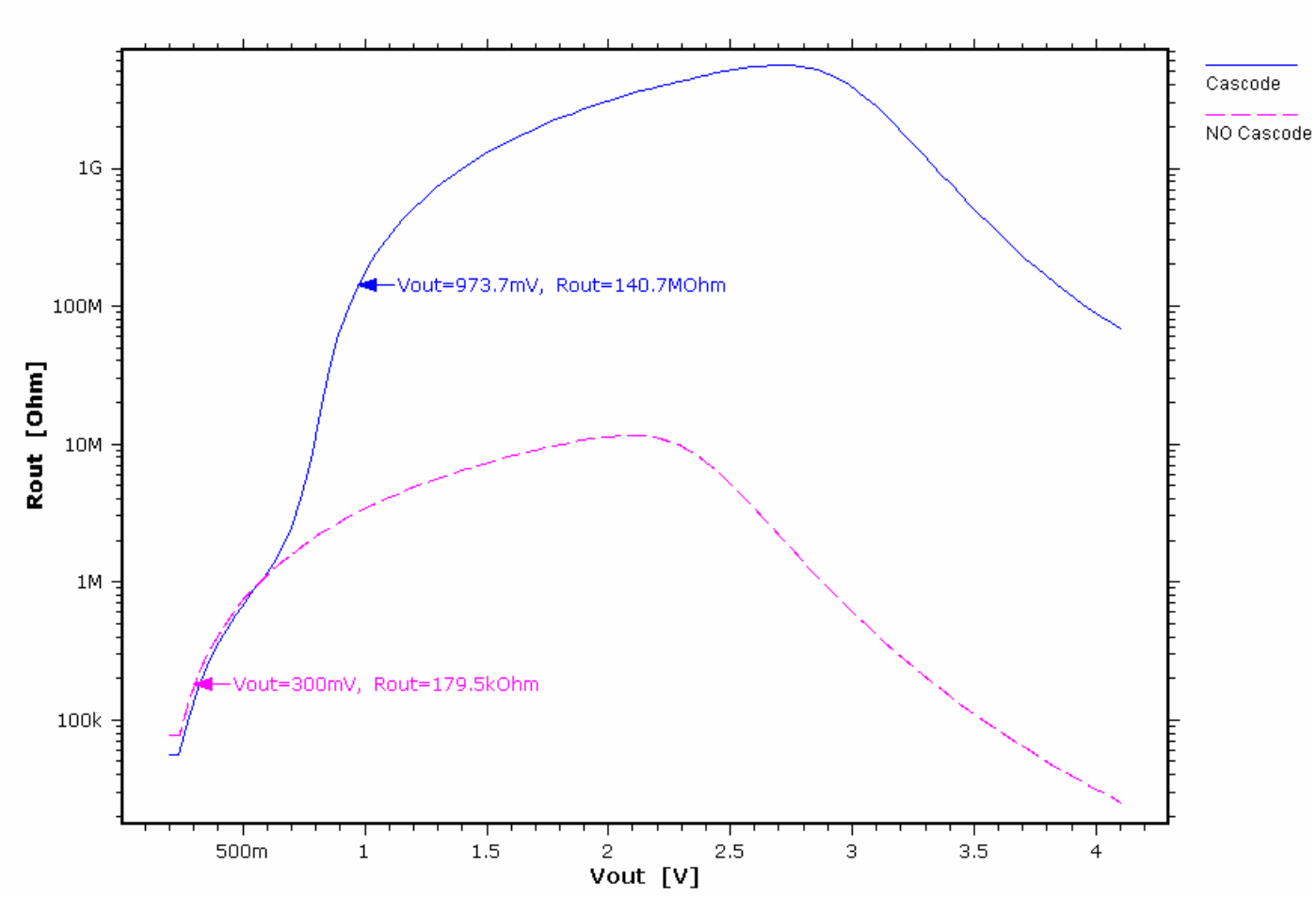


Cascoding

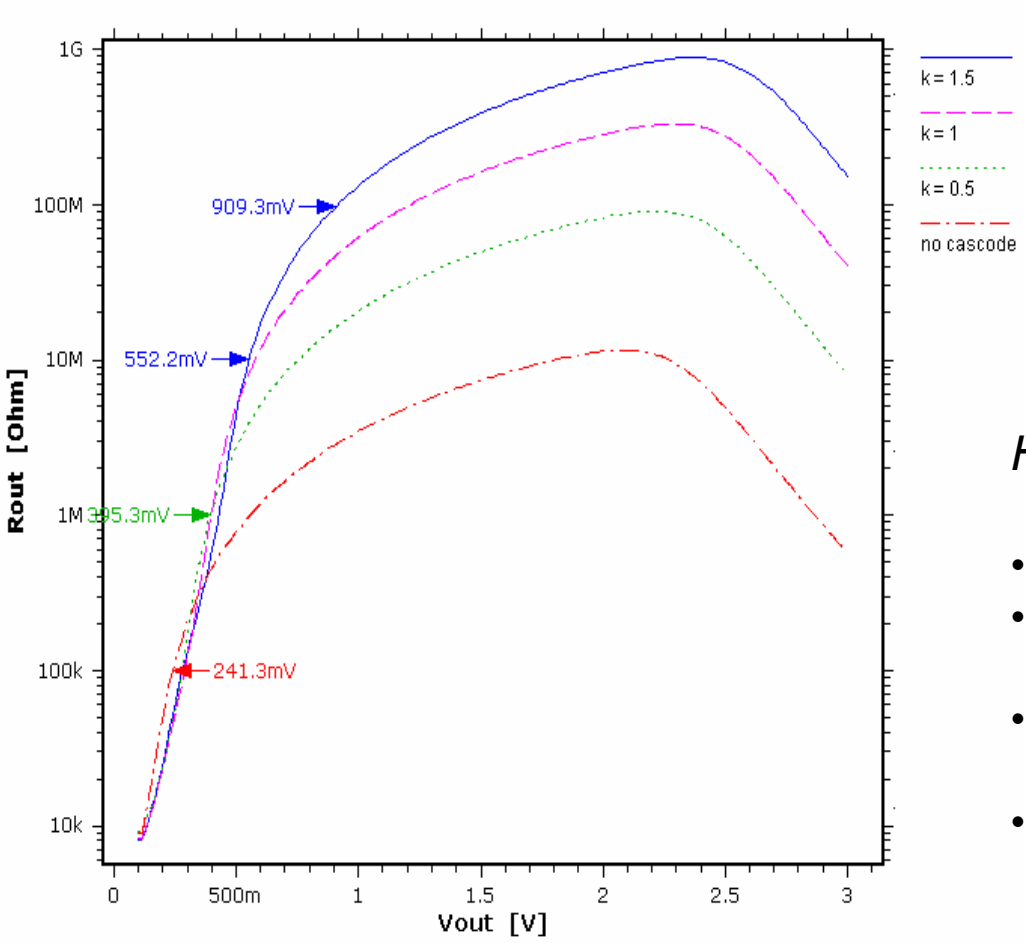


How choose V_{bias2}?

Output Resistance



$R_{out} = f(k)$

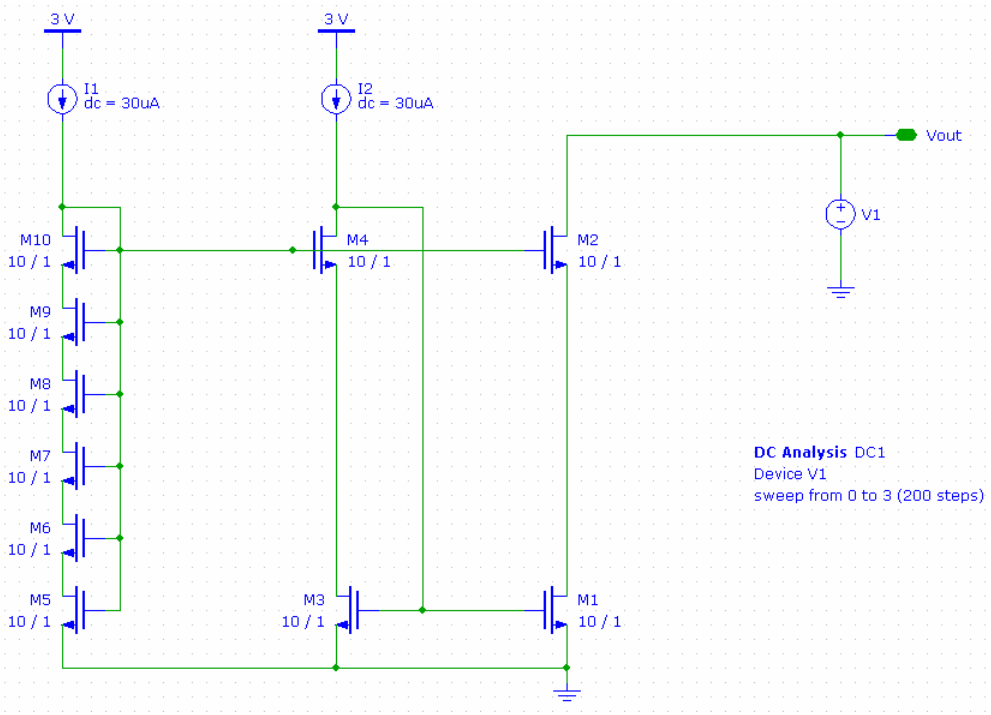


$$V_{DS1} = kV_1^*$$

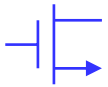
How choose k? Issues:

- Swing versus R_o
- Large k useful only for large V_{min} simultaneously
- Note: small or no penalty for large k and small V_{min}
- → typically choose k>1

High-Swing Bias Example



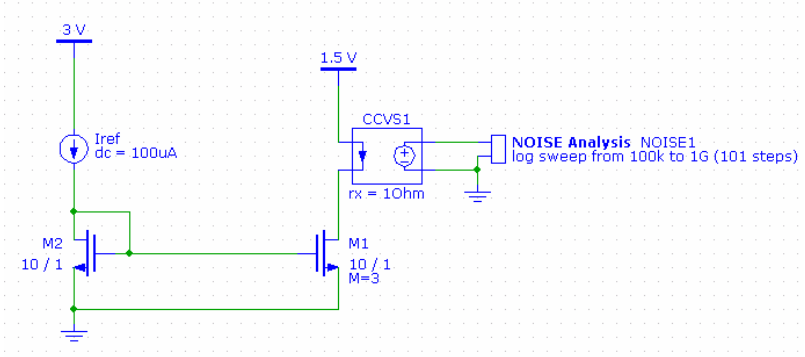
- M5 … M10 replace quarter size device
- All devices same size
- Less sensitive to body-effect
- $L_{current\text{-}source} = L_{cascode}$



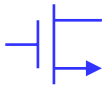
Noise

$$\overline{i_{on}^2} = \overline{i_{d1}^2} + M^2\overline{i_{d2}^2}$$
$$= 4k_BT\gamma\left(g_{m1} + M^2 g_{m2}\right)\Delta f$$
$$= 4k_BT\gamma g_{m1}\left(1+M\right)\Delta f$$
$$= 4k_BT\frac{1}{R_N}\Delta f$$

$$R_N = \frac{1}{g_{m1}}\frac{\gamma^{-1}}{1+M}$$
$$= \frac{r_o}{a_{v0}}\frac{\gamma^{-1}}{1+M} << R_o = r_o$$



- M2 (and I_{ref}!) can add noise
  - Choose small M (power penalty), or
  - Filter at gate of M1
- Current source FOMs
  - Output resistance R_o
  - Noise resistance R_N
  - **Active sources boost R_o, not R_N**



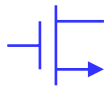
V_{min} versus Noise

$$V_{\min} = k \times V^* \qquad \text{typ.} \quad k = 1...2$$

$$R_N = \frac{1}{g_{m1}} \frac{\gamma^{-1}}{1+M}$$

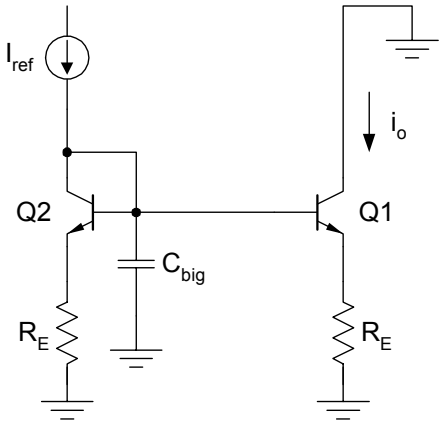
$$= \frac{V_{\min}}{2KI_D} \frac{\gamma^{-1}}{1+M}$$

- Voltage required for large R_o (saturation): V_{min} ~ V* (based on intuition from square-law model)
- Minimizing noise (for given I_D):
  → large R_N
  → **large V_{min} (k >> 1)**
- At odds with signal swing
  (to maximize the dynamic range)



Bipolar's, GaAs, …

$$\overline{i_{on}^2} = \underbrace{\overline{i_{cn}^2}\left|\frac{1}{1+g_m R_E}\right|^2}_{\text{BJT}} + \underbrace{\overline{i_{Rn}^2}\left|\frac{g_m R_E}{1+g_m R_E}\right|^2}_{R_E}\Delta f \qquad \left(\overline{i_b^2}=0\right)$$



a) $g_m R_E = 0$ $\qquad \overline{i_{on}^2} = 2k_B T g_m \Delta f$

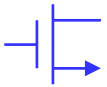
$$R_N = \frac{2}{g_m} = \frac{2V_t}{I_C} \qquad \text{set by } I_C$$

b) $g_m R_E >> 1$ $\qquad \overline{i_{on}^2} = 4k_B T \frac{1}{R_E}\Delta f$

$$R_N = R_E = \frac{V_{\min}}{I_C}\frac{V_{\min} - V_{ce}^{sat}}{V_{\min}}$$

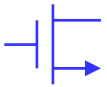
compare $\qquad R_{N,MOS} = \frac{V_{\min}}{I_D}\frac{\gamma^{-1}}{2K}$

- BJT and R_E contribute noise
- Increasing R_E lowers overall noise
- BJT and MOS exhibit essentially same noise / V_{min} tradeoff
- Lowest possible noise source is a resistor (and large V_{min}, V_{DD})



Small Signal Design Summary

- Determine g_m (from design objectives)
- Pick L
  - Short channel → high f_T
  - Long channel → high r_o, a_{v0}
- Pick $V^* = 2I_D/g_m$
  - Small V^* → large signal swing
  - High V^* → high f_T
  - Dynamic range: $P_{sig} \sim 1/V^*$, $P_{noise} \sim V^*$
- Determine I_D (from g_m and V^*)
- Determine W (SPICE / plot)
- **<u>Accurate</u> for short channel devices → key for design**



Device Parameter Summary

Device Parameter	Circuit Implications
V*	• Current efficiency, g_m/I_D • Power dissipation (I_D) • Speed (g_m) • Cutoff frequency, f_T → phase margin • Headroom, $V_{DS,min}$
L	• Cutoff frequency, f_T → phase margin • Intrinsic transistor gain (a_{v0})
W	• Obtain from L, I_D • Self loading (C_{GS}, C_{DB}, …)