A 90nm Power Optimization Methodology and its' Application to the ARM1136JF-S Microprocessor

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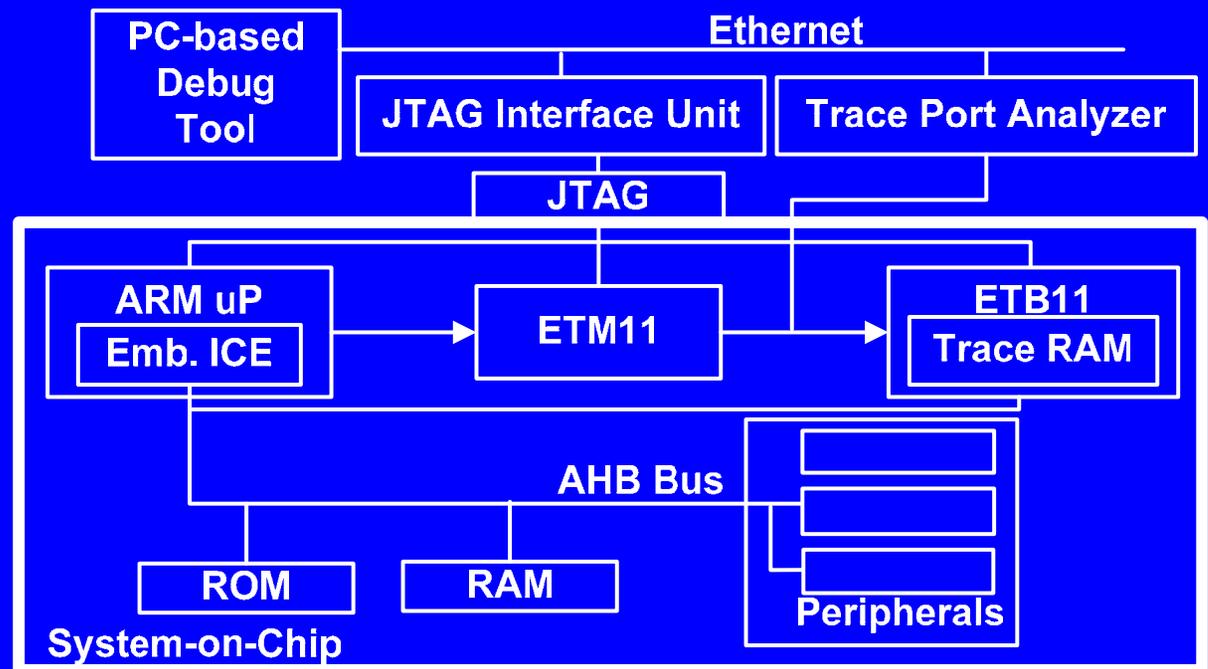San Jose, CA.
September 21, 2005**

Topics

- Introduction

- System and IC architecture

- Electrical/physical design methodology
  - RTL synthesis for multiple supply voltage operation and leakage/speed optimization
  - V_{DD} selection and power distribution
  - Clock gating

- System-level design validation

- Summarized parametric data

- Summary
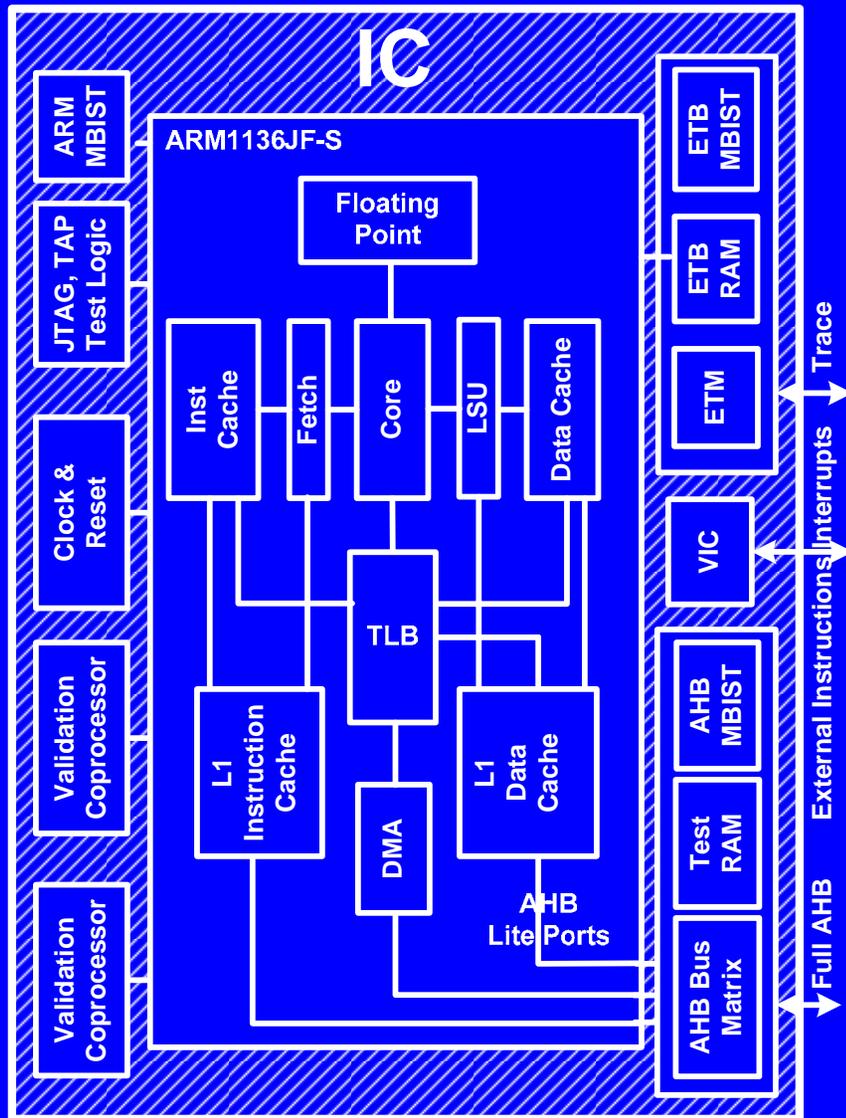
- Acknowledgments and references

Introduction

- SOC designs developed for consumer electronics products: Energy-efficient design critical
- Develop design methodology and techniques for power reduction
  - Focus on methodologies leverageable to synthesis-driven digital designs
    - IC: 355 MHz (typ.) in 90 nm CMOS
      - ARM1136JF-S microprocessor → higher frequency operation
    - Dual V_{DD} domains, dual-V_T cell libraries
- Collaborative effort (ARM, Cadence and TSMC)
  - SoC designed and manufactured
  - Measured power dissipation results (instrumented system)
    - Gaming and other applications utilized for evaluation
- Results to be presented

System architecture

- ARM RealView® Validation System
  - Instrumented system
- Run applications, measure performance
  - Games, other; power dissipation

PC-based Debug Tool		Ethernet	
	JTAG Interface Unit	Trace Port Analyzer	

JTAG

ARM uP Emb. ICE	ETM11	ETB11 Trace RAM

AHB Bus

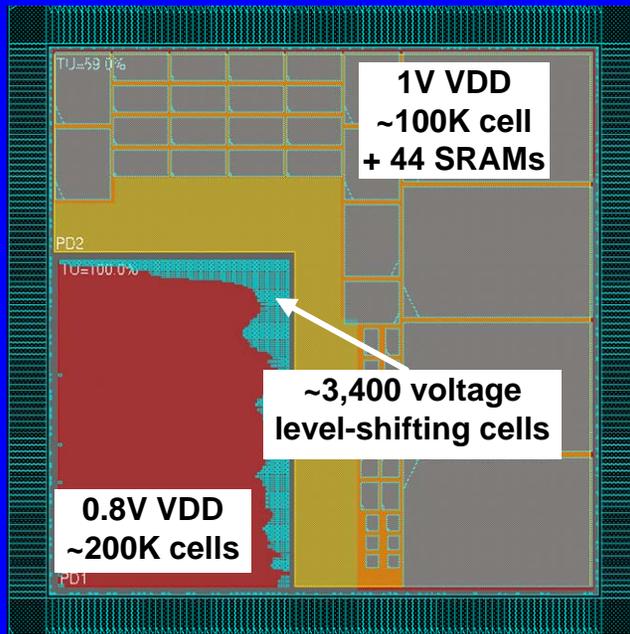| ROM | RAM | Peripherals |

System-on-Chip

IC architecture

- ARM1136JF-S microprocessor
  - 16k data + instruction cache
  - 16 kB TCM
  - Additional Tag RAMs and TLBs
  - 44 memory instances
  - ARM and Thumb instruction sets
  - Extended DSP instructions
  - Jazelle enabled technology
    - Direct execution of Java byte codes
- ETM11 trace macro, ETB11 trace buffer
- Advanced high-performance bus (AHB) bus fabric
  - Connect core AHB Lite ports to full AHB interface (pin accessible)
  - Access to 128 KB on-chip test RAM: Enable concurrent data transfers from any four ports
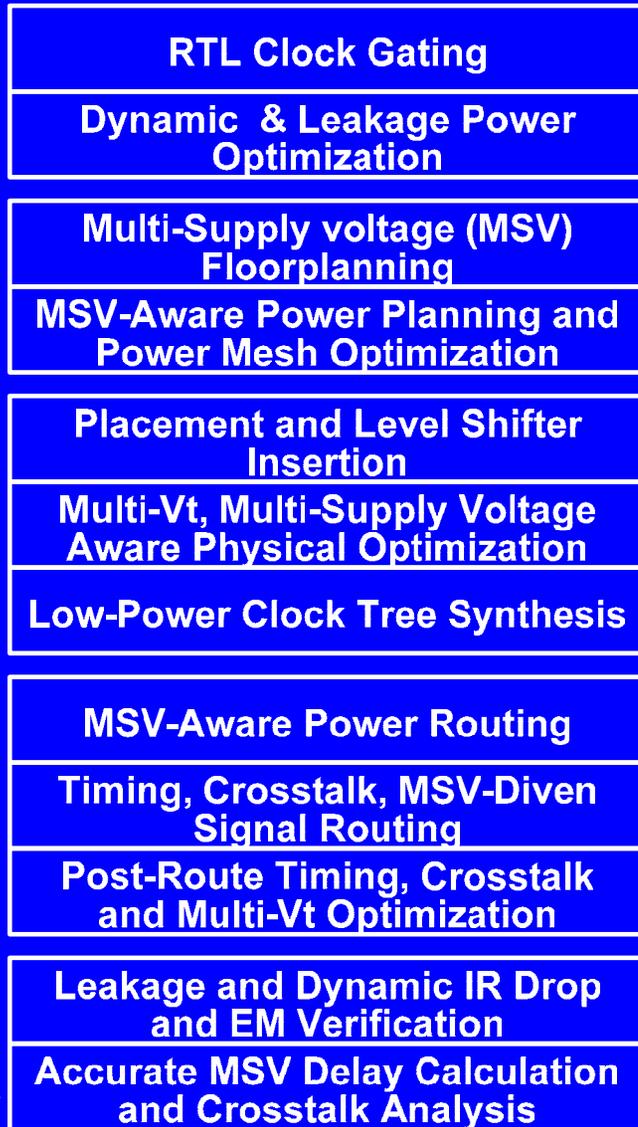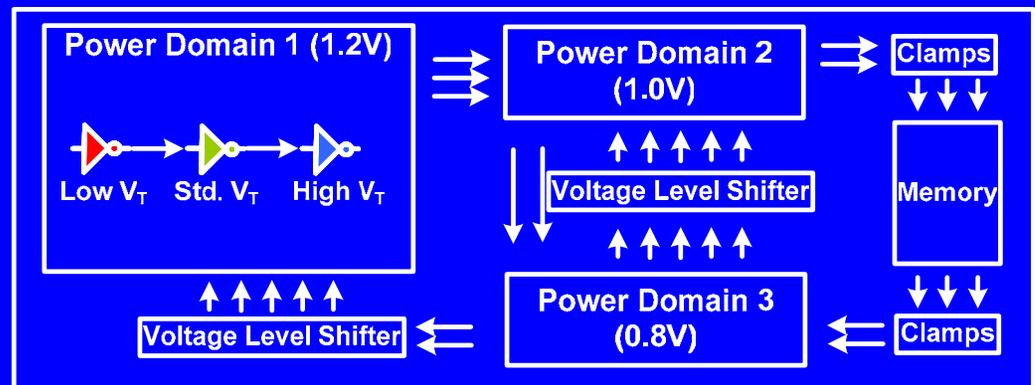
IC, design overview

1V VDD
~100K cell
+ 44 SRAMs

~3,400 voltage
level-shifting cells

0.8V VDD
~200K cells

- 300 K standard cell instances

- 44 SRAM instances

- 355 MHz typical operation in 90nm standard CMOS

- Electrical/physical design

  – ARM Artisan Physical IP

  – RTL synthesis for multiple supply voltage operation and leakage/speed optimization

  – V_{DD} selection and power distribution

  – Clock gating

  – Timing (electrical) closure in a multi-V_{DD} domain design (including ECOs)

Design methodology overview

Timing, Power and Area Optimization

RTL Clock Gating
Dynamic & Leakage Power Optimization

Multi-Supply voltage (MSV) Floorplanning
MSV-Aware Power Planning and Power Mesh Optimization

Placement and Level Shifter Insertion
Multi-Vt, Multi-Supply Voltage Aware Physical Optimization
Low-Power Clock Tree Synthesis

MSV-Aware Power Routing
Timing, Crosstalk, MSV-Diven Signal Routing
Post-Route Timing, Crosstalk and Multi-Vt Optimization

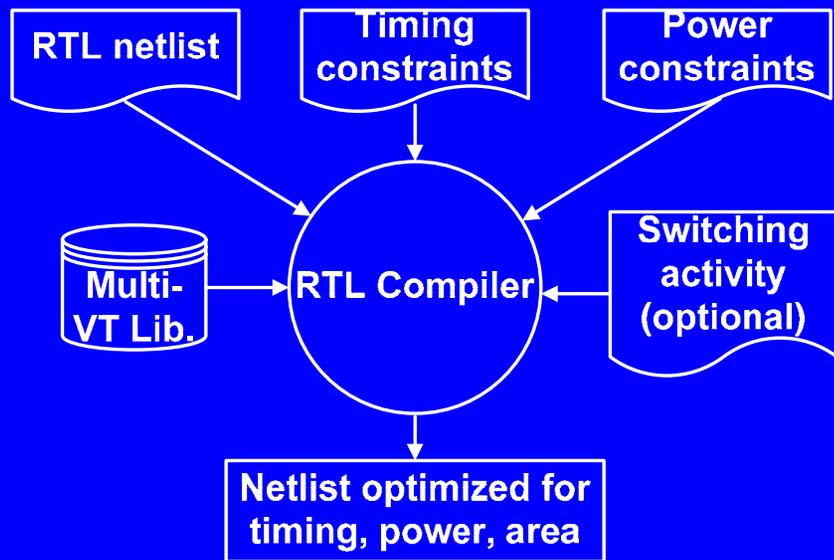| |
|---|
| **Leakage and Dynamic IR Drop and EM Verification** |
| **Accurate MSV Delay Calculation and Crosstalk Analysis** |

- Methodology leverageable to synthesized digital designs
  - Newly-developed and current-generation EDA tools
    - Single-pass concurrent optimization (timing, power, area)
    - Instance-specific numerical modeling of delay at multiple V_{DD} levels
      - <2% variance with respect to full circuit simulation

Power Domain 1 (1.2V) → **Power Domain 2 (1.0V)** → Clamps

Low V_T Std. V_T High V_T

Memory

Voltage Level Shifter

Voltage Level Shifter ← **Power Domain 3 (0.8V)** ← Clamps

Microprocessor verification

- Set code and memory configurations for microprocessor
- Verify RAM functionality in 90nm CMOS process
- Verify microprocessor functionality (RTL)
  - 700 test cases (>135K vectors)
  - Multi-day run time
  - Vector sets generated used subsequently for power dissipation analysis
    - VCD and TCF formats
- Fully verified RTL used as "golden reference"
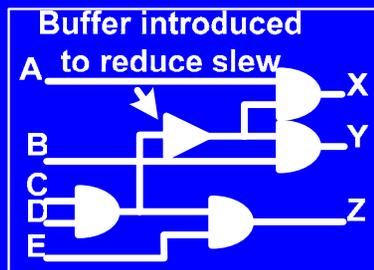 - Regression tests / functional verification prior to tape-out

MSV RTL synthesis

RTL netlist

Timing constraints

Power constraints

Multi-VT Lib.

RTL Compiler

Switching activity (optional)

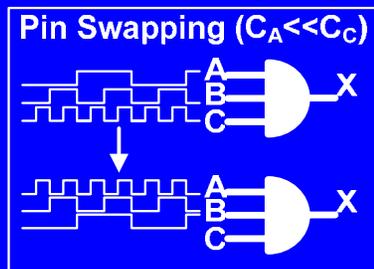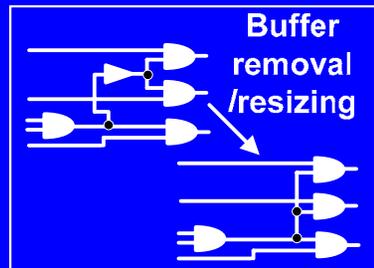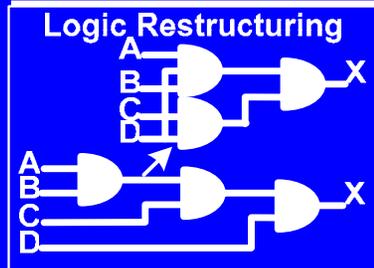Netlist optimized for timing, power, area

- Multiple supply voltages (MSV) synthesis
  - Newly-developed technology
  - Single-pass concurrent optimization for timing, area and power
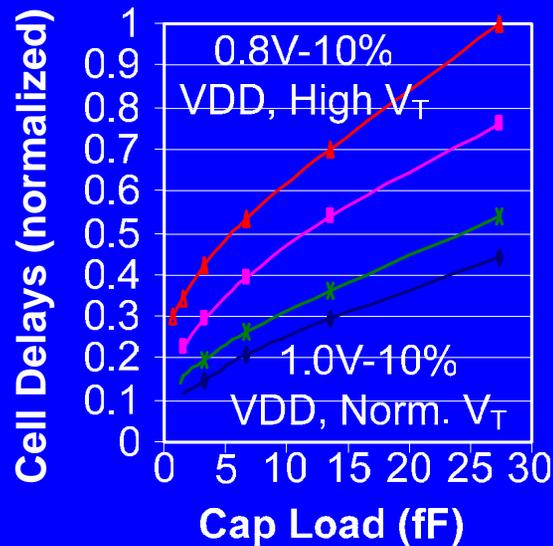 - 0.8 and 1.0 V_{DD} domains, dual-V_T cell libraries

Low V_T

Std. V_T

High V_T

Multi-VT Optimization
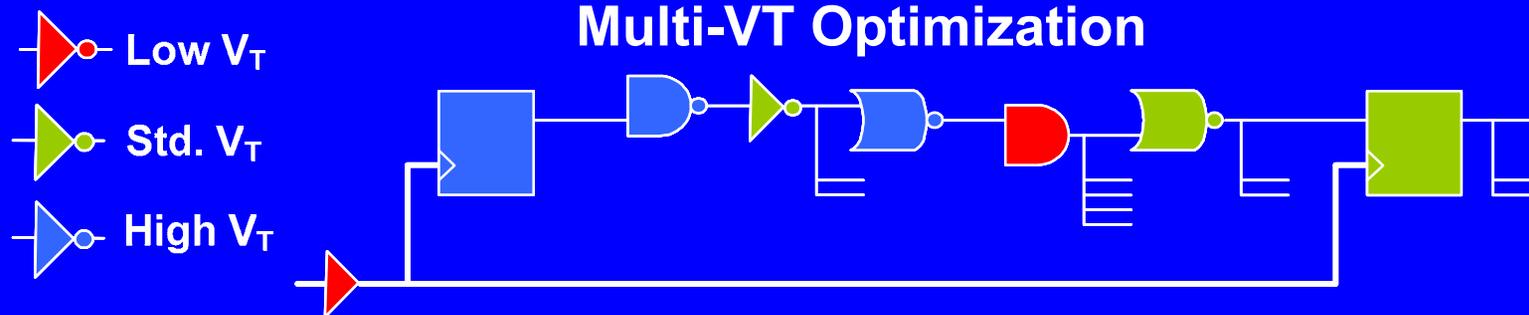
- 62% std. cells in 0.8 V domain; 38% in 1.0 V domain

Power optimization in synthesis

Logic Restructuring

Buffer removal /resizing

Pin Swapping ($C_A \ll C_C$)


Buffer introduced to reduce slew

- Logic restructuring
- Logic resizing
  - Before clock tree synthesis
- Buffer removal/resizing
- Pin swapping
  - Apply high transition rate signal nets to low capacitance inputs
- Transition rate buffering
  - Buffer slow transition nets to minimize duration in which both pFET and nFET conduct current simultaneously

V_{DD} domains and VLS cells

Cell Delays (normalized) vs Cap Load (fF)

0.8V-10% VDD, High V_T

1.0V-10% VDD, Norm. V_T

Optimum placement of level shifters

Automatic power routing

- 0.8 V, 1.0 V V_{DD} domains
  - Analyze standard cells delay, leakage, standby and dynamic power (2.5x delta)
  - Adequate performance for timing critical nets per domain
  - Customization → further improvements feasible
- Automated voltage level-shifting cells (VLS) insertion
  - For nets traversing V_{DD} domains
  - Align cells to avoid n-well spacing violations (domain perimeter placements)
 - Automated multi-V_{DD} power distribution and cell placements, antenna diode insertion
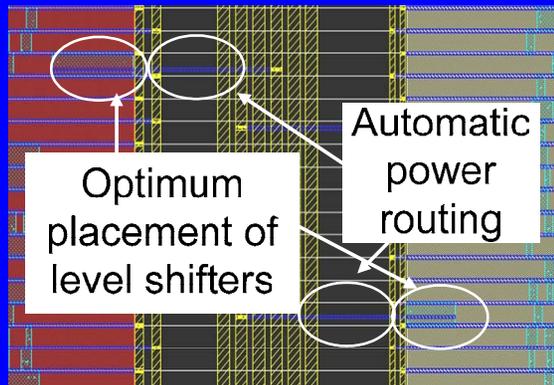
Clock gating

- Architectural clock gating included in uP RTL
- Automated design flow →add further clock gating inferred from RTL through low-power synthesis
  - 1,000 clock gated cells identified and managed → 85% registers gated
  - Shut off dynamic current in quiescent logic (application requirements)
- Clock de-cloning: reduce number of cells from 1,112 to 703
  - Move clock gating to the highest hierarchical node of the logic tree
   - Reduce power dissipation, insertion delay

Timing closure in multi- V_{DD} design (1)

Non-optimized

Optimized
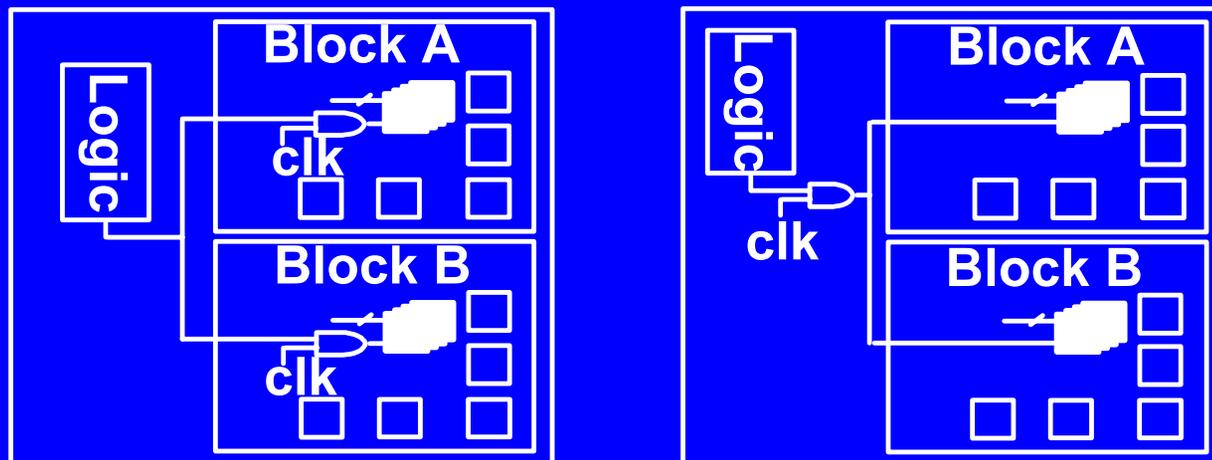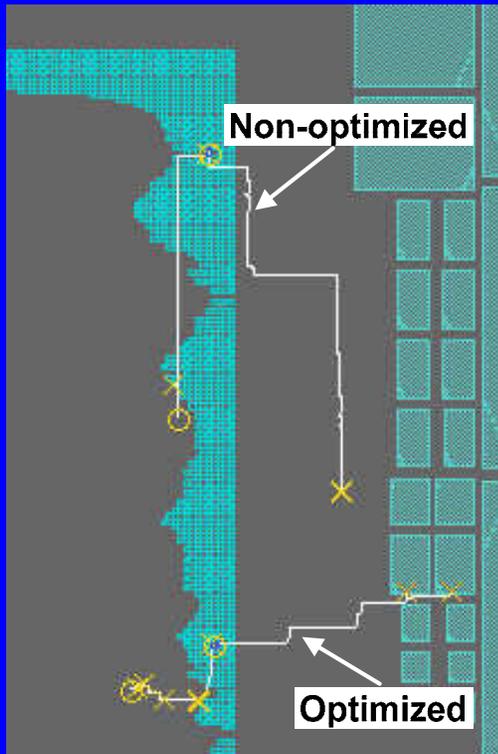
- VLS placement directly affects electrical performance
  - Optimal or detoured routing
  - Power-supply-aware timing and multi-V_{DD} supply constraints → drive placement
  - Support ECOs
  - Netlist modified to insert VLS cells where needed
- Present approach (automated)
  - Complete timing driven P&R without VLS; insert VLS; optimize

Timing closure in multi- V_{DD} design (2)

- Cell substitution with timing constraint
  - Replace standard-V_T with high-V_T cells
    - Net by net basis; same footprint as original cell
- Signal integrity addressed within P&R
  - ~10 of 500K nets required post-layout optimization
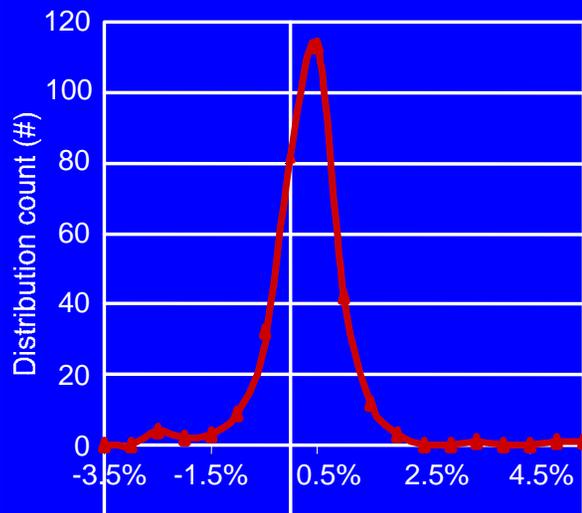
- Effective current source model (ECSM) →instance-specific multiple V_{DD} delay calculation
  - Standard cell libraries characterized for multiple V_{DD} values at outset
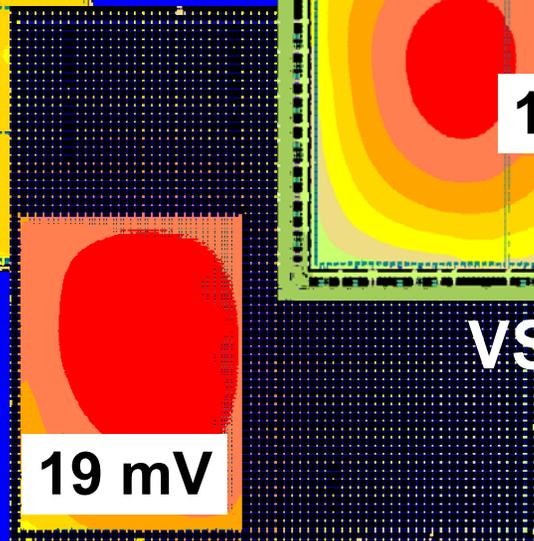 - Numerical model <2% deviation vs. full circuit simulation

IR drop analysis and optimization

- Grid-specific resistor meshes
- Dynamic power (manage di/dt)
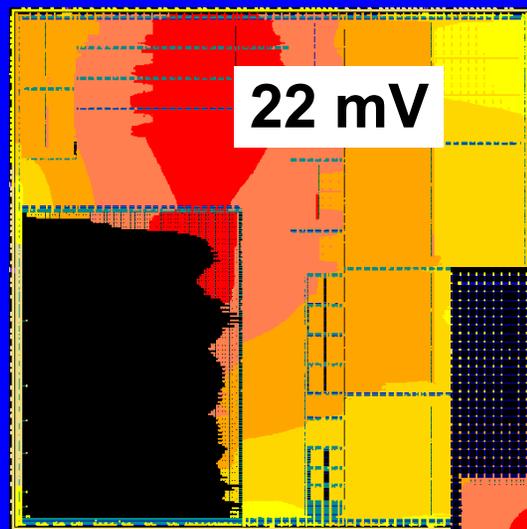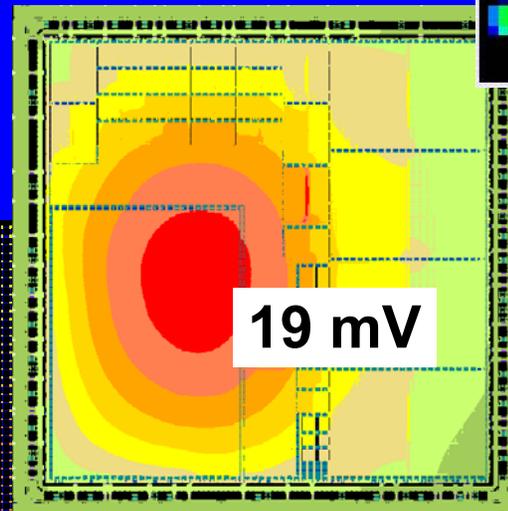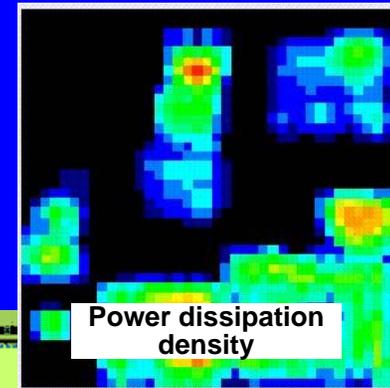
Power dissipation density

22 mV

1.0V V$_{DD}$

19 mV

0.8V V$_{DD}$

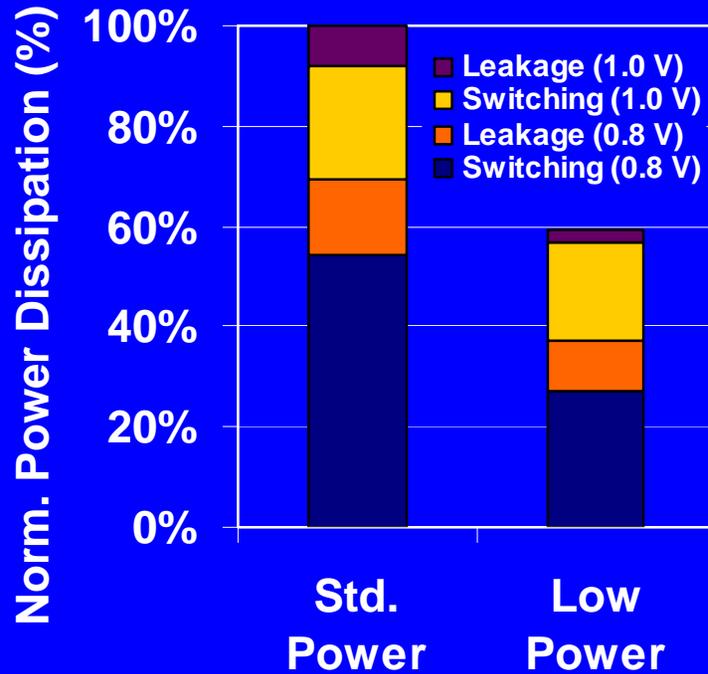**19 mV**

VSS
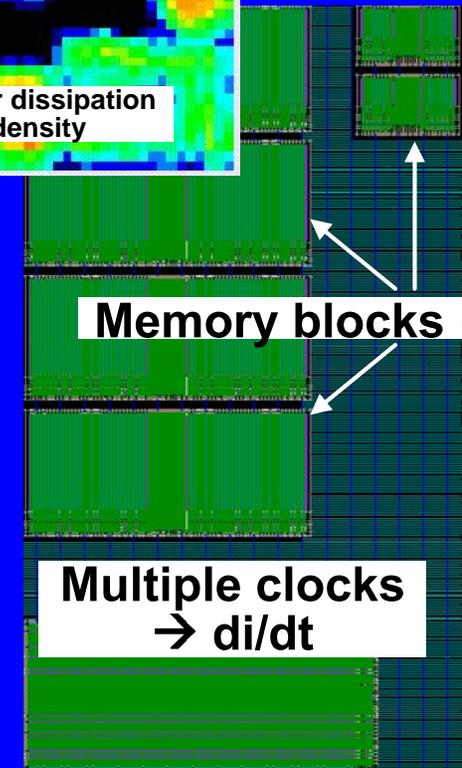
Memory blocks

Multiple clocks → di/dt

Dynamic IR drop analysis

System-level validation

- ~40% overall power reduction
- ~46% leakage power reduction
- 1.0V: 97.5% high-V_T cells
- 0.8V: 8.5% high-V_T cells

Chart legend:
- Leakage (1.0 V)
- Switching (1.0 V)
- Leakage (0.8 V)
- Switching (0.8 V)

Chart categories: Std. Power, Low Power. Y-axis: Norm. Power Dissipation (%)

Power Dissipation Reduction	VDD Domains		Total
	1.0V	0.8V	
Dynamic	12%	50%	38%
Leakage	69%	34%	47%
Total Power Savings			40%
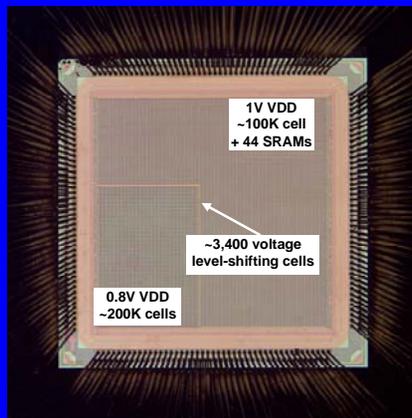
IC Functional Block	Dynamic Power Dissipation (mW/MHz)			
	Simulated Baseline (90nm)	Simulated Low Power (90nm)	Measured Low Power (90nm)	Measured Power (130 nm; ARM)
Core	0.28	0.14	0.10	0.60
Other	0.36	0.32	0.21	
Total	0.64	0.46	0.31	

1V VDD ~100K cell + 44 SRAMs

~3,400 voltage level-shifting cells

0.8V VDD ~200K cells

Summary

- Methodology obtained ~40% overall and 46% and leakage power reduction
  - Managed leakage power with dual-V_T cells and dual V_{DD} domains
  - Managed dynamic power with dual V_{DD} domains, dual-V_T cells, voltage scaling and automated clock gating
  - Power integrity verified throughout the design process
- Developed design methodology and techniques for power reduction
  - Single-pass synthesis with concurrent optimization (timing, power, area)
  - Newly-developed and current-generation EDA tools
  - Methodology leverageable to synthesis-driven digital designs

Summarized IC data

Parameter	Data
Clock Frequency	355 MHz (Typ. Conditions)
Technology	TSMC 90G
Transistor Count	22M
Core Voltage	1.0V, 0.8V
I/O Voltage	3.3V
Pin Count	362

Acknowledgments and references

- Acknowledgments
  - We thank C. Chu, A. Gupta, J. Goodenough, A. Harry, C. Hopkins, L. Jensen, T. Valind, L. Milano, A. Iyer, P. Mamtora, J. Willis, M. McAweeney, R. Williams and the ARM Physical IP team for their contributions

- References
  - Gartner- WW ASIC/ASSP, FPGA/PLD and SLI/SOC App. Fcst., 1Q04
  - B. Calhoun, "Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS," ISSCC, 2/05
  - S. Henzler, "Sleep Transistor Circuits for Fine-Grained Power Switch-Off with Short Power-Down Times," ISSCC, Feb. 05
  - http://www.arm.com/pdfs/DUI0273B_core_tile_user_guide.pdf.
  - A. Khan et al., "Design and Development of 130-nanometer ICs for a Multi-Gigabit Switching Network System," CICC, Oct. 04
  - D. Desharnais, "Nanometer IC routing requires new approaches," EEDesign.com, Dec. 03
  - A. Khan et al., "A 150 MHz Graphics Rendering Processor with 256Mb Embedded DRAM," ISSCC, Feb. 2001
  - G. Paul, et al., "A Scalable 160Gb/s Switch Fabric Processor with 320Gb/s Memory Bandwidth," ISSCC, Feb. 04