26.8: A 1.9GHz Single-Chip CMOS PHS Cellphone

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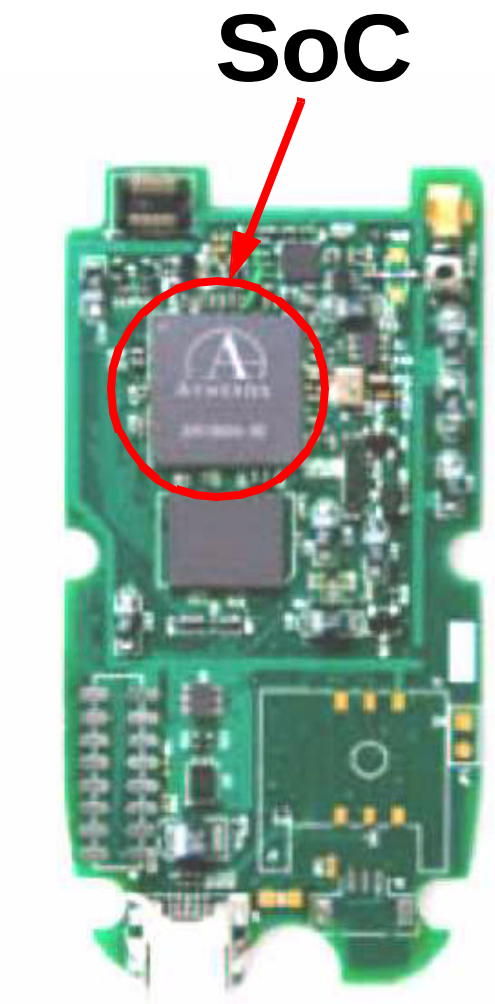
Outline

- Introduction
- Overall Architecture
- RF Transceiver
  - Synthesizer
  - Receiver
  - Transmitter
- Calibration
- Measurement Results

Integrated PHS SoC Solution

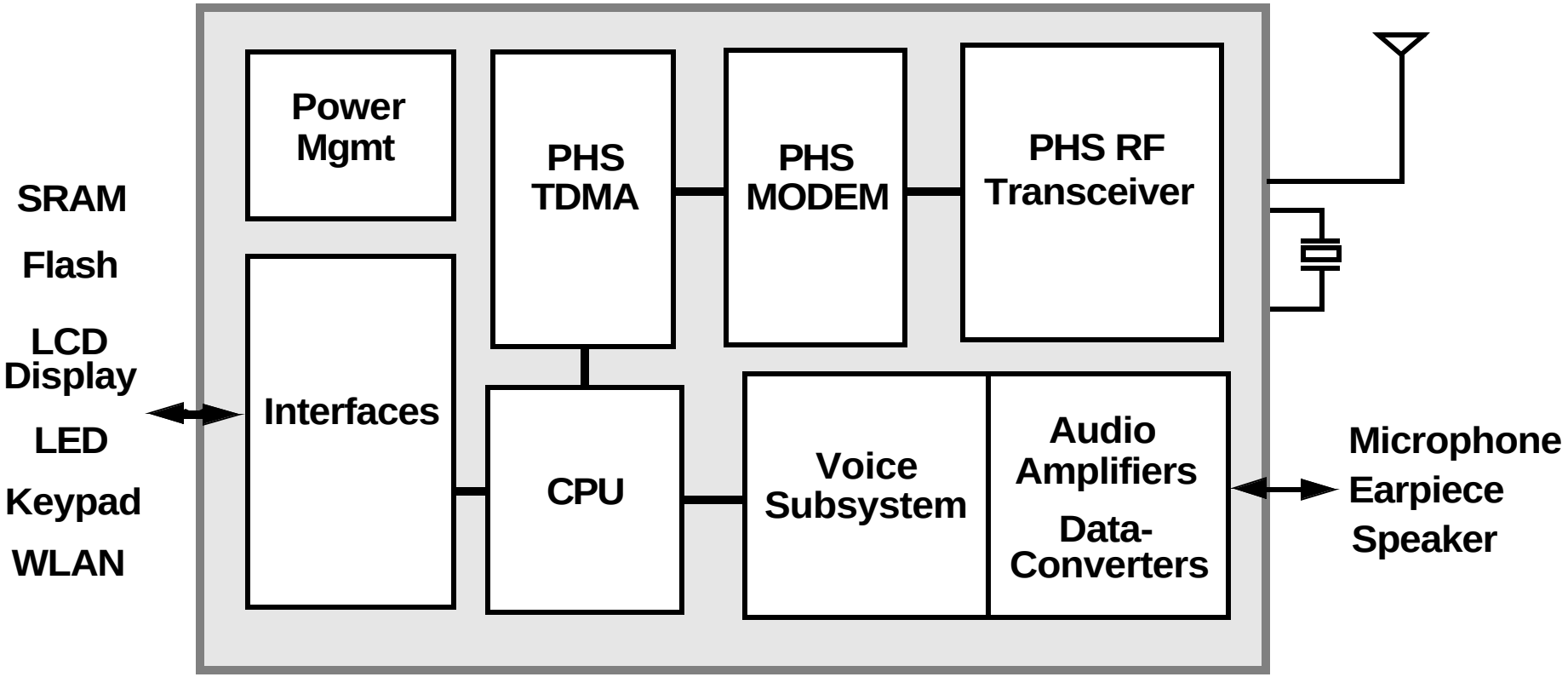
- **Personal Handy-Phone System (PHS)**
  - **Commercially launched in 1995**
  - **Resurgence in China (> 50M subscribers in 2004)**
- **Single-Chip PHS Solution in 0.18㎜ CMOS**
  - **RF/Analog: RF transceiver, audio/voiceband data converters and audio amplifiers**
  - **Digital: PHS MODEM, TDMA, CPU, Voice subsystem, Interfaces**
- **PHS System**
  - **TDMA/TDD - Time Domain Multiple Access / Duplexing**
  - **π/4 QPSK modulation with 192kHz channel bandwidth**
  - **1.9GHz frequency band, 300kHz channel spacing**
  - **Support seamless handover ® fast channel switching**

Advantages of System-on-Chip

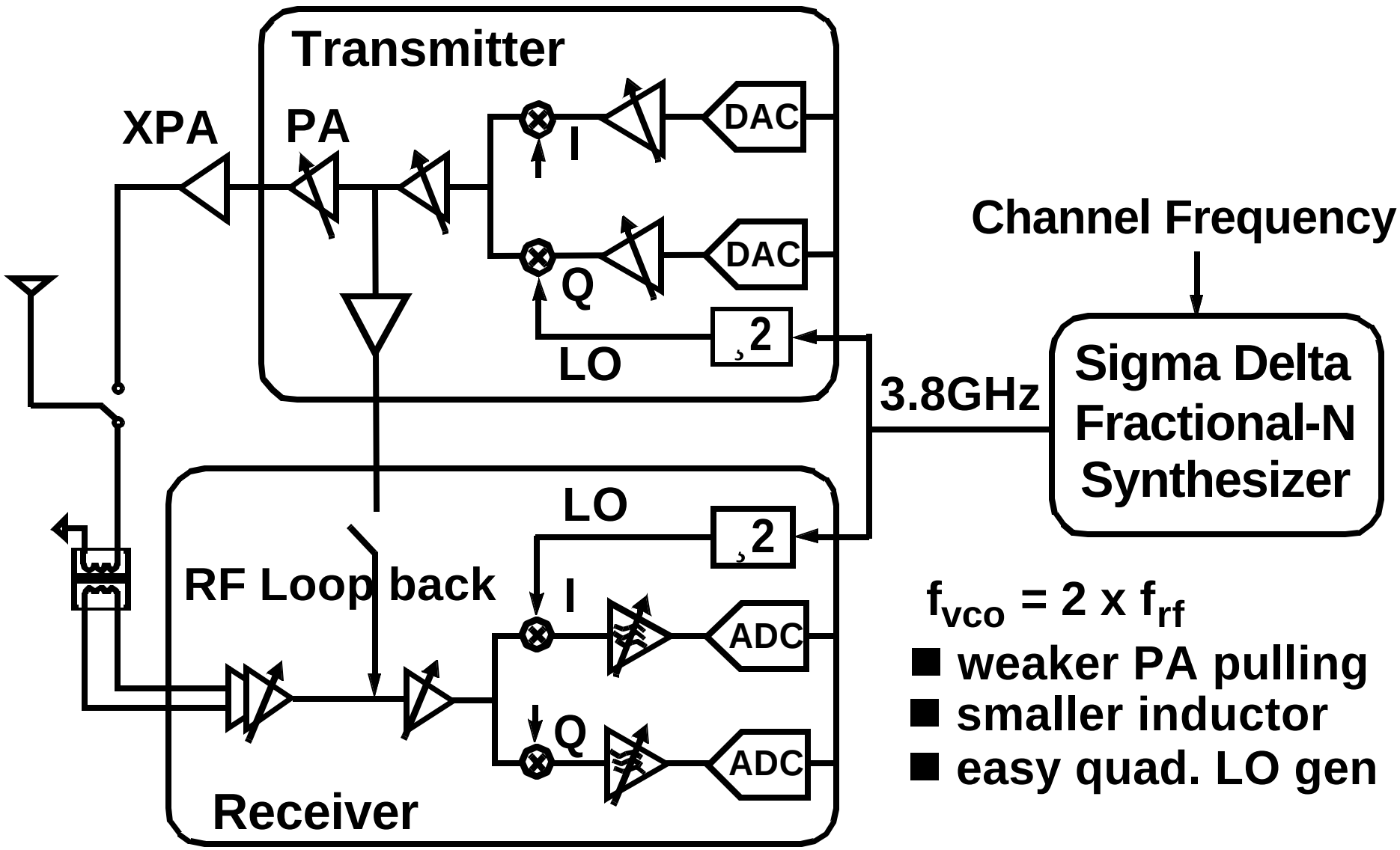


- **Low cost, small form factor with fewer external components**
- **Digital calibration**
  - **Wide digital-analog interface without package pins and associated power for I/Os**
  - **Digital calibration to repair analog impairments, eases requirements of analog RF circuits**

Block Diagram of Single-Chip PHS Cellphone



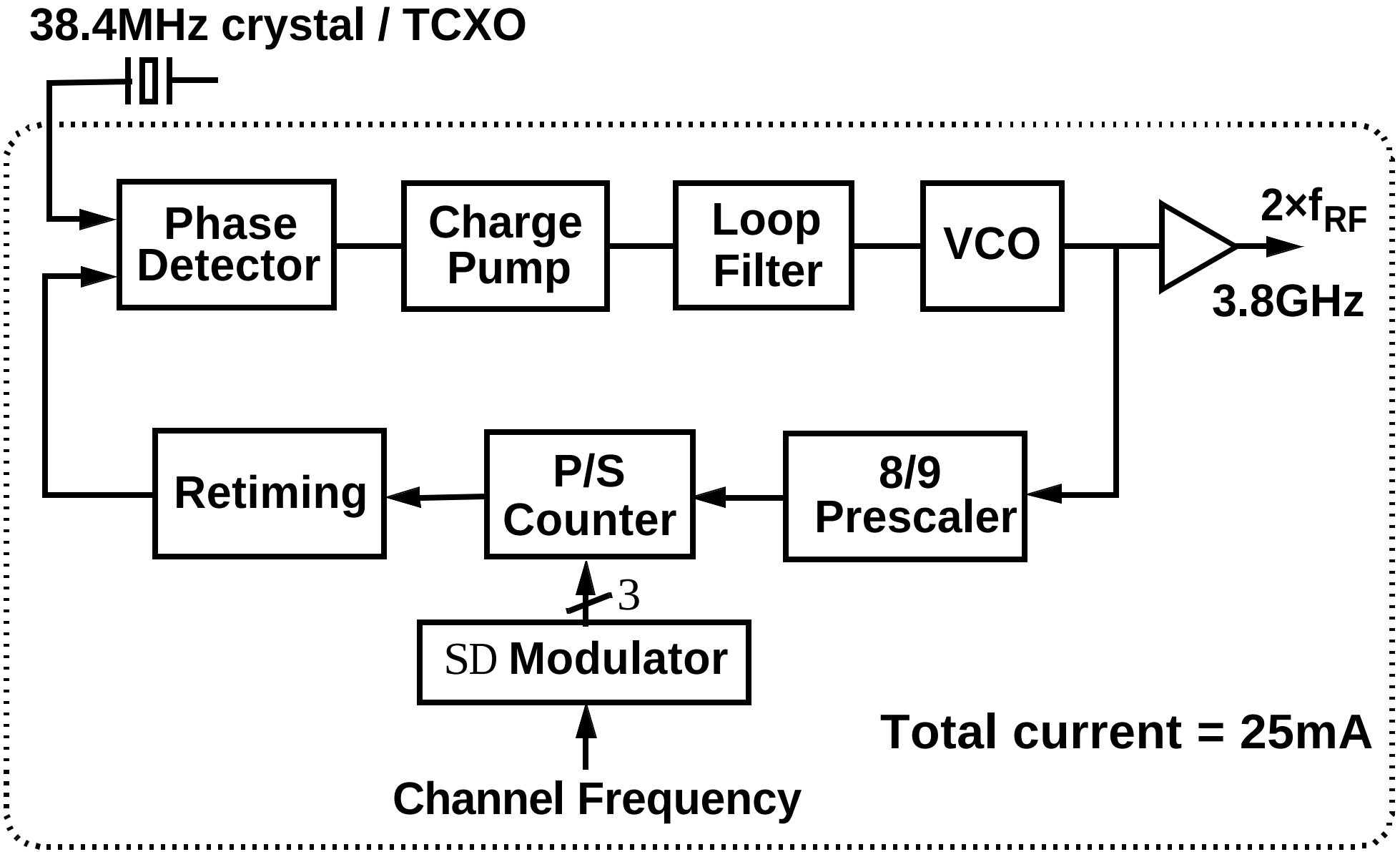
RF Transceiver Block Diagram



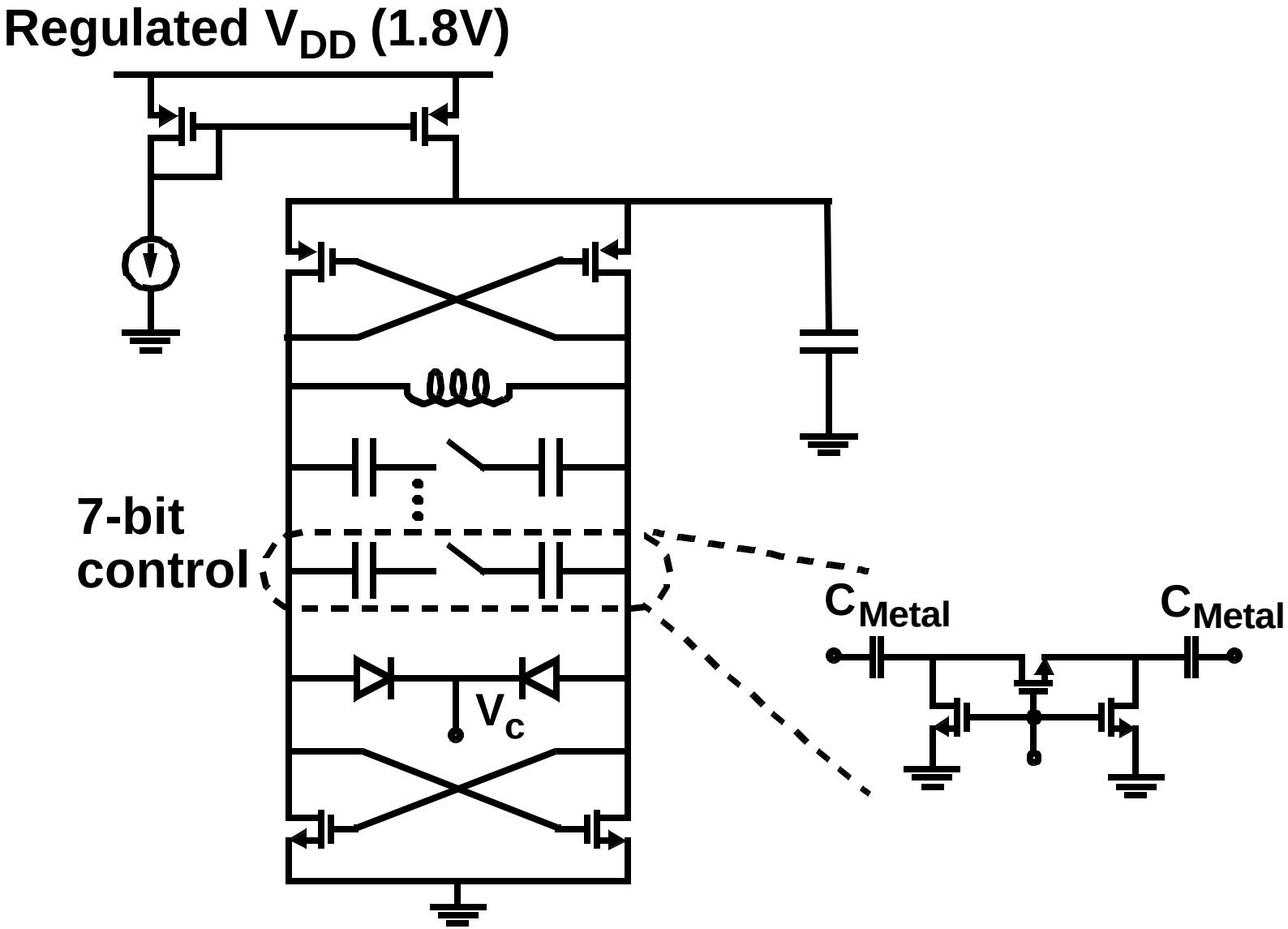
$f_{vco} = 2 \times f_{rf}$

- weaker PA pulling
- smaller inductor
- easy quad. LO gen

Sigma-Delta Fractional-N Synthesizer

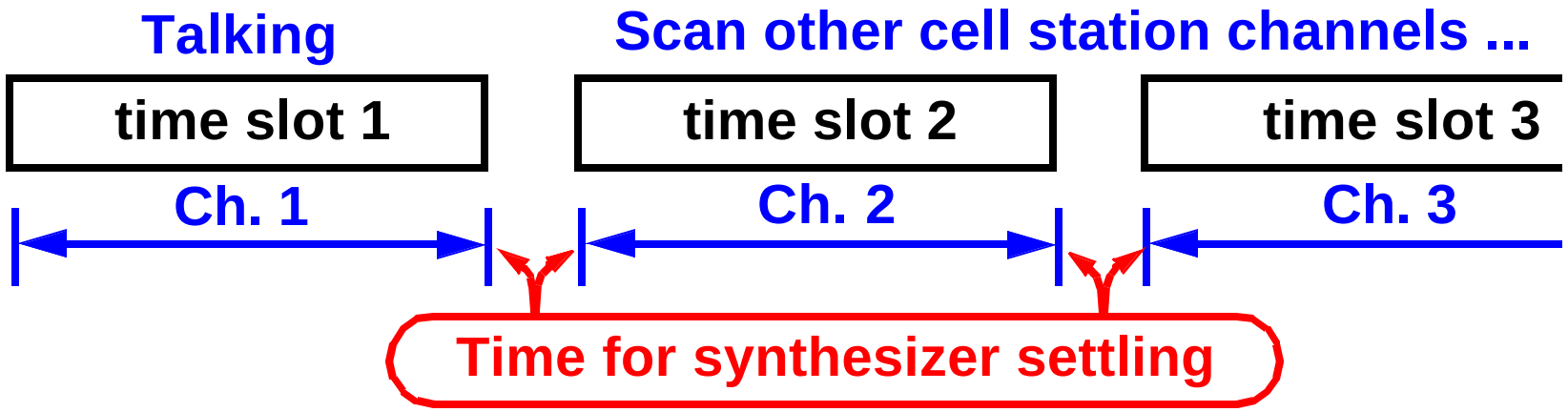


Voltage Controlled Oscillator

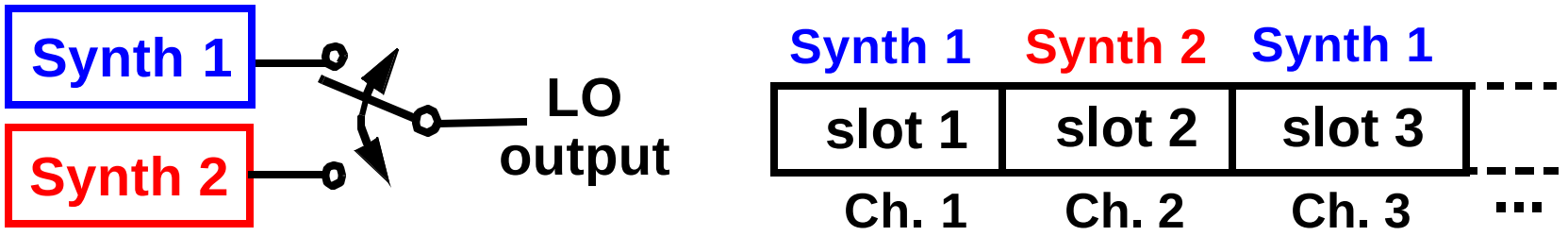


Fast Synthesizer Settling (I)

- Seamless handover support ® requires fast channel switching



- Traditional approach: Use two interleaving synthesizers ® power and area penalty

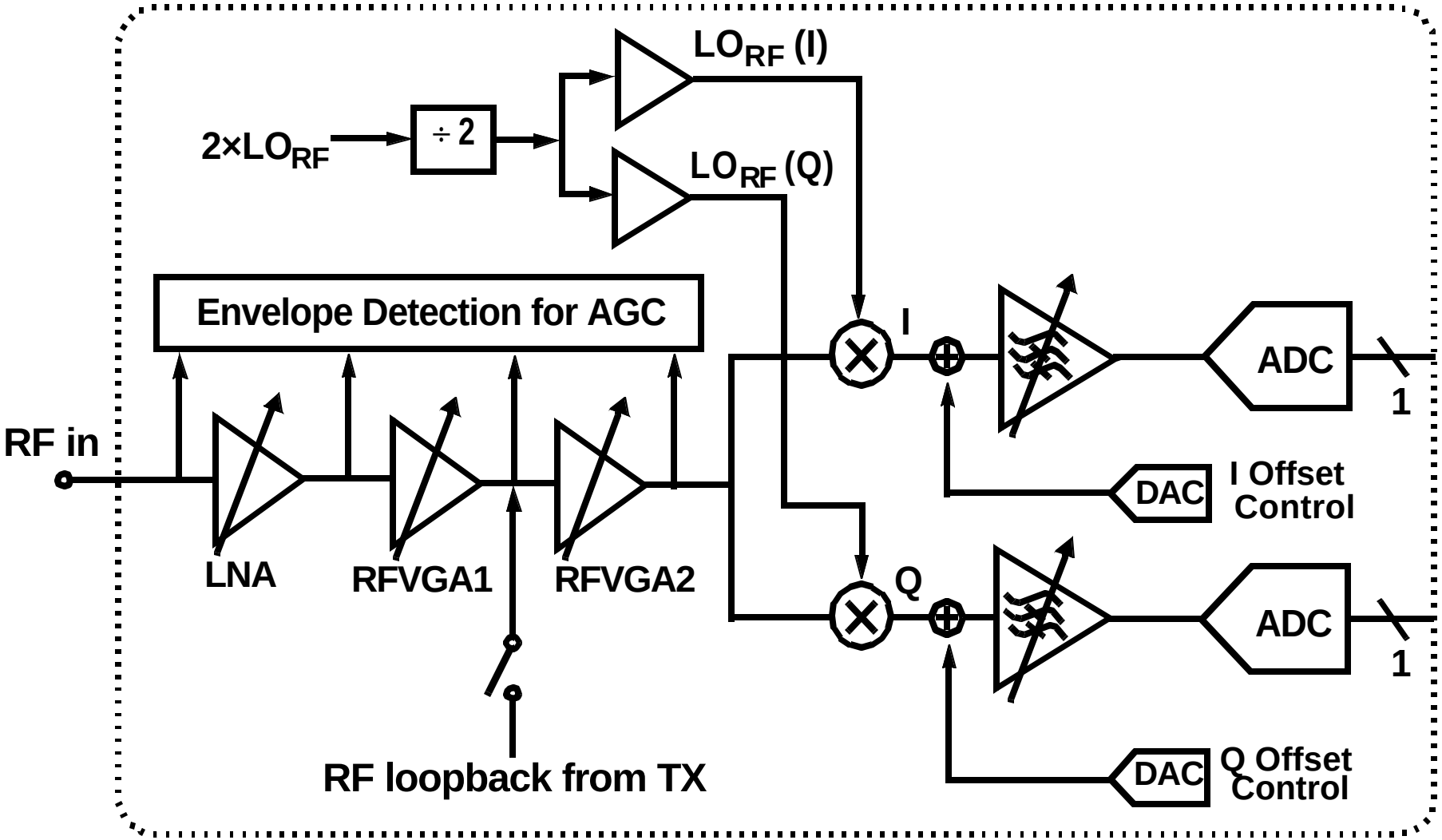


- We use only one synthesizer with fast settling

Fast Synthesizer Settling (II)

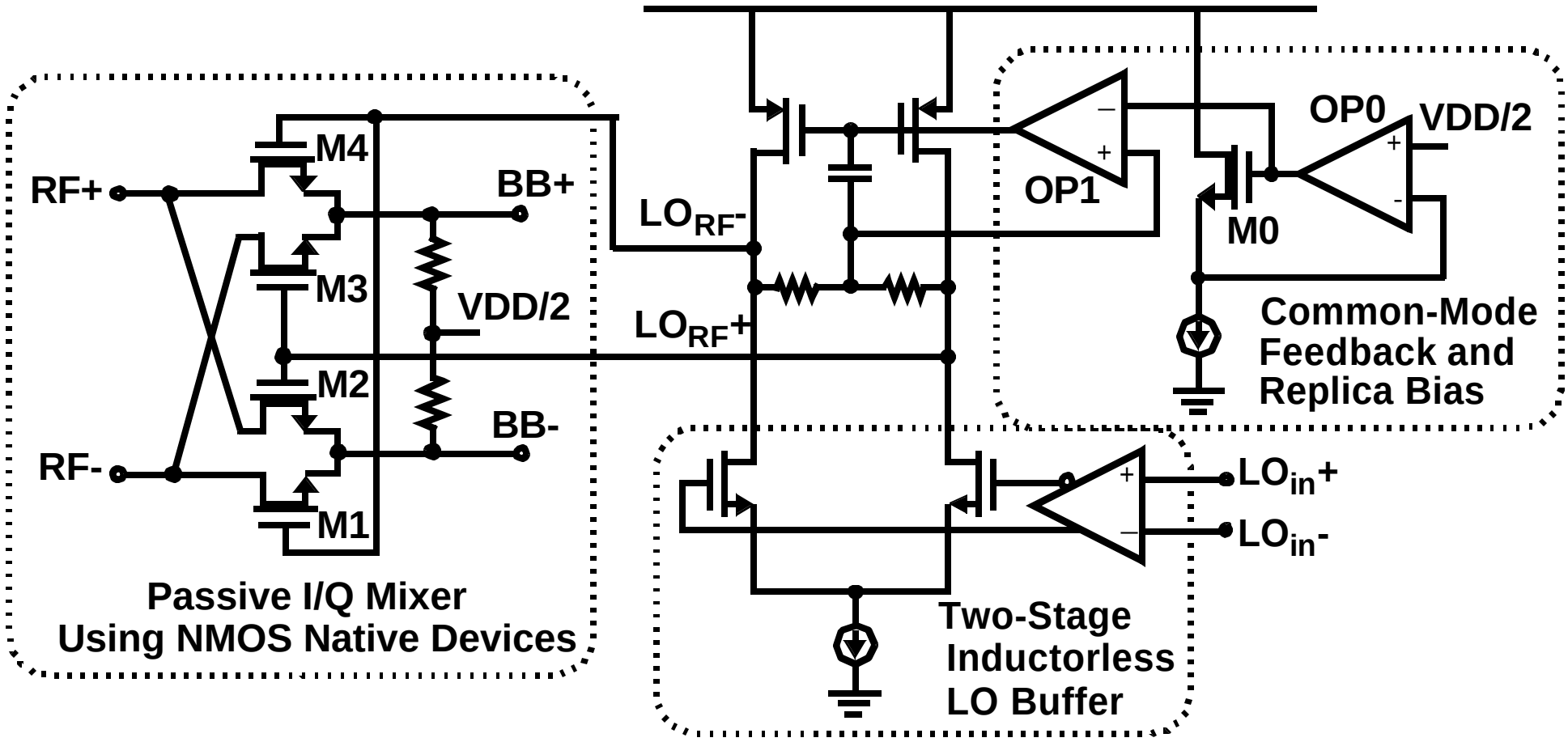
- **Tradeoff between settling time and phase noise: Loop bandwidth optimization**
  - **Wide loop BW for fast settling**
  - **Low loop BW to suppress $\Sigma\Delta$ quantization noise**
  - **Optimized loop BW = 120kHz**
- **Avoid over-design ® Minimizing loop BW variation**
  - **BW = $(K_{vco}\, I_{cp}\, R_s) / (2\pi N)$**
  - **V_{ctrl} within 200mV ® K_{vco} is roughly constant**
  - **I_{cp} tracks process variation of R_s ® $I_{cp}R_s$ constant**
- **Loop BW dynamically adjusted during switching to speed up frequency transient response**
- **Resulting settling time = 15μs**

Direct Conversion Receiver

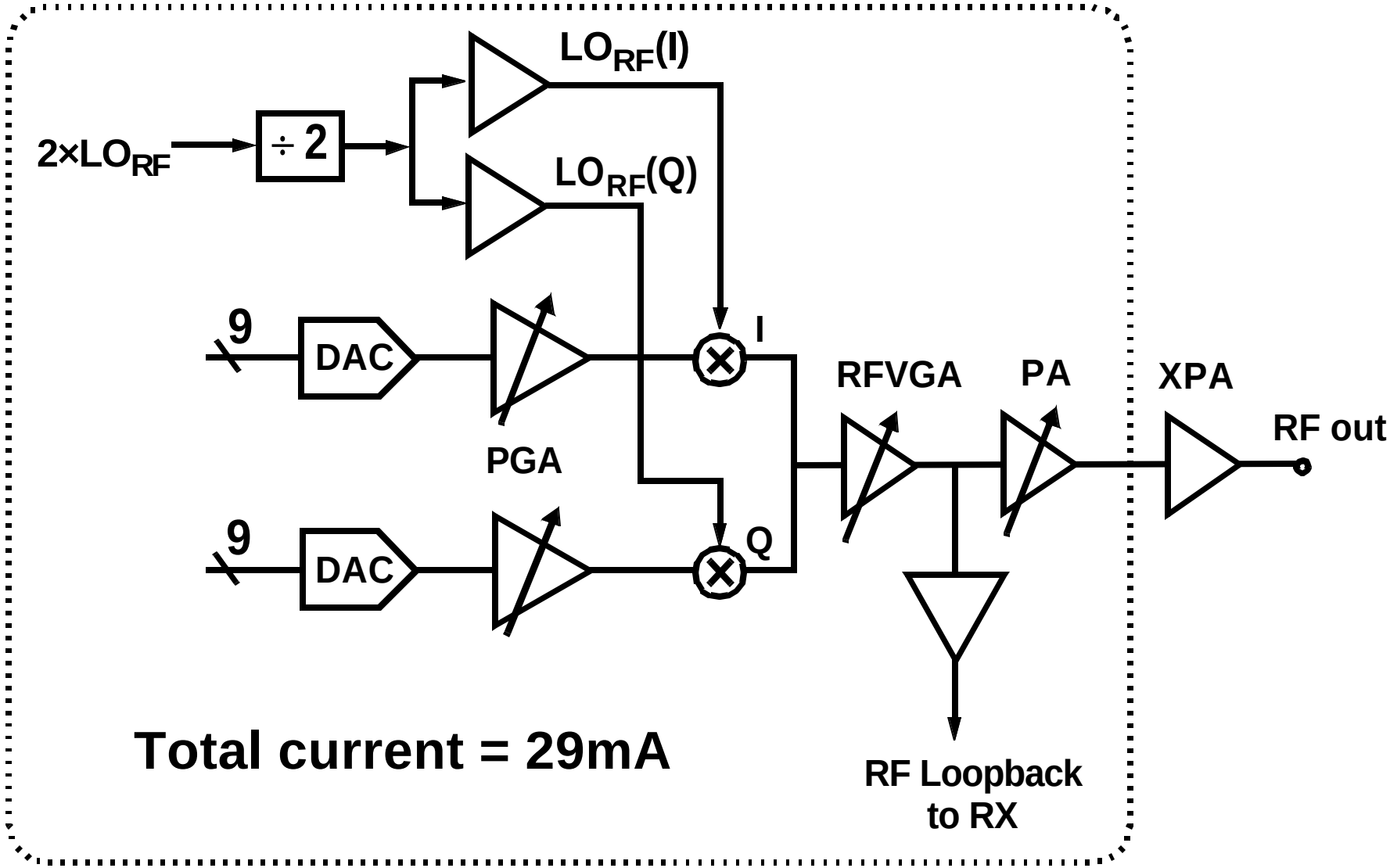


Total current = 32mA

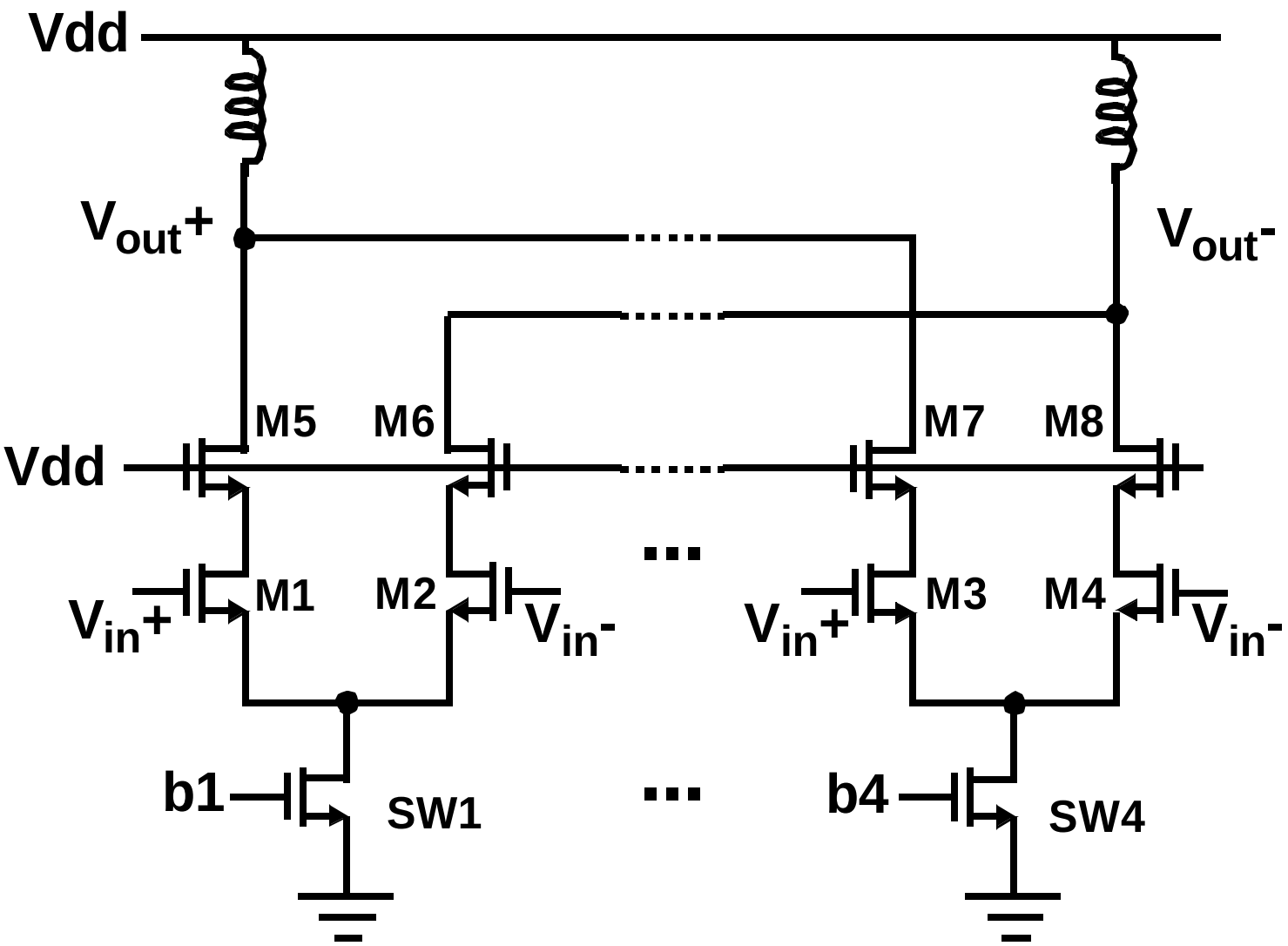
Receive Mixer and LO Buffers



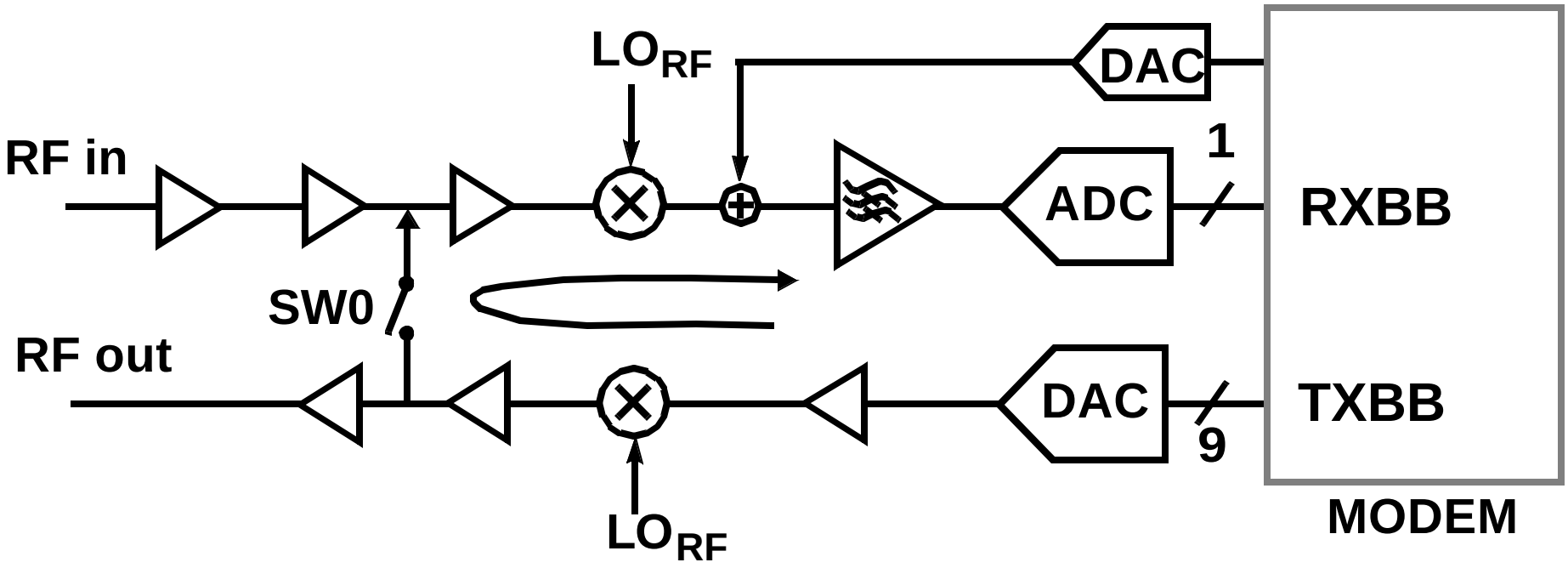
Direct Conversion Transmitter



Segmented Power Amplifier

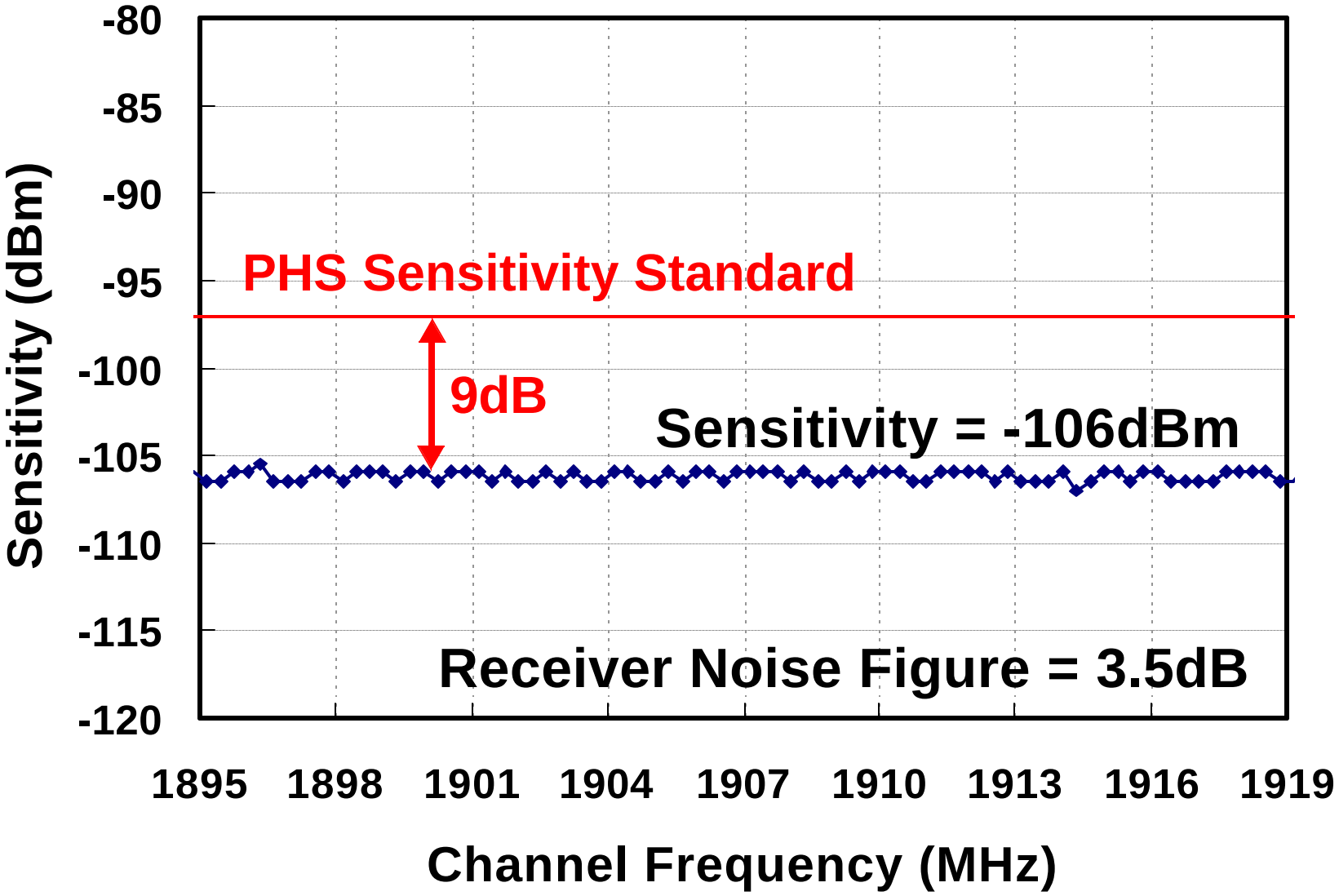


Digital Calibration and RF Loopback

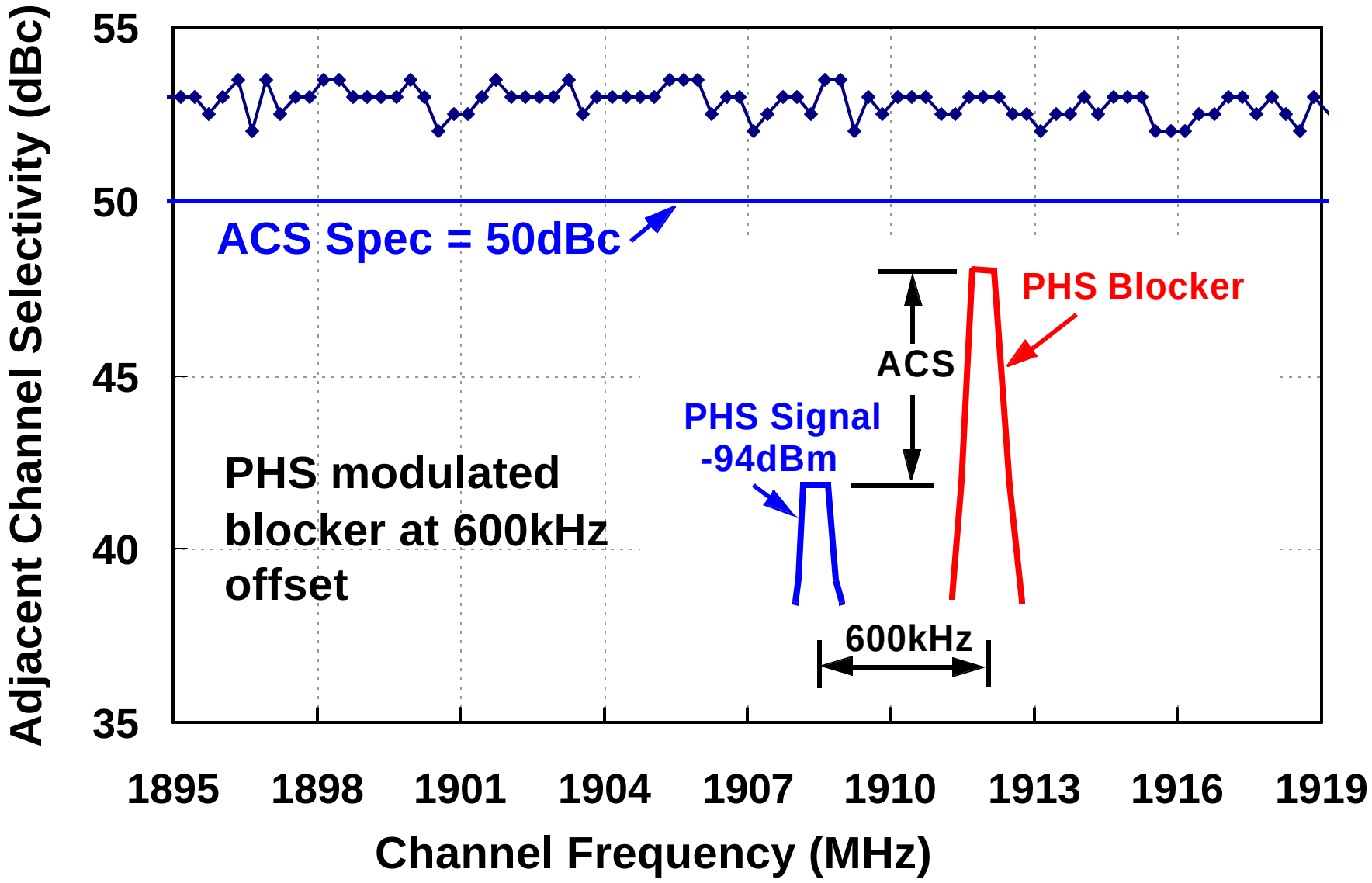


- **Calibration of Analog Imperfections**
  - **Receiver filter bandwidth**
  - **Receiver DC offset**
  - **I/Q mismatch**
  - **Transmitter carrier leak**

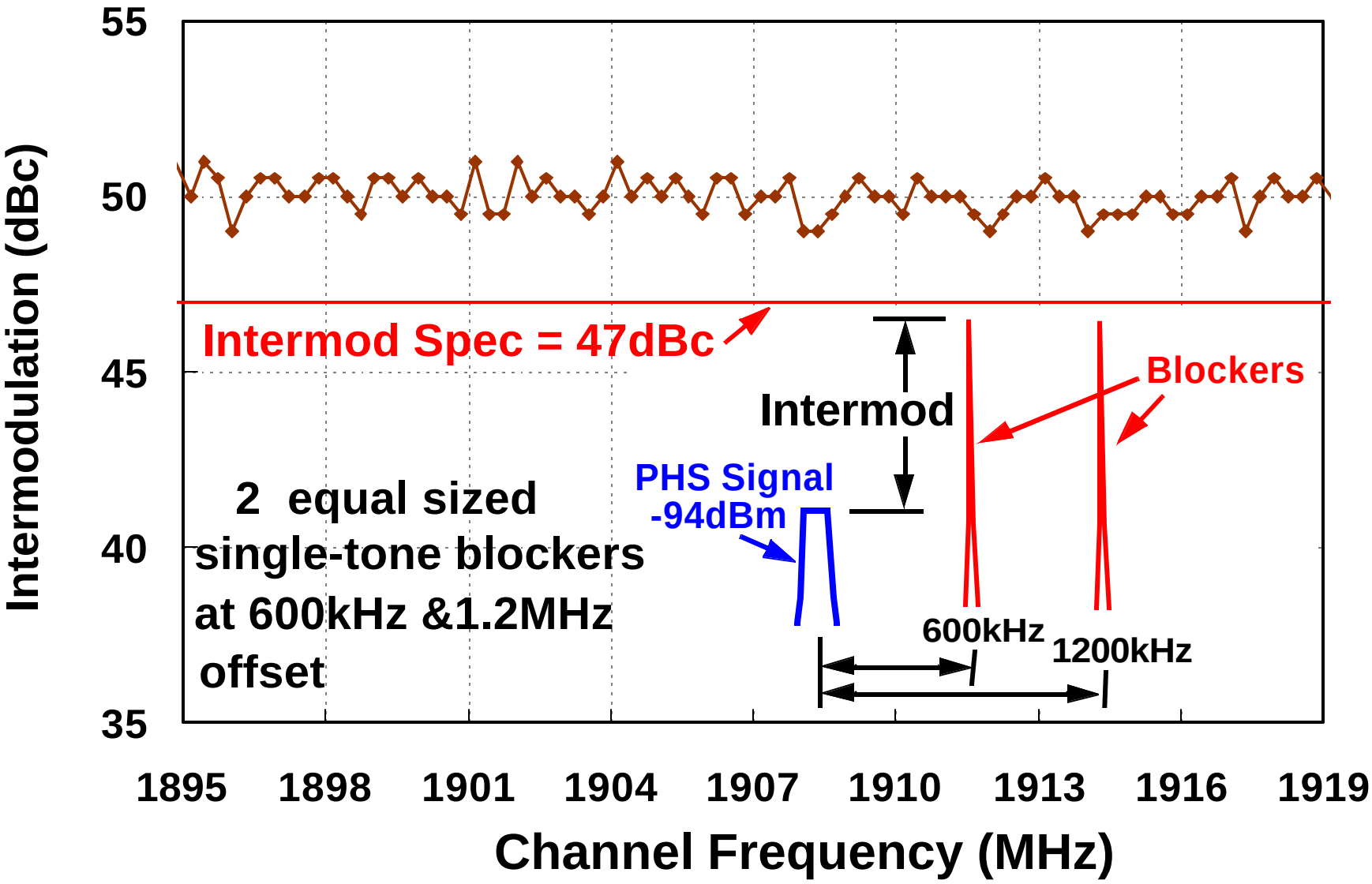
Receiver Sensitivity



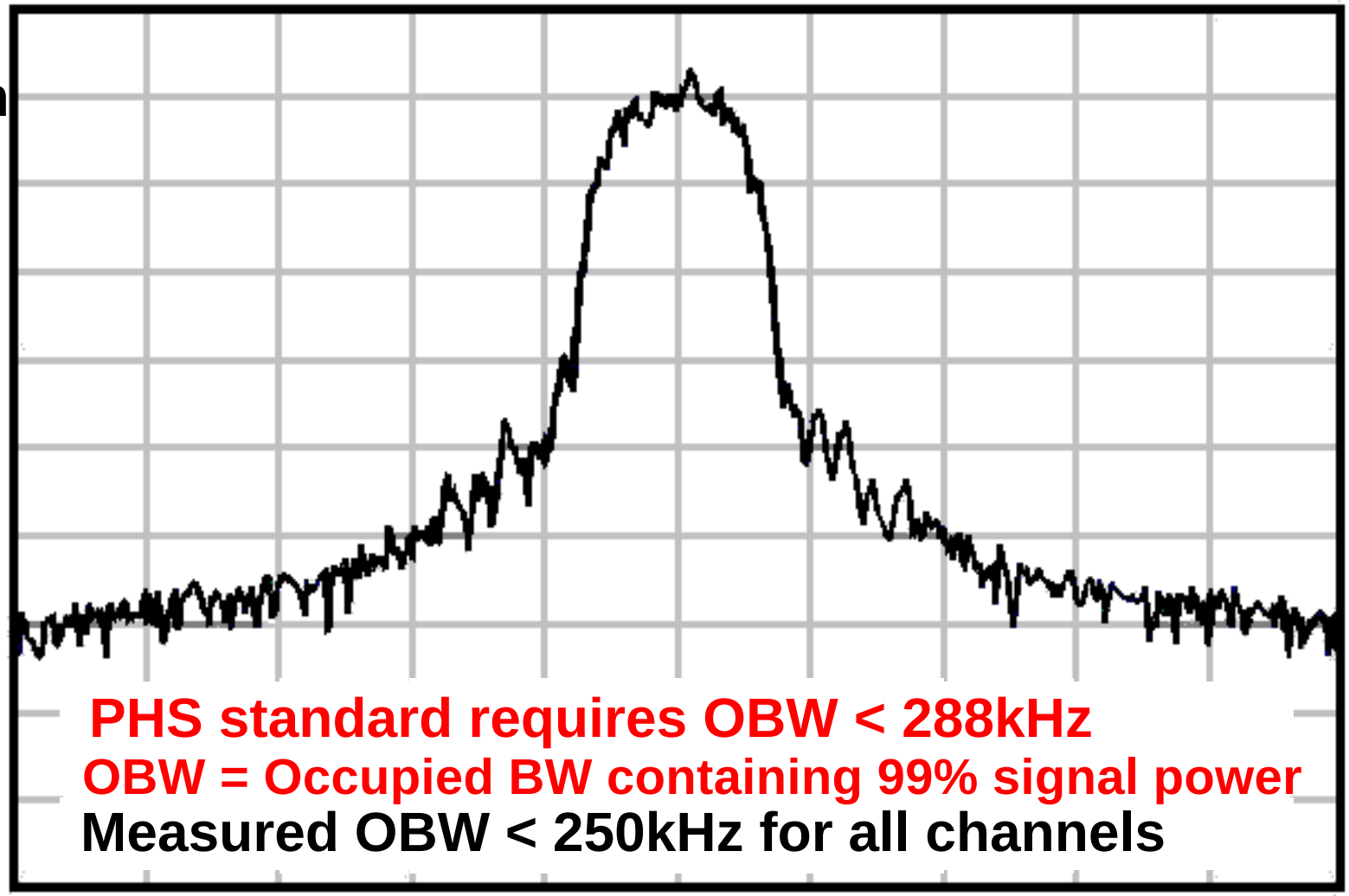
Receiver Adjacent Channel Selectivity (ACS)



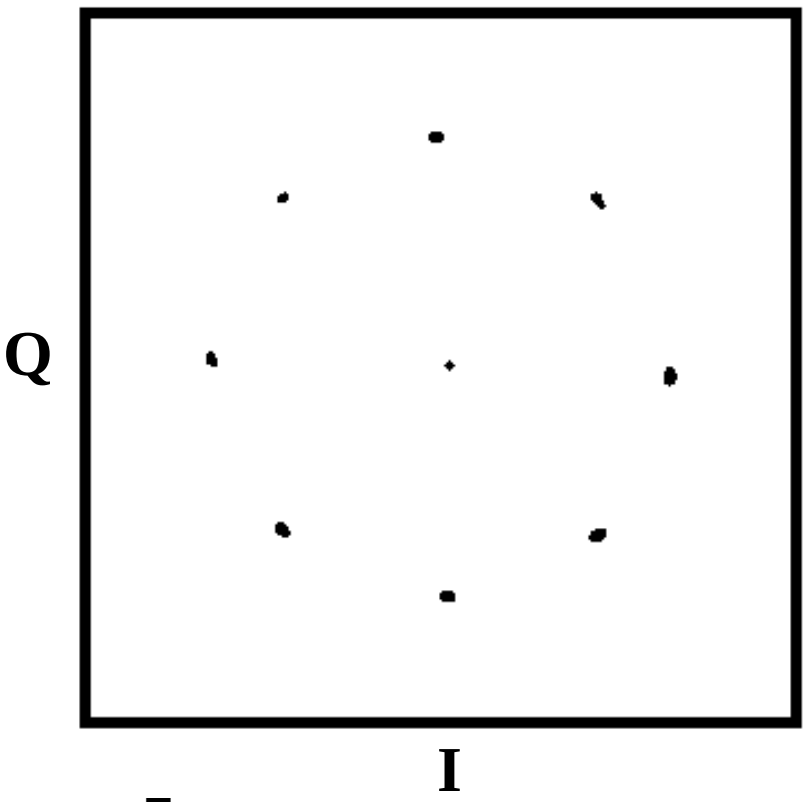
Receiver 2-Tone Intermodulation



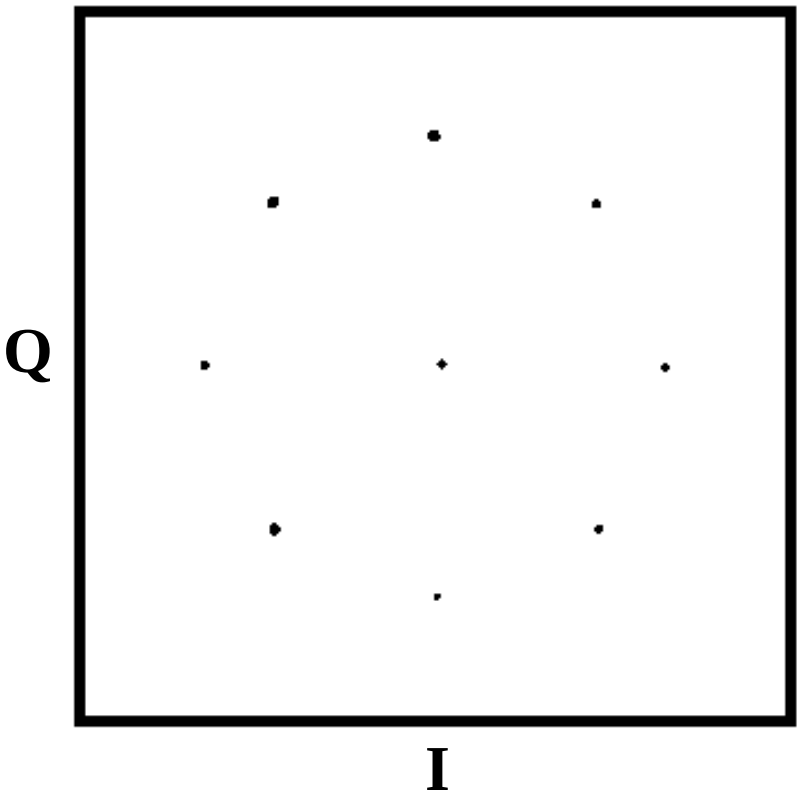
Transmit Spectrum



Transmitter Modulation Accuracy



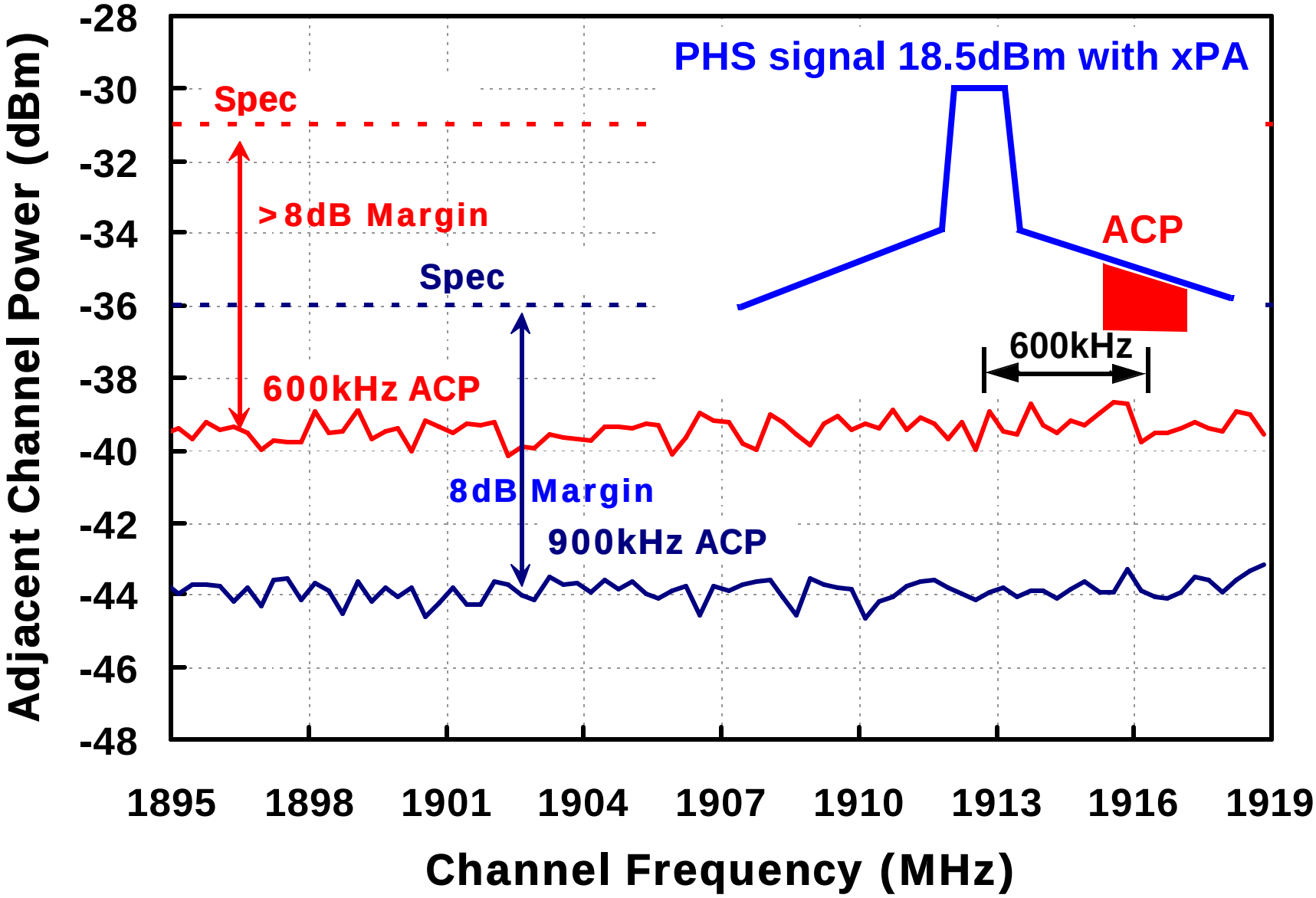
Frequency:
1 906.847 373 1 MHz
Frequency Error:
-2.626 9 kHz
RMS Vector Error: 3.80%
Peak Vector Error: 7.82%
Output Power: 0dBm



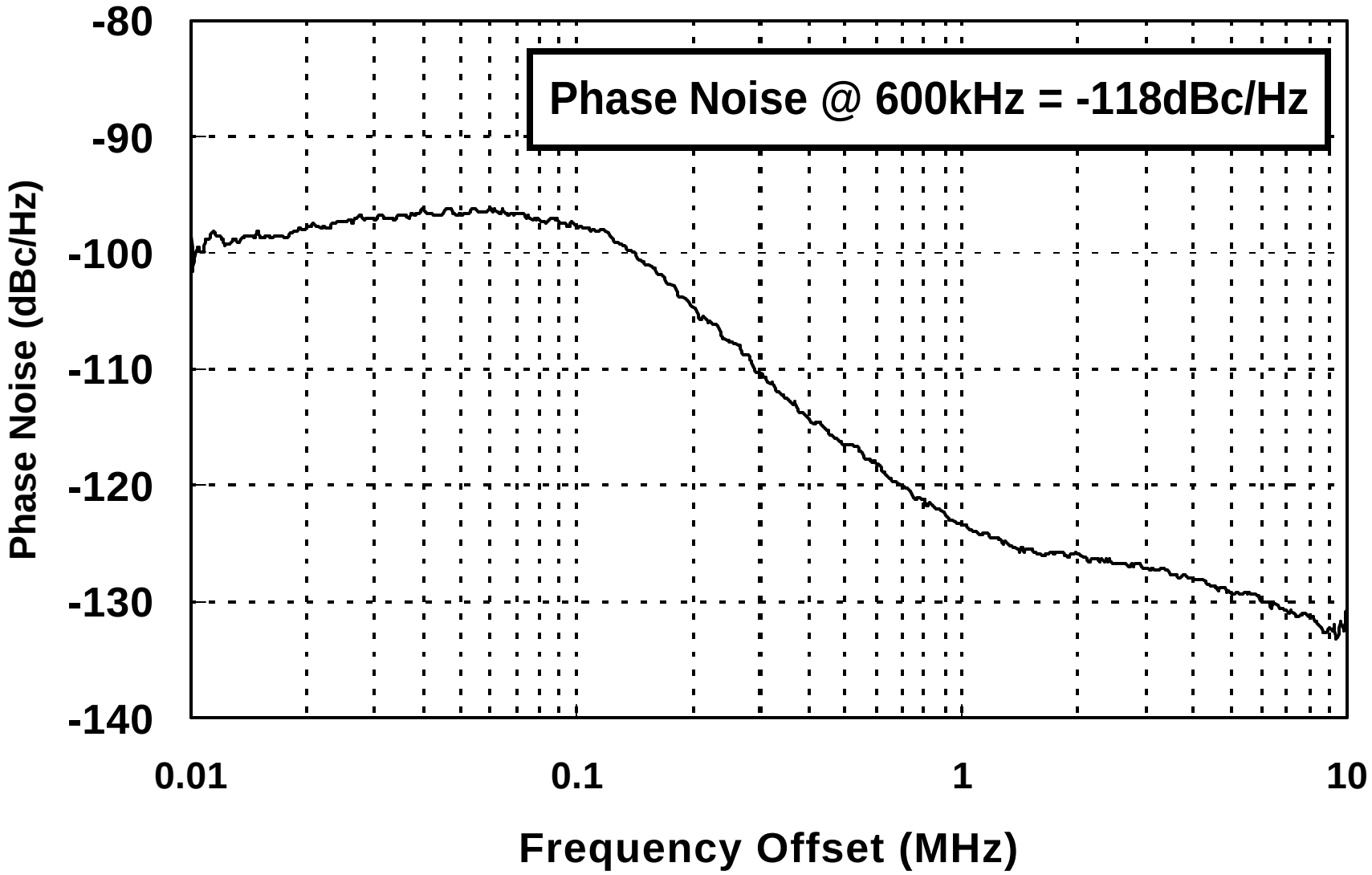
Frequency:
1 906.847 366 4 MHz
Frequency Error:
-2.633 6 kHz
RMS Vector Error: 1.03%
Peak Vector Error: 2.50%
Output Power: -10dBm

PHS Standard requires EVM less than 12.5%

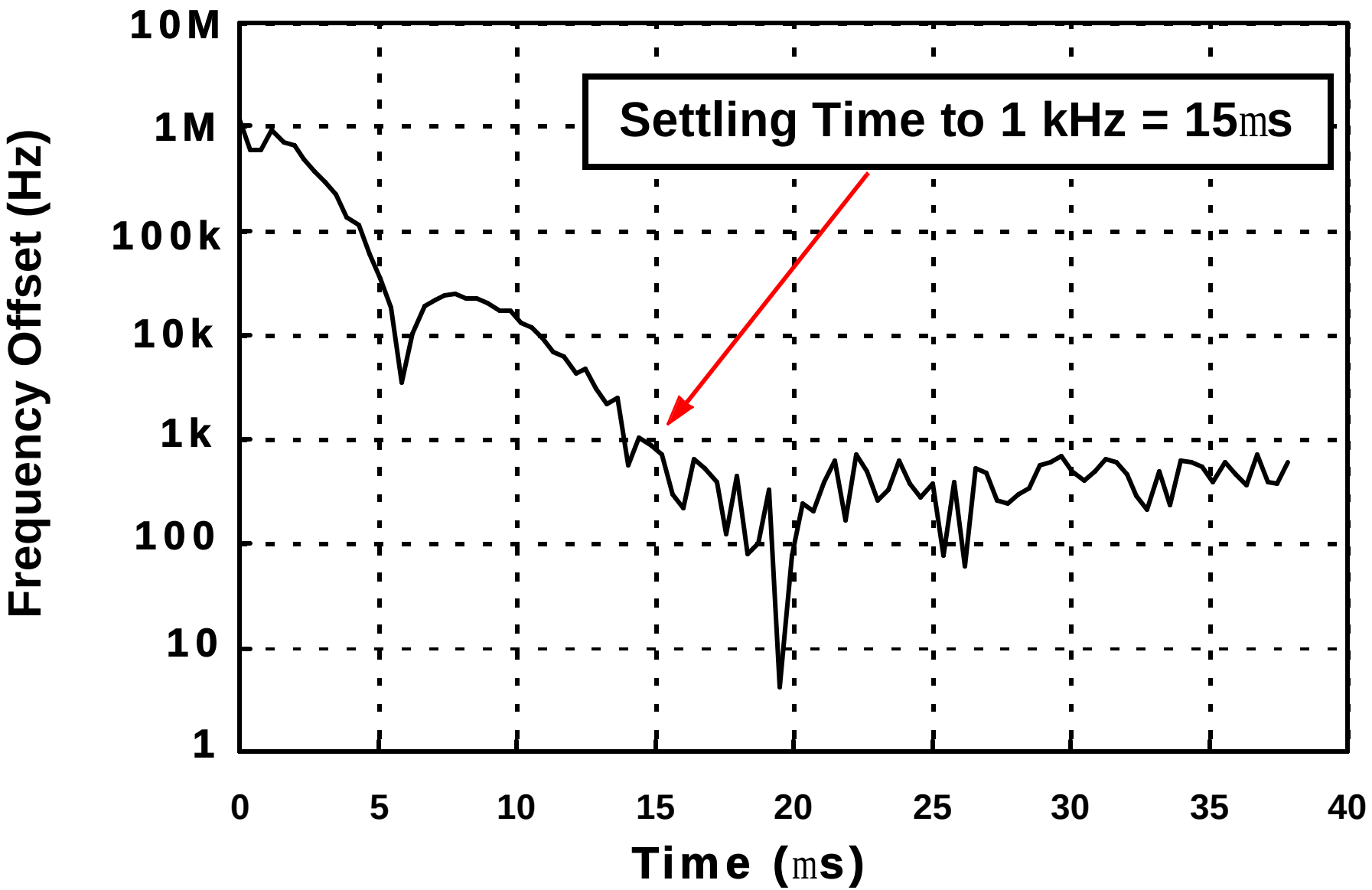
Transmit Adjacent Channel Power (ACP)



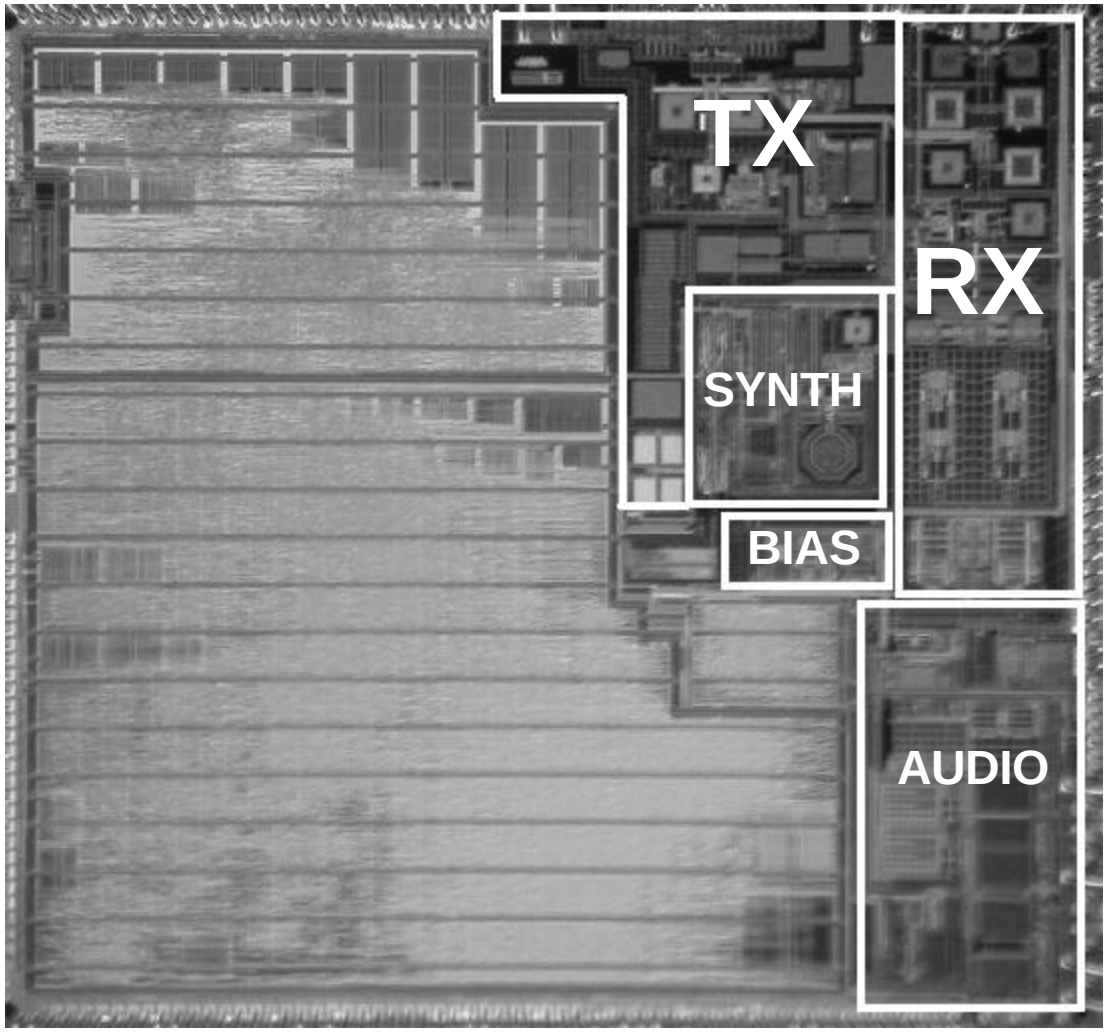
Synthesizer Phase Noise at 1895.15MHz



Measured Synthesizer Settling Time



Die Micrograph



Performance Summary

Power Dissipation **RF Transmitter** **RF Receiver** **RF Synthesizer** **Talk Mode (1/8 duty cycle Tx & Rx)** **Standby Mode**	 **29mA** **32mA** **25mA** **81mA (including audio and digital)** **1mA (including audio and digital)**
Phase Noise @ 1.9GHz	**-118dBc/Hz @ 600kHz offset**
Settling time to +/- 1kHz	**15μs**
Receive Sensitivity	**-106dBm**
Receiver Noise Figure	**3.5dB**
Transmit Power (EVM compliant)	**+4 dBm**
Transmit EVM	**4% rms @ 1dBm** **1% rms @ -10dBm**
Technology	**Standard 0.18μm CMOS**
Supply Voltage	**3.0V with internally regulated 1.8V**
Die Size: Total **RF and Analog**	**33 mm^2** **12 mm^2**
Package	**276-pin BGA**

Conclusions

- **Demonstrated single-chip PHS cellphone in 0.18 μm standard digital CMOS**
- **SoC performance meets or exceeds all PHS specifications**
- **System on a single chip allows for digital calibration to ease requirements of analog circuits**

Acknowledgments

The authors wish to acknowledge the contributions from the entire PHS team at Atheros, especially their efforts in algorithm development, digital design, and system design and verification