An 802.11a/b/g SoC for Embedded WLAN Applications

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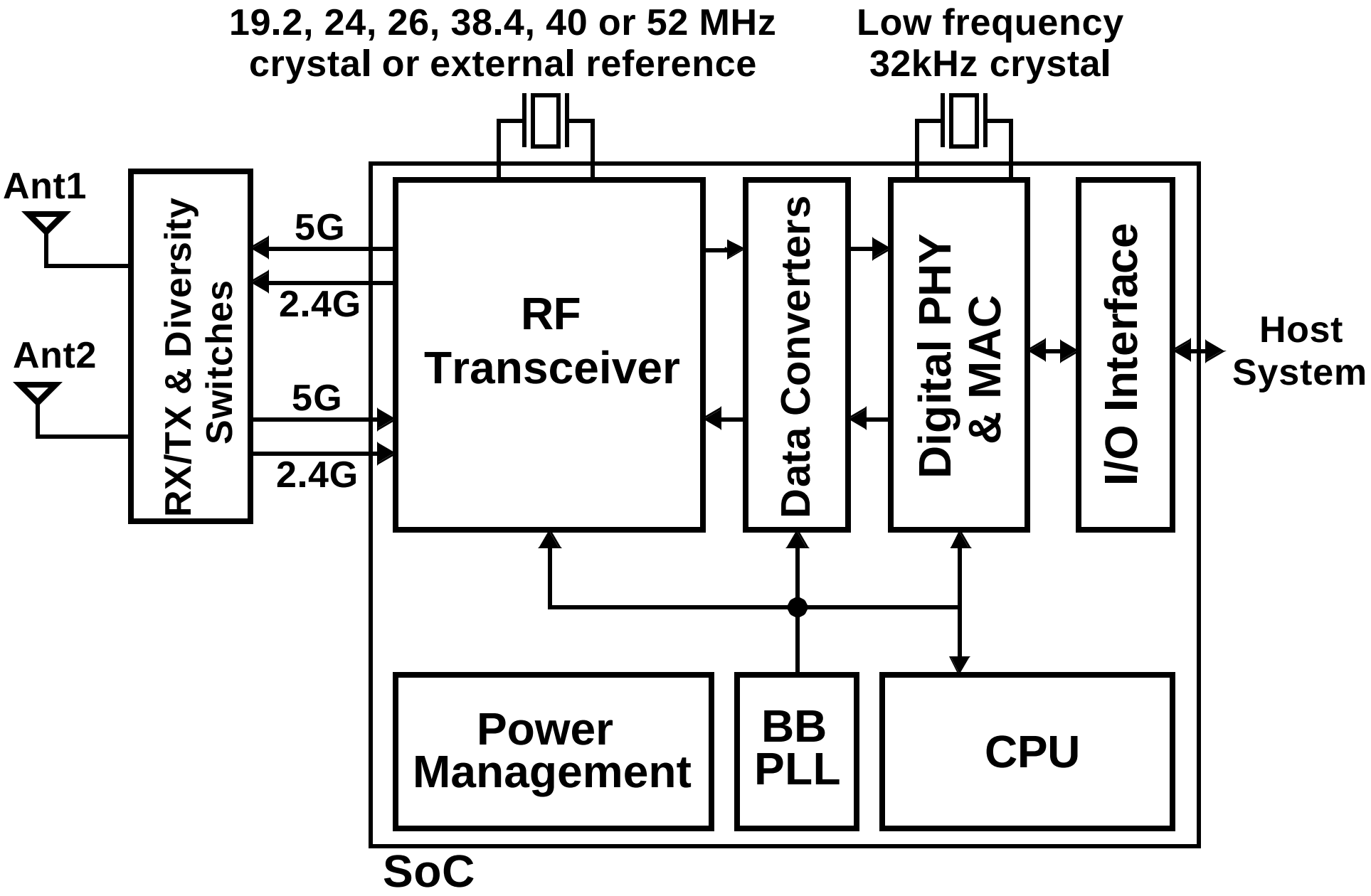
Outline

- **Introduction**
  - ⇒ **Embedded WLAN applications**
- **SoC block diagram**
- **Power management**
- **Transceiver architecture**
  - ⇒ **5GHz/2.4GHz transmitter**
  - ⇒ **5GHz/2.4GHz receiver including ADC**
  - ⇒ **Frequency synthesizer**
- **Measurement results**

Embedded WLAN

- **Applications: Wi-Fi phones, digital cameras, networked gaming, PDAs, MP3 players, etc.**
  - $\Rightarrow$ **Long battery life $\rightarrow$ low sleep/standby power**
  - $\Rightarrow$ **Small form-factor $\rightarrow$ single chip integration**
- **Support for wide range of crystal frequencies**
  - $\Rightarrow$ **Share crystal oscillator with host system**
- **Support for common I/O interfaces**
  - $\Rightarrow$ **SDIO, SPI, CF, etc.**
- **Dual-band operation at 2.4GHz and 5GHz**

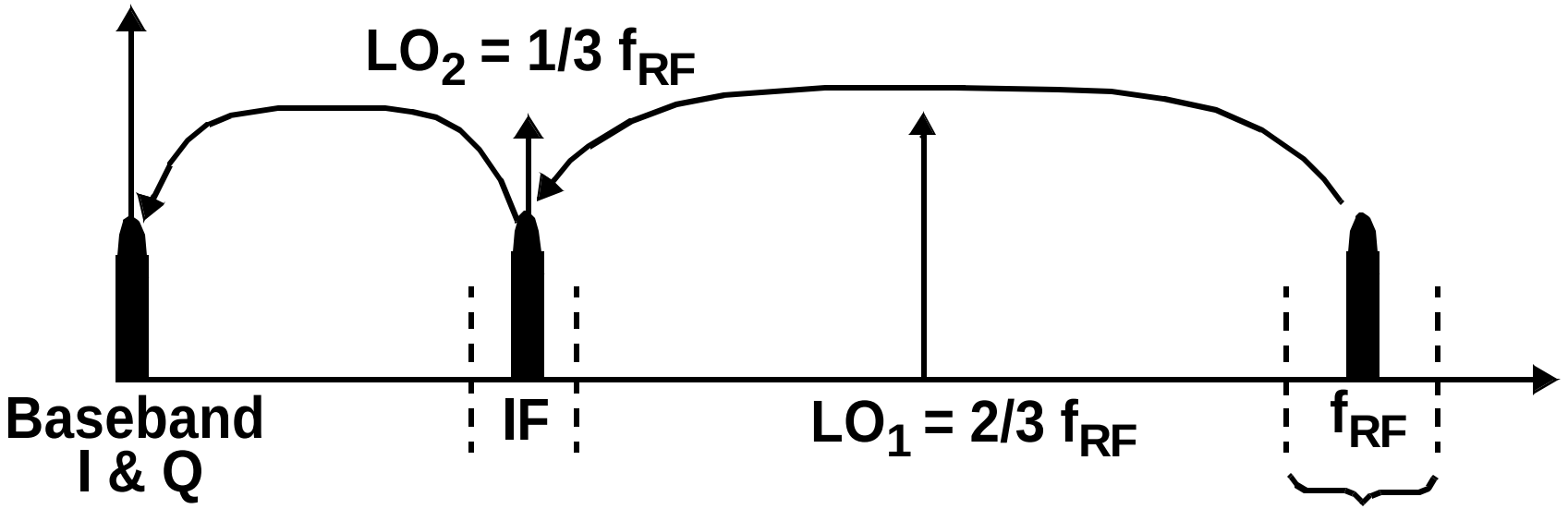
SoC Block Diagram



Power Management

- **Operating modes: Sleep, Standby, RX, TX**
- **Programmable LDO regulators used to lower the supply voltage in sleep mode**
  - ⇒ **All register states maintained.**
  - ⇒ **Reduced supply leakage current**
- **Standby power depends on RX duty cycle**
  - ⇒ **Reduce power by staggering the power-on of analog blocks based on settling time.**
  - ⇒ **Gate clock signals to inactive digital circuits**
  - ⇒ **Run off of the 32kHz clock when idle**

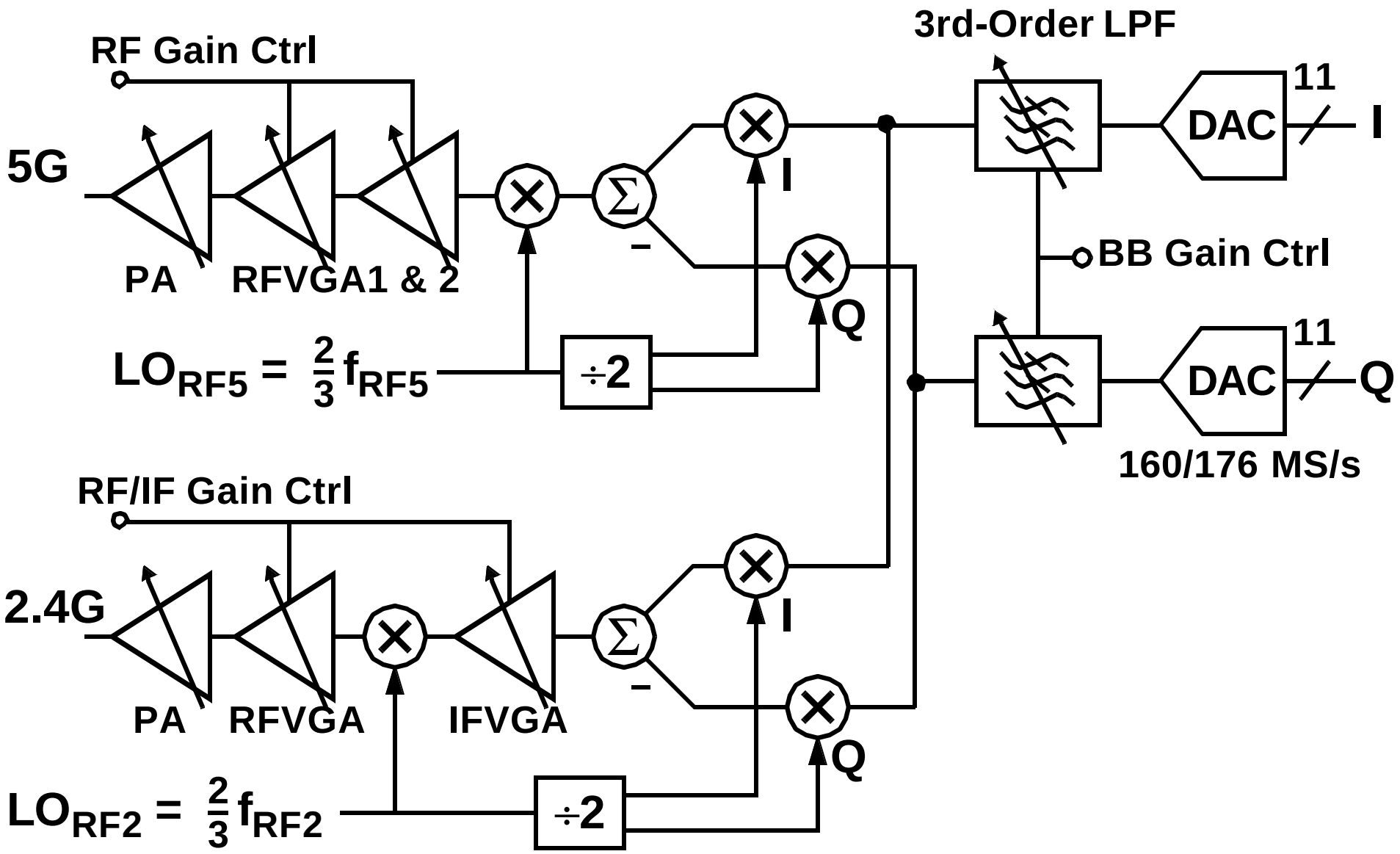
Sliding-IF Architecture



5GHz Band: 4.9 - 5.925 GHz
2.4GHz Band: 2.412 - 2.484 GHz

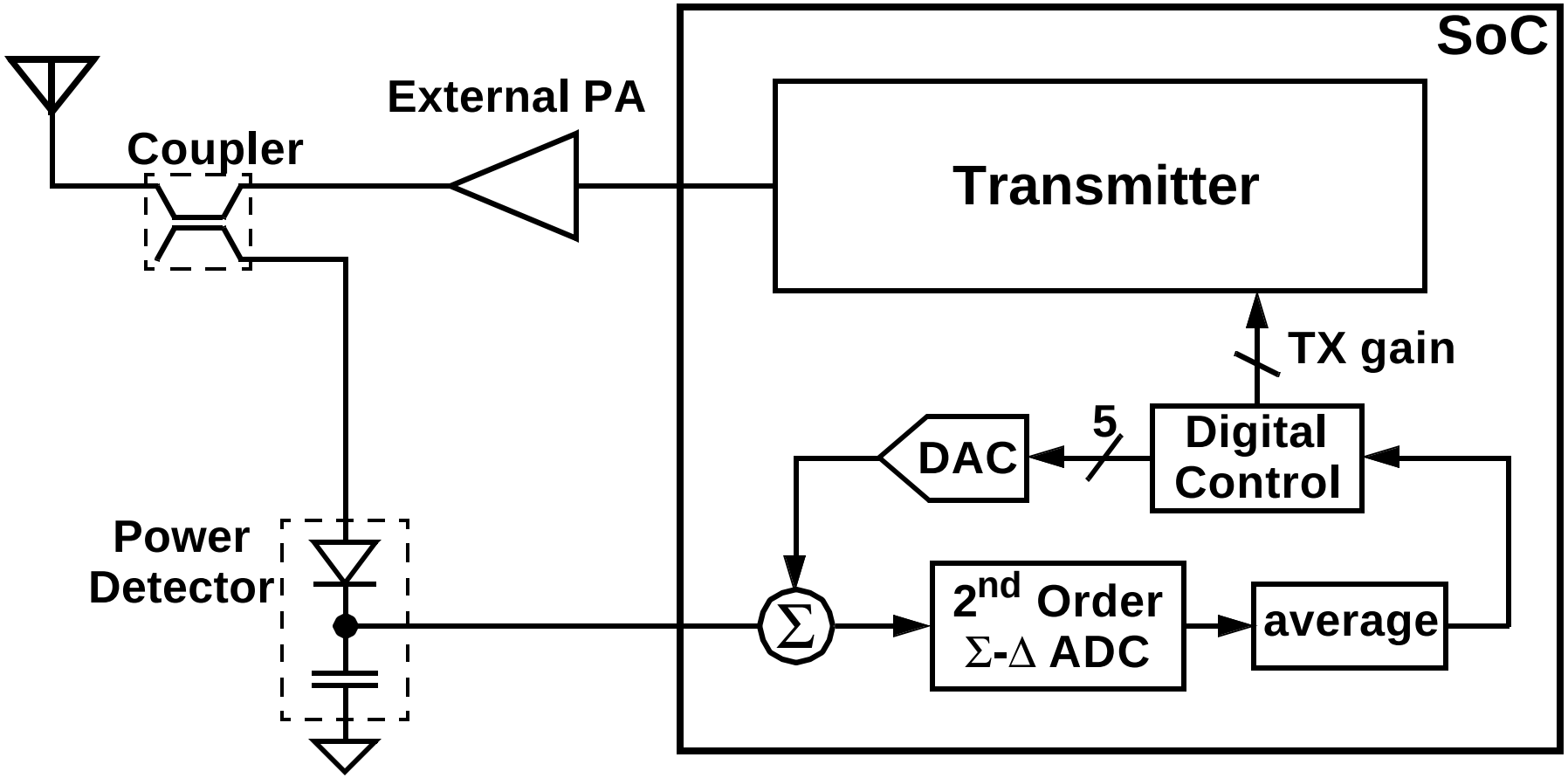
- **Only one synthesizer needed to generate LO frequencies**
- **$f_{VCO} = 2/3\ f_{RF5}, 4/3\ f_{RF2} \rightarrow$ No LO Pulling**

Dual-Band Transmitter

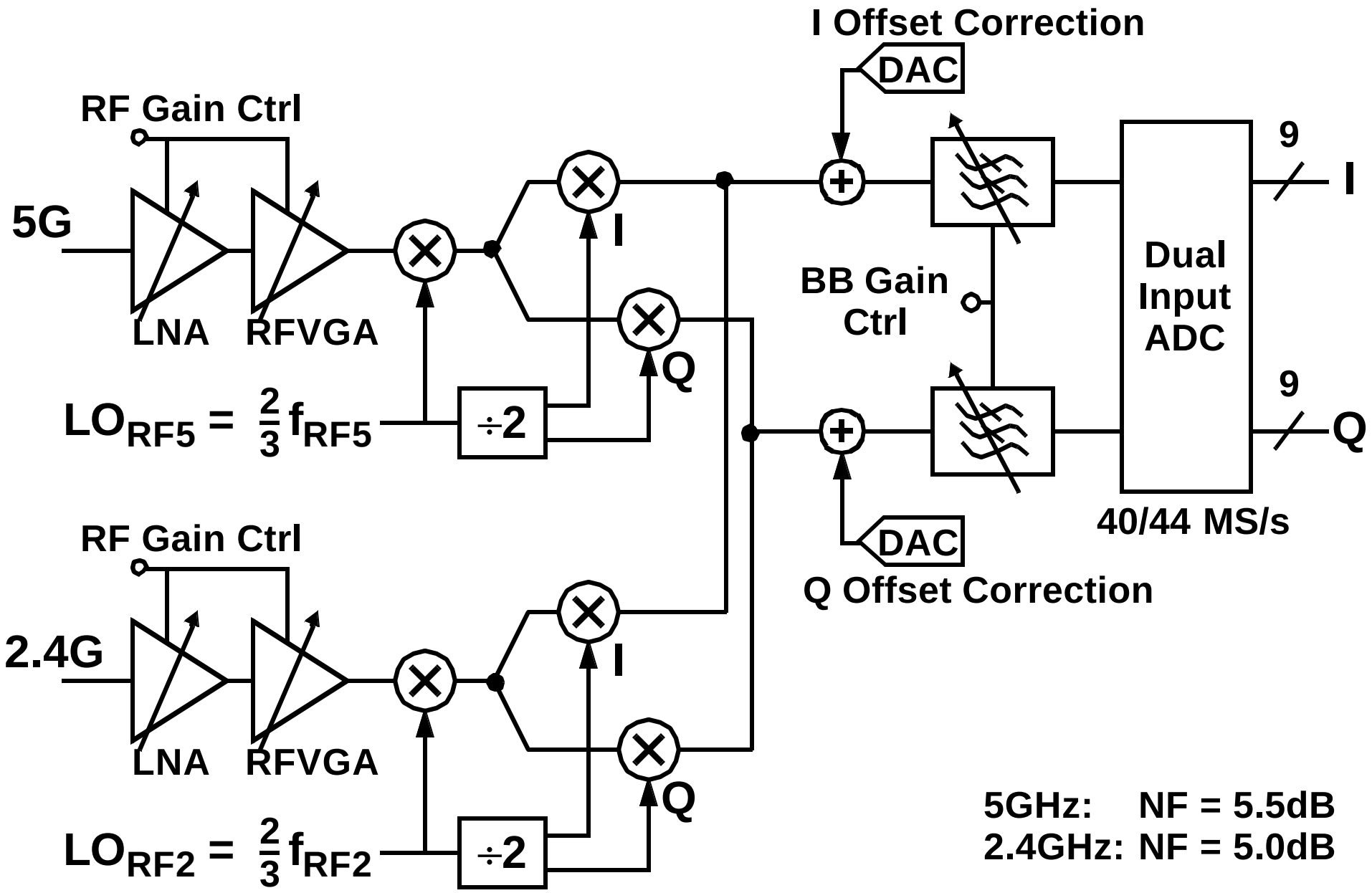


Transmit Power Control

- 5b DAC to correct power detector DC offset
- TX gain adjusted on a per packet basis

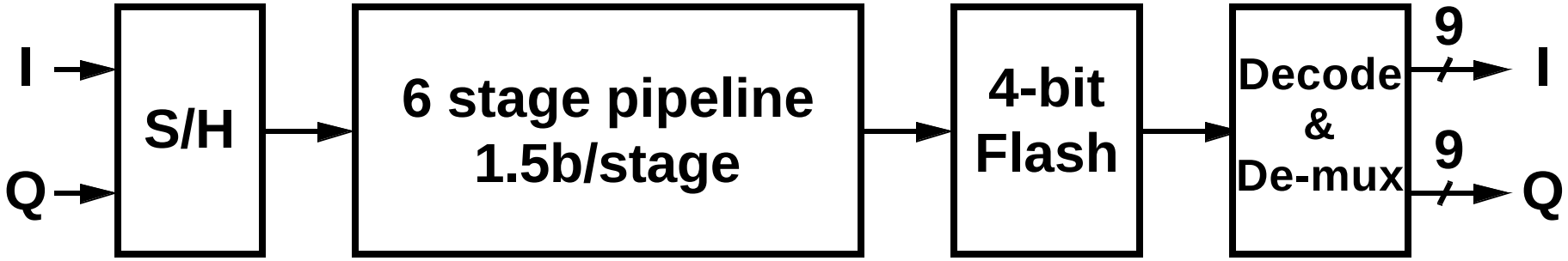


Dual-Band Receiver



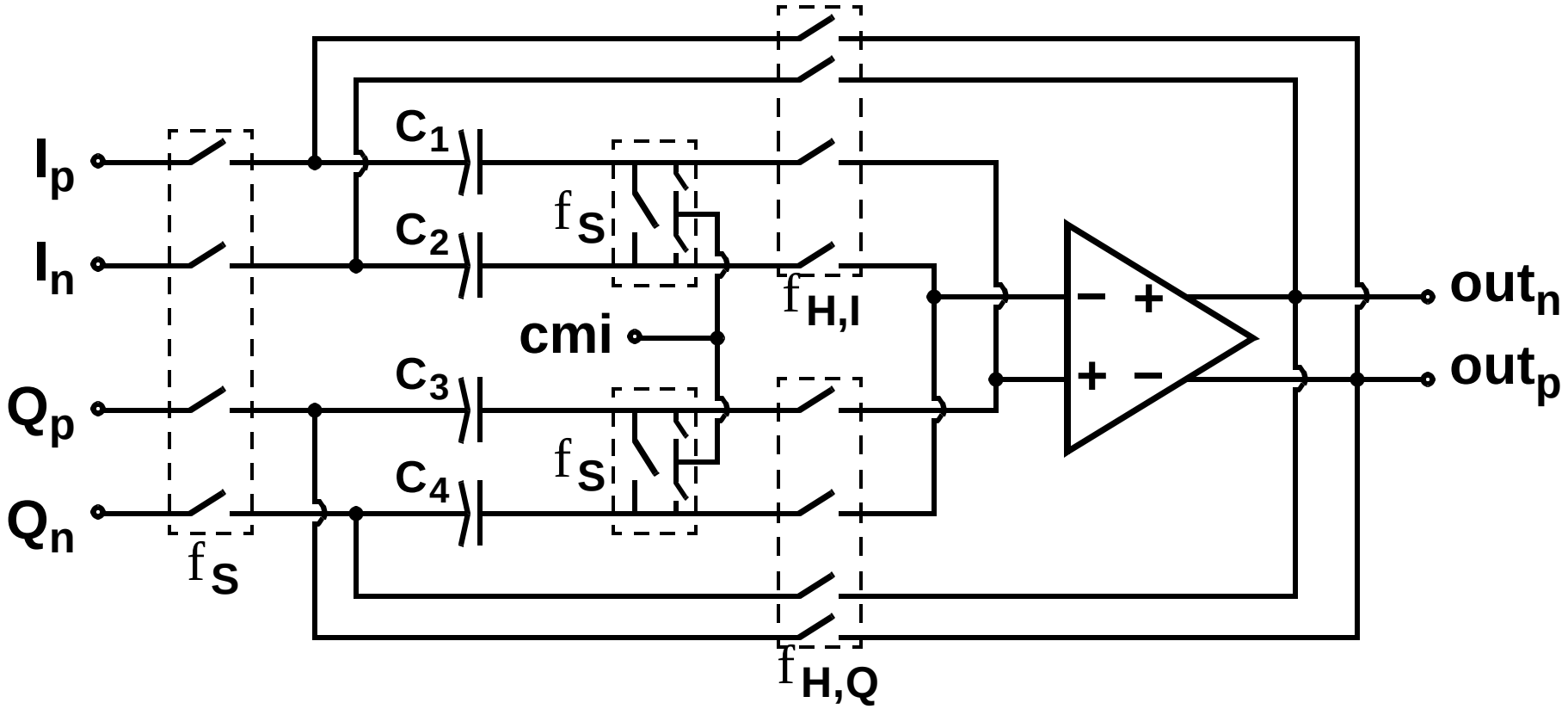
5GHz: NF = 5.5dB
2.4GHz: NF = 5.0dB

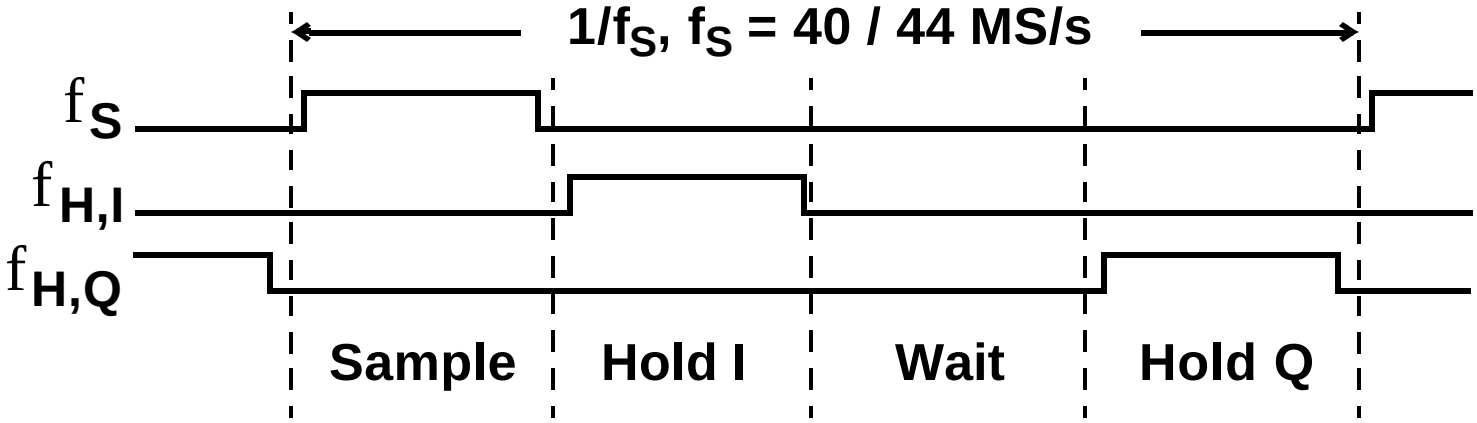
Dual-Input A/D Converter



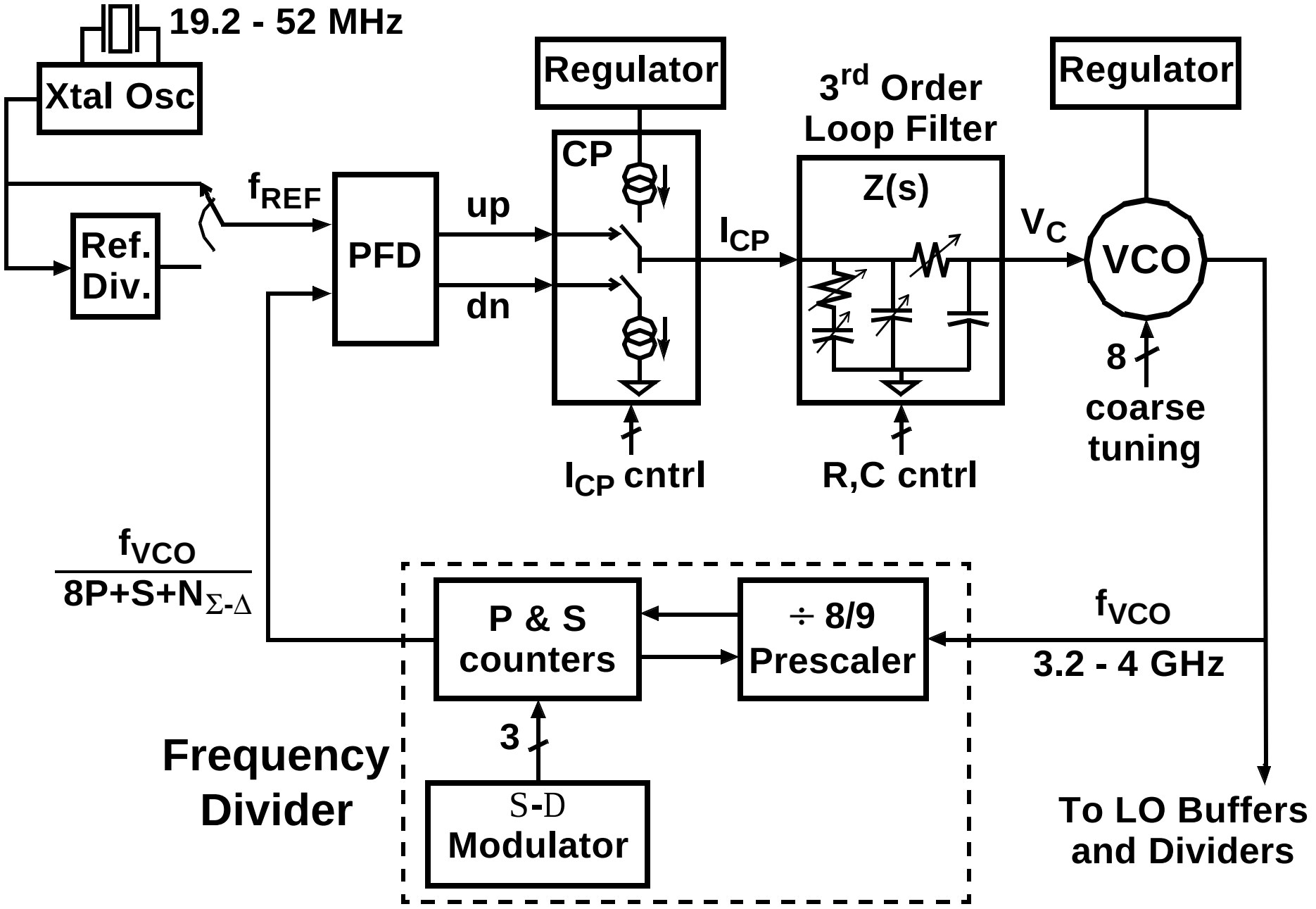
- **Time-multiplexed pipeline architecture**
  - ⇒ **I & Q inputs are sampled simultaneously**
  - ⇒ **Pipeline stages run at 80/88 MHz ($2 \times f_S$)**
- **Almost half the area and similar power as 2 non-multiplexed ADC's**
  - ⇒ **Area: 0.45mm x 1.0mm, Power: 48mW**

ADC Sample/Hold Circuit

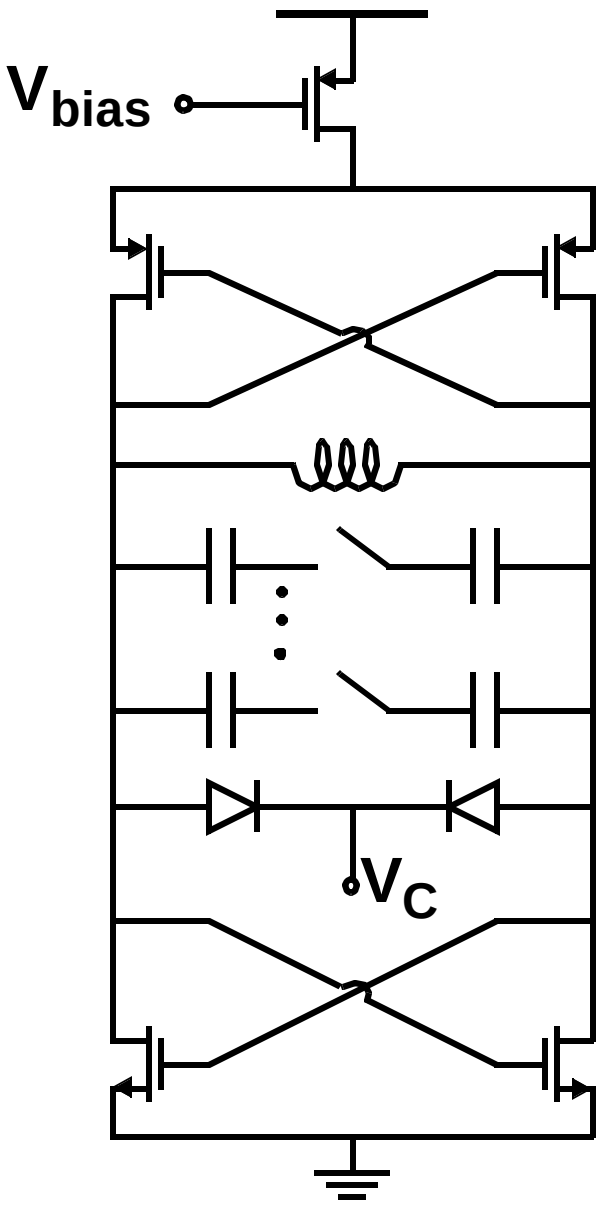




Fractional-N Synthesizer



CMOS LC-tank VCO



- **Tuning range: 3.2 - 4 GHz**
  - ⇒ **8-bit switch-capacitor bank for coarse tuning**
  - ⇒ **diode varactor for continuous fine tuning**
- **Voltage-to-freq. gain:**

$$K_{VCO} = 2\pi^2 L \times f_{VCO}^3 \times \frac{\partial C}{\partial V_C}$$

- **Large variation in K_{VCO}:**
  K_{VCO} = 34MHz/V @3.2GHz
  K_{VCO} = 66MHz/V @4GHz

Synthesizer Design

- **Loop Gain =** $\frac{I_{CP} \cdot Z(s) \cdot K_{VCO}}{s \cdot N_{div}}$**, where** $N_{div} = \frac{f_{VCO}}{f_{REF}}$

  ⇒ **I_{CP} is digitally varied as $1/f_{VCO}^2$ for constant loop gain over tuning range.**

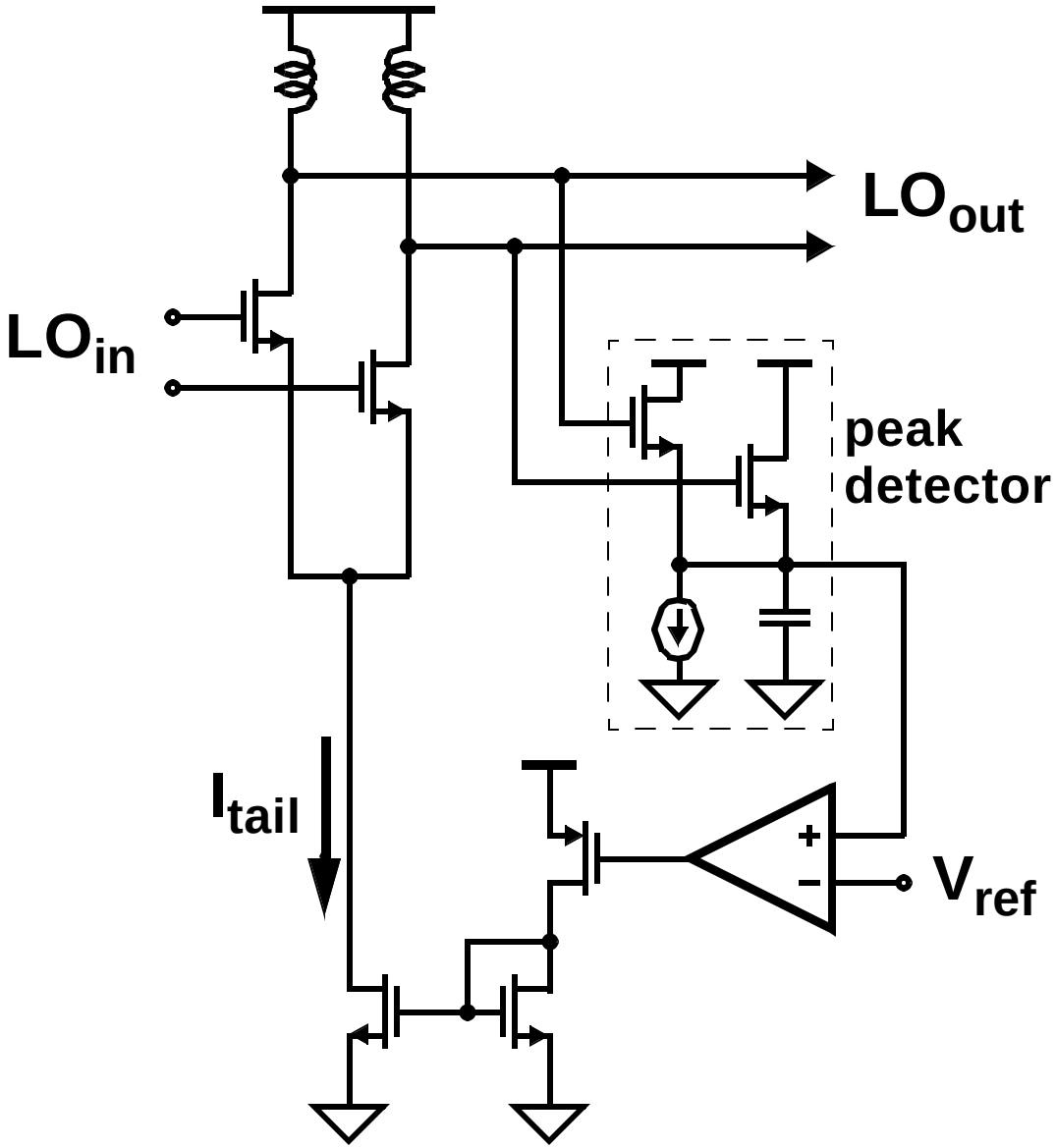
- **On-chip programmable loop filter, Z(s)**

  ⇒ **Program for 50° PM with given f_{REF}**

  ⇒ **Optimize loop BW for low integrated PN**

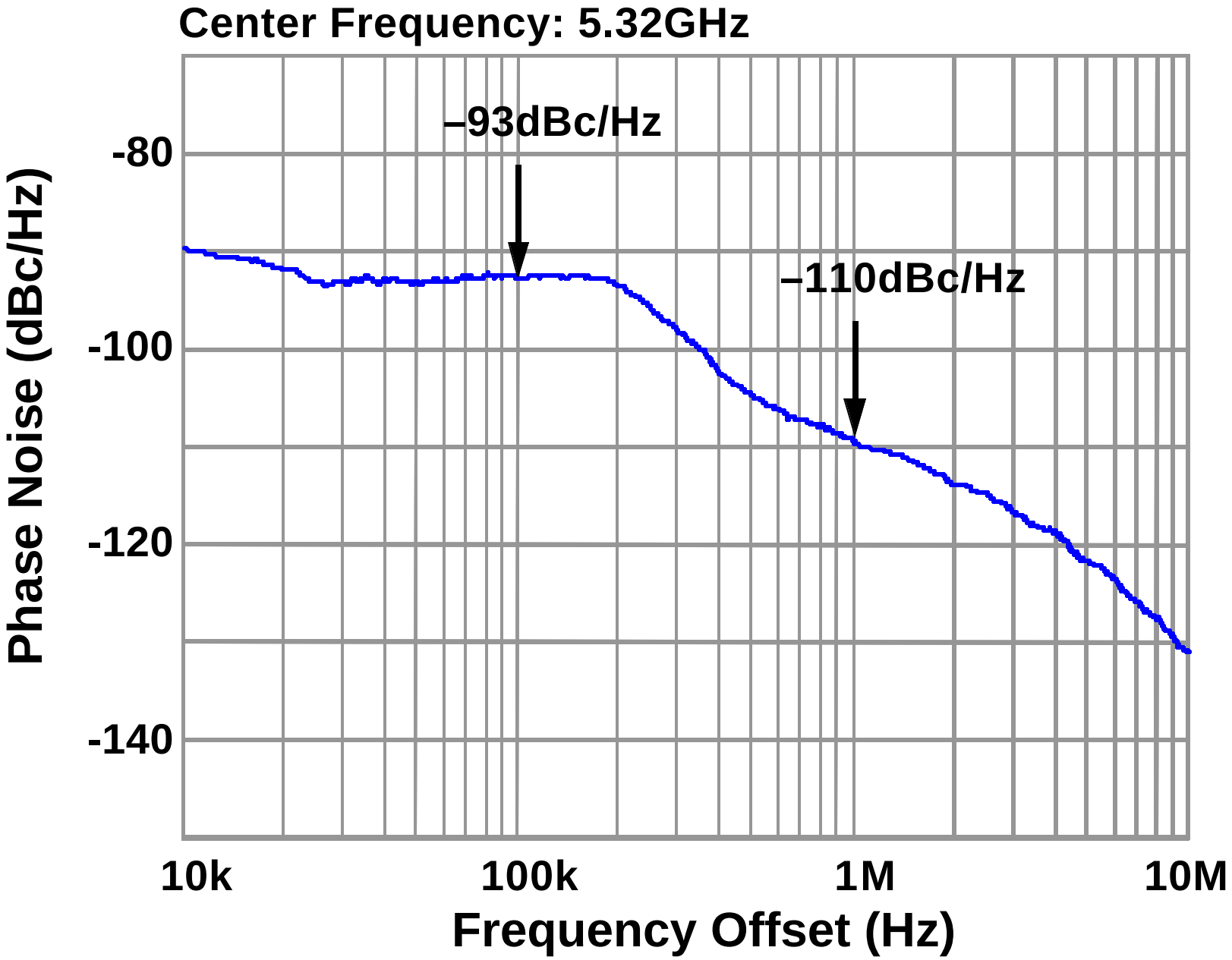
  ⇒ **For stability, 3rd pole of Z(s) >> loop BW.**

LO Buffer with AGC

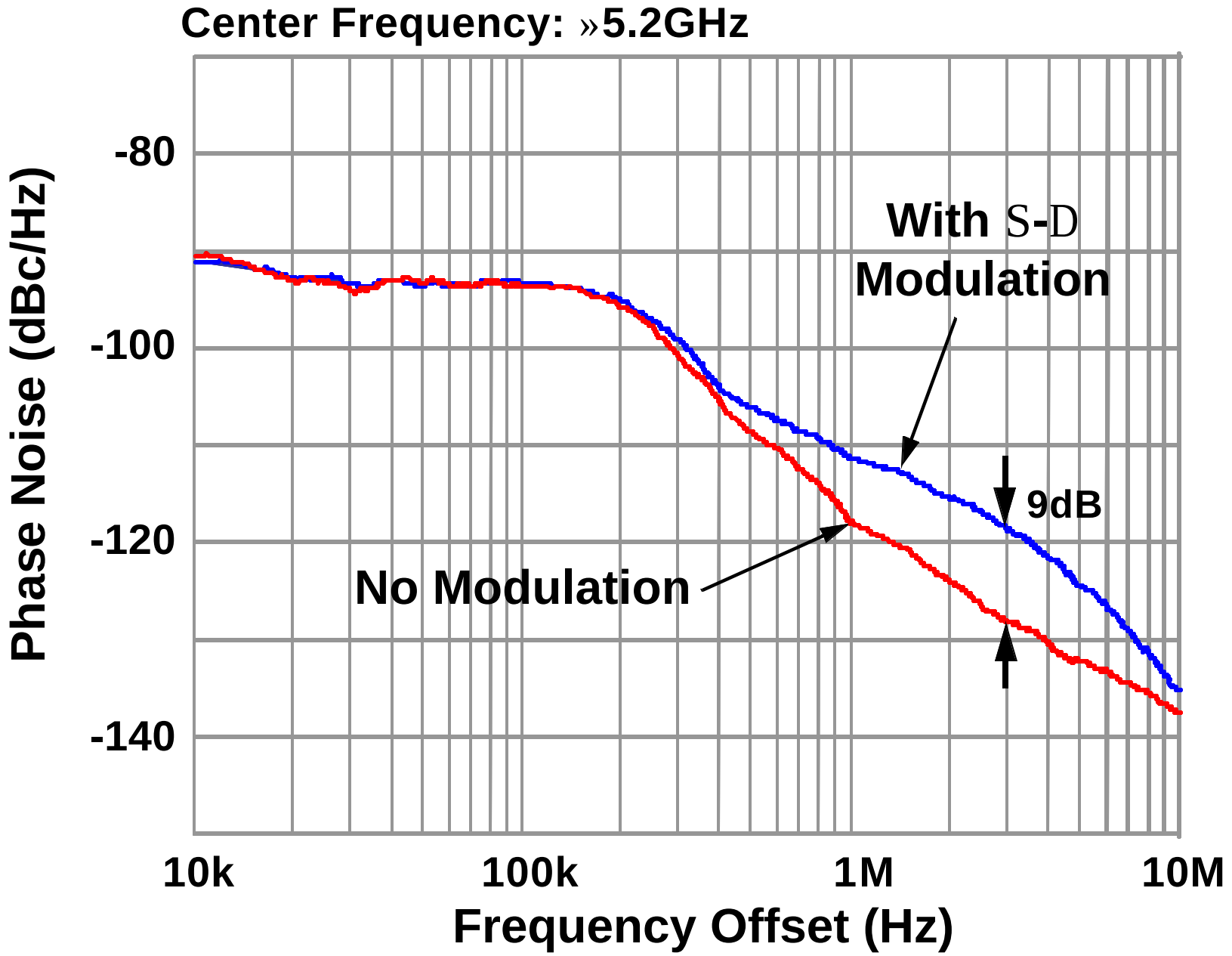


- Inductively-tuned
- $3.2GHz < LO_{RF5} < 4GHz$
- Desire an LO amplitude $\gg 1V_{diff}$
- Use AGC to minimize bias current
  - $\Rightarrow$ $3.5mA < I_{tail} < 12mA$ over P.V.T. & freq.

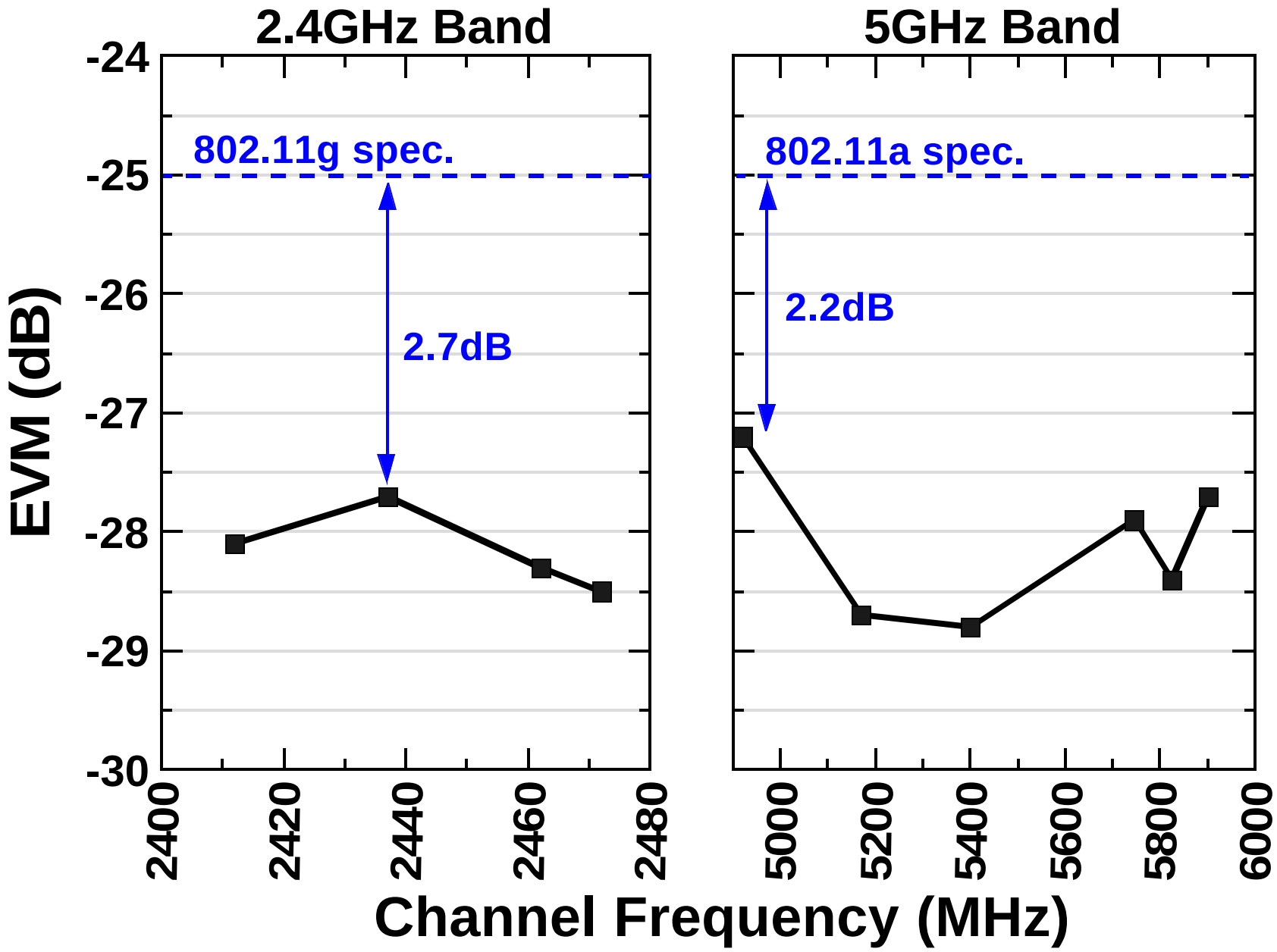
5GHz TX Phase Noise



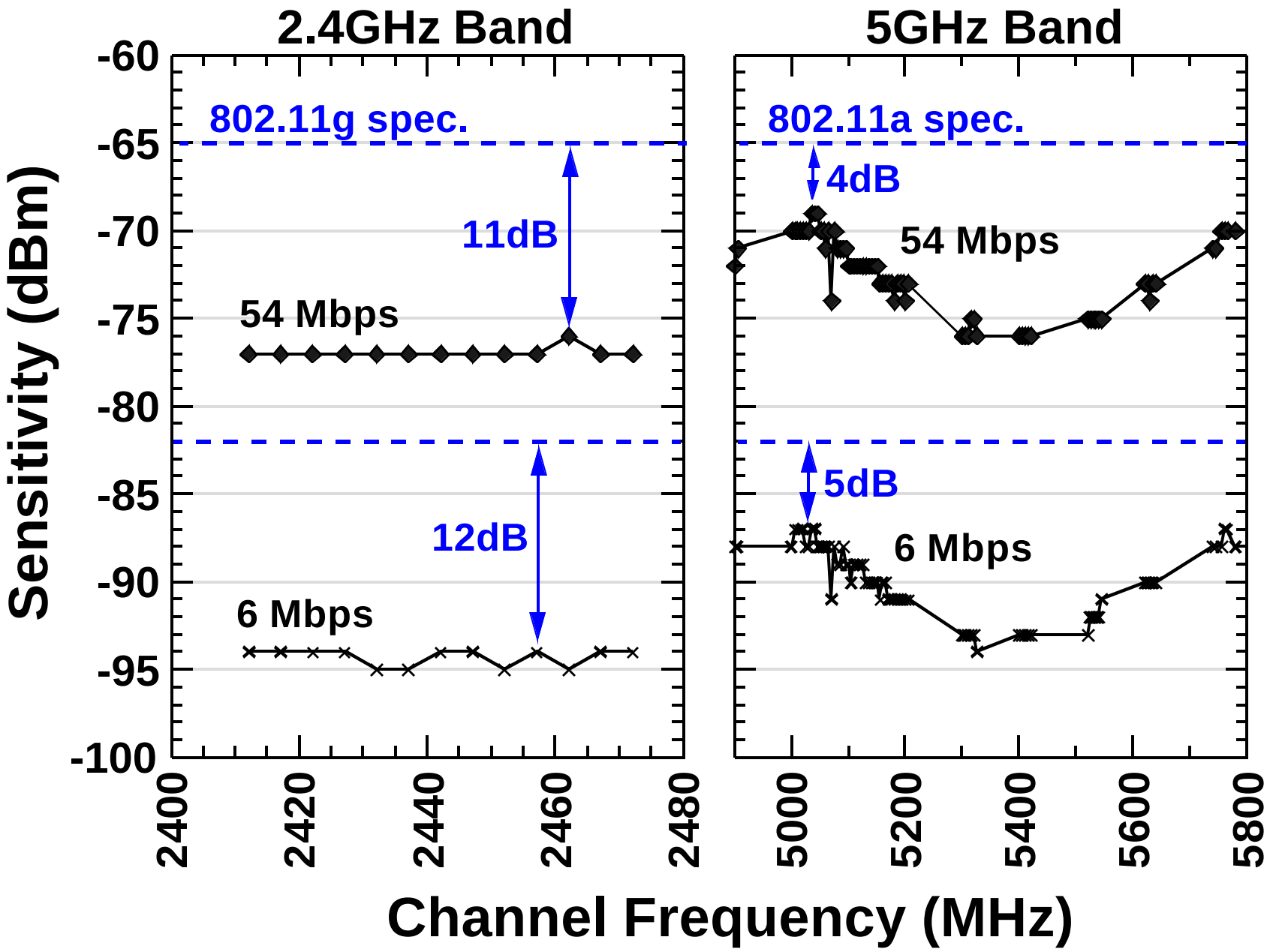
S-D Modulator Noise Contribution



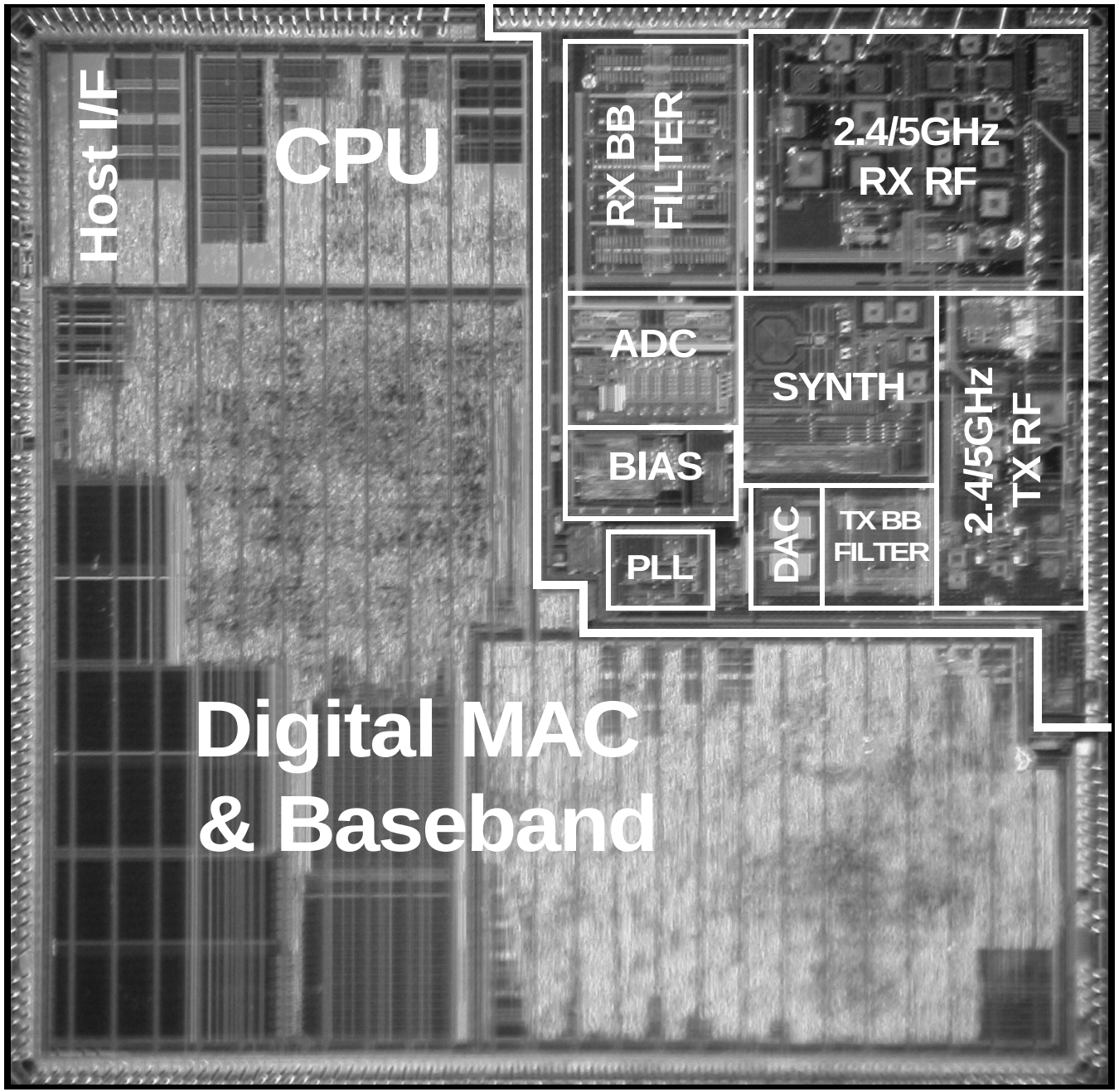
Transmit EVM @P_{out} » –4dBm



Receiver Sensitivity



Die Photo



- **Process: 0.18㎜m CMOS with 3V I/O**
- **Die Size: 6.6 ´ 6.7 mm^2**
- **Analog Area: 13.5 mm^2**
- **Packages: 216-pin BGA or CSP**

Performance Summary

Parameter	2.4GHz Band	5GHz Band
Transmit EVM at 54Mbps	-27.5dB@-3.5dBm	-28dB@-4dBm
Receiver Sensitivity for 6Mbps for 54Mbps	-94dBm -76dBm	-91dBm -73dBm
Receiver Noise Figure	5.0dB	5.5dB
SoC Power Dissipation RX mode TX mode (P_{out}=-4dBm)	 424mW 380mW	 398mW 425mW
RF Transceiver Power RX (excl. ADC) TX (P_{out}=-4dBm, excl. DACs)	 287mW 272mW	 267mW 310mW
Sleep Power Dissipation	< 300㎼W	
Technology	Standard 0.18㎛ CMOS w/ 3V I/O	
Die Area (analog area)	44.6 (13.5) sq. mm	

Conclusions

- **Demonstrated a single-chip IEEE 802.11a/b/g SoC suitable for embedded WLAN**
- **Receiver sensitivity of -76dBm and -73dBm at 54Mbps for 2.4GHz and 5GHz, respectively**
- **Fractional-N frequency synthesis allows operation with a range of crystal frequencies**
- **Power management features reduce sleep and standby current**

Acknowledgements

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