A Pulse-Based CMOS Ultra-Wideband Transmitter for WPANs

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03/20/2008

Outline

- Motivation (Why UWB?)
- FCC Emission Limits
- Antenna Characterization
- UWB Transmitter Design
- Wide Tuning-Range VCO Design
- Summary

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Motivation

- **Consumers demand indoor wireless connectivity**
- **Current WLAN/WPAN solutions insufficient**
  - 802.11a/g→ 54Mbps (WLAN)*
  - Bluetooth→ 3Mbps (WPAN)
- **High data-rate applications:**
  - Wireless USB (480Mbps)
  - Real time AV Streaming (HDTV), AV Conference

*w/o MIMO

Motivation Cont.'d

Shannon's Law: The theoretical maximum information rate of a channel in bits per second is

$$C = BW \cdot \left(1 + \log_2 SNR\right)$$

UWB can provide very high data rates at low transmit power levels compared to narrowband

Low SNR ⇨

- implement in low-cost CMOS
- Power Amplifier not required

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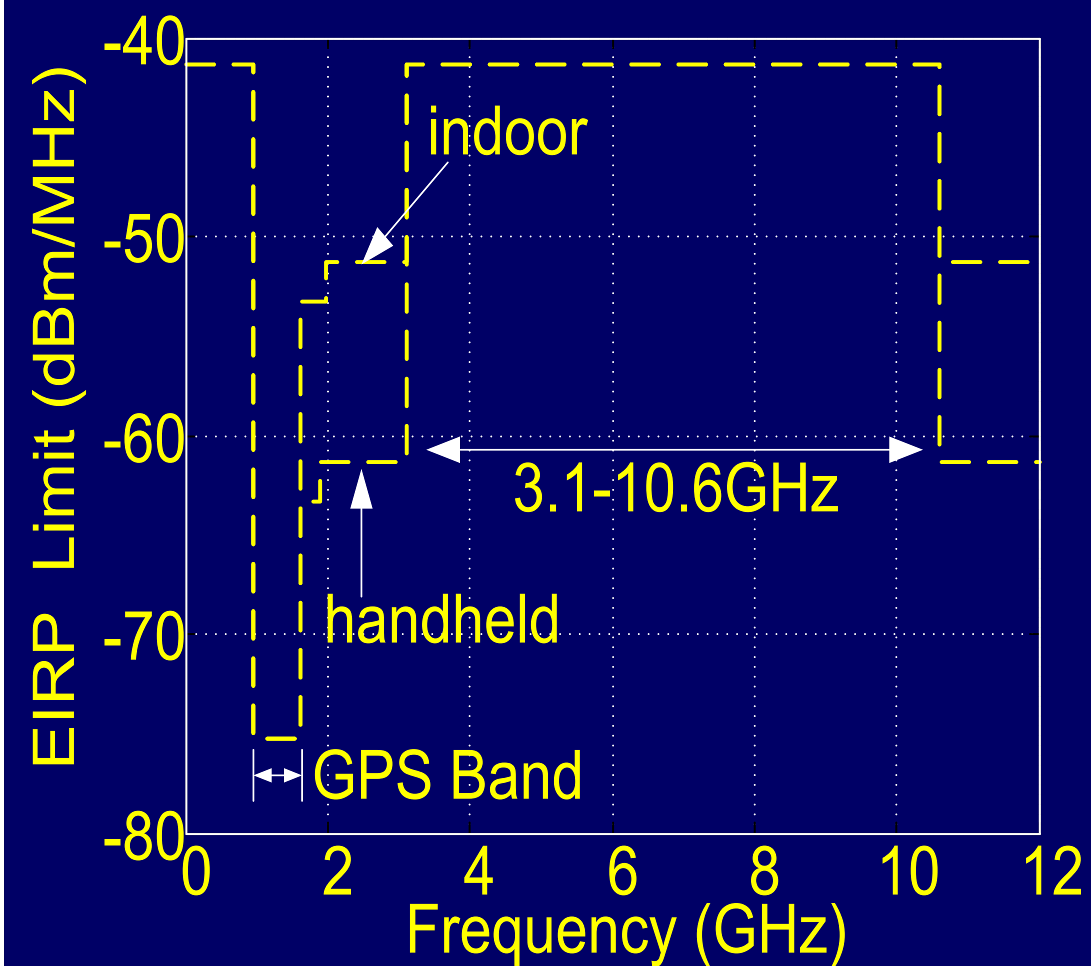
FCC Limits



FCC:

UWB device has

BW_{frac}>0.2 or BW>500MHz

$$BW_{frac} = \frac{2(f_H - f_L)}{f_H + f_L} = \frac{BW}{f_c}$$

Peak power limit:

0 dBm EIRP within 50 MHz of f_c

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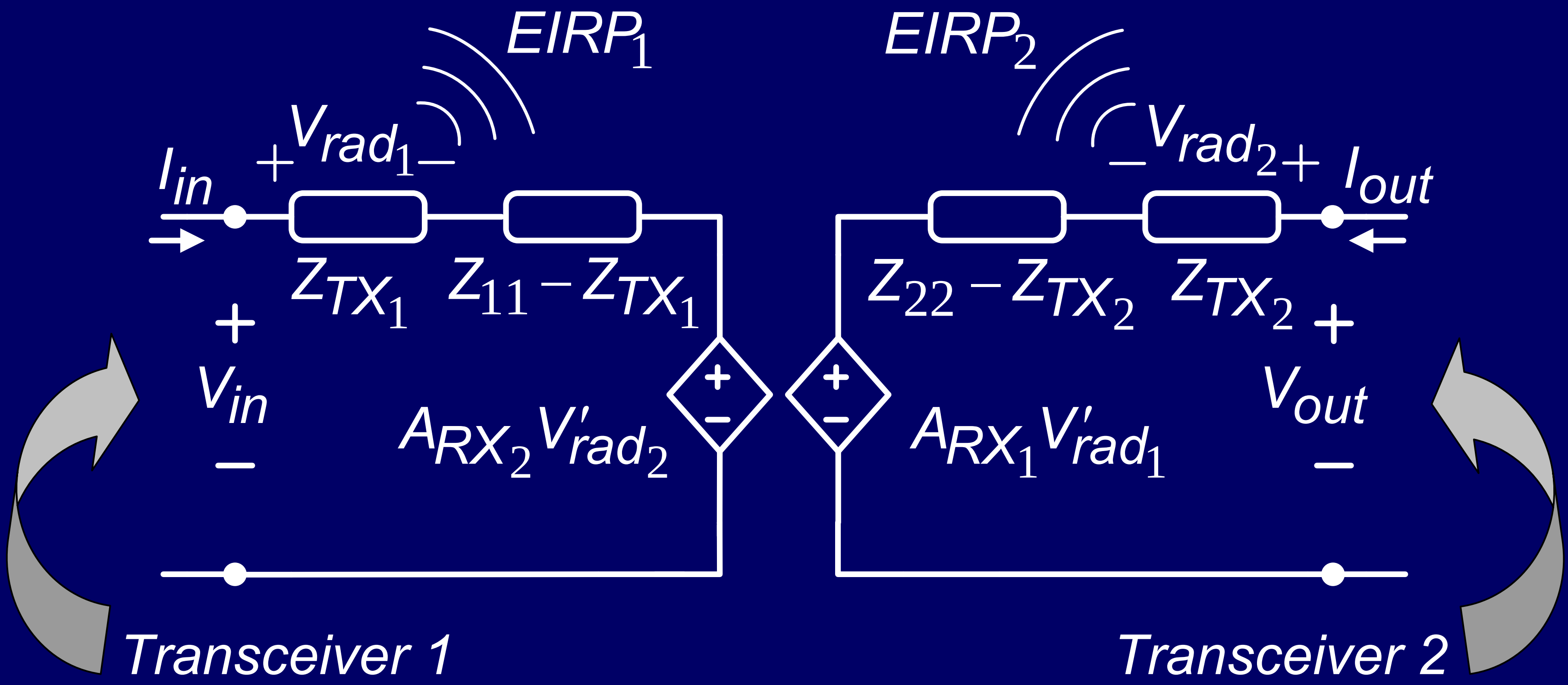
UWB Antenna Modeling

- Narrowband Antennas are frequency independent ($Z_{in}=Z_o$, Gain)
- UWB radios operate in 3.1-10.6GHz ($Z_{in}(\omega)$, $H(\omega)$)
  - Need to simulate EIRP before fabrication
  - Need a circuit-level model to facilitate design
  - Simple lumped models are NOT adequate

Modeling UWB Antennas



Bilateral equivalent circuit model for the 2-antenna network.

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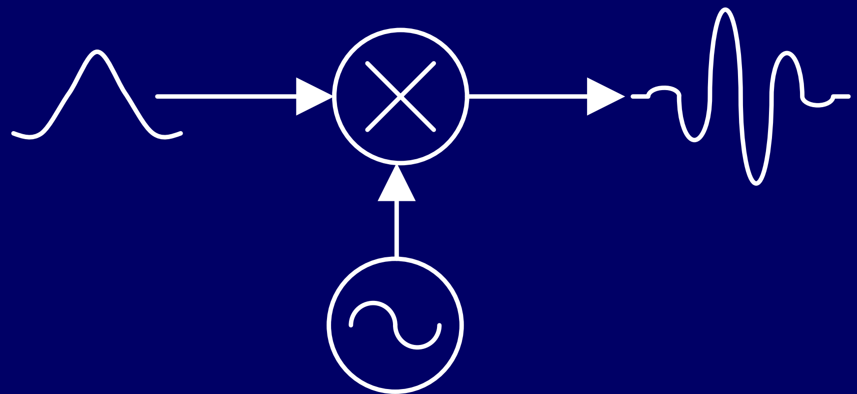
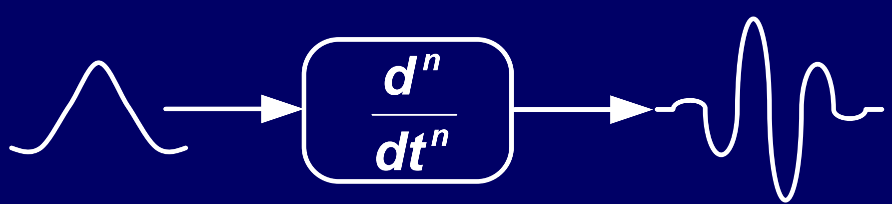
Pulse Generation Methods

Up-Conversion:



ISSCC 2005
[Iida et al.]

Filtering:

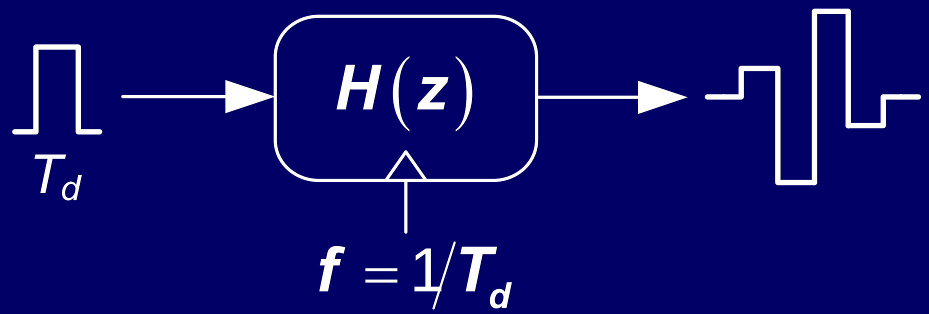


CT Filter

ISSCC 2006
[Zheng et al.]

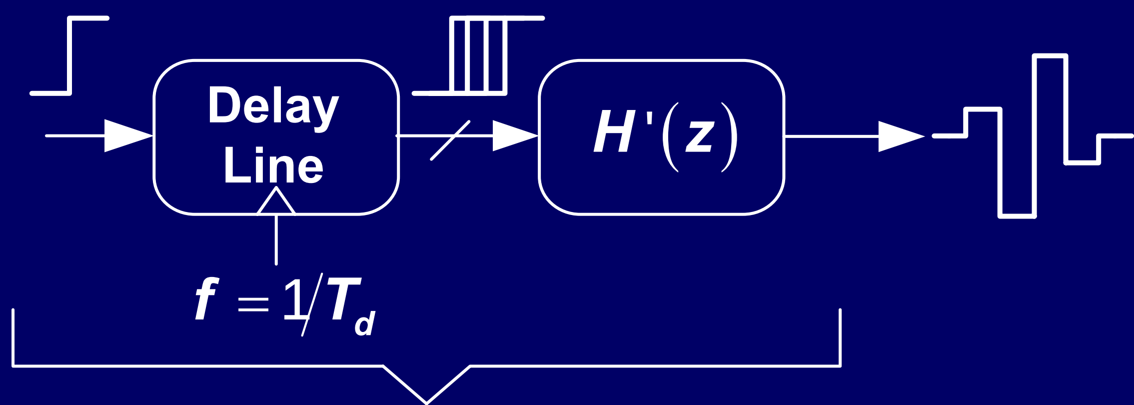
FIR Pulse Generator

DT-FIR Filter:



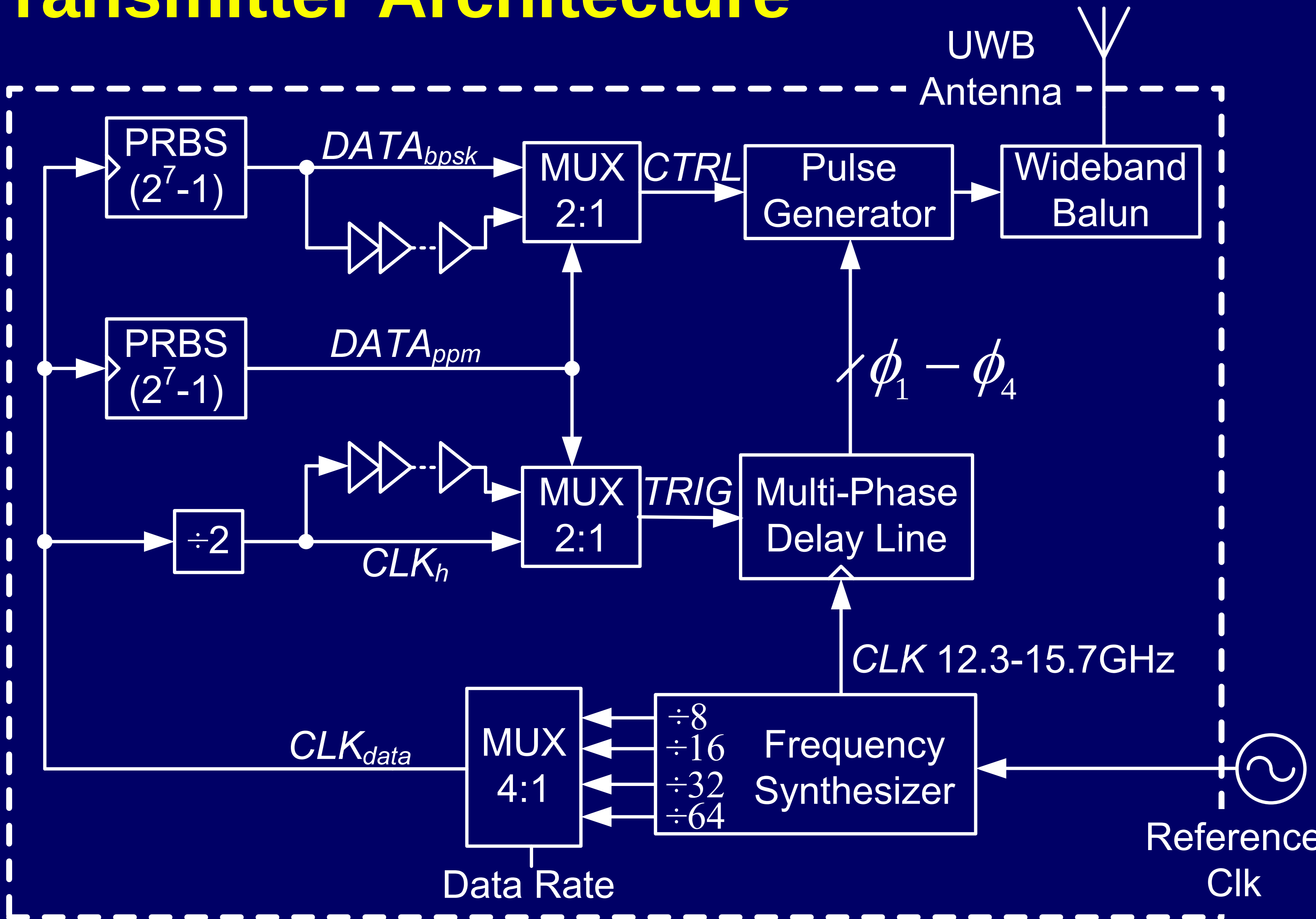
$$H(z) = (1 - z^{-1})^N$$

This work:

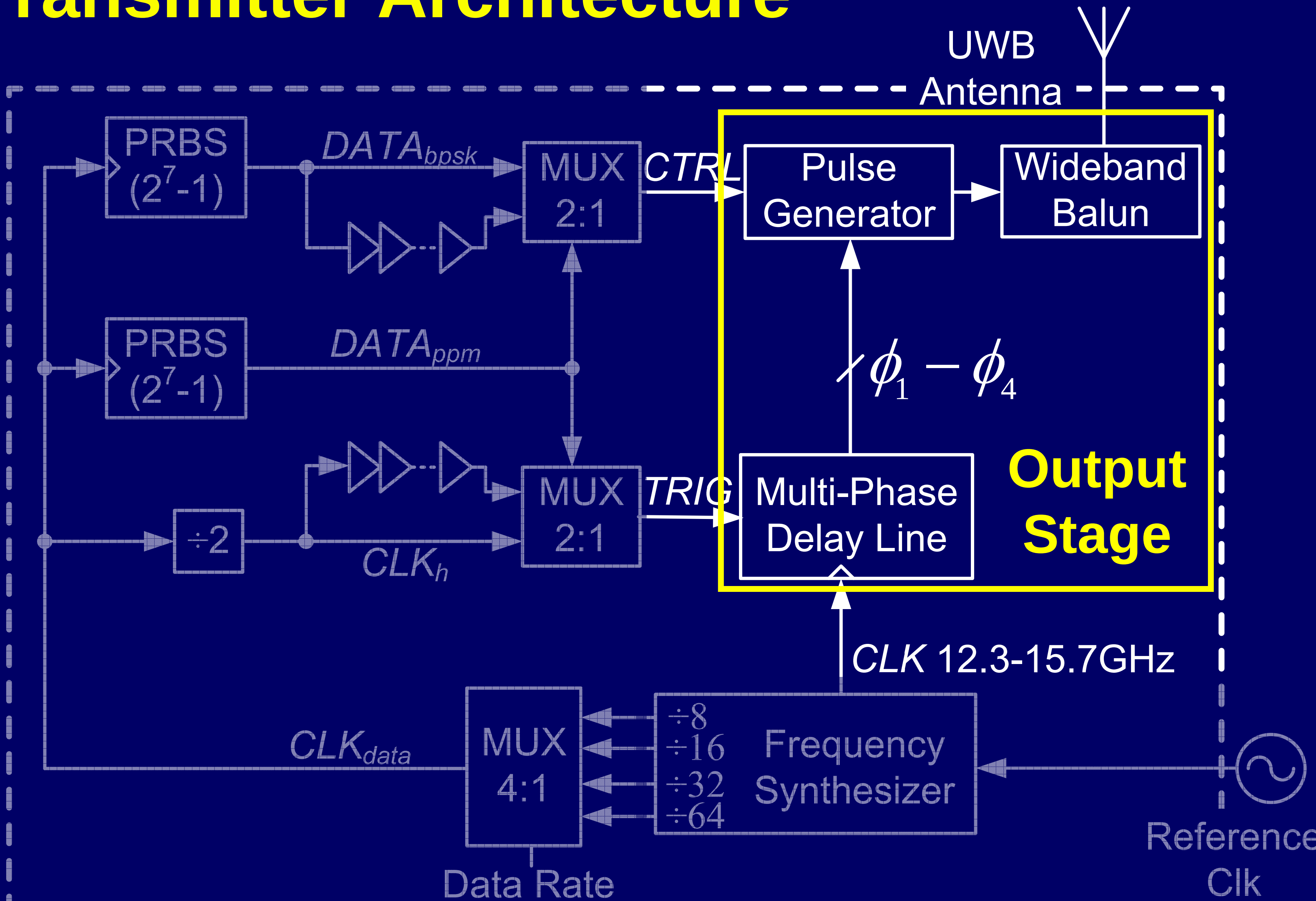


$$H'(z) = (1 - z^{-1})H(z) = (1 - z^{-1})^{N+1}$$

Transmitter Architecture



Transmitter Architecture



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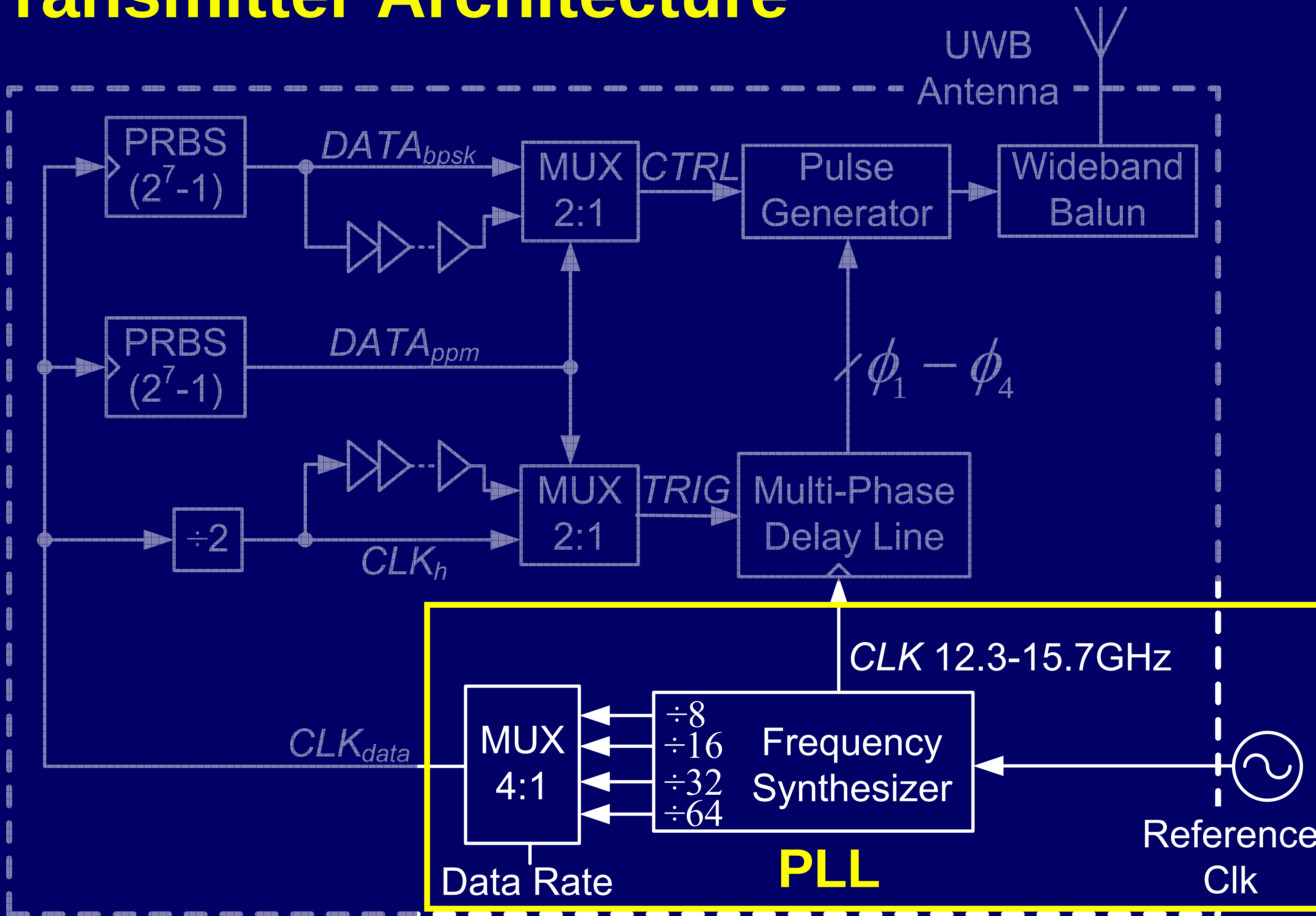
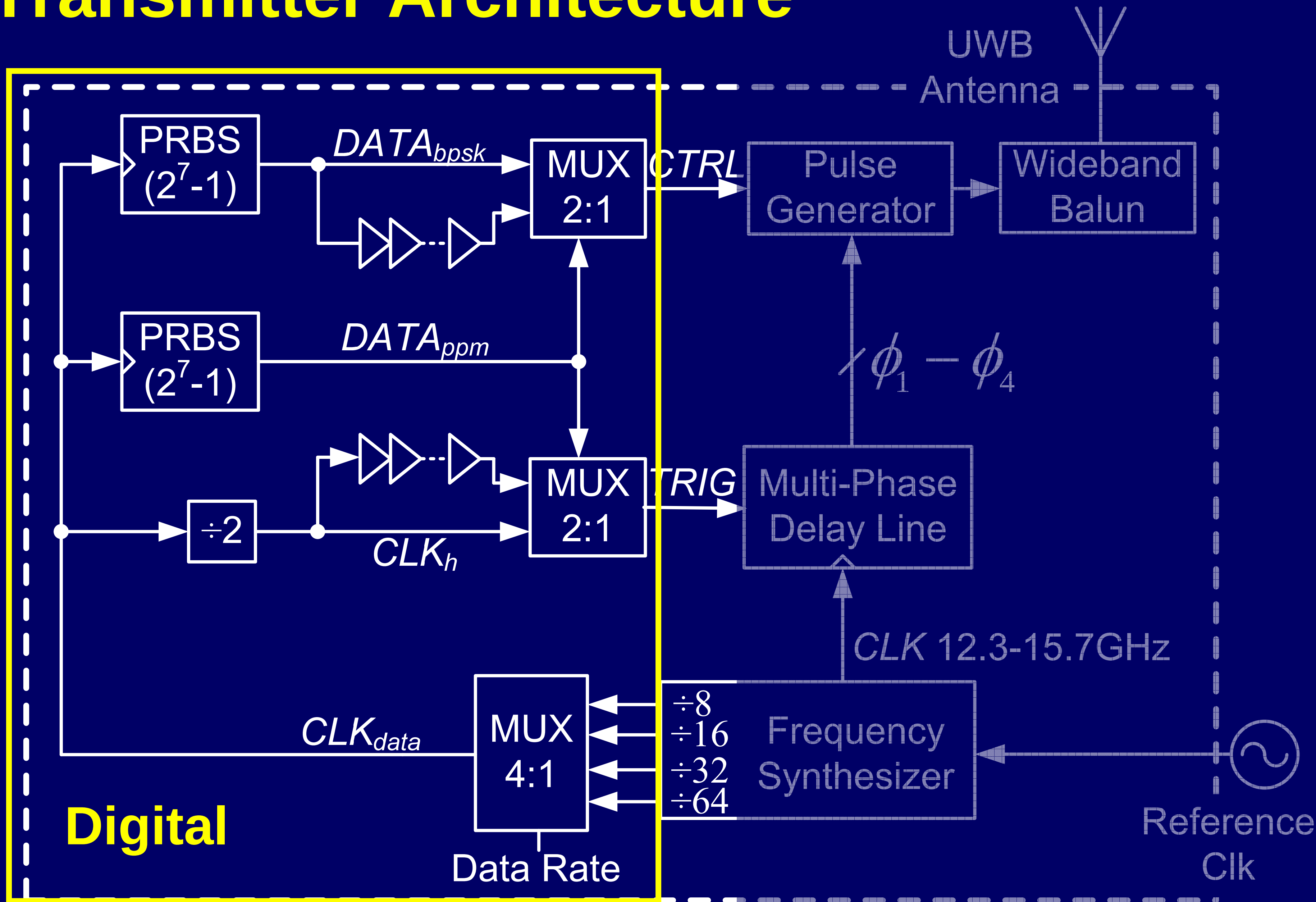
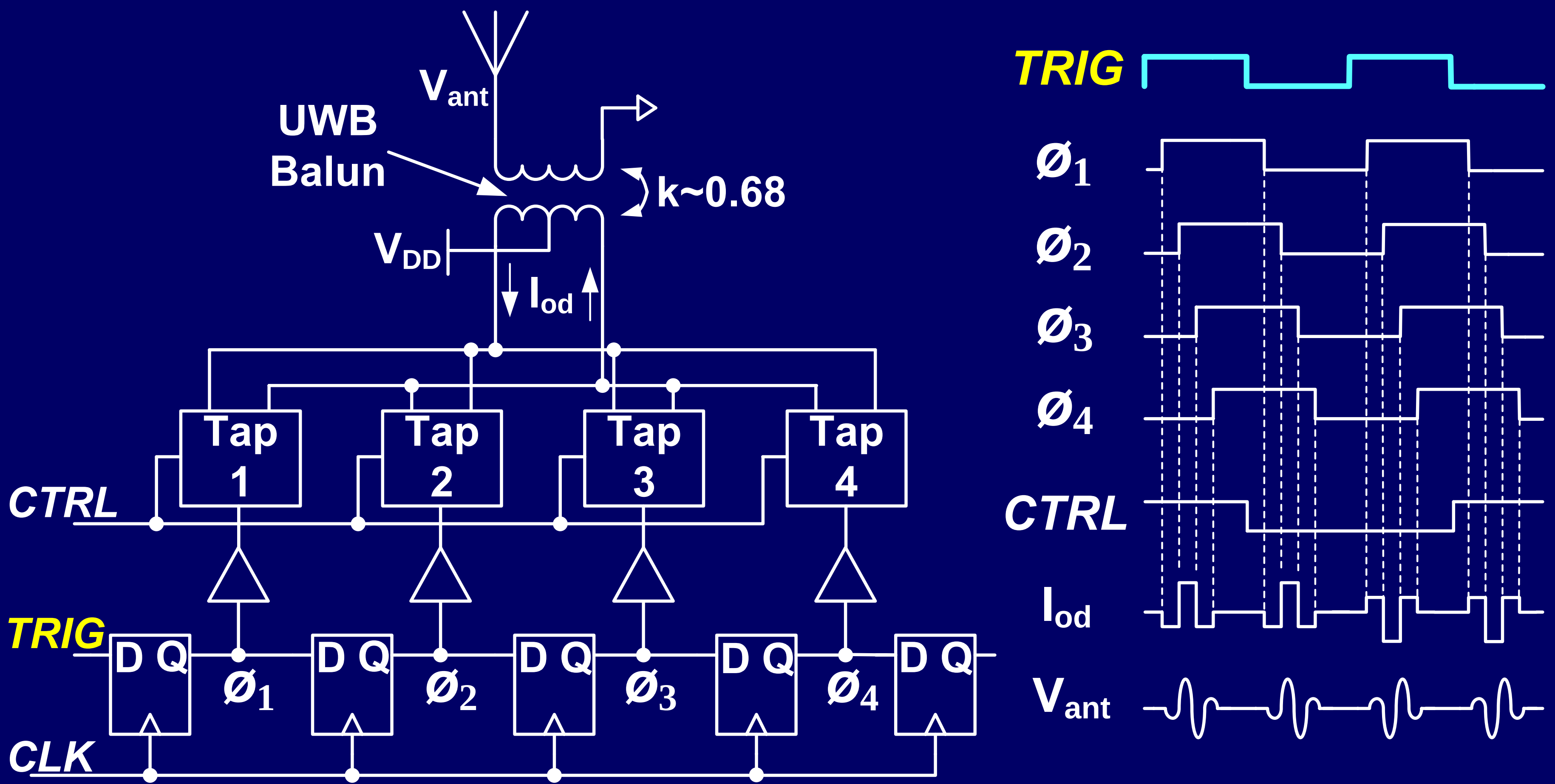


Transmitter Architecture



Output Stage



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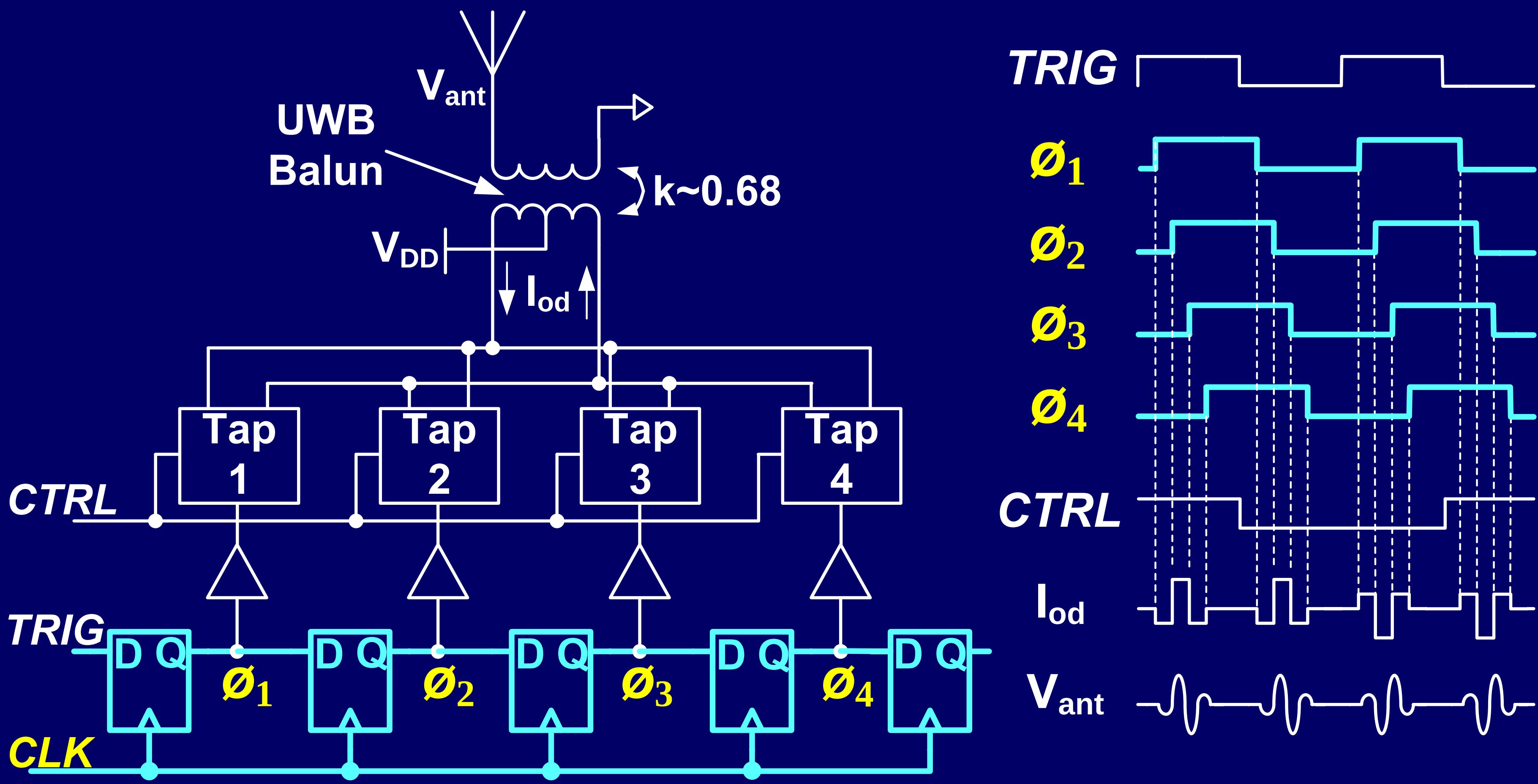

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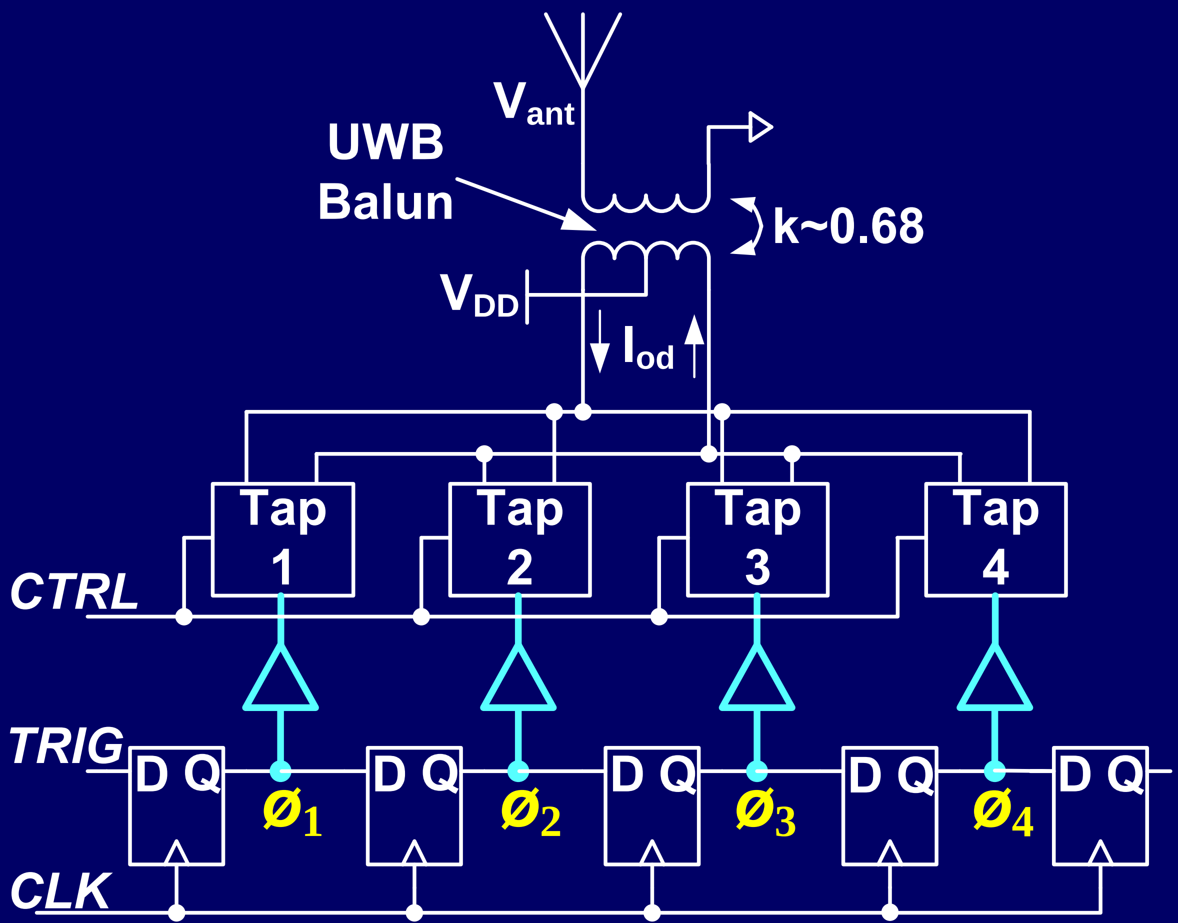
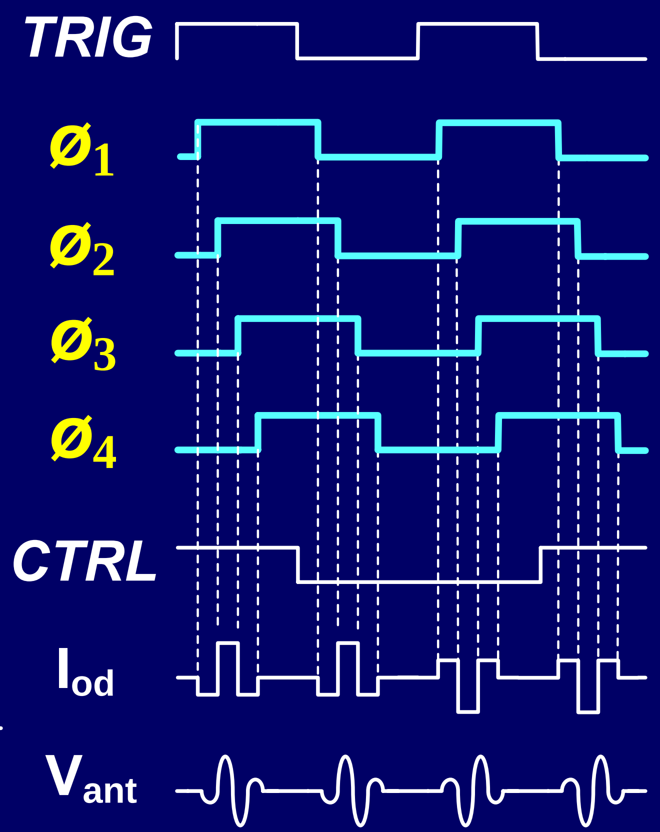
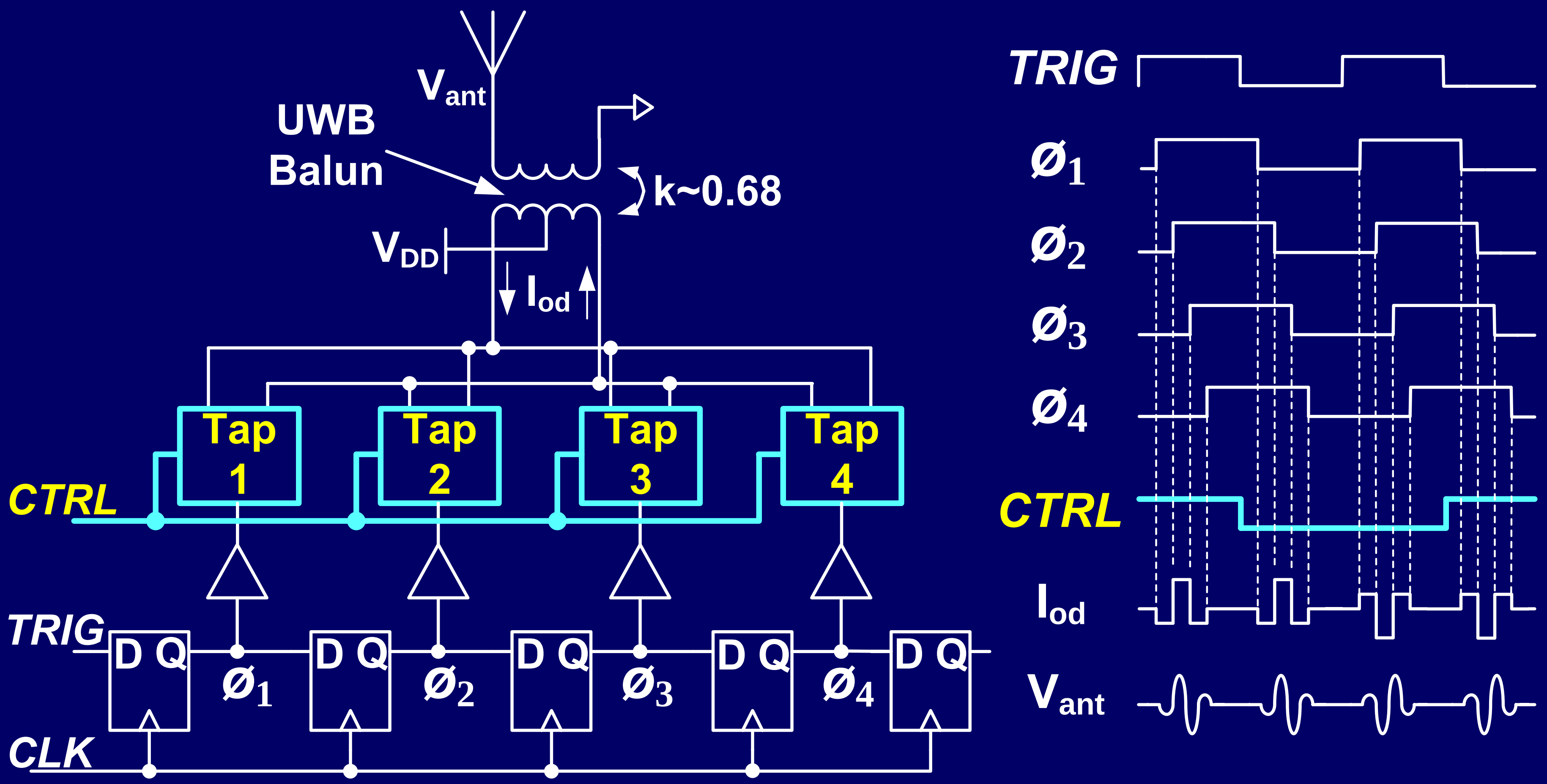
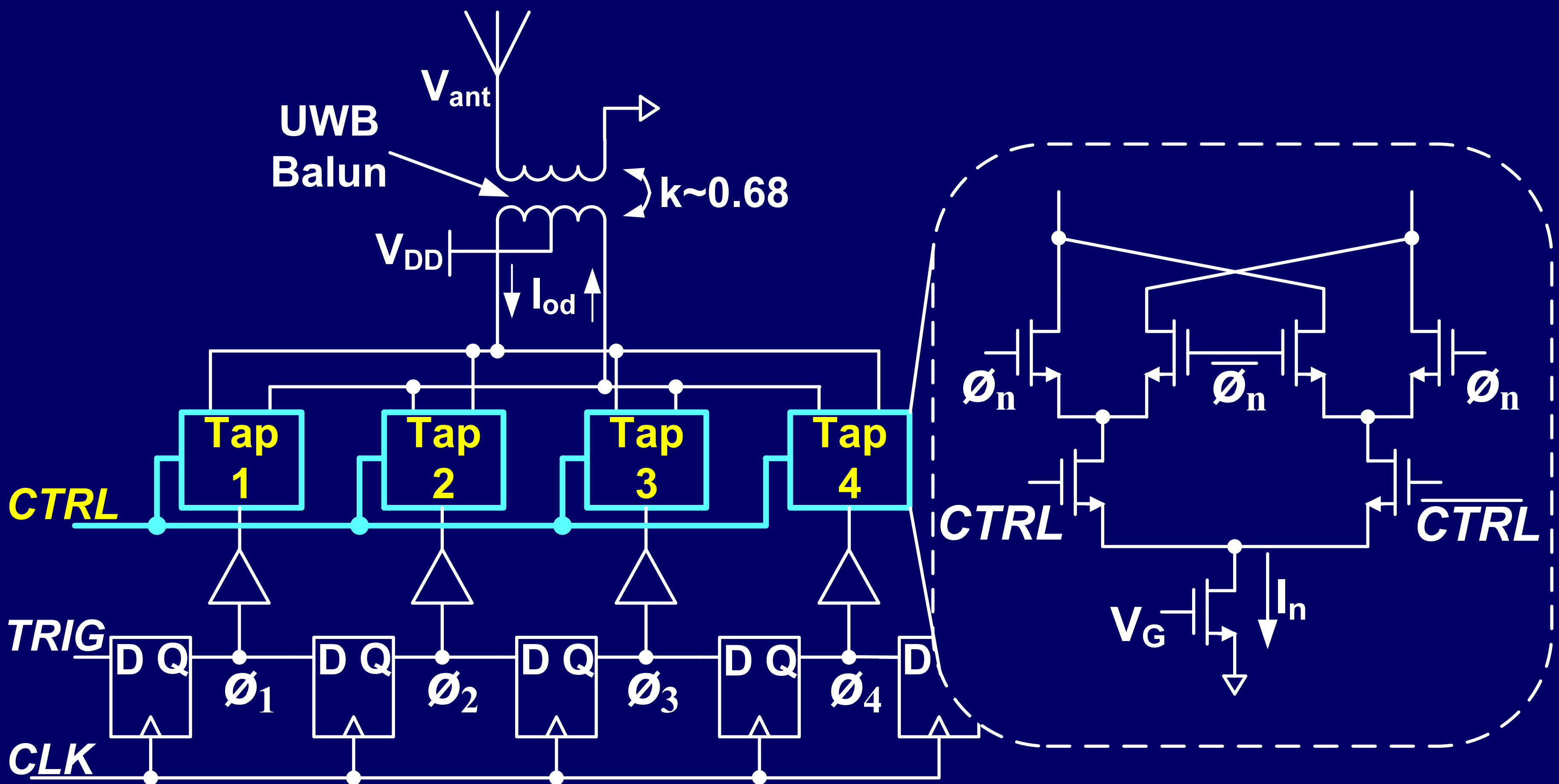




Output Stage



Output Stage



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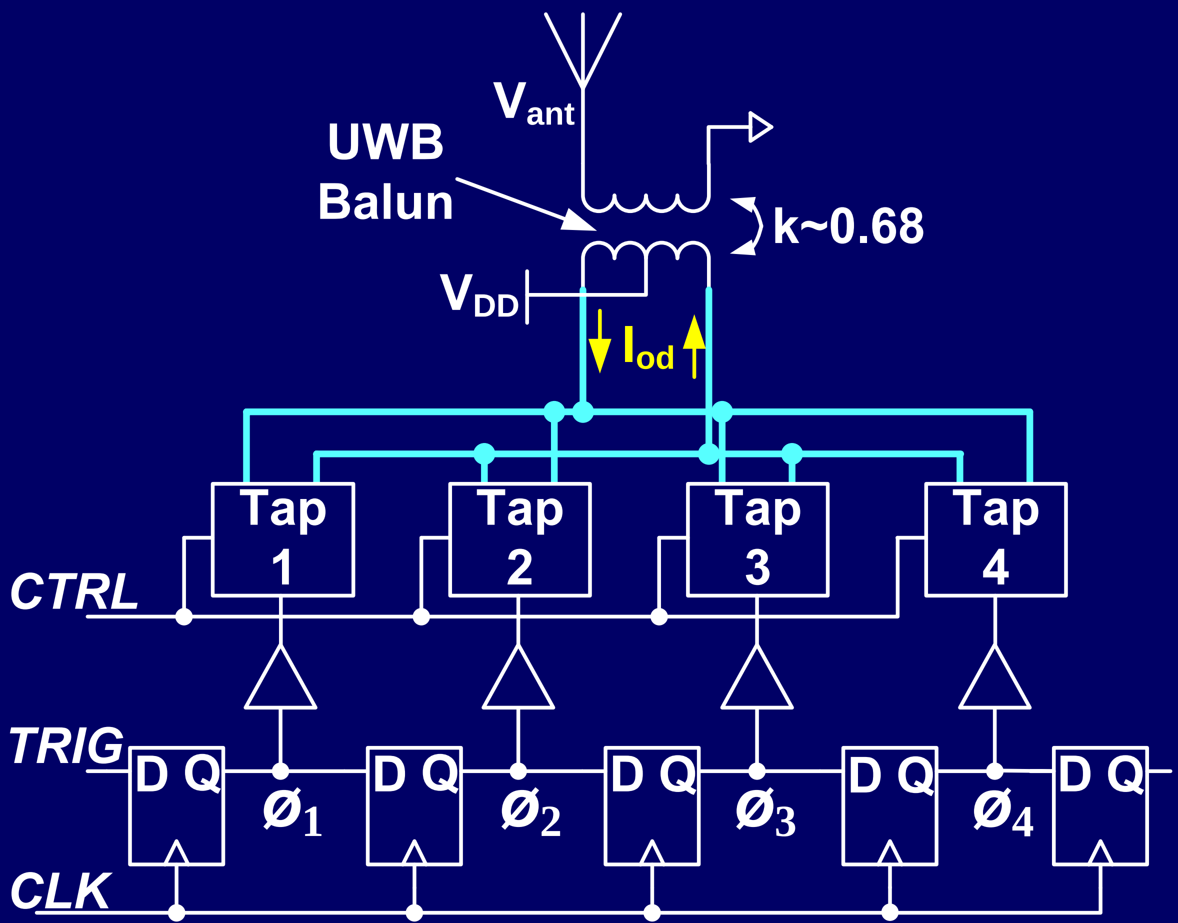

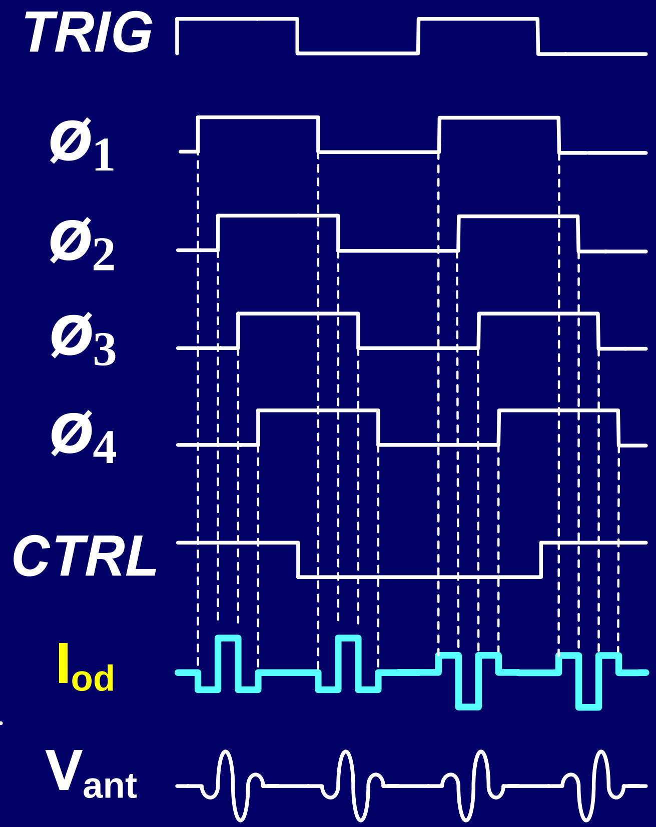

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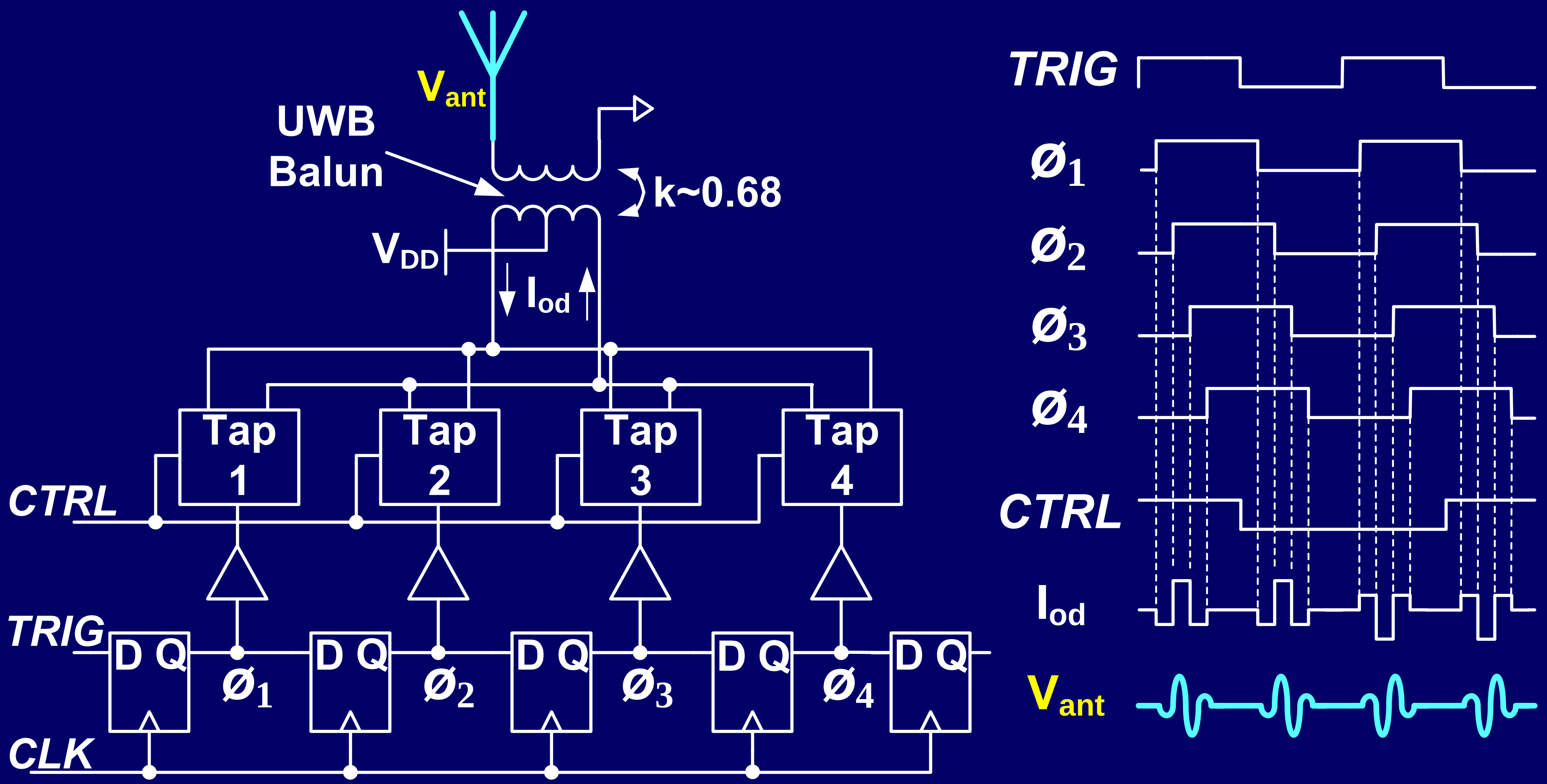
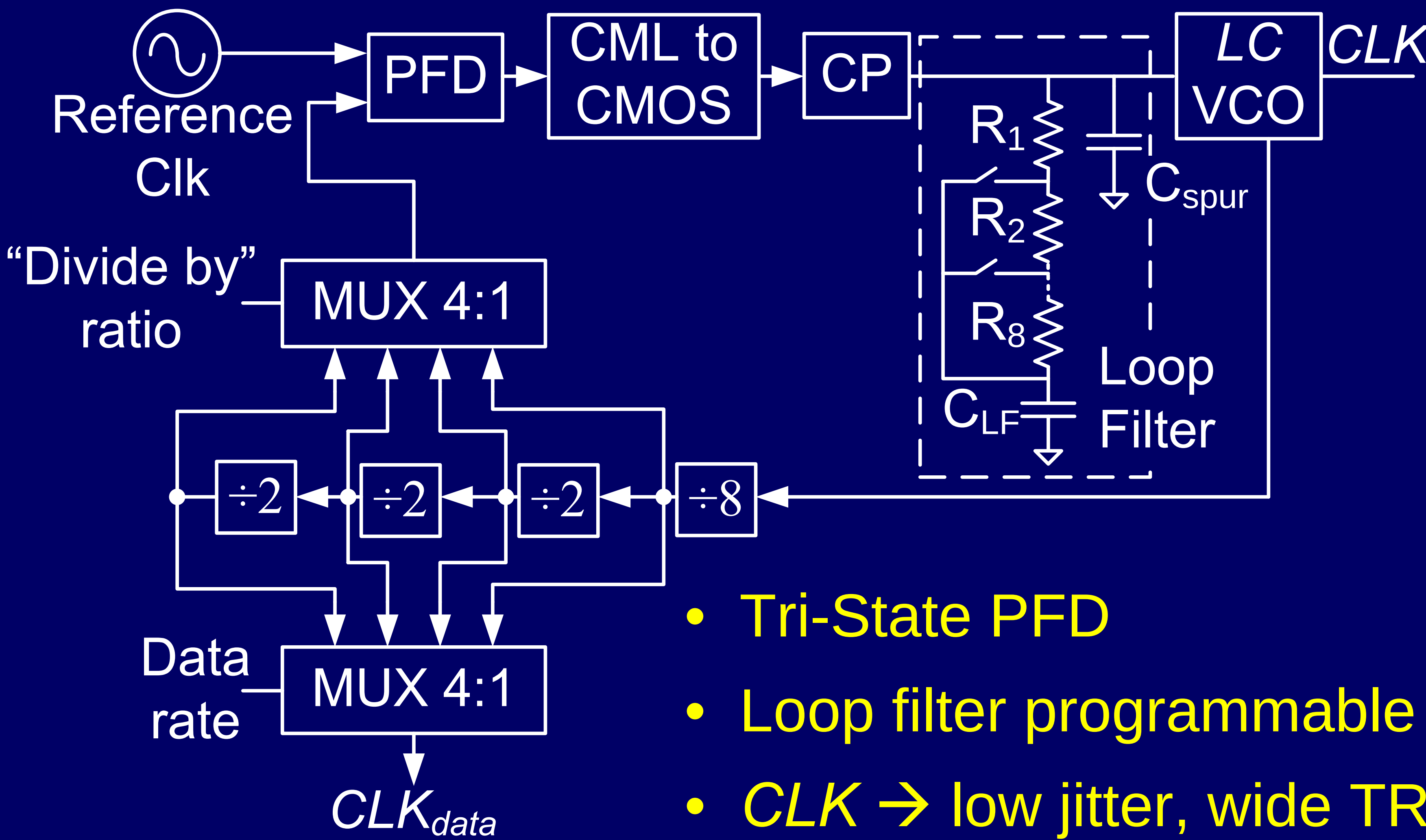
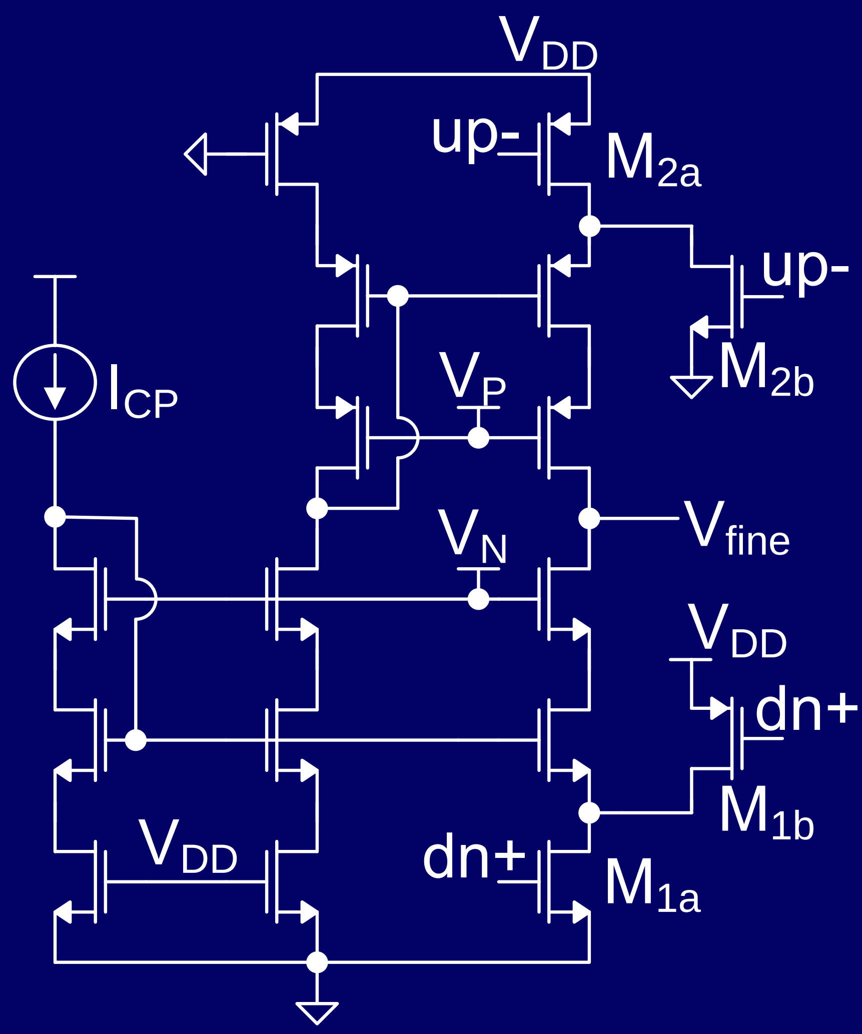


Frequency Synthesizer (PLL)



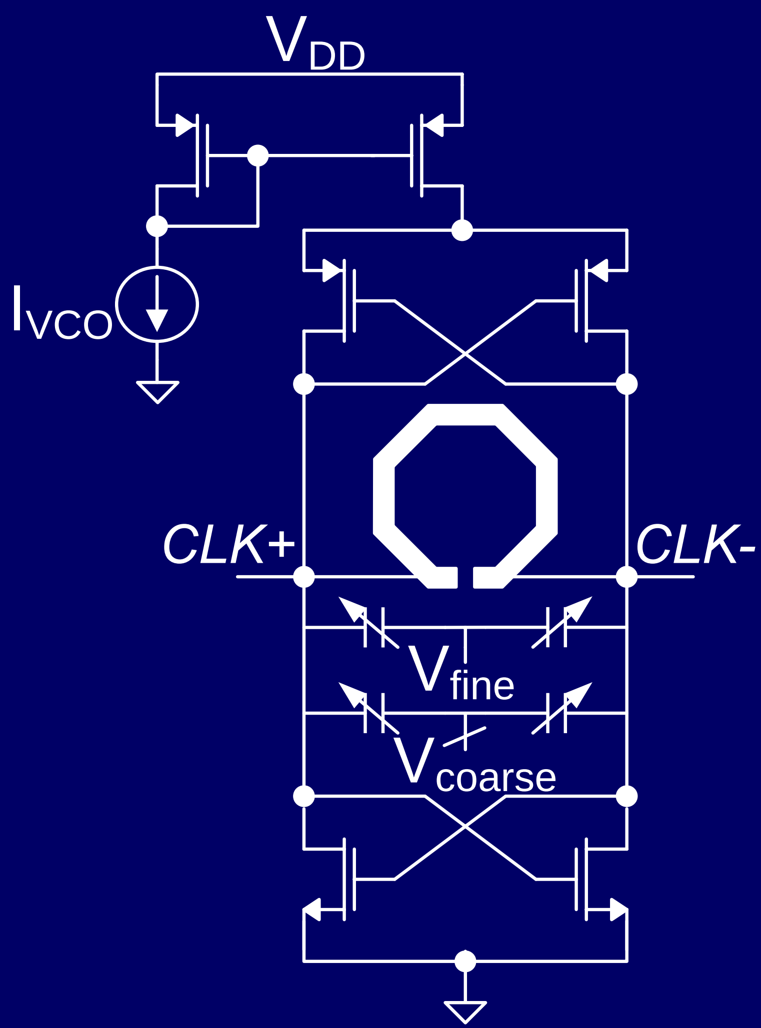
- Tri-State PFD
- Loop filter programmable
- *CLK* → low jitter, wide TR

Charge Pump



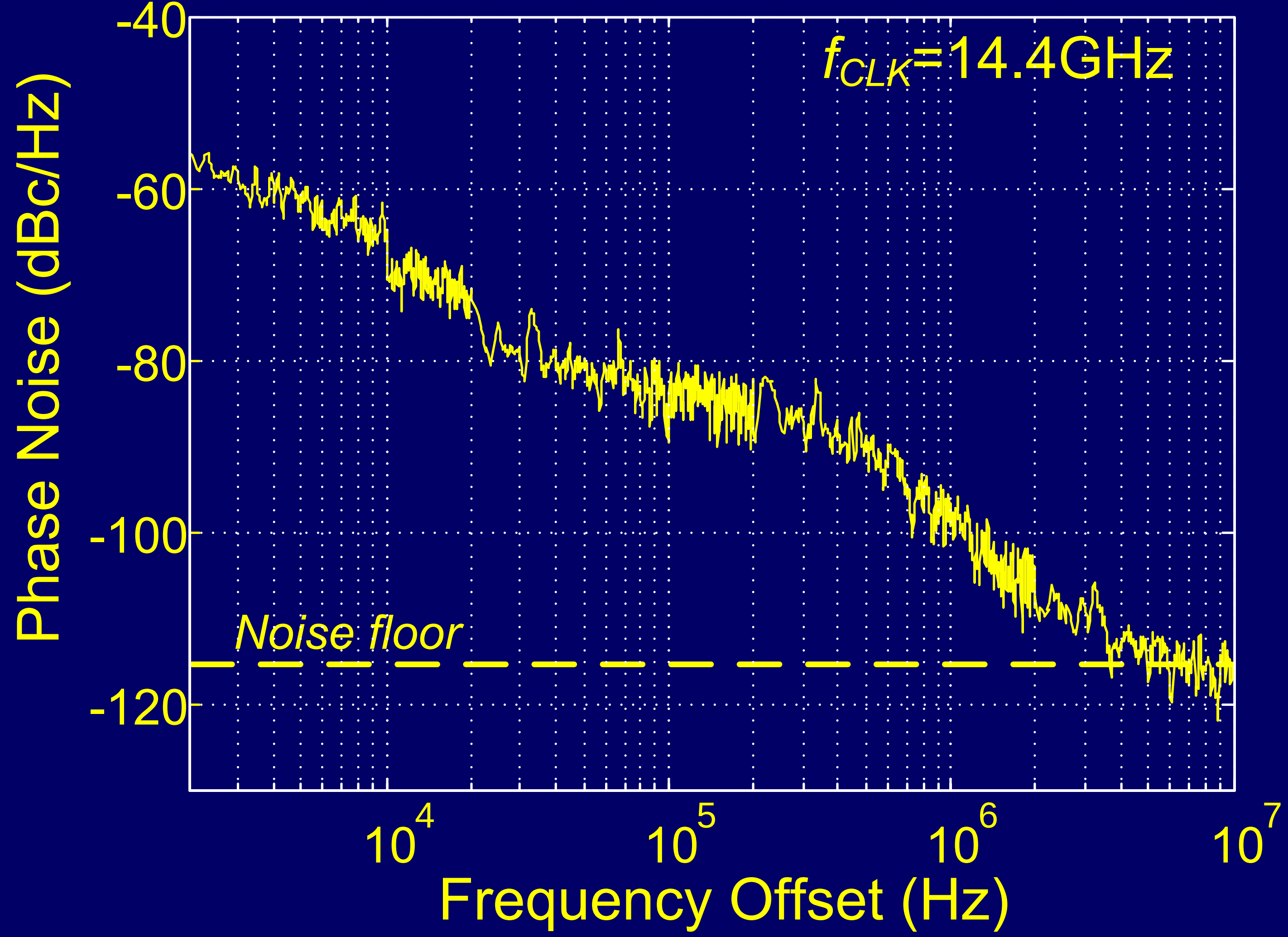
- Single-ended design for simplicity
- Low-voltage cascode current mirrors
- M_{1a} and M_{2a} are switches
- M_{1b} and M_{2b} provide discharge path

Voltage Controlled Oscillator

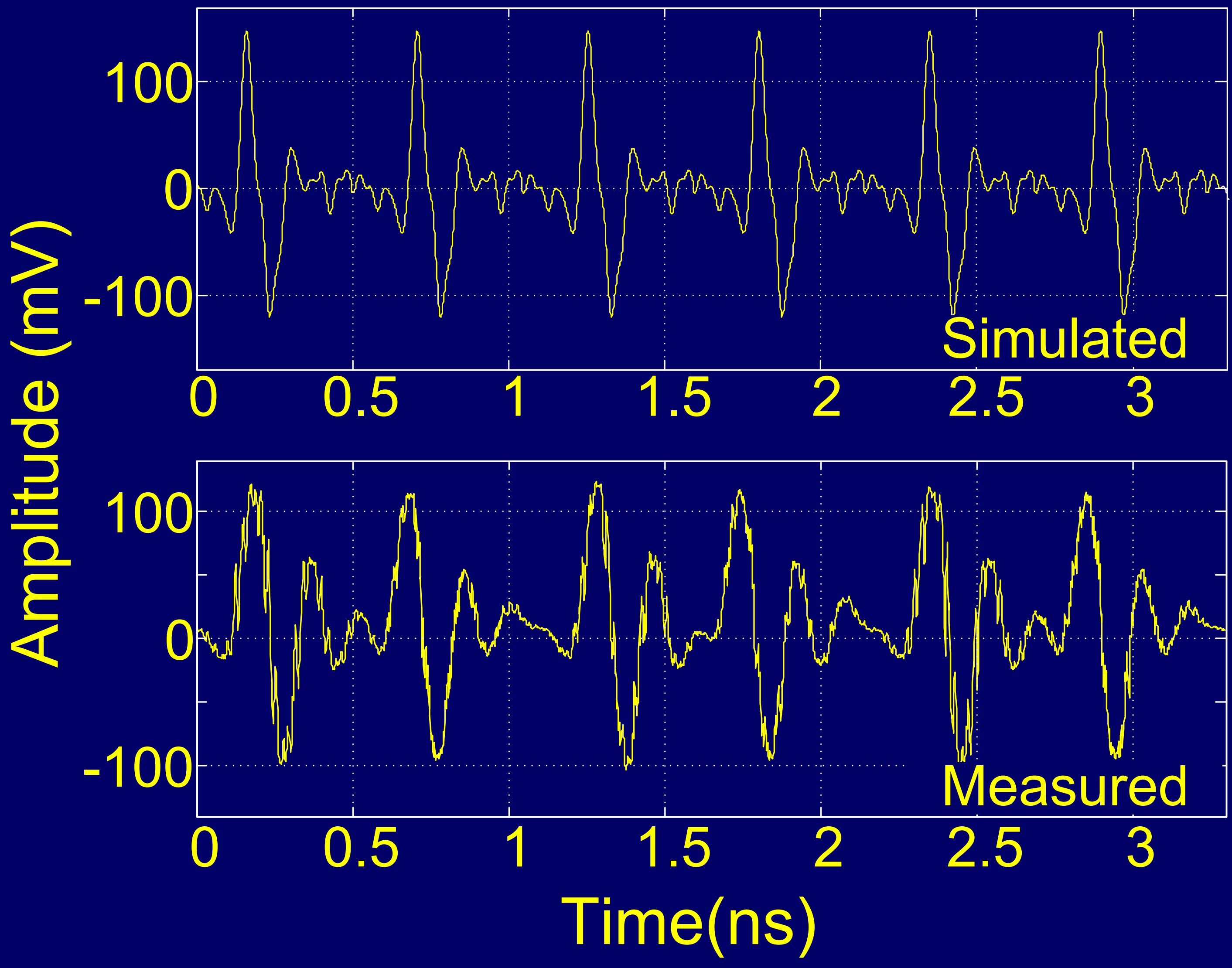


- Single-loop inductor
- AMOS varactors for fine and coarse tuning
- Cross-coupled CMOS
  - –Sets bias for AMOS
  - –Reduces 1/f noise upconversion

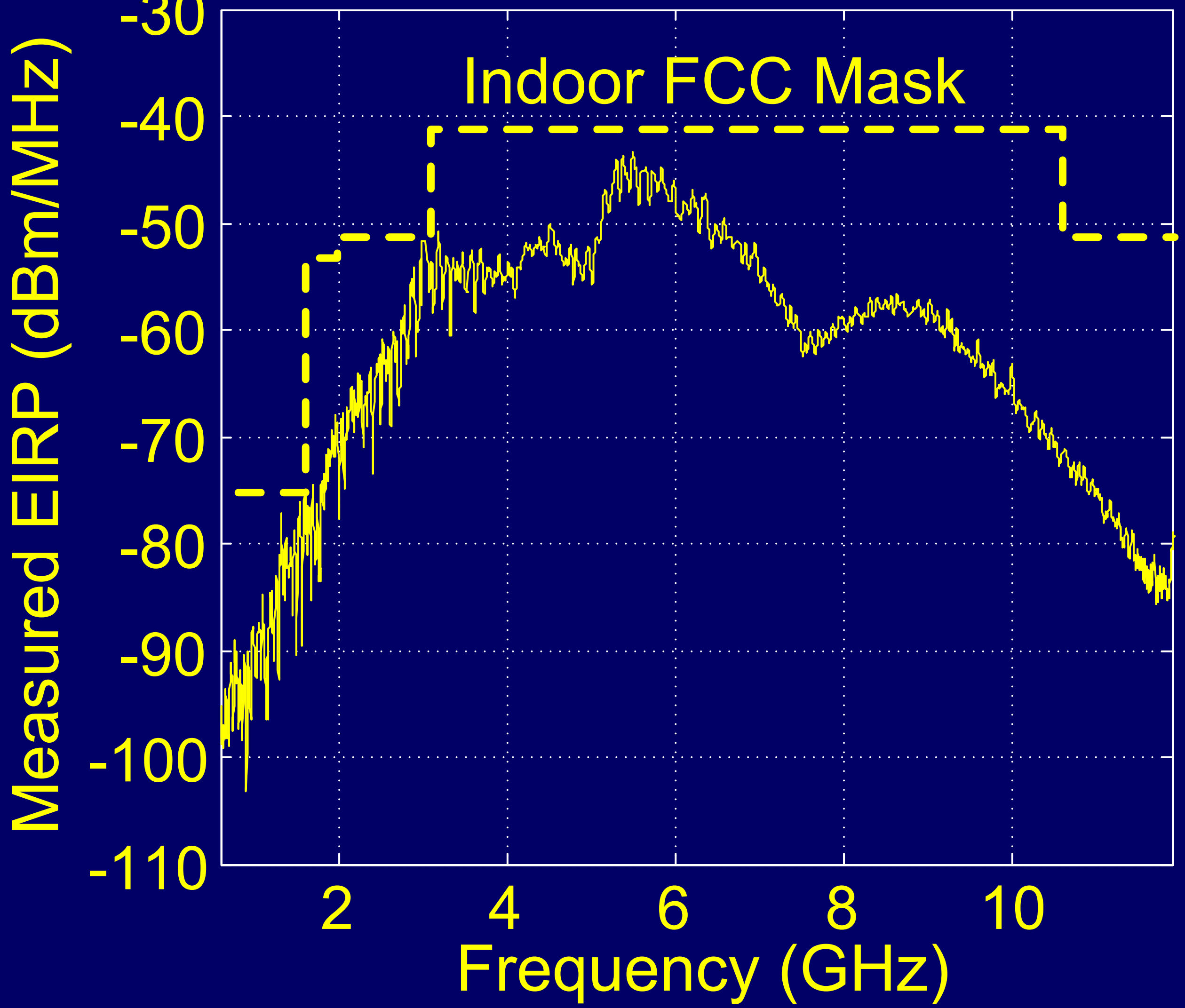
Measured Phase Noise at 14.4GHz



Simulated and Measured Pulses



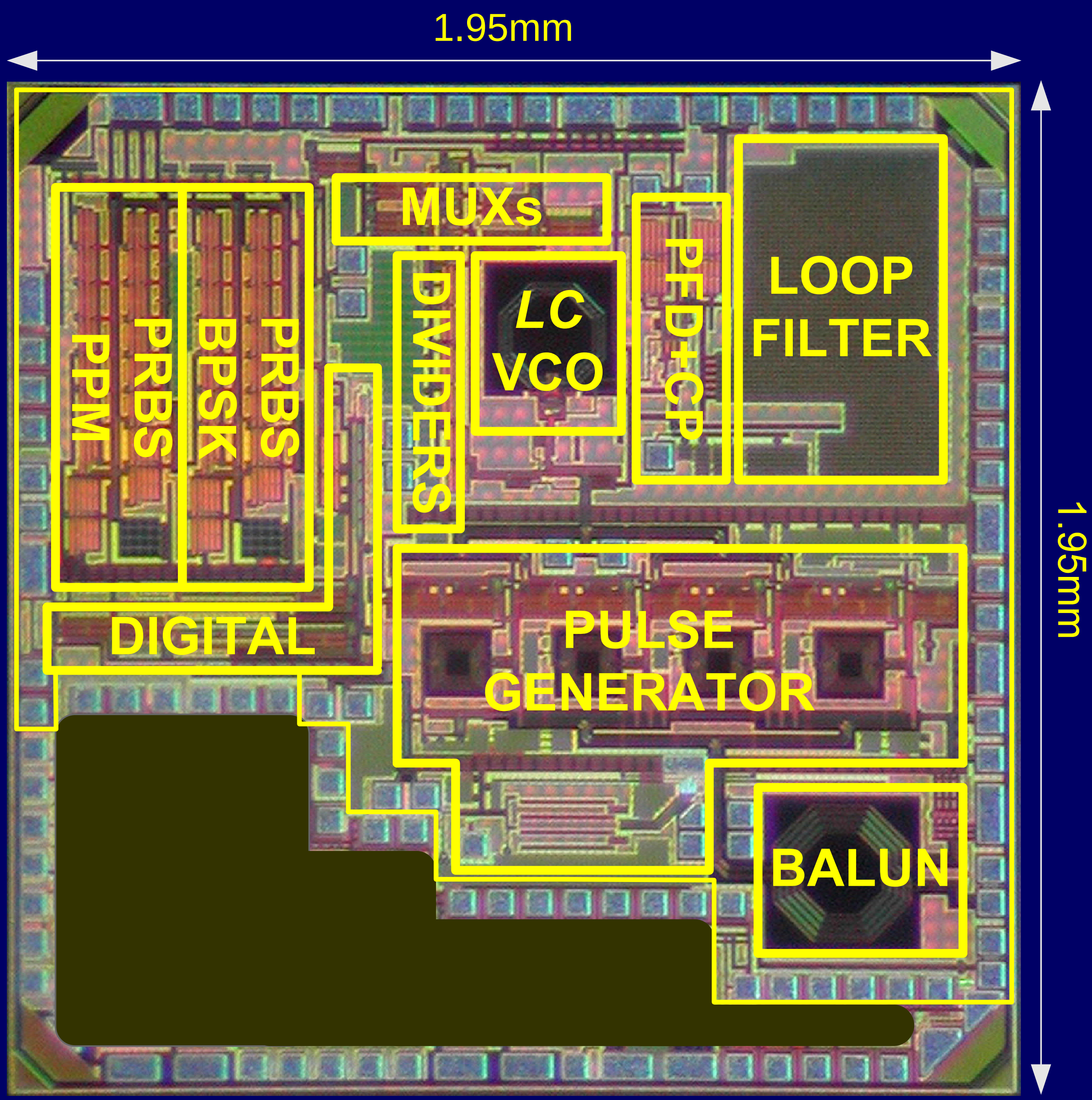
Measured EIRP



Performance Summary at 25°C

Technology	90nm CMOS
Die Area	$2.83mm^2$
Max. Pulse Rate	1.8Gpulses/s
Max. Pulse Amplitude	220mVpp
Modulation	BPSK+PPM
VCO Range	12.3-15.7GHz
Jitter (rms)	1.9ps
Jitter (peak-to-peak)	15.1ps
Supply Voltage	1.0V
Power Dissipation	
Pulse Generator	129mW
PLL	98mW
Test-Mode Circuitry	143mW
Total Transmitter Power	227mW
Energy/Pulse	126pJ/pulse

Die Micrograph



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- Wide Tuning-Range VCO Design (with Stephen Bruss)
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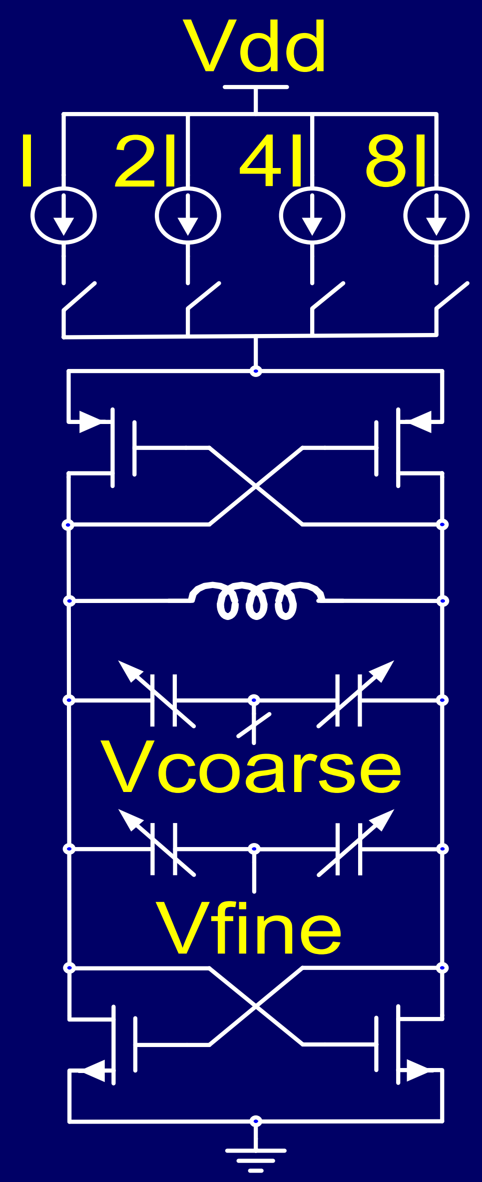
Motivation

- How can we improve the tuning range of a conventional *LC* VCO without increasing phase noise and area significantly?

- **Key observertion:** Capacitor Q is low at high frequencies ($Q_C=1/\omega RC$) but inductor Q is high!

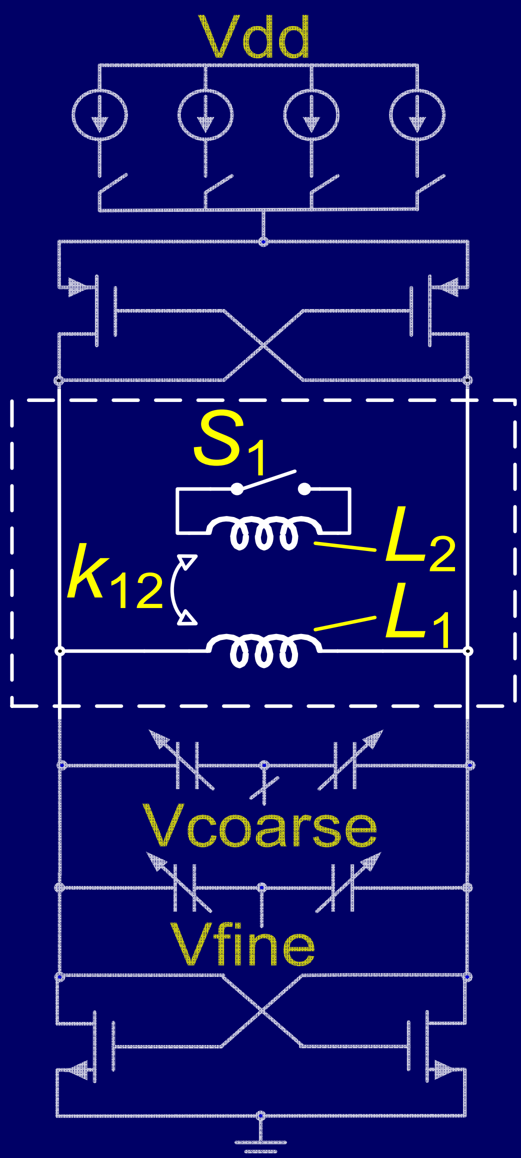
VCO1: Single-inductor *LC* VCO

- **Built as reference for comparison**
- **Inductor**
  – Single-turn
  – Uses both M8 & M9
  – Has high self resonant freq.
  – Flat *L* and Q vs. Frequency
- **AMOS varactors**
  – Fine tuning (Kvco=150MHz/V)
  – Coarse tuning (Binary weighted)



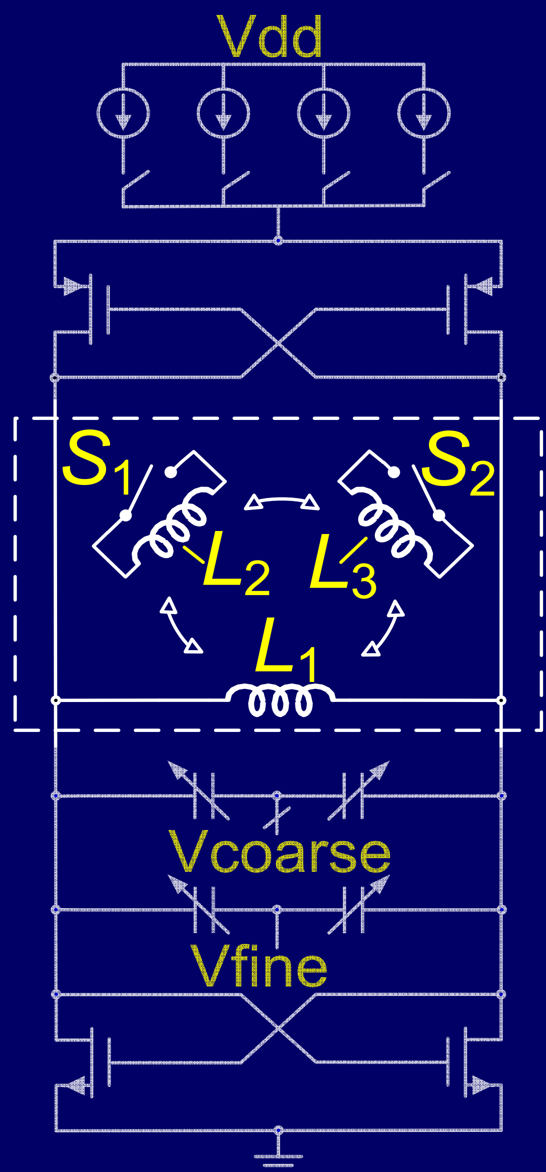
VCO2: *LC* VCO with one extra coil

- **Coil L_2 mutually coupled to L_1**
- **When S_1 is OPEN**
  - No Eddy Currents in L_2
  - Inductance is L_1
- **When S_1 is CLOSED**
  - Eddy Current flow in L_2
  - Inductance drops to $L_1 - k_{12}^2 L_2$

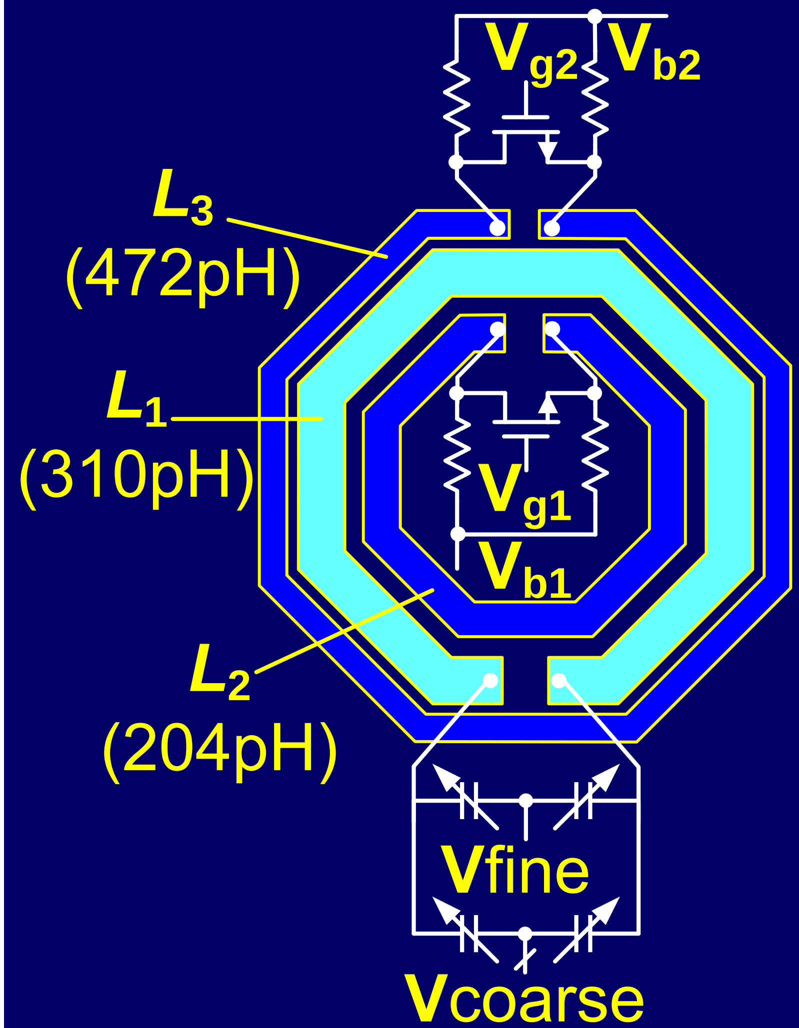


VCO3: *LC* VCO with two extra coils

- **Coils L_2 and L_3 are mutually coupled to L_1**
- **Switches S_1 and S_2 control currents in L_2 and L_3**
- **Four frequency bands**

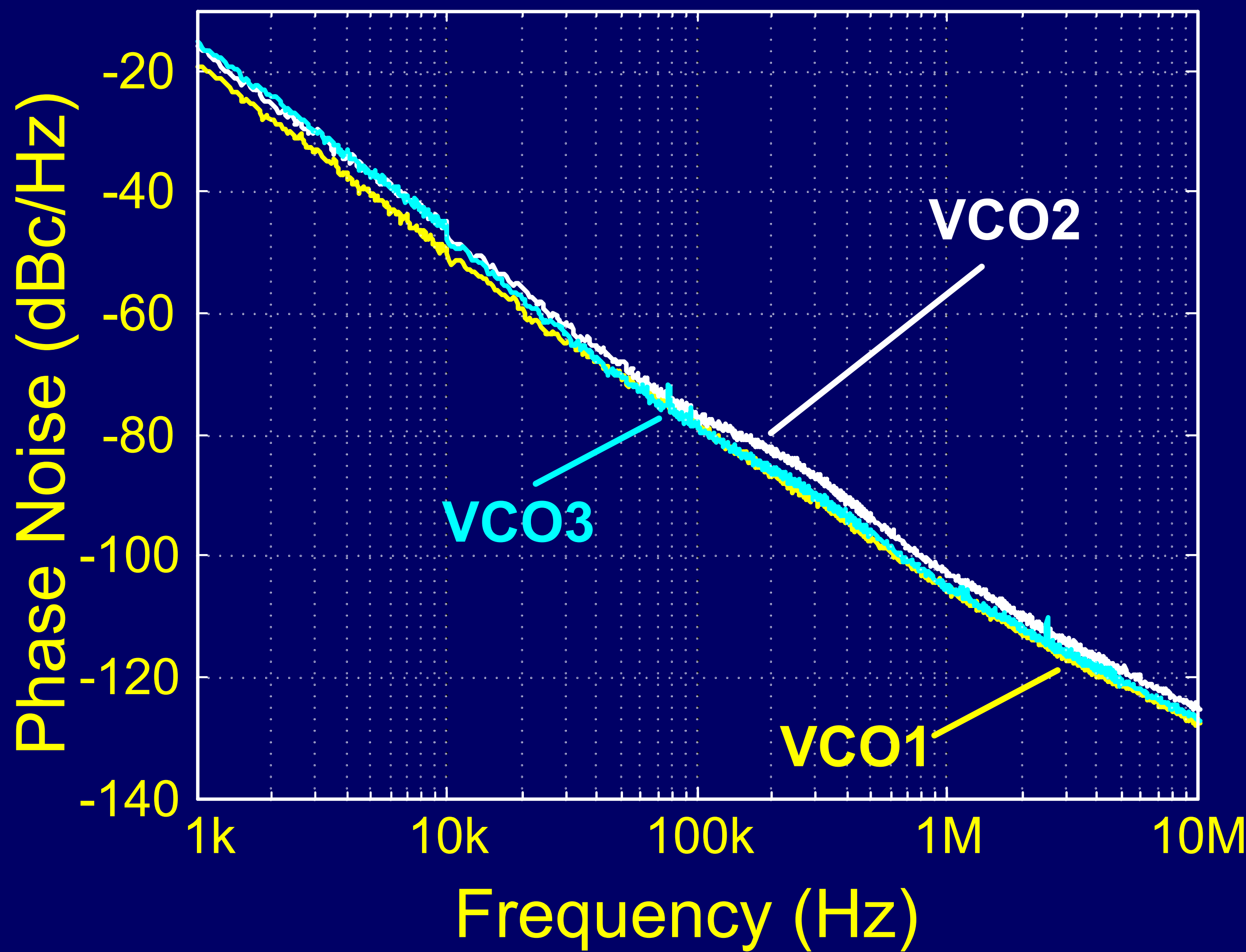


Resonator Layout

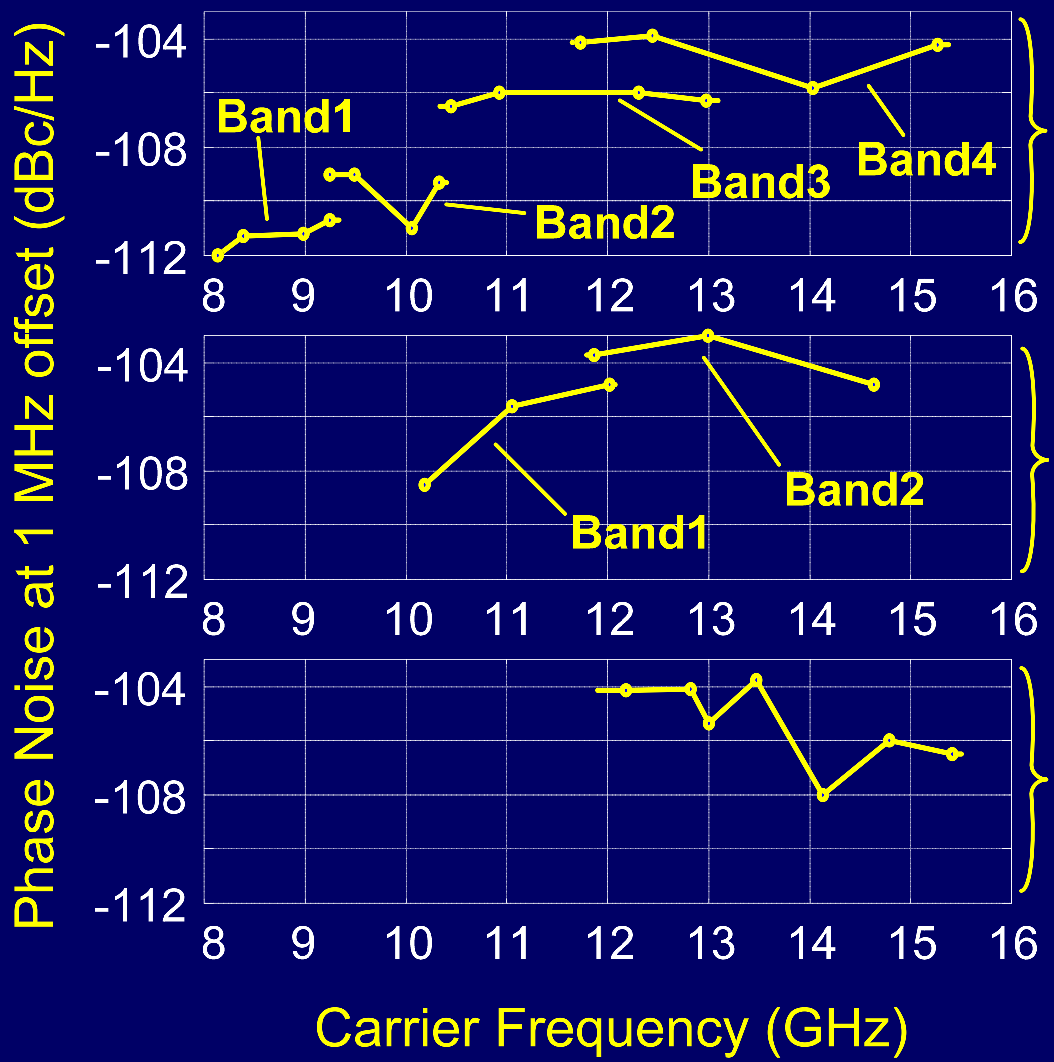


- **Extra coils add small area**
- **L_2 & L_3 biased independently**
  - Set V_{b1} & V_{b2} to opposite polarity of V_{g1} & V_{g2}
  - Improves (Q x TR) by 1.6
- **Switch size critical (R_{on}, C_{off})**

Measured Phase Noise at 13GHz



Phase Noise at 1MHz offset



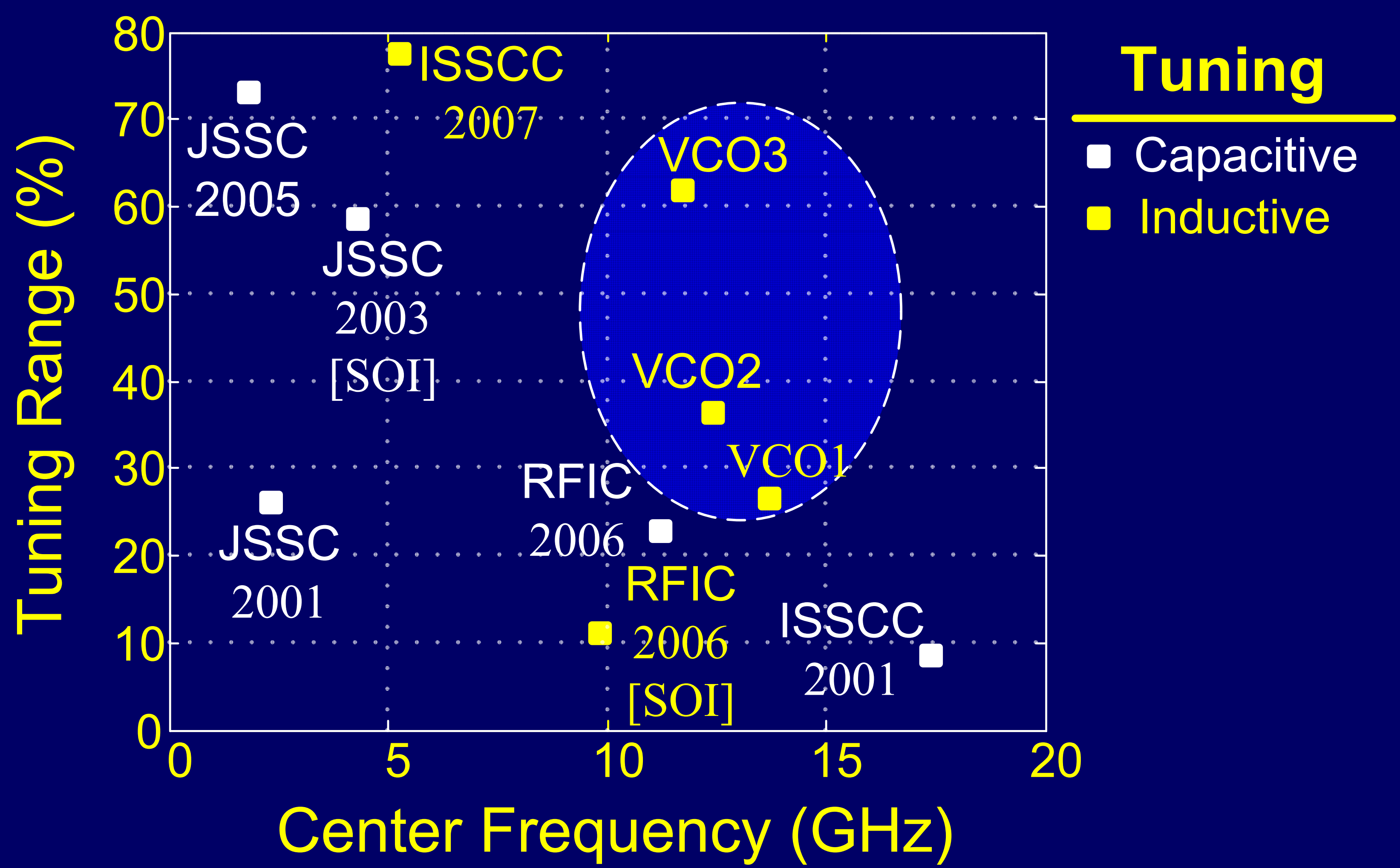
Tuning Range

VCO3	61.9%
VCO2	36.3%
VCO1	26.6%

Performance Summary at 25°C

	VCO1	VCO2	VCO3
Process	90nm CMOS	90nm CMOS	90nm CMOS
Power Supply	1.2V	1.2V	1.2V
Center Frequency	13.7GHz	12.4GHz	11.8GHz
Tuning Range	26.6%	36.3%	61.9%
Power	2.81mW	5.65mW	7.7mW

Performance Comparison



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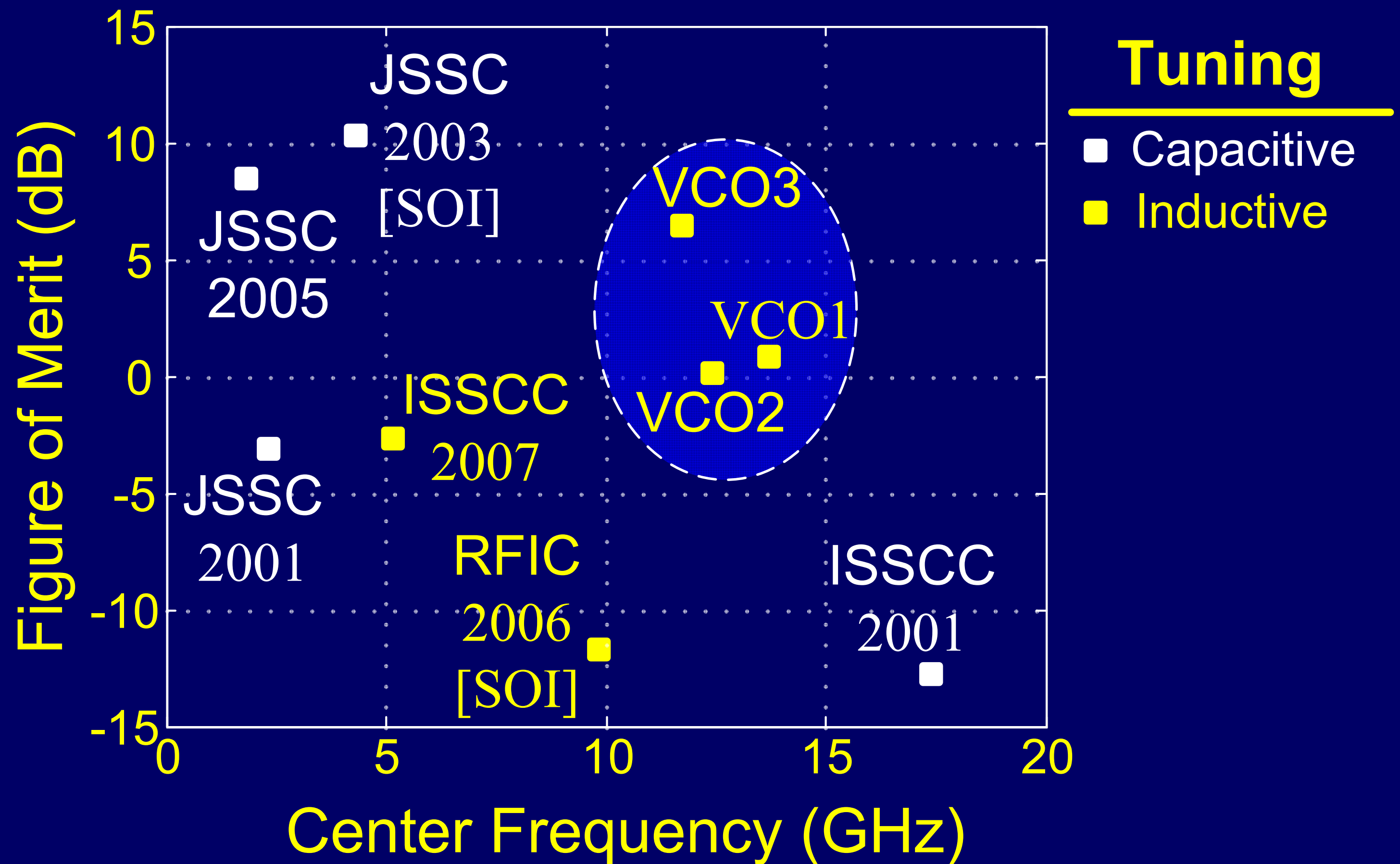
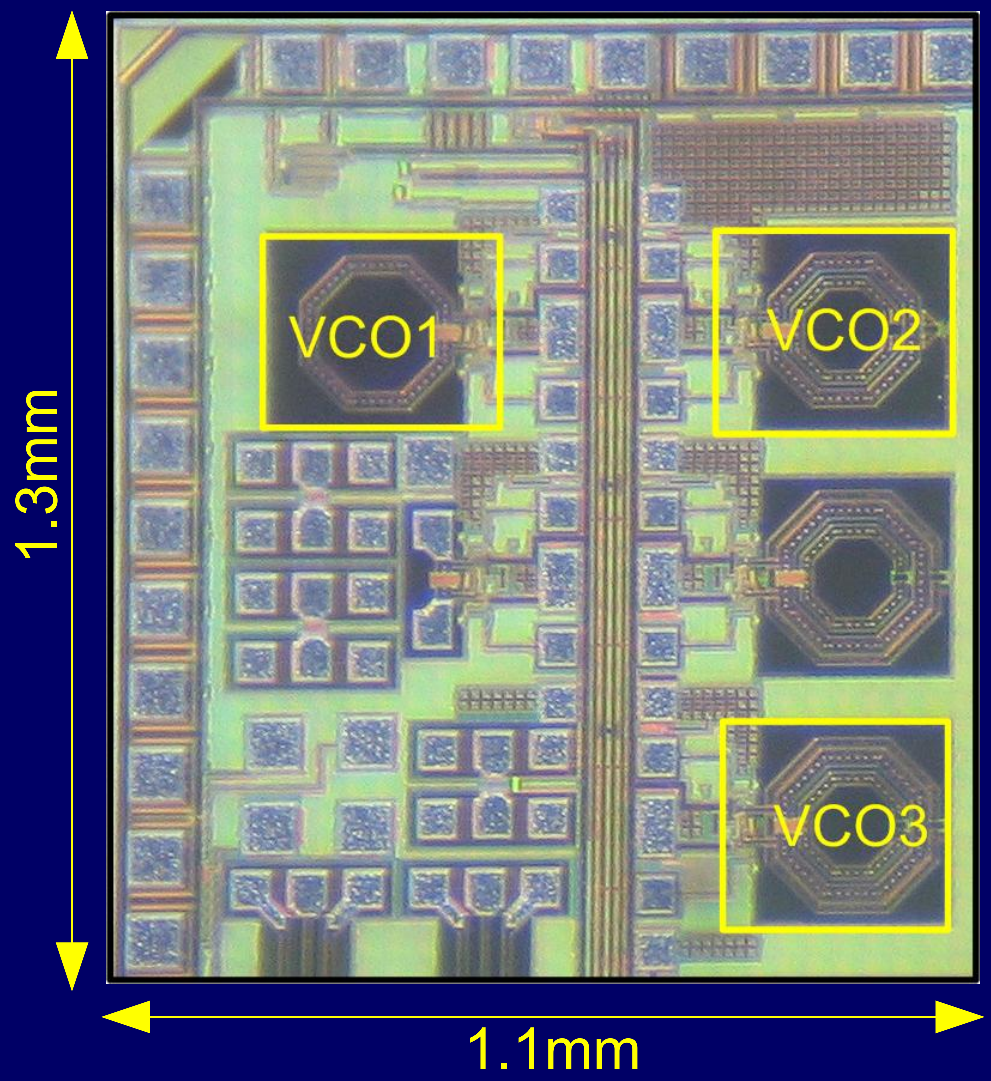


$$FOM = 10\log\left[\frac{kT}{P}\cdot\left(\frac{f_{max}-f_{min}}{f_{off}}\right)^2\right] - PN(f_{off})$$

[Ham, Hajimiri, JSSC 01]

Die Micrograph



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- Modeling of UWB Antennas in RF Circuit Simulators
- A new pulse-based UWB transmitter architecture
- A Method to improve to tuning ranges of conventional *LC* VCOs using switched coupled-inductors

Acknowledgements

- **Advisor: Prof. Richard R. Spencer**
- **Professors P.J. Hurst, A. Knoesen**, **B. Kolner, S. H. Lewis**, **A. H. Pham** and **D. Yankelevich** for their generous help
- **Stephen P. Bruss (VCO Project)**
- **Dan Oprica and the IEEE SCV SSCS**
- **Fabrications were graciously provided by TSMC**
- **Research was supported by:**

  Agilent, Broadcom, Intel, Marvell, TDK, Texas Instruments and the UC MICRO Program

-END-