A Low-Power 60GHz Transceiver with Integrated Baseband Circuitry

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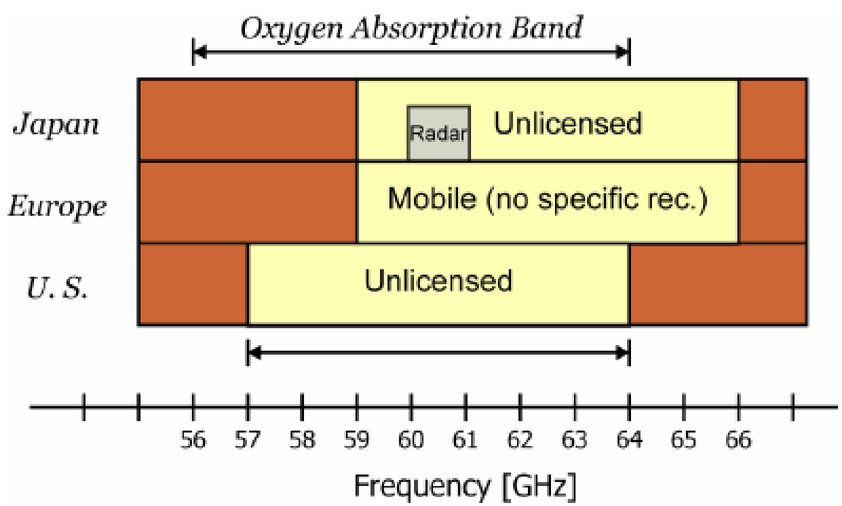
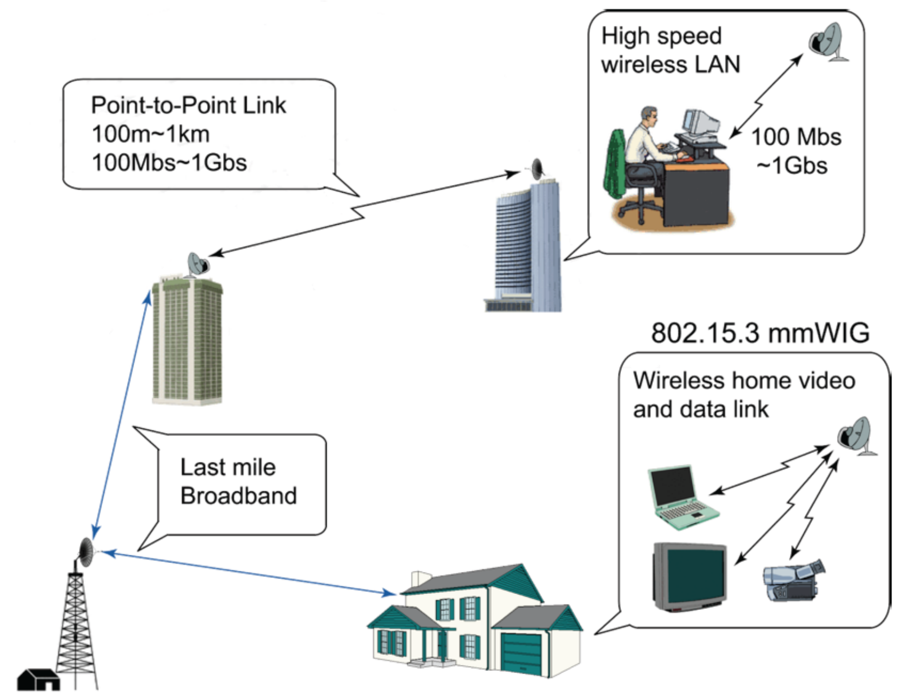
The 60GHz Band





- World-wide license-free 60GHz spectrum allows Gbps communication
- Applications range from Last-Mile to Last-Inch
- Generally limited to LOS due to power constraints
- Security due to absorption by O_2 and building materials

Why CMOS for 60GHz?

- Energy efficiency and cost are key for mobile applications
- Leverage low-power digital and cost advantage of CMOS
- CMOS allows integration of RF and baseband on single chip as well BIST capabilities

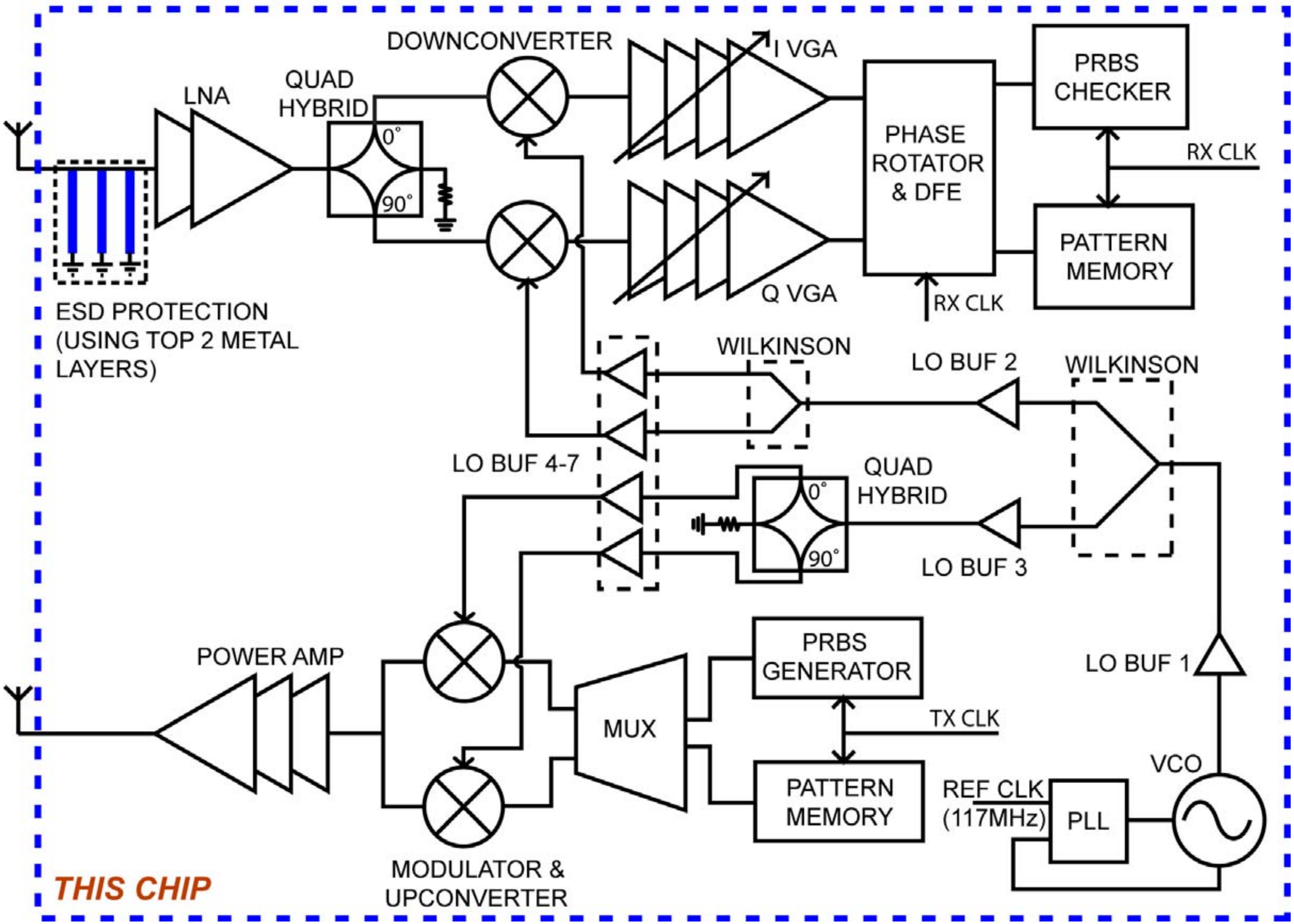
60GHz in Mobile Applications

- Significant progress in mm-wave building blocks
- Transceivers for high-def. video in development
  - WirelessHD demo at CES
  - Wall-powered, multi-Watt
- Improved energy-efficiency is key for multi-gigabit mobile communication
  - Many open questions remain
  - Multiple efforts from industry and academia

Recent 60GHz Transceiver Efforts

Ref.	Tech	Pwr (mW) TX/RX	PA o/p /Vdd	Integration	Data Rate
Pinel ISSCC ‘08	90nm CMOS	173/189	+8.4dBm /1.8V	Baseband integration not clear	7Gbps (QPSK) 15Gbps (16-QAM)
Wang ISSCC ‘07	130nm CMOS	-/-	-2dBm/--	No digital	4Gbps (BPSK)
Floyd ISSCC ‘06	130nm SiGe	801/527	+17dBm /4V	No digital / 2 RF chip module	0.63Gbps (OFDM/QPSK)
Tanomura ISSCC ’08	90nm CMOS	133/206	+8.3dBm /0.7V	No digital, VCO, or PLL / separate TX/RX	2.6Gbps (QPSK)
Vonigescu CICC ‘08	65nm CMOS	223/151	+2.4dBm /1.2V	No digital, VCO, or PLL	3.5Gbps (BPSK)

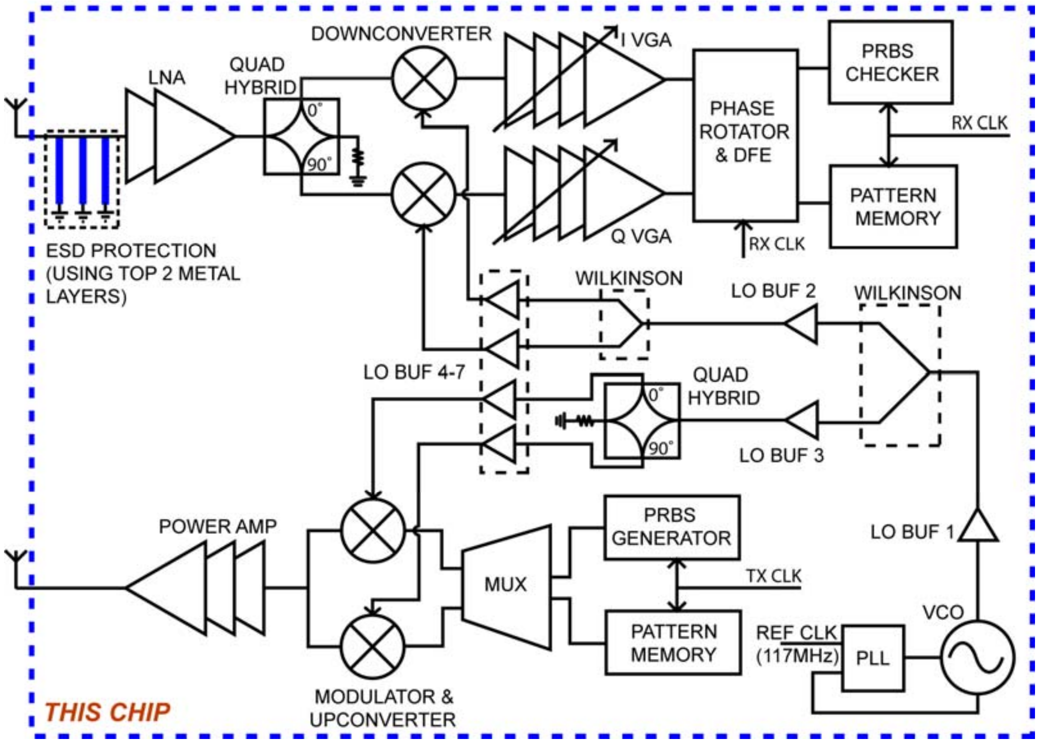
60GHz Transceiver Overview



Ref: C. Marcu et al, ISSCC 2009.

Outline

- Transmitter Blocks
- Receiver Blocks
- Phase Locked Loop and LO Chain
- Measurement Summary



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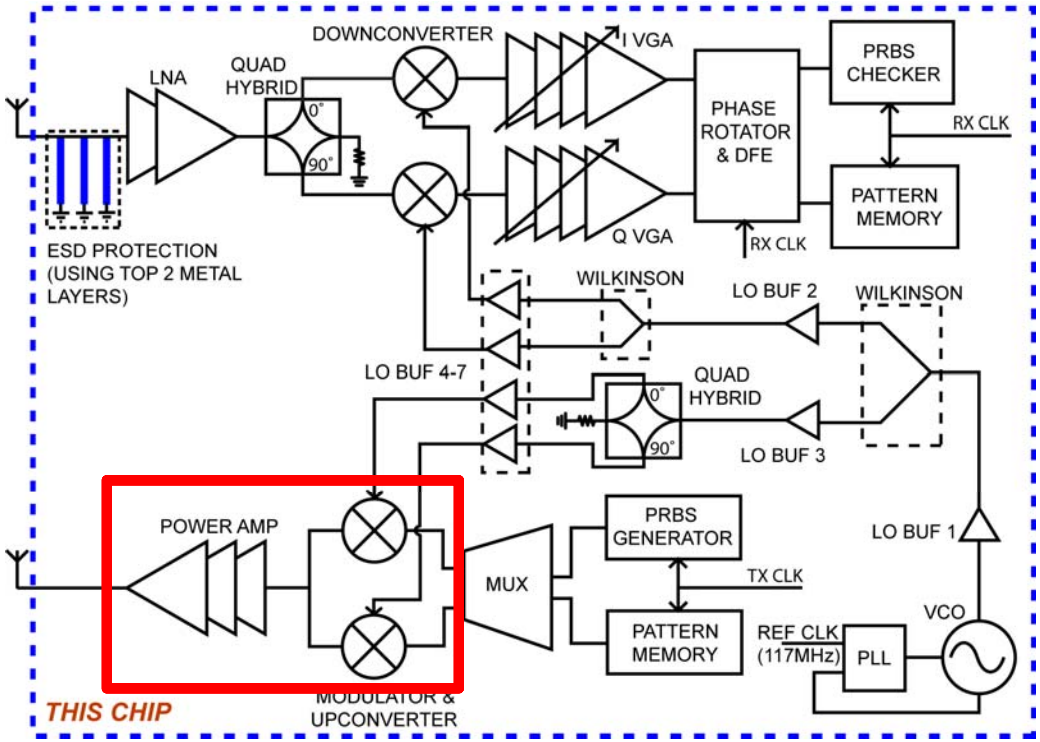

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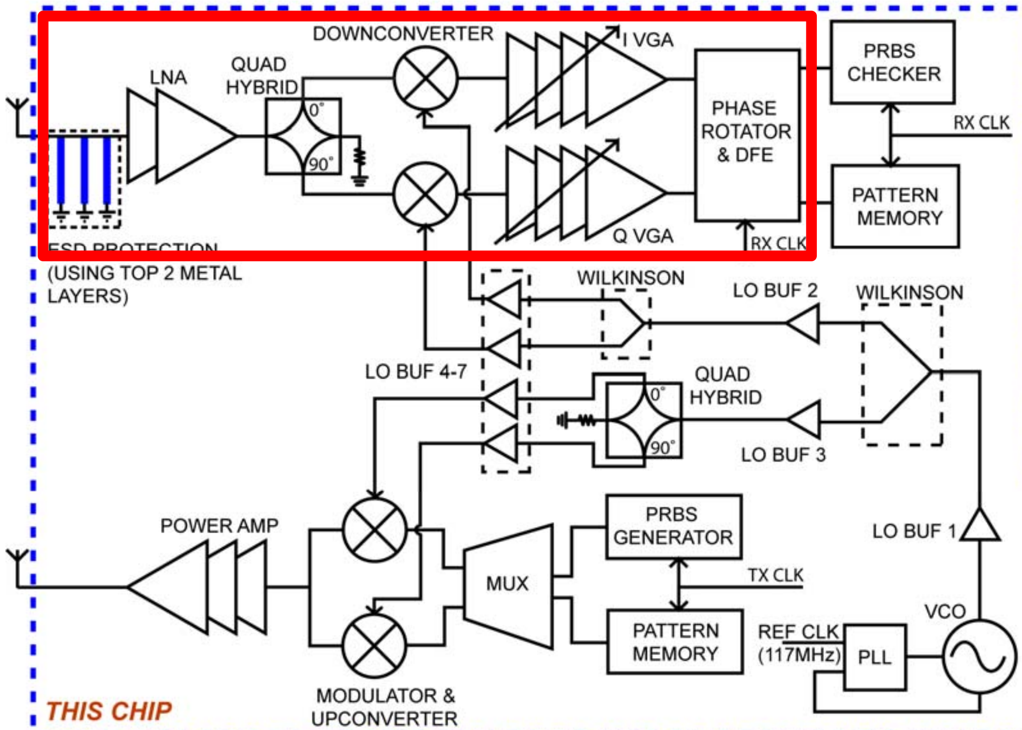

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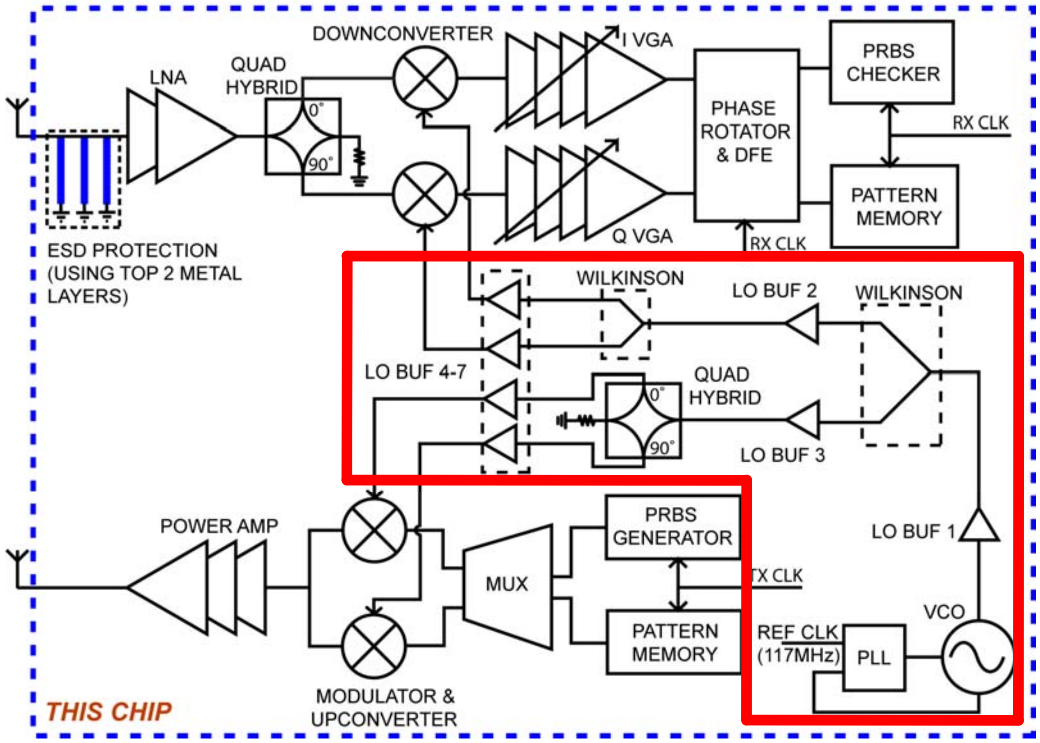

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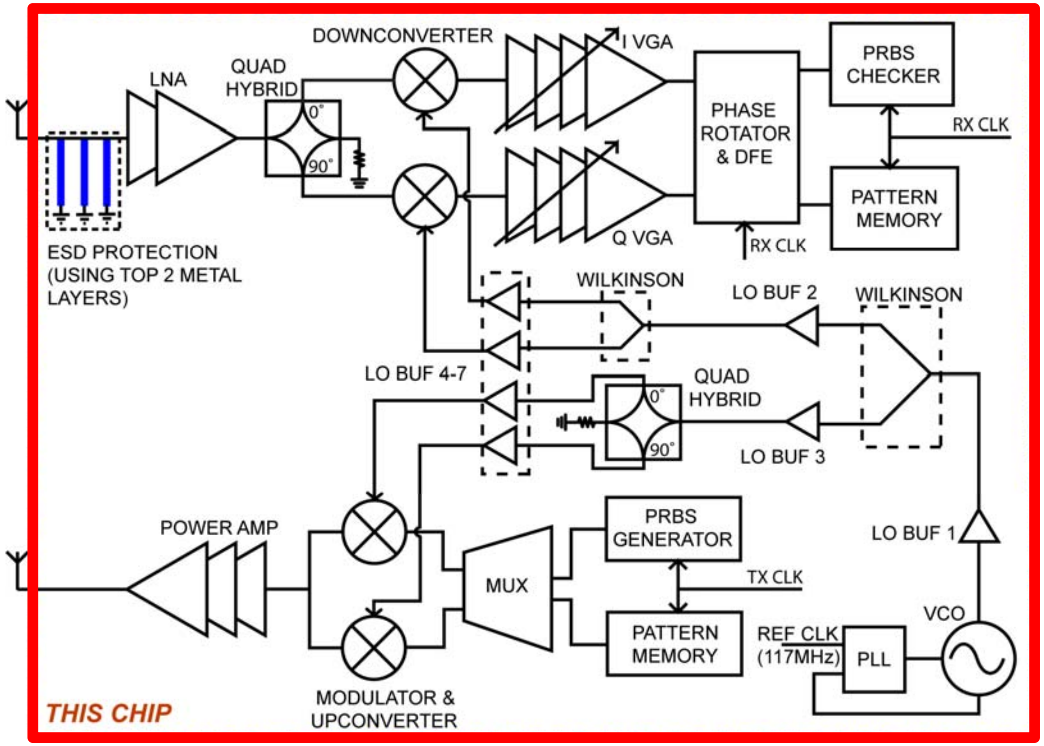
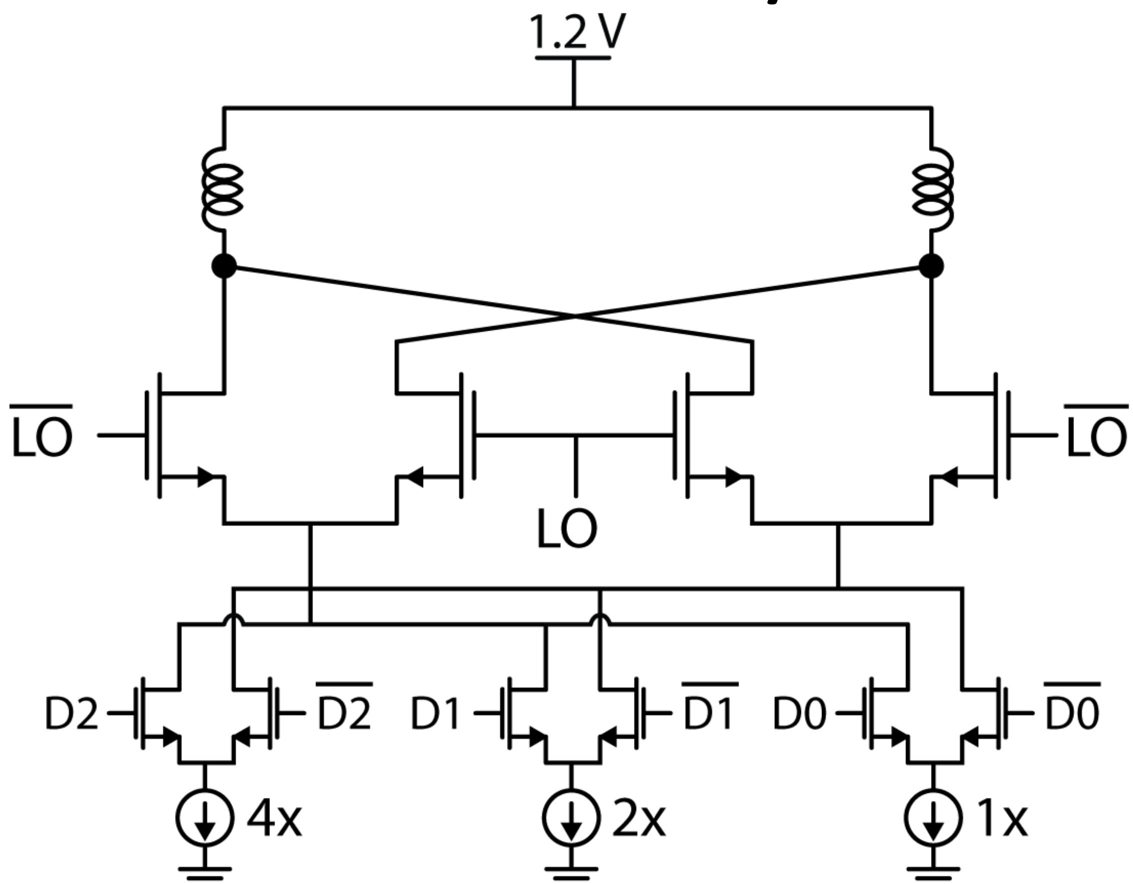


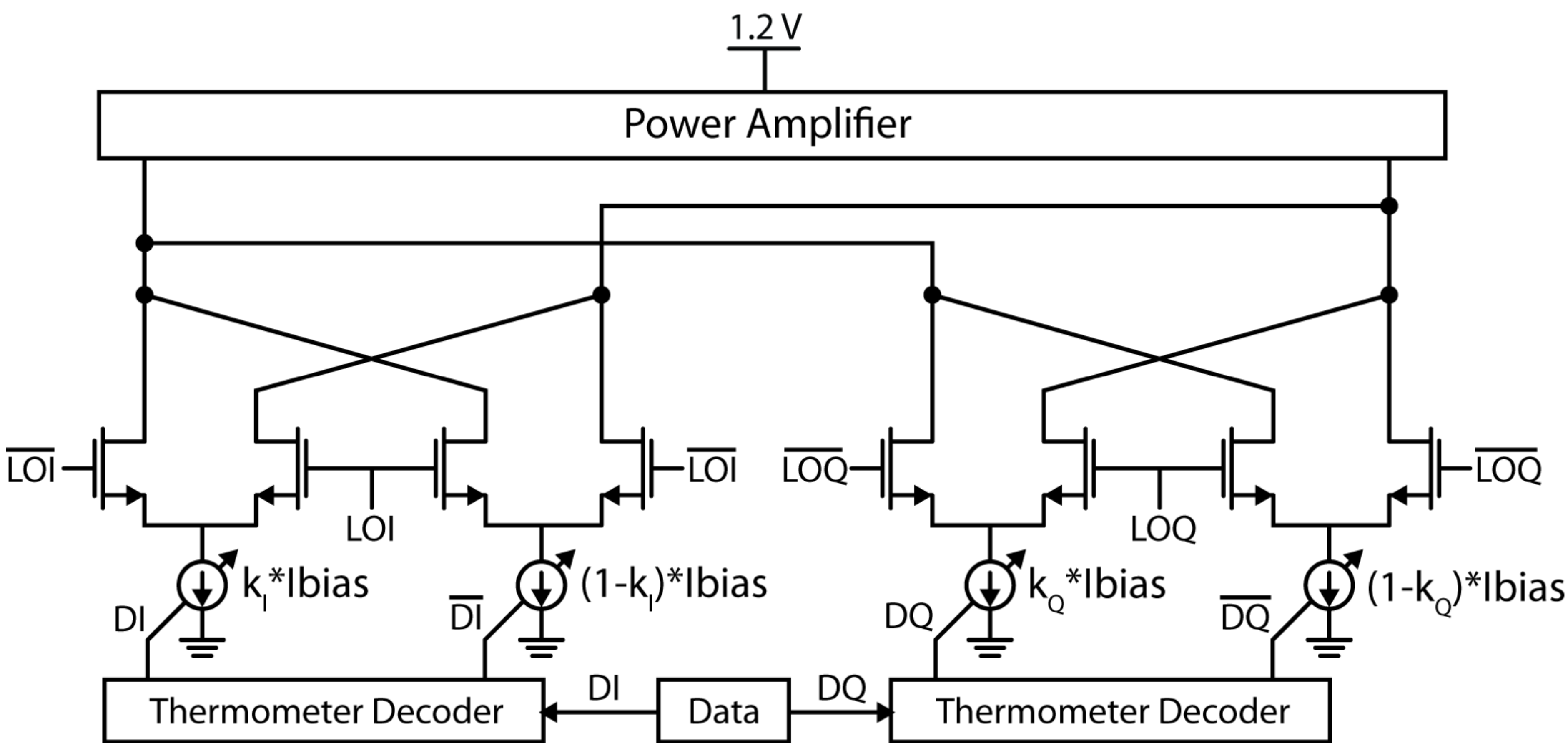
Combined DAC/Mixer



- Target: 5GS/s, 3-bit combined DAC/Mixer
  - Bias current set by swing needed at output

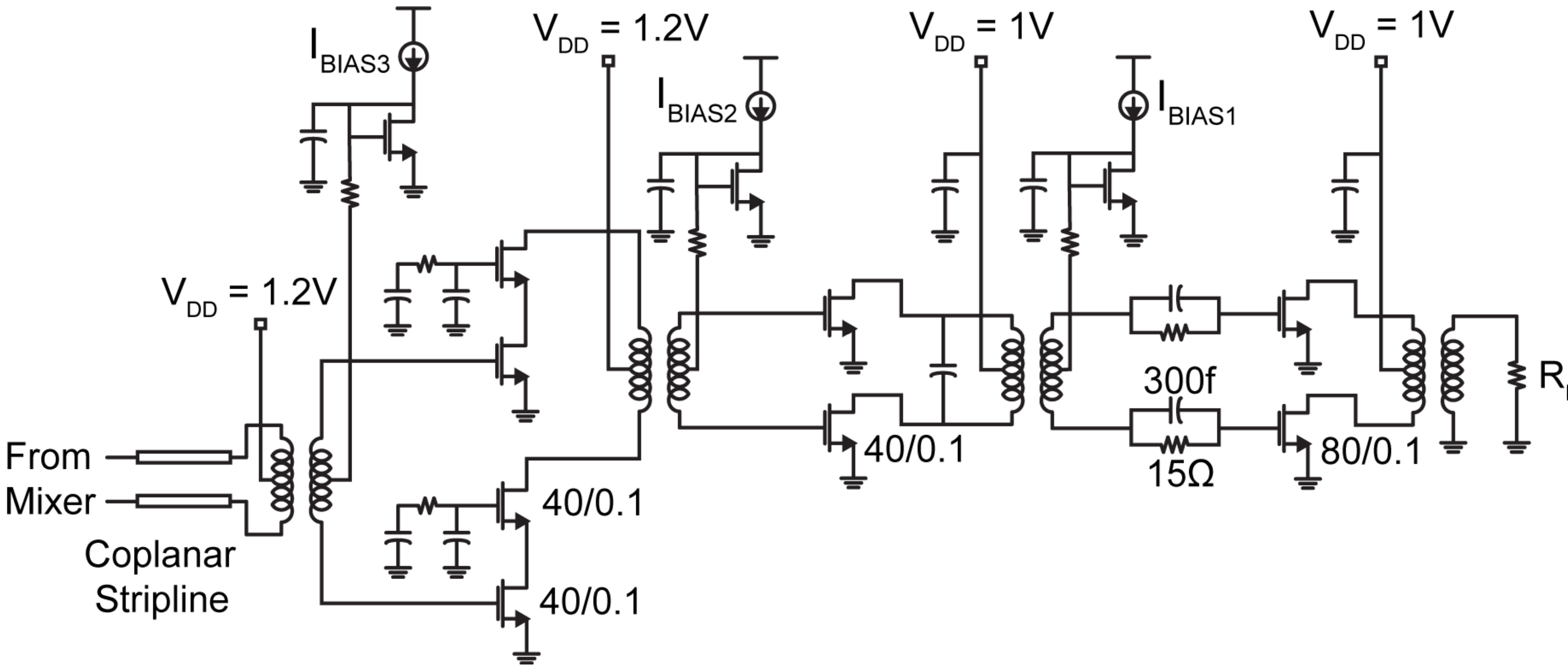
Ref: S. Luschas et al, JSSCC 2004.

DAC and Up-Conversion Mixer



- Current mode summation of I and Q mixers challenging at 60GHz

Power Amplifier

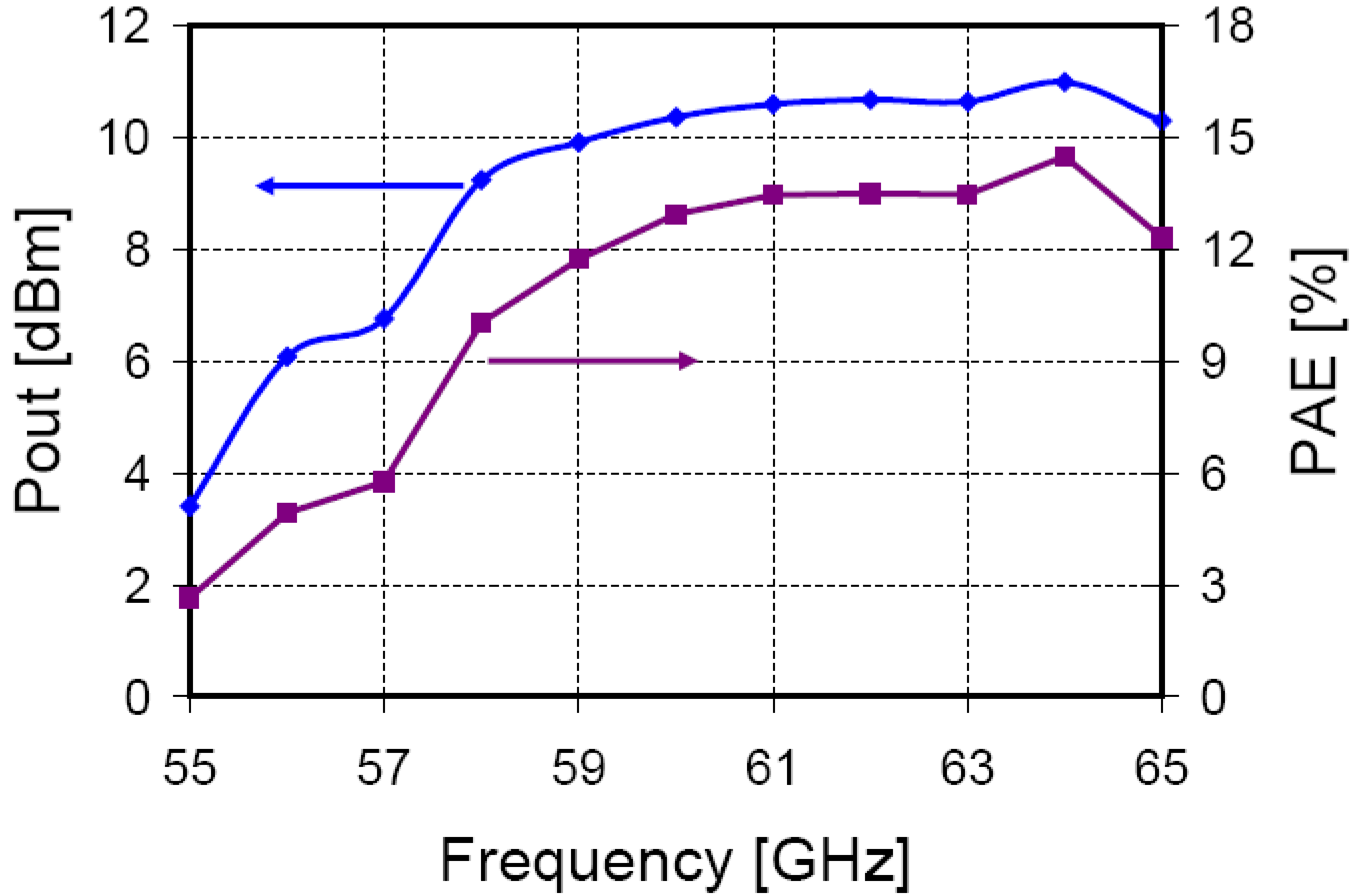


- Coplanar stripline and transformer based input matching network to present low impedance to mixer
- Optimized driver stages for higher power gain
- Output transformer adds inherent ESD protection
- Successfully tested protection using MM up to 400V

Ref: D. Chowdhury et al, ISSCC 2008.

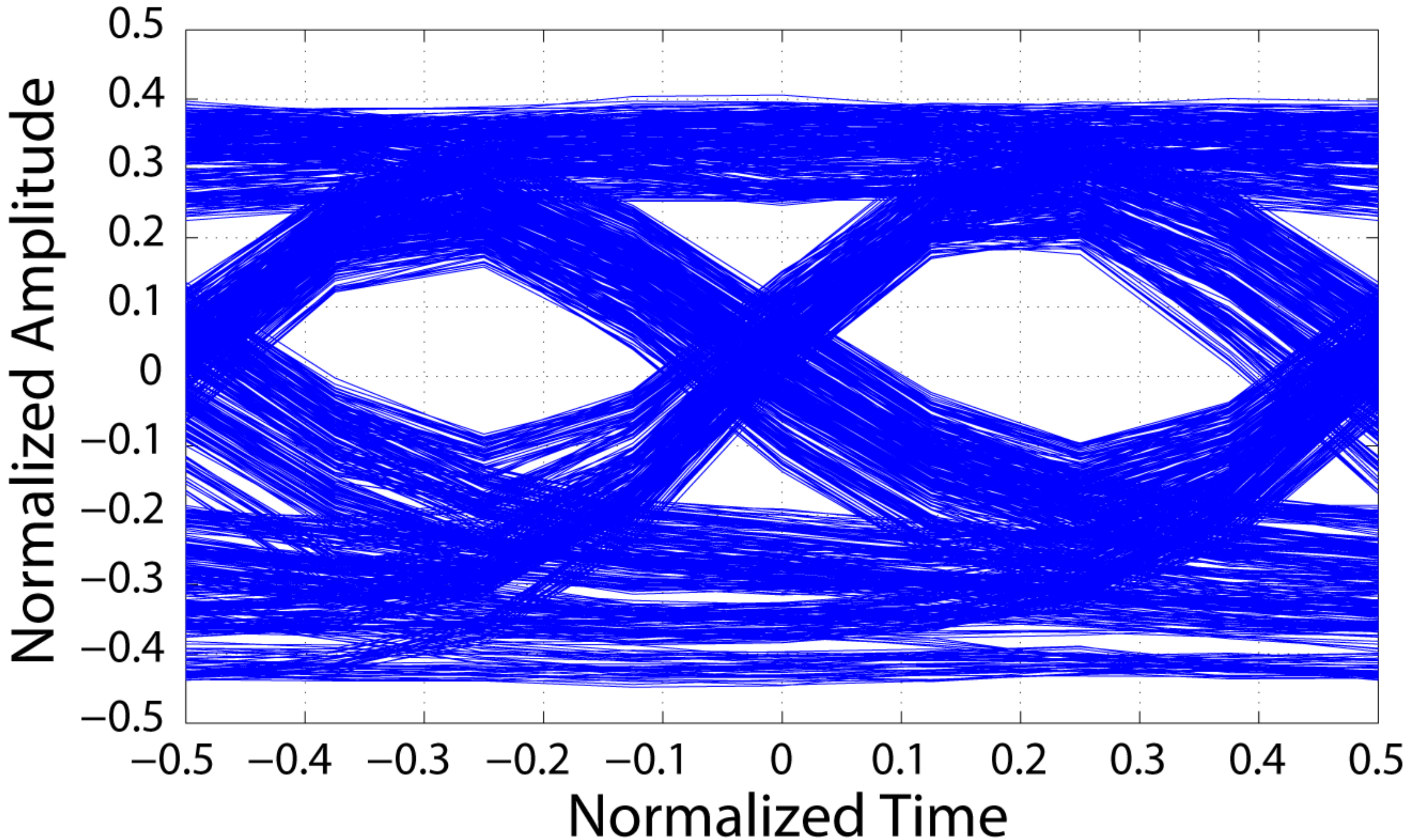
Transmitter Measurement

- Peak Pout=11dBm with 14.6% PA efficiency



Transmit Eye Diagram

- Measured I-channel transmit eye diagram at 5GS/s



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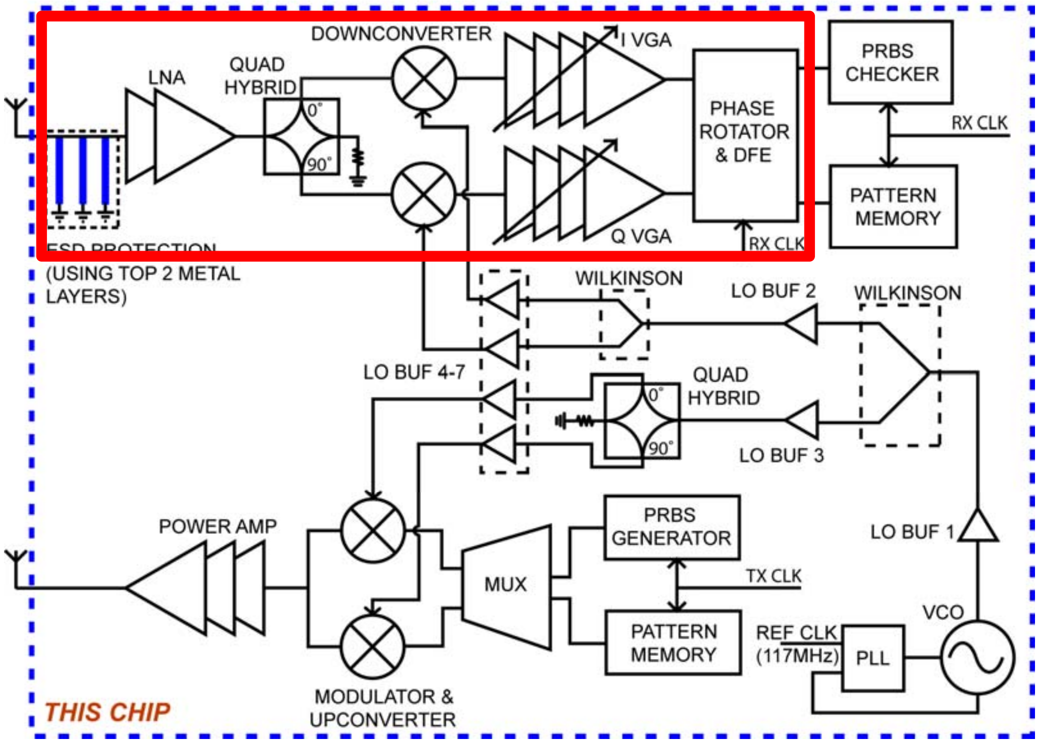
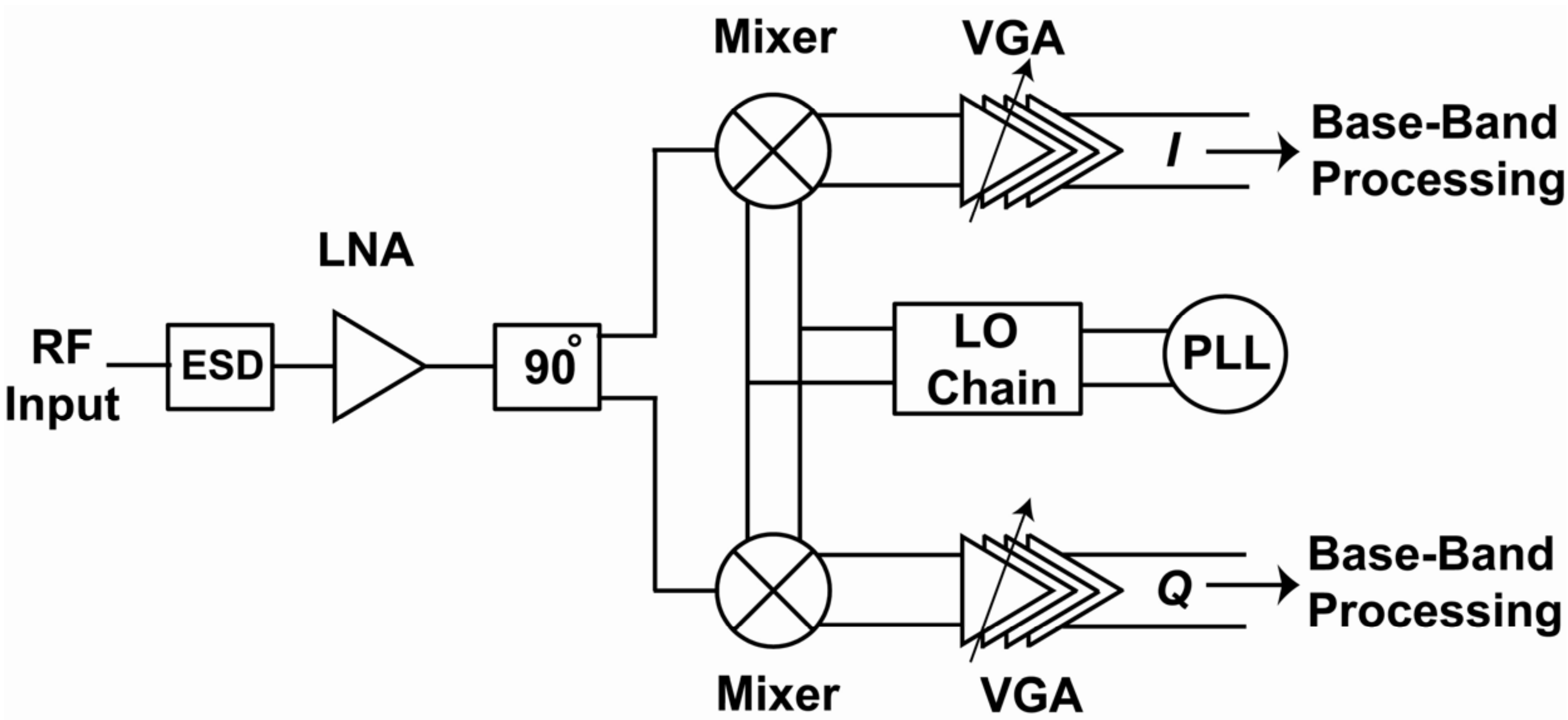


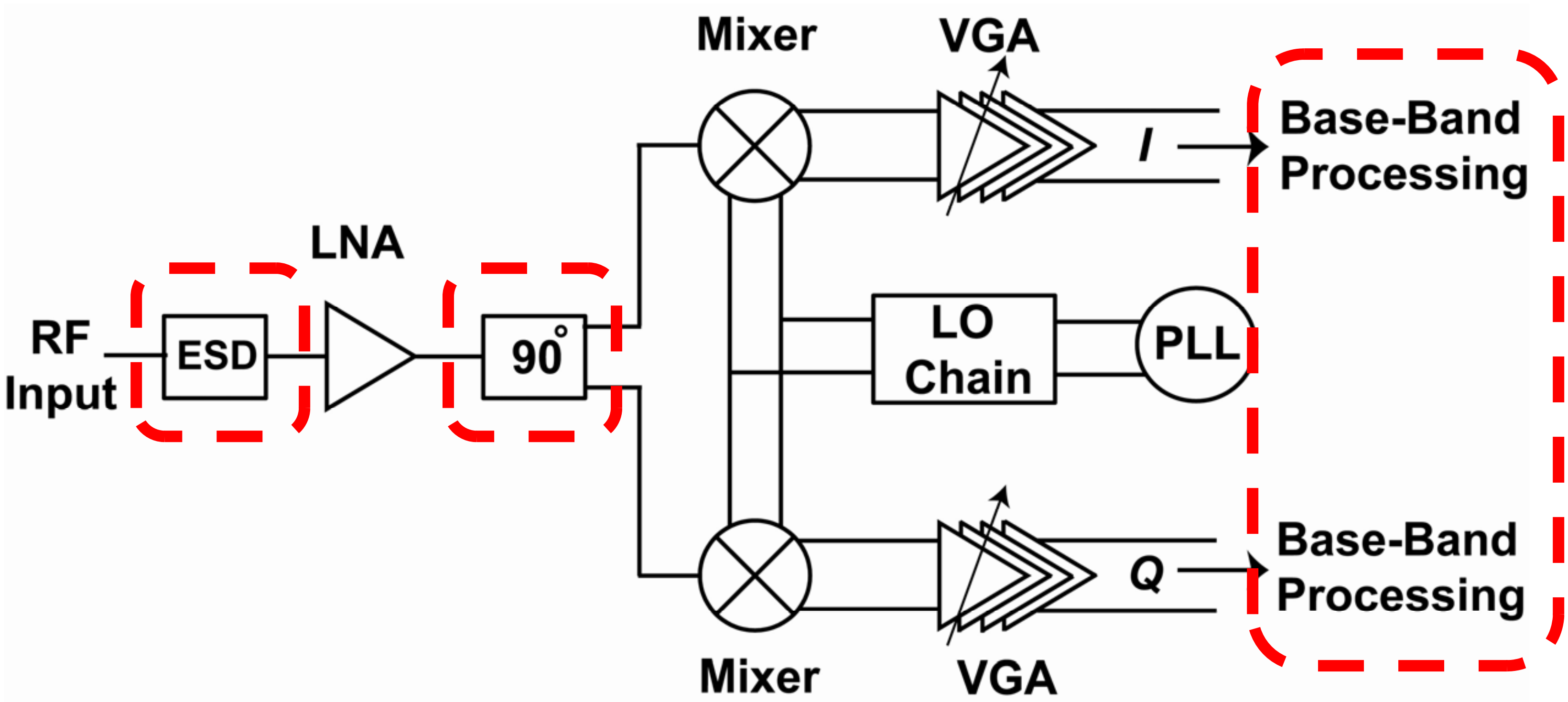
Receiver



- Direct conversion receiver
  - Hybrid for quadrature separation in the signal path
  - ESD protected LNA

Ref: B. Afshar et al, ISSCC 2008.

Receiver



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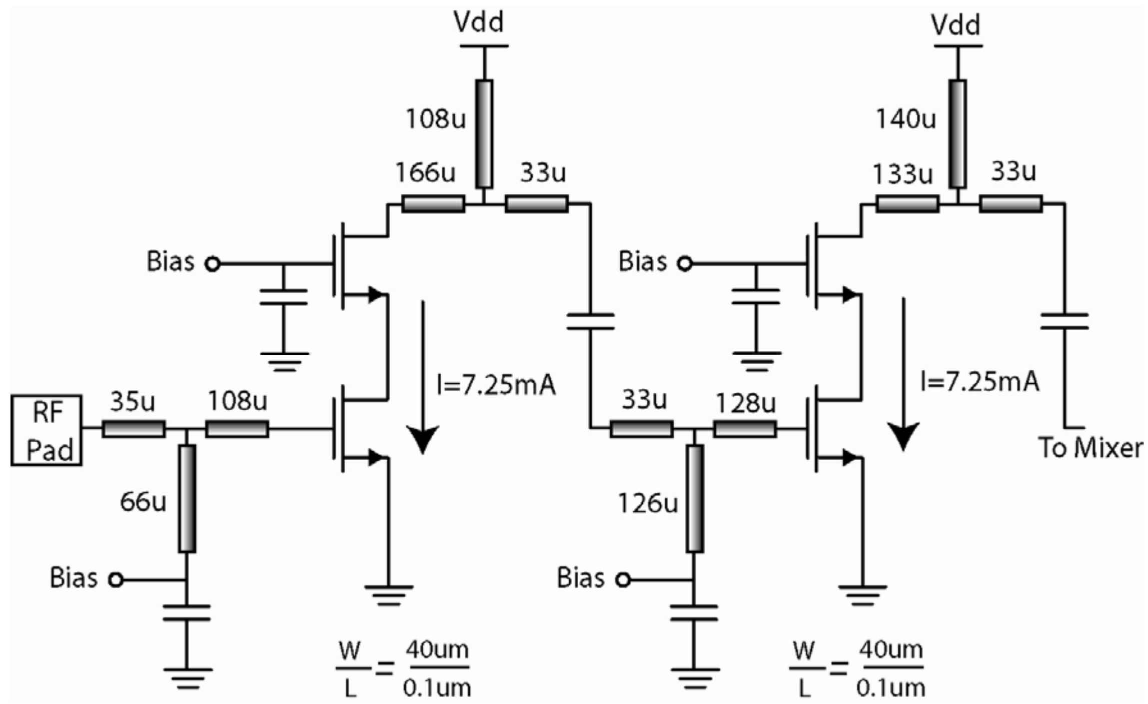
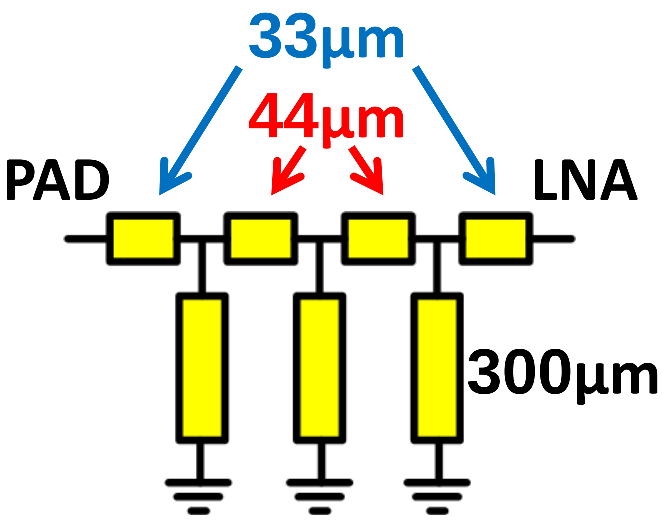
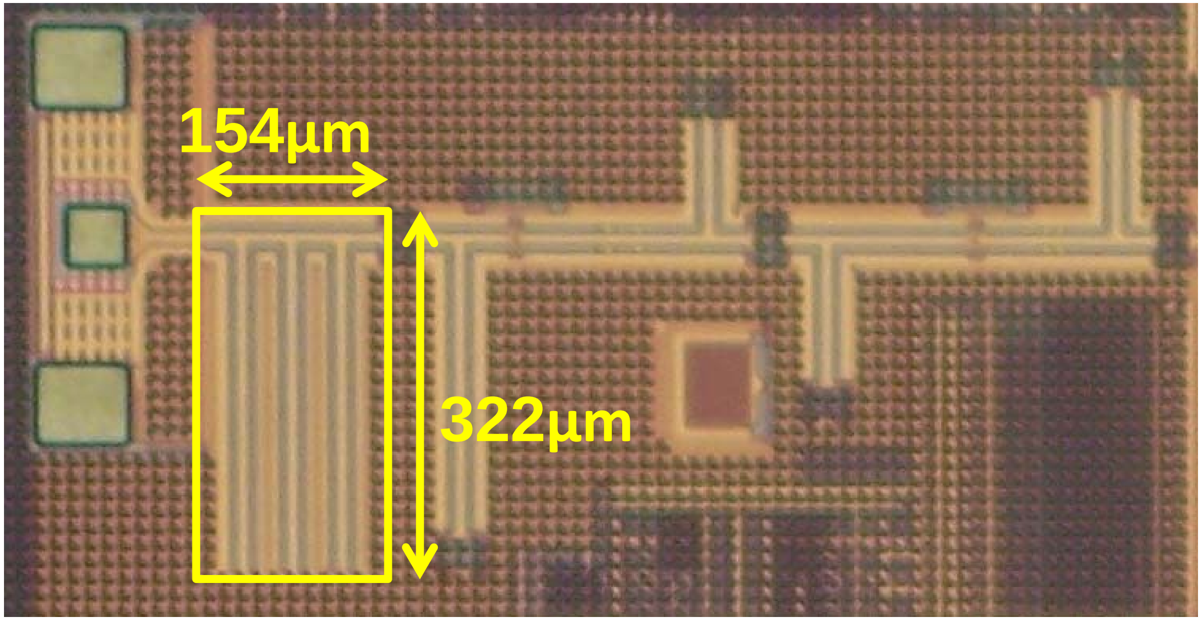
Original LNA Design



- Two stage cascode LNA
  - Unconditionally stable at 60GHz
  - High maximum available gain and isolation
- CPW transmission lines with Z0 =50.8Ω
- Power consumption from 1.2V supply: 17mW

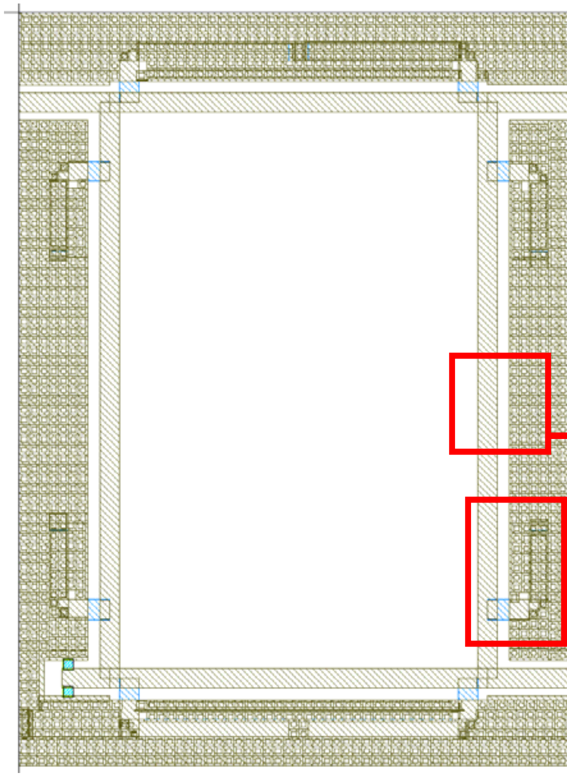
LNA ESD Protection





- ESD desirable to enable packaging
  - At 60GHz ESD diodes too lossy
- Proposed ESD protection circuit :
  - Triple-shunt stub to GND merged into input matching circuit
  - Simulated insertion loss <0.7 dB
  - Successfully tested protection using MM up to 400V

Size-reduced Hybrid with C Loading



- Shorter length (θ) → high C and Z_0

$$C = \frac{\cos\theta}{\omega Z_{o,MSTL}} \qquad \theta = \sin^{-1}\left(\frac{Z_{o,CPW}}{Z}\right)$$

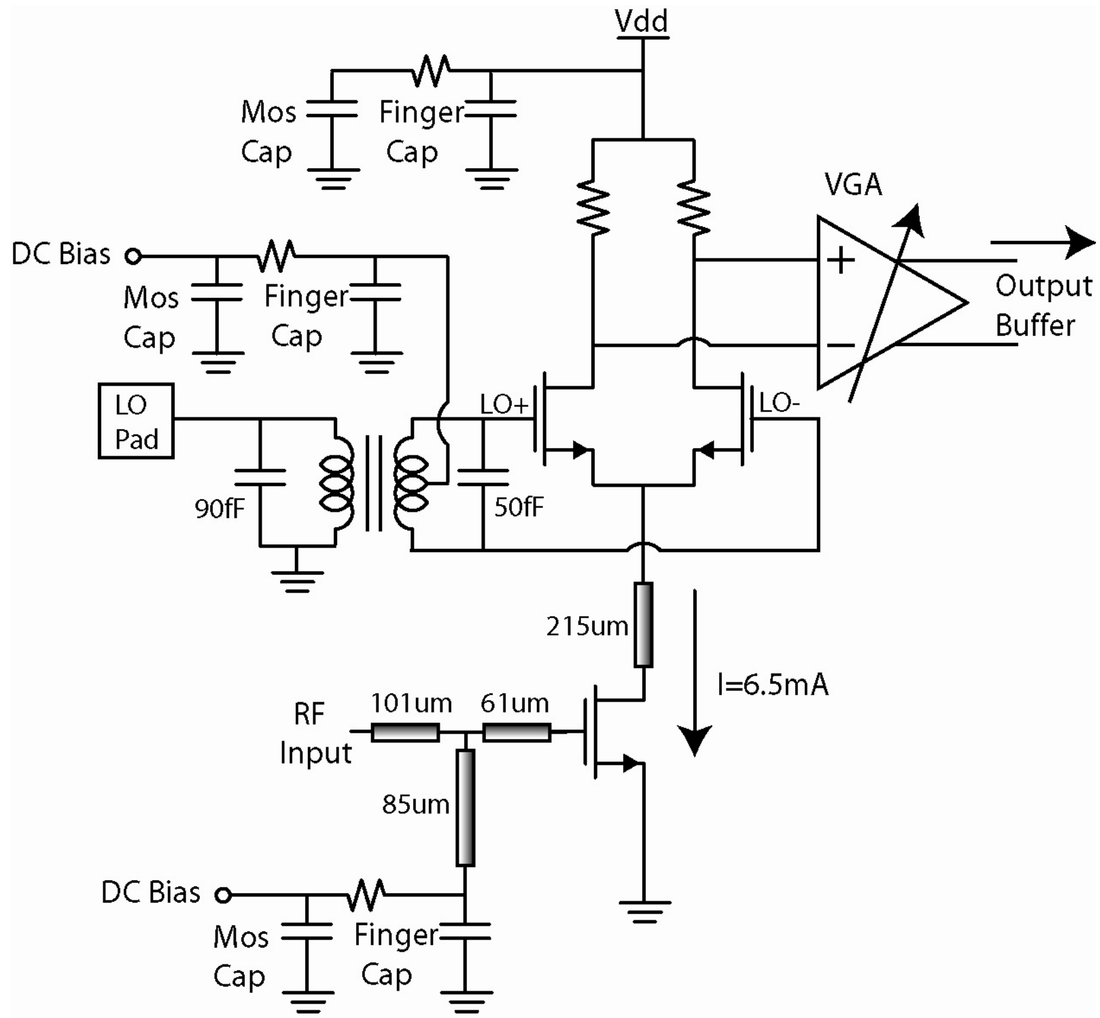
Asymmetric CPW for a high $Z_{0,CPW}$

MSTL shunt-stubs for C loading

- Size = 355um×254um (80% area reduction)
- Simulated insertion loss ≈ 2dB
- Simulated in-band gain mismatch < 0.5dB, phase mismatch < 4°

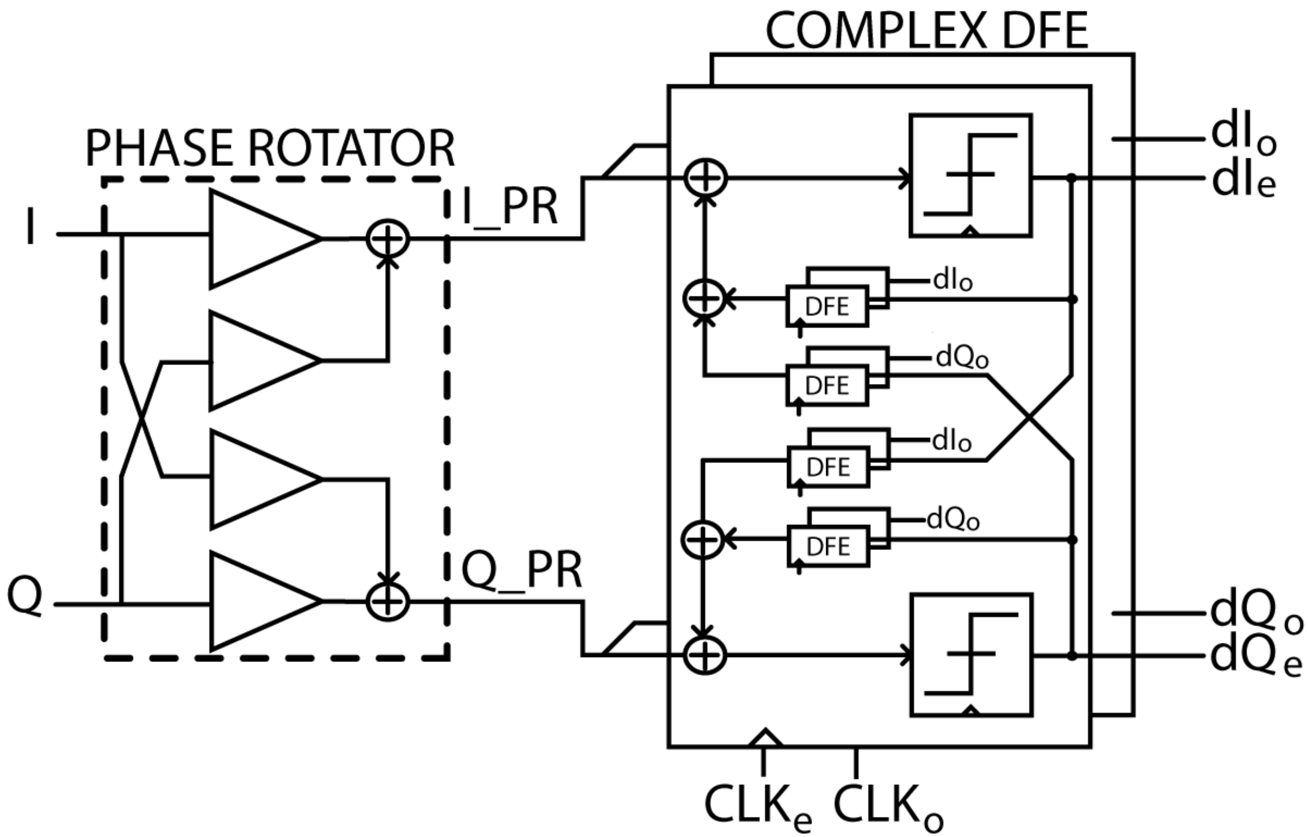
Downconversion Mixer

- Single balanced mixer
- On-chip tuned balun
- Balun center tap provides convenient gate bias point
- Gain enhancement tuning network between g_m stage and switches
- Power consumption from 1.2V supply: 6.5mW



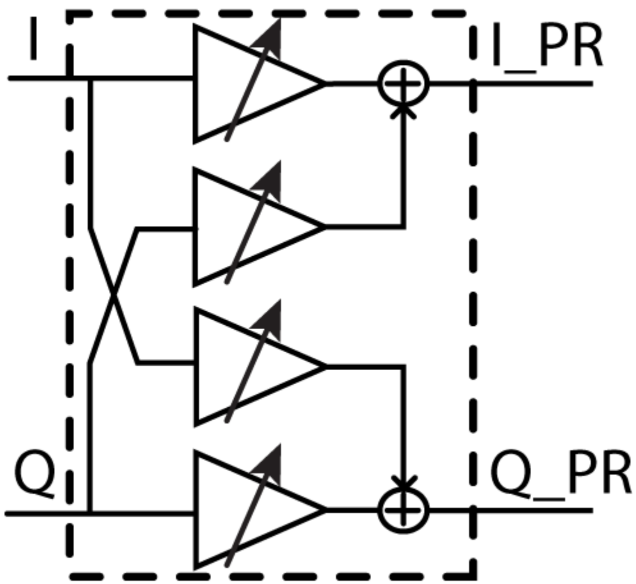
Base-Band Design

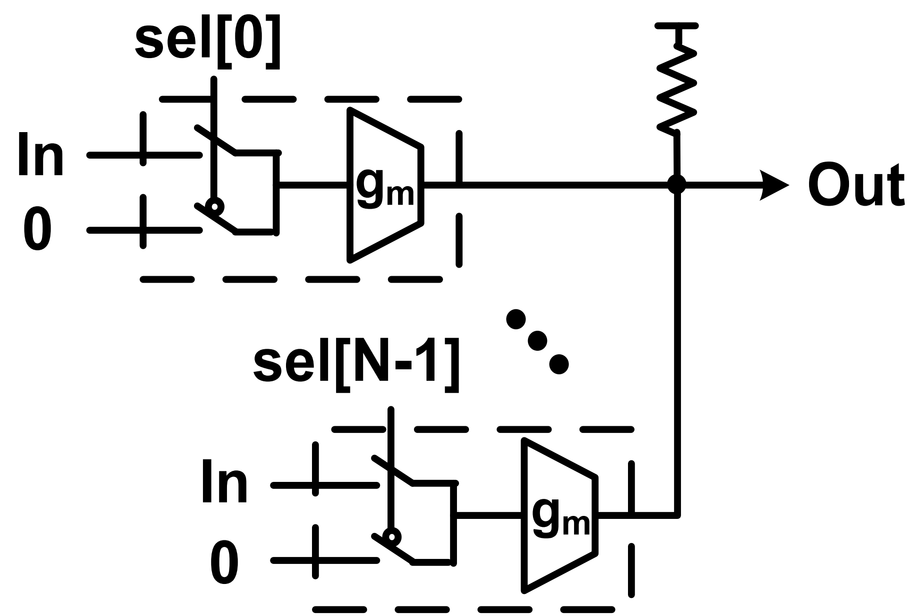
- Traditional ADC/DSP inefficient at GHz bandwidths
  - 100's of mW for DAC, ADC, …
- High-speed electrical link-based approach
  - Mixed-signal phase rotator and 5-tap complex DFE



Phase Rotator

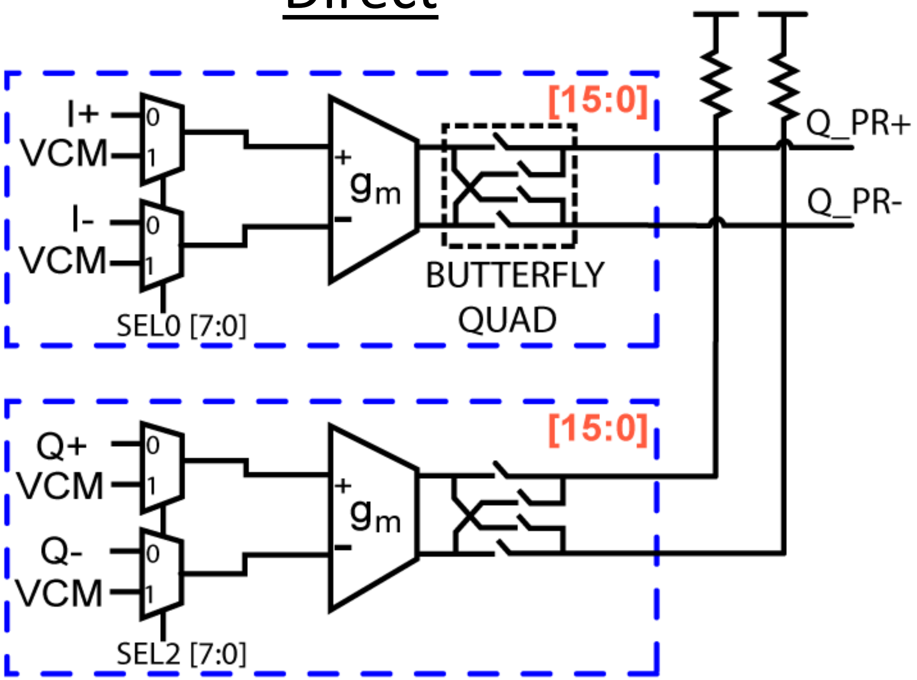
- Phase rotator: 4 digitally controlled VGAs
  - Set gain by switching unit gm cells
  - 4-bit gain control → 16 unit cells/VGA

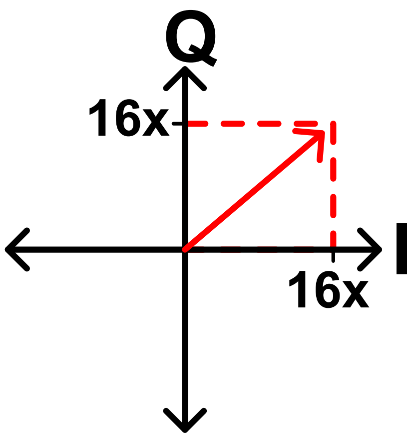




4-bit/Quadrant Phase Rotator

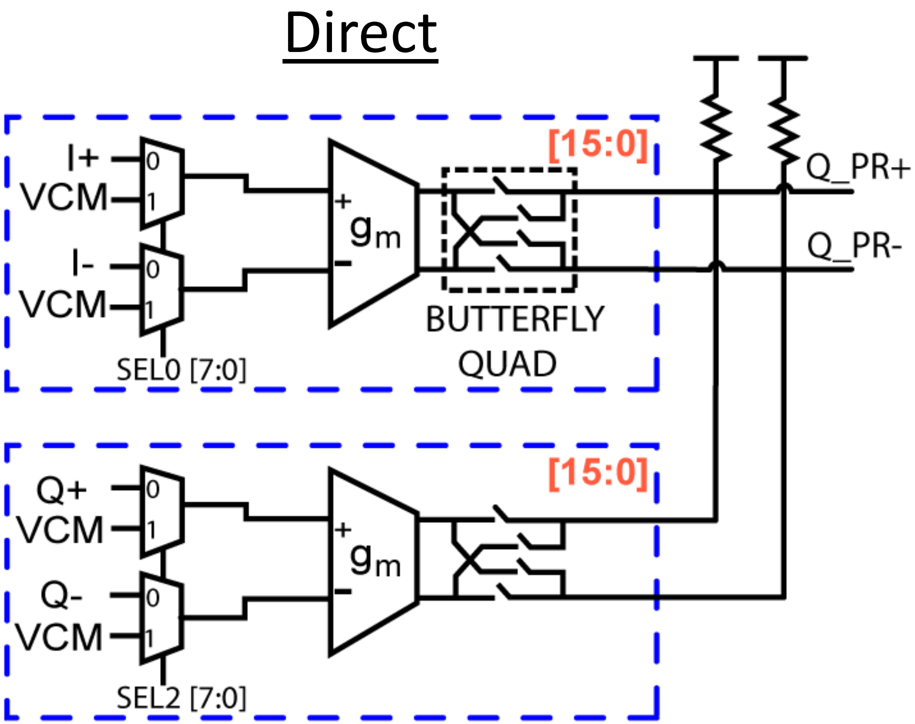
Direct

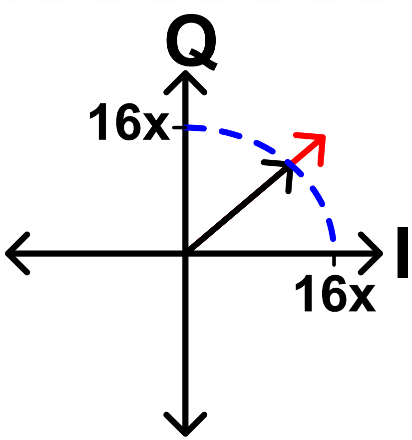


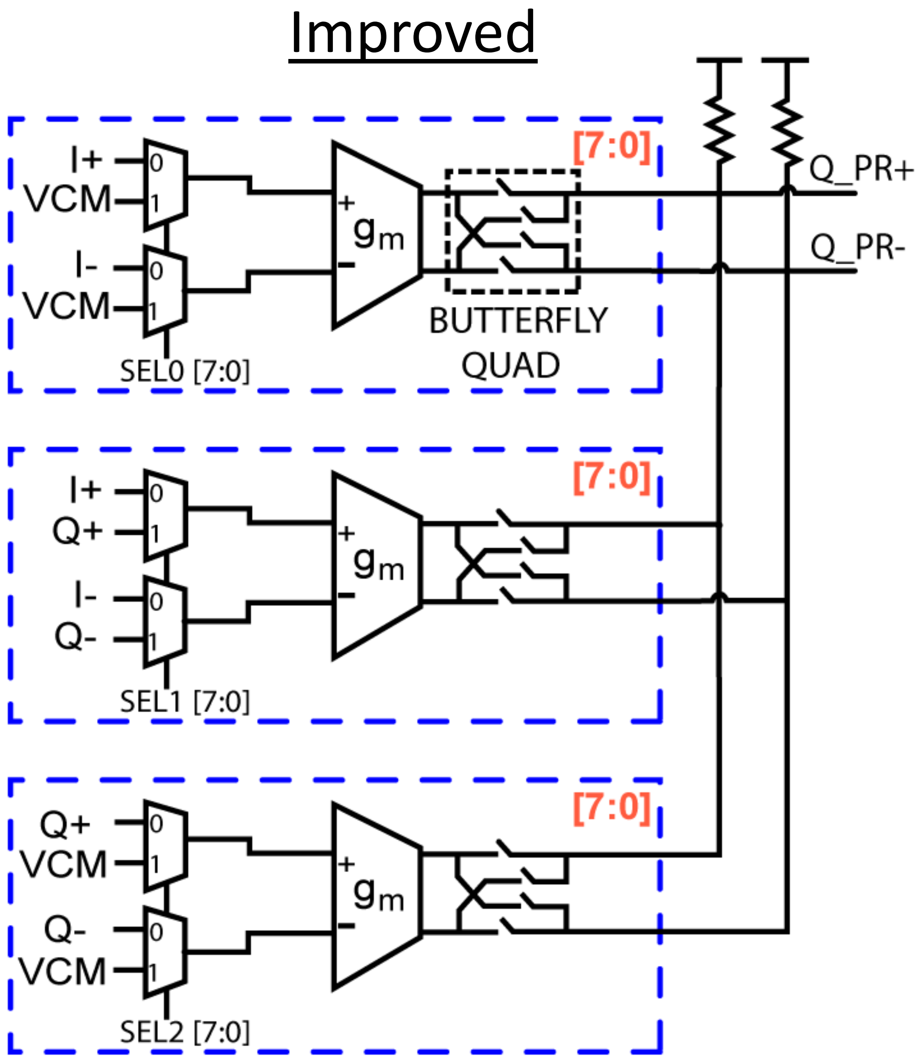


Improved

4-bit/Quadrant Phase Rotator

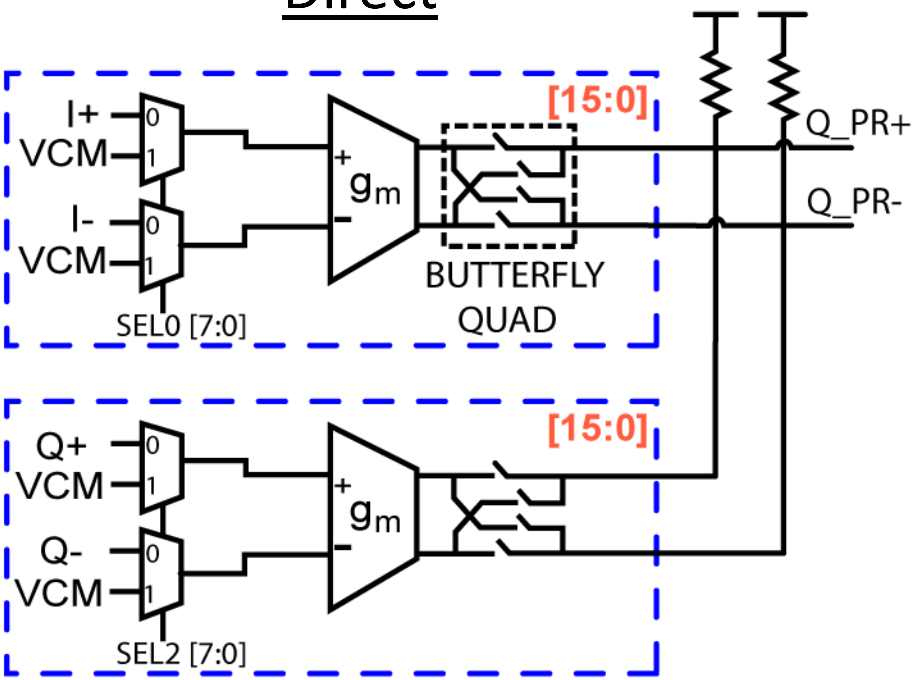




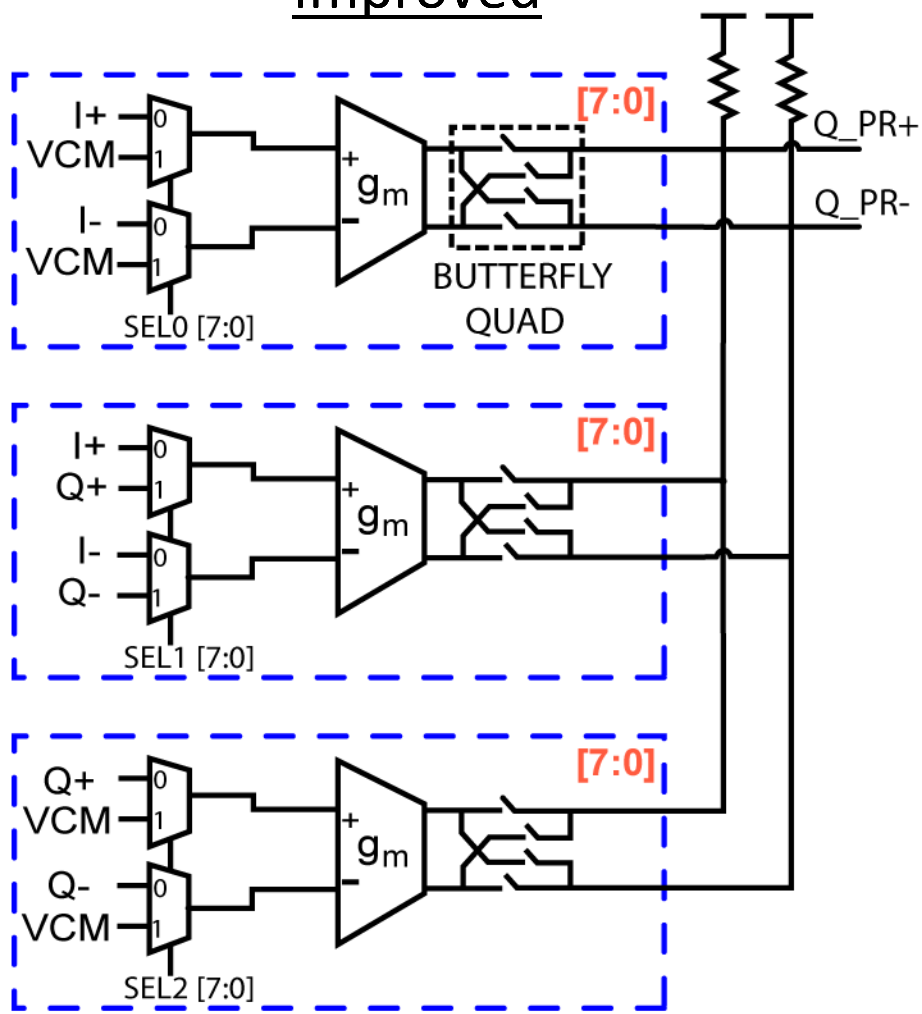


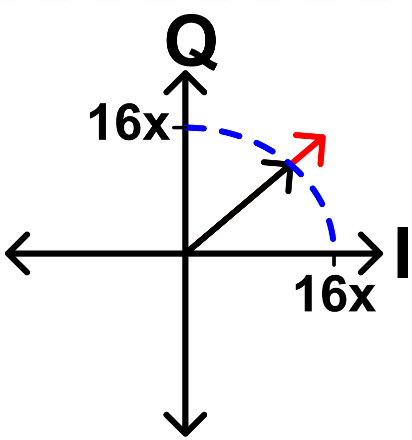
4-bit/Quadrant Phase Rotator

Direct



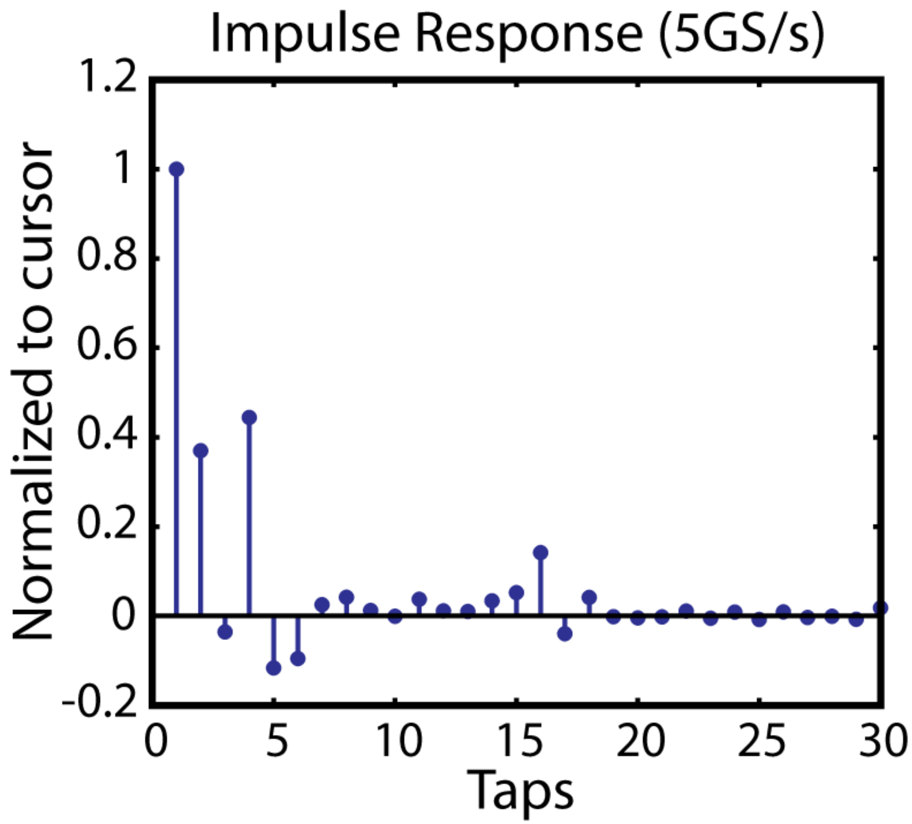
Improved

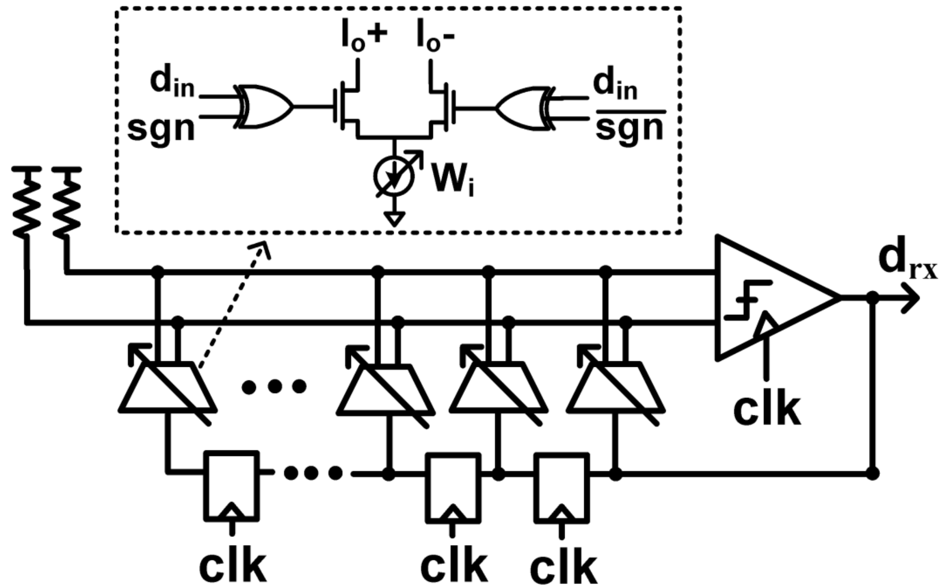




- Sim. BW: >3.5GHz
- Power: 2.2mA @ 1.2V

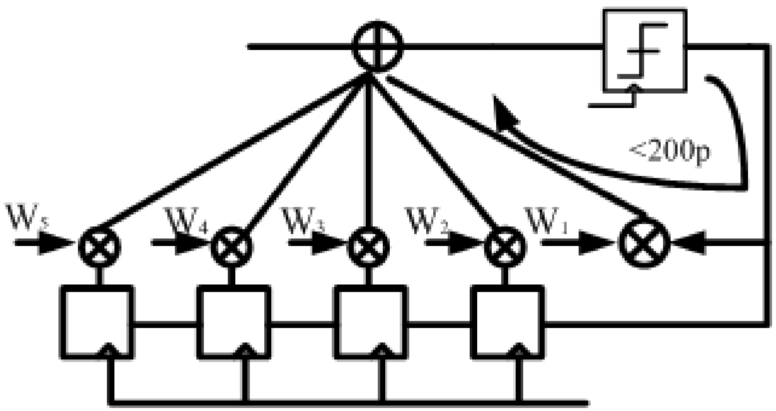
Decision Feedback Equalizer





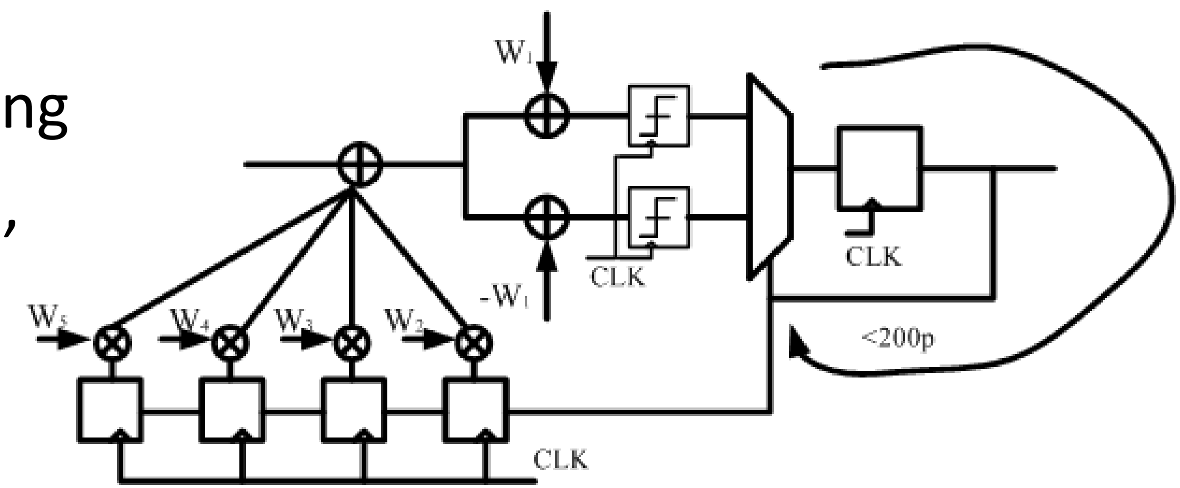
- DFE to compensate for reflections
- FIR summation and weighting in analog domain
- Initial design: 5 taps (5 bits each)

Decision Feedback Equalizer



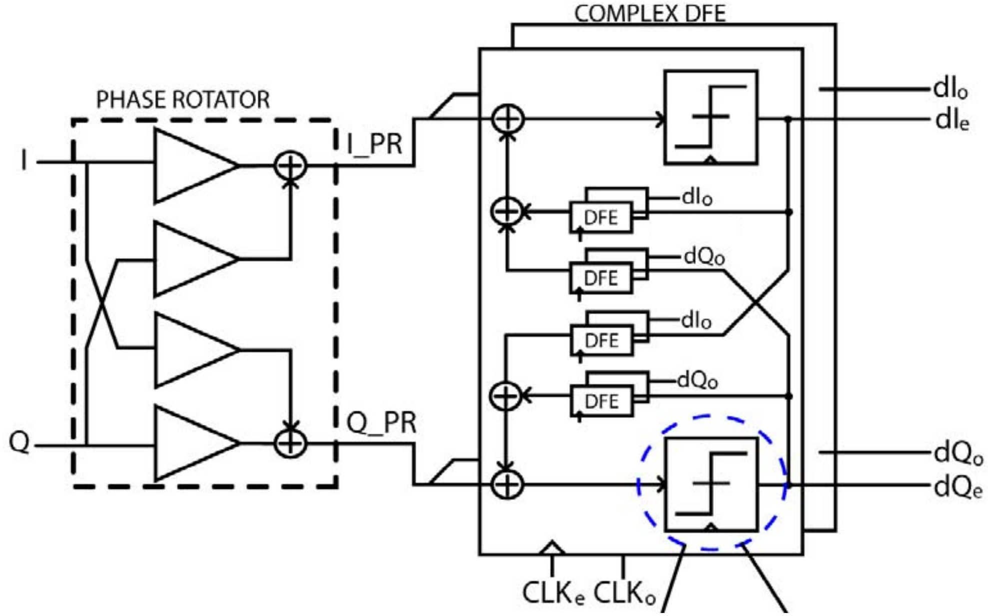
- 1^{st} tap most challenging in mixed-signal DFE
- Resolve-subtract loop < 200ps @ 5GS/s

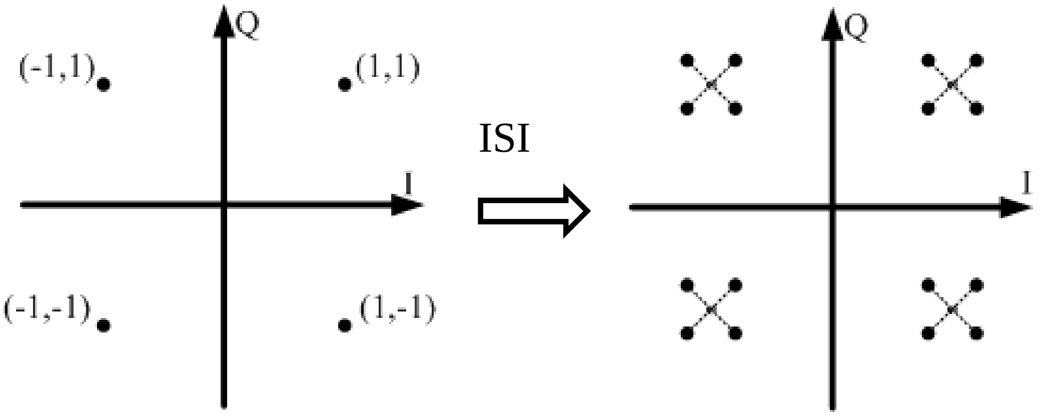
- Solution: loop unrolling
- Resolve both options, then choose
- Moves critical loop into digital domain



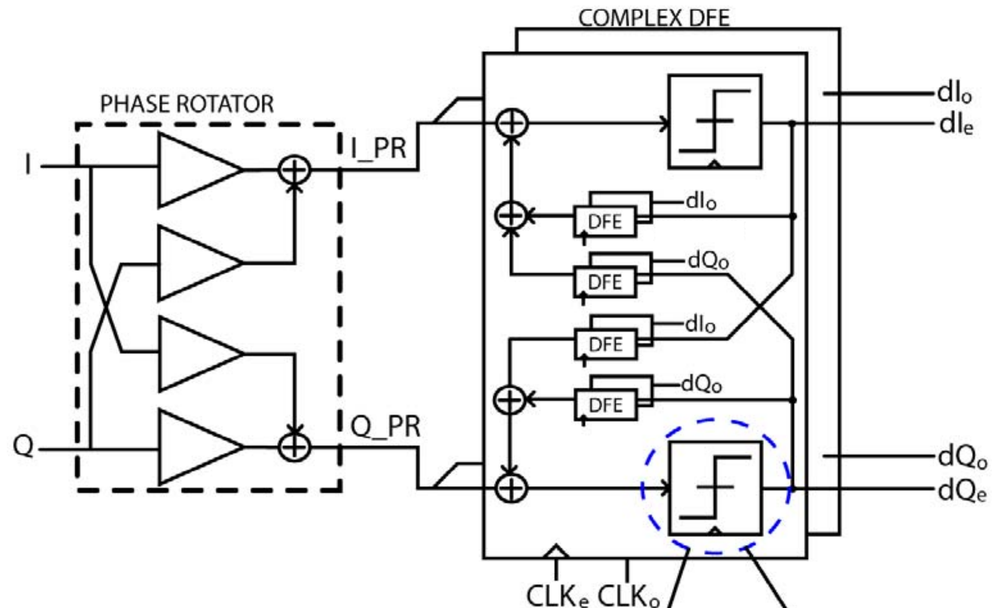
Ref: K.K. Parhi, ISCAS 1990.

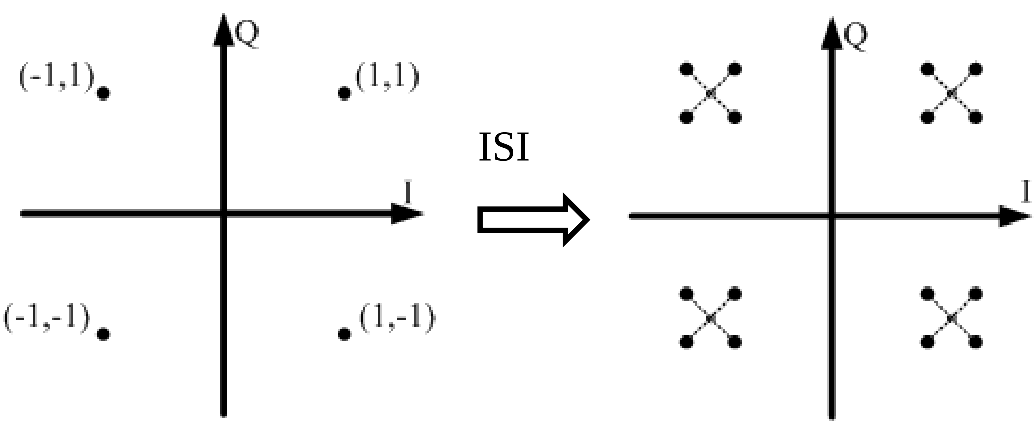
QPSK DFE

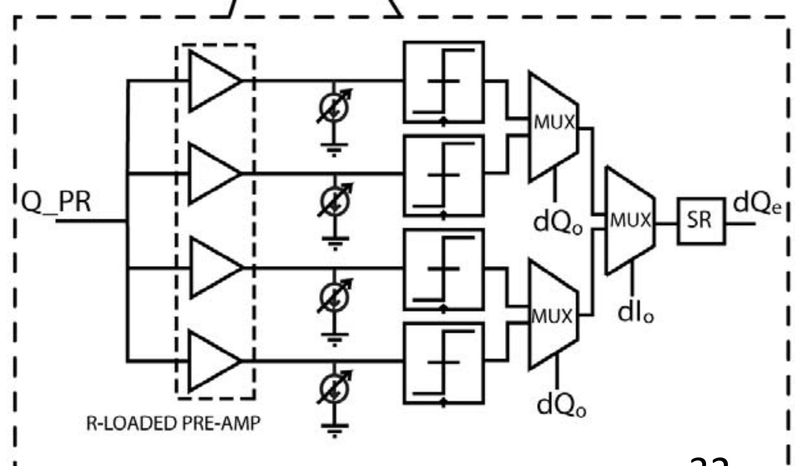

COMPLEX DFE
PHASE ROTATOR
I
Q
I_PR
Q_PR
DFE
dIo
dQo
dIe
dQe
CLKe CLKo


Q
I
(-1,1)
(1,1)
(-1,-1)
(1,-1)
ISI

QPSK DFE

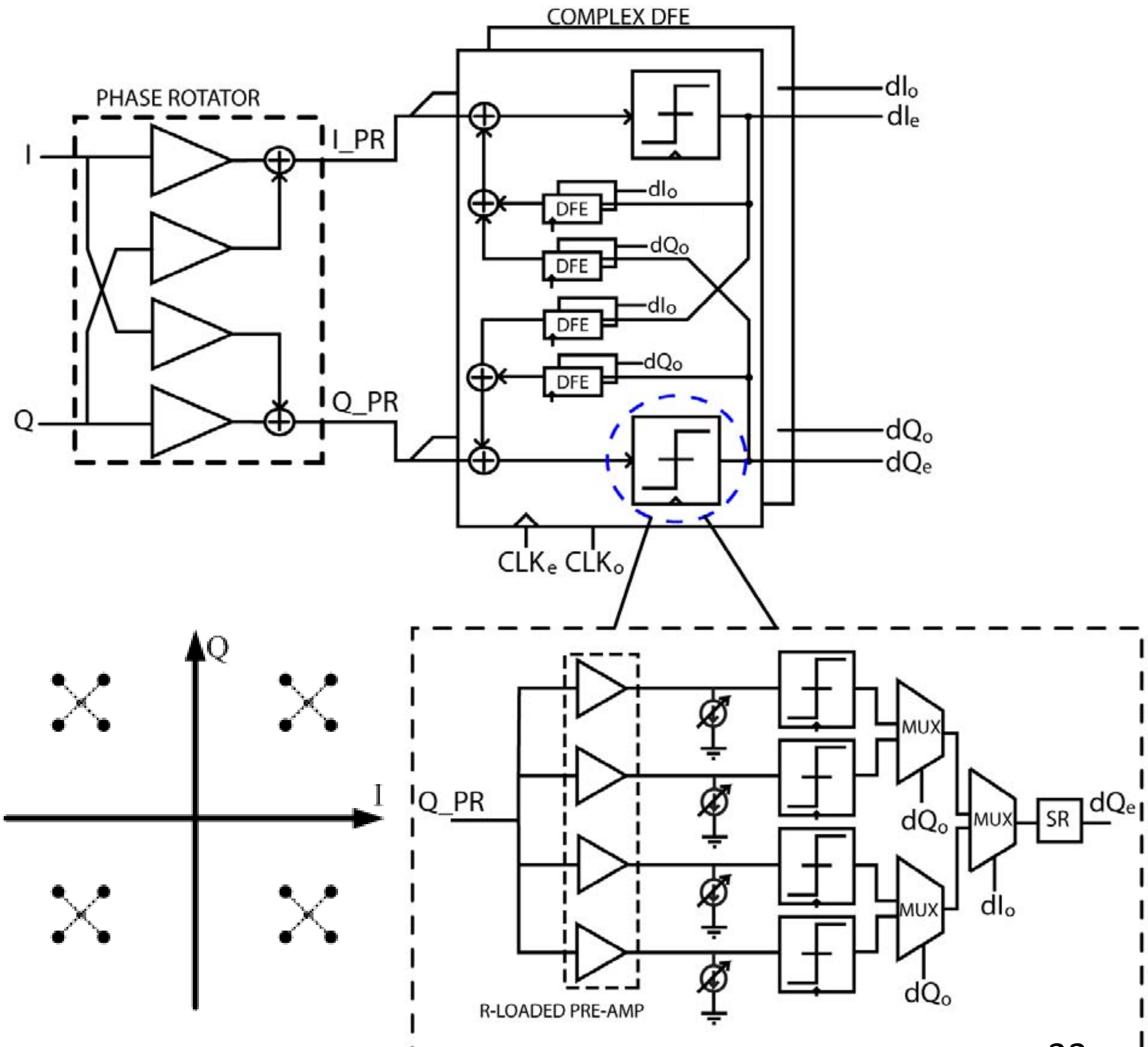

PHASE ROTATOR
I
Q
I_PR
Q_PR
COMPLEX DFE
DFE
dI$_o$
dI$_e$
dQ$_o$
dQ$_e$
CLK$_e$ CLK$_o$

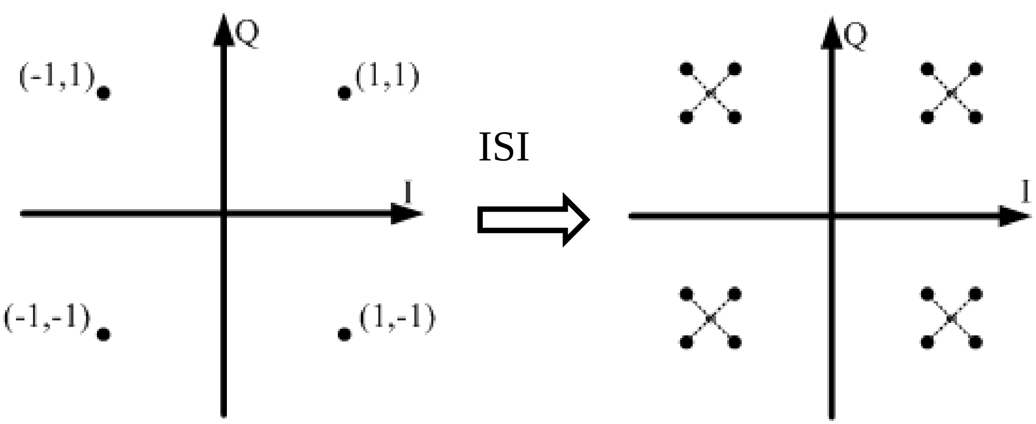

Q
I
(-1,1)
(1,1)
(-1,-1)
(1,-1)
ISI


Q_PR
MUX
SR
dQ$_e$
dQ$_o$
dI$_o$
R-LOADED PRE-AMP

QPSK DFE

Total BB power (measured): 12mW @ 10Gbps





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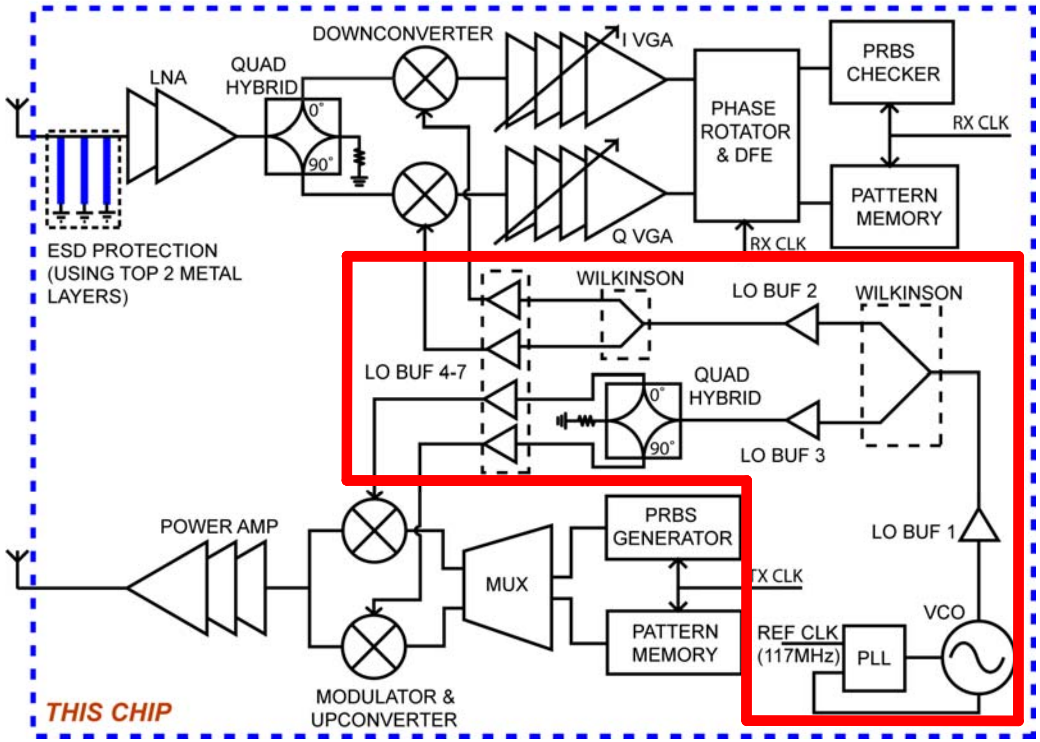
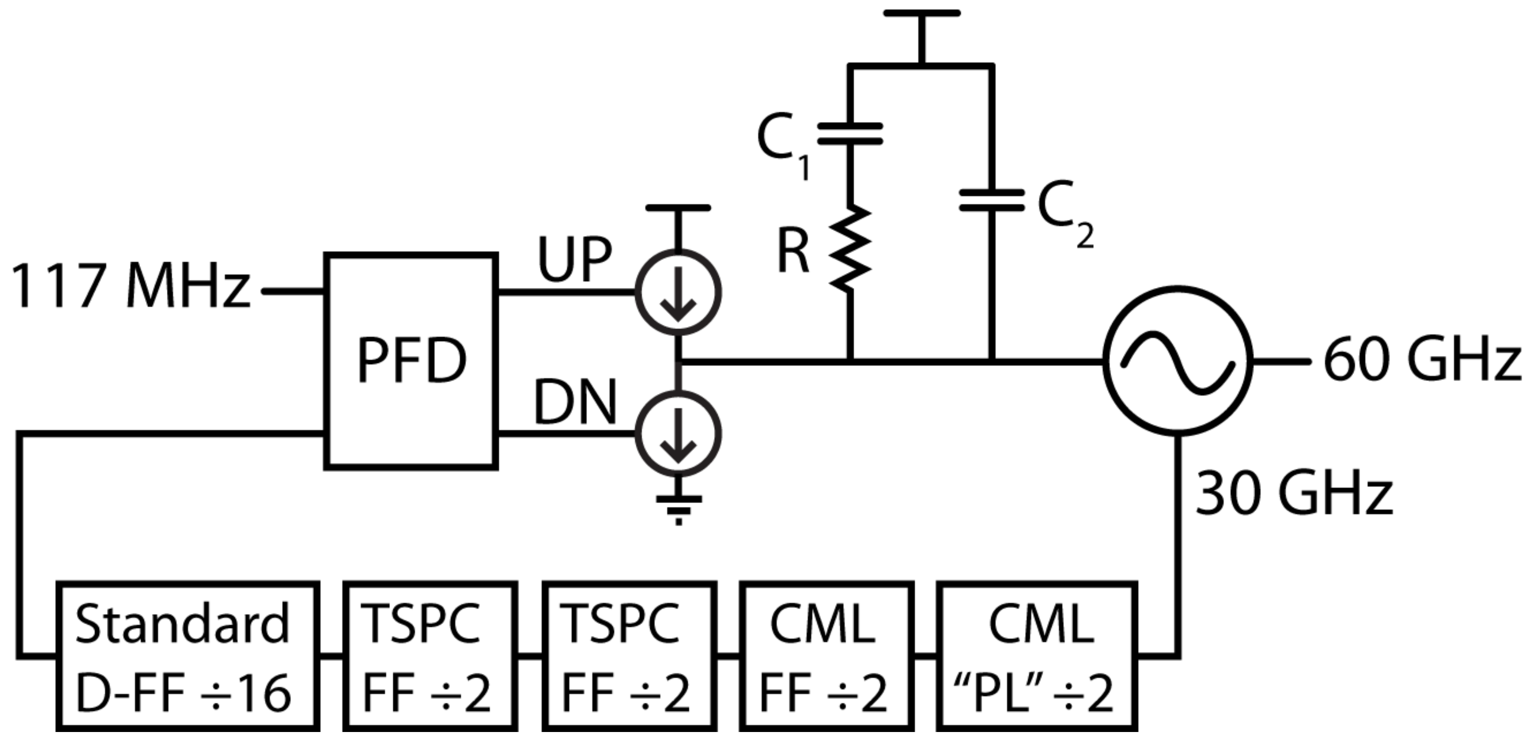
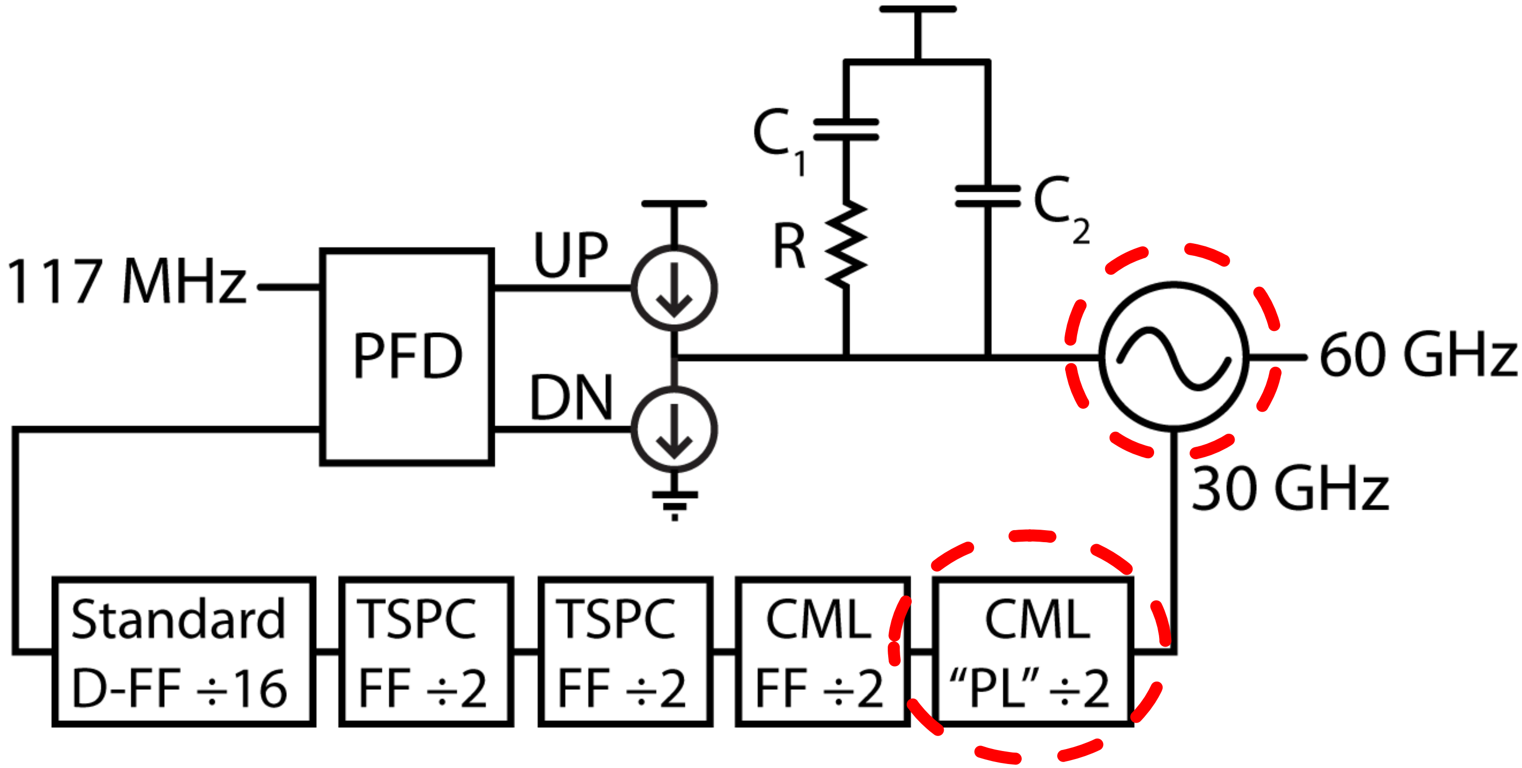


Phase Locked Loop



- Fixed-N, charge pump based PLL
  - Loop BW ≈ 1 MHz
  - Total power: 26.3mW
- F_{REF} ≈ 117 MHz (crystal or MEMS reference feasible)

Phase Locked Loop



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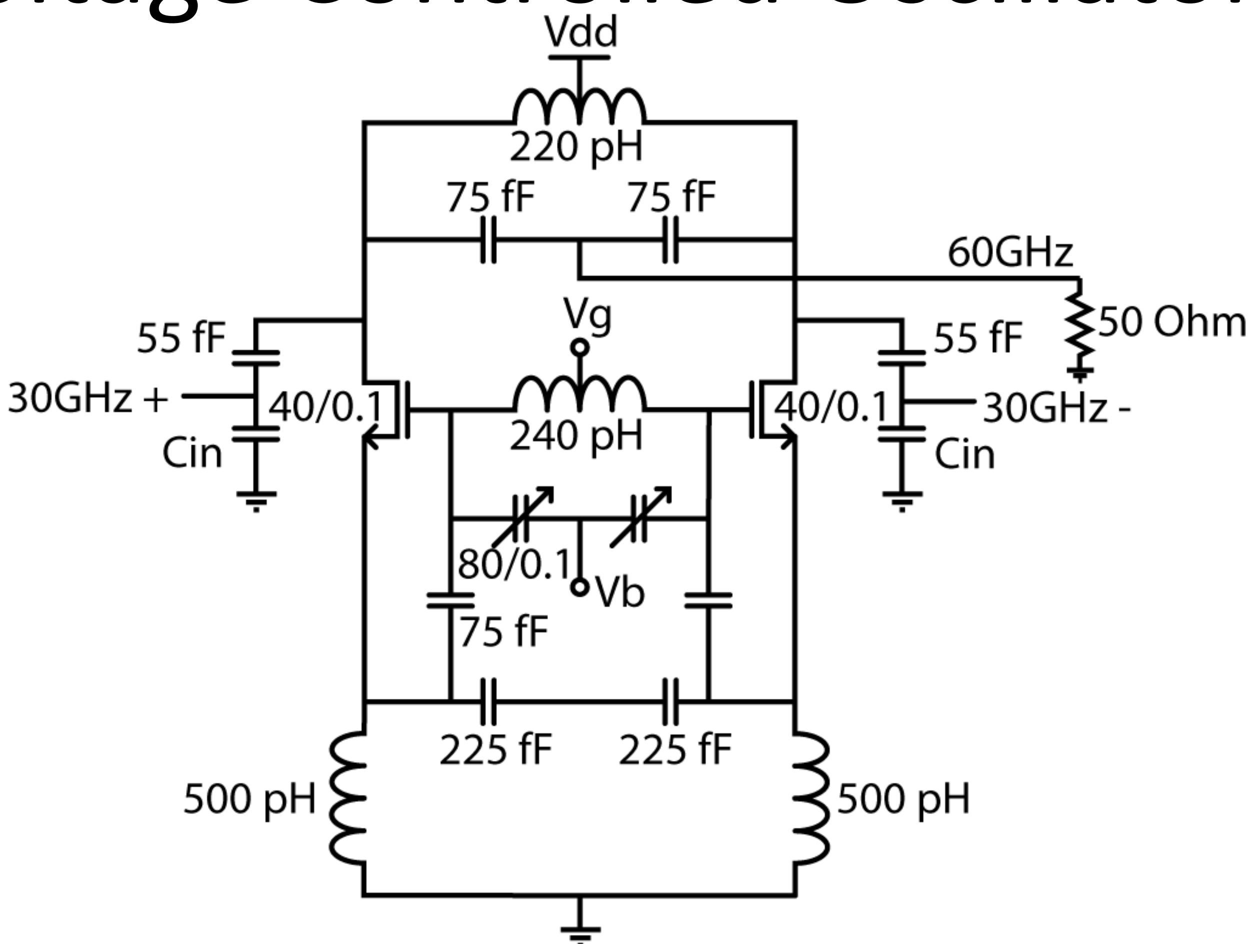
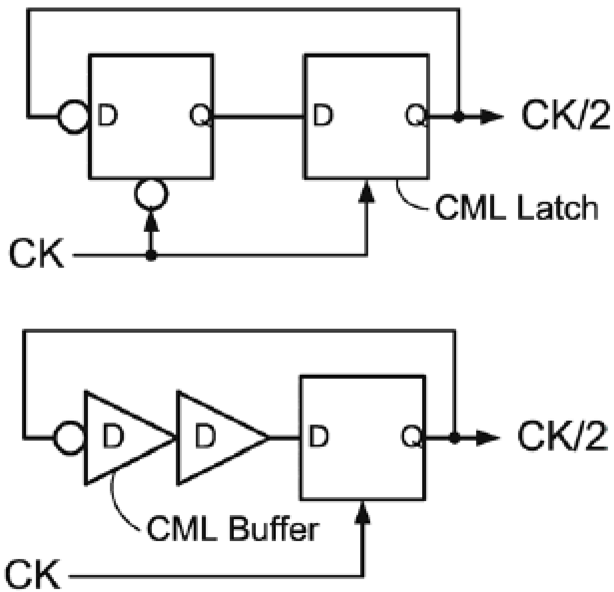
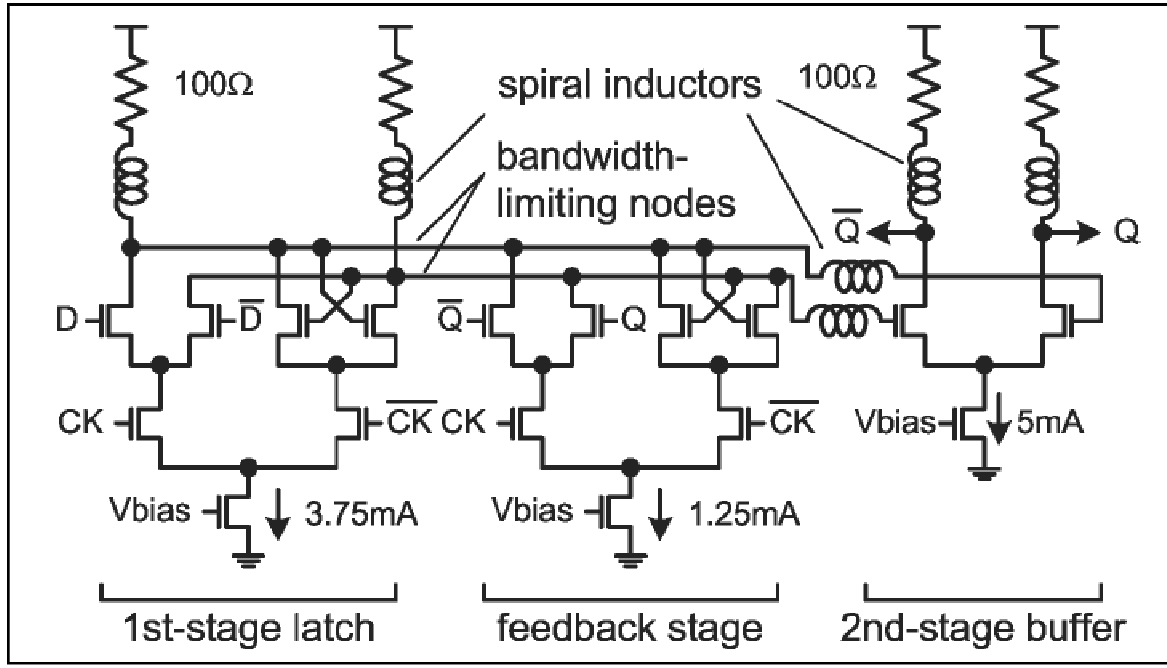
Voltage Controlled Oscillator



- Push-push VCO → no need for frequency doubler
- 30GHz Clapp based core
  - Careful with common-mode stability
- Low Vdd (0.7V) required for reliability

Pulsed-Latch Divider

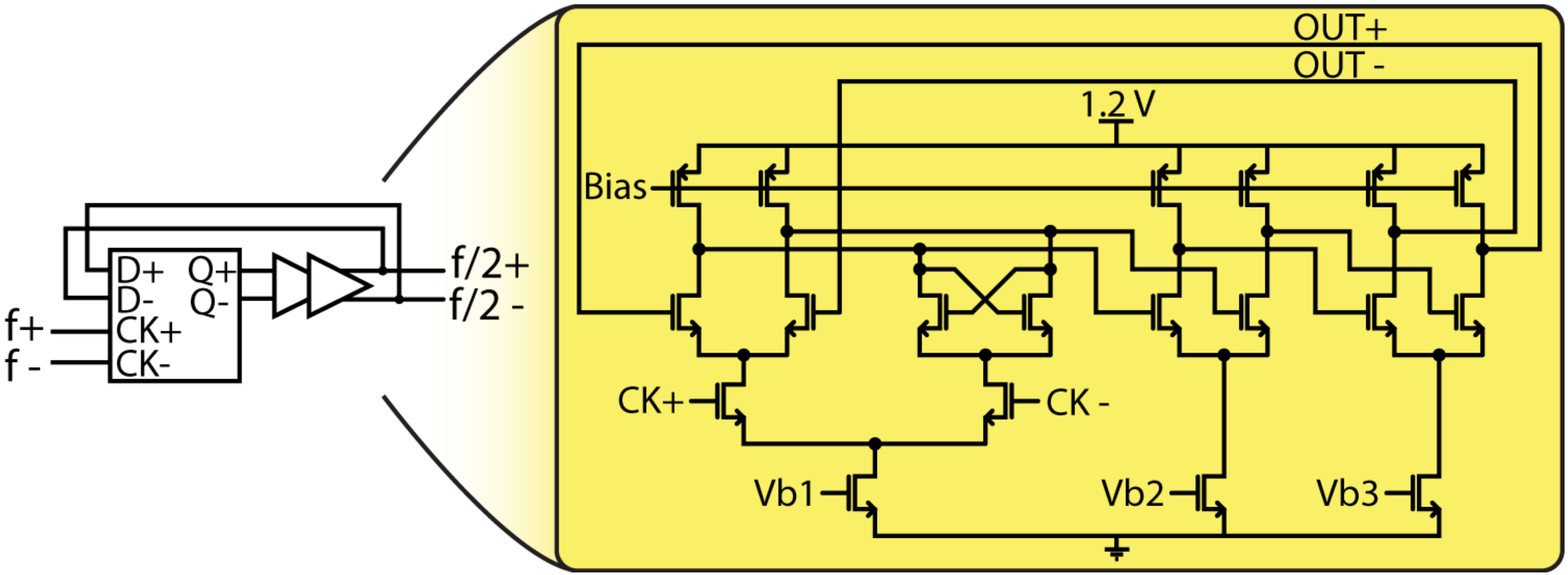




- Pulsed-Latch can increase maximum frequency of static divider while increasing minimum frequency from DC
- Minimum frequency set by race-through delay
- Complicated design in 0.13µm due to speed limitations

Ref: J. Kim et al, VLSI 2005.

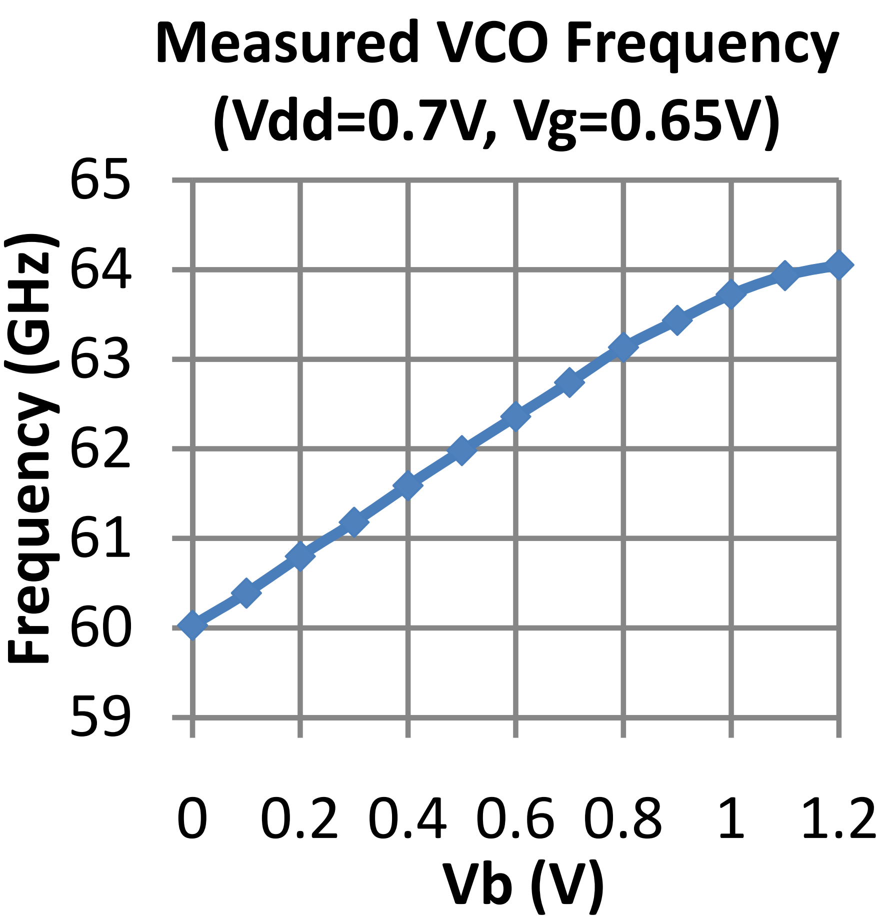
CML Pulsed Latch Divider Design

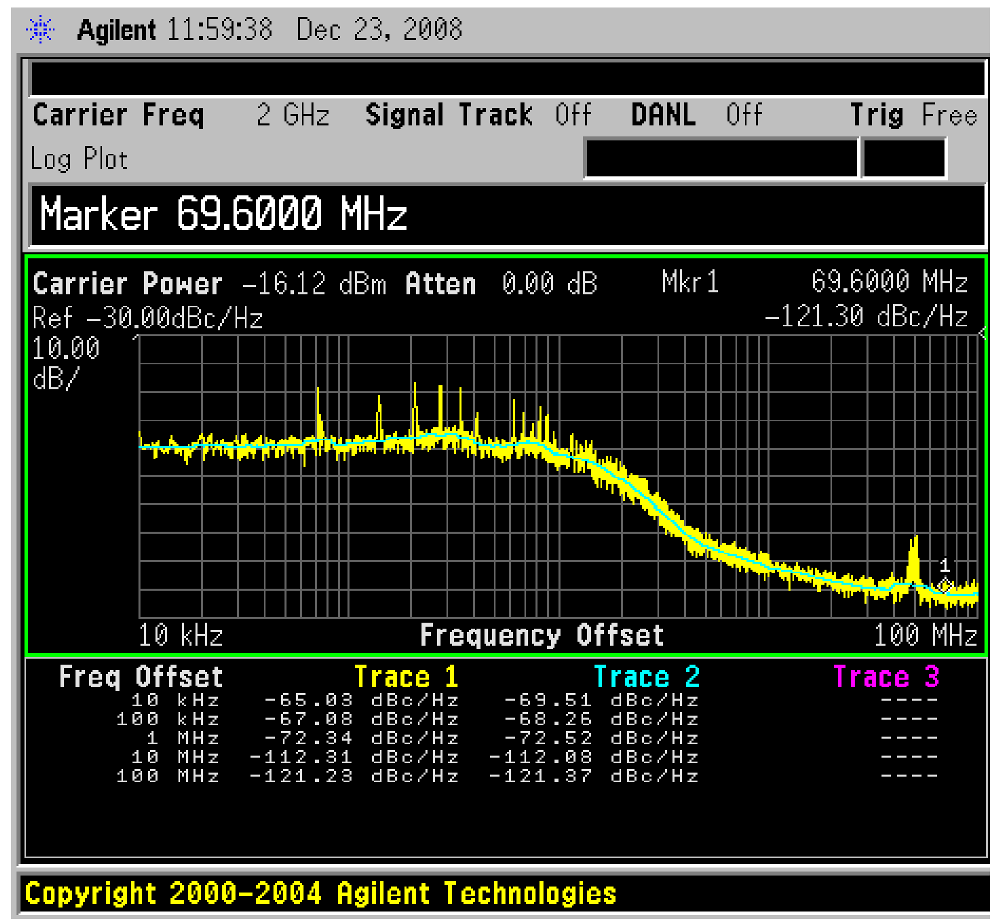


- Latch heavily loaded so output taken from 2nd buffer
- Tunable triode region PMOS load for tuning over PVT
- No inductors required → reduced area
- Additional buffer, not shown, to isolate next stage loading

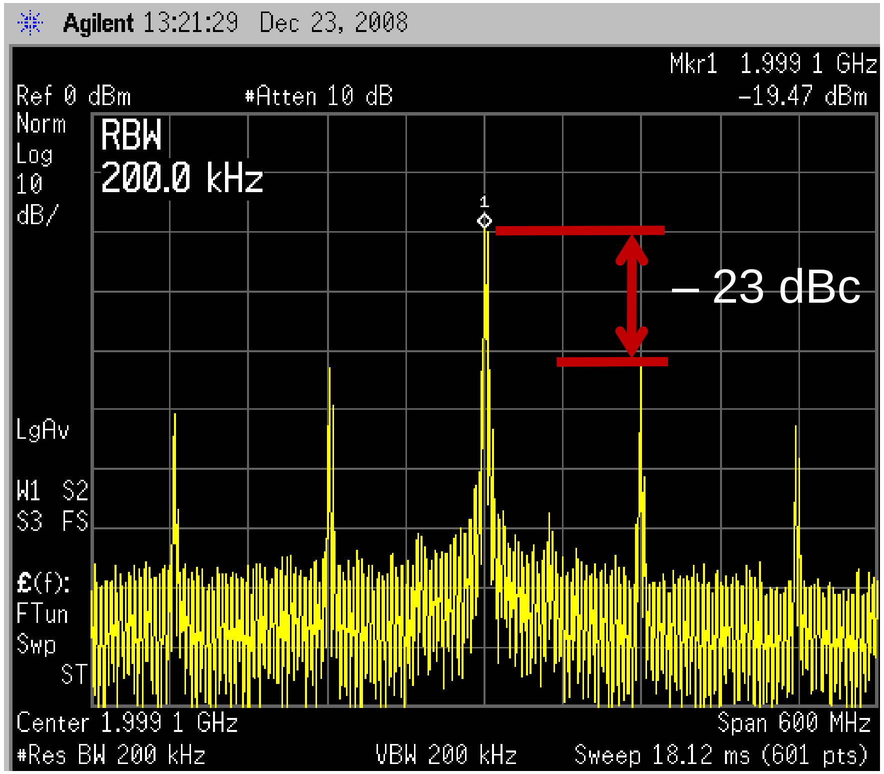
VCO/PLL Measurements

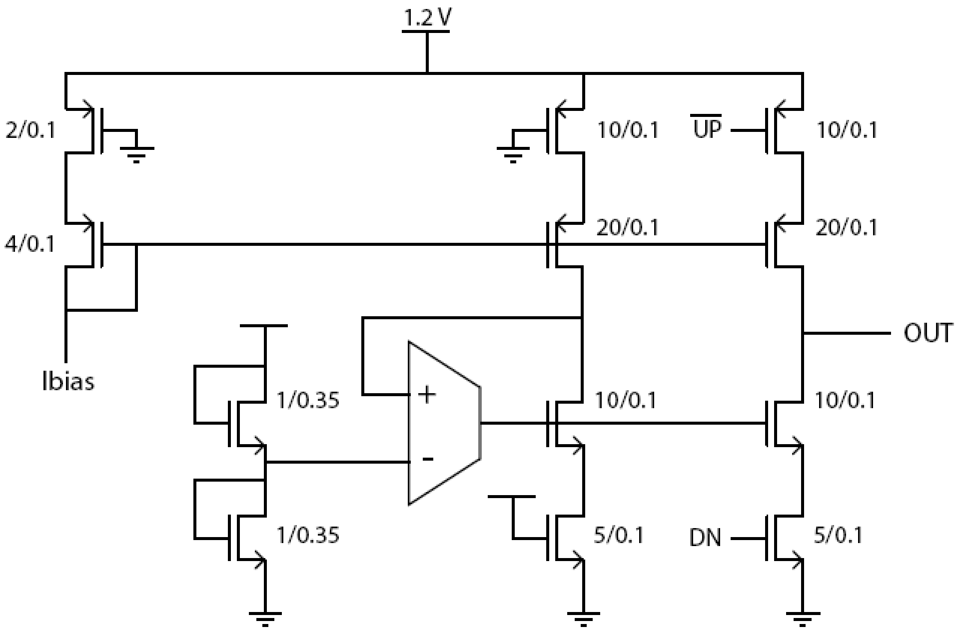
- VCO tuning range larger than expected
- Measured output power lower than expected by 10dBm
- Phase noise @ 10MHz offset: –112.08 dBc/Hz (FOM: -178.4dB)





Locked PLL Spectrum Measurement



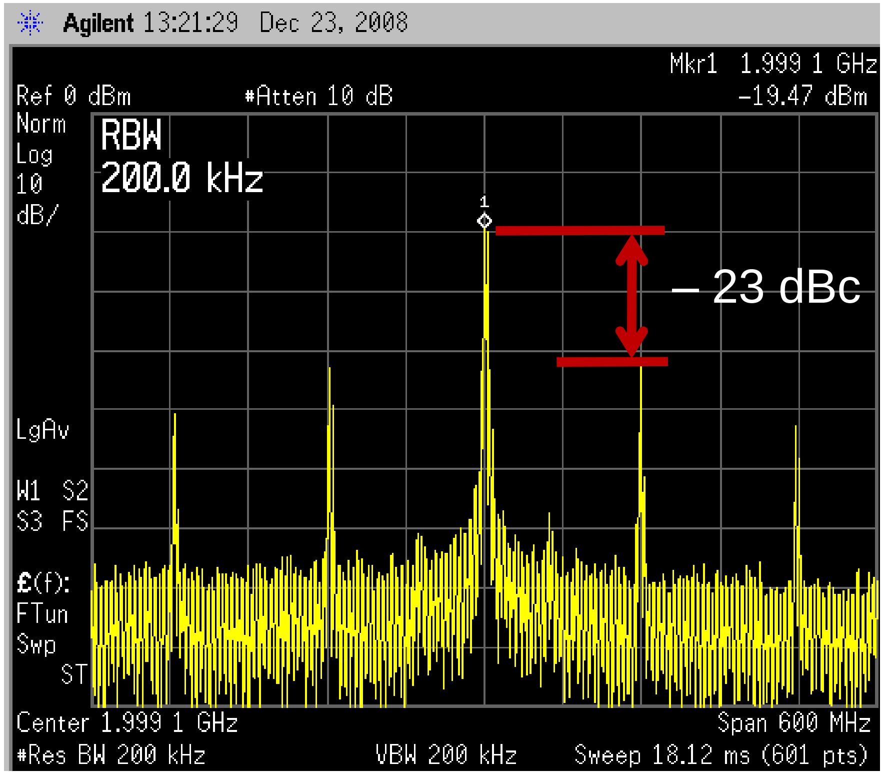


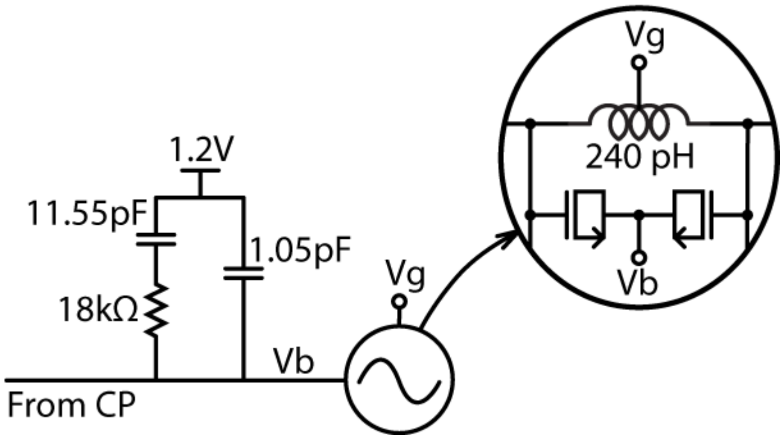
Input cap of OTA was too large to tie to OUT

- Large reference spurs likely due to loop filter reference supply, substrate injection, charge pump mismatch

Ref: E. Temporiti et al, JSSC Sep. 2004.

Locked PLL Spectrum Measurement

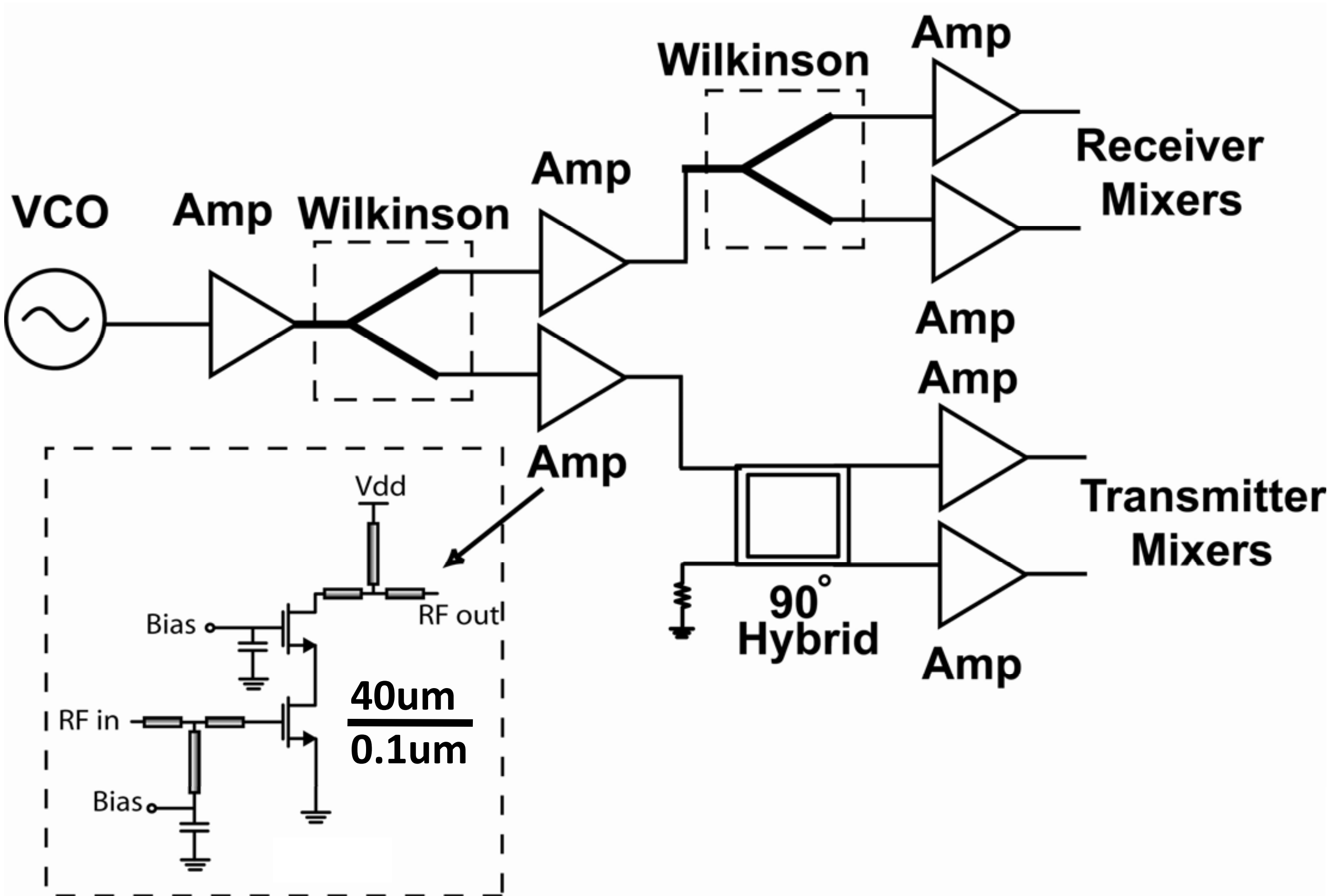




- Large reference spurs likely due to loop filter reference supply, substrate injection, charge pump mismatch

Ref: E. Temporiti et al, JSSC Sep. 2004.

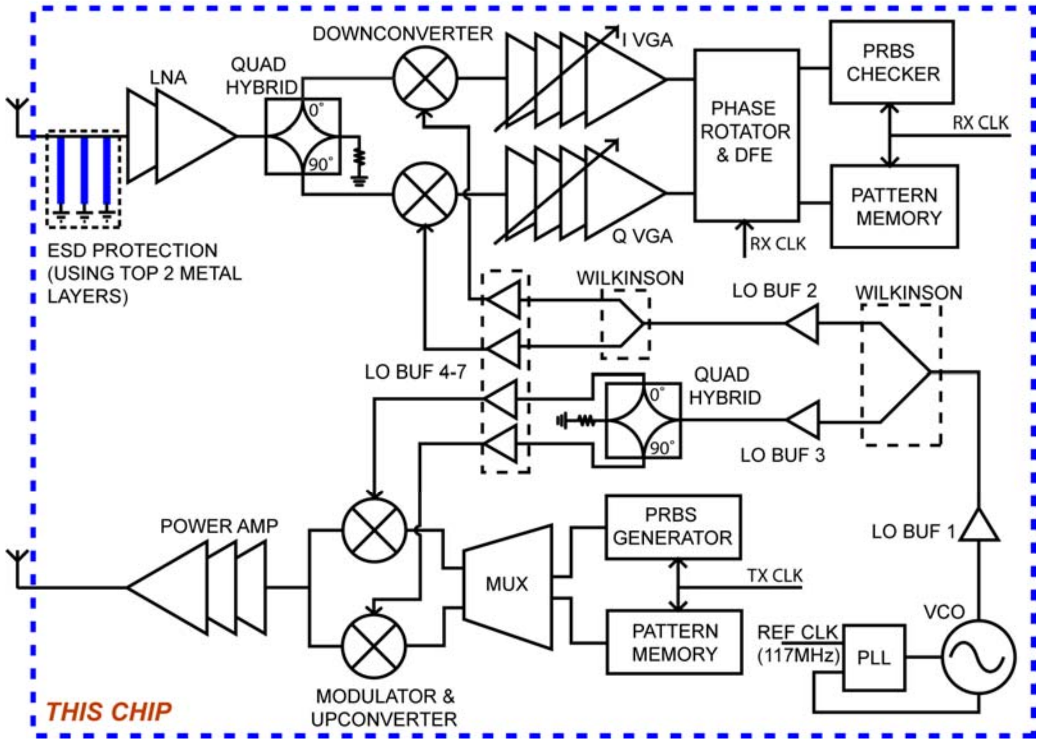
60GHz LO Chain



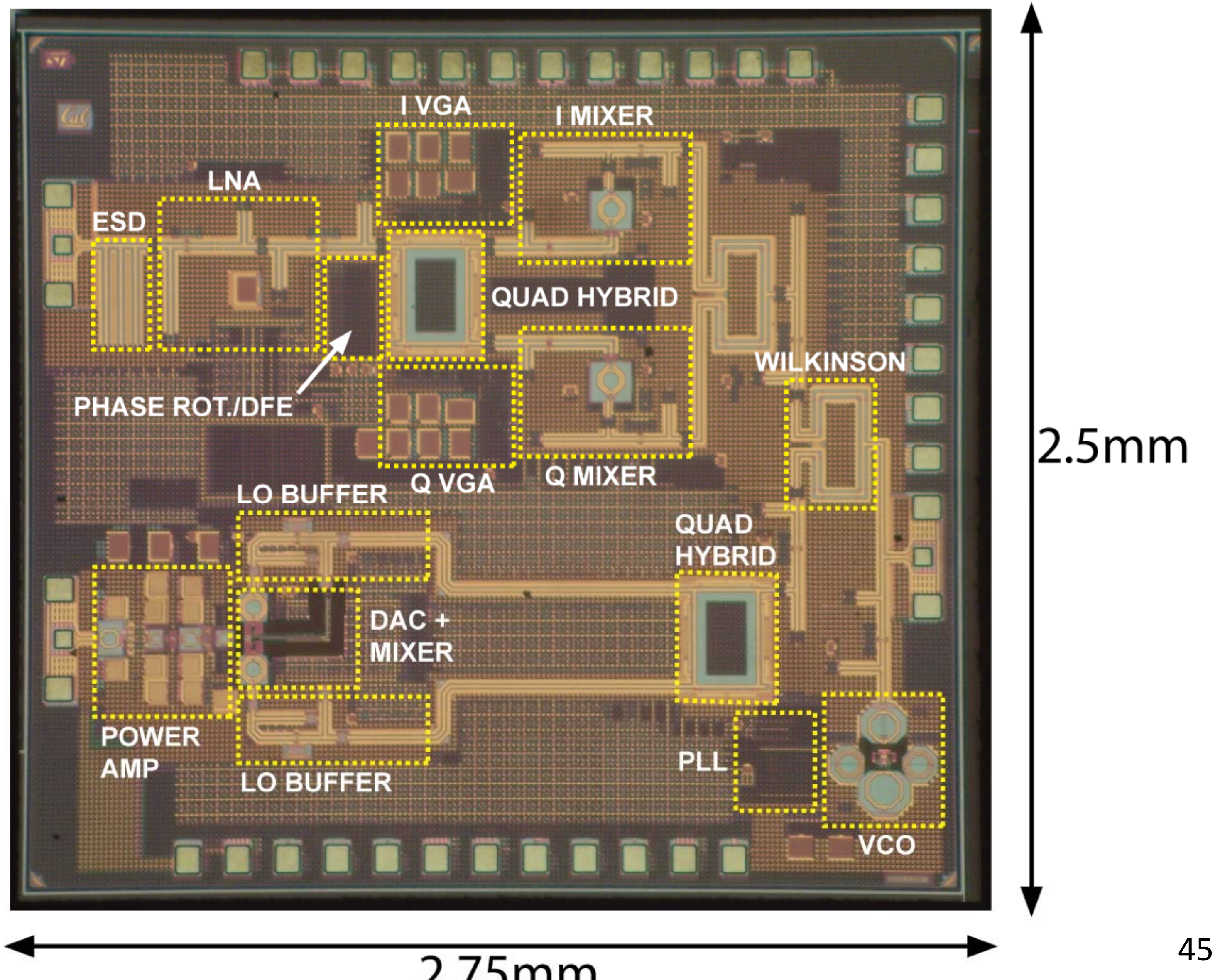
- Total power: 50mW (not including VCO)
- Delivers -2.5dBm to each of the 4 mixers

Outline

- Transmitter Blocks
- Receiver Blocks
- Phase Locked Loop and LO Chain
- Measurement Summary

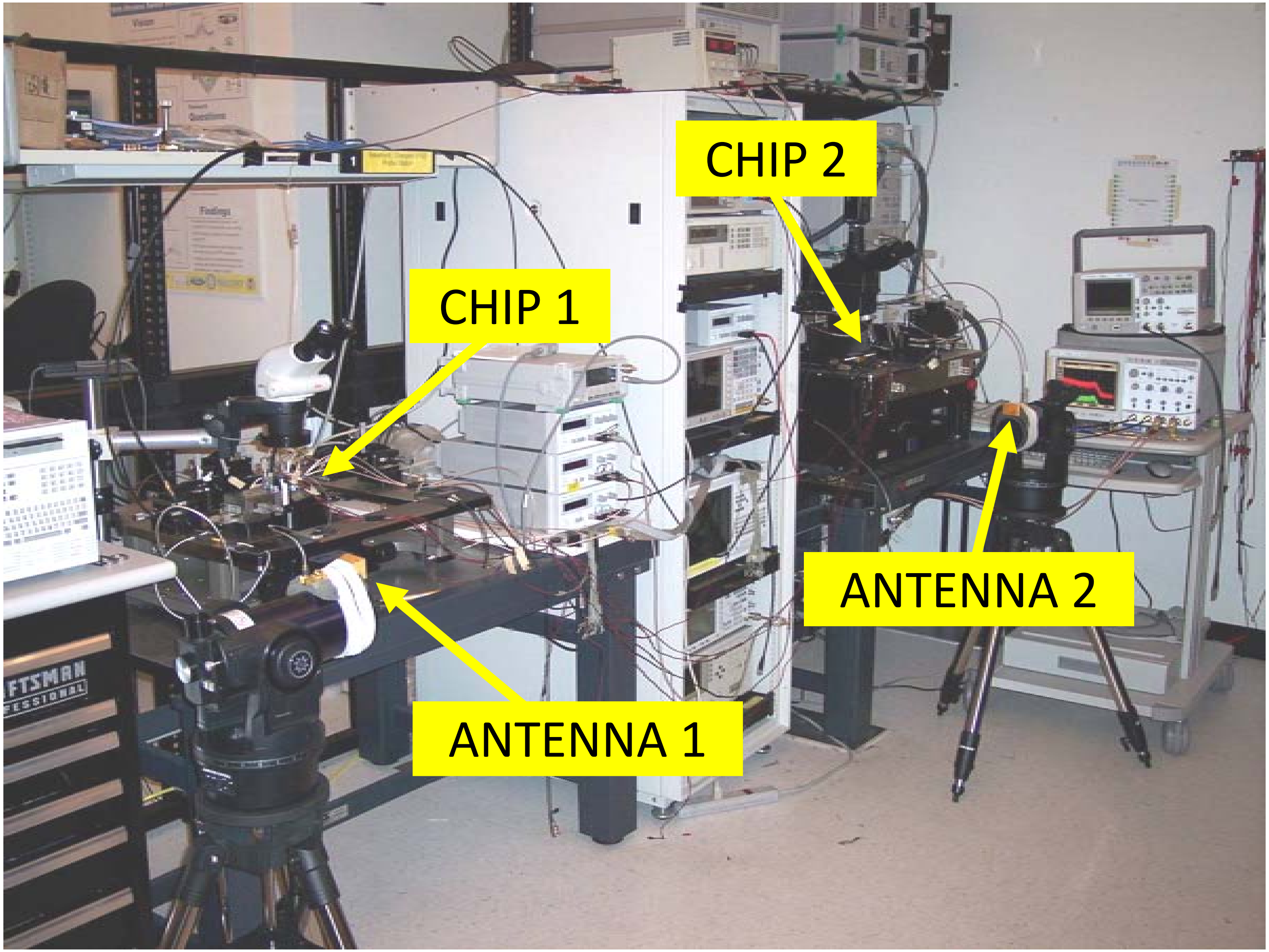


Die Photo



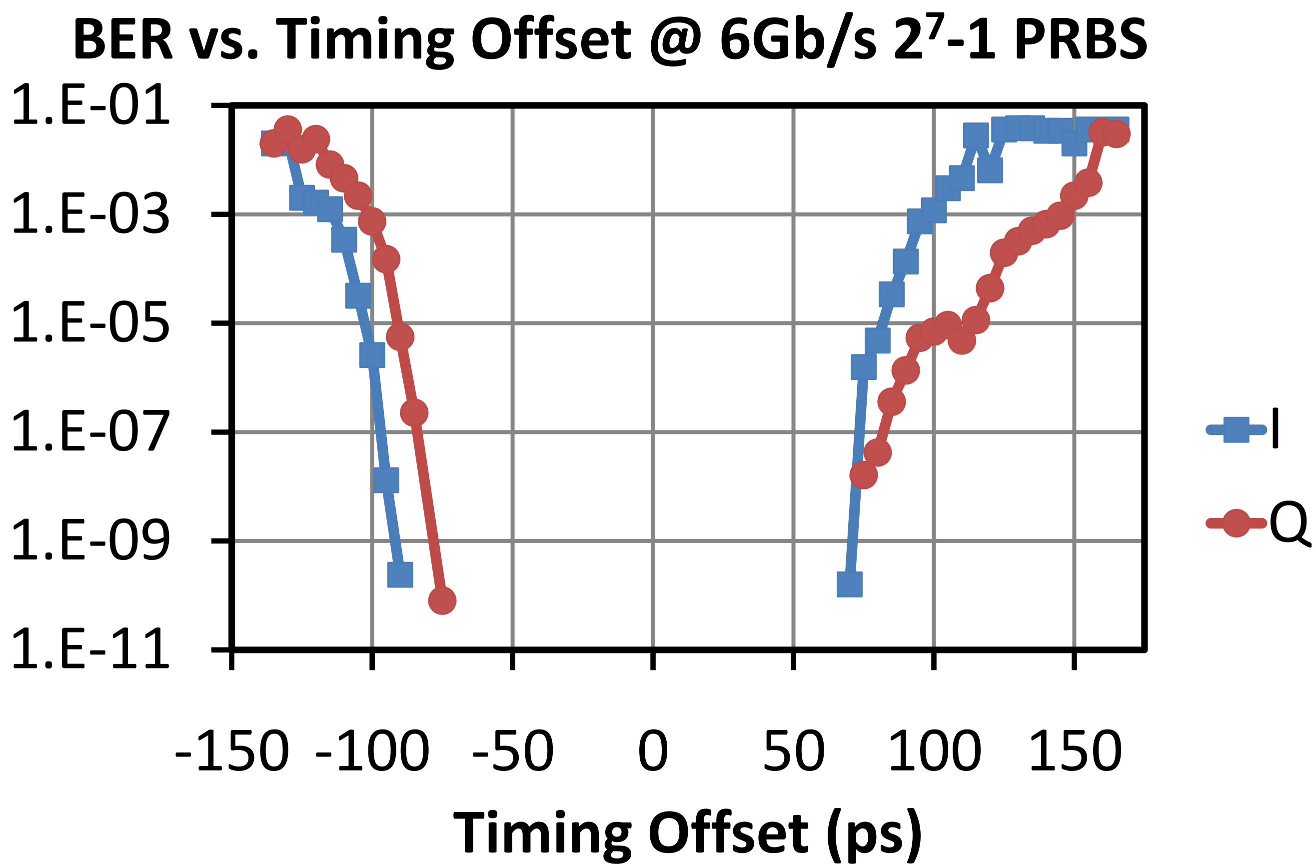
I VGA
I MIXER
LNA
ESD
QUAD HYBRID
PHASE ROT./DFE
WILKINSON
Q VGA
Q MIXER
LO BUFFER
QUAD
HYBRID
DAC +
MIXER
POWER
AMP
LO BUFFER
PLL
VCO
2.5mm
2.75mm

Test Set-Up



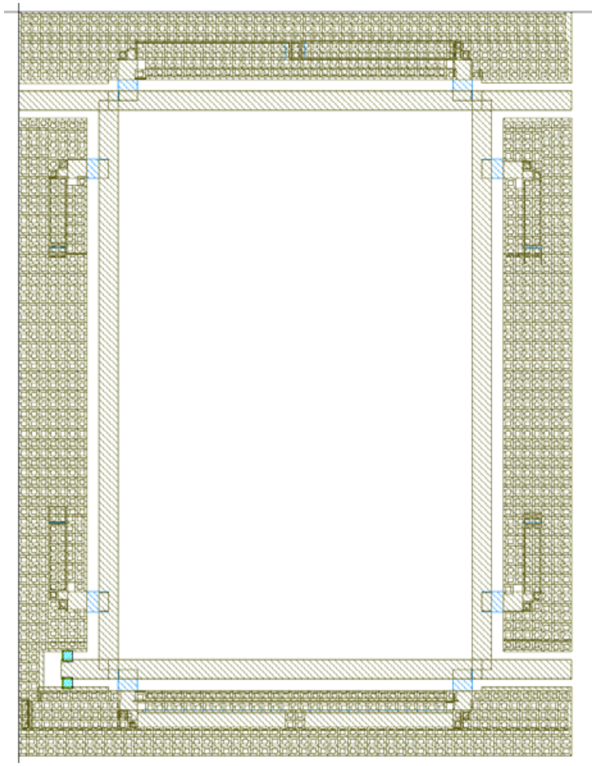
Data Transmission

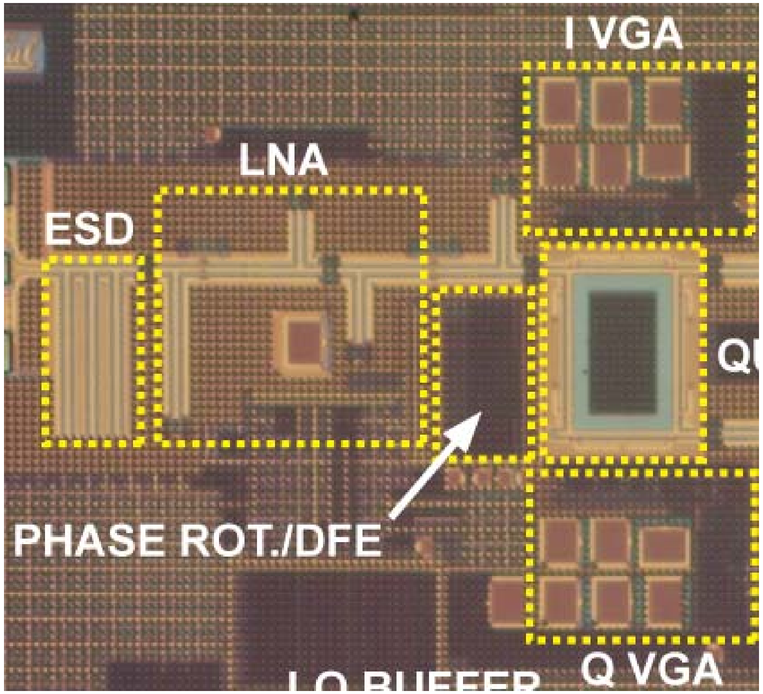
Setup:	Loop-Back	Chip-to-Chip (wired)	Chip-to-Chip (wireless)
Highest Data Rate Achieved	7Gb/s	6Gb/s	4Gb/s over 1m distance



Sources of I/Q Mismatch

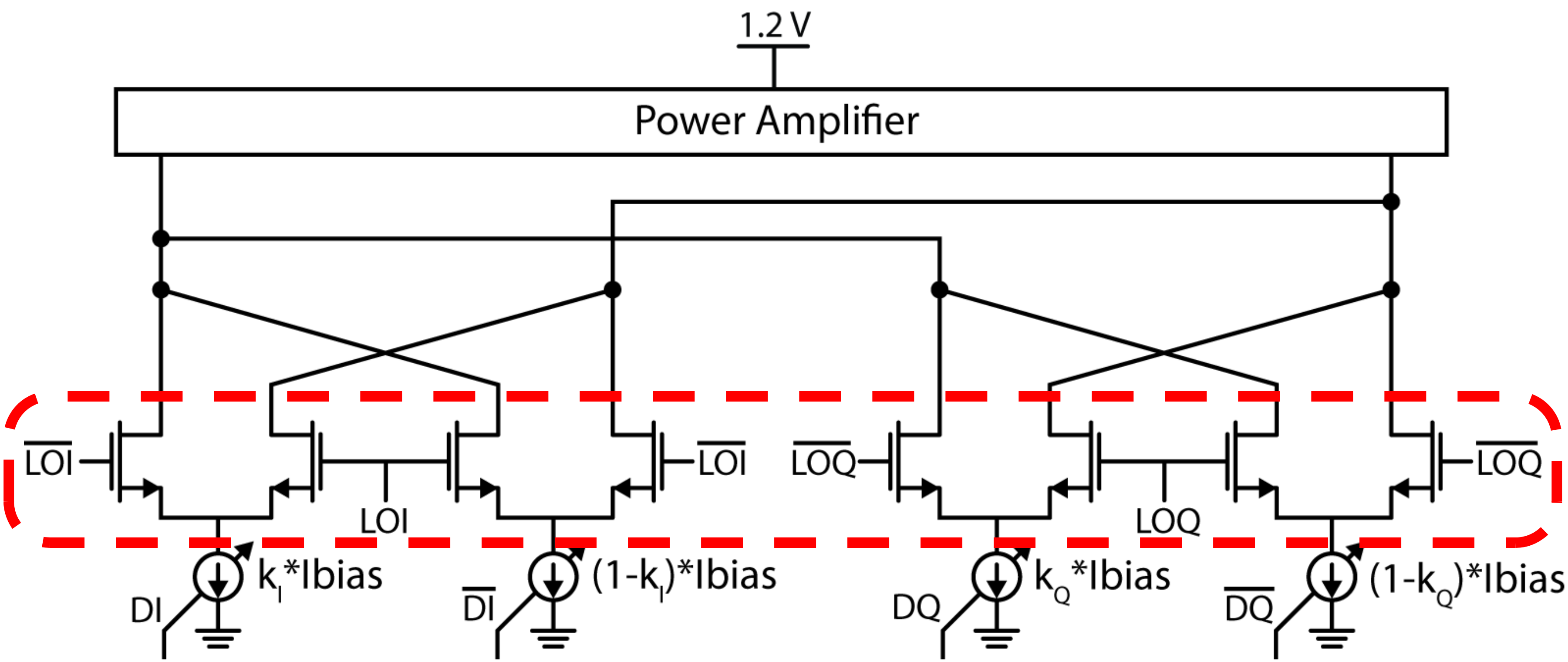
- Gain and phase mismatch in the hybrid
- Unbalanced routing of VGA outputs to phase rotator inputs





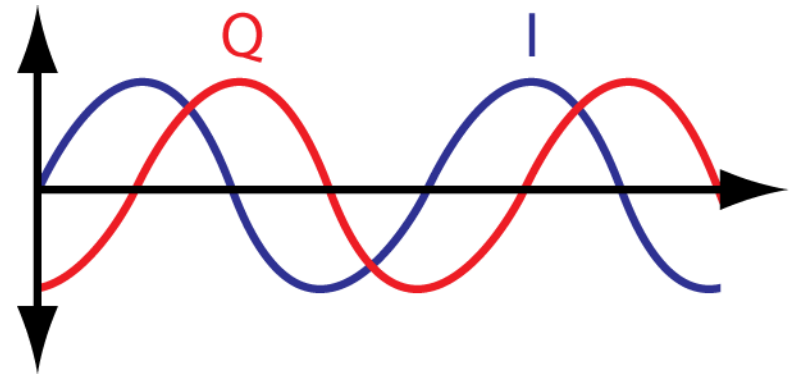
Sources of I/Q Mismatch

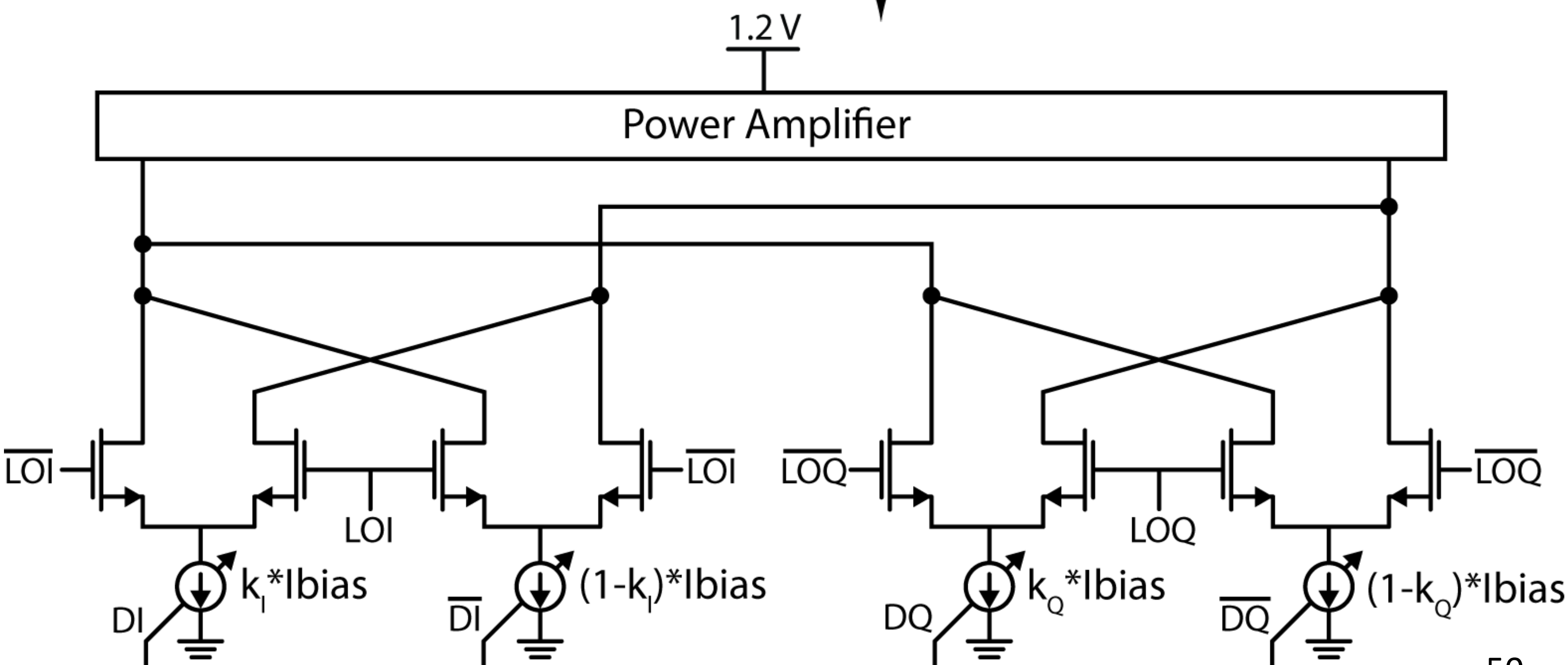
- Routing of LO and RF in up-conversion mixer quads
  - Symmetric routing practically impossible



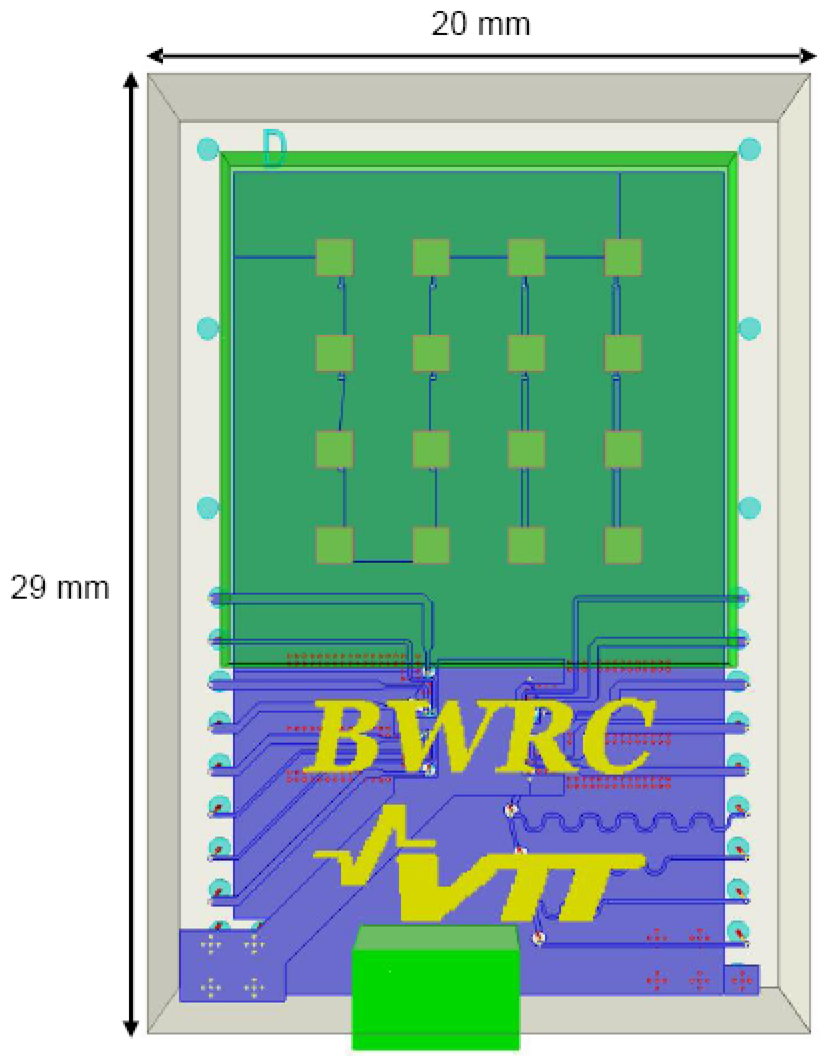
Sources of I/Q Mismatch

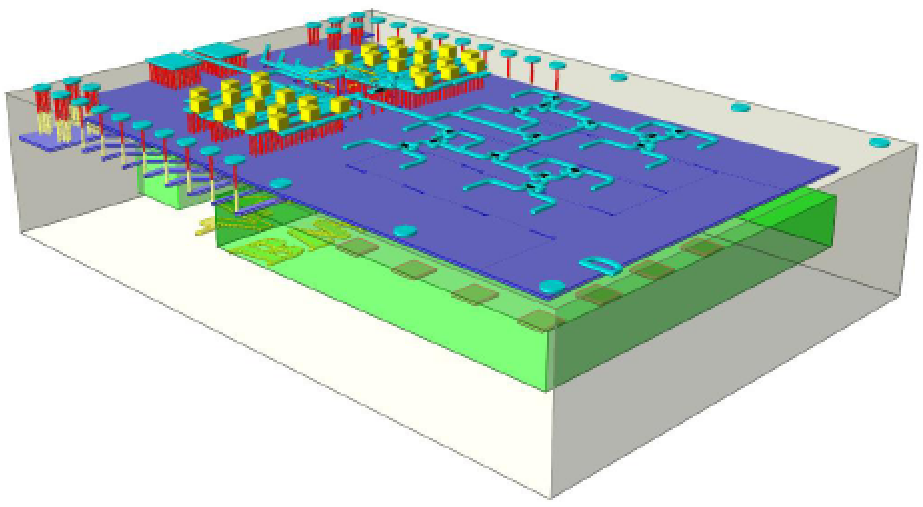
- Unbalanced mixer loading due to 90° separation between LOI and LOQ





Packaged Transceiver Testing Underway





z-axis not is scale

Ref: A. E. I. Lamminen et al, IEEE Trans. Antennas Propag. Sept. 2005.

Conclusion

- Designed an integrated 60GHz transceiver including RF, LO, PLL, and BB
  - 170mW in TX mode and 138mW in RX mode
  - Mixed-signal baseband processing can be very efficient
  - LO distribution can be expensive both in area and power
- Future directions
  - Closing the loops
  - Packaged testing

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