Analog Verification

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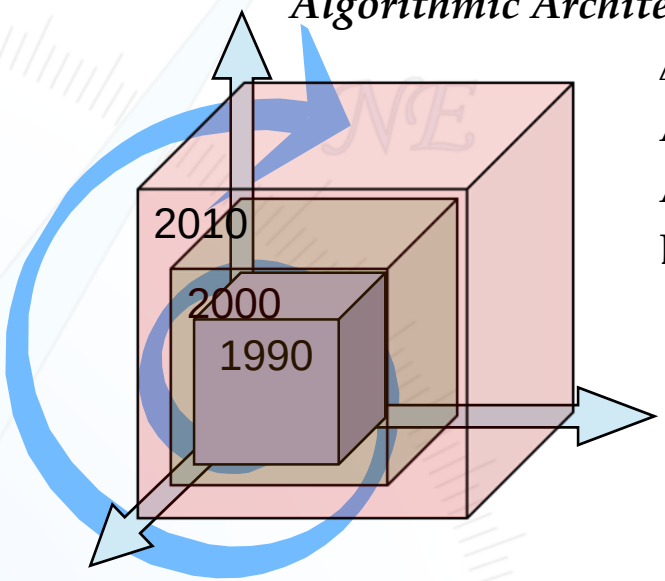
Designs They Are A-Changin'

Bob Dylan, 1964

The Complexity of Design is Growing Rapidly

Algorithmic Architectures

ΔΣ architectures
Auto calibration
Adaptive filtering
Etc.



Modes & Settings

Power modes
Digital trimming
Multiple standards
Etc.

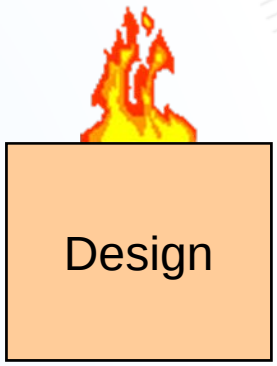
Size

> 100K transistors

In Multiple Dimensions!

Functional Errors

- Functional errors are often very simple errors
  - Inverted signals
  - Corrupt logic
  - Flipped busses
  - Unaccounted for dependencies (chicken/egg problem)
  - Communication errors
- But are generally catastrophic



In Recent Verification Efforts

- We found
  - swapped inputs
  - logic error that precluded sleep mode
  - busses swapped
  - dependency loop (chicken & egg problem)
  - inverted bias current
  - wires swapped
  - inverted input
  - swapped reset & reset bar
  - logic lines crossing supply domains w/o level shifters
  - incorrect RTL
  - undriven logic signal in analog top level
  - errors in register map
  - many spec errors
  - And more…

The Three Basic Issues

- Detailed verification only performed at block level
  - All required signals are assumed to be present
  - Assumptions on inter-block dependencies never verified
- Verification on most modes never performed
  - Only typical or worst case modes
  - Any control logic that supports untested mode could contain hidden error
- No analog – digital co-verification

Transistor-Level Verification

- Too expensive for *functional verification*
  - 10K transistors, 30K cycles, 250 modes
  - One week for one mode with timing simulator
- Need nightly regression tests
  - 10K× speed up needed
- Chip level requires
  - 100K-1M× speed ups

What's Needed

- Systematic approach to verifying design & specification
- Confidence that all flaws have been found
- More verification, earlier in design flow
  - Errors are easier to fix & less disruptive
- Help with performance verification
- Accurate model of mixed-signal section

The Answer

- Functional verification with …
  - Model-based verification
    - Dramatically accelerates the simulation
    - Moves it earlier in design cycle
  - Exhaustive regression testing
    - Check every mode and every setting
    - Automated pass/fail tests (self-checking tests)
  - Creation of a verified "sign off" quality top-level model
    - Often must be pure Verilog or VHDL

This is Analog Verification

- Exhaustive regression testing
- Traceable to transistor level
- Verifies both models and circuits
  - Test benches verify behavior of models
  - Methodology assures models are consistent with circuit
- Driven by analog verification engineer

We can now imagine a future where we are surprised when an analog chip does not function the first time.

Conclusions

- Complex system design requires a rigorous system verification methodology
- Chip design and analog implementation needs to be linked for verification
- AV can be done today
  - Modeling and Regression Testing
- The bigger the system, the more benefit will be derived from using AV

Designer's Guide Consulting

- Adopting analog verification is a difficult process, filled with potential pitfalls
- We can help guide you through the process
  - Teach classes
  - Training your verification engineers
  - Guide verification planning
  - Consult on difficult models & tests
    - How to create very fast analog models in verilog
    - How to overcome performance issues
  - Provide AV services

References

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For More Information

www.designers-guide.com