Low-Power CMOS Optical Interconnect Transceivers

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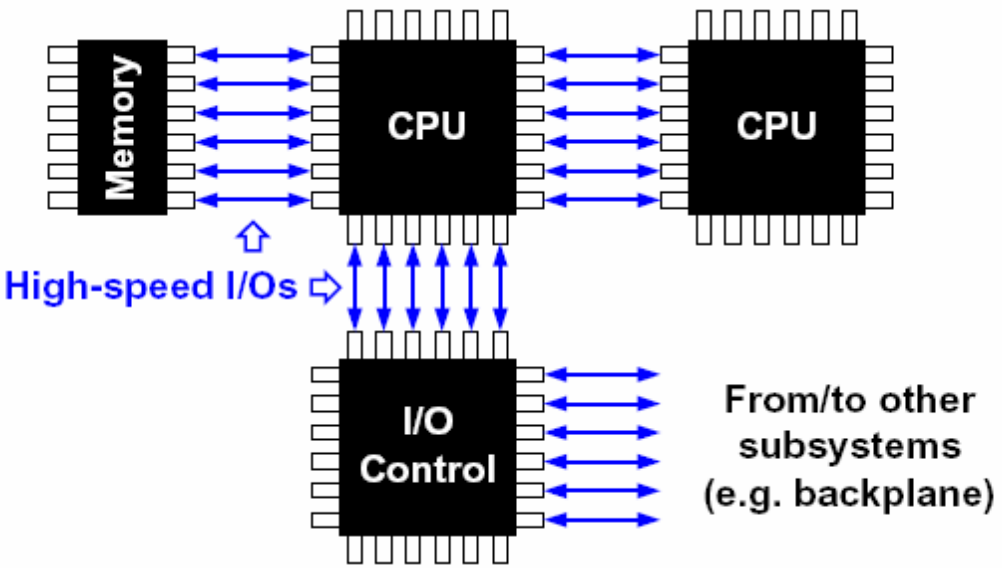
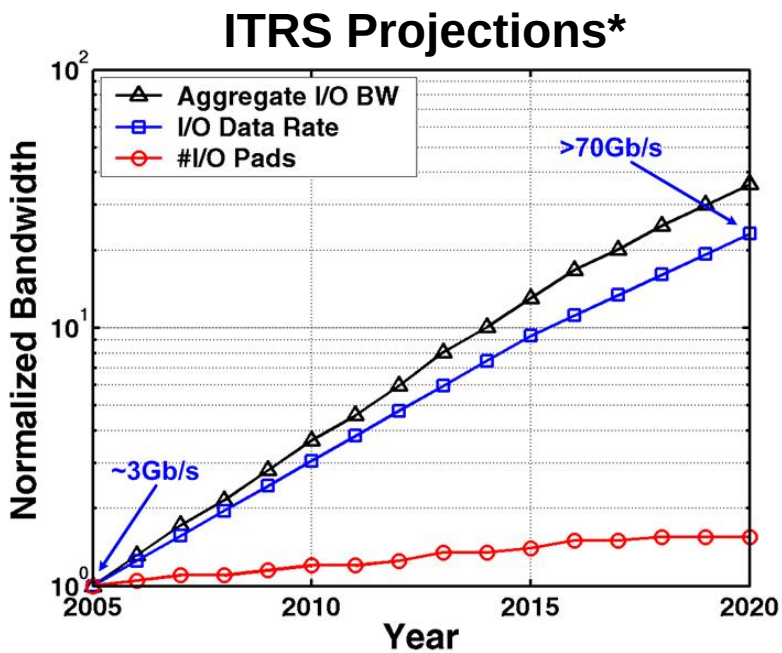
Outline

- Introduction
- Optical transmitters
- Optical receiver
- Clock and data recovery
- Optical link system performance
- Conclusion

High Speed Links

- Increasing computation power and today's networked society requires chip-to-chip I/O bandwidth to increase
  - Routers, Processor – Memory Interface

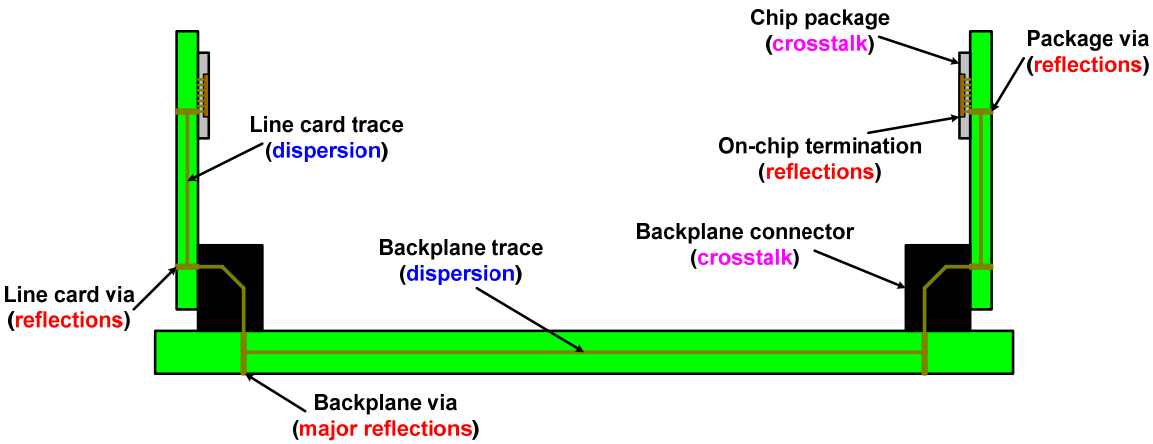




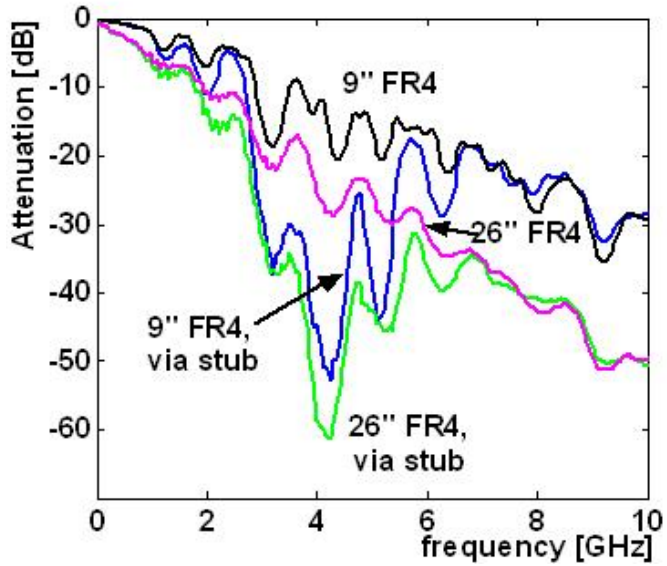
*2006 International Technology Roadmap for Semiconductors

Chip-to-Chip Electrical Interconnects

Electrical Backplane Channel



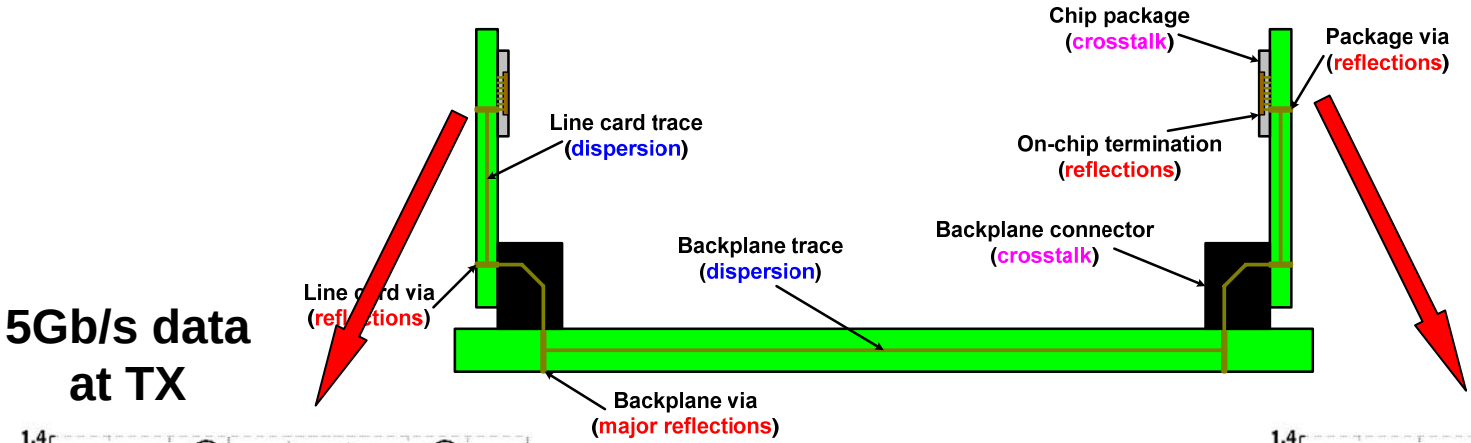
Channel Responses*

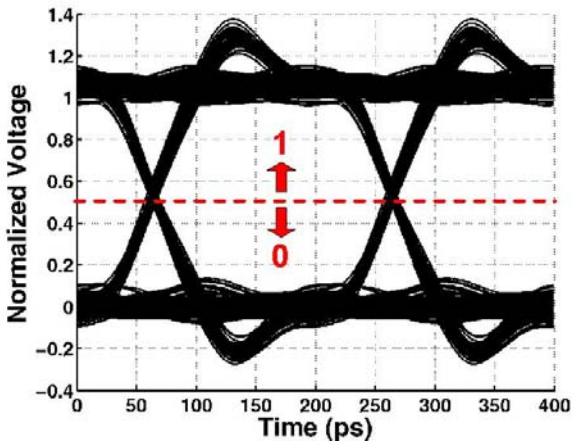


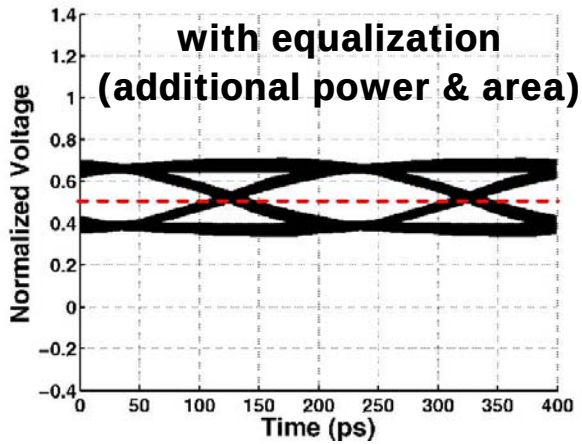
- Electrical channel characteristics limit performance

*V. Stojanovic and M. Horowitz, “Modeling and Analysis of High-Speed Links," *CICC*, 2003.

Chip-to-Chip Electrical Interconnects

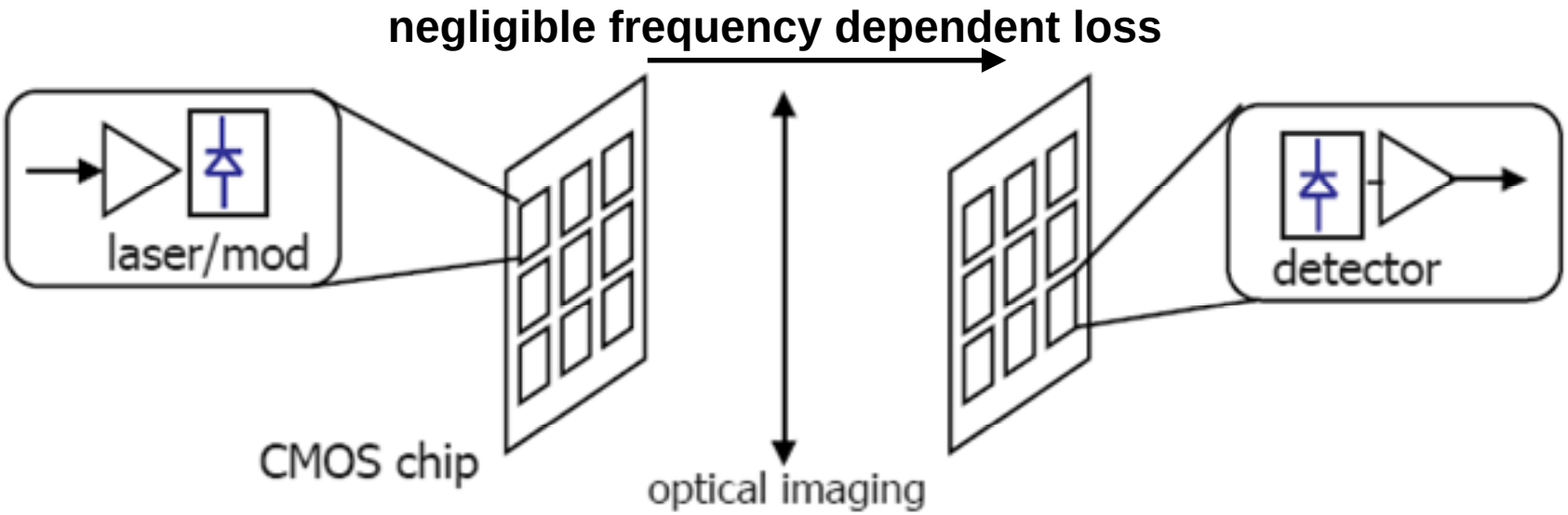






- Sophisticated equalization circuitry required
- Typical commercial electrical I/O xcvr
  - ~20mW/Gb/s at 10Gb/s

Chip-to-Chip Optical Interconnects

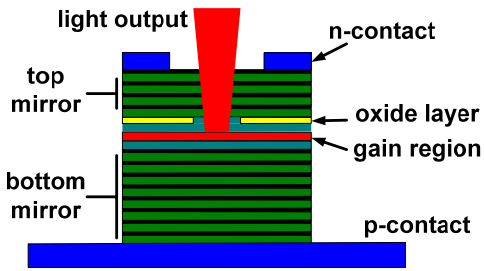


- Optical interconnects remove many channel limitations
  - Reduced complexity and power consumption
  - Potential for high information density with wavelength-division multiplexing (WDM)

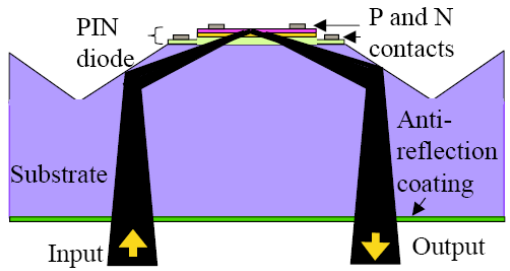
Optical Sources & Detectors

- Sources

VCSEL

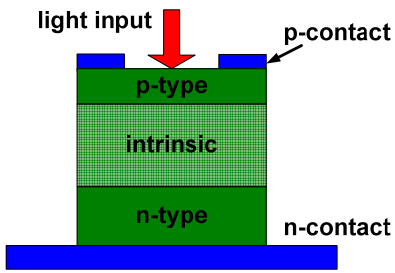


MQW Electroabsorption Modulator

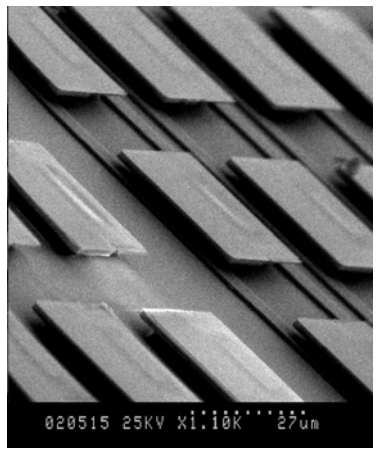


- Detector

p-i-n Detector



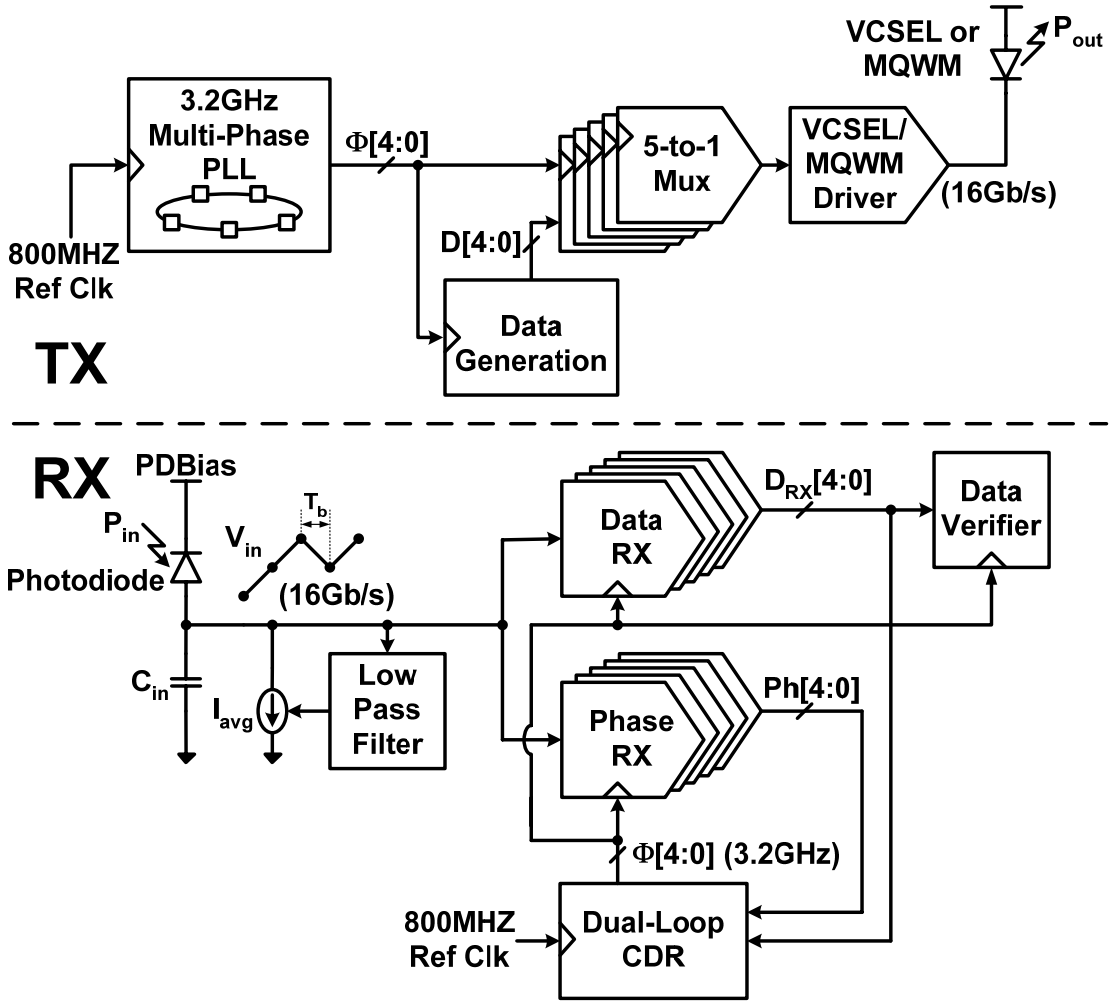
- Integration



CMOS Optical Link Issues

- VCSEL bandwidth
  - Inherent device RC
  - Optical bandwidth requires high average current density
- Modulator voltage swing limited by CMOS reliability constraints
- Reduced gain/headroom in scaled technologies
  - Motivates use of integrating RX vs traditional TIA
- Dealing with mismatch
  - Offset compensation (voltage & timing)
- Power and area reduction

90nm CMOS 16Gb/s Optical Transceiver Architecture



1. **S. Palermo** *et al*, "A 90nm CMOS 16Gb/s Transciever for Optical Interconnects," *ISSCC*, 2007.
2. J. Roth, **S. Palermo** *et al*, "1550nm Optical Interconnect Transceiver with Low Voltage Electroabsorption Modulators Flip-Chip Bonded to 90nm CMOS," *OFC*, 2007.

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  - VCSEL TX
  - MQWM TX
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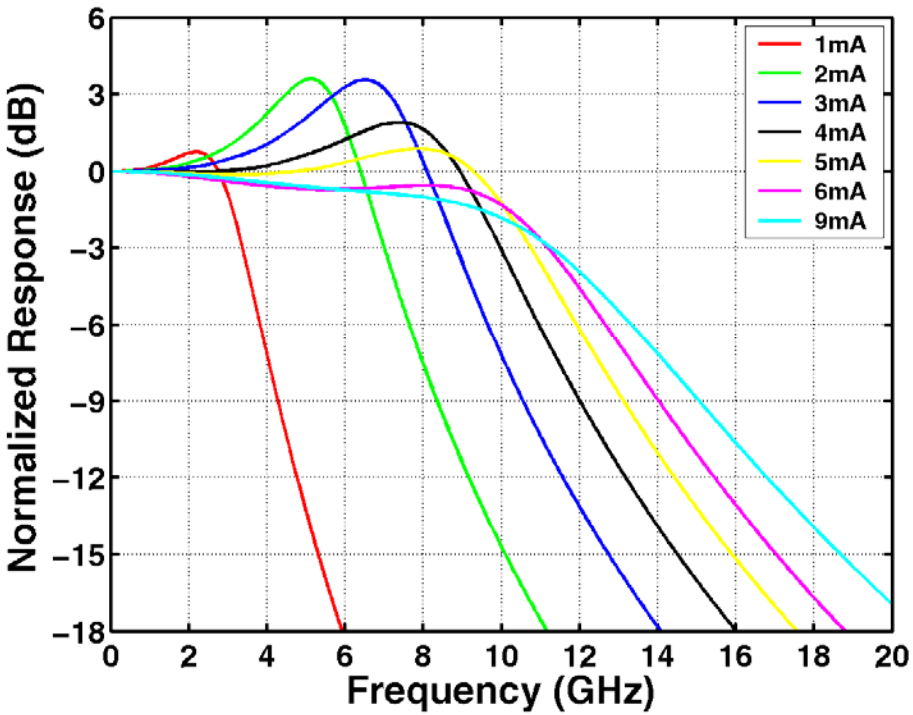
VCSEL Bandwidth vs Reliability

10Gb/s VCSEL Frequency Response [1]



$$BW \propto \sqrt{I_{avg} - I_{TH}}$$

- Mean Time to Failure (MTTF) is inversely proportional to current density squared

$$MTTF = \frac{A}{j^2} e^{\left(\frac{E_A}{k}\right)\left(\frac{1}{T_j} - \frac{1}{373}\right)} \quad [2]$$

- Steep trade-off between bandwidth and reliability

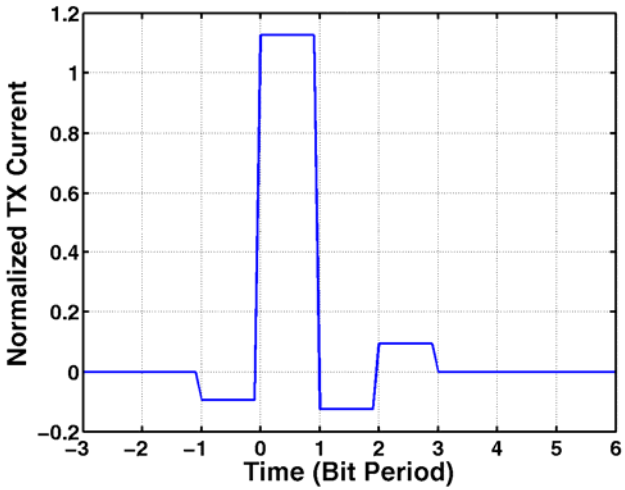
$$MTTF \propto \frac{1}{BW^4}$$

1. D. Bossert *et al*, "Production of high-speed oxide confined VCSEL arrays for datacom applications," *Proceedings of SPIE*, 2002.
2. M. Teitelbaum and K. Goossen, "Reliability of Direct Mesa Flip-Chip Bonded VCSEL's," *LEOS*, 2004.

VCSEL TX Equalization

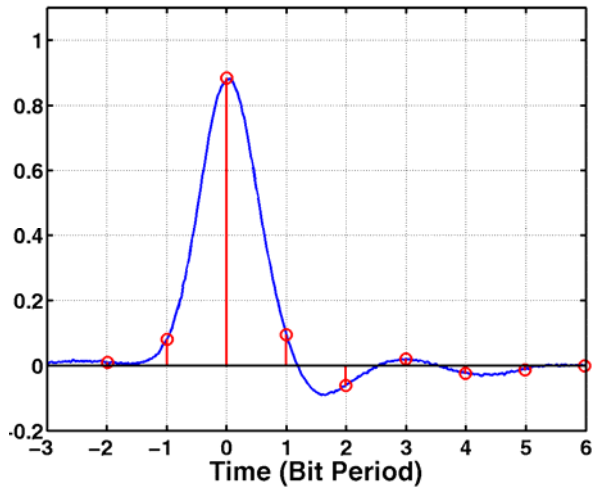
TX Current

$h(n)=I_{-1}(-1) + I_0(0) + I_1(1) + I_2(2)$



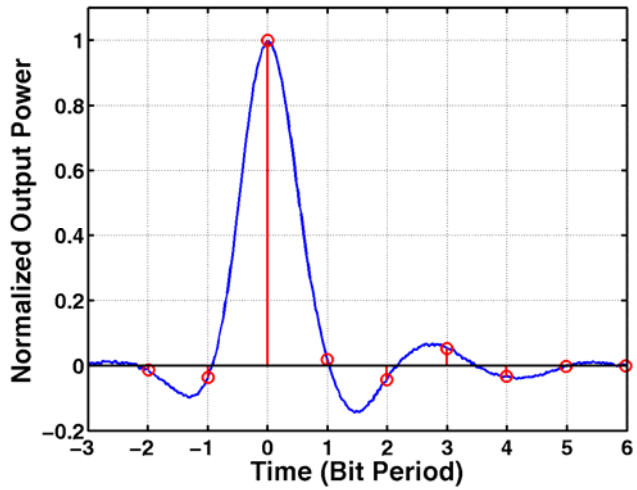
Channel Pulse Response

$p(n)$



Received Optical Power

$v(n)$

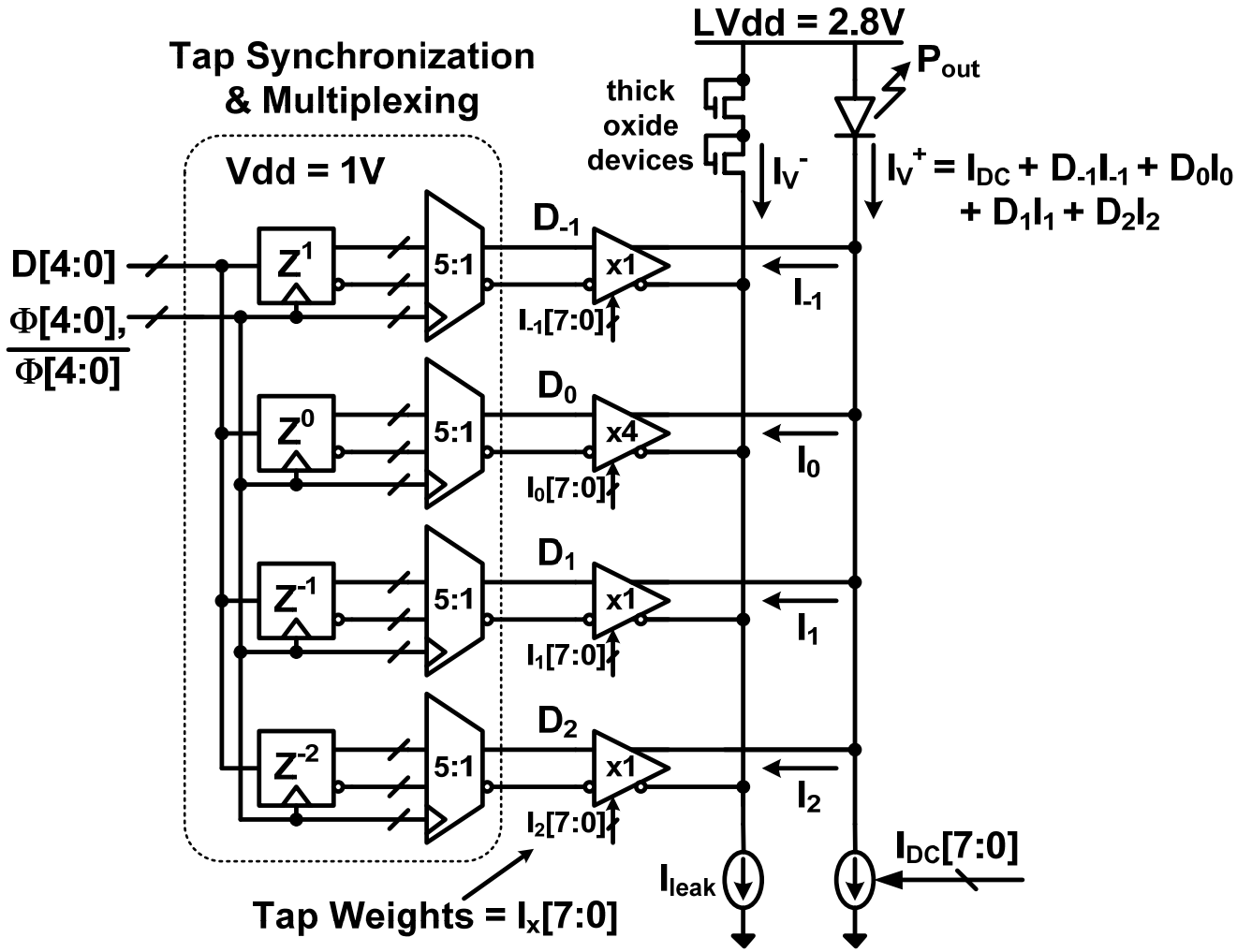


Measured pulse responses at 17Gb/s w/ I_{avg}=6.7mA

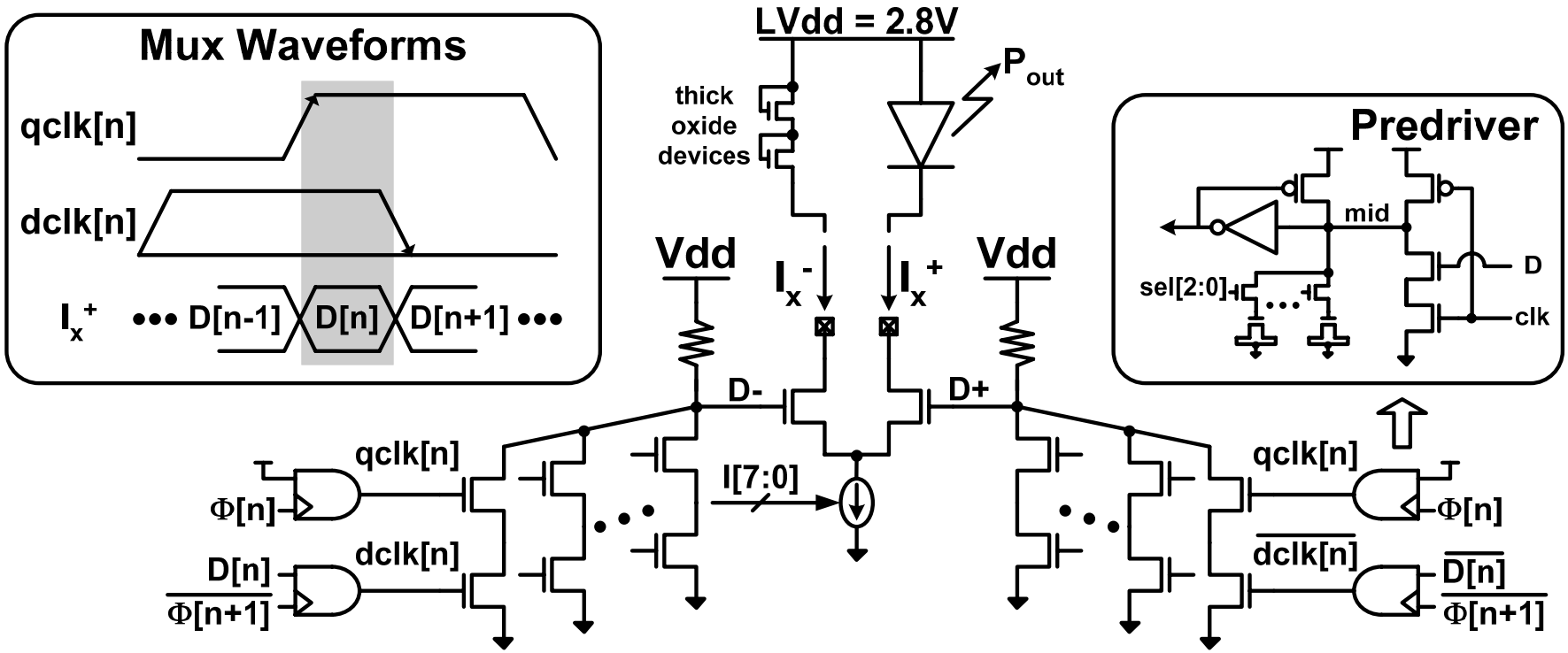
$$H_{ls} = \left(P^T P\right)^{-1} P^T Y_{des}$$

- 4-tap FIR filter – 1 precursor, 1 main, and 2 postcursor is a good compromise between power and performance

Multiplexing FIR Circuit Implementation

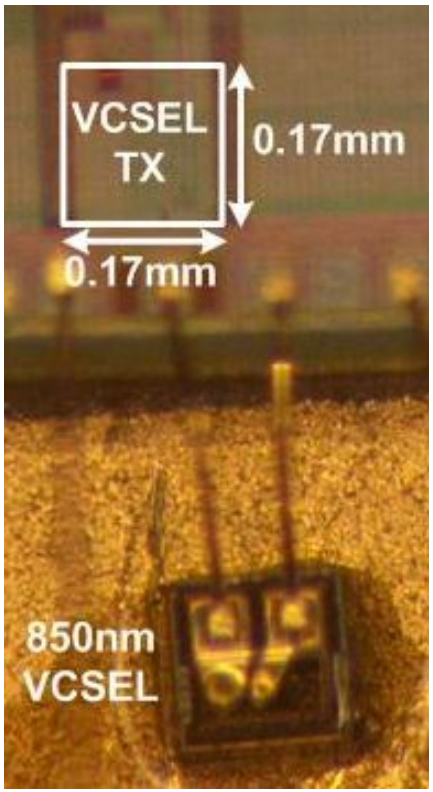


Tap Mux & Output Stage

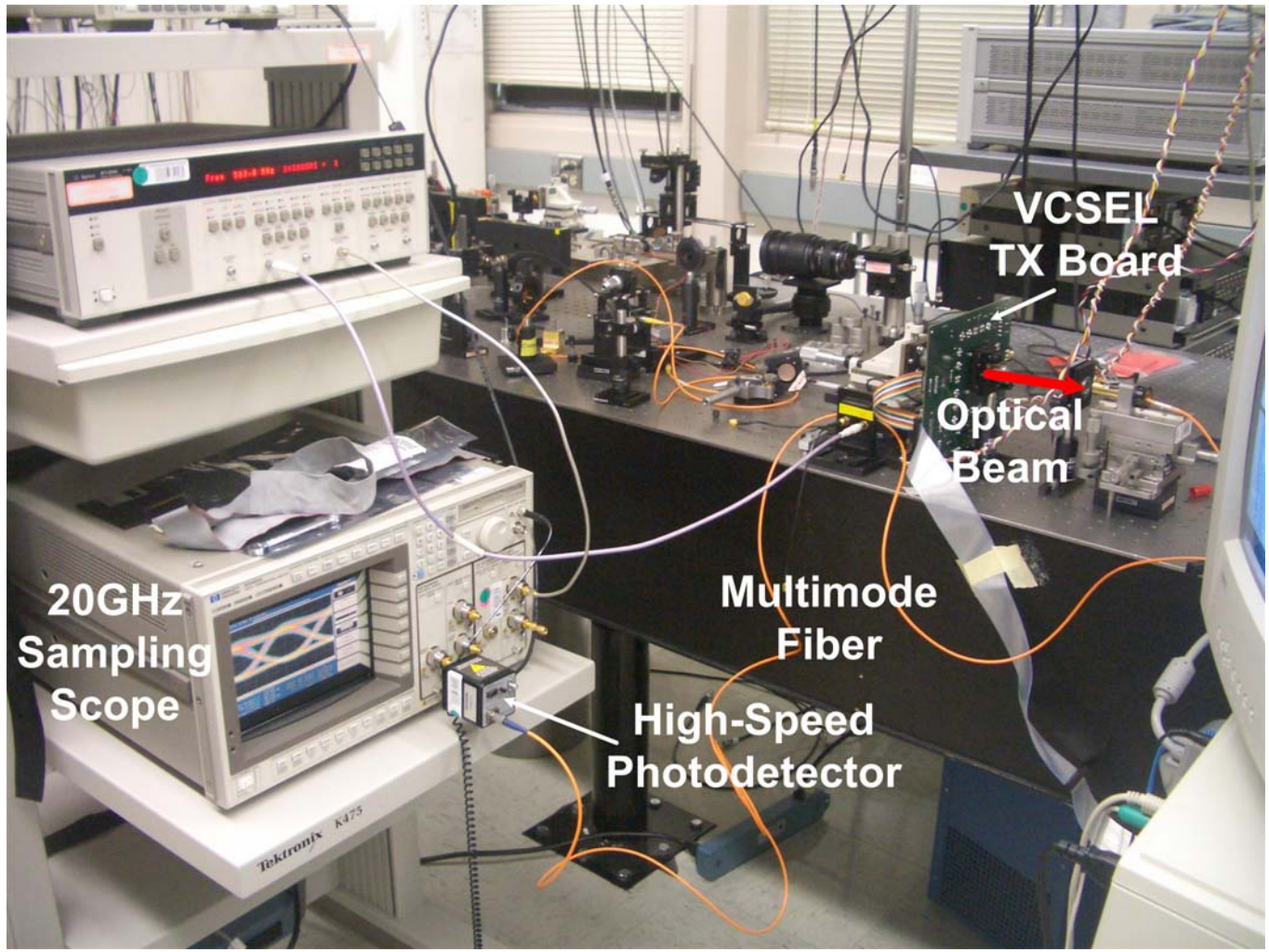


- 5:1 multiplexing predriver uses 5 pairs of complementary clock phases spaced by a bit time
- Tunable delay predriver compensates for static phase offsets and duty cycle error

VCSEL TX Optical Testing



Wirebonded
10Gb/s VCSEL



VCSEL 16Gb/s Optical Eye Diagrams

I_{avg}=6.2mA, ER=3dB

No Equalization

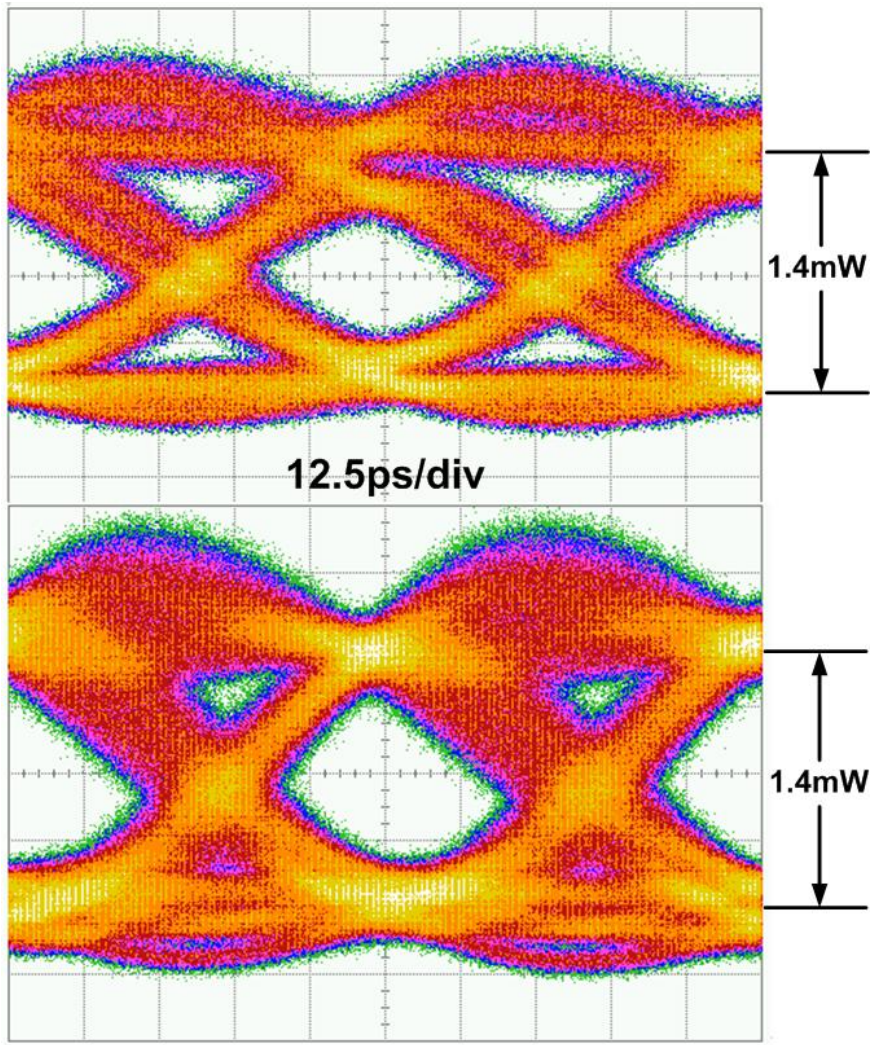
I_{DC} = 4.37mA
I_{MOD} = 3.66mA

w/ Equalization

I_{DC} = 3.48mA
I_{-1} = -0.70mA
I_0 = 4.36mA
I_1 = -0.19mA
I_2 = 0.19mA

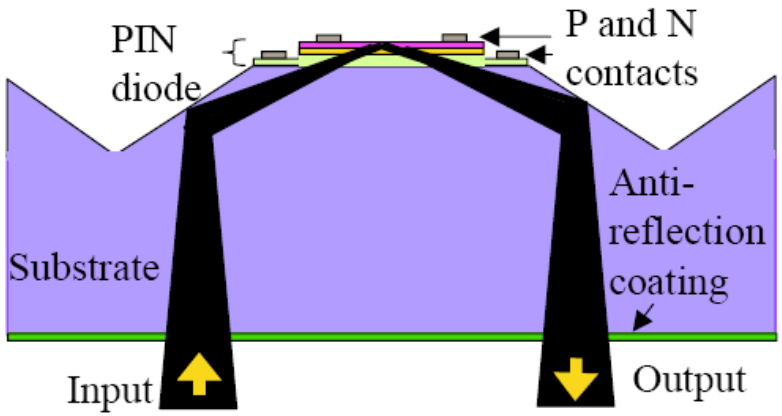
Equalization increases vertical eye opening

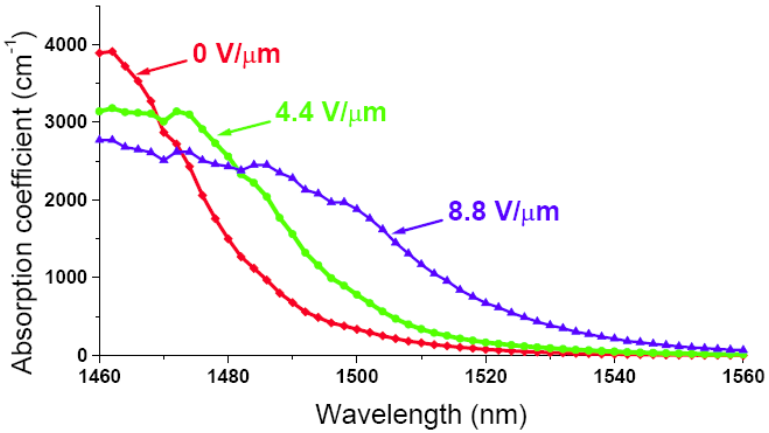
45% at 16Gb/s



External Modulation with MQWM

QWAFEM Modulator*



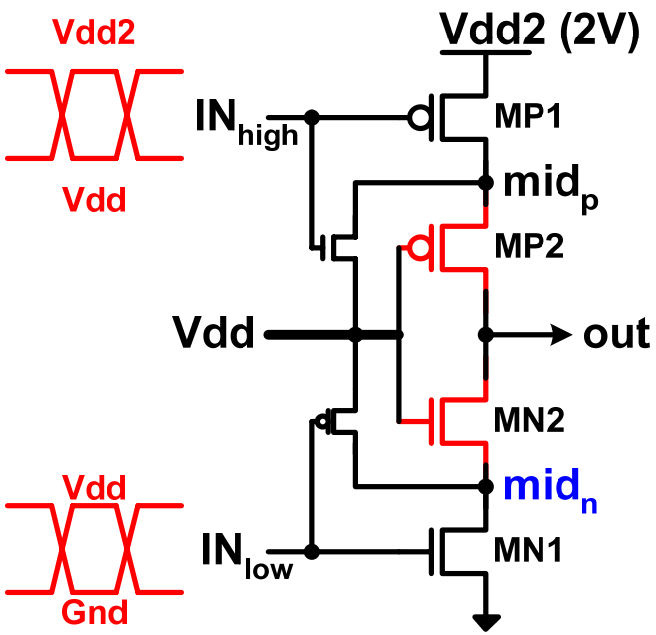


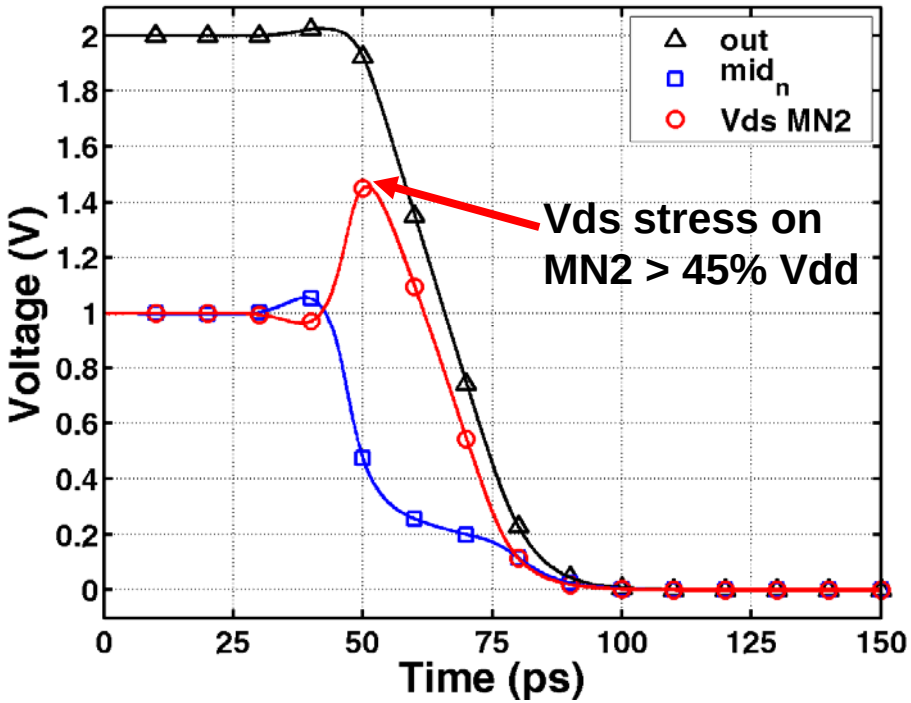
- Absorption edge shifts with changing bias voltage due to the “quantum-confined Stark effect” and modulation occurs
- Maximizing voltage swing allows for good contrast ratio over a wide wavelength range

*N. Helman *et al*, “Misalignment-Tolerant Surface-Normal Low-Voltage Modulator for Optical Interconnects," *JSTQE*, 2005.

High-Voltage Output Stage Issues

Cascode Driver*

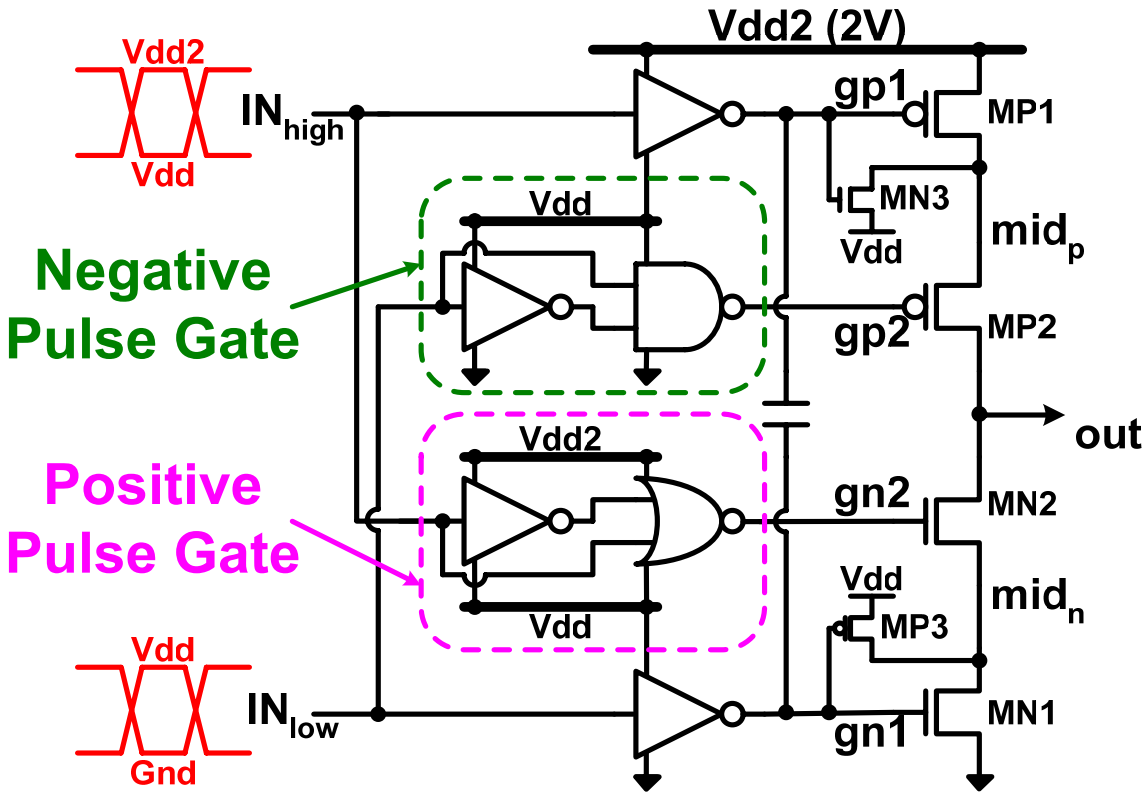




- ☺ Cascode driver has potential for 2x Vdd drive at high speed
- ☹ Static-biased cascode suffers from V_{ds} stress during transients

*T. Woodward *et al*, "Modulator-Driver Circuits for Optoelectronic VLSI," *IEEE Photonics Technology Letters*, 1997.

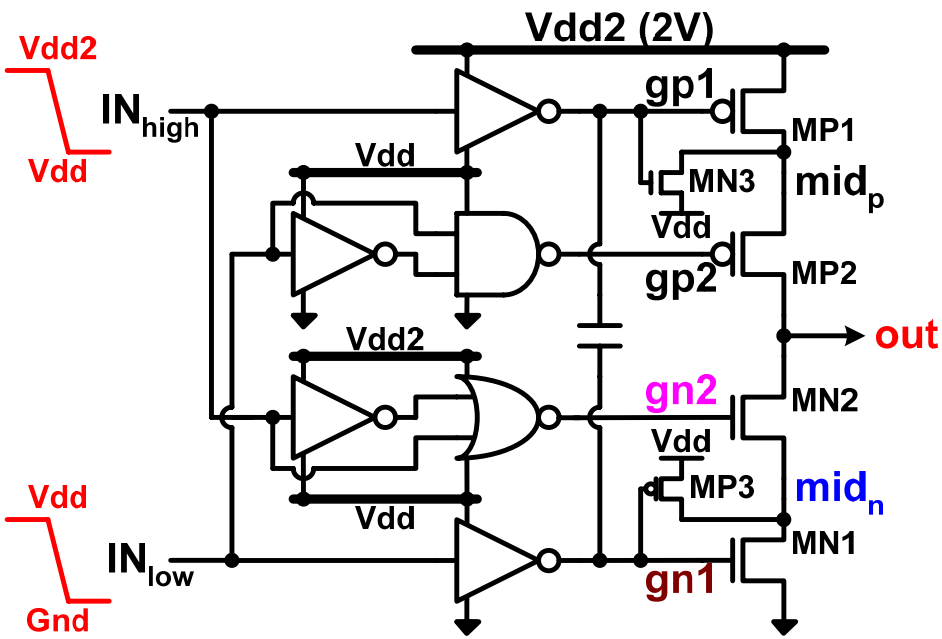
Pulsed-Cascode Output Stage

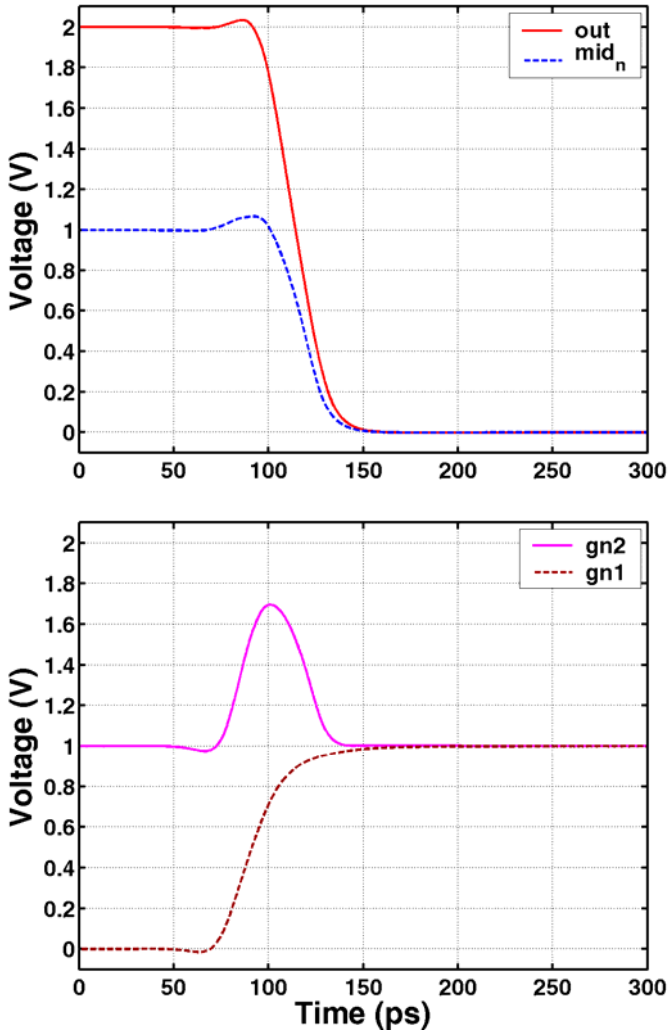


- Preserves two-transistor stack configuration for maximum speed
- Cascode transistors' gates pulsed during transitions to prevent V_{ds} overstress

S. Palermo and M. Horowitz, "High-Speed Transmitters in 90nm CMOS for High-Density Optical Interconnects," *ESSCIRC*, 2006.

Output Stage Waveforms





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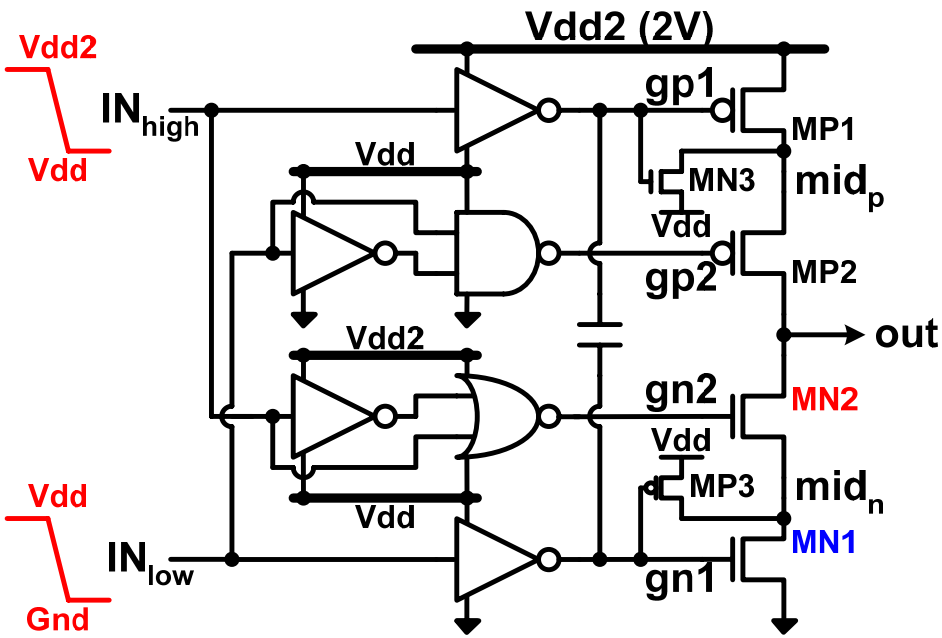
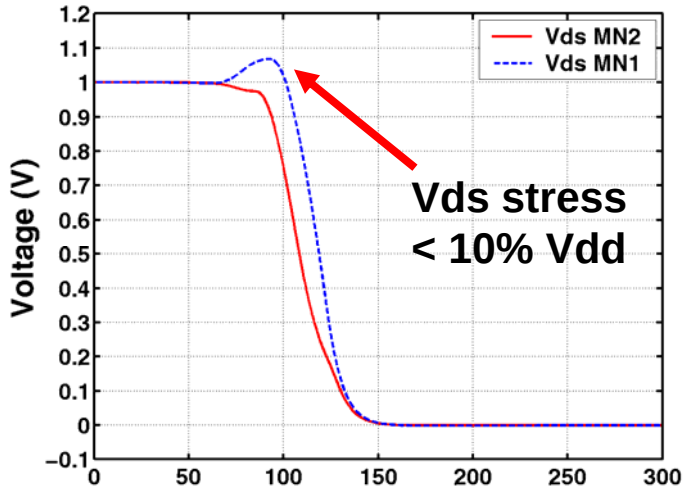
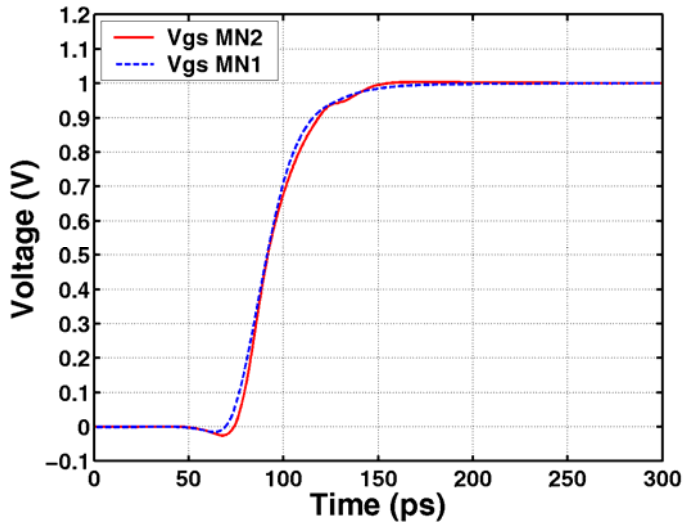
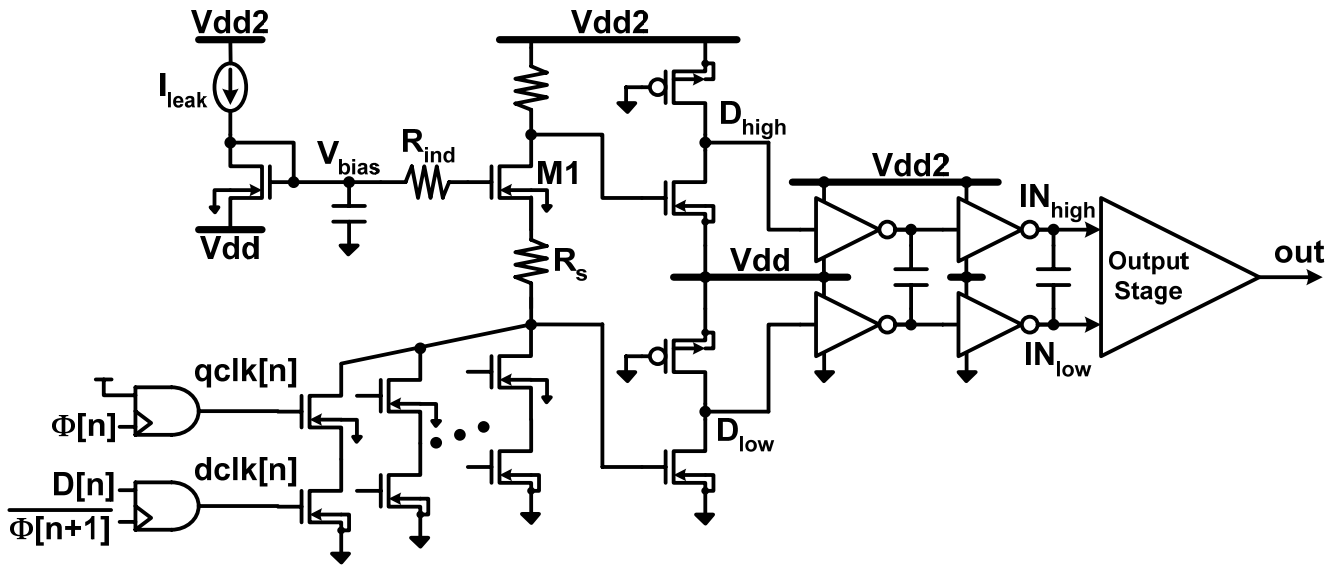




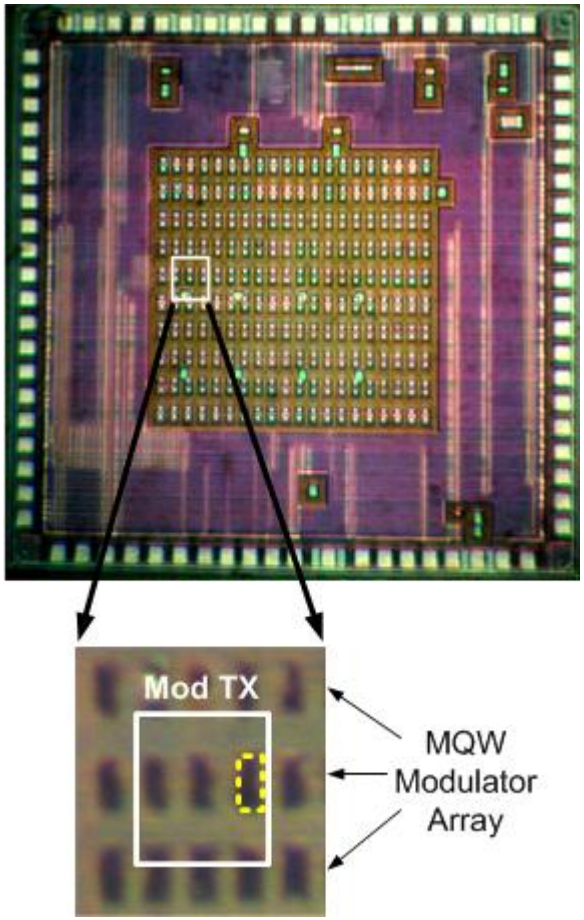


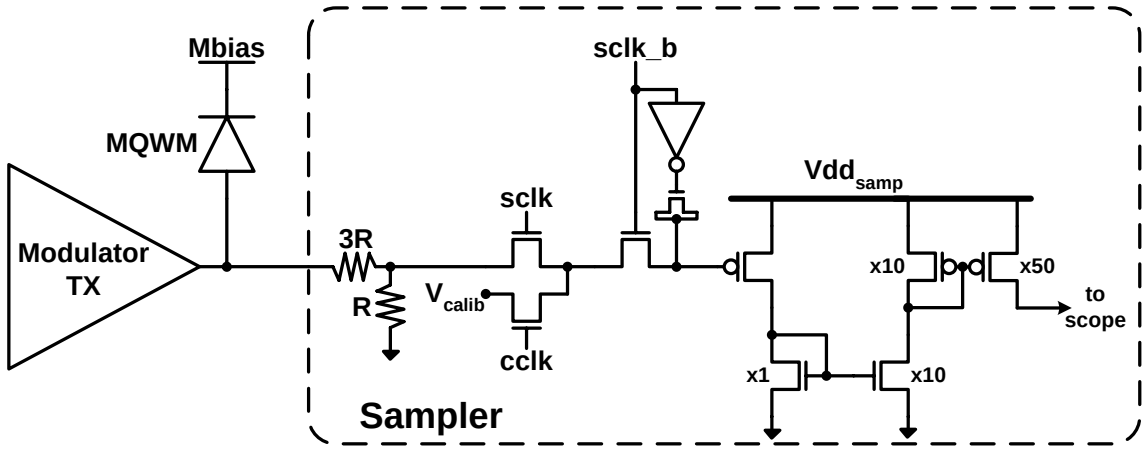
Modulator TX with Level-Shifting Multiplexer



- Level-shifter combined with multiplexer
- Active inductive shunt peaking compensates multiplexer self-loading (reduces transition times by 37%)
- Slightly lower fan-out ratio in “high” signal path to compensate for level-shifting delay
- Delay Tracking
  - “High” path inverter nMOS in separate p-well
  - Metal fringe coupling capacitors perform skew compensation

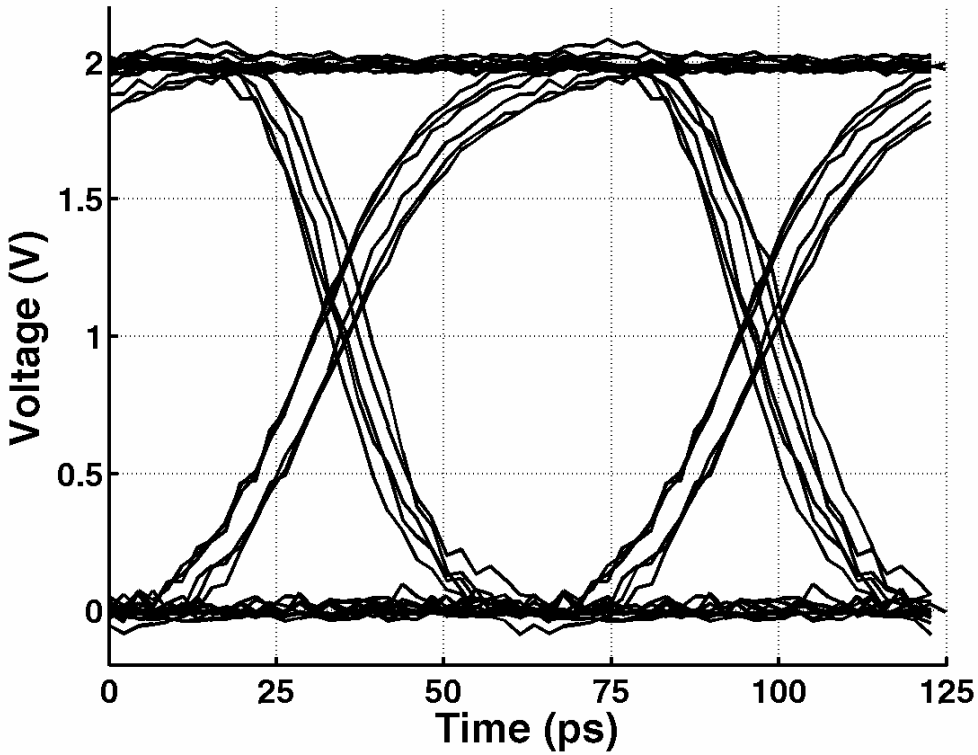
MQWM TX Testing





Electrical sampler at modulator transmitter output

Modulator Driver Electrical Eye Diagram



- 16Gb/s data subsampled at modulator driver output node
- Experimental full optical link operation at 1.8Gb/s*
  - Limited by excessively high contact resistance

*J. Roth, **S. Palermo** *et al*, "An optical interconnect transceiver at 1550nm using low voltage electroabsorption modulators directly integrated to CMOS," *JLT*, 2007.

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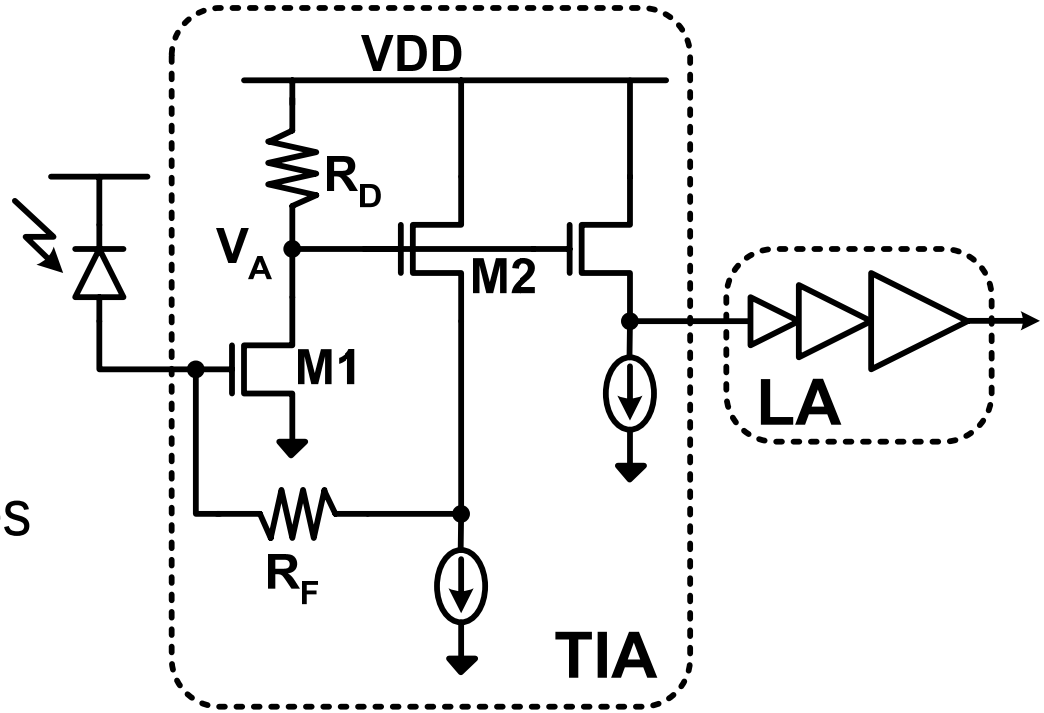
Optical RX Scaling Issues

- ☺ Traditionally, TIA has high R_T and low R_{in}

$$R_T = R_F\left(\frac{A}{1+A}\right)$$

$$\omega_{3dB} \approx \frac{1+A}{R_F C_{IN}}$$

- ☹ Headrooom/Gain issues in 1V CMOS
  - A ≈ 2 – 3



$$V_A = V_{GS1} + V_{GS2} \approx 0.8 * VDD$$

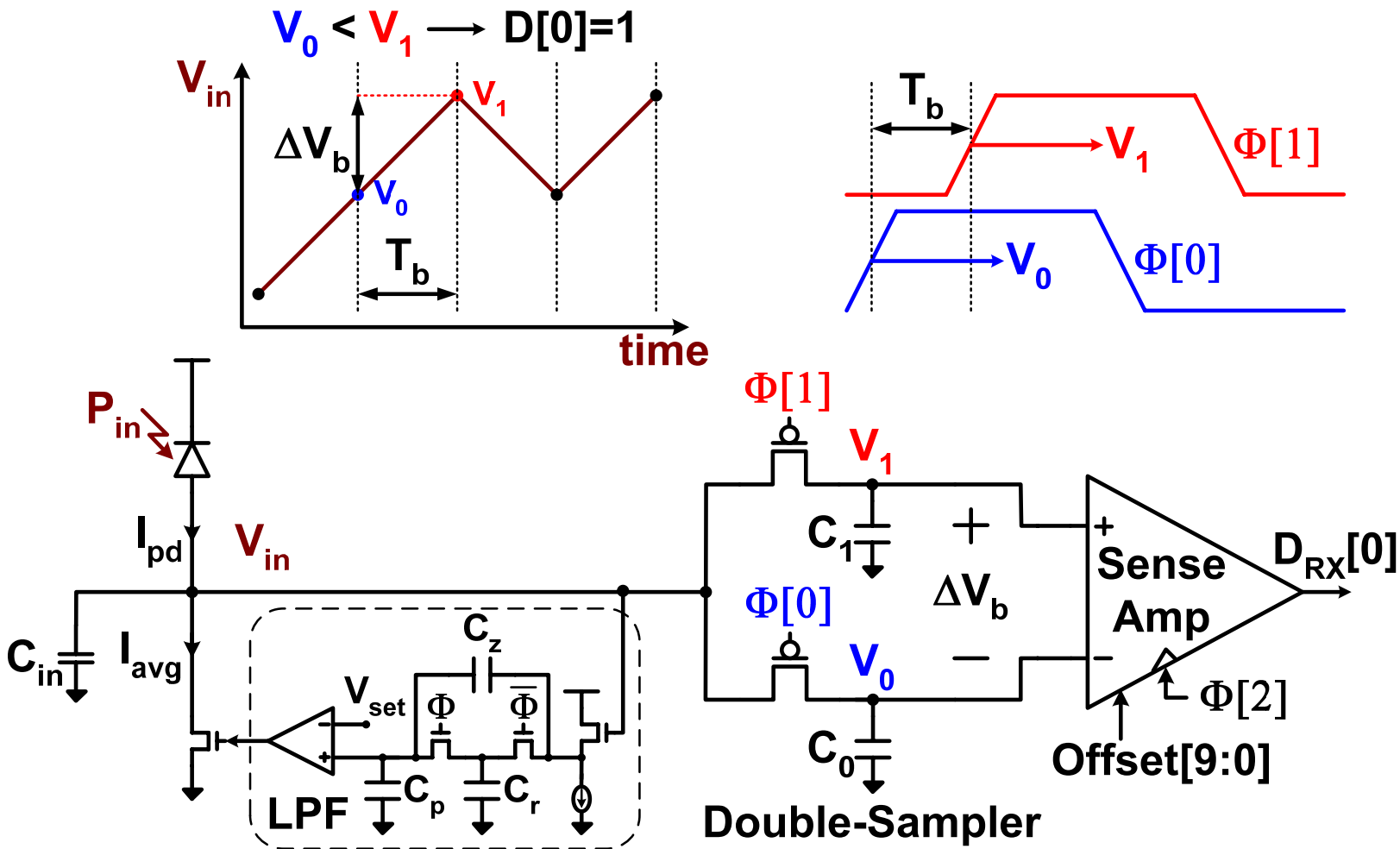
$$A \approx g_{m1} R_D = \frac{\alpha(VDD - V_A)}{VOD} \approx \frac{\alpha(0.2 * VDD)}{VOD}$$

- ☹ Power/Area Costs

$$\text{TIA } I_D \propto (R_T C_{IN})^2 f_{3dB}^4$$

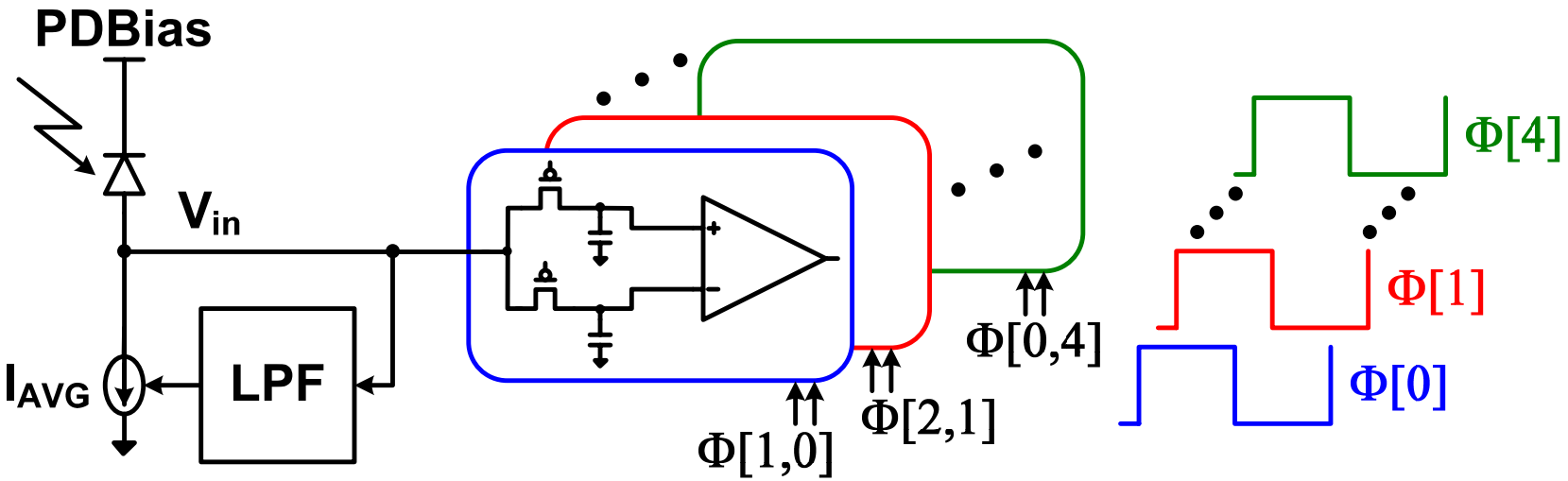
$$\text{LA } I_D \propto f_{3dB}^2$$

Integrating Receiver Block Diagram



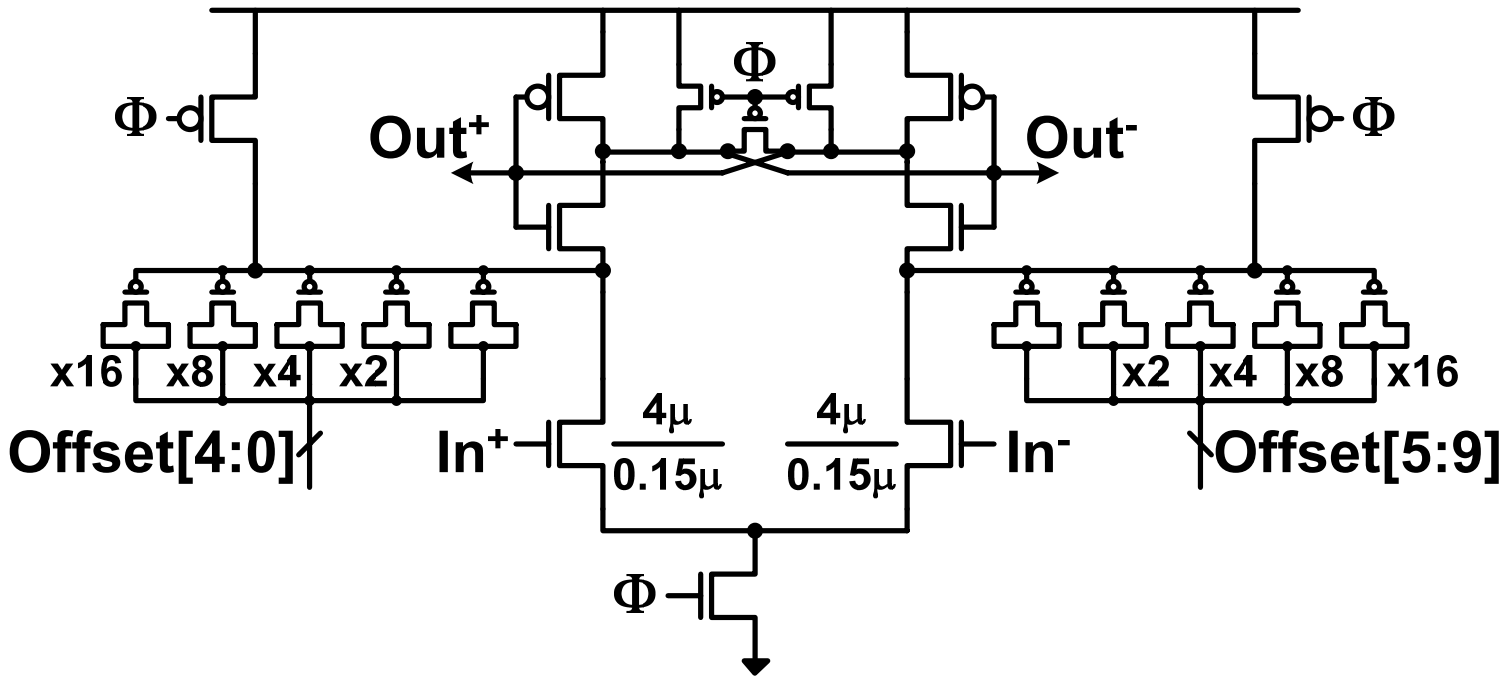
A. Emami-Neyestanak *et al*, "A 1.6Gb/s, 3mW CMOS receiver for optical communication," *VLSI*, 2002.

Demultiplexing Receiver



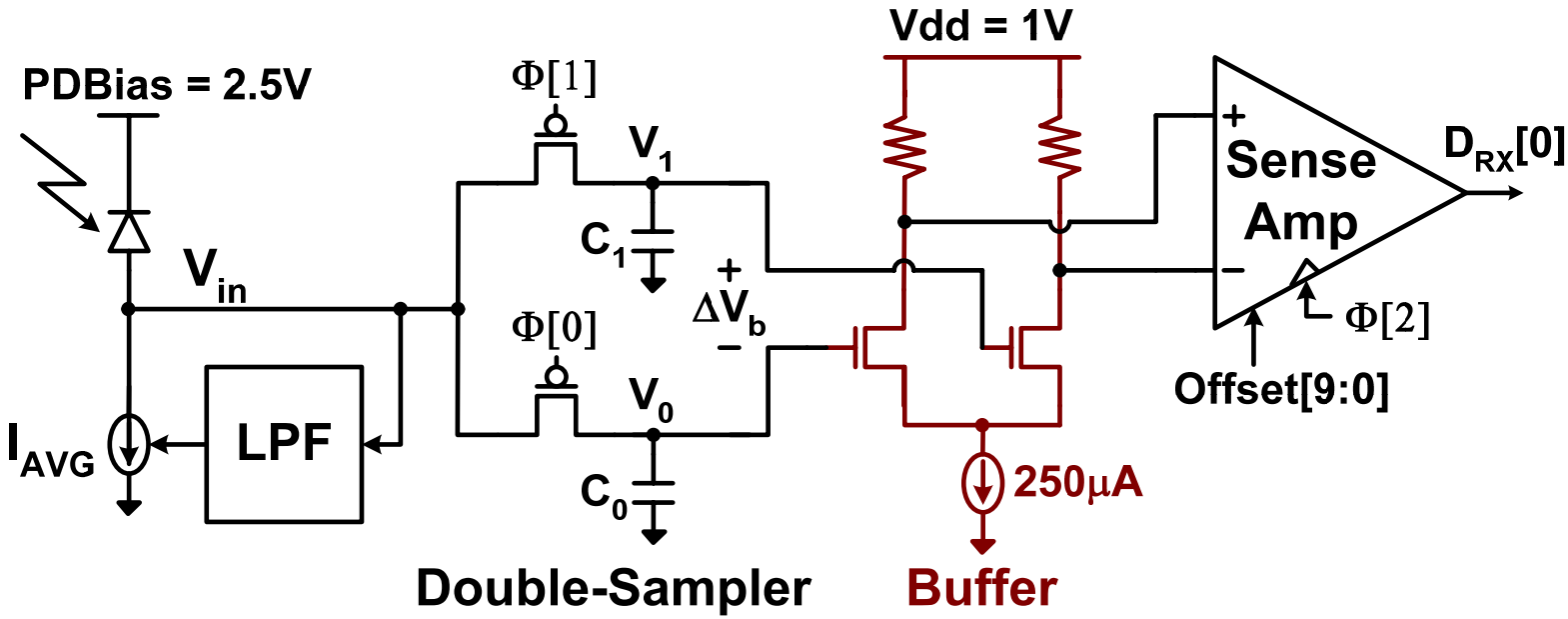
- Demultiplexing with multiple clock phases allows higher data rate
  - Data Rate = #Clock Phases x Clock Frequency
  - Gives sense-amp time to resolve data
  - Allows continuous data resolution

Clocked Sense Amplifier



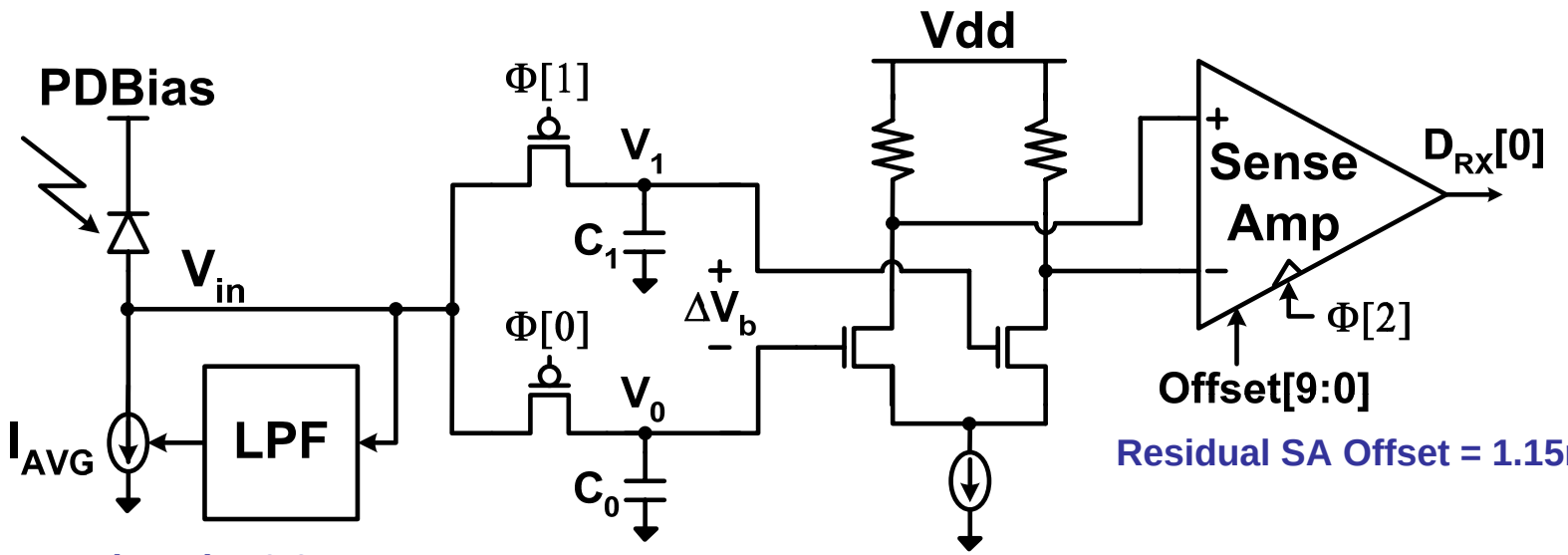
- Offset cancelled with digitally adjustable PMOS capacitors
  - Step=2.3mV, Range=±70mV
- Kickback charge can corrupt adjacent samples
- Need high common-mode input for adequate speed

1V Modified Integrating Receiver



- Differential Buffer
  - ☺ Fixes sense-amp common-mode input for improved speed and offset performance
  - ☺ Reduces kickback charge
  - ☹ Cost of extra power and noise
- Input Range = 0.6 – 1.1V

Receiver Sensitivity Analysis



$$\sigma_{samp} = \sqrt{\frac{2kT}{C_{samp}}} = 0.92mV \qquad \sigma_{buffer} = 1.03mV \qquad \sigma_{SA} = 0.45mV$$

$$P_{avg} = \frac{\Delta V_b \left(C_{pd} + C_{in}\right)}{\rho T_b}$$

Clock Jitter Noise $\sigma_{clk} = \left(\frac{\sigma_j}{T_b}\right)\Delta v_b \approx 0.65mV$ **at 16Gb/s**

Total Input Noise $\sigma_{tot} = \sqrt{\sigma_{samp}^2 + \sigma_{buffer}^2 + \sigma_{SA}^2 + \sigma_{clk}^2} = 1.59mV$

ΔV_b for BER = 10^{-10} = $6.4\sigma_{tot}$ + Offset = 11.9mV

Gb/s	P_{avg} (dBm)
10	-9.8
16	-7.8

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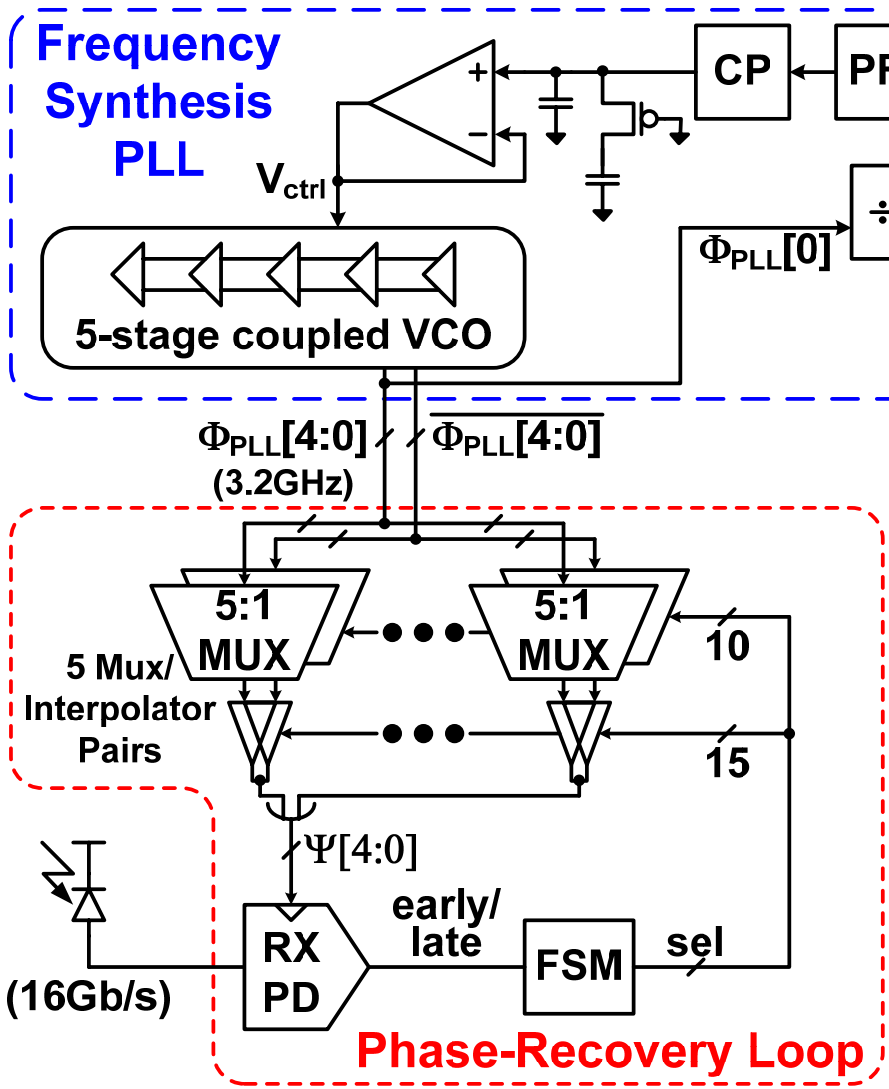
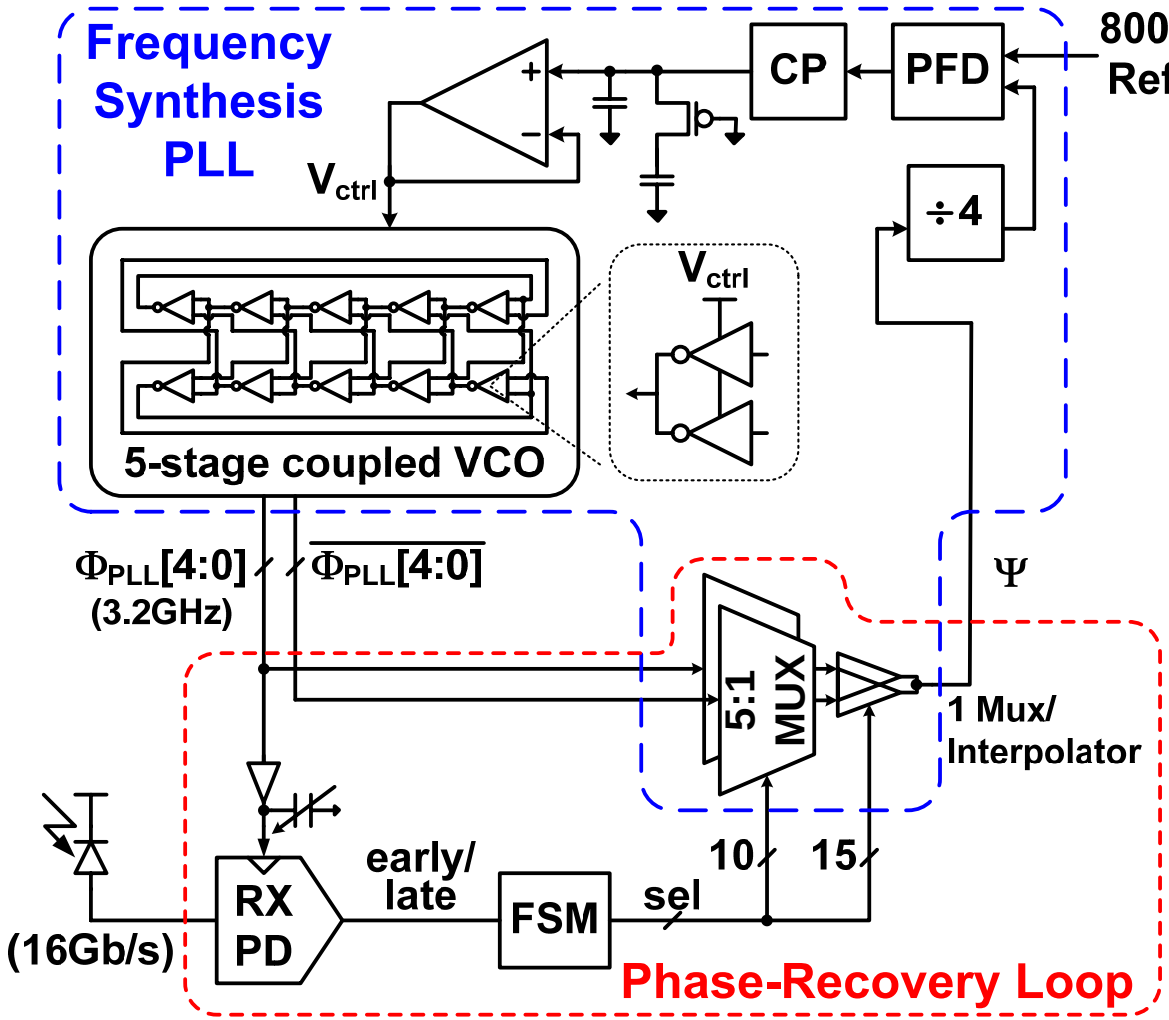
Conventional Dual-Loop CDR



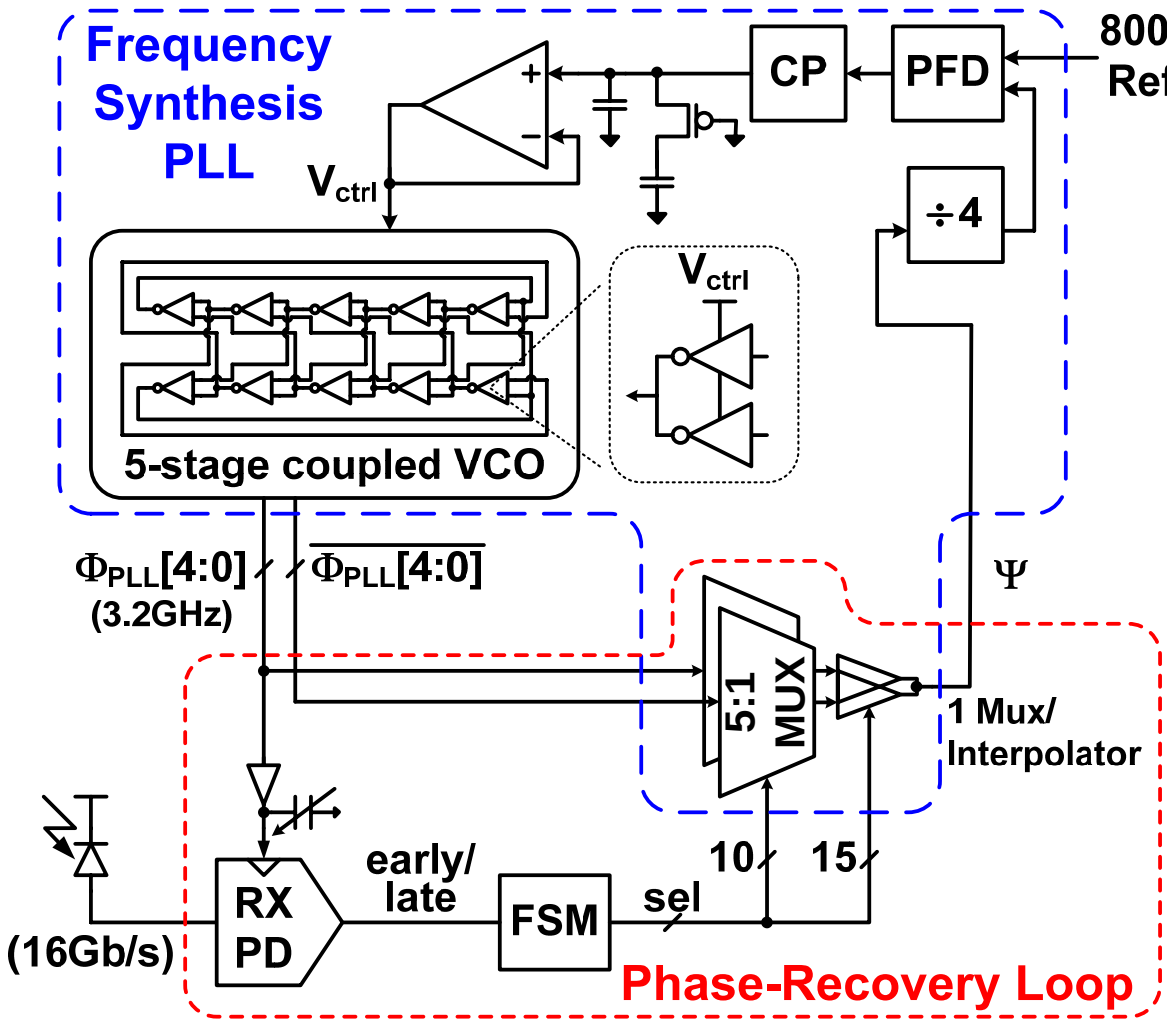
- ☺ 2 degrees of freedom to filter VCO noise & erroneous phase updates
- ☹ Input demultiplexing receiver requires multiple phase muxes & interpolators

Dual-Loop CDR w/ Feedback Interpolation



- Extends [Larsson:99] to input demultiplexing receiver
- Only one phase mux/interpolator pair
- Filtering of interpolator switching
- Path from VCO to samplers
  - Minimal Delay
  - Static – allows offset cancellation

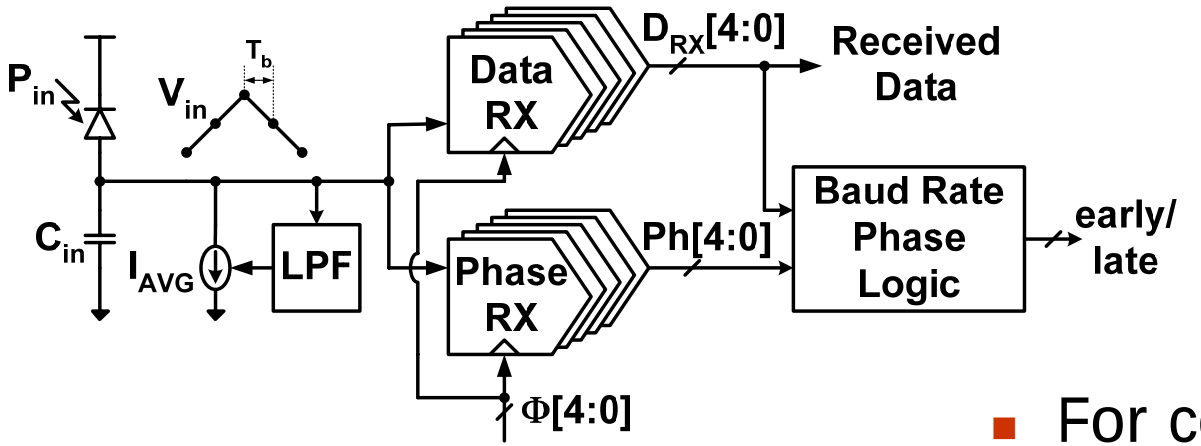
Dual-Loop CDR w/ Feedback Interpolation

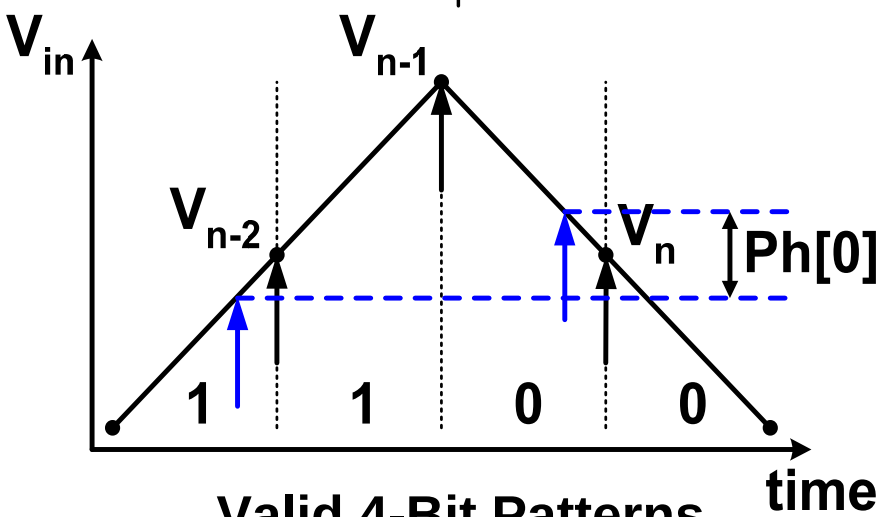


Frequency loop bandwidth = 40MHz to minimize VCO noise

Phase loop bandwidth < 4MHz to minimize input noise

Baud-Rate Phase Detection



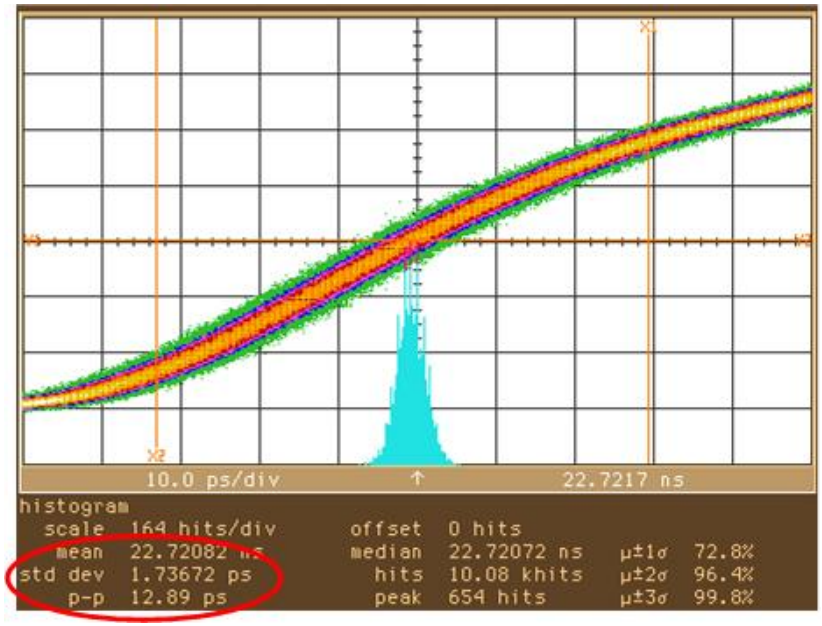


Valid 4-Bit Patterns
0011, 1100, 0010, 0100, 1011, 1101

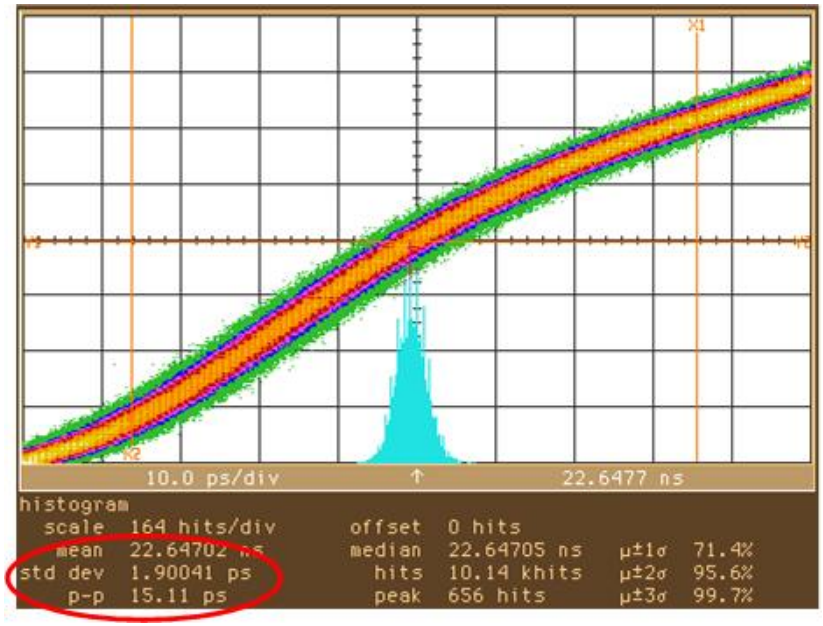
- For certain 4-bit patterns compare $V_{in}(n)$ with $V_{in}(n-2)$ [Emami:04]
- ☺ No "quadrature" phases required
- ☹ Reduces net update rate to 18.75%

Clock Recovery Performance

CDR Disabled



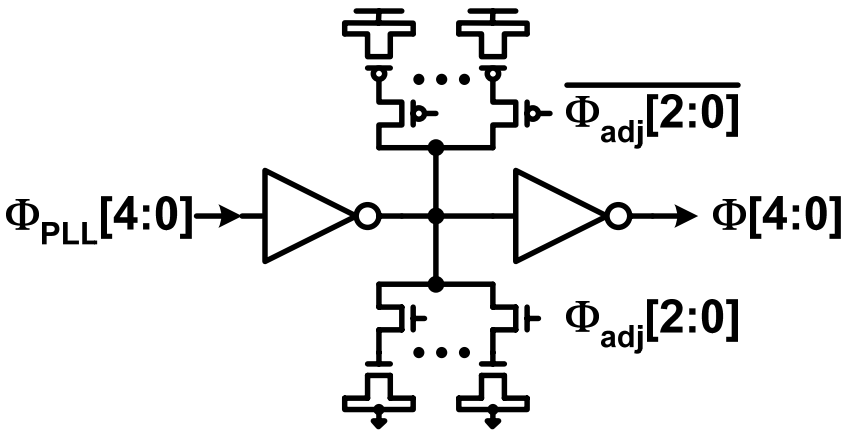
CDR Activated



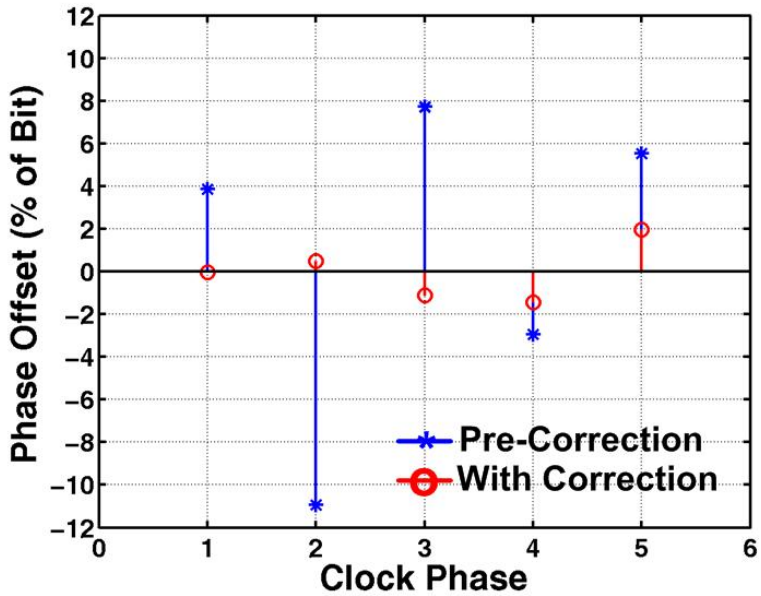
- RX clock frequency = 3.2GHz (16Gb/s)
- Jitter increases only marginally when CDR activated
  - $1.74ps_{rms}$, $12.9ps_{pp}$ » » $1.90ps_{rms,}$ $15.1ps_{pp}$
  - Sufficient filtering of input noise

Phase Correction Circuitry

Tunable Delay Clock Buffers



Phase Correction Performance

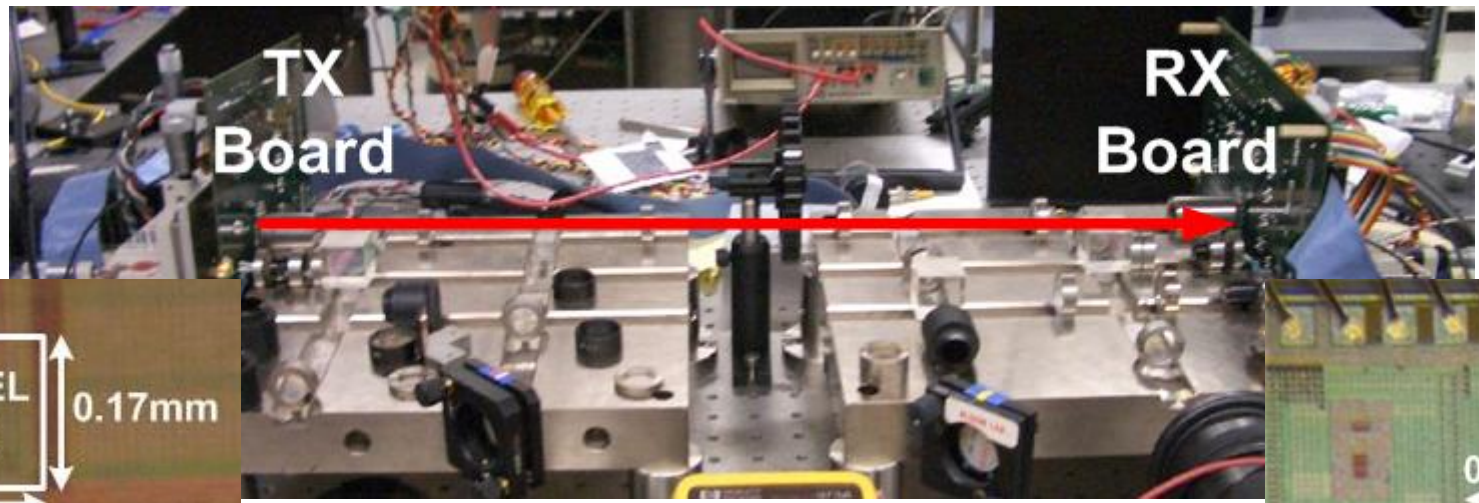


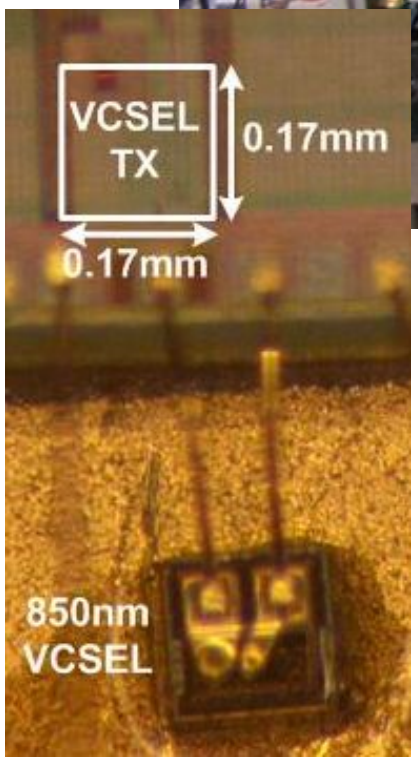
- Static phase offset corrected with tunable delay clock buffers
  - Digitally-adjustable capacitive loads
  - Phase range at 16Gb/s is ±12% UI

Outline

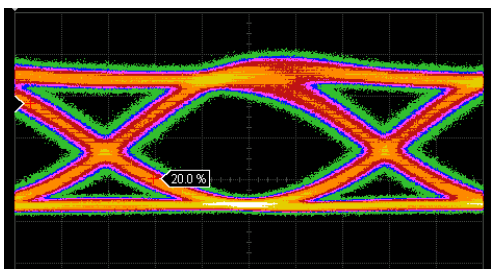
- Introduction
- Optical transmitters
- Optical receiver
- Clock and data recovery
- Optical link system performance
  - VCSEL link
- Conclusion

Optical Transceiver Testing

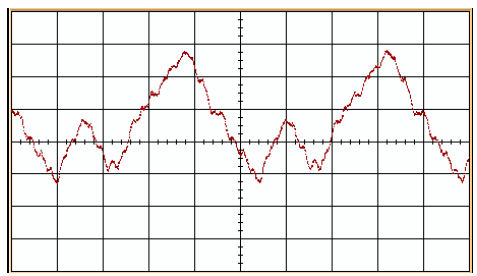


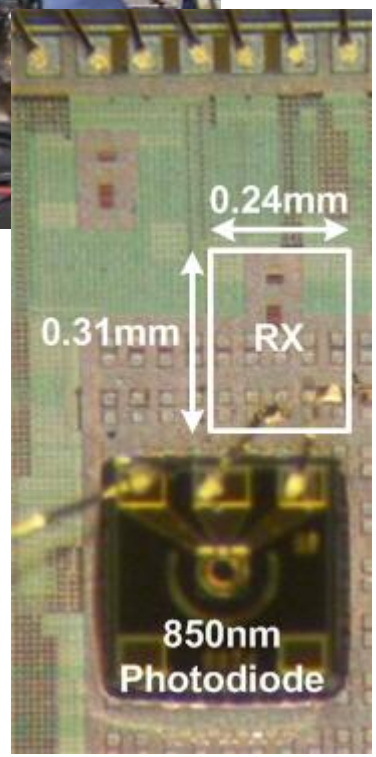


Transmitted Bits



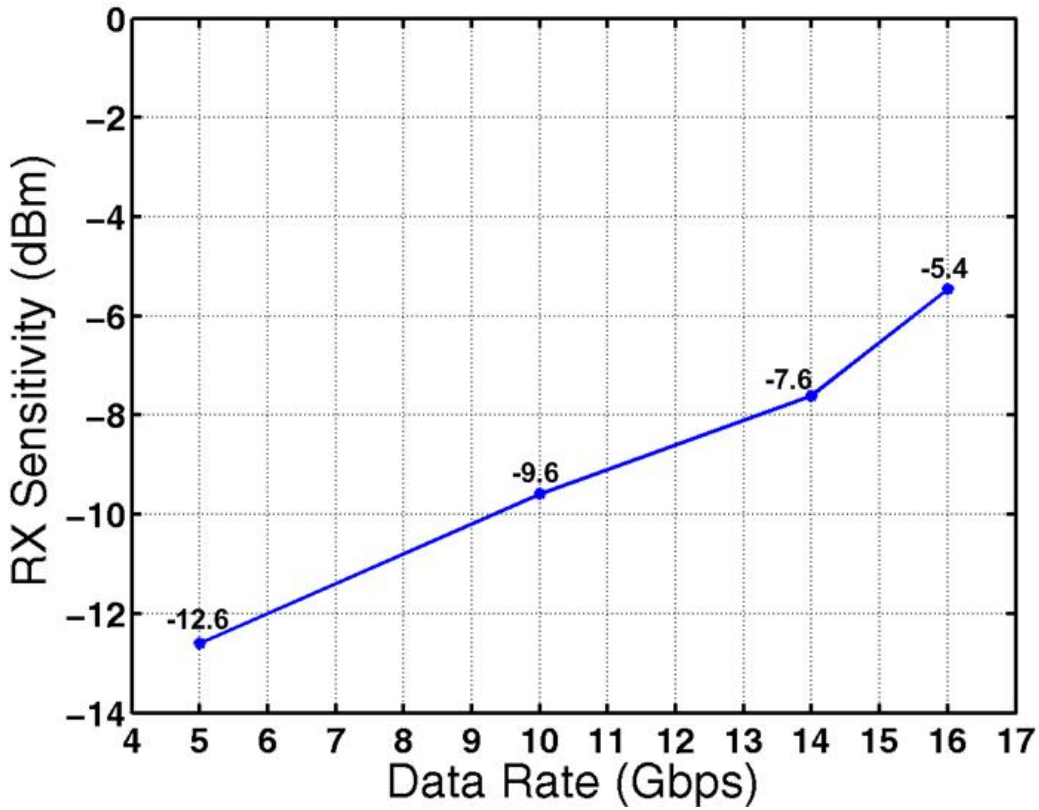
RX Input Node



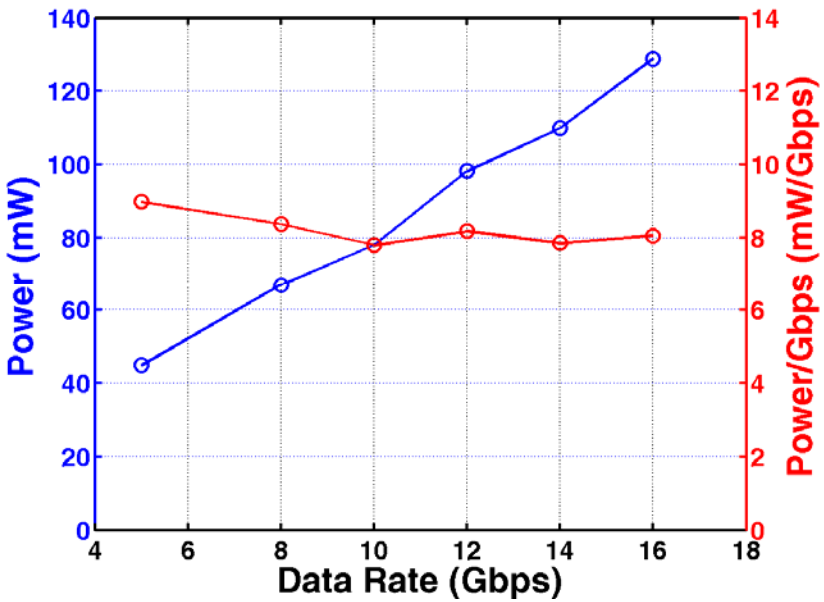


Receiver Sensitivity

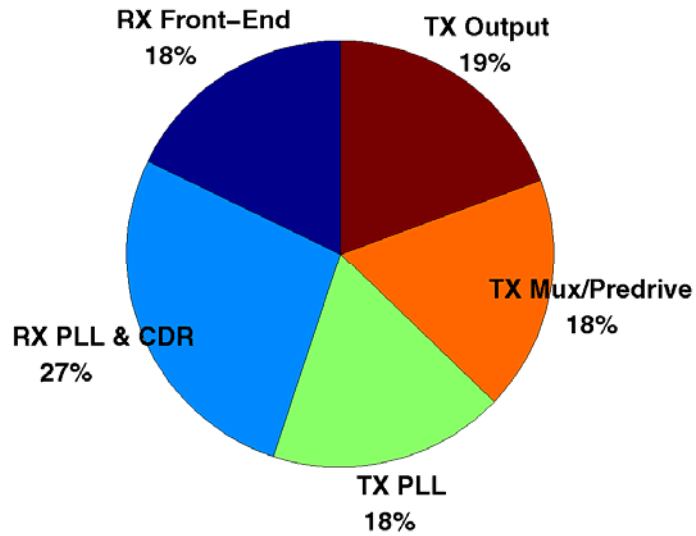
- Test Conditions
  - 8B/10B data patterns (variance of 6 bits)
  - Long runlength data (variance of 10 bits)
- BER < 10^{-10}



Transceiver Power Consumption



Power Breakdown at 16Gb/s

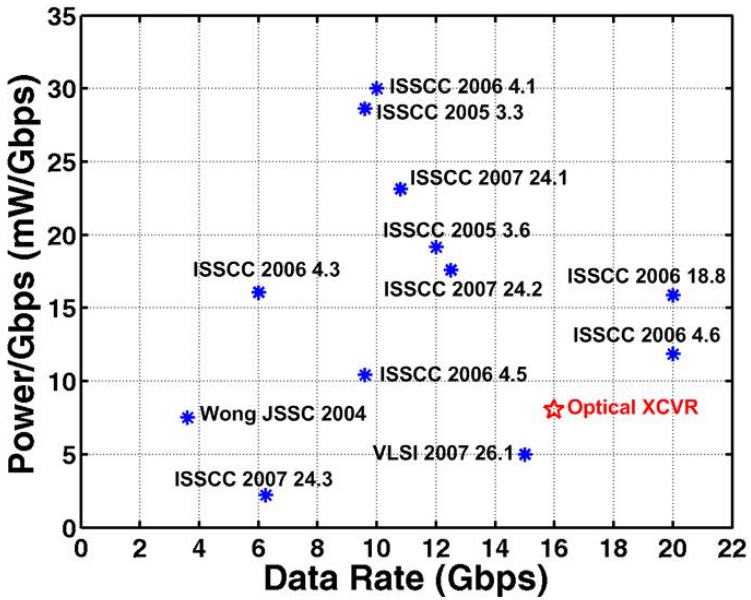


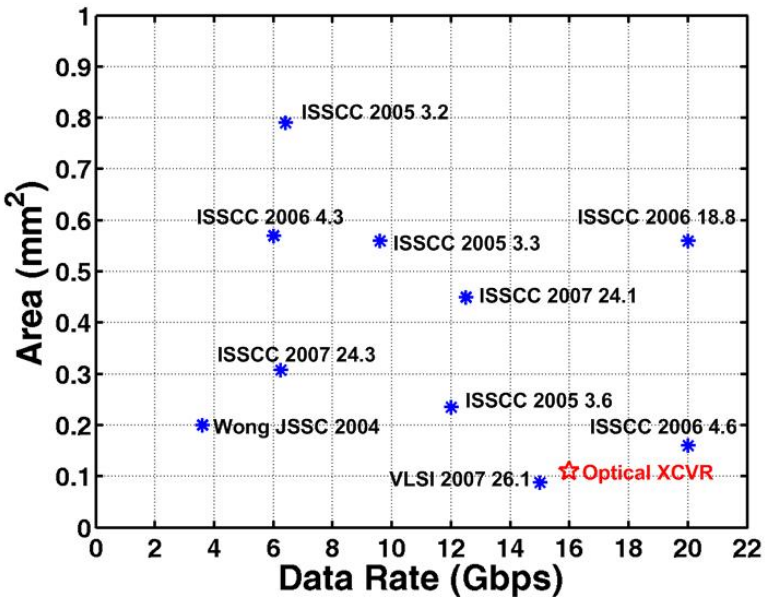
- Power at 16Gb/s = 129mW (8.1mW/Gb/s)
- Power scales with data rate
  - Mostly CMOS circuitry
  - Integrating RX sensitivity improves at lower data rates

Transceiver Performance Summary

Technology	90nm CMOS
Supply Voltages	Vdd=1V, LVdd=2.8V, PDBias=2.5V
Data Rate	5 - 16Gb/s
Extinction Ratio	3dB
Average Optical Launch Power	3.1dBm
RX Input Capacitance	440fF
RX Sensitivity (BER=10^{-10}) 10Gb/s 16Gb/s	 12.5mV (-9.6dBm) 20.2mV (-5.4dBm)
Area	0.105mm^2
Power at 16Gb/s	129mW (8.1mW/Gb/s)

Optical vs Electrical XCVR Performance Comparisons





- Compares favorably due to simple equalization circuitry
- Should scale well
  - Better VCSEL technology
  - Lower capacitance photodetectors
  - Higher data rates $\Rightarrow$ More equalization for electrical channels

Conclusion

- Optical interconnects provide a path to reducing the I/O bandwidth problem
- Proposed optical interconnect architecture is suitable for large scale integration in current/future CMOS technologies
  - VCSEL TX equalizer allows low current operation
  - Reliable MQWM TX capable of 2*Vdd voltage drive
  - Low voltage integrating receiver
  - Baud-rate clock recovery

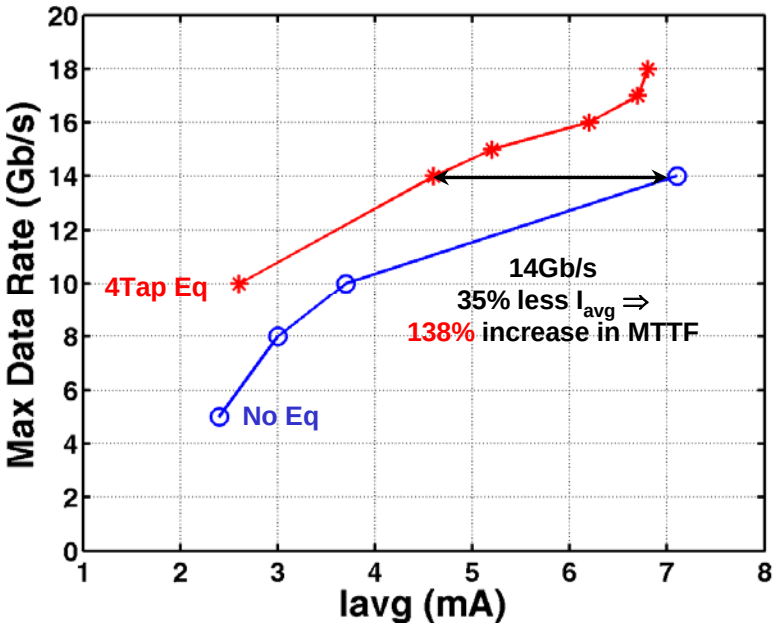
Acknowledgments

- Profs Mark Horowitz, Azita Emami, and David Miller
- Jon Roth for optics/device design of modulator link
- CMP and STMicroelectronics for chip fabrication
- ULM Photonics for VCSELs
- Albis Optoelectronics for photodetectors
- MARCO-IFC for funding support
- Sh. Palermo for encouragement and support

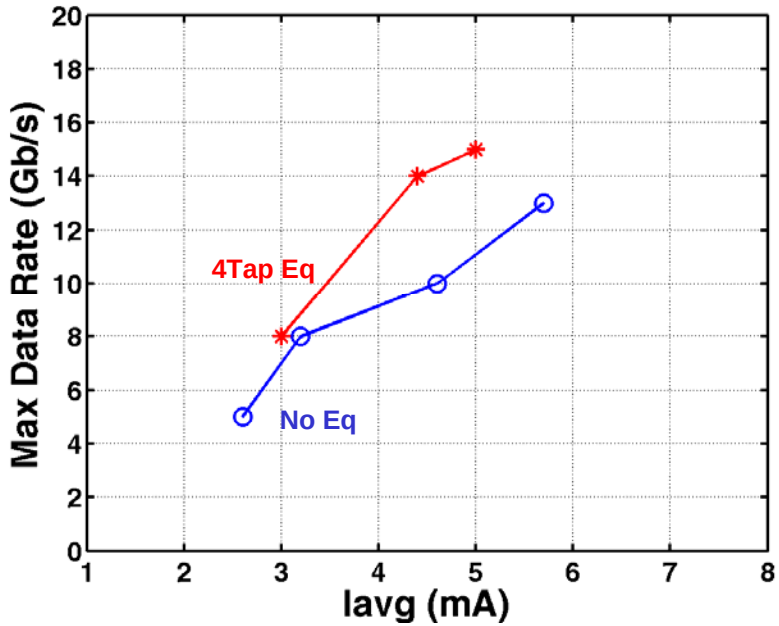
Backup Slides

Equalization Performance

ER=3dB

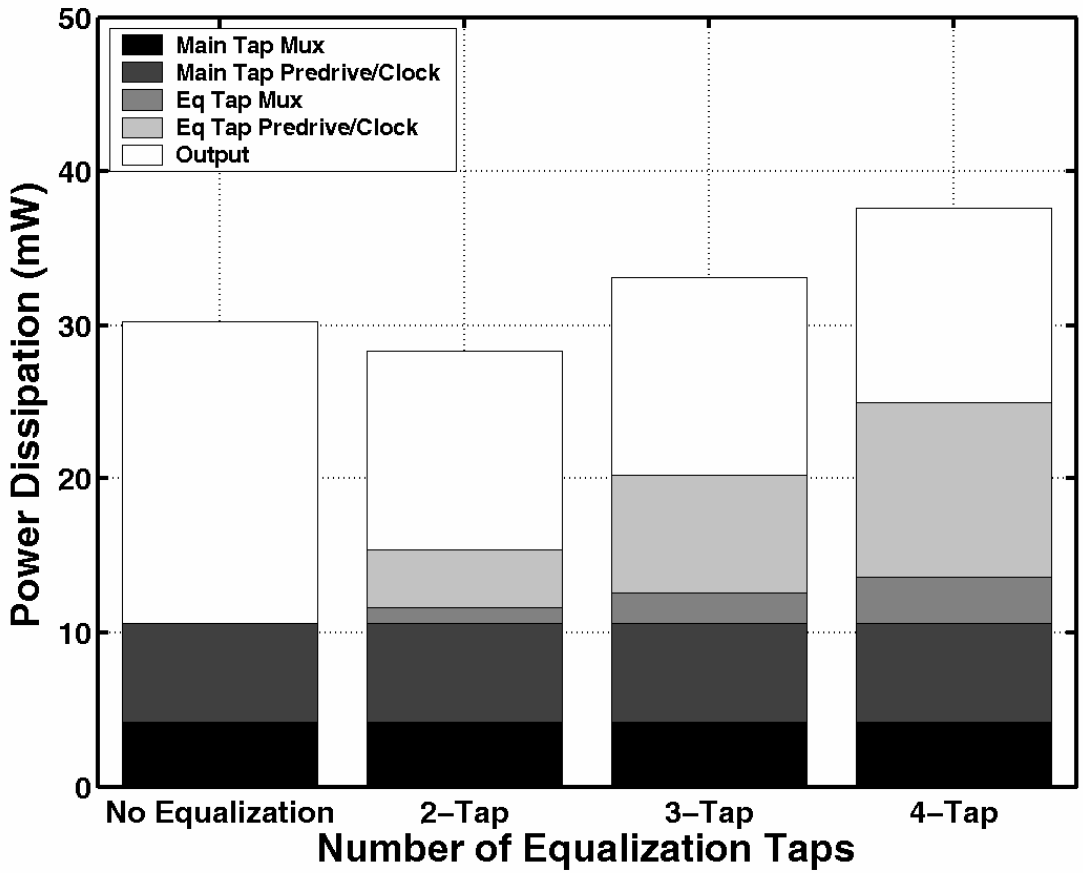


ER=6dB



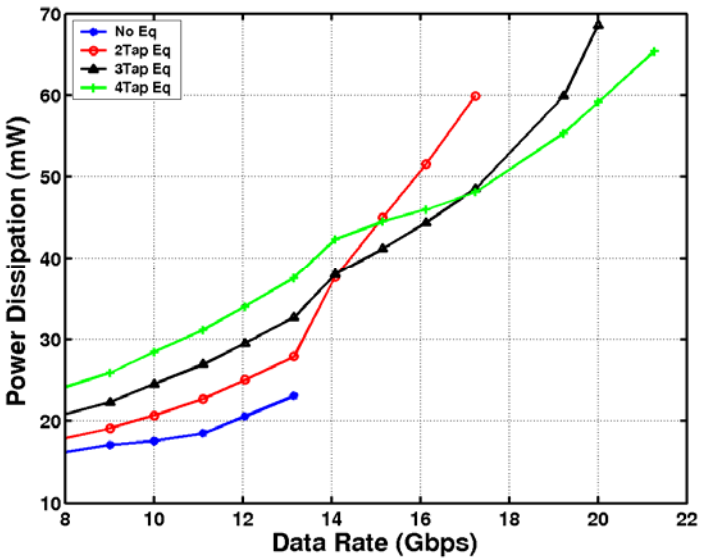
- Maximum data rate vs average current
  - Min 80% eye opening & <40% overshoot
- Equalization allows lower average current for a given data rate
- Linear equalizer limited by VCSEL nonlinearity

13Gb/s Power w/ different tap

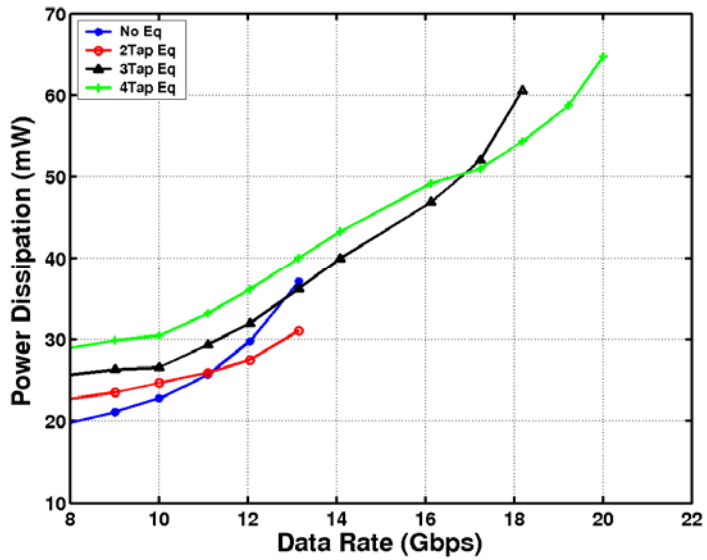


VCSEL TX Power vs Data Rate & Tap

FCB Channel

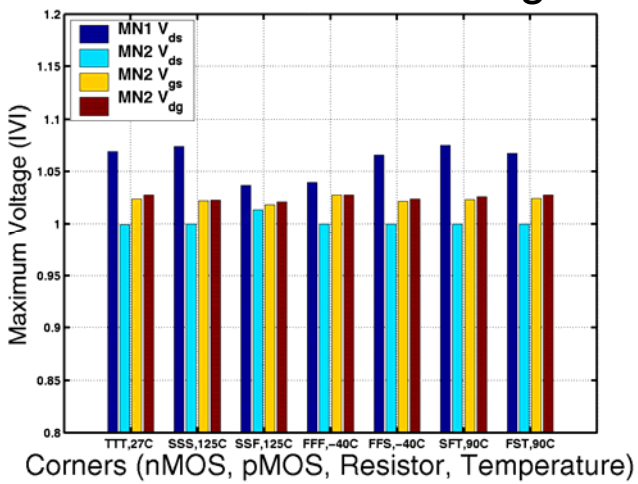


Wirebond Channel

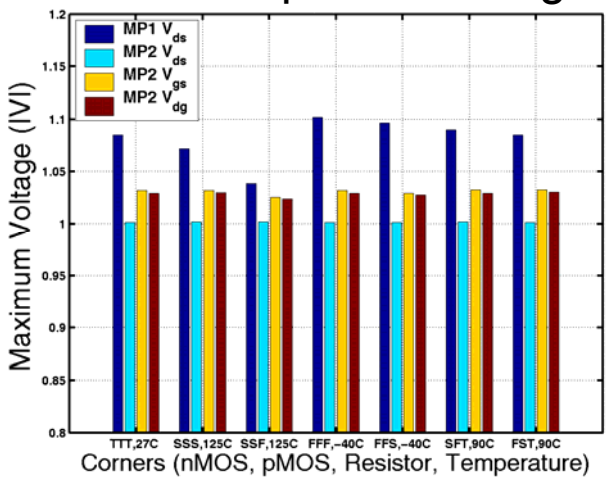


Modulator Driver Reliability Simulations

Maximum nMOS Voltages

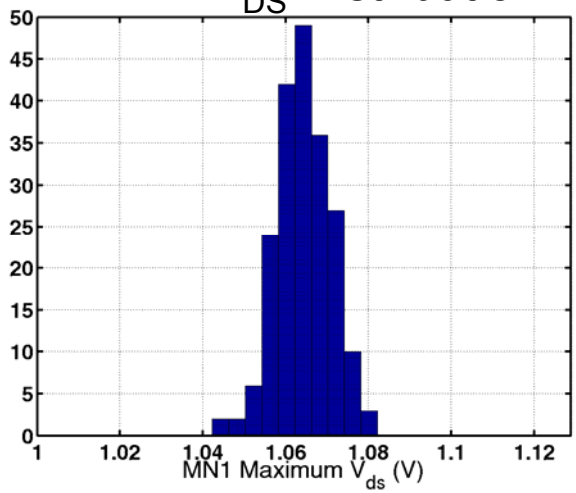


Maximum pMOS Voltages



- Transient with random data
- Corner simulations show no output stage voltages exceed 11% of nominal Vdd
- Monte Carlo simulations show tight distributions (σ < 15mV)

MN1 V_{DS} Distribution



Coupling Capacitor Skew Compensation Performance