On-chip RF Isolation Techniques

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Abstract

On-chip isolation is a function of many interdependent variables. This paper uses industry examples to highlight isolation impacts of technology – substrate doping levels and triple wells, grounding / guard rings, shielding, capacitive decoupling, and package inductance.

Introduction

On-chip isolation is becoming increasingly important due to higher integration levels, higher frequencies, and tighter specifications for next generation products. Higher integration not only results in more transistors switching, and thus, more noise creation, but it also puts noisy and sensitive components together on the same chip that were on separate chips in the past. At higher frequencies noise now couples more easily from place to place. Isolation provided by wells is reduced, and package inductance becomes critical. The package impedance at GHz frequencies may cause on-chip AC grounds to appear to float. When the tighter specifications of next generation products, such as 3G cellular, are added to the picture, the RF designer must be both knowledgeable and creative to find an effective solution. An understanding of the impact of the process technology, grounding effects, guard rings, shielding, decoupling, and package inductance is necessary to optimize isolation. This paper reviews some of the issues and presents industry examples of current techniques that affect on-chip isolation. The challenge in addressing this topic is that most of the effects are interdependent.

Technology Impacts

Most silicon-based RF chips are fabricated in bipolar, BiCMOS, SiGe, or CMOS processes using a lightly-doped bulk, p-type substrate. Heavily doped substrates, most commonly used for large digital designs, like microprocessors, where latch-up concerns dominate isolation and the extra wafer cost can be justified, will not be covered in this paper. See [1] for a basic review of heavily doped substrates. A lightly doped substrate is highly resistive, which typically means a resistivity of around 12 Ohm-cm or a doping concentration around $4x10^{14}$ cm^{-3} for a p-type substrate. Experienced designers will often be able to achieve a few more dB of isolation using a lightly doped substrate than a heavily doped substrate.

Figure 1 shows the cross-section of a BiCMOS process [2]. The channel stop region at the surface of the chip is approximately three orders of magnitude less resistive than the substrate, so breaking the channel stop between two points will increase the isolation between them. The buried layers and

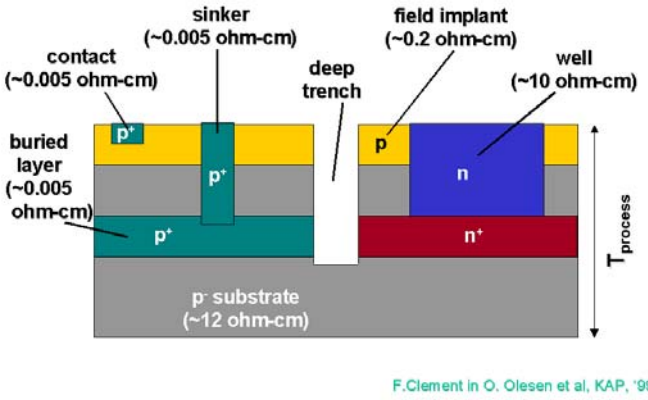

Figure 1: BiCMOS cross-section with relative resistivities.

sinker are roughly four orders of magnitude more conductive than the bulk substrate. If the sinker and buried layer are connected to a low impedance AC ground, they may form a shield and draw carriers away from devices located inside the region. However, buried layers may also provide a low impedance path for noise to travel into a sensitive area. In this case the buried layer must be broken to increase the isolation. Takeshita of Sony presented an exam-

ple of this at ISSCC'02 [3] as illustrated in Figure 2. The break in the buried layer combined with the addition of a double guard ring provided a 20x improvement in the isolation.

Triple wells, sometimes referred to as "deep nwells", are now common options in most CMOS processes at 0.18 μm and below. Figure 3 shows the cross-section of a triple well along with measured isolation results as presented by Redmond of Motorola at ISSCC'02 [4]. Although not shown in the figure, the nwell containing the isolated pwell is fabricated with a greater depth than the standard nwell. Some less common process options may include an n-type sinker and a heavily-doped n-type buried layer at the bottom of the nwell. The triple well provides a means to isolate the n-type devices that would normally exist in the p substrate. The effectiveness of triple-well isolation depends on the signal frequencies, the doping levels, the grounding schemes, and the package.

One data point for the isolation added by using a triple well is the roughly 20 dB of isolation shown in the graph in Figure 3. Three curves exist in the plot. The top curve represents the intrinsic substrate isolation of the heavily doped substrate. The middle curve is for a guard ring, and the lower curve is for the triple well. Since the process used a heavily doped substrate, the guard ring would not be expected to show the same level of isolation as in a lightly doped substrate. Additional simulation data points are found in Figure 4 for a lightly doped sub-

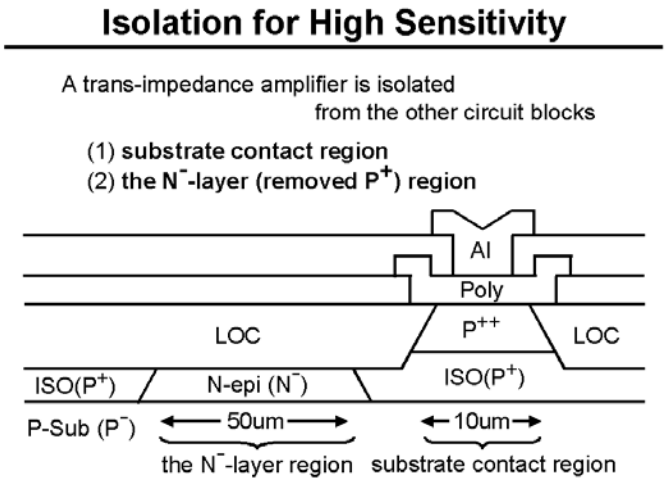

Figure 2: Sony ISSCC'02 example of breaking the buried layer to reduce coupling through the ISO(P^+) region.

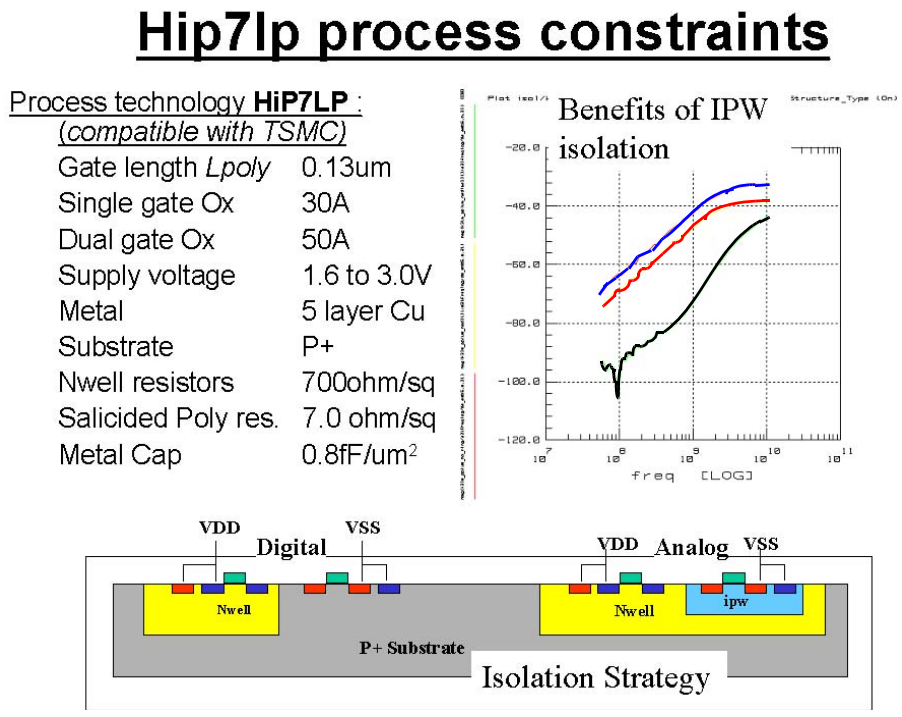

Figure 3: Motorola ISSCC'02 triple-well example showing approximately 20 dB additional isolation. The top curve is with no triple well or guard ring. The middle curve shows the isolation added by a guard ring, while the bottom curve is the triple well isolation.

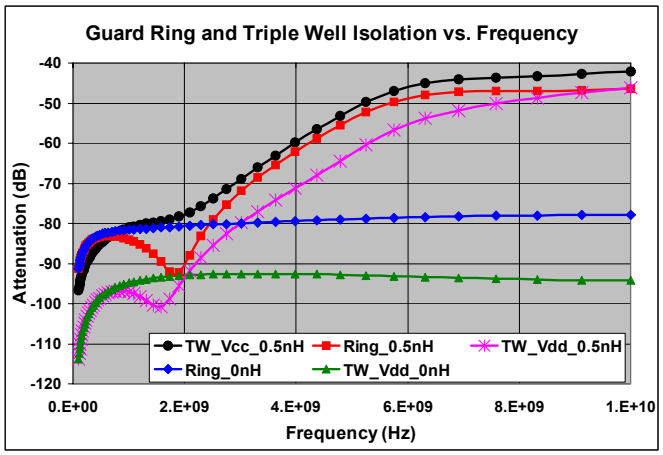

Figure 4: Comparison of guard ring and triple-well isolation versus frequency with and without 500 pH of bond wire inductance.

strate. These data points and the ones in the graphs to follow were obtained using SubstrateStorm™ [5] to generate the substrate model for simulation. The five lines in Figure 4 represent the isolation between a noise source and two different receiver structures, with and without modeling for package inductance. The noise source, located 1000 µm away from the receiver, is an inverter core connected to Vcc and ideal ground. The first receiver has a guard ring around it, while the second receiver is contained inside a triple well. If Vdd and Vss of the receiver are connected to ideal ground, the triple well provides approximately 13 dB more isolation than the guard ring. However, if 500 pH of inductance is added to Vdd and Vss, the additional isolation due to the triple well varies from 10 dB to no difference. The top line in the figure uses the supply connected to the noise source to bias the nwell portion of the triple well. In this case the Vcc connection shorts noise between the two regions and degrades the isolation. This example highlights the complexity of the designers challenge to optimize isolation. The correct solution for one technology and design may not be the right choice for different design constraints. Recent work indicates that interconnect coupling may also reduce the achievable triple-well isolation, but little has been published to this date.

Grounding Effects

It is common practice among analog designers to have separate supplies for analog and digital sections of the chip to isolate the analog circuitry from the switching noise introduced on the digital supplies. The same technique is useful to isolate different RF blocks. Dividing a chip into sections with different substrate grounds will attenuate noise coupling from area of a chip to another. Cathelin of STMicroelectronics showed an example of this at DATE'02 [6]. The surface noise distributions in Figure 5 were generated using SubstrateStorm and

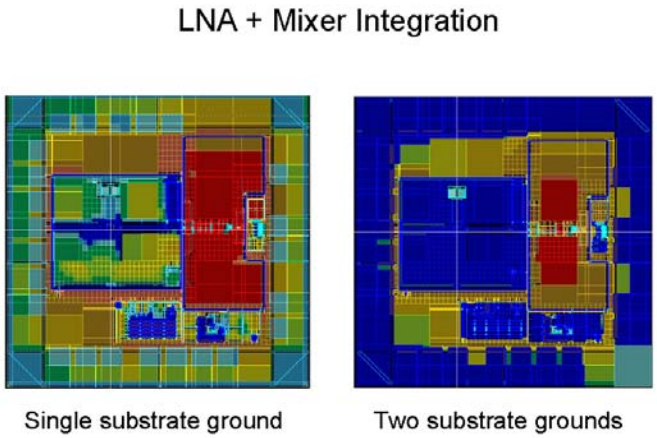

Figure 5: STMicroelectronics DATE'02 example of grounding strategy. Separating the LNA and mixer grounds increased isolation.

represent the same design with two different grounding schemes. The first layout of the LNA+mixer circuit used one substrate ground for the chip. By adding a second substrate ground so that the LNA (low noise amplifier) and mixer were on separate supplies, additional isolation was obtained and less noise coupled from the mixer to the LNA. For a black and white printout, the dark regions in the layout on the right in Figure 5 represent regions with the most isolation as compared to the lighter regions in both layouts. In the color version red is noisy, representing the noise injection location or no isolation, and blue is quiet, representing the maximum isolation achieved. The same isolation levels or color mapping has been used for both layouts.

Although a seal ring is not typically grounded and is therefore not a grounding effect, it can decrease the isolation achieved by separating supplies. In some fabrication processes, a metallized ring contacting the substrate is placed around the outside of the chip to seal the edge from alkali ions that may enter the field oxide and affect the yield.

This ring may act as a low impedance path for noise coupling between different regions on the chip. If design guidelines allow the edge seal to be broken, the ring should be severed where it provides a coupling path between different supply regions.

Guard Rings

In a lightly doped substrate, as contrasted with a heavily doped substrate, guard rings typically provide effective isolation. (This is assuming that care has been taken to ensure that the guard ring is connected to a quiet supply.) Guard rings around a sensitive circuit help to decouple noise from the circuit and ensure that noise will couple equally into both sides of a differential design. Guard rings around a noise source provide a low resistance path to AC ground for the noise and help minimize the amount of noise injected into the substrate. The efficiency of guard rings depends on the noise frequency and the package inductance. Figure 6 illustrates the change in isolation as a function of frequency between a noise source and a sensitive node with 0.5 nH, 0.3 nH, and 0.1 nH inductors between a 10 µm wide guard ring and ideal ground. The top line in the graph plots the isolation with no guard ring for comparison. For the inductance values shown, the lines start to diverge above 1 GHz. In this example the inductance value of 0.5 nH actually decreases isolation at 10 GHz because the inductive impedance causes the guard ring to "float" and become a low impedance conductor for noise.

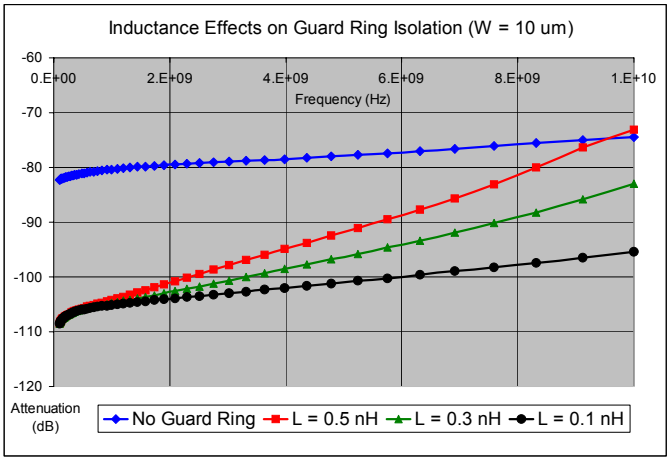

Figure 6: Guard ring isolation as a function of frequency for 0.5, 0.3, and 0.1 nH inductance values versus no guard ring.

Backside connections to the substrate can be viewed, in a very simplistic manner, as a type of guard ring. The effectiveness of the backside connection will depend on the inductance value between the backside and ideal ground, and on the frequency of the noise. Certain packages provide a very low inductance path from the backside of the chip to the board ground. In these cases a conductive connection to the backside of the chip can add considerable isolation. However, if the package is such that a backside connection is grounded through down-bonds to the paddle and significant inductance exists in the package, the backside connection may make matters worse. At higher frequencies the backside connection will then act as a floating conductor to spread noise across the chip.

Guard ring width also affects isolation. van Zeijl of Ericsson presented a single-chip Bluetooth design at ISSCC'02, as shown in Figure 7, that used a 300 µm wide guard band to isolate the radio portion of the chip [7]. In this case the width of the

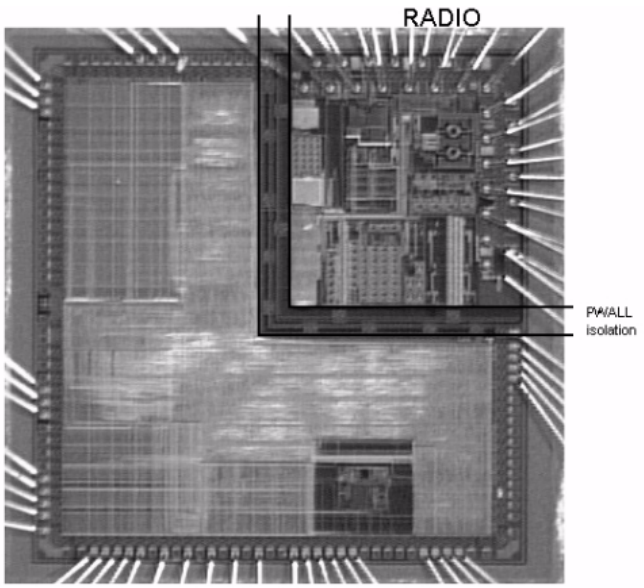

Figure 7: Ericsson single-chip Bluetooth with a 300 µm-wide, guard band isolation.

guard ring is similar to the depth of the substrate, and the package provides a very low impedance to ground. Figure 8 shows simulation results of the attenuation provided by various widths of guard rings. With a 0.3 nH inductor in series with the guard ring, the larger guard rings provide better iso-

lation at lower frequencies but lose their advantage at higher frequencies. The appropriate guard ring width will depend on the frequency of noise to be attenuated, the space available, and the attenuation needed. These simulations were run with the guard rings modeled as ideal conductors.

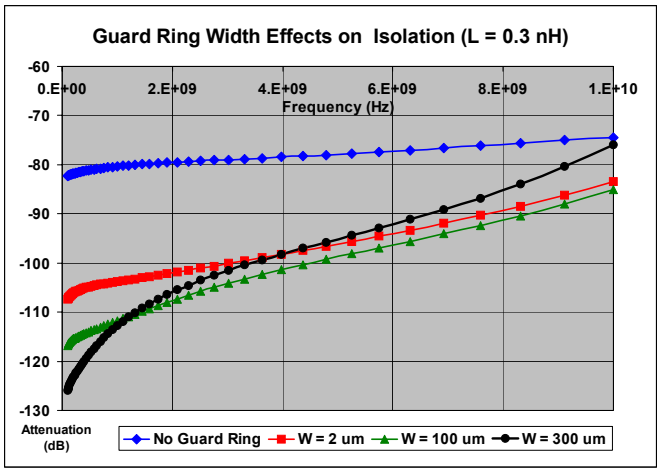

Figure 8: Guard ring isolation versus frequency as a function of width.

Shielding

Proper shielding for sensitive signal lines and passive components is an integral part of effective analog/RF IC layout. The challenge is to determine the appropriate shield layer, bias potential, and layout pattern. Sensitive signal buses are often laid out with alternating signal and shield lines to prevent crosstalk through lateral and fringing electric fields. To isolate the signal lines from the substrate, nwell or diffusion layers can be placed under the lines to prevent noise coupling. In general, shielding increases parasitic capacitance since the field lines from the signal wires terminate at a closer distance on the shielding before they reach another signal line or the substrate. The bias potential of the shield should be tied to the reference of the signals. The effectiveness of shielding also depends on the signal operating frequency. In general, there is a trade-off between a lower shield parasitic capacitance and a higher series resistance. As frequency increases, a large series resistance causes the shield to be ineffective.

Passive components such as inductors and capacitors occupy substantial die area and thus are susceptible to coupling through the substrate. In a p-type substrate, nwell can be placed under capacitors, inductors or bond pads to provide a low-capacitance shield. However, the well resistance, typically on the order of 1 KOhm/sq., may be too large to be effective at high frequencies. To lower shield resistance, a diffusion or polysilicon layer may be used. Inductors are a special case, since the magnetic field will induce eddy current in a conductive shield beneath the inductor. Inserting a pattern of slots in the shield perpendicular to the inductor traces, as shown in Figure 9, will prohibit the eddy current by creating a “patterned ground shield” [8].

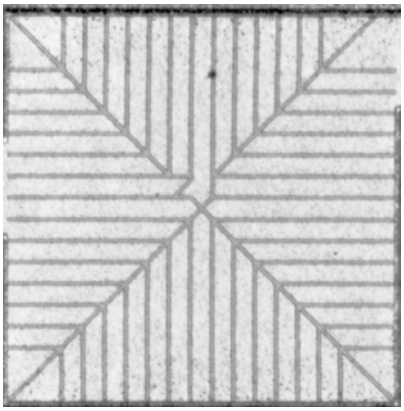

Figure 9: Close-up photo of the patterned ground shield.

The effectiveness of a patterned ground shield to provide isolation was measured in terms of crosstalk between two inductors using the test structure shown in Figure 10. Each of the inductors are surrounded with ground paths that act as guard rings. Therefore, the inductors are electrically isolated except that they reside on the same substrate. Substrate coupling between two adjacent inductors was measured by the transmission coefficient, S_{21}. The S-parameters were measured using a network analyzer and Cascade coplanar ground-signal-ground probes. Figure 11 shows that the more conductive substrate results in stronger coupling due to its higher admittance. The peaks in $|S_{21}|$ for the no ground shield (NGS) cases correspond to the onset of significant penetration of the electric field into the silicon. This also implies that coupling is dominated by parasitic capacitance to the substrate, and that the magnetic coupling is weak. If magnetic coupling was the dominant coupling mechanism,

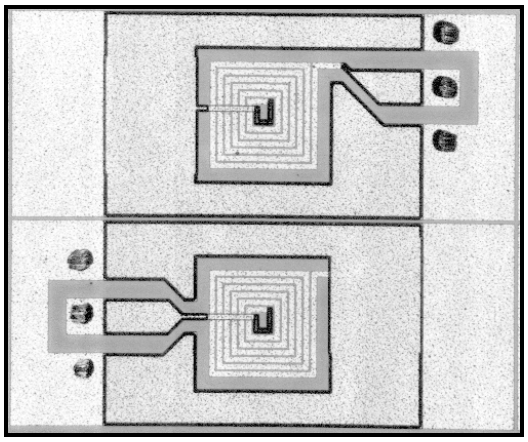

Figure 10: Two-port test structure to measure substrate coupling between adjacent inductors. Each inductor has one end grounded. The ground rings surrounding the inductors are not connected.

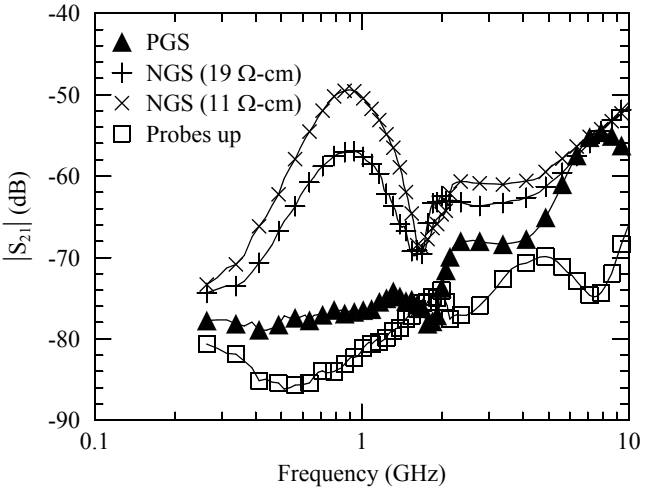

Figure 11: Effect of polysilicon patterned ground shield (PGS) on substrate coupling between two adjacent inductors. NGS denotes no ground shield placed under the inductors. The "Probes up" data represents the intrinsic noise floor of the testing setup.

increasing the resistance of the substrate would not change the isolation between the inductors. In contrast to no shielding, the inductors with polysilicon patterned ground shields show improved isolation up to 25 dB at GHz frequencies. Figure 12 shows a 5 GHz, 0.25 μm CMOS transceiver incorporating more than 40 on-chip inductors [9]. The patterned ground shields are placed beneath each inductor to suppress noise coupling through the substrate.

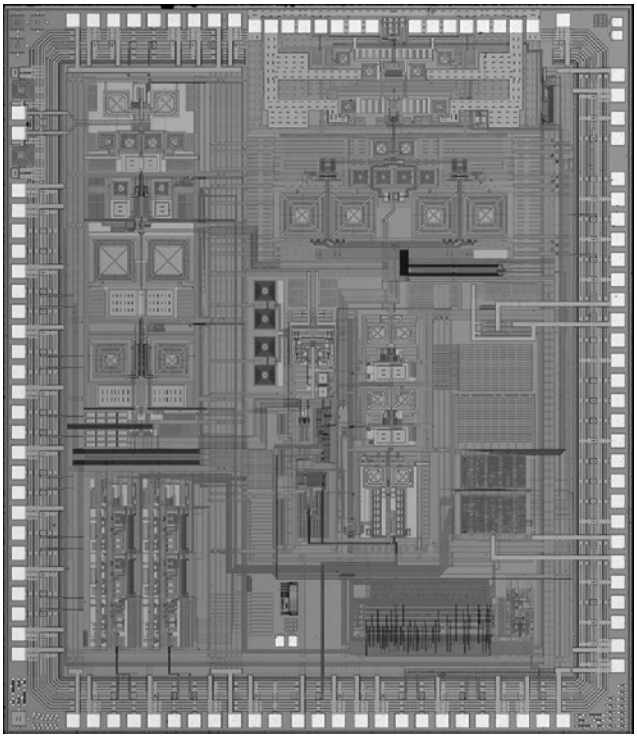

Figure 12: 5 GHz, 0.25 μm CMOS transceiver incorporating more than 40 on-chip inductors. Patterned ground shields are placed beneath each inductor to suppress noise coupling through the substrate.

On-chip Decoupling

Decoupling capacitance is not always thought of as something that increases the isolation between two points, but it serves the same role. Isolation is desirable to attenuate noise coupling from one portion of a chip to another. If decoupling capacitance can reduce the amount of noise created by supplying local charge for nearby switching and thus lowering the peak current drawn across the package inductance, careful use of it essentially isolates a sensitive circuit that no longer sees the same supply and substrate noise levels. An excellent example of this was presented by Connell of Motorola at ISSCC'02 [10] as illustrated in Figure 13. A broadband tuner was implemented with a digital synthesizer that generated large switching currents. An initial simulation with a 100 pF bypass capacitor showed 82 mV of substrate noise created by the switching. Increasing the bypass capacitor to 1400 pF reduced the noise to 9 mV. Adding an on-chip voltage regulator with 5 pF of input capaci-

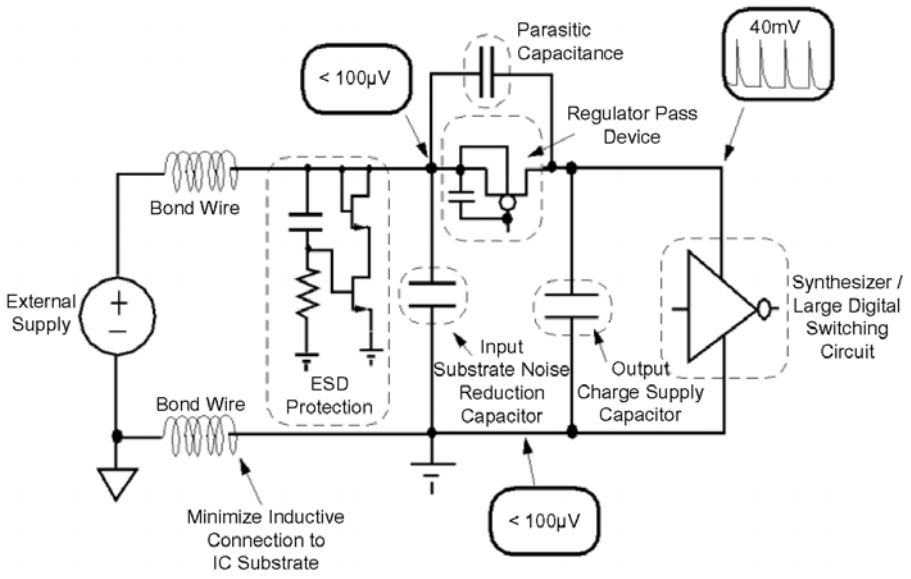

Figure 13: Motorola ISSCC'02 use of decoupling capacitance to decrease noise.

tance and 1100 pF of output capacitance decreased the noise to 1.5 mV. The fabricated design used 300 pF of decoupling capacitance at the input of the voltage regulator and 1100 pF of decoupling capacitance at the output of the voltage regulator to achieve a substrate noise level of 98 µV. Care was taken to minimize the inductive connection to the substrate to reduce the amount of supply noise.

Summary

Meeting the specifications of the next generation RF products requires an experienced designer who understands a variety of isolation techniques. This paper has detailed several commonly used isolation techniques while trying to emphasize their interdependent nature. Process technology options, grounding strategies, guard rings, shielding, decoupling capacitance, and package parasitics all play an important role in isolation. However, it is the combination of them that ultimately determines whether the final design will meet the product specifications.

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