High-Precision Low-Voltage Low-Power Analog-to-Digital Conversion

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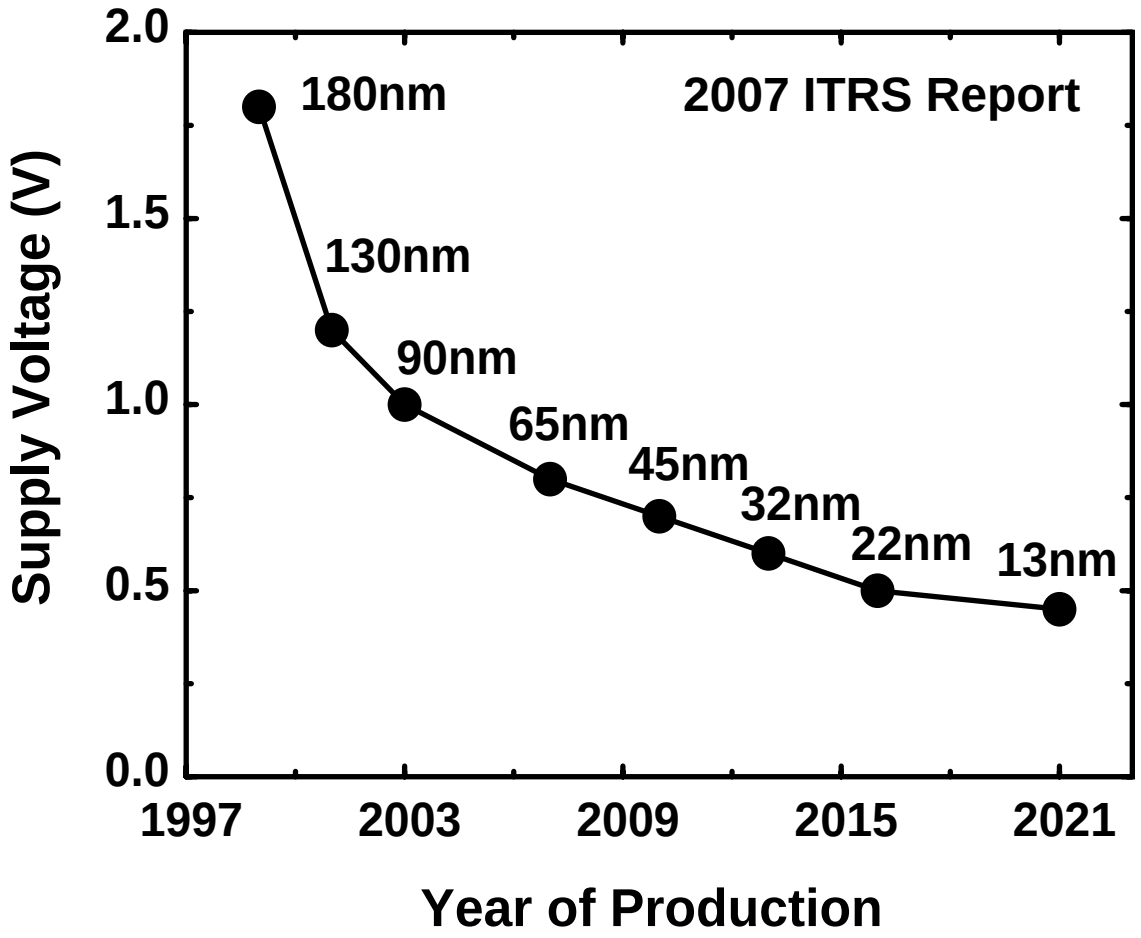
Outline

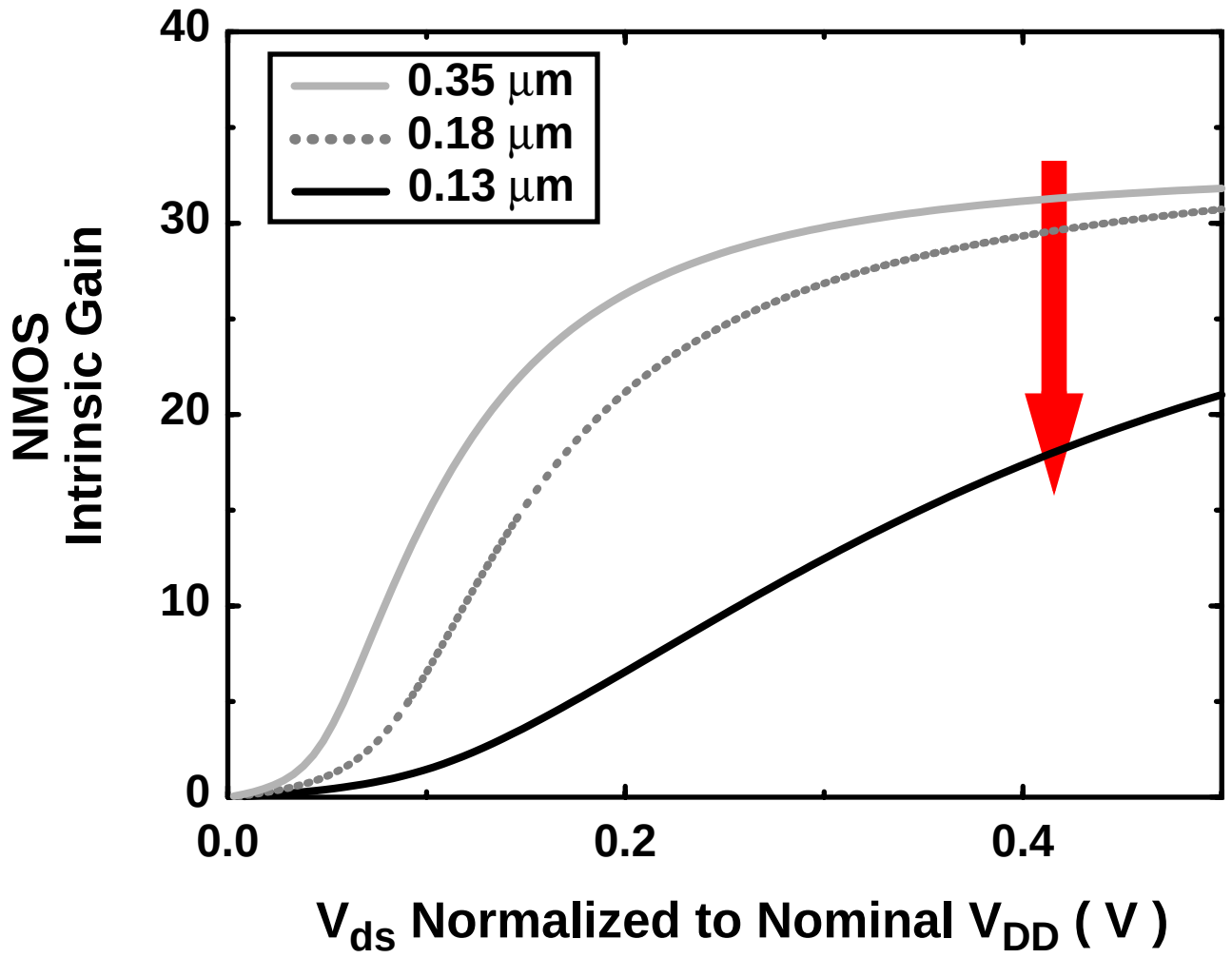
- **Introduction**
- **Proposed ADC architecture**
- **Implementation**
- **Experimental results**
- **Conclusion**

Toward Lower Supply Voltage



- **Reduced voltage headroom: limited circuit topologies**
- **Reduced dynamic range: higher power for the same DR**

Reduced Device Intrinsic Gain



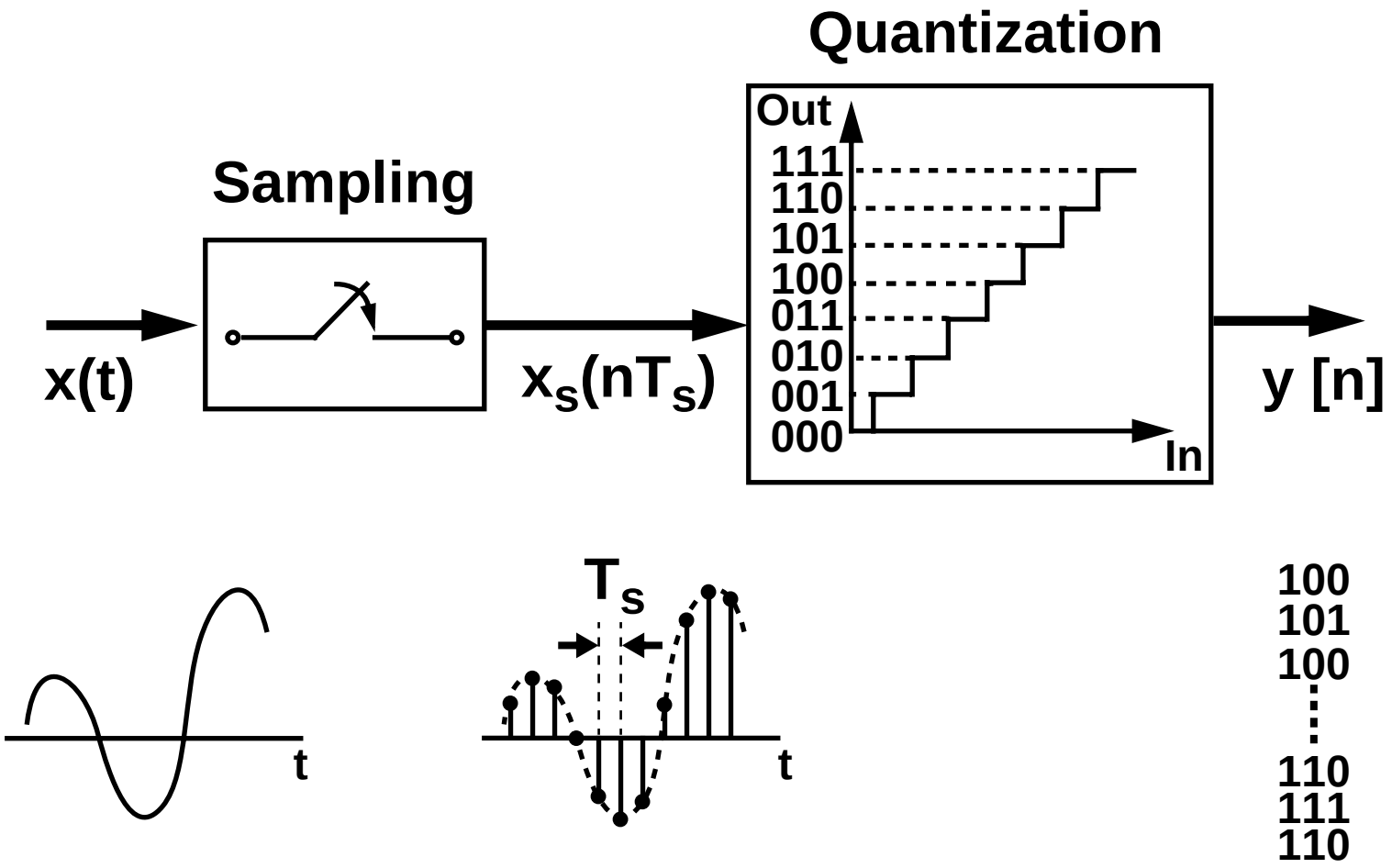
- **Difficult to build precision analog blocks**
- **System robustness becomes important**

Research Objectives

- **Goal: Explore novel architectures and circuits for realizing high-precision, low-voltage, low-power CMOS ADCs**
- **Target application: Portable digital audio devices, sensor, instrumentation**
- **Target performance**

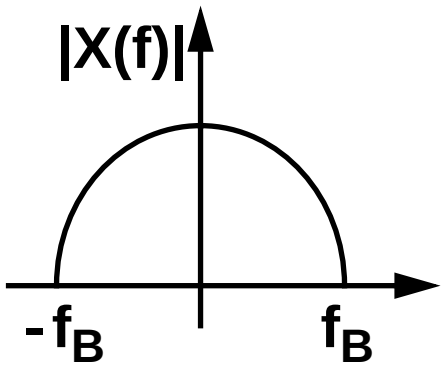
Supply Voltage	**0.7 V**
Technology	**CMOS 0.18-μm**
Dynamic Range	**> 95 dB**
Signal Bandwidth	**25 kHz**
Power Dissipation	**Minimize**

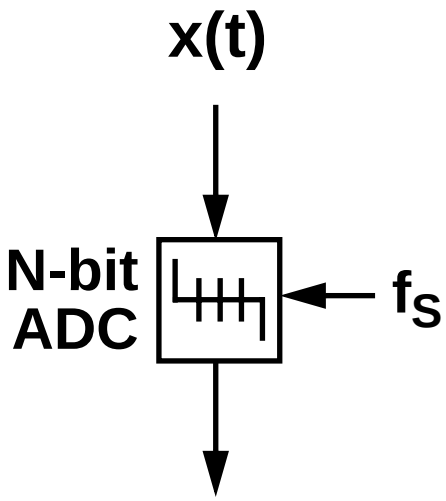
Analog-to-Digital Conversion



- **Sampling in time**
- **Quantization in amplitude**

Nyquist-Rate ADC vs. Oversampling ADC

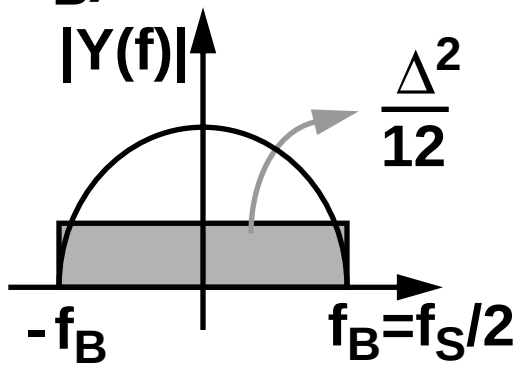




$y[n] = x[n] + e_q[n]$

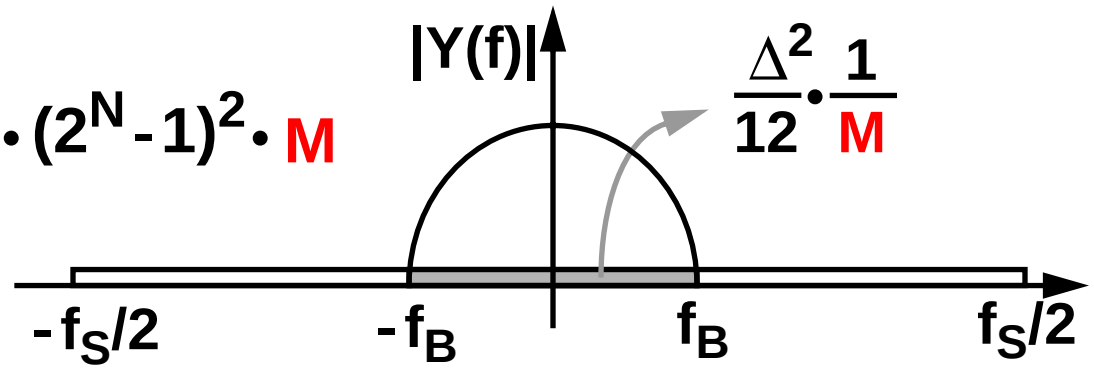
Nyquist-rate ($f_S = 2 \cdot f_B$)

$$DR = \frac{3}{2} \cdot (2^N - 1)^2$$

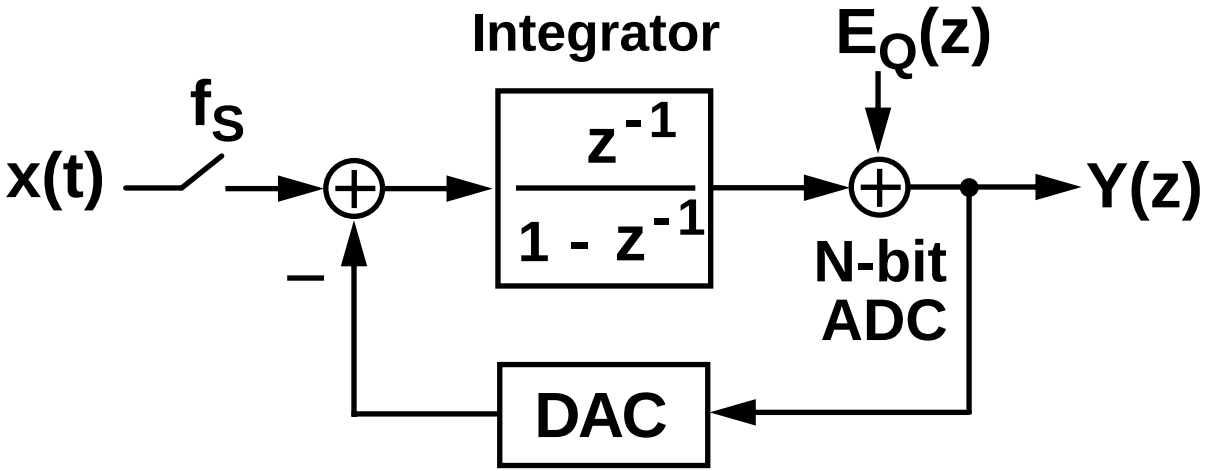


Oversampling ($f_S = 2 \cdot f_B \cdot M$)

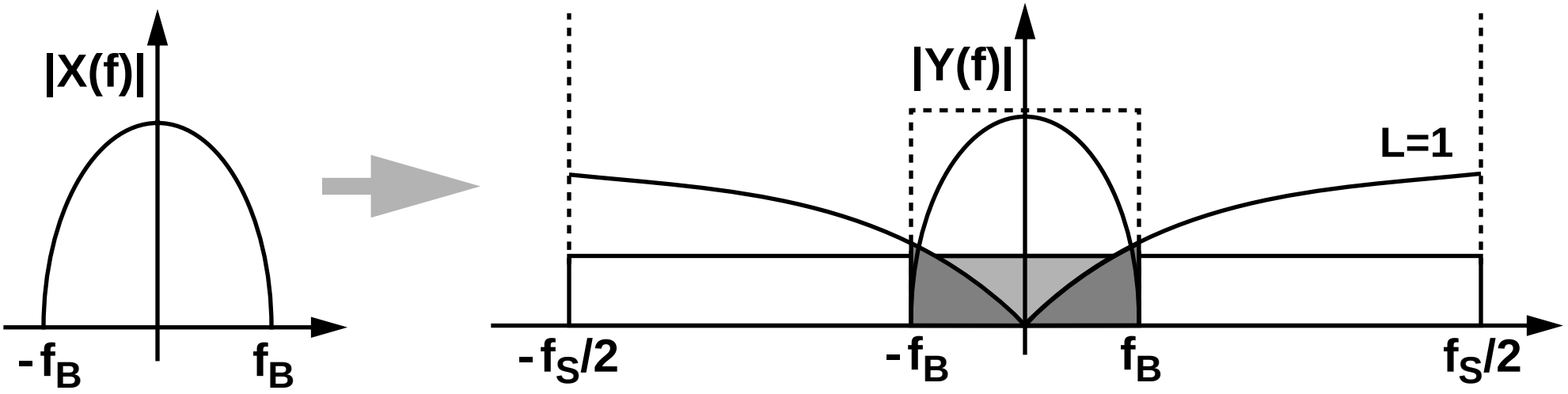
$$DR = \frac{3}{2} \cdot (2^N - 1)^2 \cdot M$$



ΣΔ Oversampling ADC

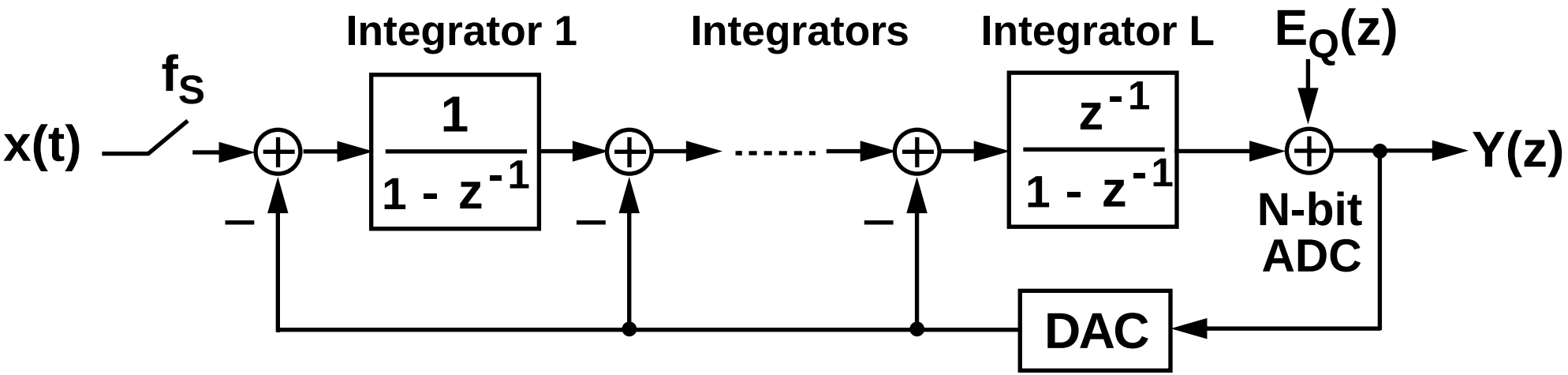


$$Y = z^{-1} \cdot X + (1 - z^{-1}) \cdot E_Q$$



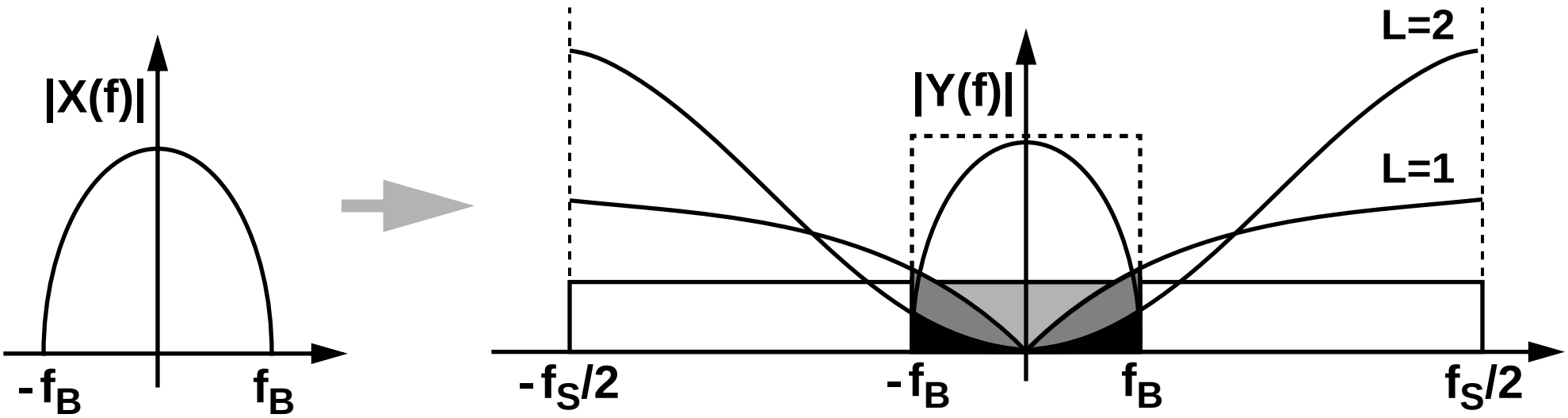
- **Filtering and feedback → Noise shaping**

ΣΔ Oversampling ADC: Higher Order



$$Y = z^{-1} \cdot X + (1 - z^{-1})^L \cdot E_Q$$

$$DR \sim \frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1} \cdot (2^N - 1)^2$$

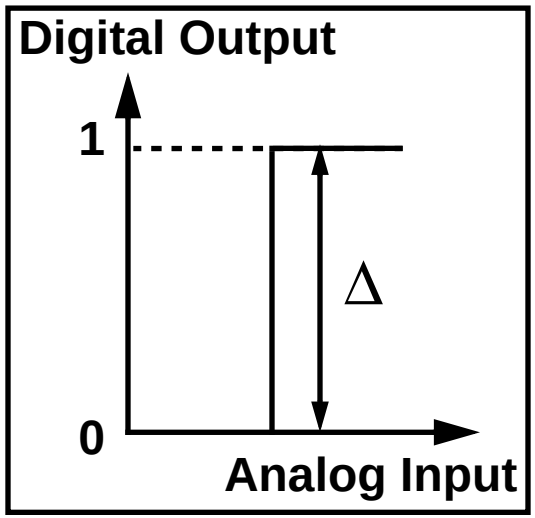


Quantization

- **Single-bit quantization**

  (+) Inherent DAC linearity
  (+) Relaxed comparator design constraints
  (power, loading, offset, complexity, ...)

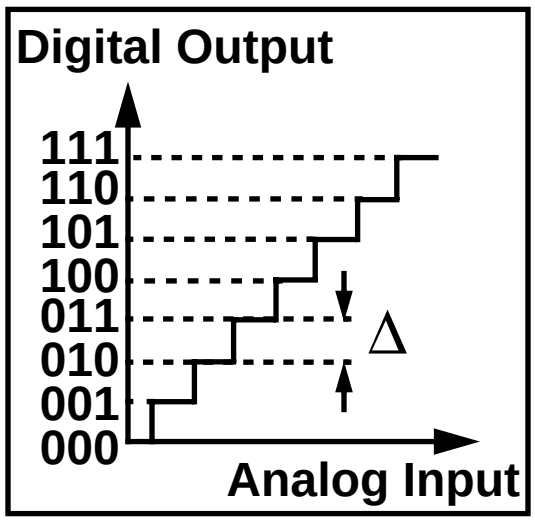
  (-) Increased integrator swings



- **Multi-bit quantization**

  (+) Reduced integrator swings
  (+) Higher performance
  without order or OSR increase

  (-) Feedback DAC linearity issues
  (-) Higher performance comparator needed



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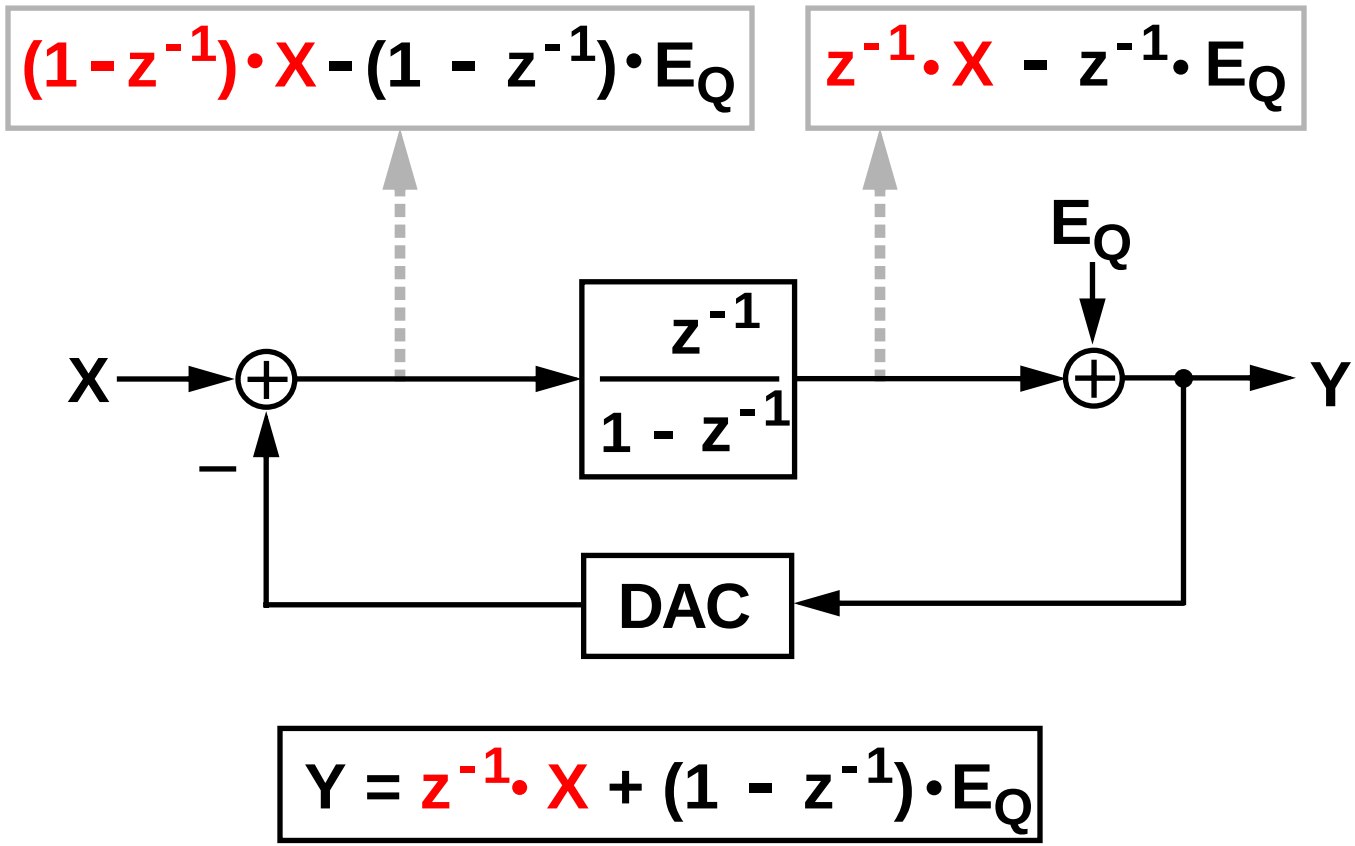
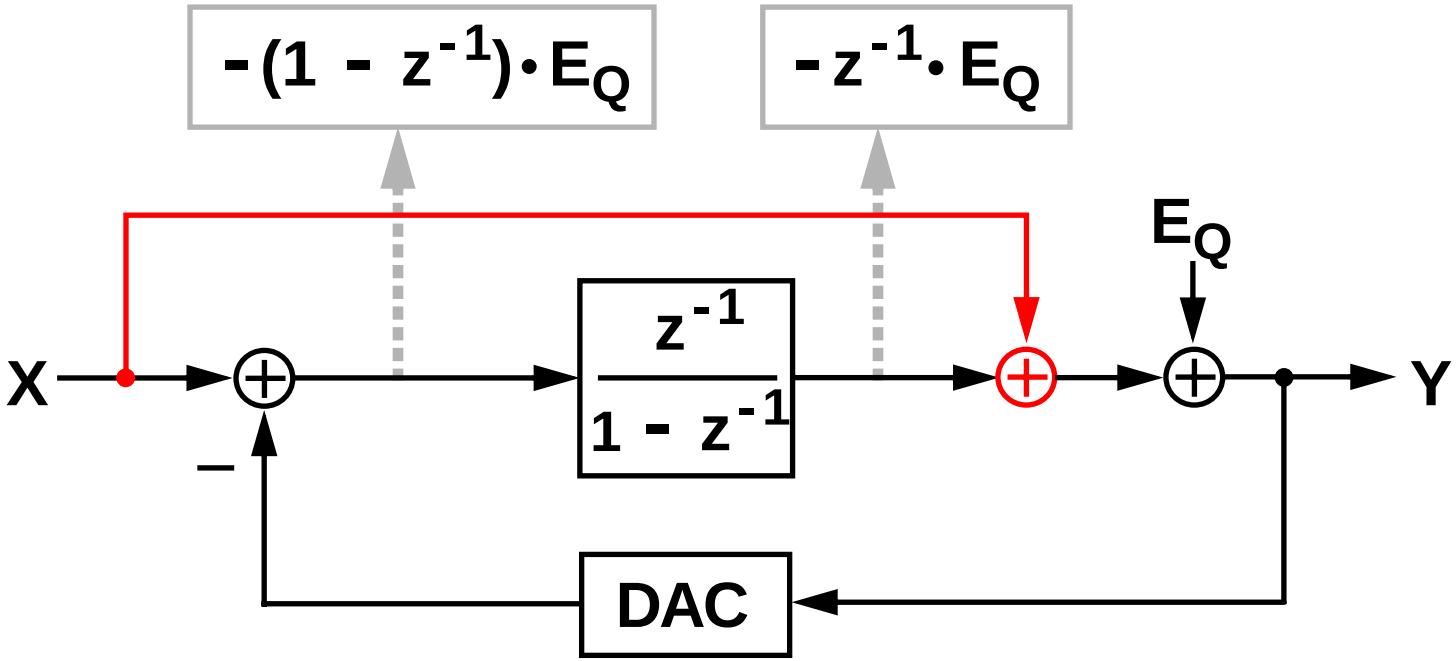
Conventional ΣΔ Modulator



- Integrator swings depend on input
- Large input → nonlinear operation of integrator op amp

Input Feedforward ΣΔ Modulator*

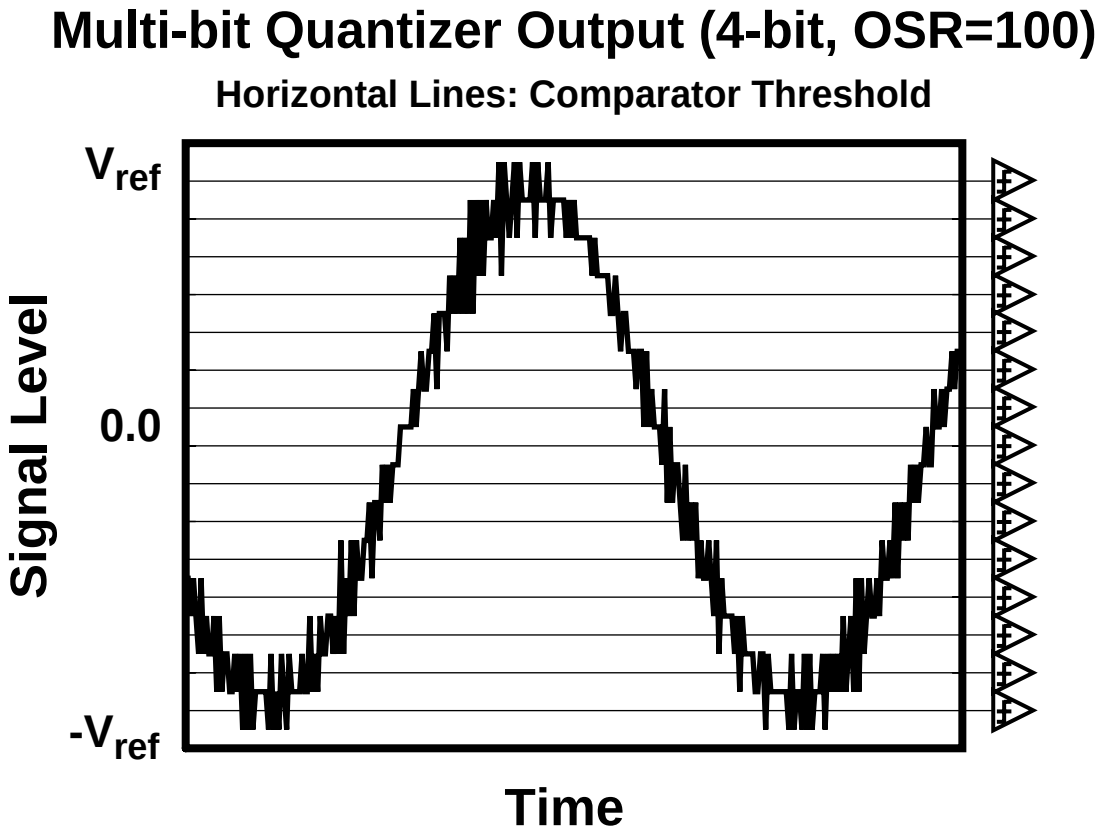


$$Y = X + (1 - z^{-1}) \cdot E_Q$$

- Input independent integrator swings
- Analog summation and timing overhead issues

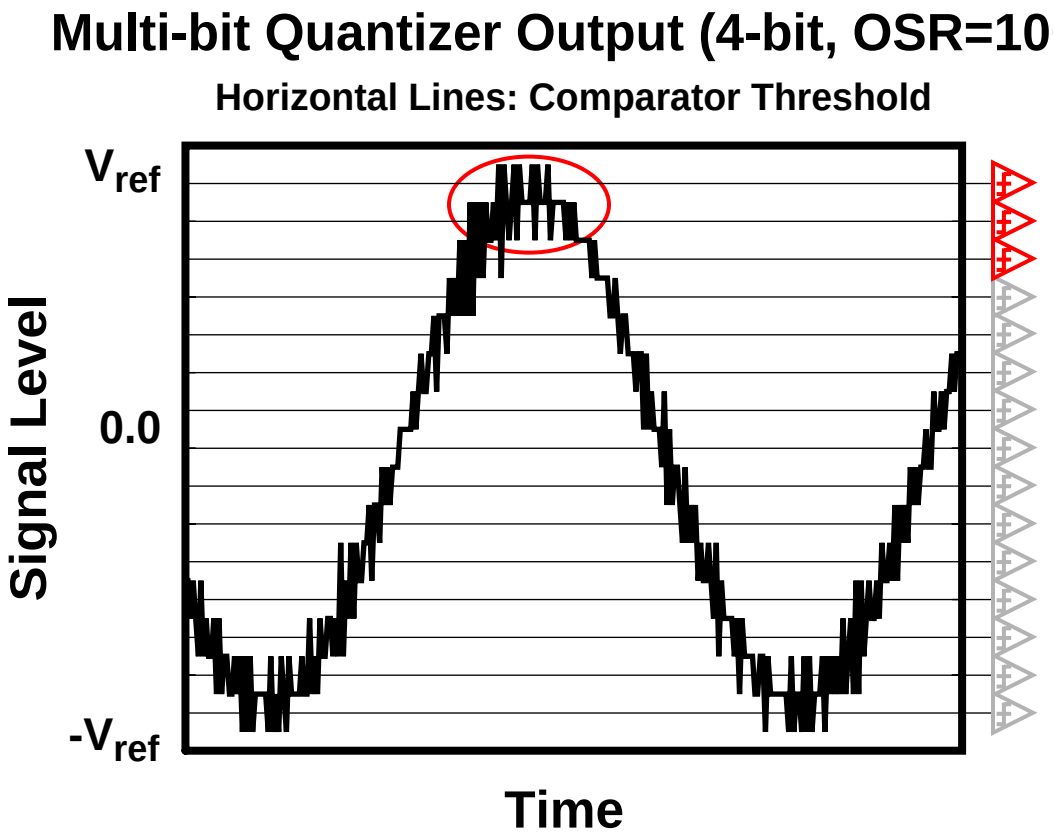
* K. Nam, et al., CICC 2004

Oversampling ADC with Multi-bit Quantization



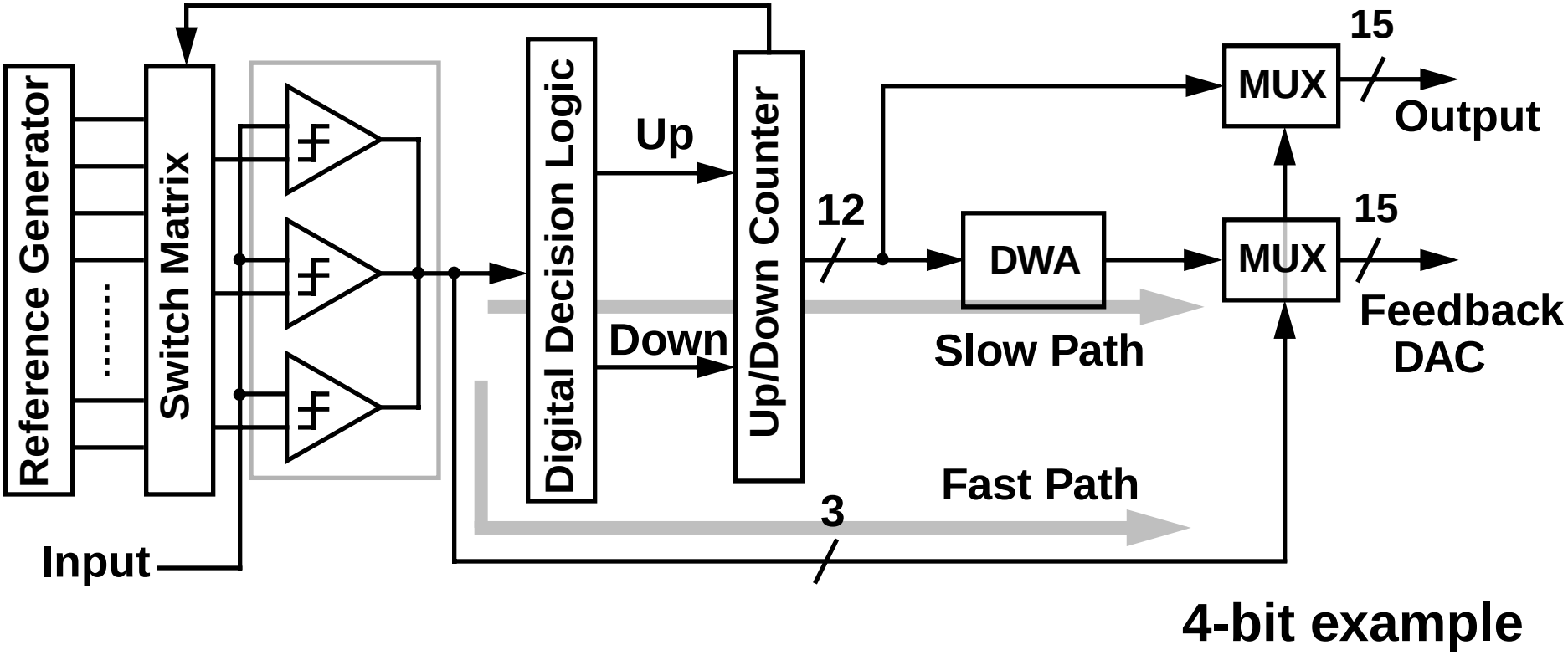
- Reduced integrator swings
- Higher power dissipation

Multi-bit Quantization: Idling Comparators



- **Comparator redundancy**

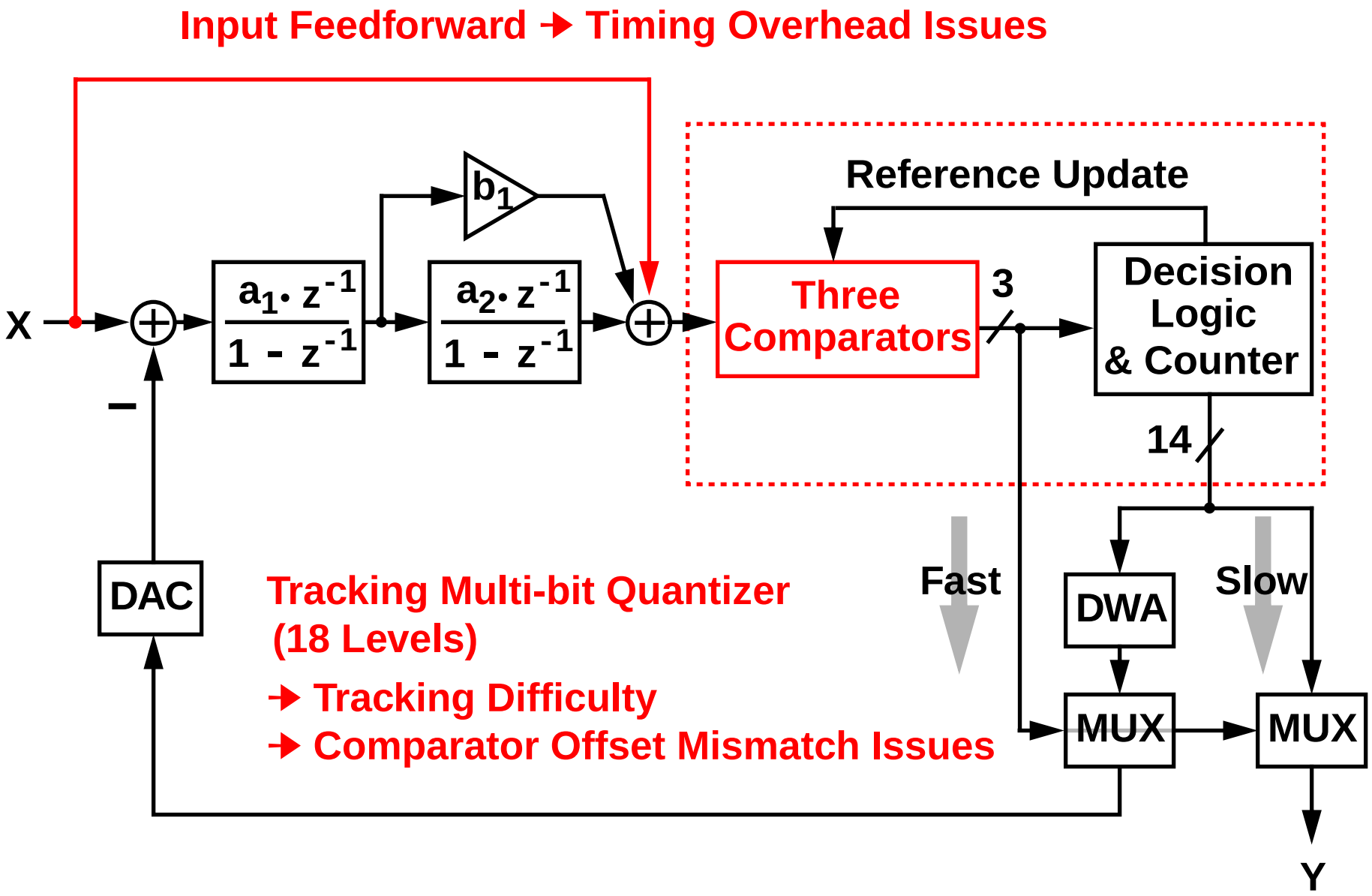
Tracking Multi-bit Quantizer*



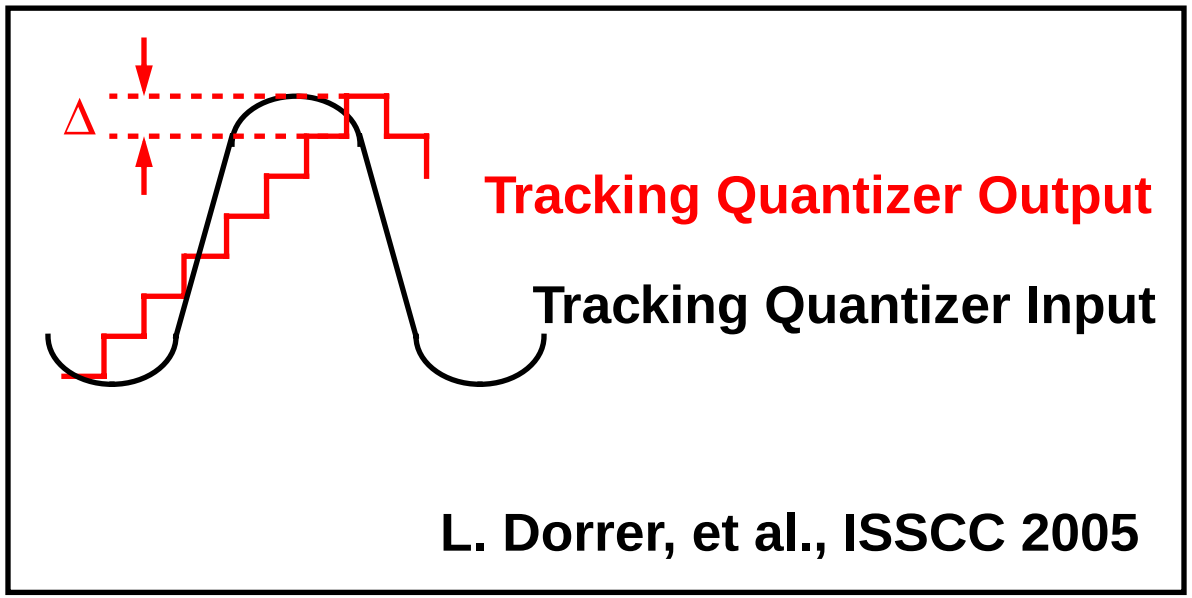
- Multi-bit quantizer with a few comparators
- Tracking difficulty
- Comparator offset mismatch problem

* L. Dorrer, et al., ISSCC 2005

Low-Voltage Low-Power Architecture



Tracking Difficulty (1 of 2)



$$V_{ref} \cdot 2\pi \cdot f_{BWmax} < \frac{\Delta}{T_{clk}}$$

$$\left(\Delta = \frac{V_{FS}}{2^N} = \frac{V_{ref}}{2^{N-1}} \right)$$

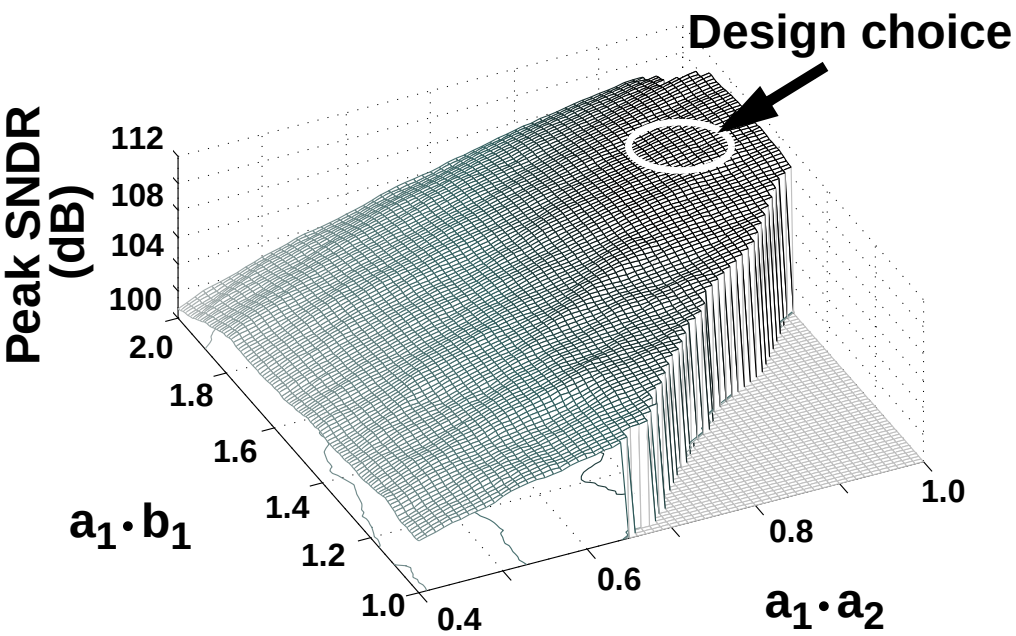
$$OSR > \pi \cdot 2^{N-1}$$

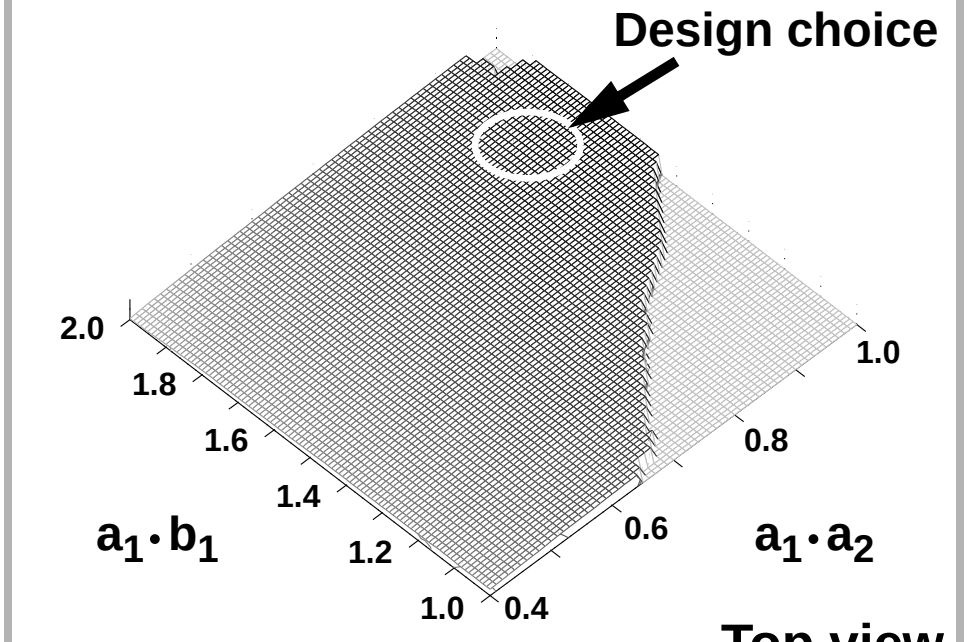
$$\left(OSR = \frac{1}{2 \cdot f_{BWmax} \cdot T_{clk}} \right)$$

- OSR and number of bits trade-off
  - 4-bit quantization requires minimum OSR of 26
- Quantization error degrades tracking operation

Tracking Difficulty (2 of 2)

Modulator coefficient vs. peak SNDR



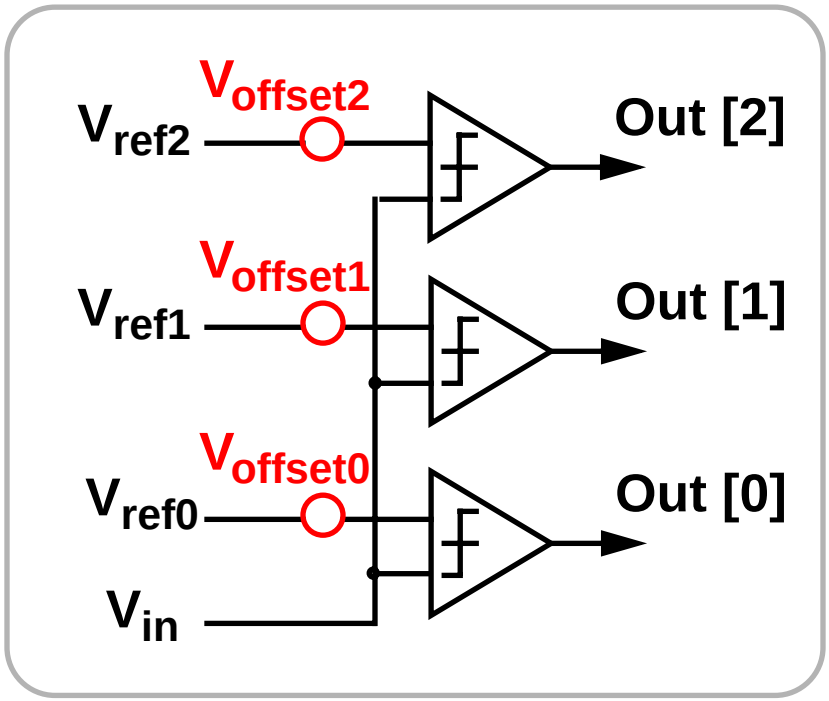


a_1: 1st integrator gain
a_2: 2nd integrator gain
b_1: 1st integrator output feedforward gain

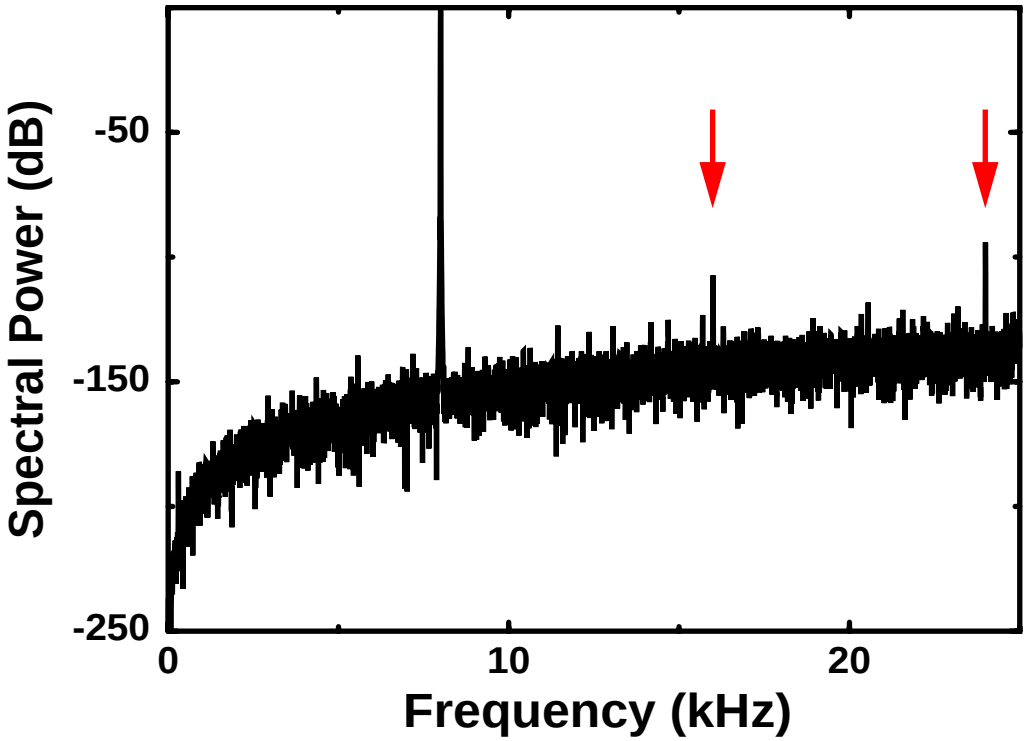
(-1 dB, 24.5 kHz input sinusoid)

- **Integrator gain scaling helps tracking operation**

Comparator Offset Mismatch



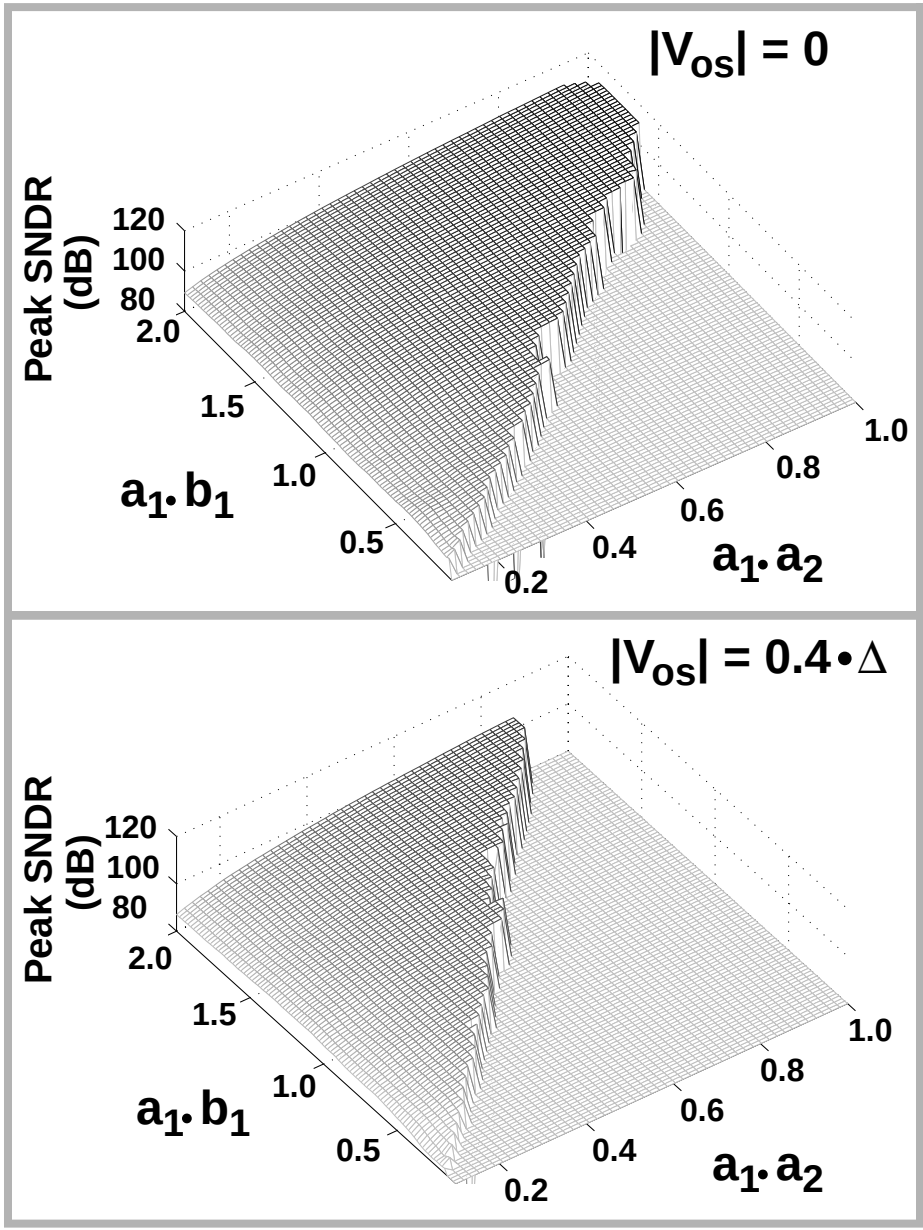
Modulator Baseband Output Spectrum*

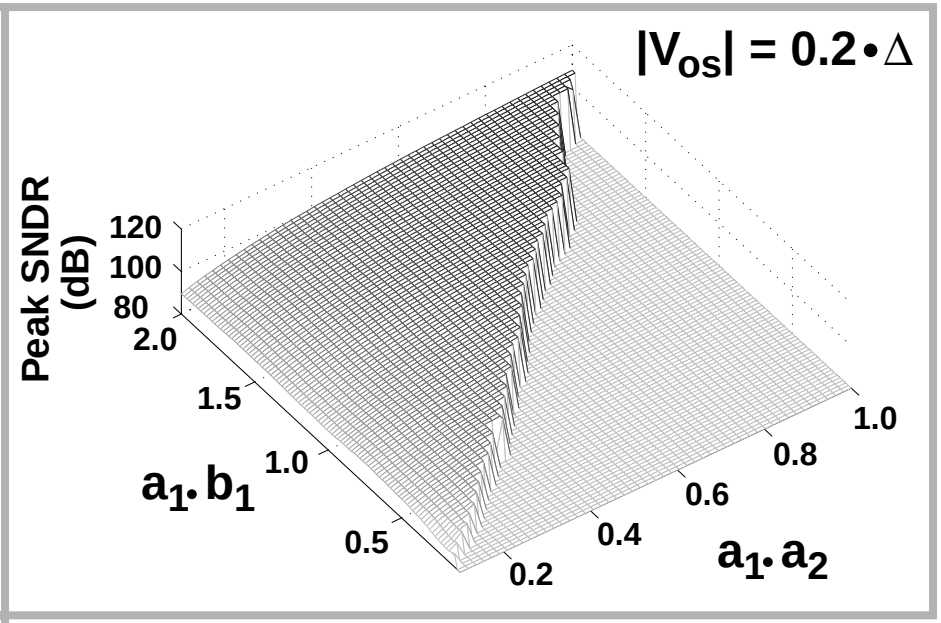


*| 0.4•Δ | offset mismatch

- Offset mismatch increases harmonics and noise floor
- Degraded tracking operation

Comparator Offset Mismatch: Tracking





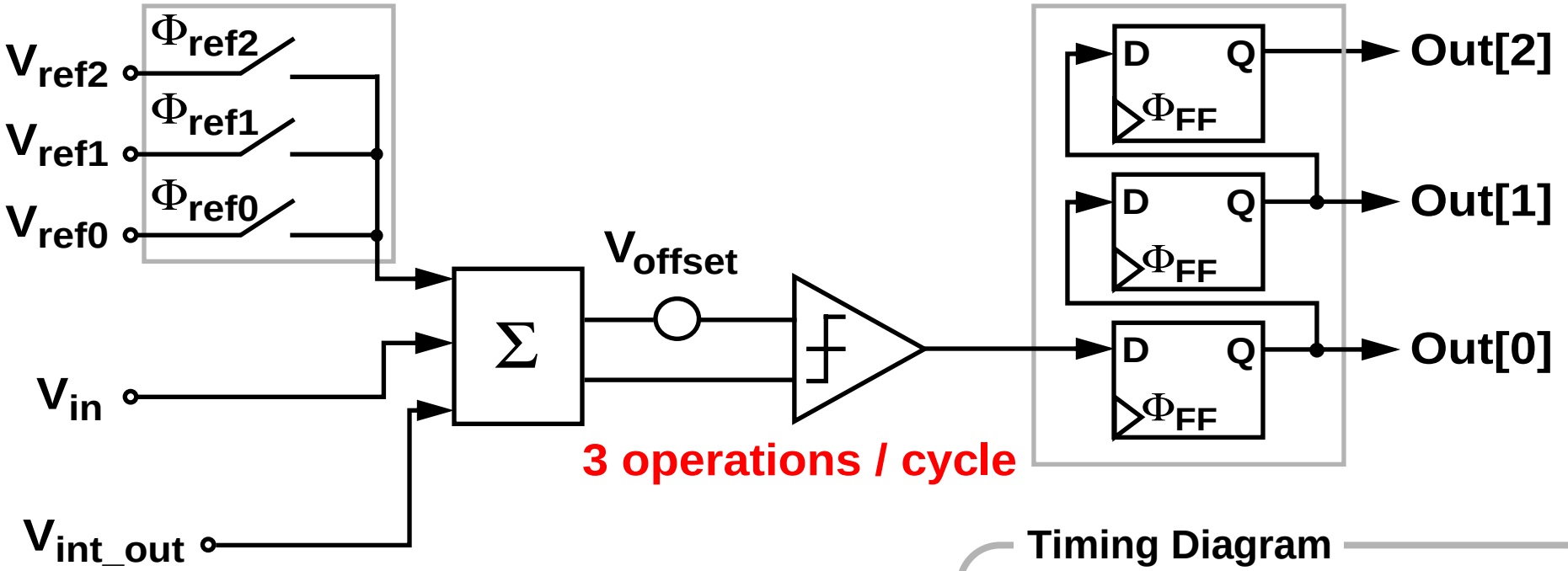
(-1 dB, 24.5 kHz input sinusoid)

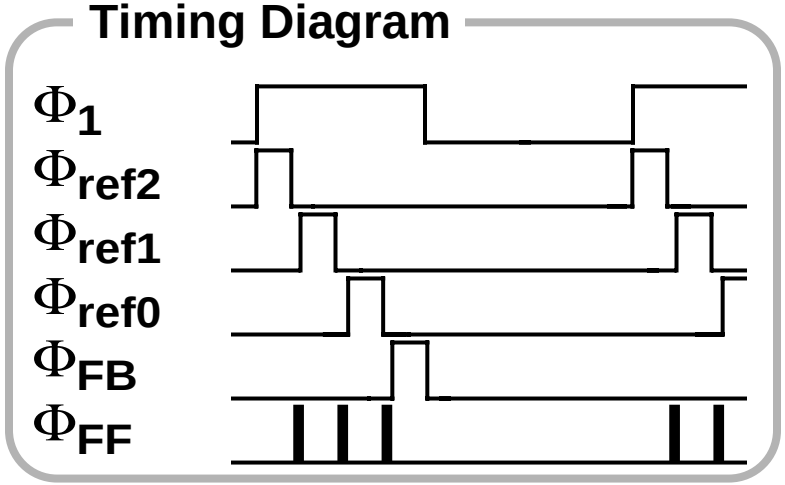
a_1: 1st integrator gain

a_2: 2nd integrator gain

b_1: 1st integrator output feedforward gain

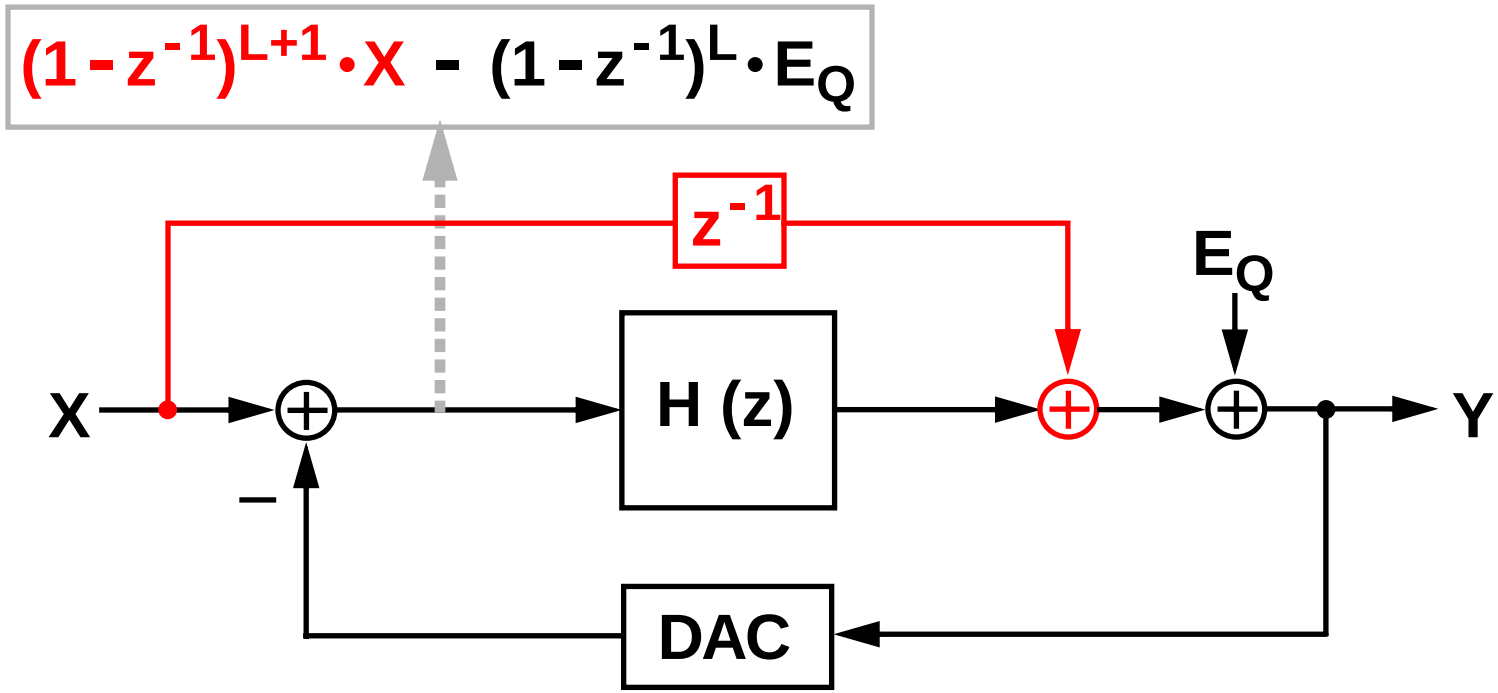
Single Comparator Tracking Multi-bit Quantizer





- **Timing overhead worse with input feedforward**

Delayed Input Feedforward

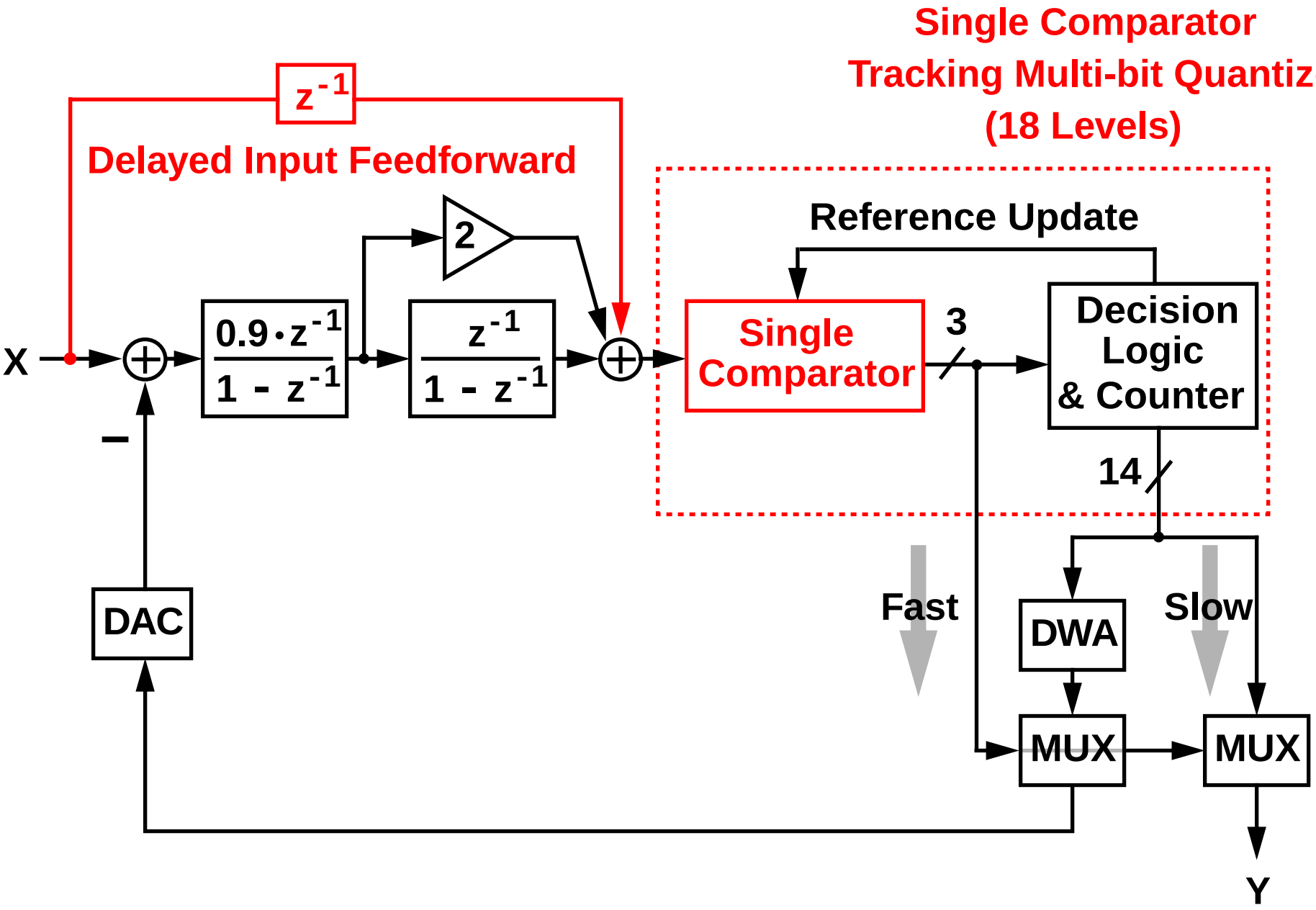


$$Y = \frac{z^{-1} + H(z)}{1 + H(z)} \cdot X + \frac{1}{1 + H(z)} \cdot E_Q$$

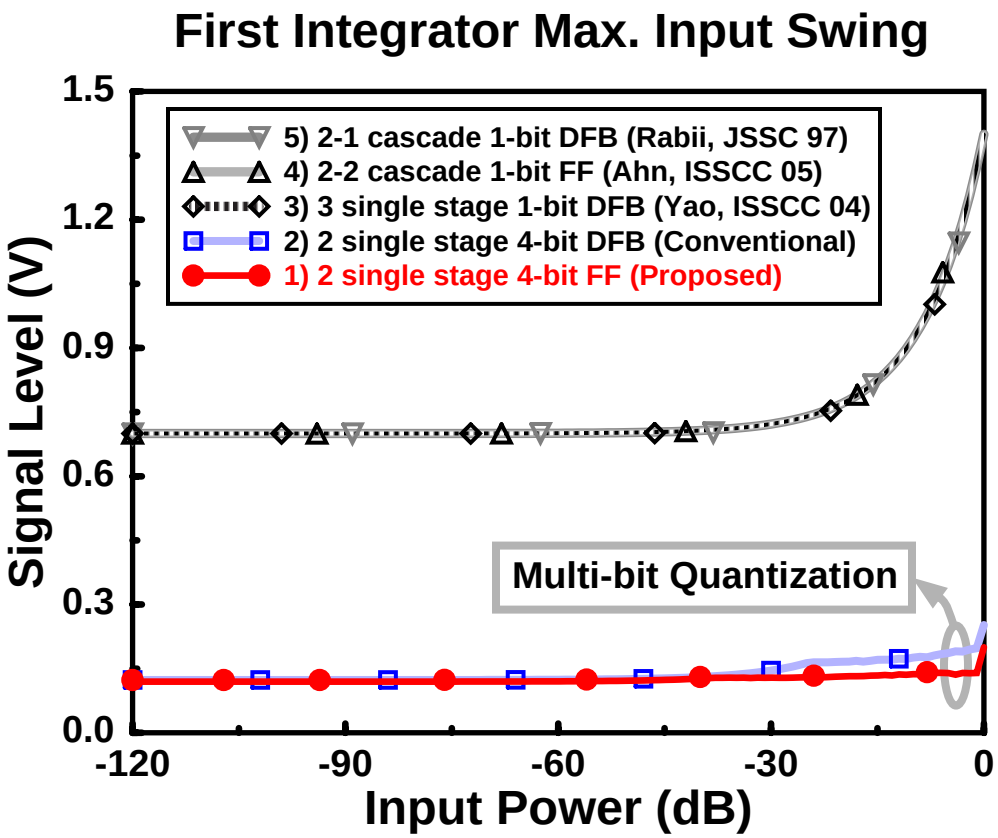
$$\text{if } \frac{1}{1 + H(z)} = (1 - z^{-1})^{L}$$

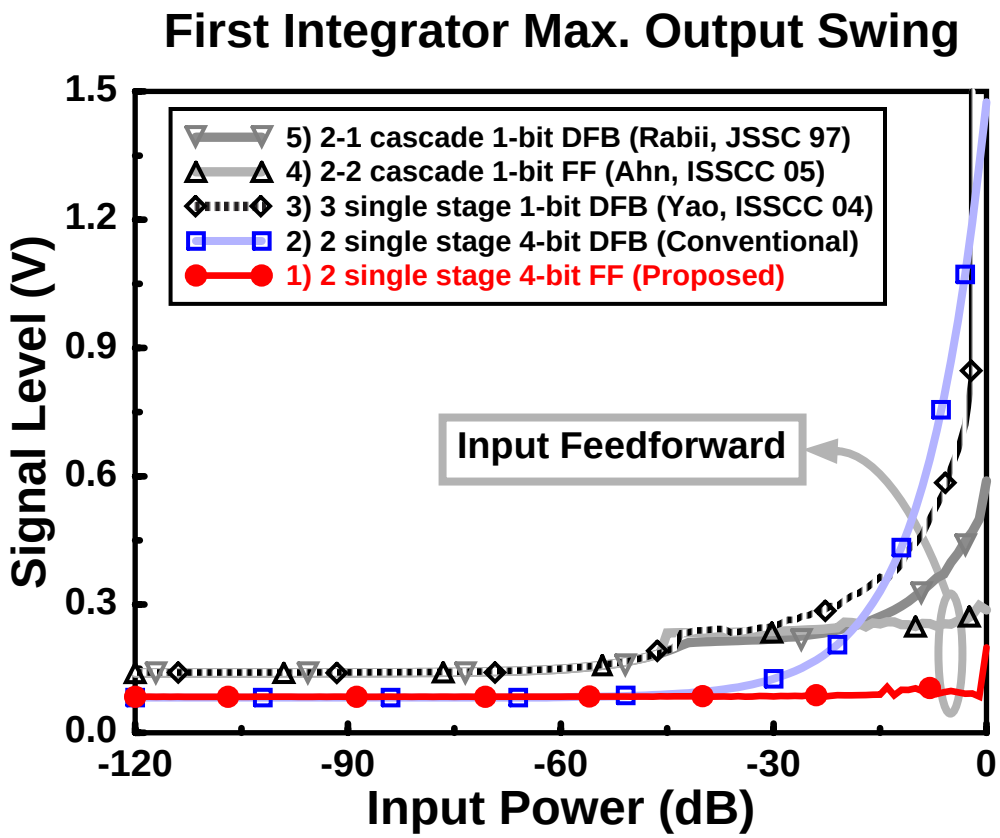
$$Y = (1 - (1 - z^{-1})^{L+1}) \cdot X + (1 - z^{-1})^{L} \cdot E_Q$$

Proposed ΣΔ Modulator Architecture



Integrator Swing Comparison*

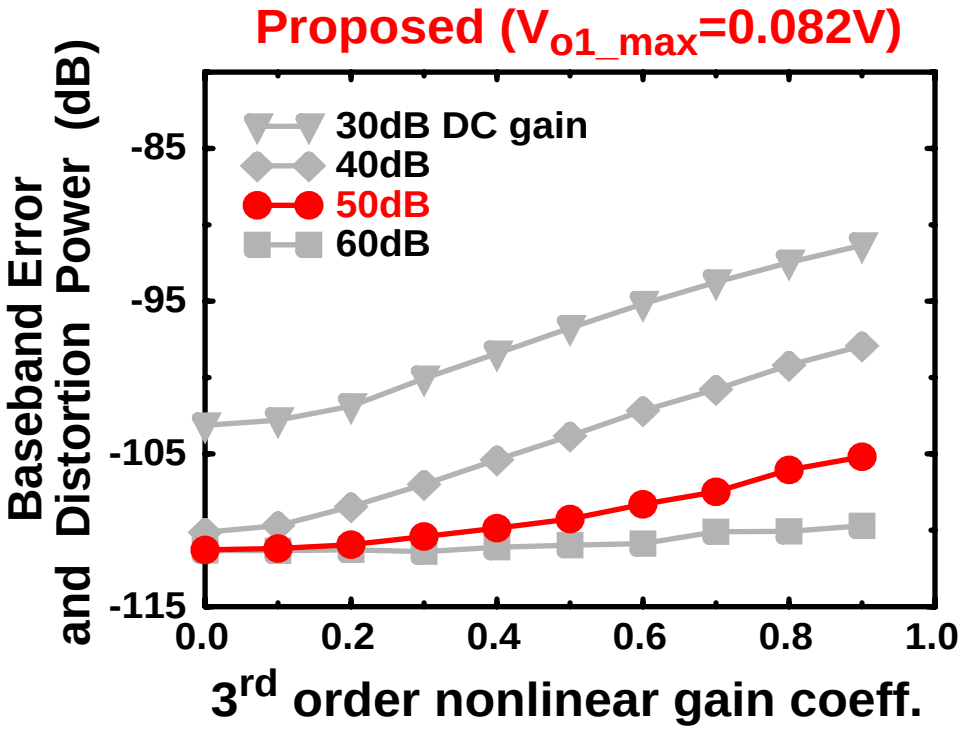


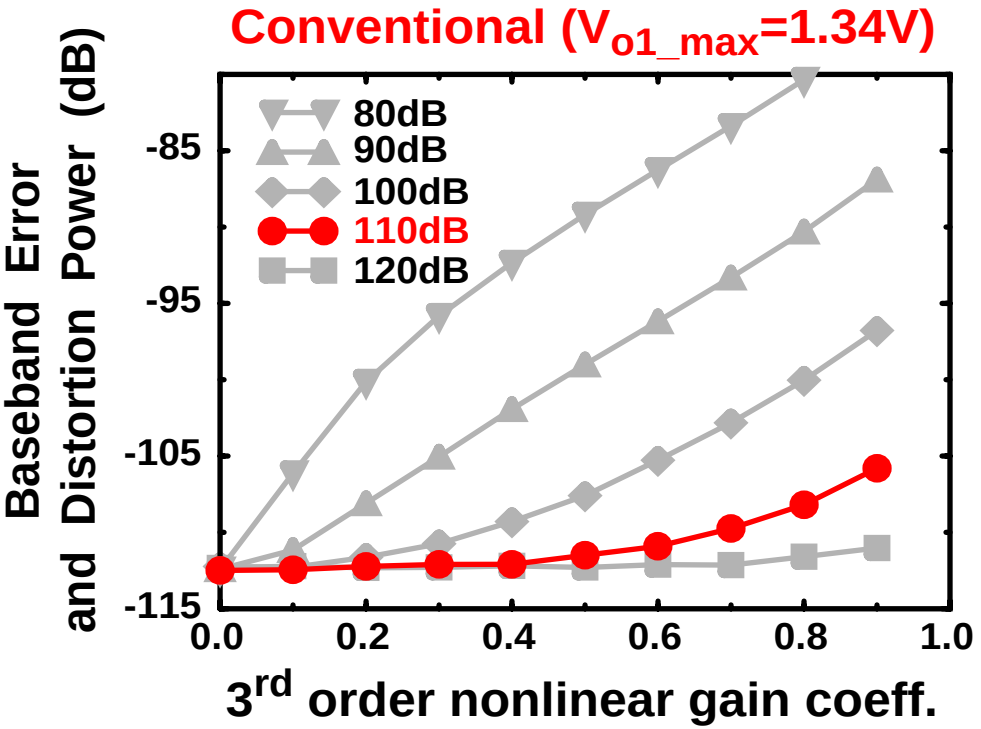


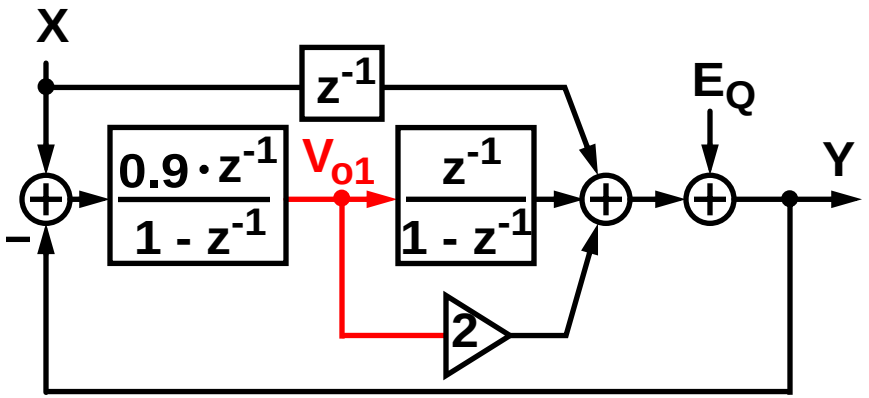
- **FF (Feedforward), DFB (Distributed Feedback)**
- **Multi-bit quantization → input swing reduction**
- **Input feedforward → output swing reduction**

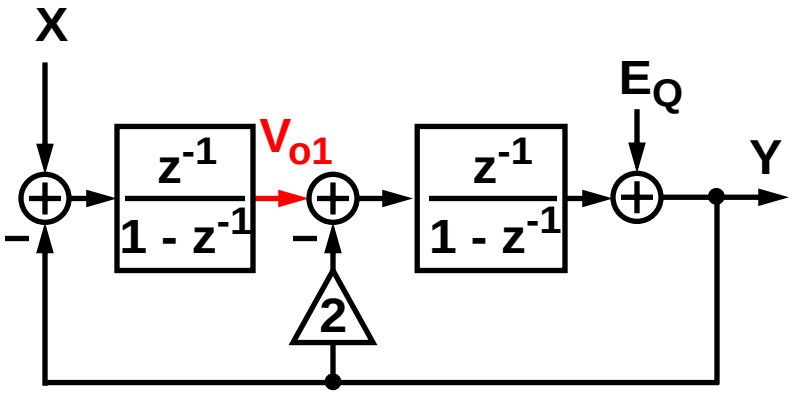
*** 24.5 kHz input sinusoid, OSR=100, V_{ref}=0.7V**

System Robustness: Amplifier Gain Nonlinearity *







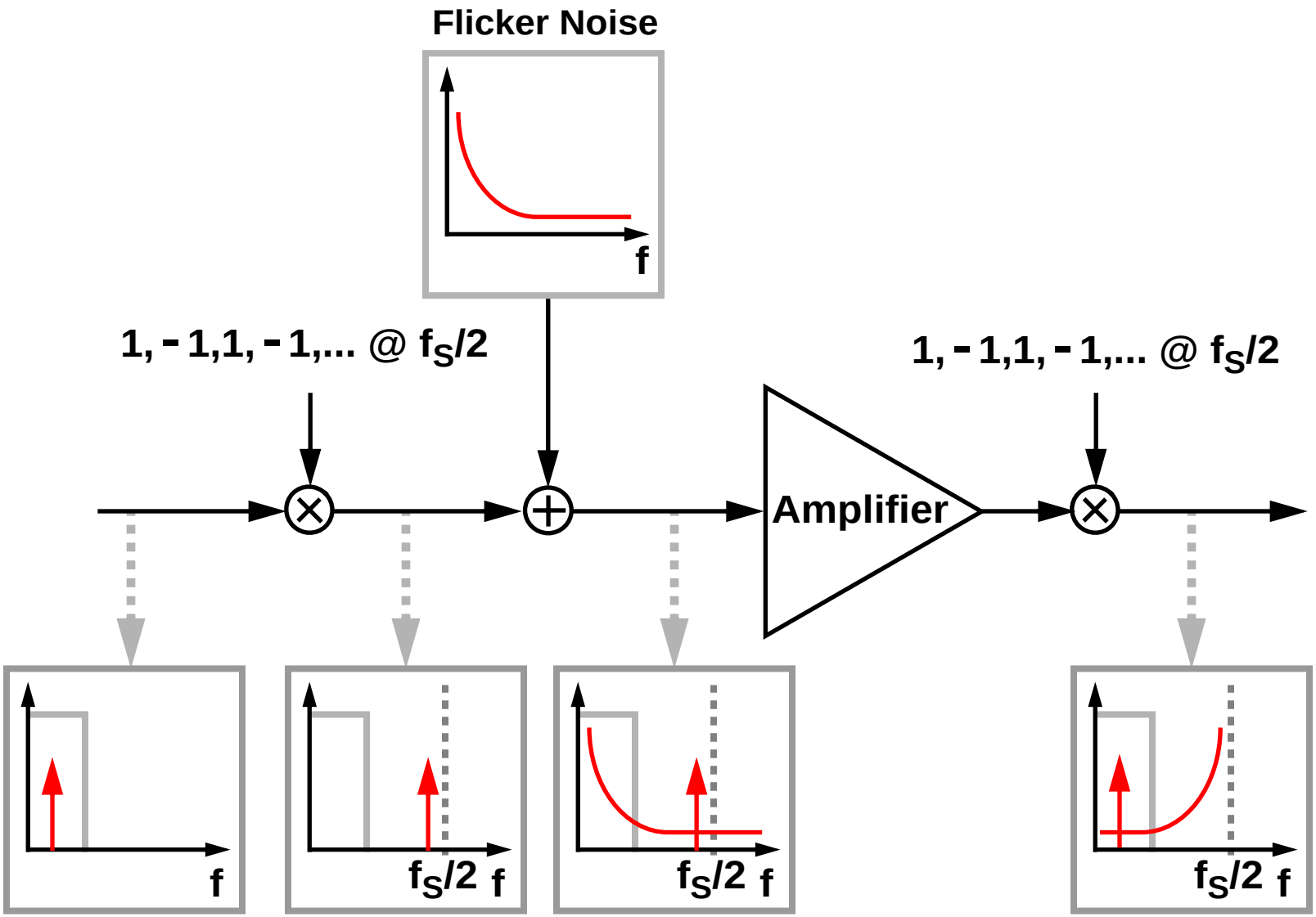


$V_{o1} \sim z^{-1}(1-z^{-1})^2 \cdot X - z^{-1}(1-z^{-1}) \cdot E_Q$

$V_{o1} = (1+z^{-1}) \cdot X - z^{-1}(1-z^{-1}) \cdot E_Q$

* -1 dB, 8 kHz input sinusoid (V_{ref}=0.7V)

Flicker Noise Reduction



- **Chopper stabilization**

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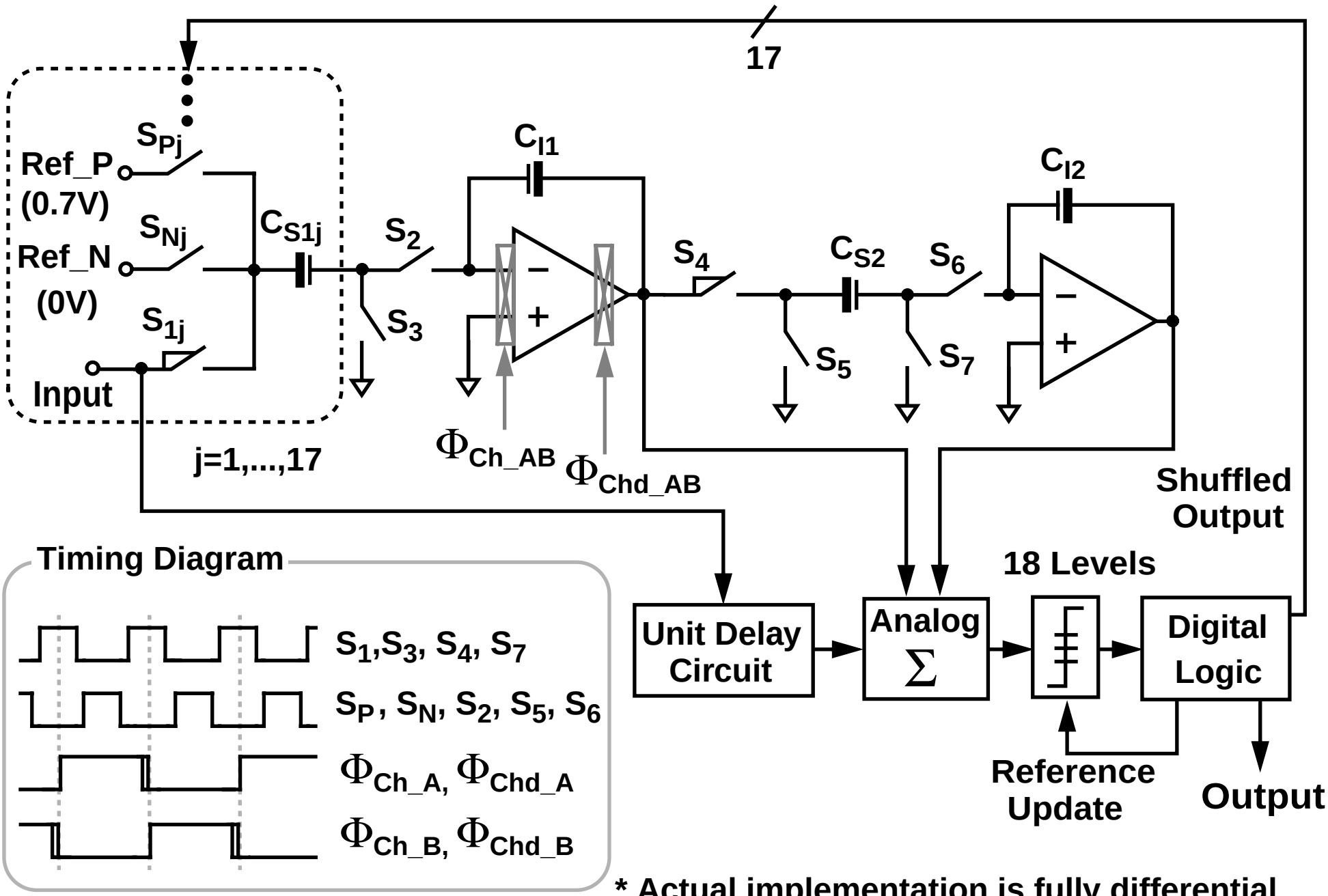
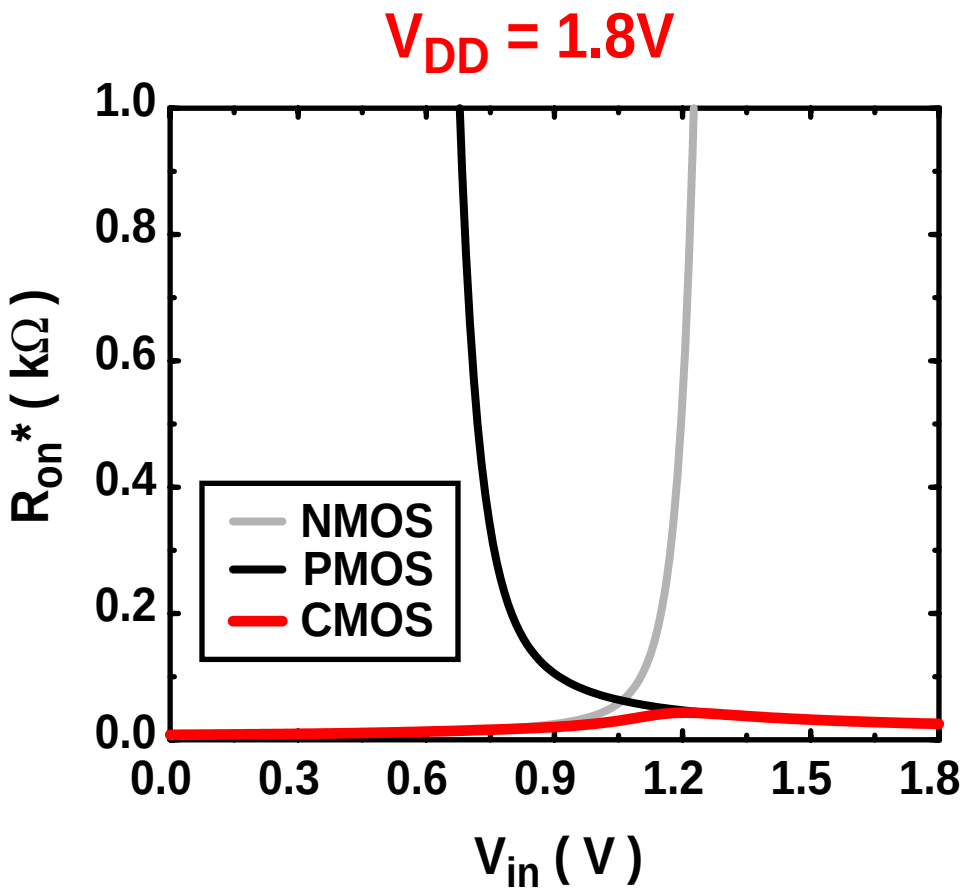
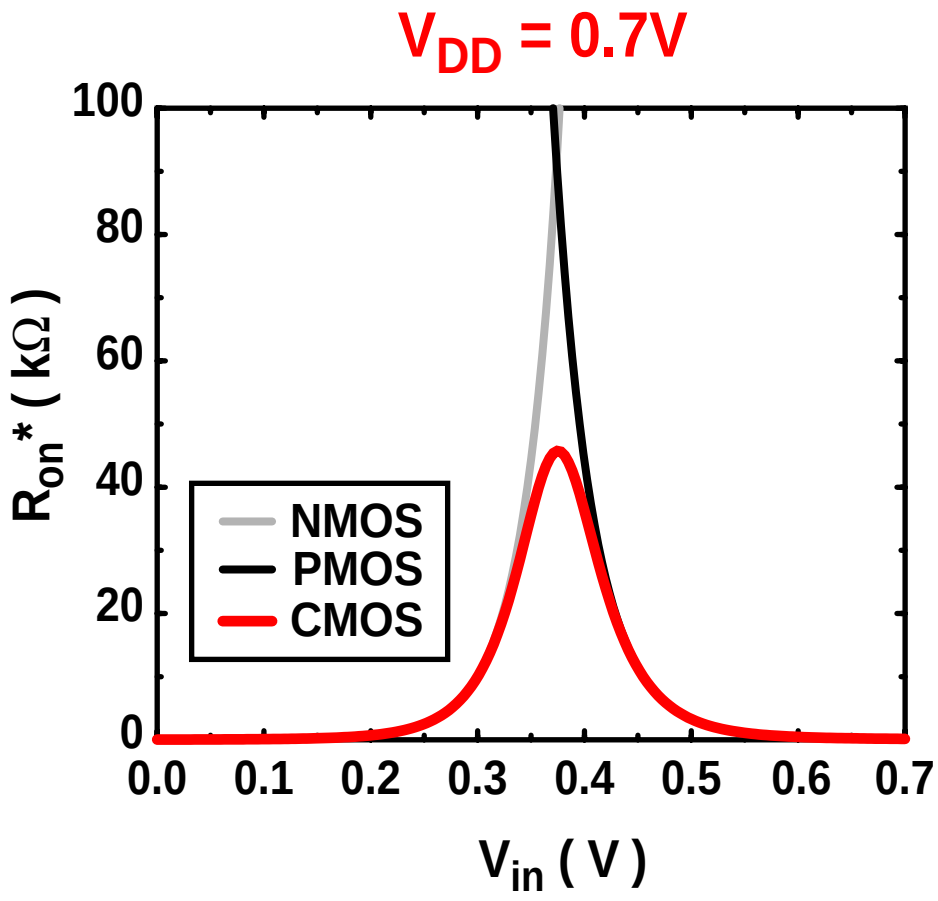
Modulator Architecture*



* Actual implementation is fully differential

Switch at Low Supply Voltage

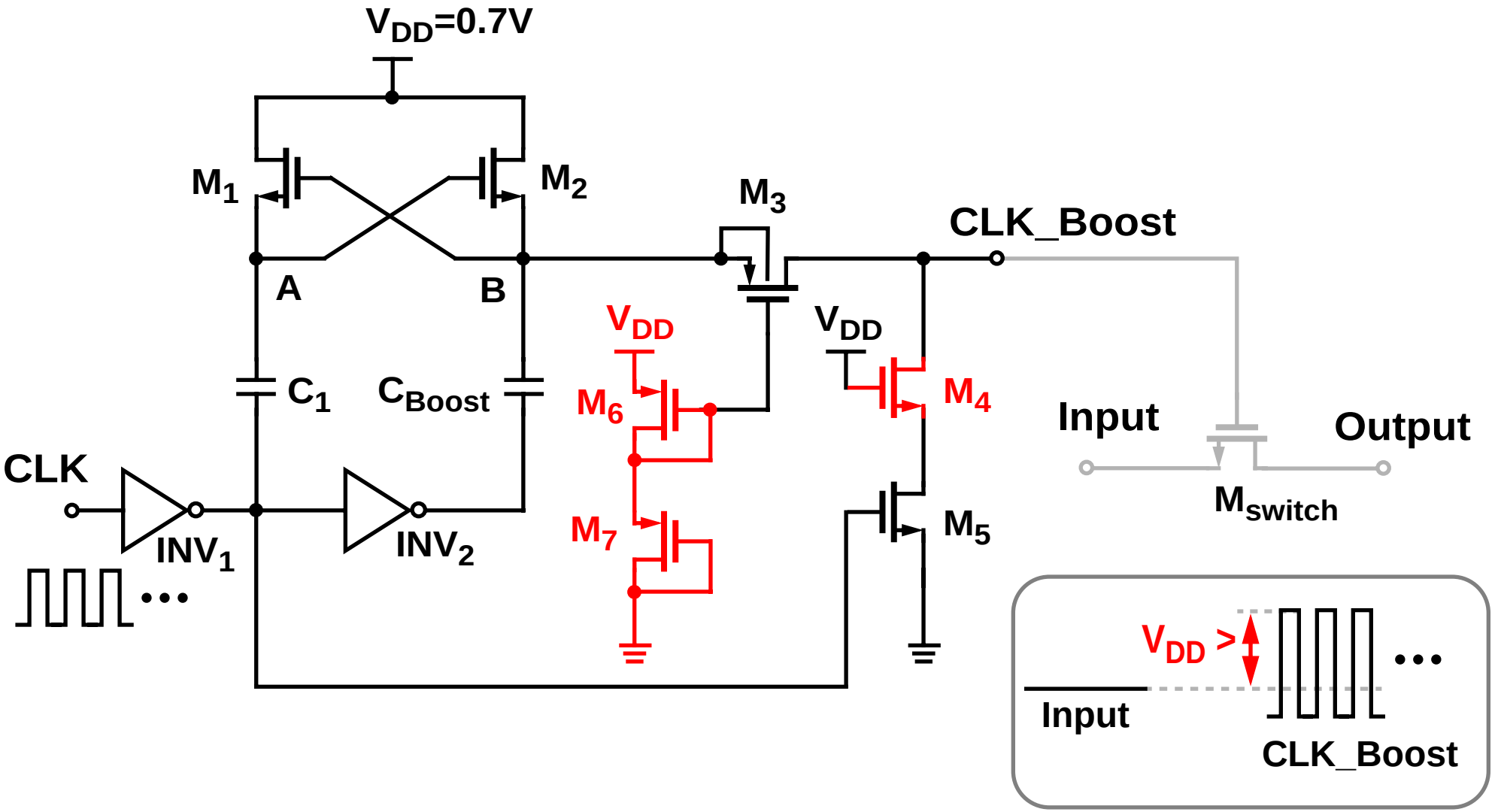




*CMOS 0.18μm, L=0.18μm, W=100μm, V_{ov}=0.2V

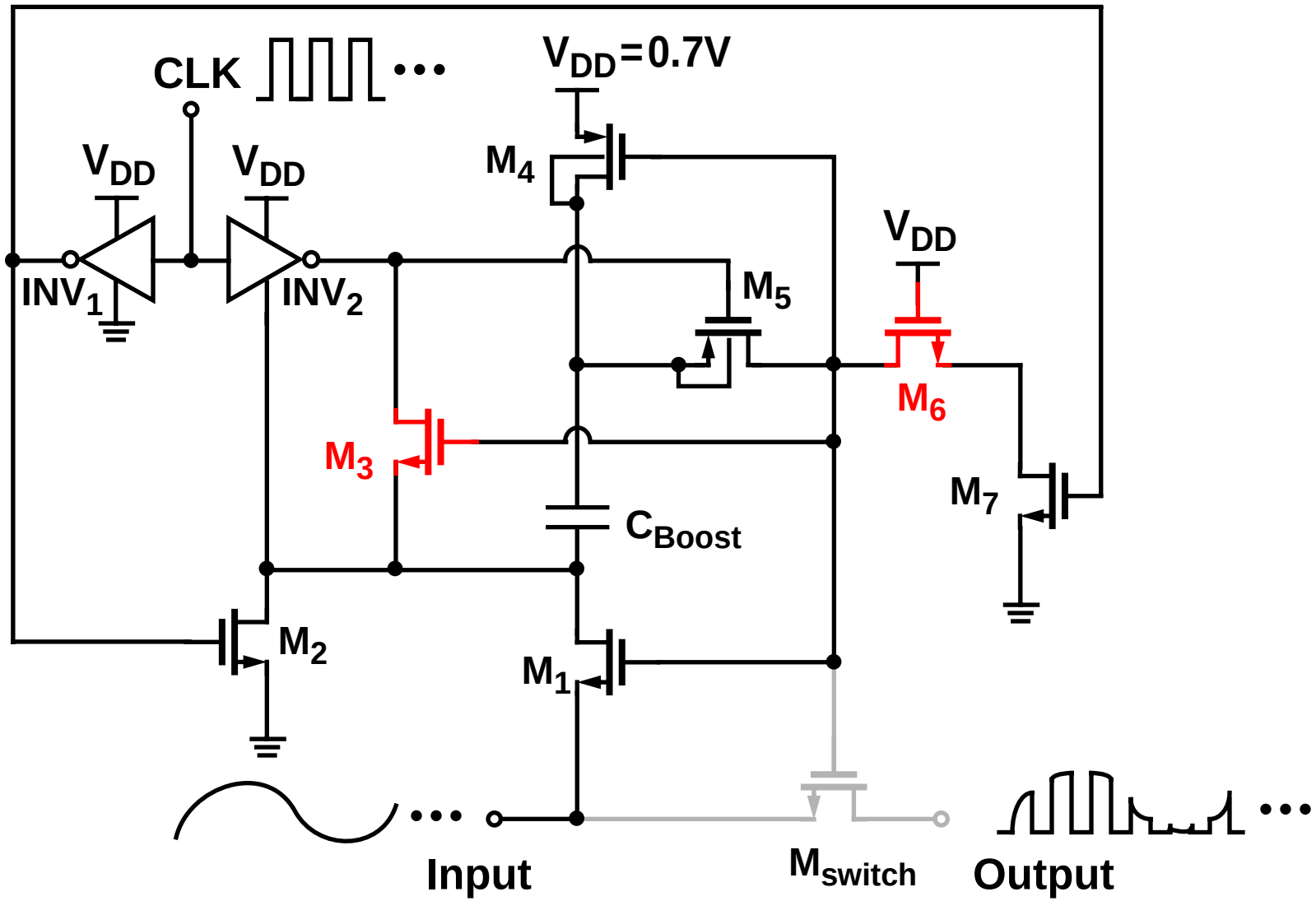
- **Limited switch input range at low supply voltage**

Low-Voltage Switch: Local Boosting



- **Used to process DC signals**

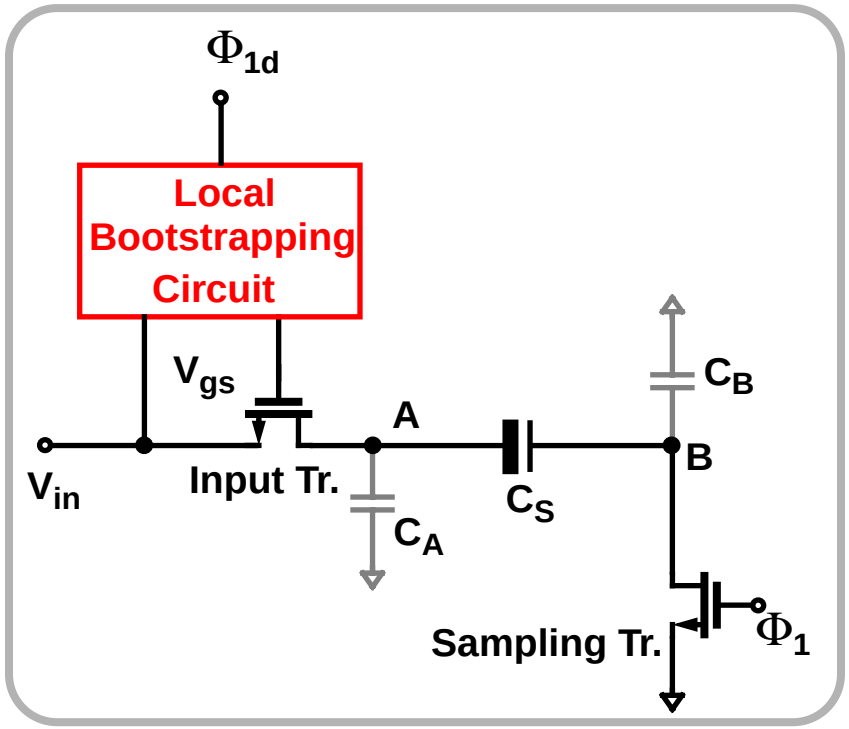
Low-Voltage Switch: Local Bootstrapping*



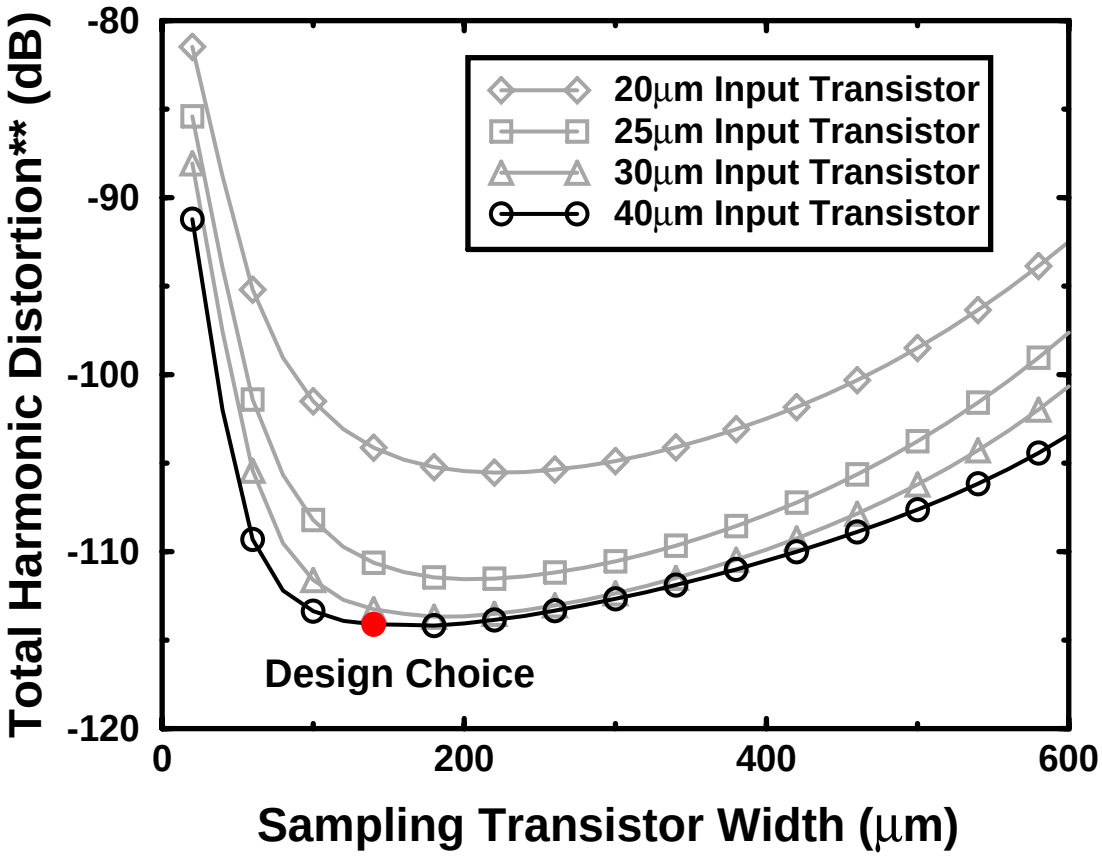
- **Used to process dynamic signals with high-precision**

*** M. Dessouky, JSSC 2001**

Input Sampling Network Design*



Timing Diagram

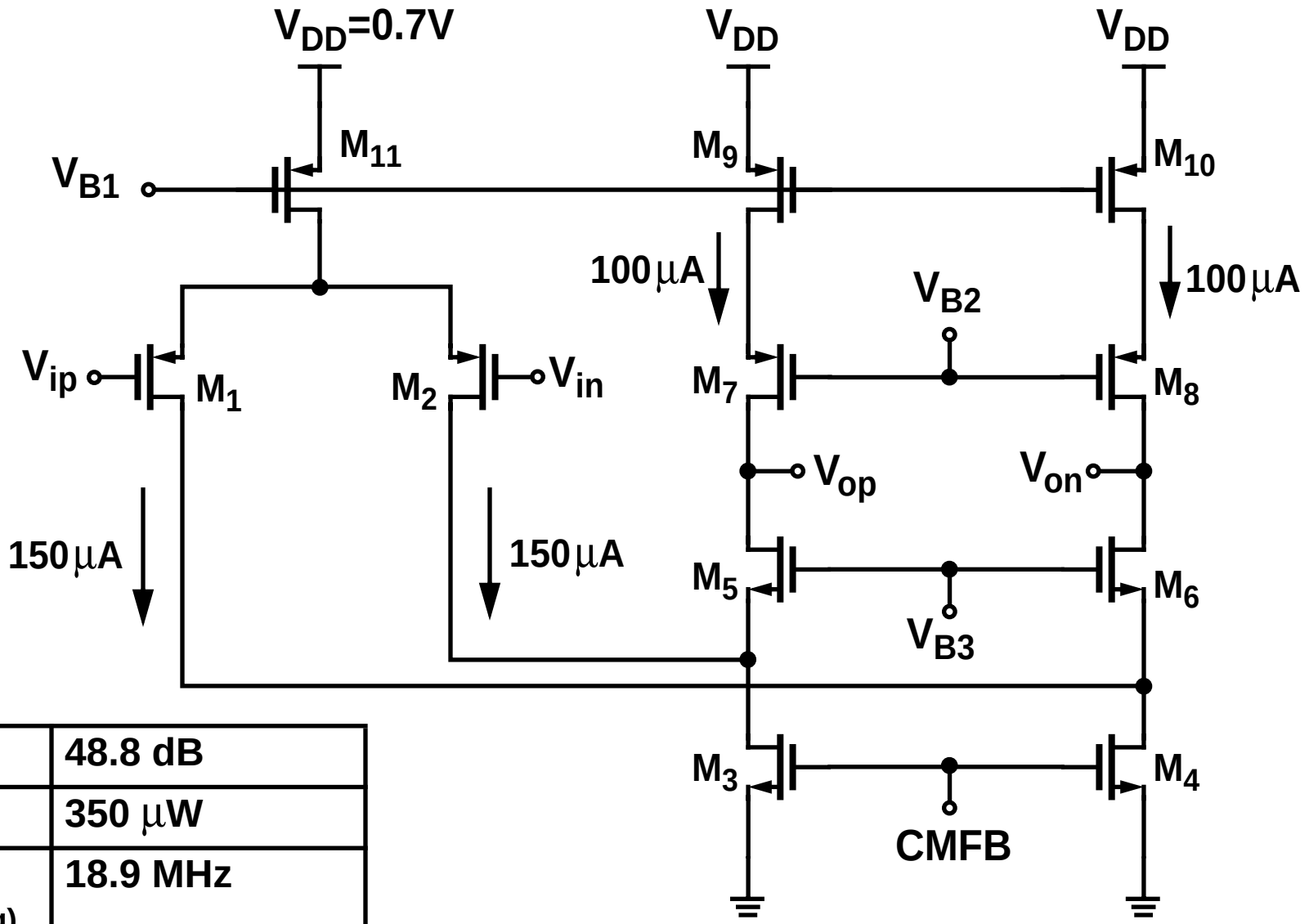


* Actual implementation is fully differential

**0 dB, 7.328 kHz Input Sinusoid (V_{ref} = 0.7V)

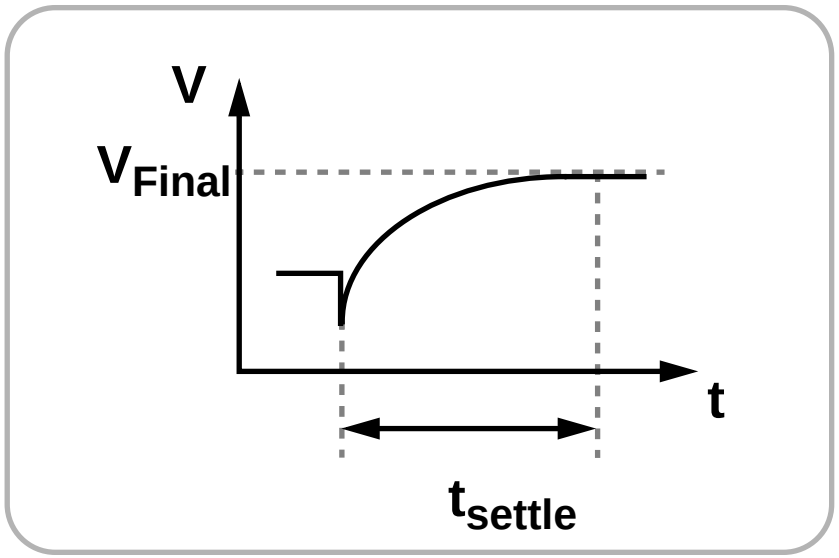
- **-113 dB THD with 18pF input sampling capacitor (C_S) @ 0.7-V supply**

First Integrator Op Amp



DC Gain	48.8 dB
Power	350 μW
BW_u (@ 18pF loading)	18.9 MHz
V_{CM}	0V (Input), 0.35V (Output)

Op Amp Power Reduction



$$n = \frac{t_{settle}}{\tau}$$

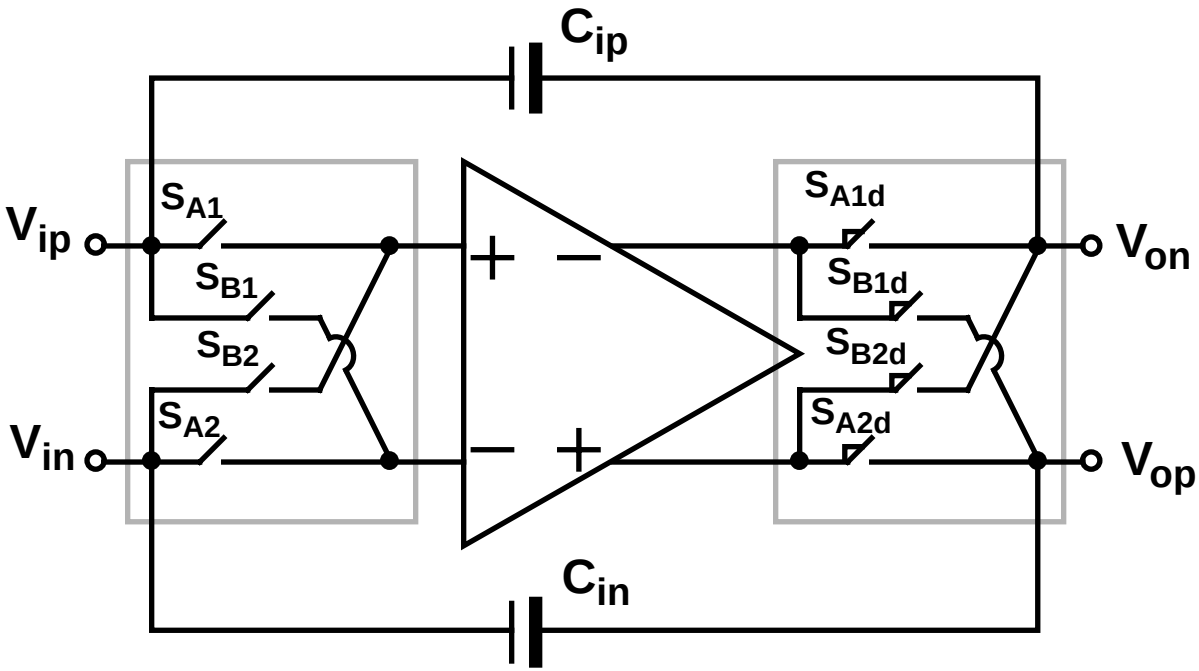
n	Gain Error
1	0.632
2	0.865
3	0.950
4	0.982
5	0.993
6	0.998

$$V(t_{settle}) = V_{Final} \cdot \left(1 - e^{-\left(\frac{t_{settle}}{\tau}\right)}\right)$$

Fixed Integrator Gain Error

- Reduced integrator input swing → op amp never slews
- Incomplete but linear settling op amp → low power
- In implementation, n ~ 3.8

Chopper Stabilization Circuit

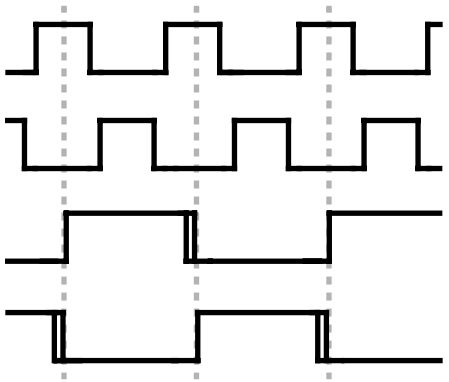


Switch Symbols

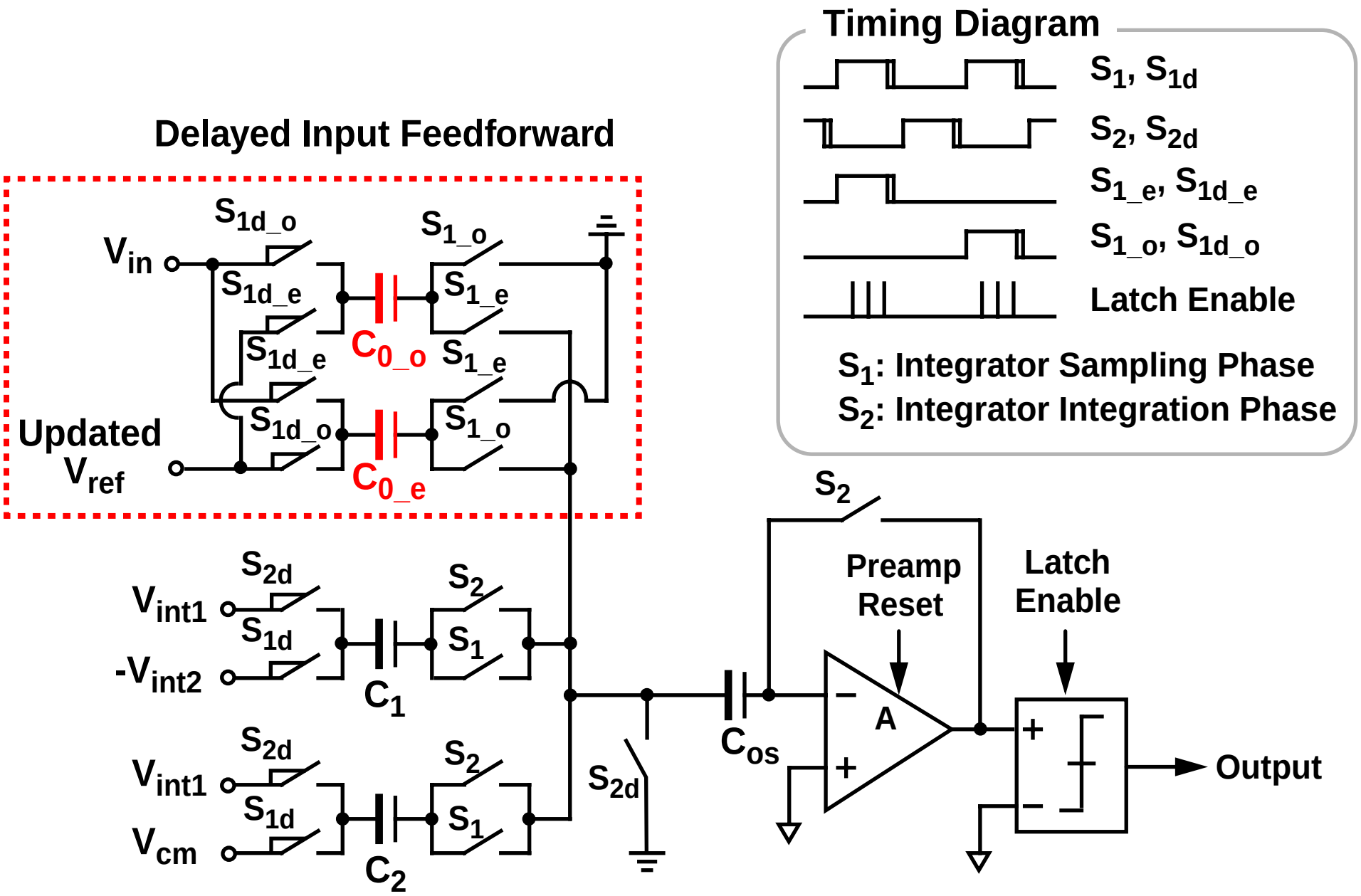
NMOS switch

NMOS switch with local gate bootstrapping

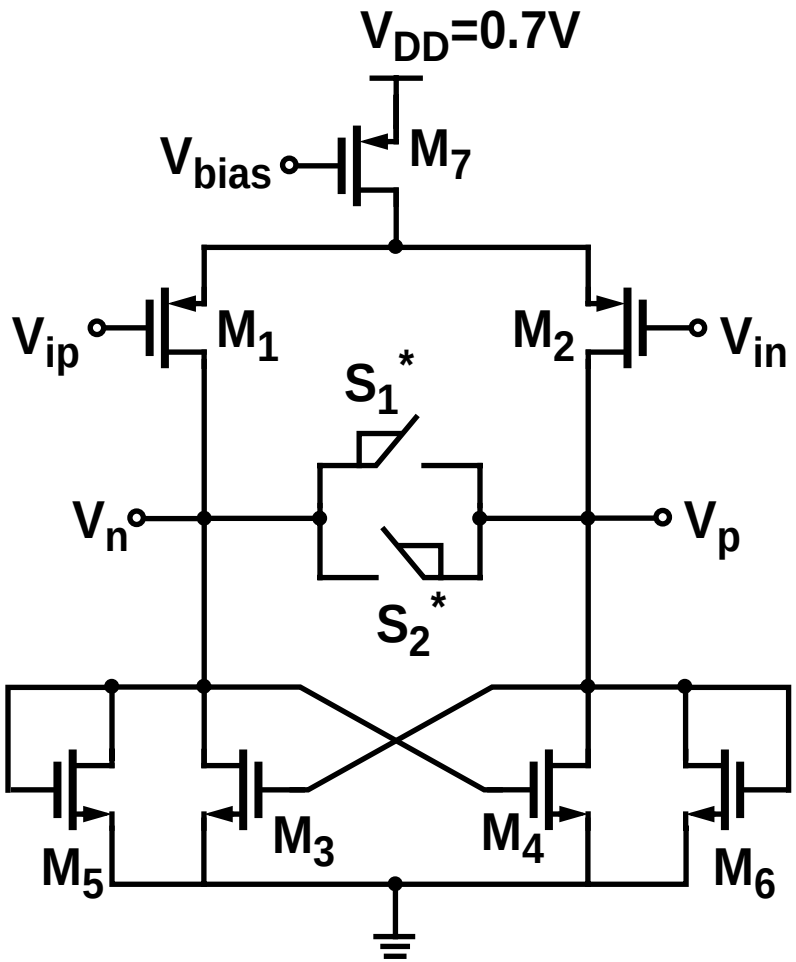
Timing Diagram

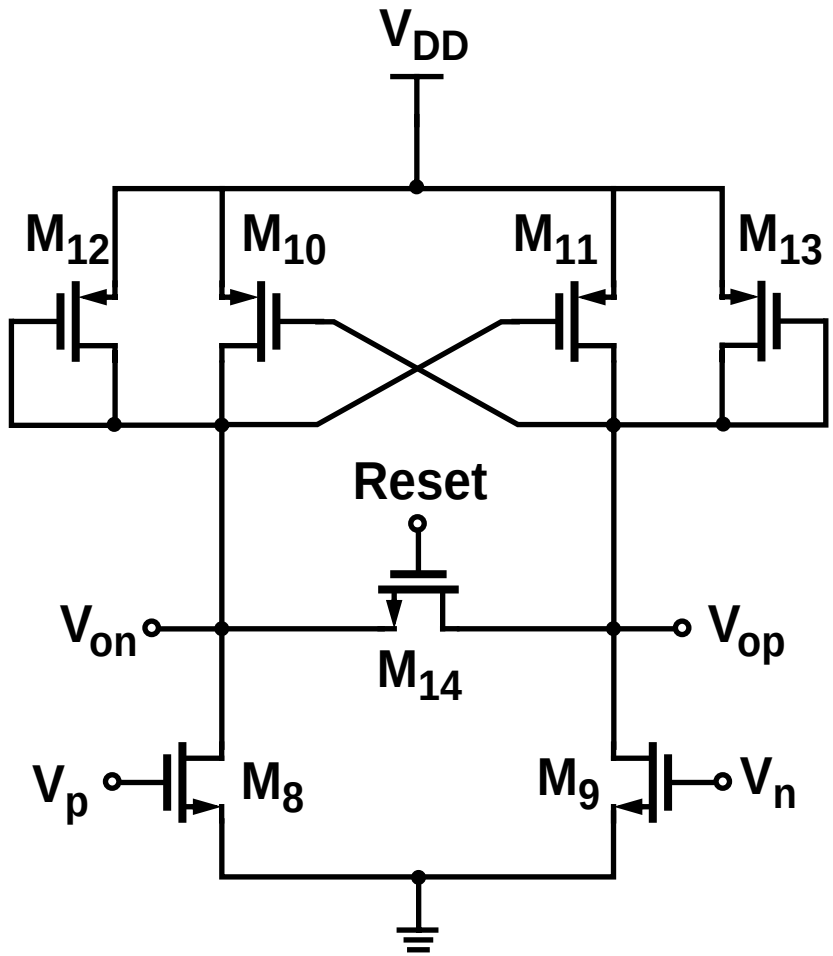


Analog Summation and Quantizer



Comparator Preamps



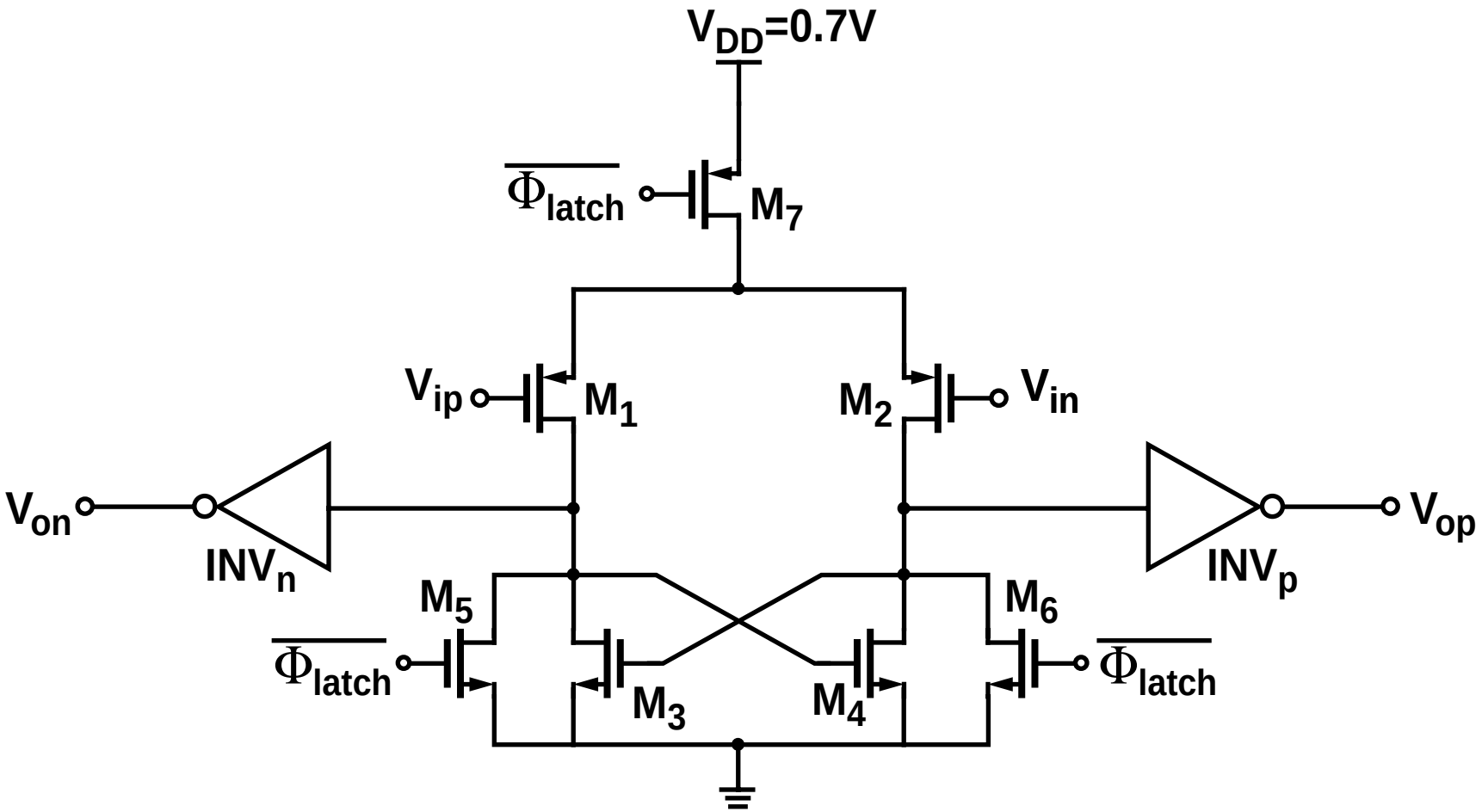


*S_1, S_2: Bootstrapped NMOS Switch

When cascaded,

DC Gain	6.8	$BW_{open\text{-}loop\ 3dB}$	174 MHz
Power	149 μW	$BW_{closed\text{-}loop\ unity}$	140 MHz
3-σ V_{os}	19 mV	Phase Margin	58 Degree

Comparator Latch*



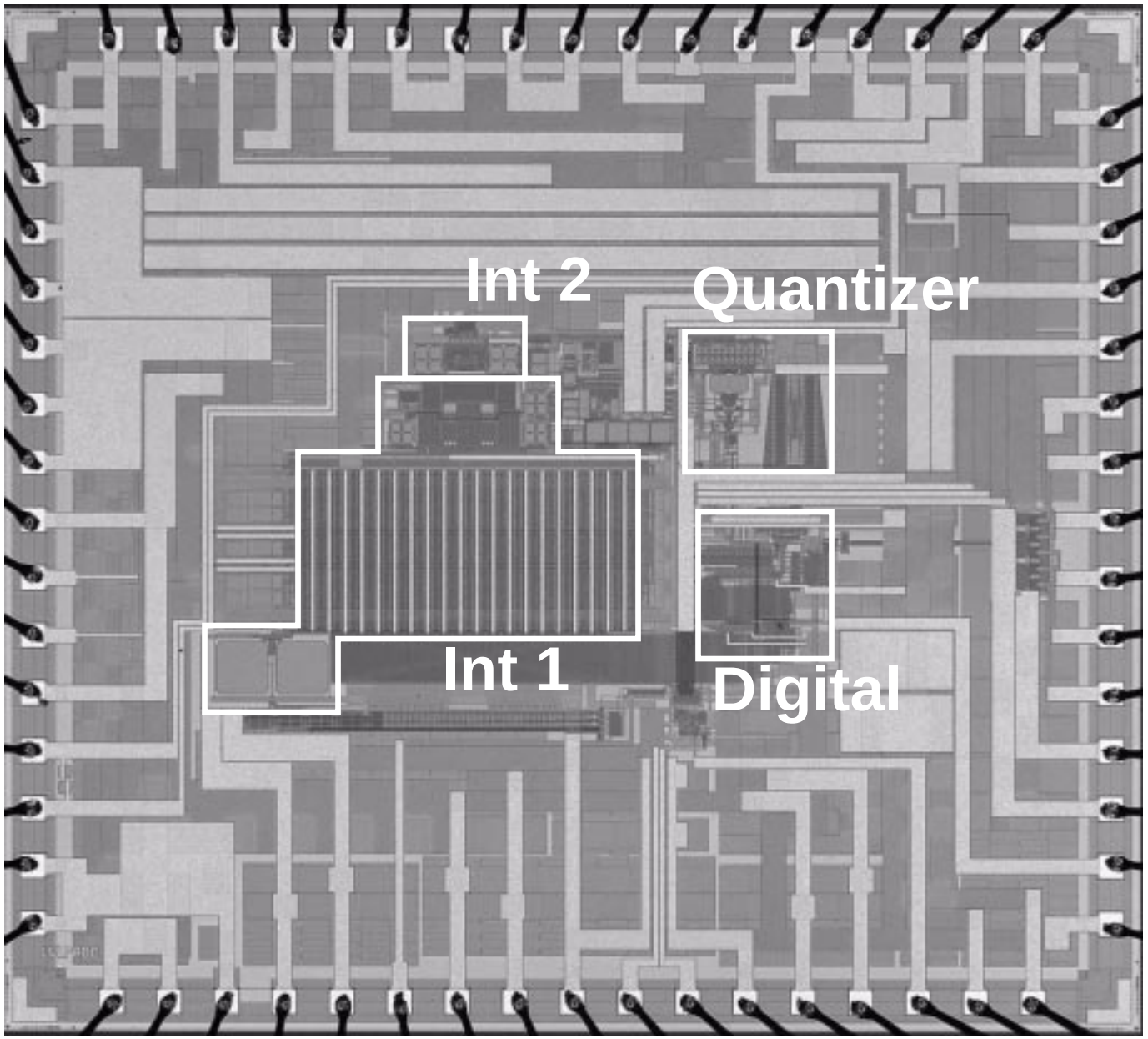
Average Power	~14 μW
t_{regen} @ 5 mV_{pp} input	~2.1 nsec
3-σ V_{os}	23 mV

*S. Limotyrakis, ISSCC 2004

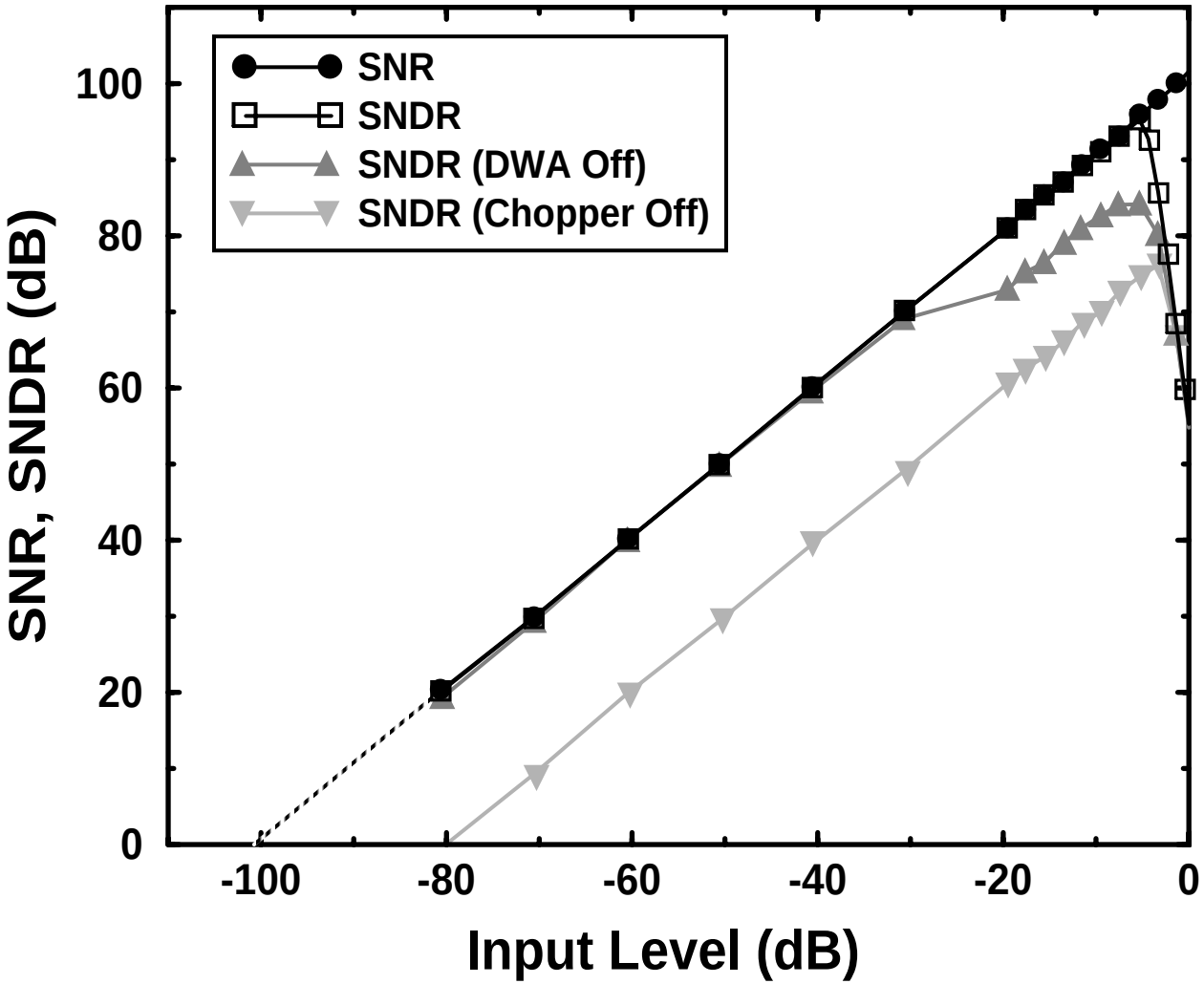
Outline

- Introduction
- Proposed ADC architecture
- Implementation
- **Experimental results**
- Conclusion

Prototype Chip Photograph

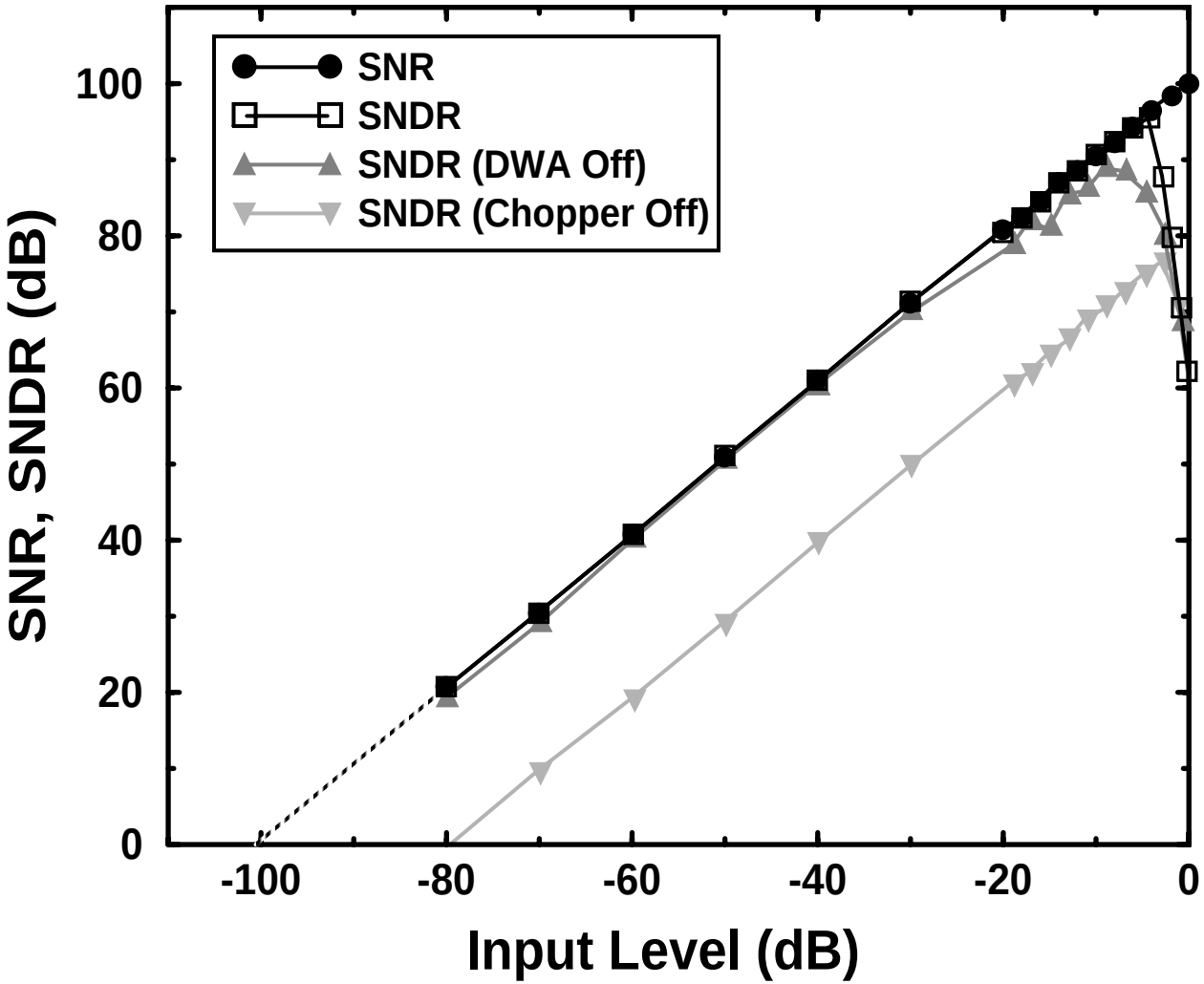


Measured SNDR (1 of 2)



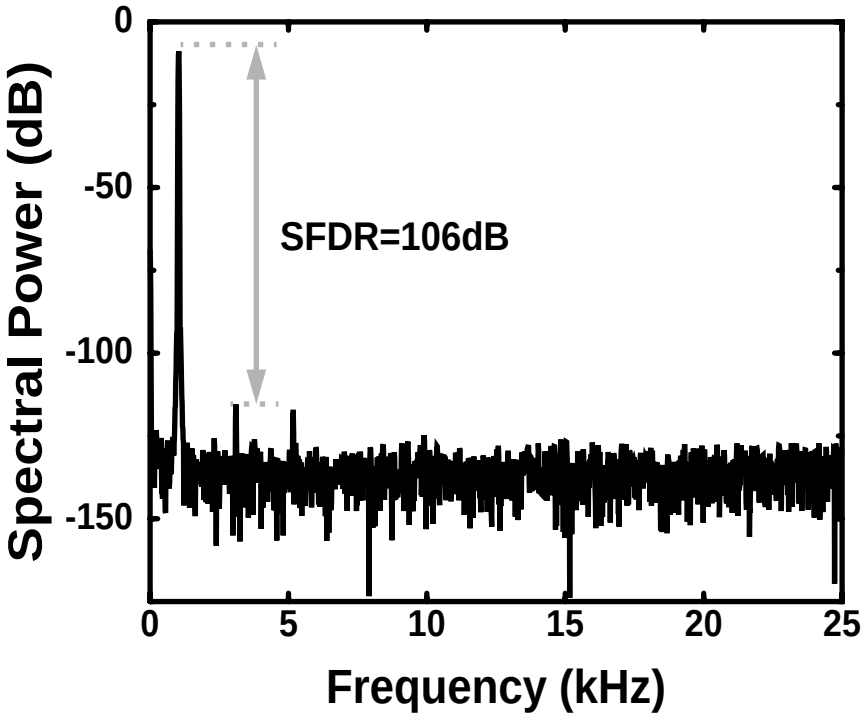
- 1 kHz input sinusoid

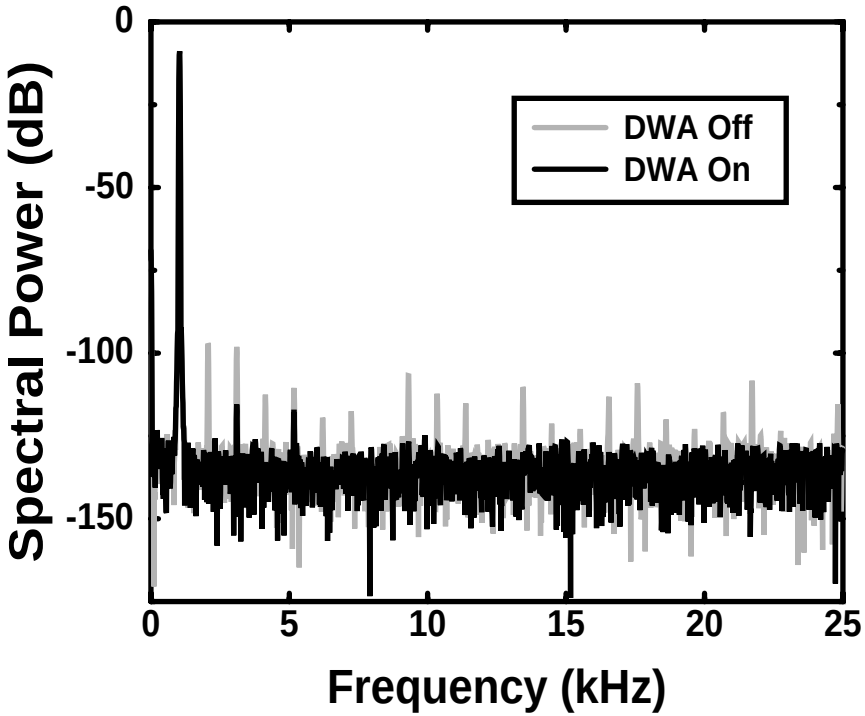
Measured SNDR (2 of 2)



- **8 kHz input sinusoid**

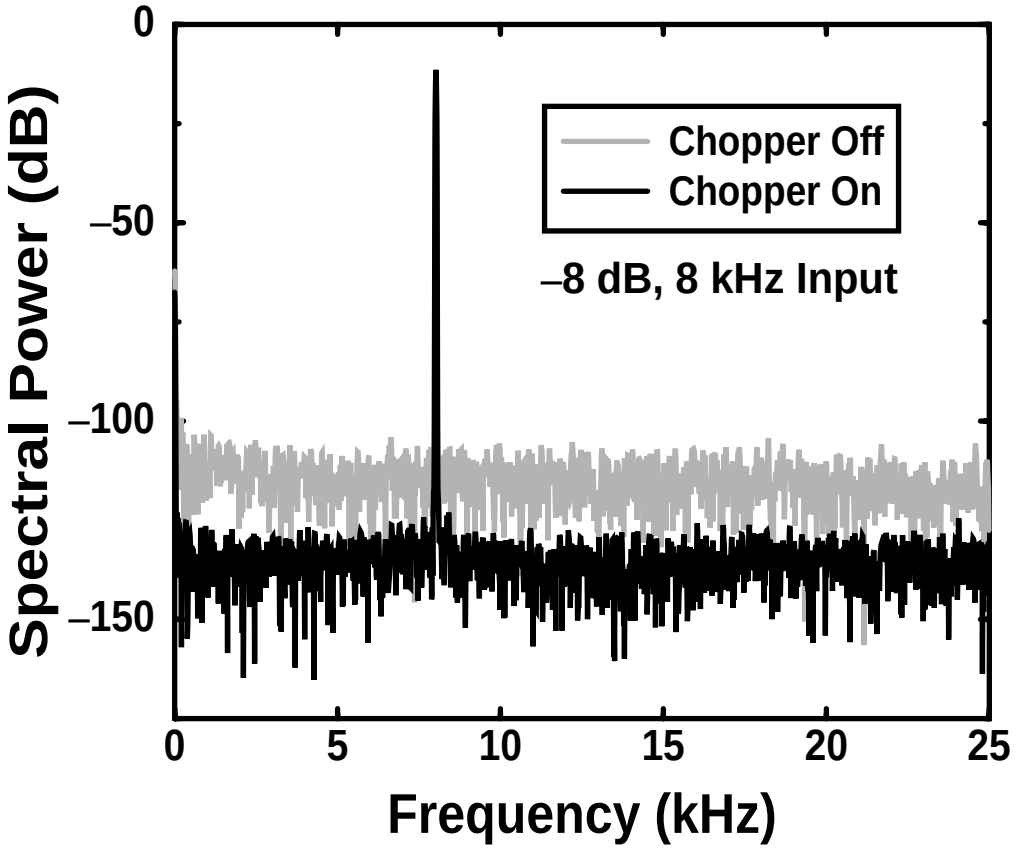
Measured Output Spectrum (1 of 2)





- -5 dB, 1 kHz input sinusoid
- DWA provides required linearity

Measured Output Spectrum (2 of 2)



- -8 dB, 8 kHz input sinusoid
- Chopper stabilization effectively removes flicker noise

Performance Summary

Supply Voltage	0.7 V
Sampling Rate	5 MHz
References	0 V, 0.7 V
Signal Bandwidth	25 kHz
Dynamic Range	100 dB
Peak SNR	100 dB
Peak SNDR	95 dB
Power: Analog Digital	680 μW 190 μW
Area (excluding decoupling capacitors, pads & output drivers)	2.16 mm^2
Technology	0.18-μm CMOS

Comparison

	This Work	G. Ahn, et al., ISSCC 05	K. Poon, et al., ISSCC 06	M. Kim, et al., VLSI 06
Power Supply (V)	0.7	0.6	0.5	0.9
Signal Bandwidth (kHz)	25	24	25	24
Clock Frequency (MHz)	5	3.072	3.2	6.144
OSR	100	64	64	128
Total Power (μW)	870 (Analog : 680)	1000	300	1500
Input Range (Vpp)	1.4	0.8	1	1.1
Dynamic Range (dB)	100	78	N/A	92
Peak SNR (dB)	100	77	76	91
Peak SNDR (dB)	95	77	74	89
Active Die Area (mm^2)	1.8 x 1.2	1.8 x 1.6	0.6	1.6 x 0.9
Technology	0.18μm CMOS	0.35μm CMOS Low V_{th}	0.18μm CMOS Triple Well	0.13μm CMOS
Type	Switched Cap	Switched Cap	Continuous	Switched Cap
Order	2	2 - 2	3	3
Quantization	Multi-bit (18 levels)	1.5-bit	1-bit	1.5-bit

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Conclusion

- **Low-voltage strategies**
  - **Input feedforward + Multi-bit quantization**
  - **Locally boosted or bootstrapped switches**
- **Low-power strategies**
  - **Tracking multi-bit quantization**
  - **Delayed input feedforward**
  - **Incomplete but linear op amp settling**
- **High-precision strategies**
  - **Input feedforward**
  - **Single comparator multi-bit quantization scheme**
  - **Chopper stabilization**
- **Analog-to-digital interface design challenges imposed by technology scaling can be overcome by architecture level innovation and circuit level solutions**