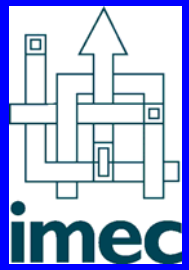
RF ESD Protection Strategies – The Design and Performance Trade-off Challenges



Ph.Jansen, S.Thijs, D.Linten, M.I.Natarajan
V.Vassilev, M.Liu, D.Trémouilles,
S.Decoutere, G.Groeseneken

T.Nakaie, M.Sawada, T.Hasebe

A.Concannon, V.Vashchenko, M.ter Beek

Outline of Presentation

- Introduction
- Key performance parameters
- Diode protection with Power Clamp
- Inductor protection with Power Clamp
- Full circuit – ESD co-design
- Partial circuit – ESD co-design
- Conclusions

Introduction: RF circuit design

Integrated RF front-ends @ 5.5 GHz

- **90nm CMOS technology**
- **BiCMOS technology**

Typical design for performance:

- **Large gain**
- **Low noise**
- **Linearity**

➢ **But ESD protection is often overlooked**

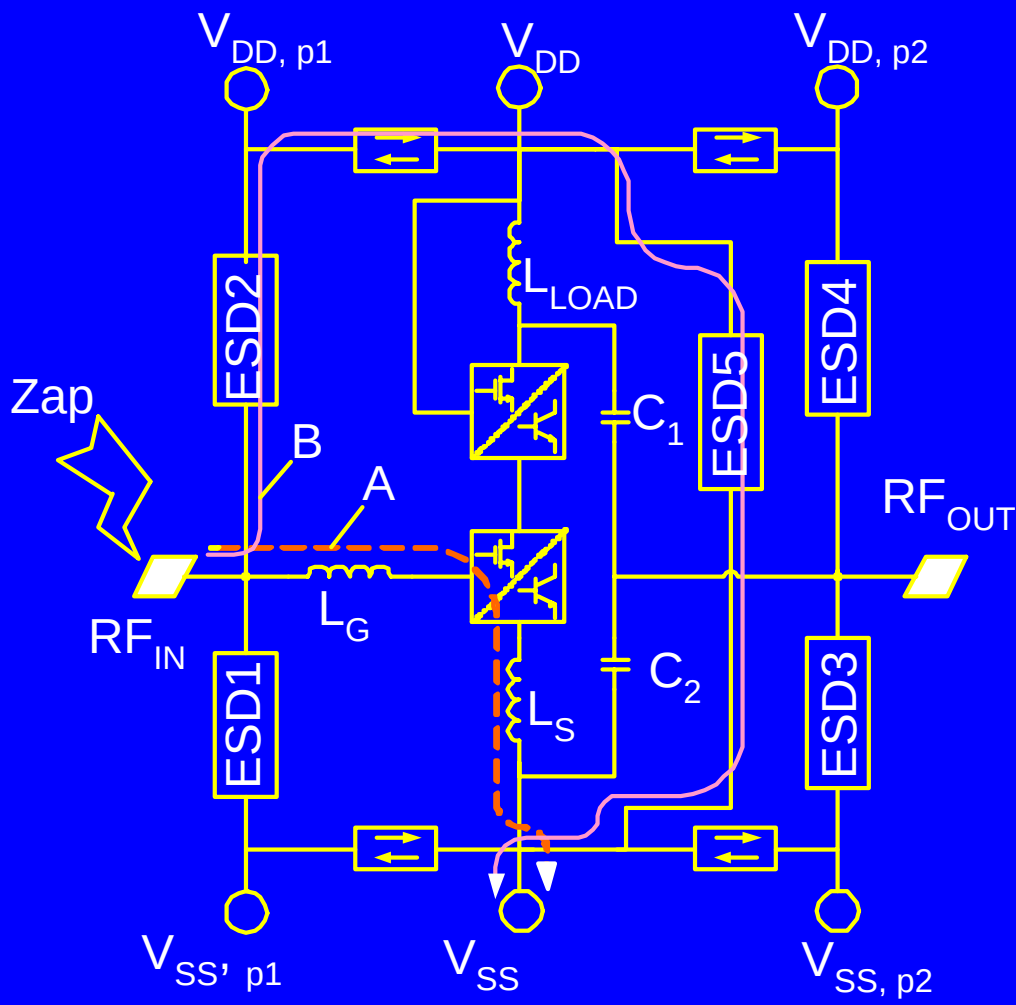
Introduction: RF circuit design

Common issues of ESD protection:

- **Extra input capacitance**
- **Gain reduction**
- **Noise increase**
- **…**

➢ **Comparison of advantages and dis-advantages of several ESD protection strategies**

Introduction: ESD protection



- Diode protection with power clamp
- Inductor protection with power clamp
- Distributed protection
- Resonant and cancellation
- Co-design

Key performance parameters

Performance figure	Target Value (@ f_C)
f_C	5.5 GHz
S11	< -10 dB
S22	< -10 dB
S21	> 15 dB
S12	< -30 dB
NF	< 3 dB
IIP3	As high as possible
Ptot	As low as possible
Area	As small as possible
ESD protection level	> 2 kV HBM

Key performance parameters

- **Low-power RF Figure-Of-Merit**

$$FOM_1[mW^{-1}] = \frac{Gain[abs]}{(NF[abs]-1).P_{DC}[mW]}$$

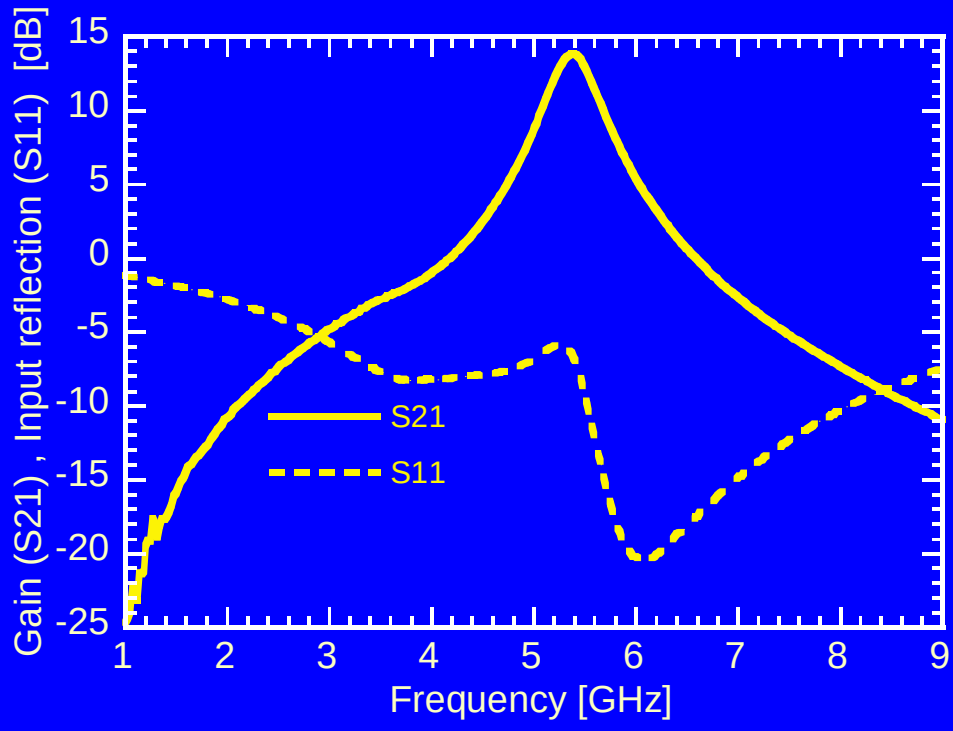
- **Brederlow's RF Figure-Of-Merit**

$$FOM_2[GHz] = \frac{Gain[abs].IIP3[mW].f_C[GHz]}{(NF[abs]-1).P_{DC}[mW]}$$

Diode protection with Power Clamp

BiCMOS LNA

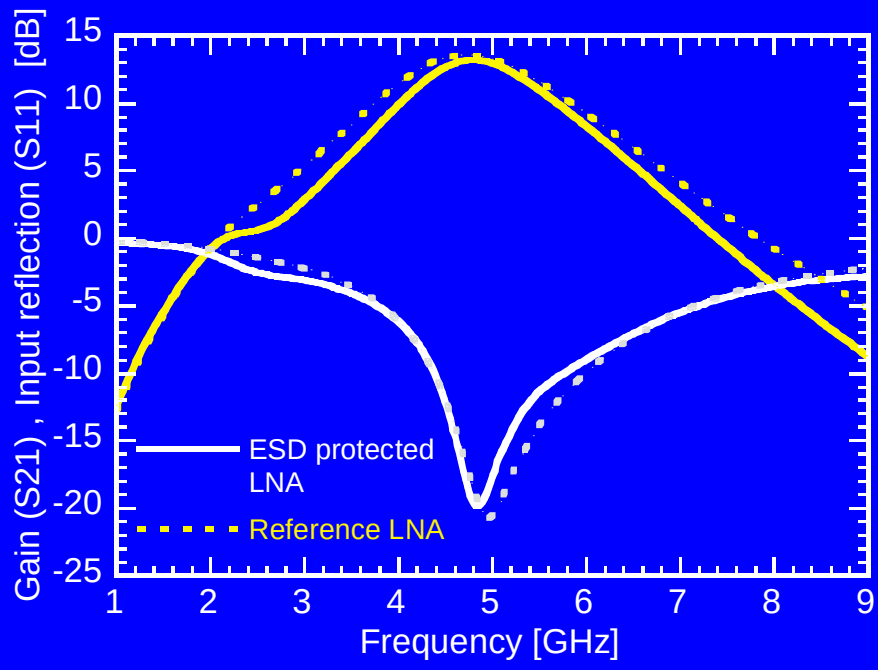
- **F_c = 5.5 GHz**
- **Pn and Np diodes of 71μm^2 (~100fF)**
- **S21 reduction**
- **NF: +0.4 dB**
- **FOM_2 increase**
- **50V -> 3kV HBM**

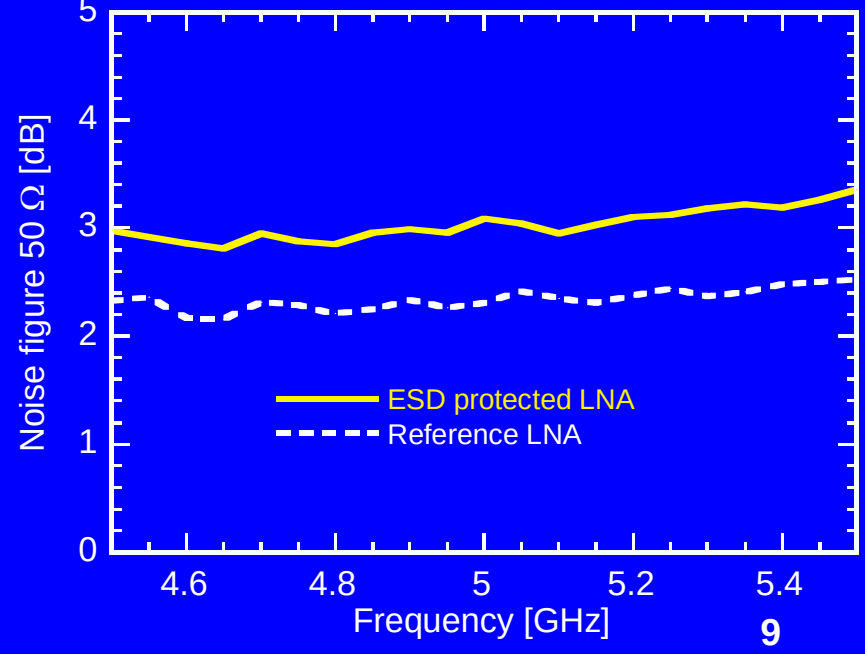


Diode protection with Power Clamp

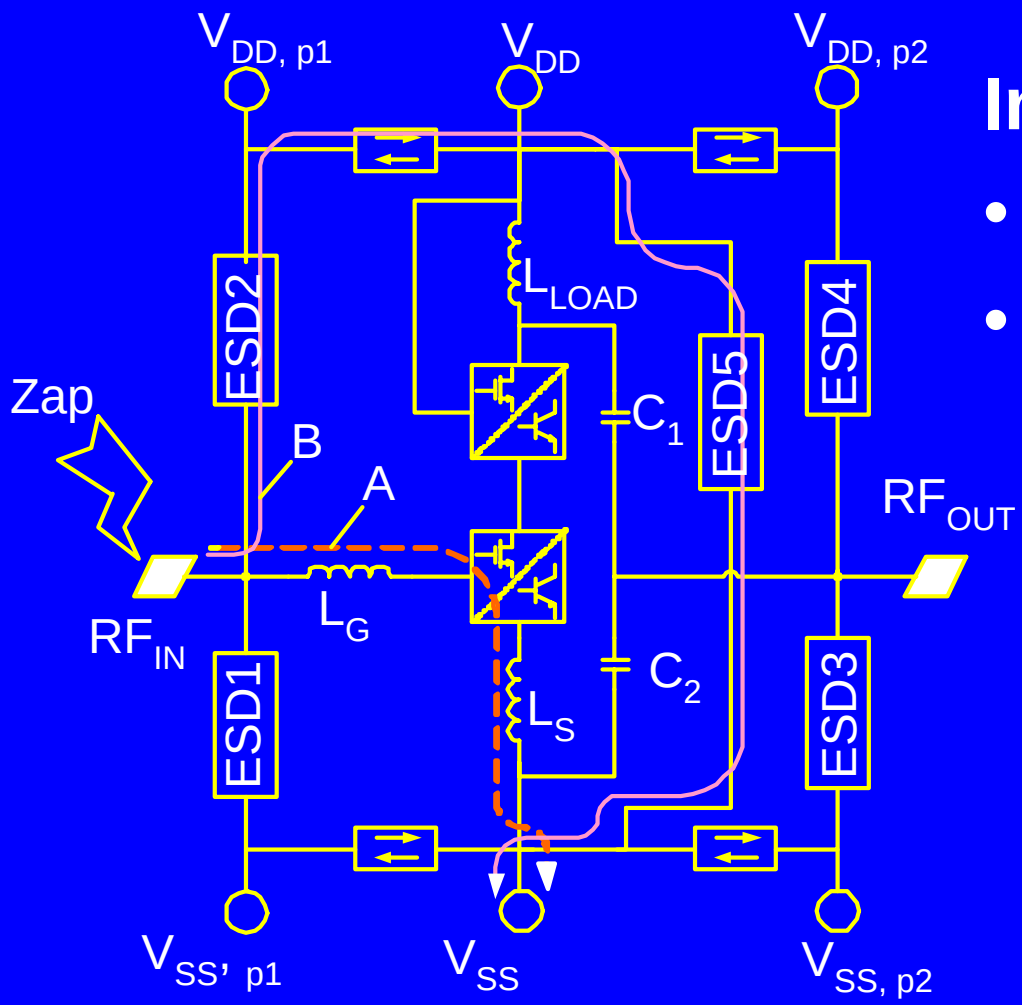
90nm CMOS LNA

- F_c = 5 GHz
- Pn and Np diodes of 65μm^2 (~100fF)
- S21 reduction
- NF: +0.6 dB
- FOM_2 increase
- <50V -> 500V HBM
- Insufficient: Why ?





Diode protection with Power Clamp



Insufficient protection

- **ESD current path B**
- **Parasitic current path A**

Diode protection with Power Clamp

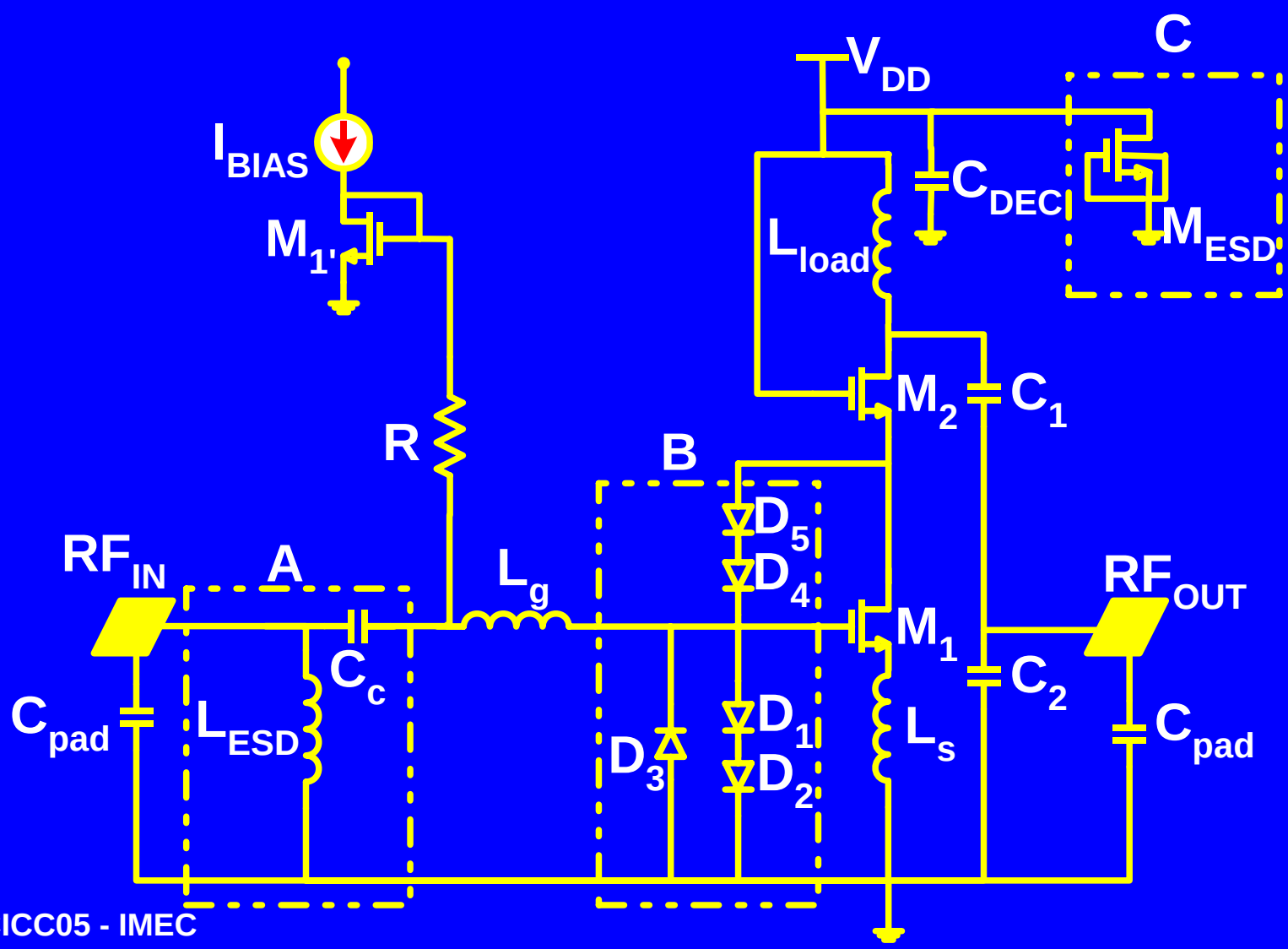
Insufficient protection:

- **BiCMOS LNA: parasitic ESD current flows through L_G, emitter diode and L_S to ground**
- **90nm CMOS LNA: parasitic ESD current loads gate capacitor and builds up over-voltage**

Solutions:

- **On-chip capacitor**
- **Series resistor**

Inductor protection with Power Clamp



Inductor protection with Power Clamp

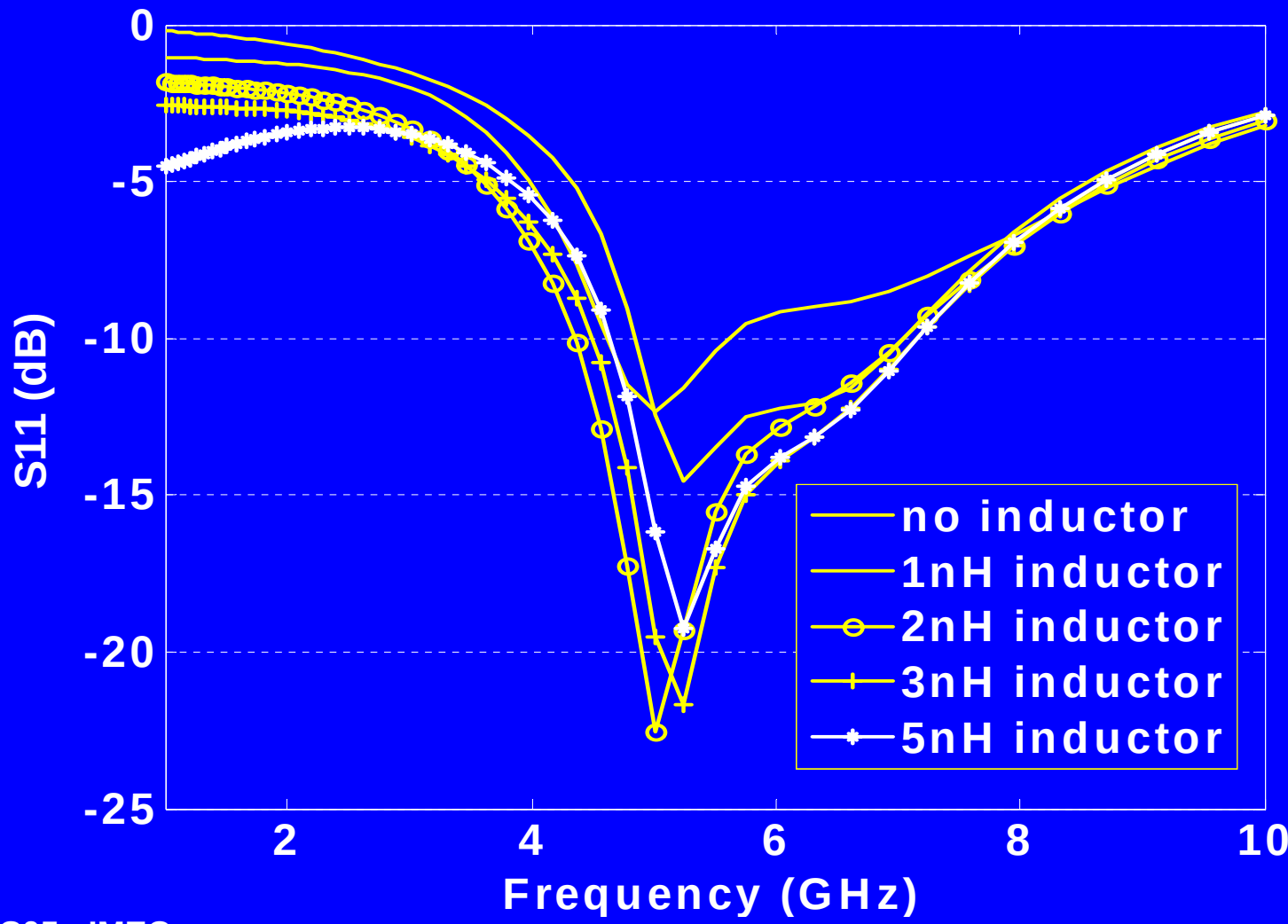
Addition of inductor as “plug-n-play”

- Diverts ESD current to ground
- Is transparent for the RF signal

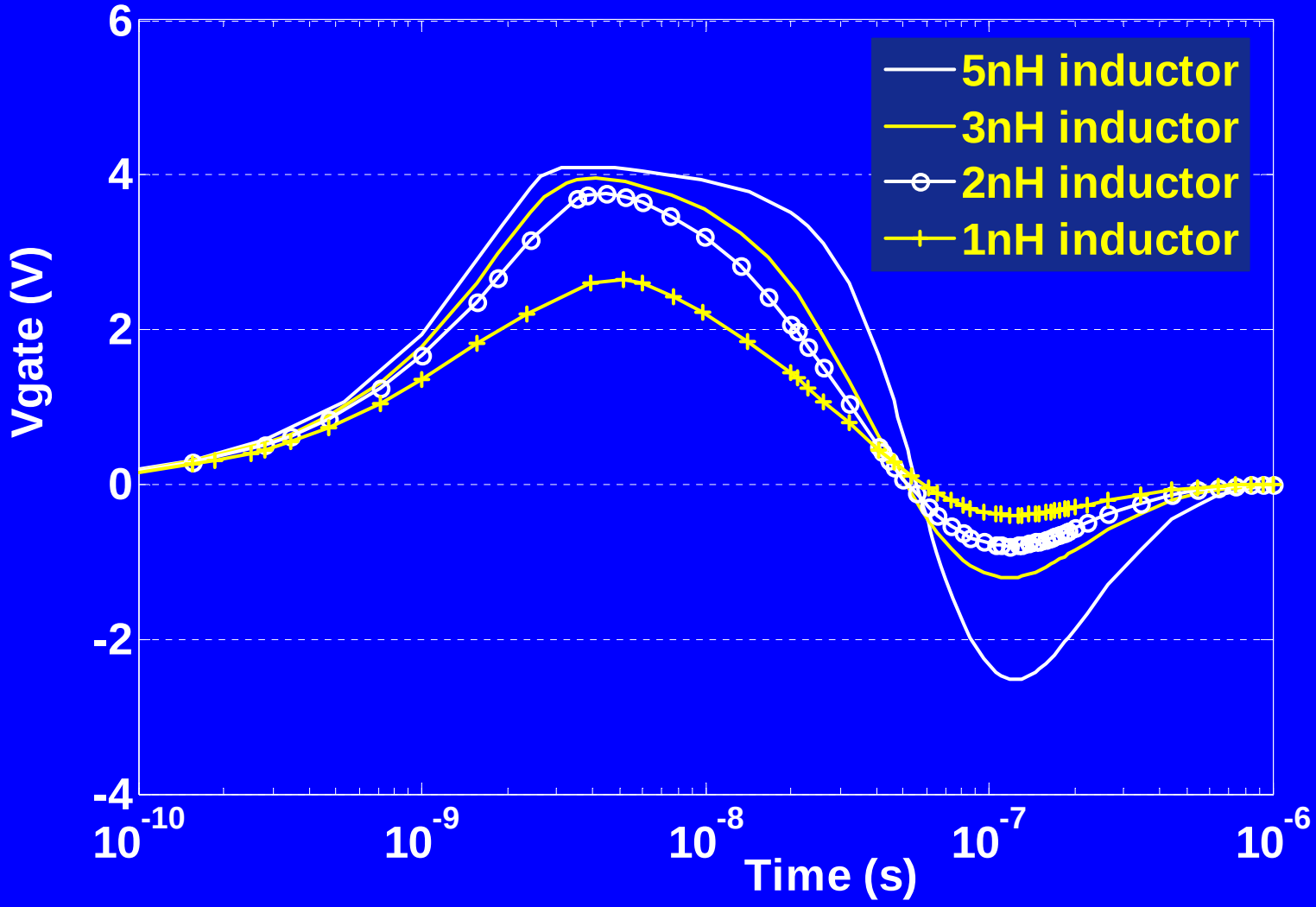
Inductor selection:

- S11 input matching
- Over-voltage at the gate during ESD
- Parasitic resistance of the inductor during ESD and in RF operation

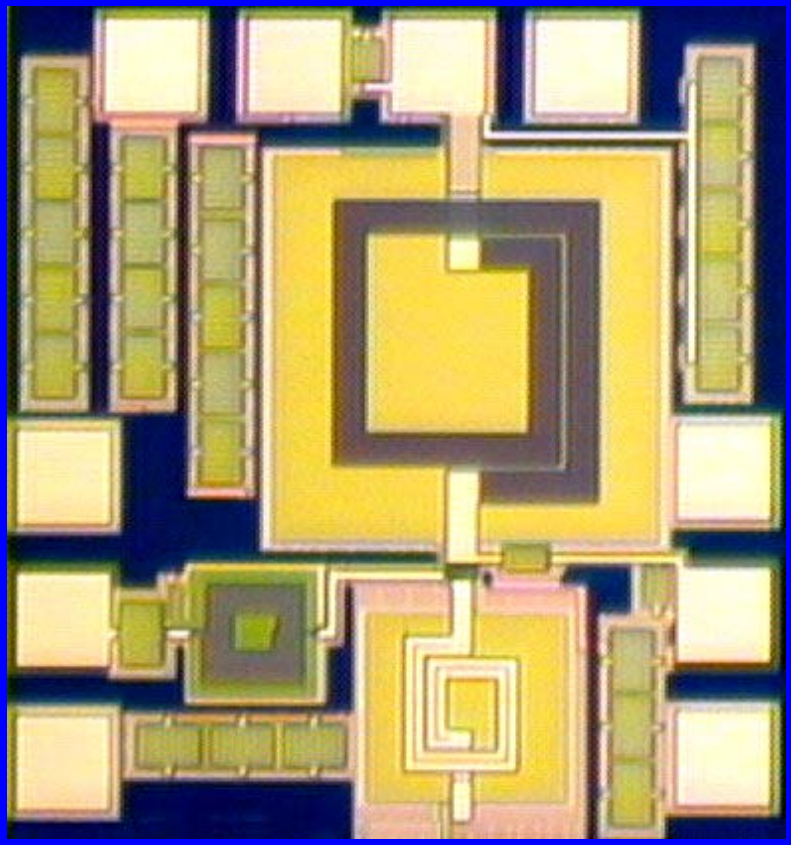
Inductor protection with Power Clamp

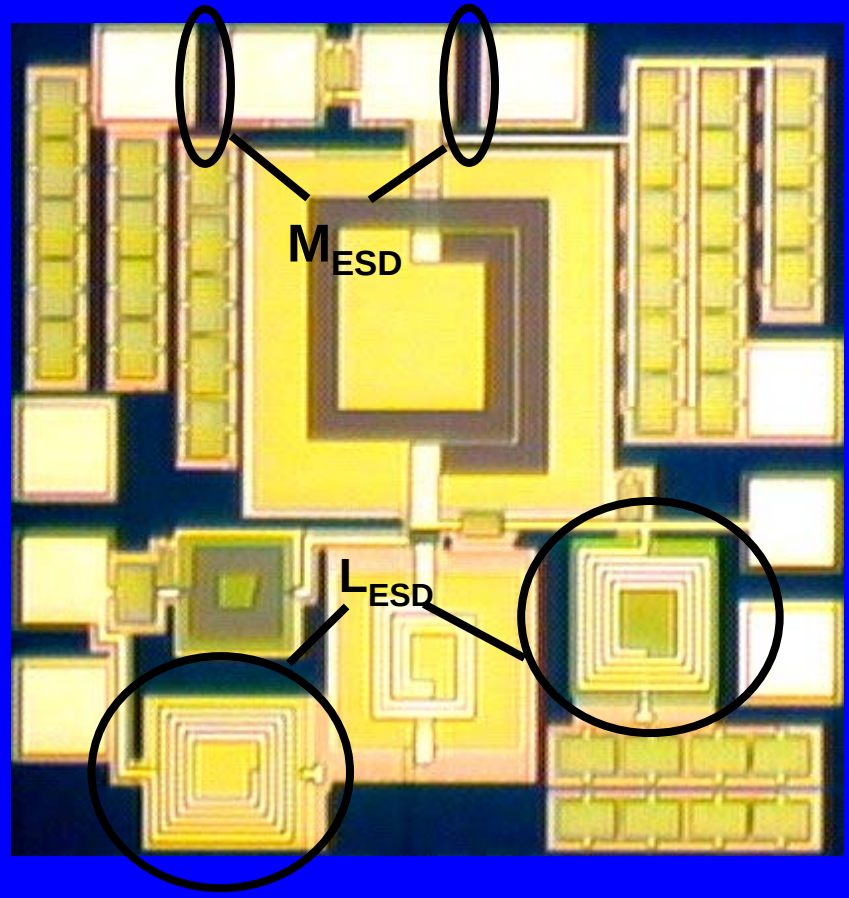


Inductor protection with Power Clamp



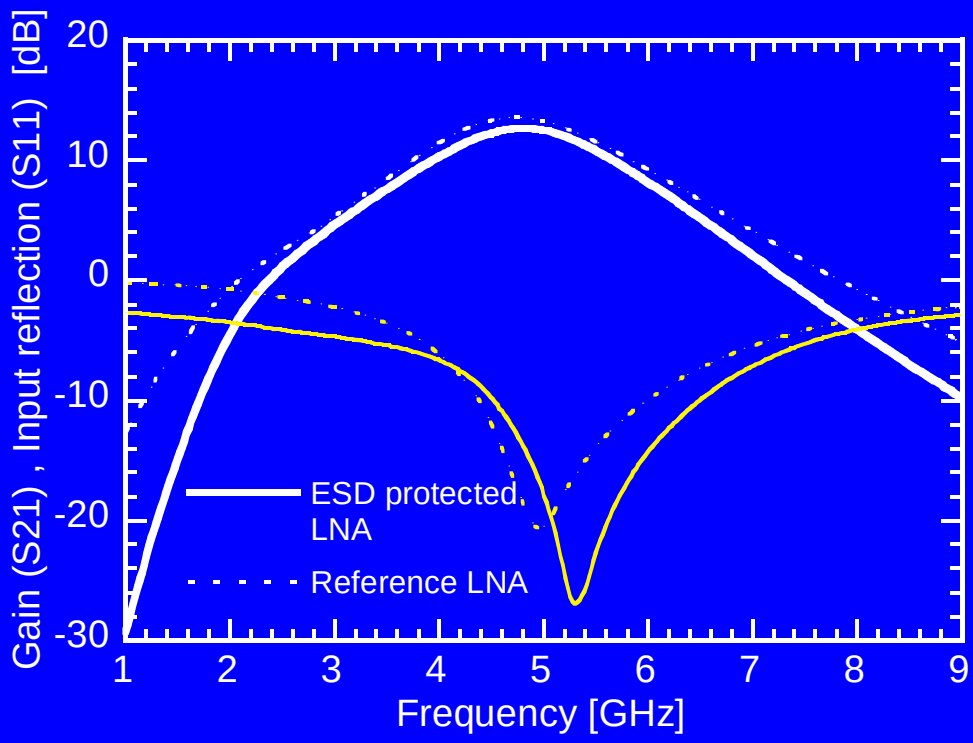
Inductor protection with Power Clamp

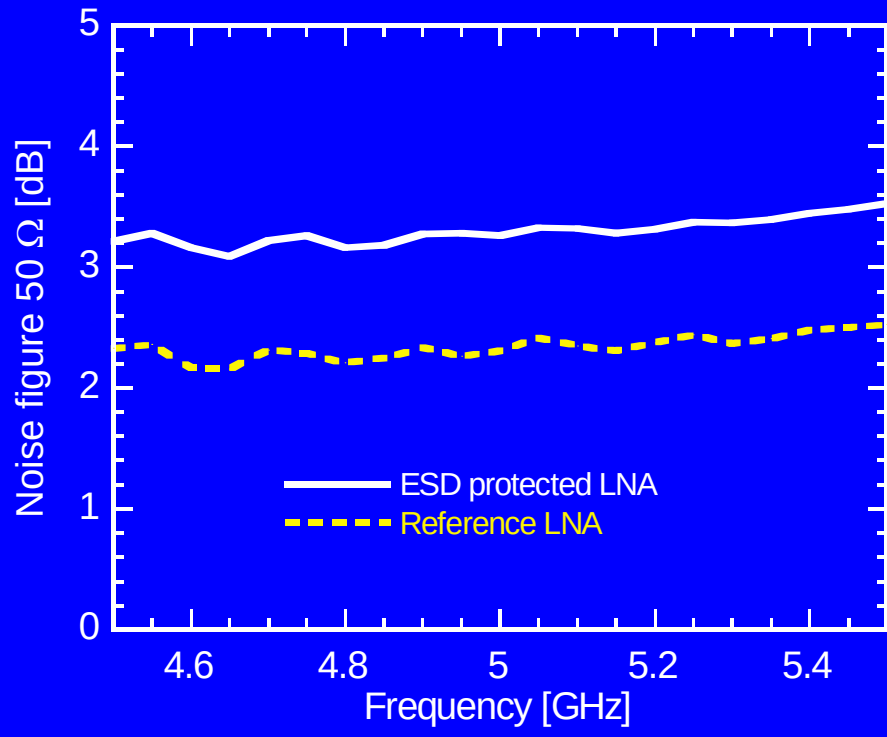




Inductor protection with Power Clamp

- **Measurement results**





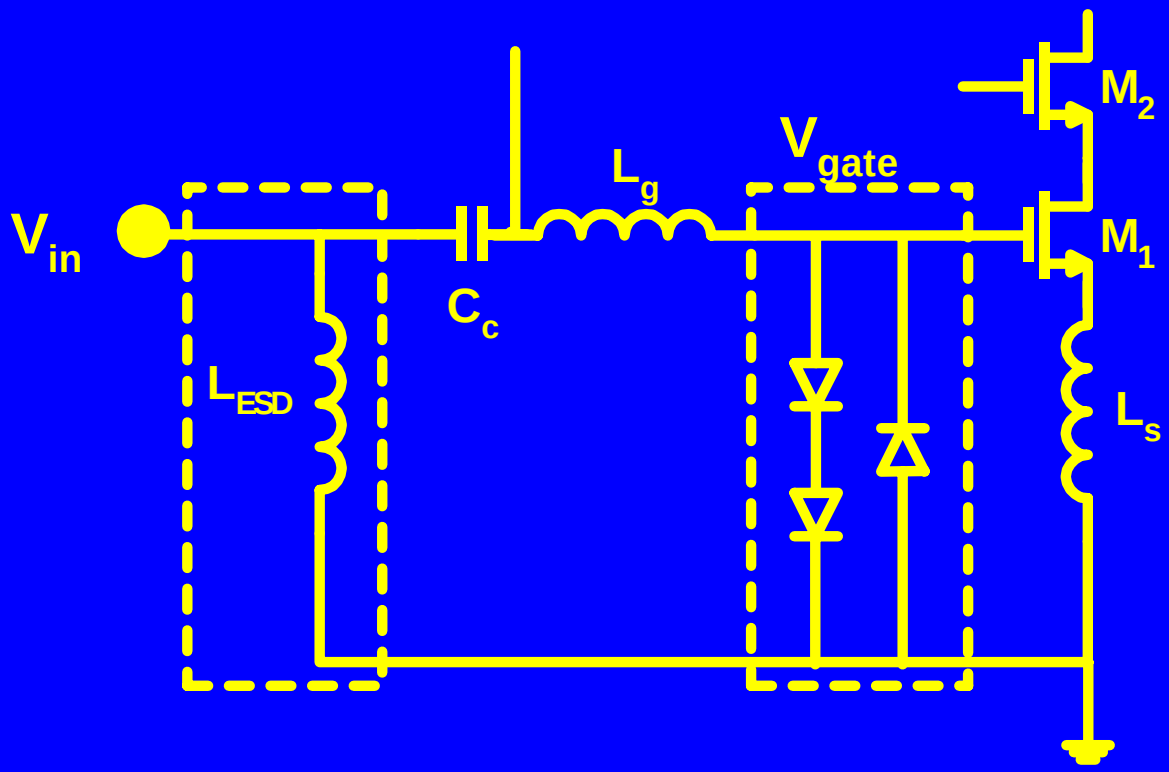
Inductor protection with Power Clamp

Gate over-voltage protection

- Add a minimum size reverse diode at the gate to block negative over-voltage
- Add two minimum size forward diodes at the gate, biased at 0.6V to block positive over-voltage

These diodes are placed right in front of the gate

Inductor protection with Power Clamp



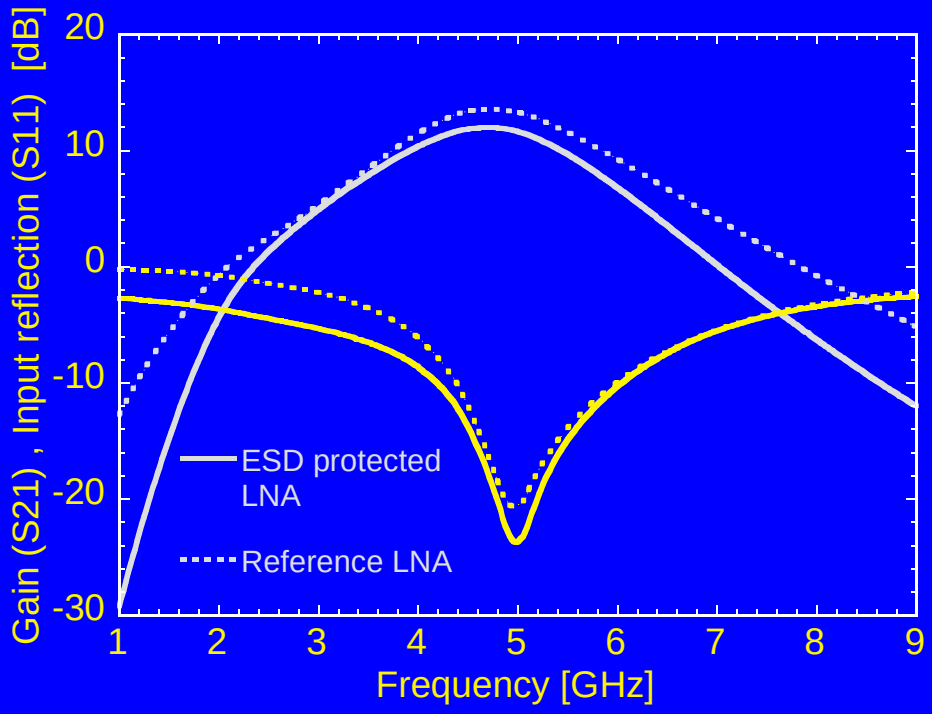
Schematic with additional diodes to clamp the voltage at M1

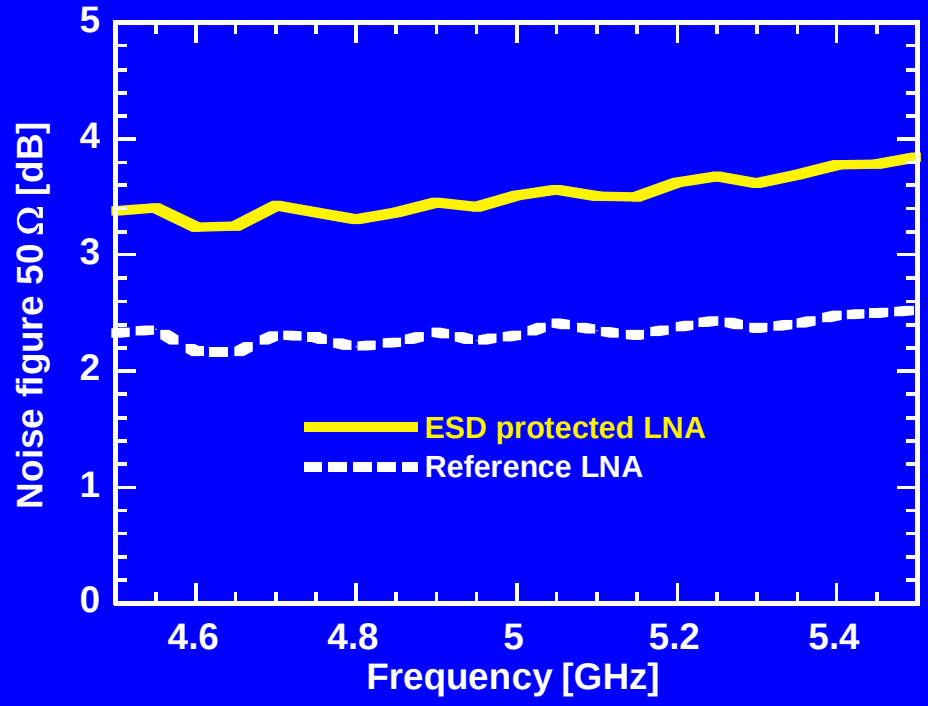
Inductor protection with Power Clamp

Circuit	LNA no ESD	ESD-LNA w/o diodes	ESD-LNA with diodes
Vdd [Volt]	1.2	1.2	1.2
Current [mA]	7.5	7.5	7.5
Gain [dB]	13.5	12.6	12
S11 [dB]	-21	-18	-24
S22 [dB]	-11	-14	-14
S12 [dB]	-31	-32	-32
NF [dB]	2.2	3.2	3.4
1dB CP [dBm]	-11.5	-10.5	-9.6
IIP3 [dBm]	-1	-0.5	0.4
TLP [A]	-	2.2	4
HBM [kV]	0.009	2.5	5.5
MM [V]	-	225	350

Inductor protection with Power Clamp

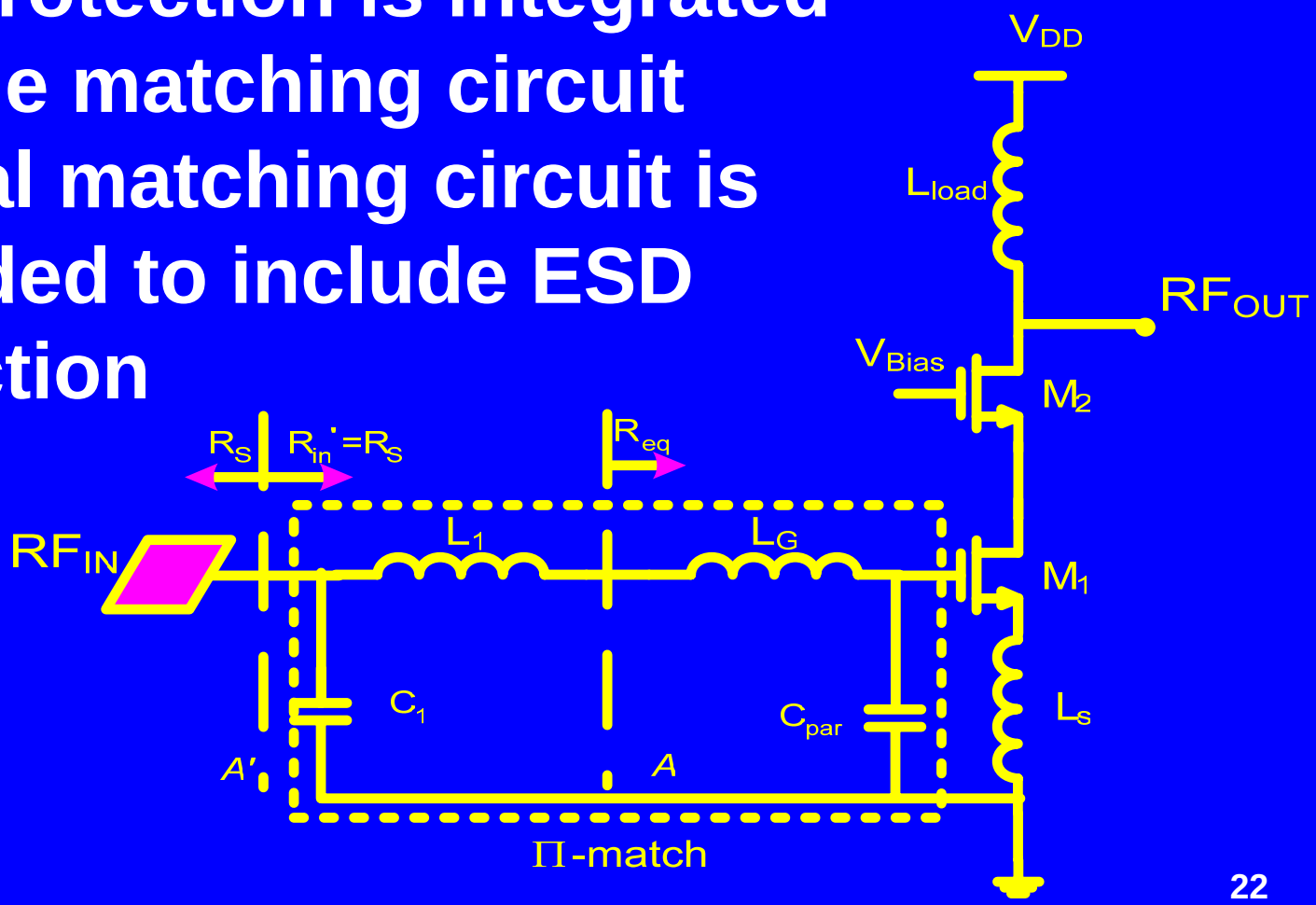
- **Measurement results**



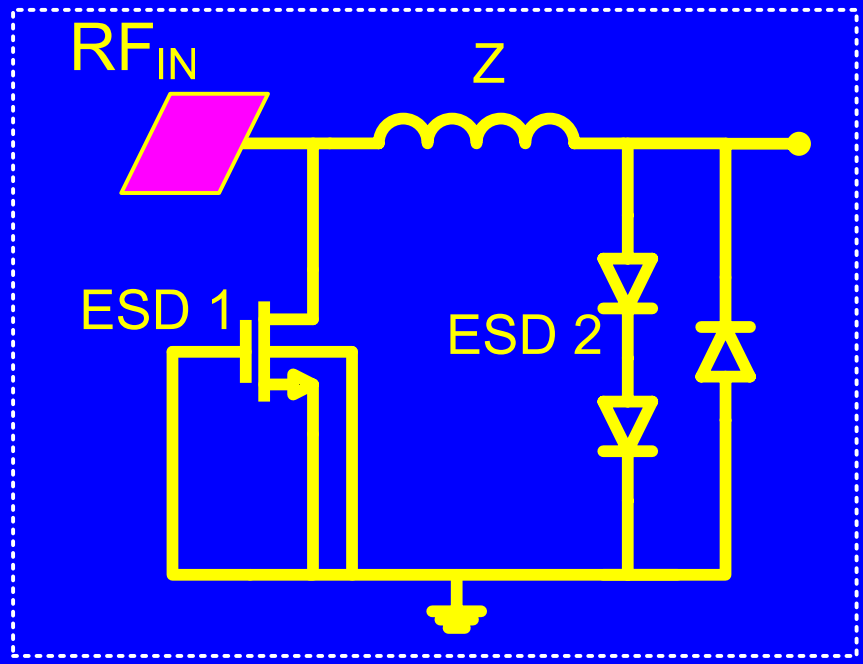


Full circuit – ESD co-design

- ESD protection is integrated into the matching circuit
- Typical matching circuit is extended to include ESD protection



Full circuit – ESD co-design



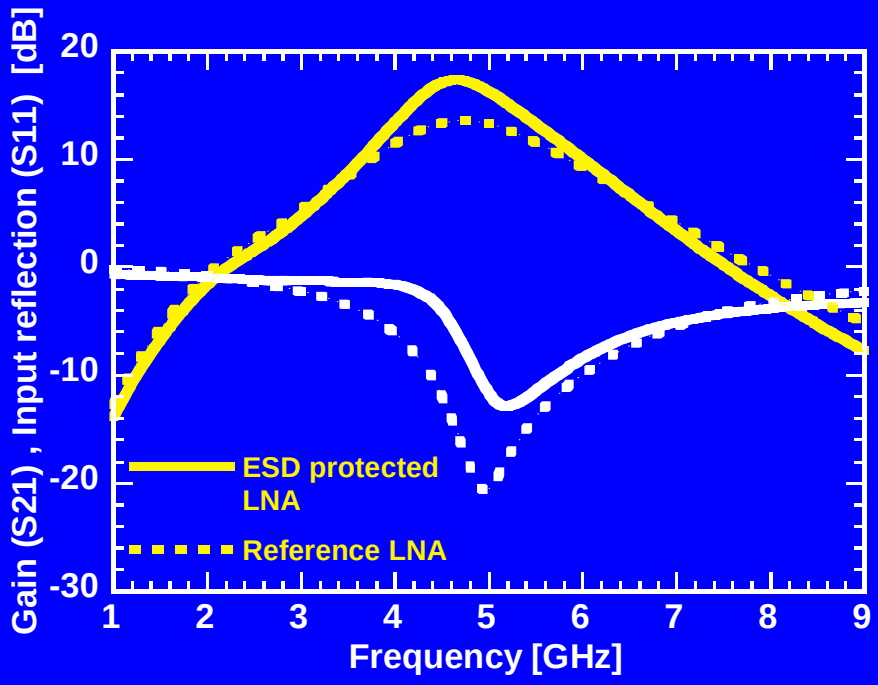
Schematic including the ESD protection into the matching circuit

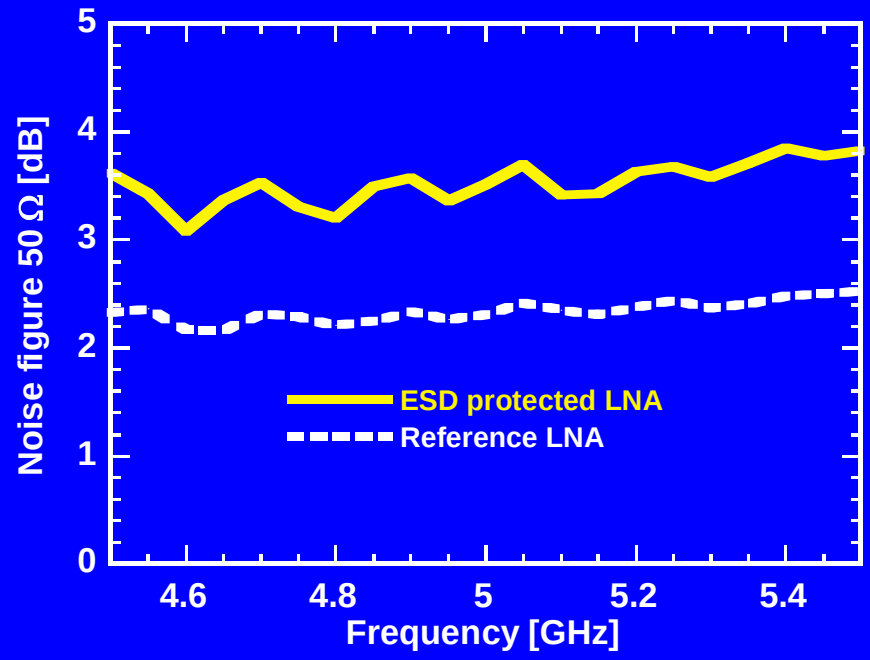
Full circuit – ESD co-design

Circuit	LNA no ESD	ESD-LNA Co-design
Vdd [Volt]	1.2	1.2
Current [mA]	7.5	7.5
Gain [dB]	13.5	16.2
S11 [dB]	-21	-11.5
S22 [dB]	-11	-8
S12 [dB]	-31	-25.4
NF [dB]	2.2	3.5
1dB CP [dBm]	-11.5	-15.4
IIP3 [dBm]	-1	-5
HBM [kV]	0.009	1.9

Full circuit – ESD co-design

- **Measurement results**





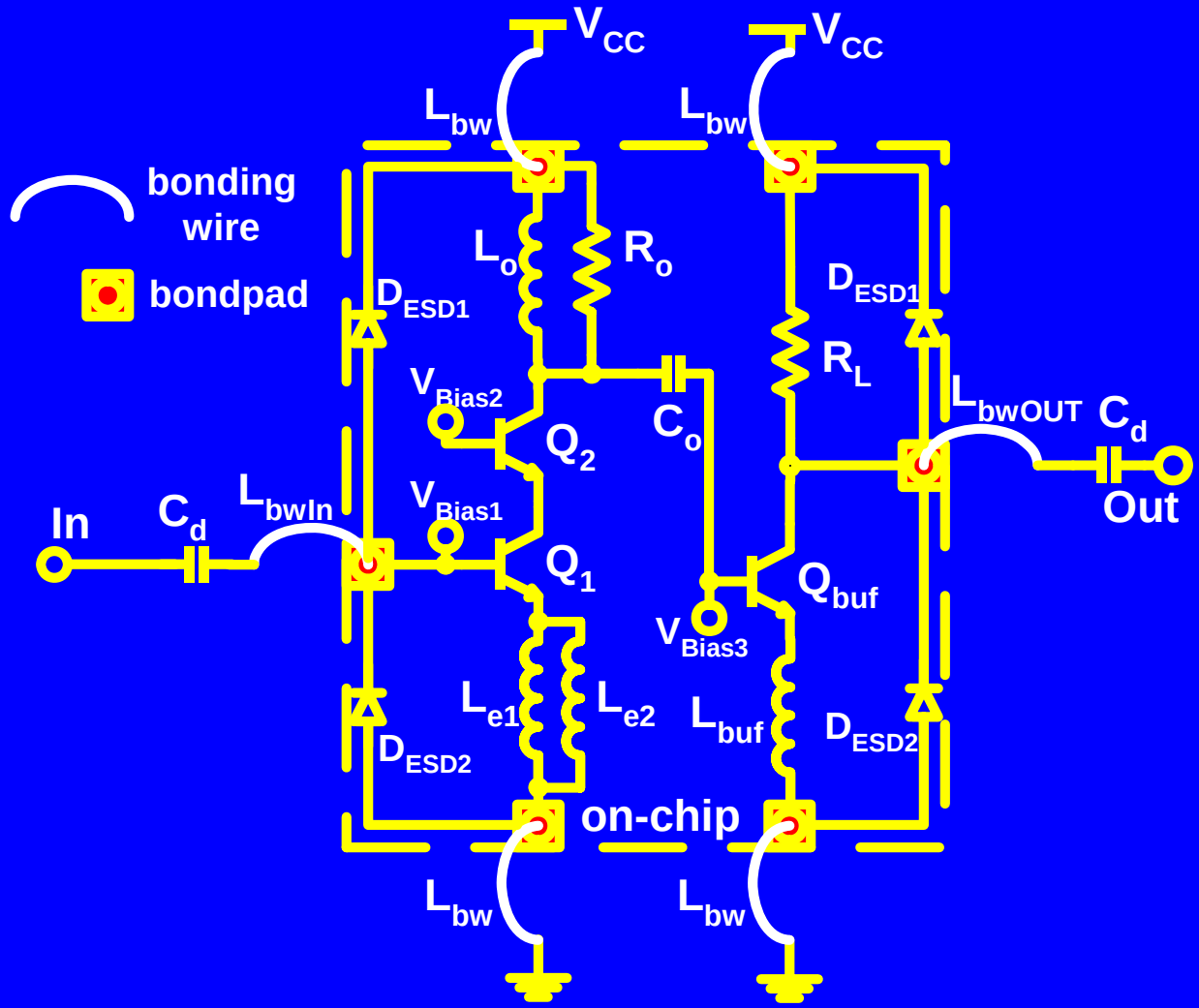
Partial circuit – ESD co-design

- Determine parasitic loading due to the ESD protection and other parasitics
- Take this value into account for input/output matching

Opposite to previous methods

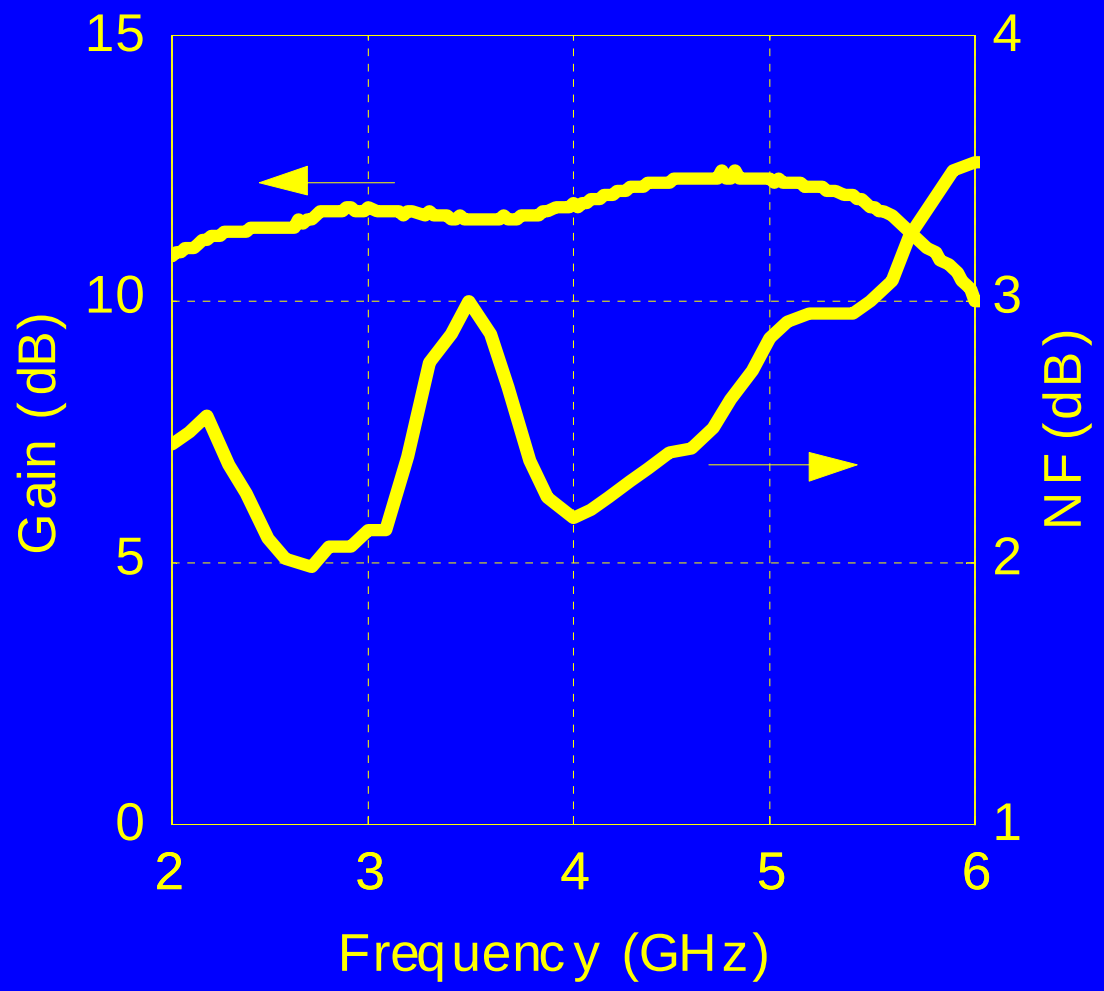
- Determine ESD robustness
- Optimize LNA for this robustness

Partial circuit – ESD co-design



Partial circuit – ESD co-design

- **Measurement results for an ultra wideband LNA in 0.35μm BiCMOS technology**



Conclusions

- Comparison of 4 RF ESD protection strategies with respect to their respective performance trade-offs
- Discussion of the limiting factors and proposal of solutions for further improvement
- Review of the performance parameters for 90nm CMOS LNA's at 5 GHz

Conclusions

Circuit	LNA	LNA diodes	ESD-LNA inductor w/o diodes	ESD-LNA inductor with diodes	ESD-LNA co-design
Vdd [V]	1.2	1.2	1.2	1.2	1.2
Current [mA]	7.5	7.5	7.5	7.5	7.5
Gain [dB]	13.5	13	12.6	12	16.2
S11 [dB]	-21	-18	-18	-24	-11.5
S22 [dB]	-11	-14.5	-14	-14	-8
S12 [dB]	-31	-30	-32	-32	-25.4
NF [dB]	2.2	3	3.2	3.4	3.5
1dB CP [dBm]	-11.5	-10.6	-10.5	-9.6	-15.4
IIP3 [dBm]	-1	-0.4	-0.5	0.4	-5
TLP [A]	-	-	2.2	4	-
HBM [kV]	0.009	0.5	2.5	5.5	1.9
MM [V]	-	-	225	350	-