Future Directions in Mixed-Signal IC Design

December 12, 2008

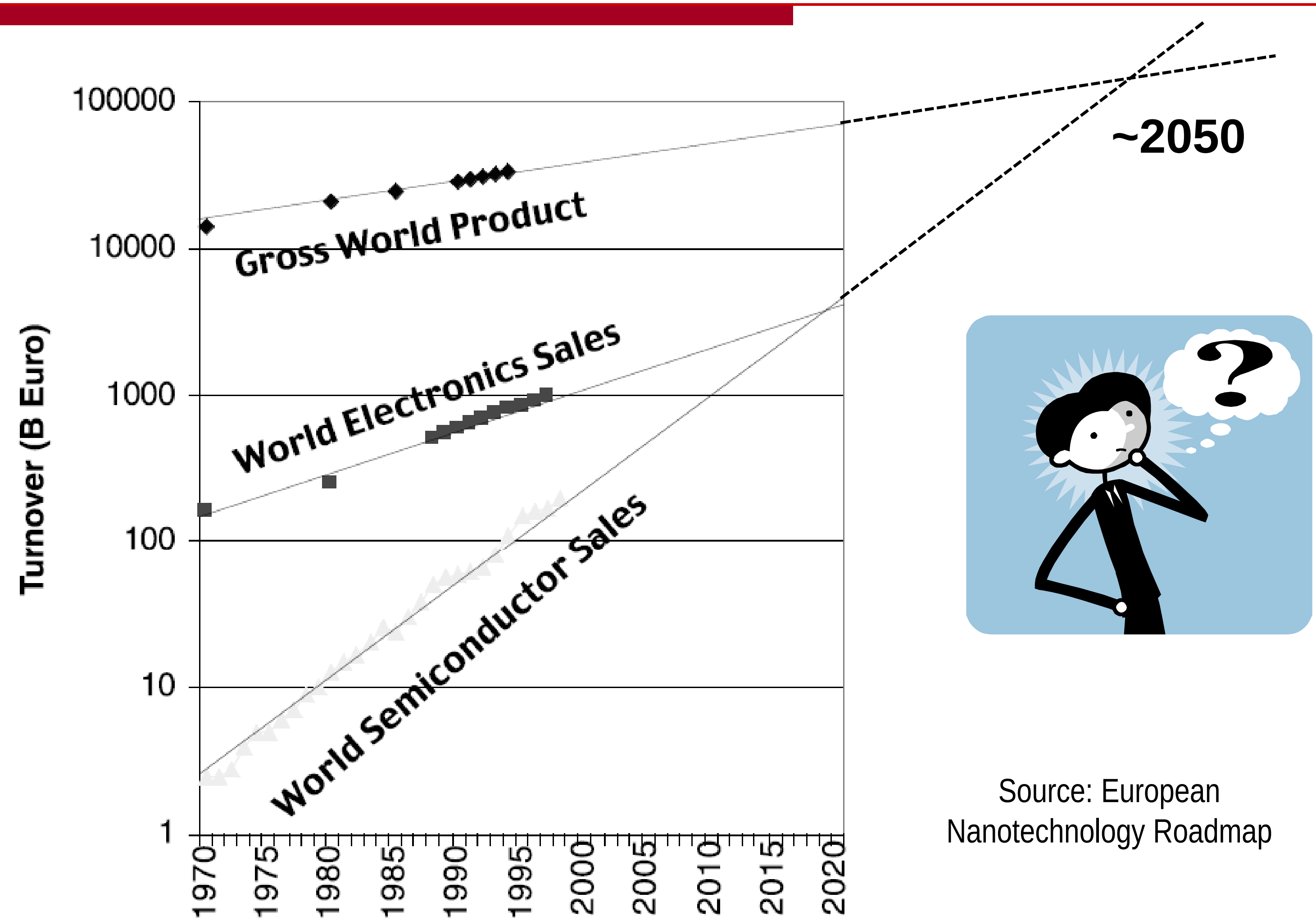
Boris Murmann

murmann@stanford.edu

Murmann Mixed-Signal Group

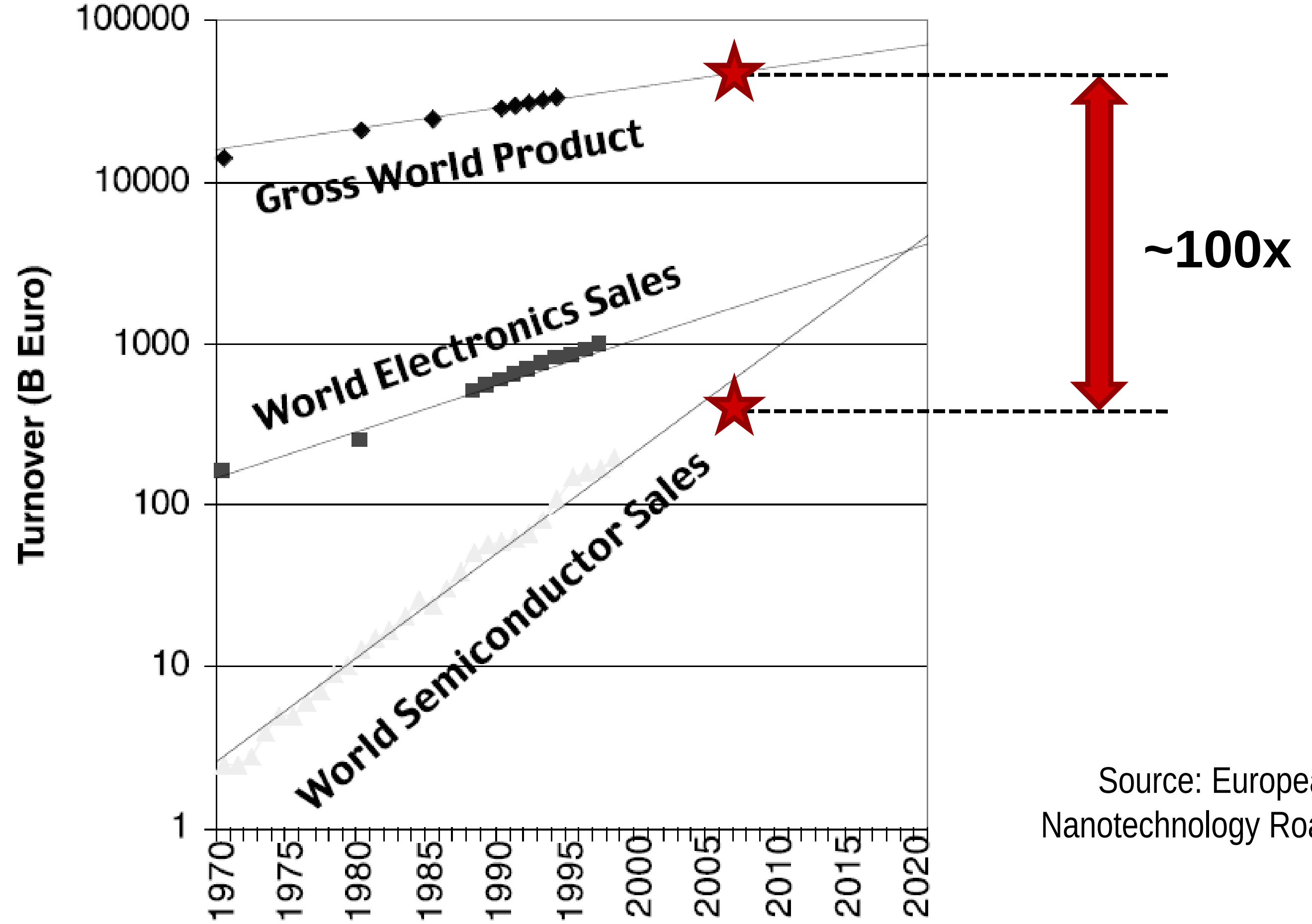
STANFORD ELECTRICAL ENGINEERING

Growth



Source: European Nanotechnology Roadmap

Business as Usual?

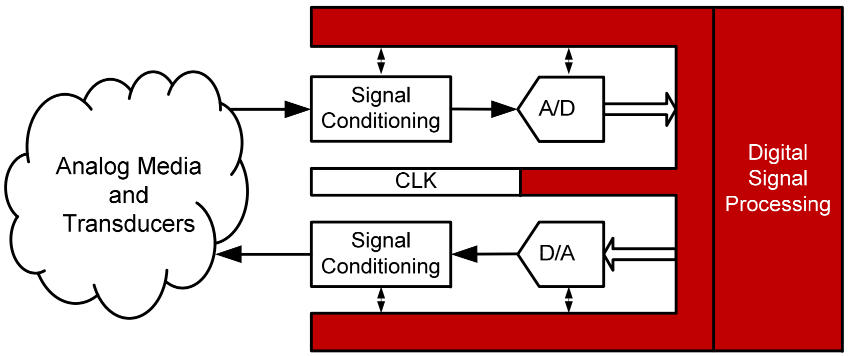


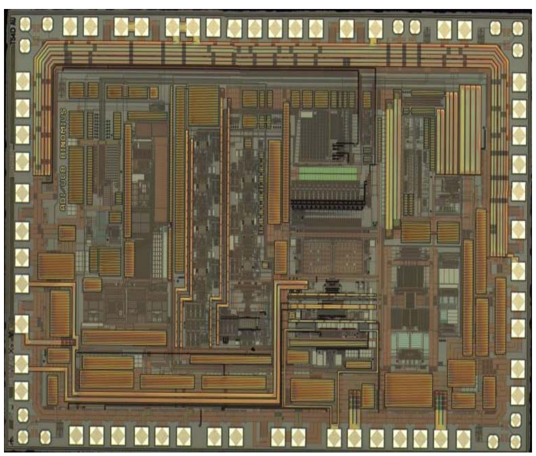
Source: European Nanotechnology Roadmap

Murmann Mixed-Signal Group

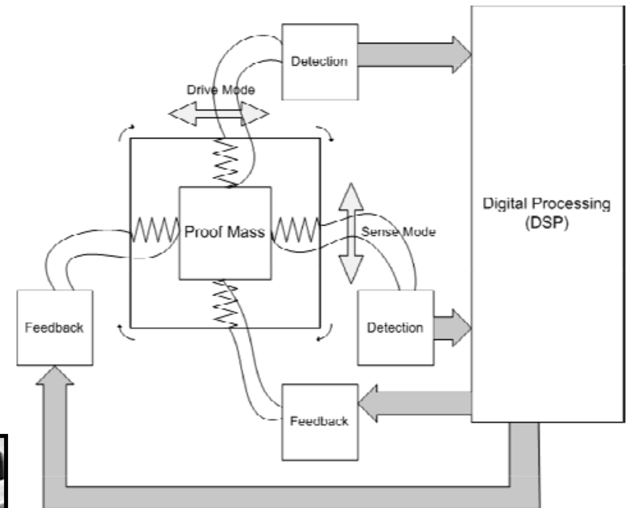
Research Overview (1)

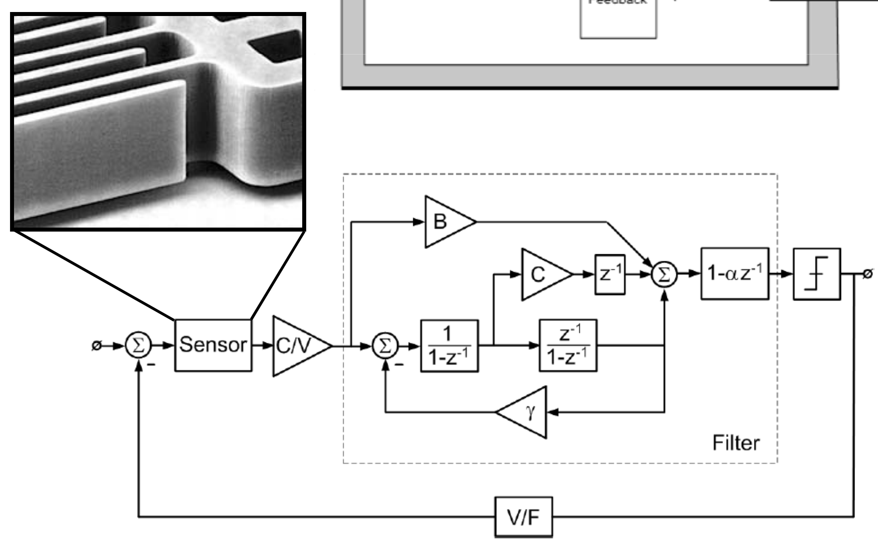
Digitally Assisted Data Converters



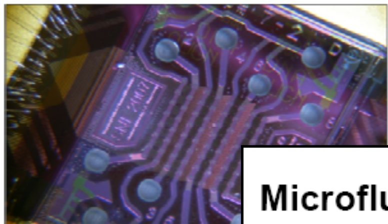


MEMS/Sensor Interface Electronics

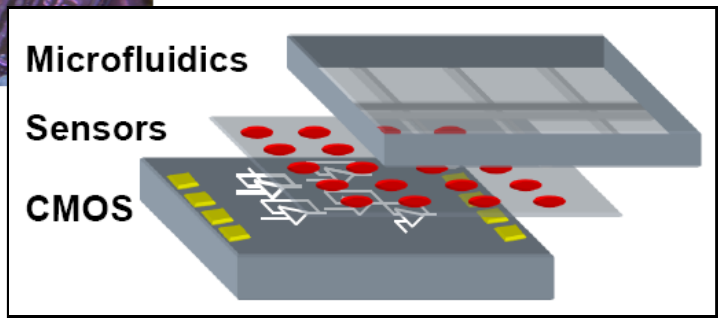


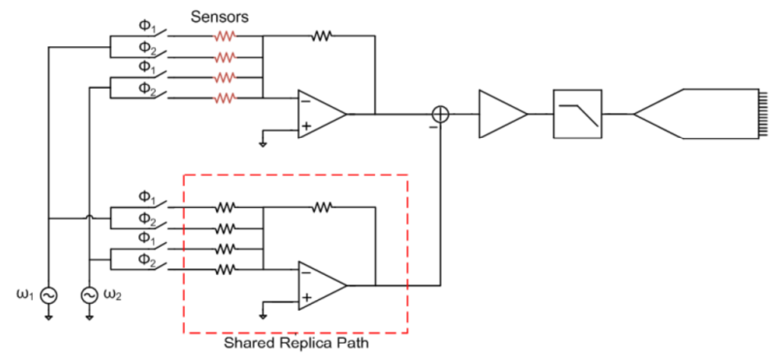


Research Overview (2)

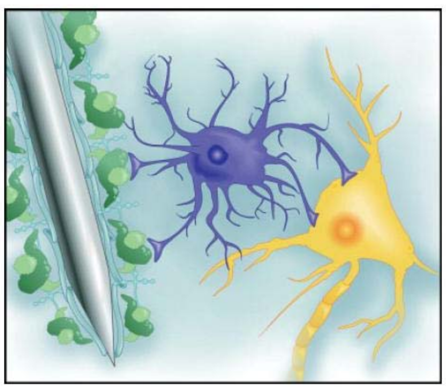


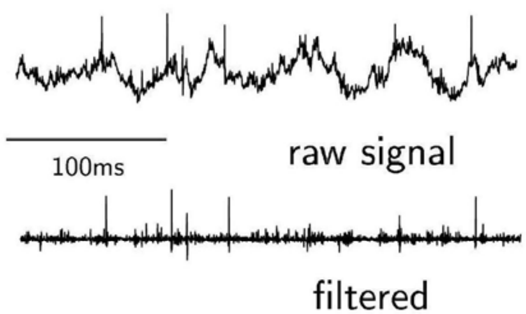
Bio-molecule detection

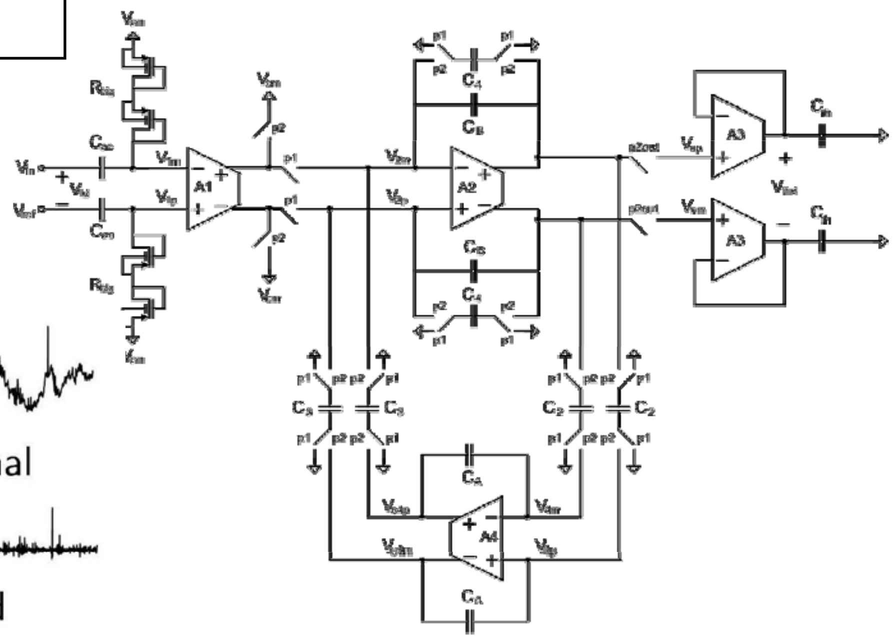




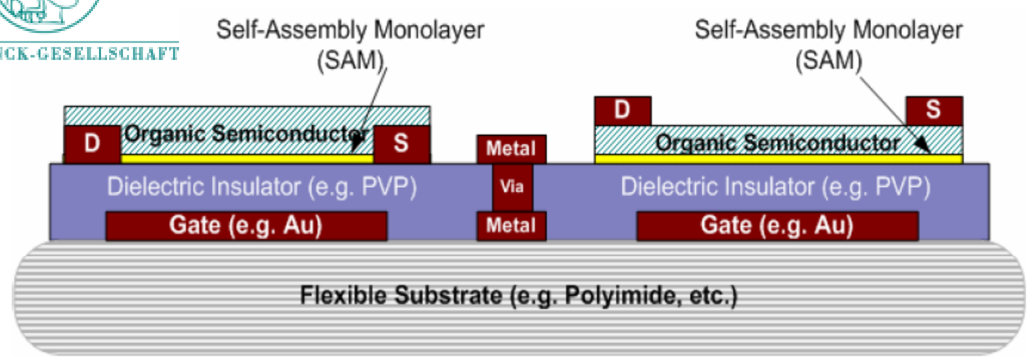
Neural signal acquisition

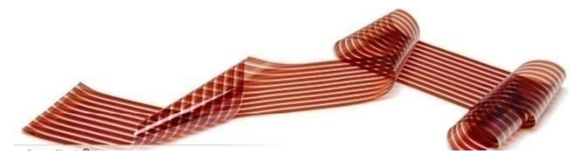


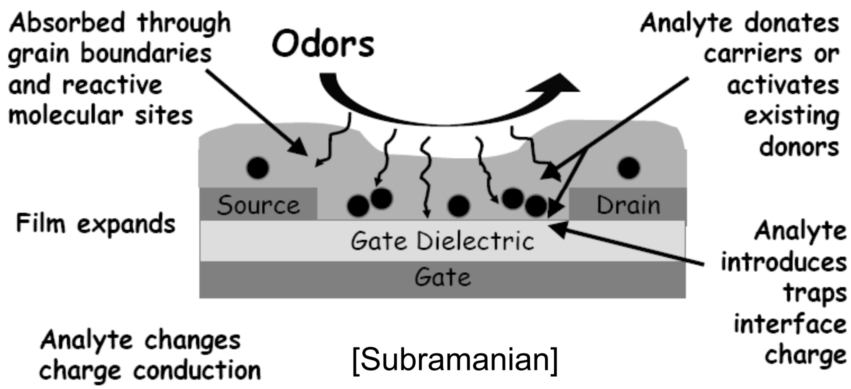




Research Overview (3)





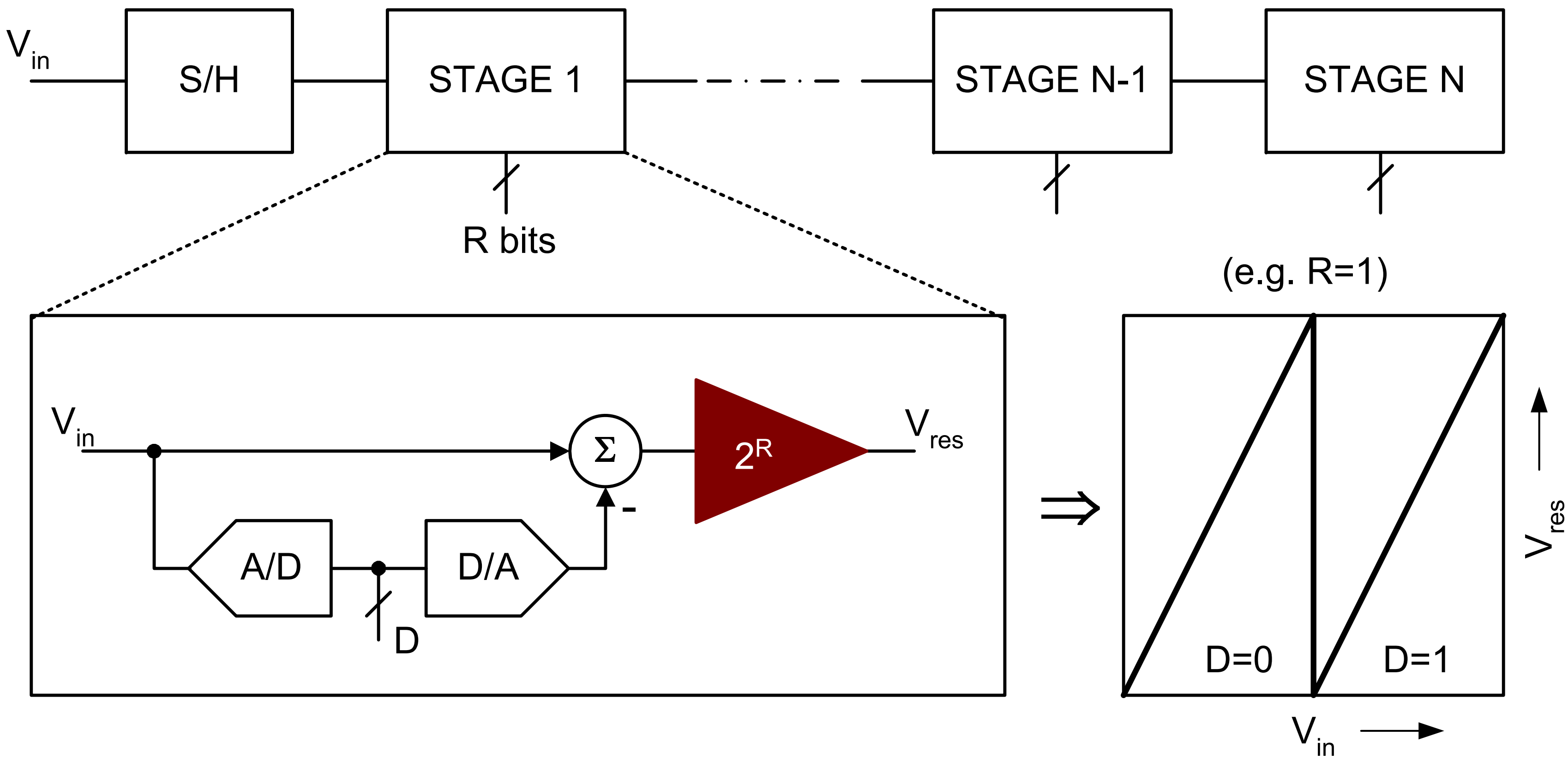


[Subramanian]

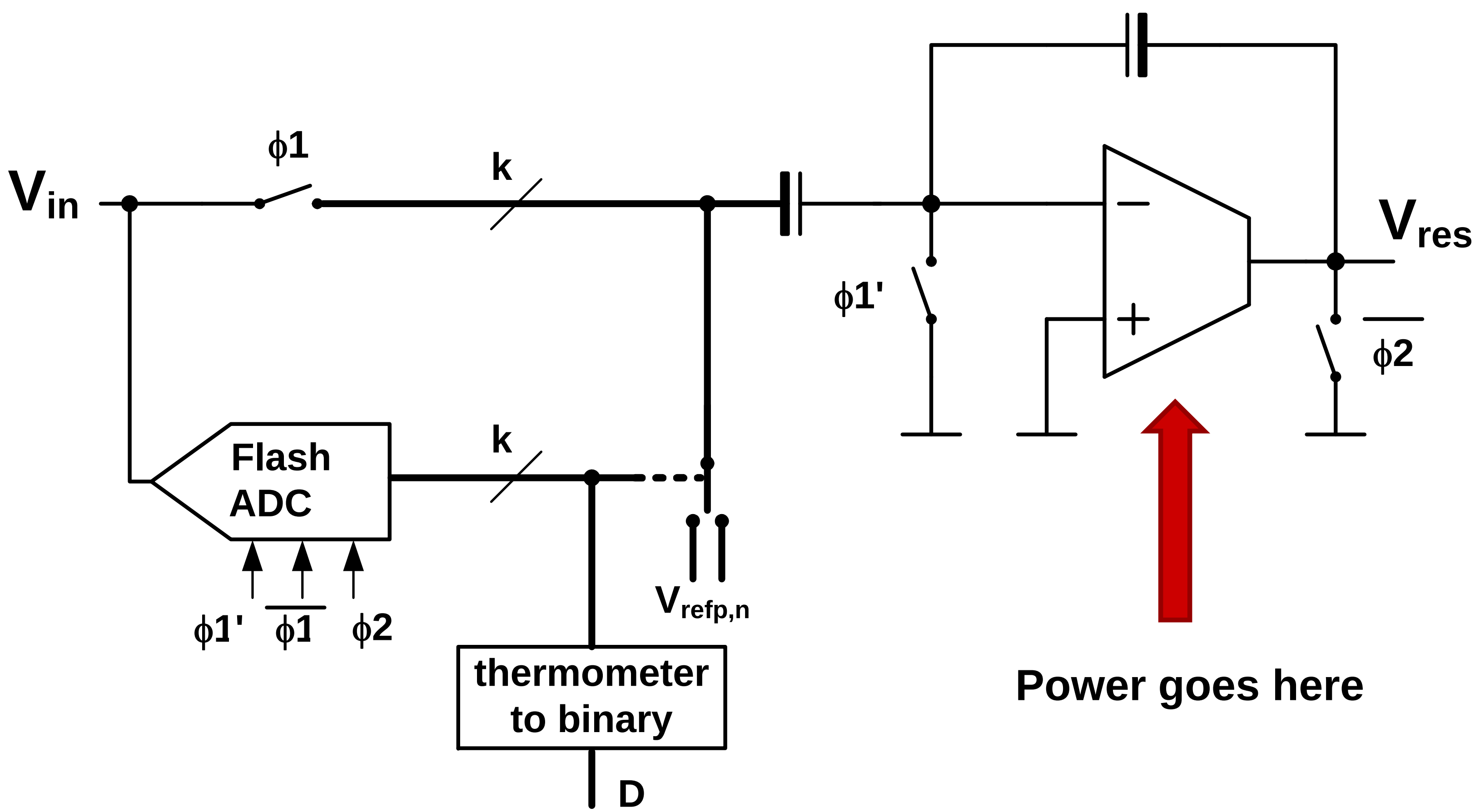
Specific Examples

- Minimalistic pipeline ADC
  - Using a previously “unknown” amplification mechanism
- Digitally corrected track-and-hold circuit
  - Analog-digital co-design
- Offset-calibrated accelerometer
  - Electro-mechanical co-design
- Analog circuit design using organic thin film transistors
  - Designing analog circuits using “lousy” technology

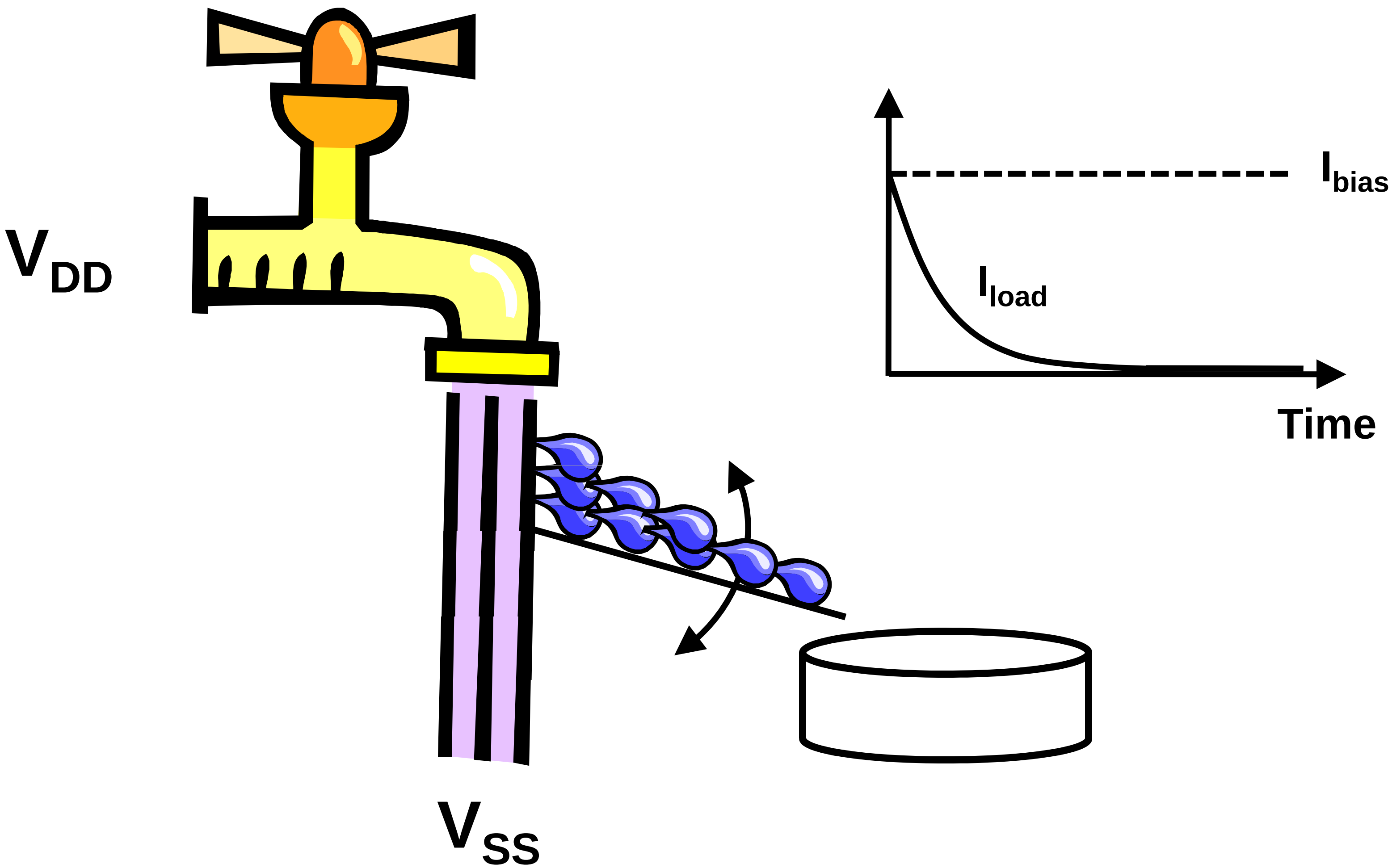
Pipeline ADC



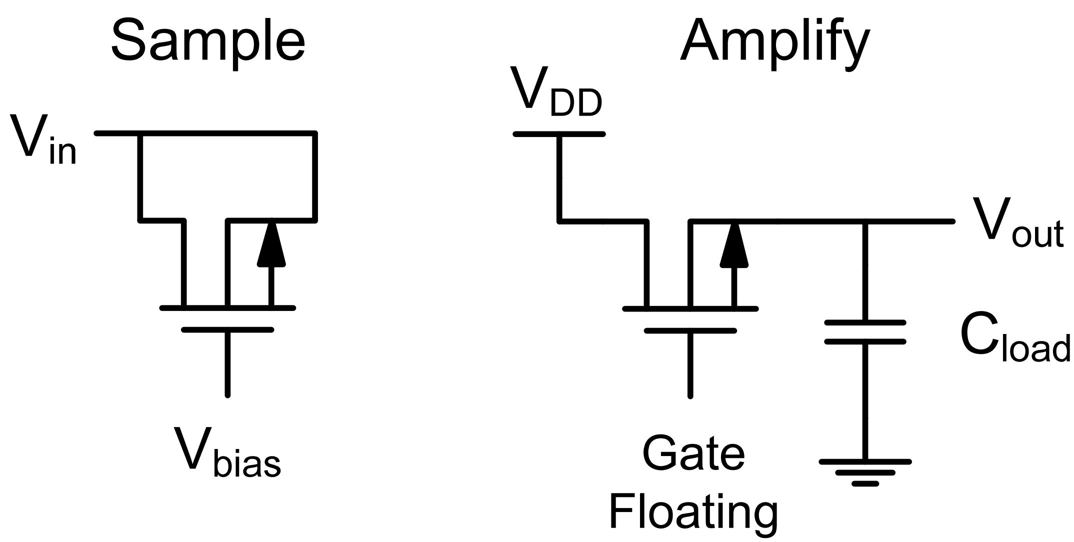
Stage of a Conventional Pipeline ADC



Inefficiency of Class-A Amplifiers

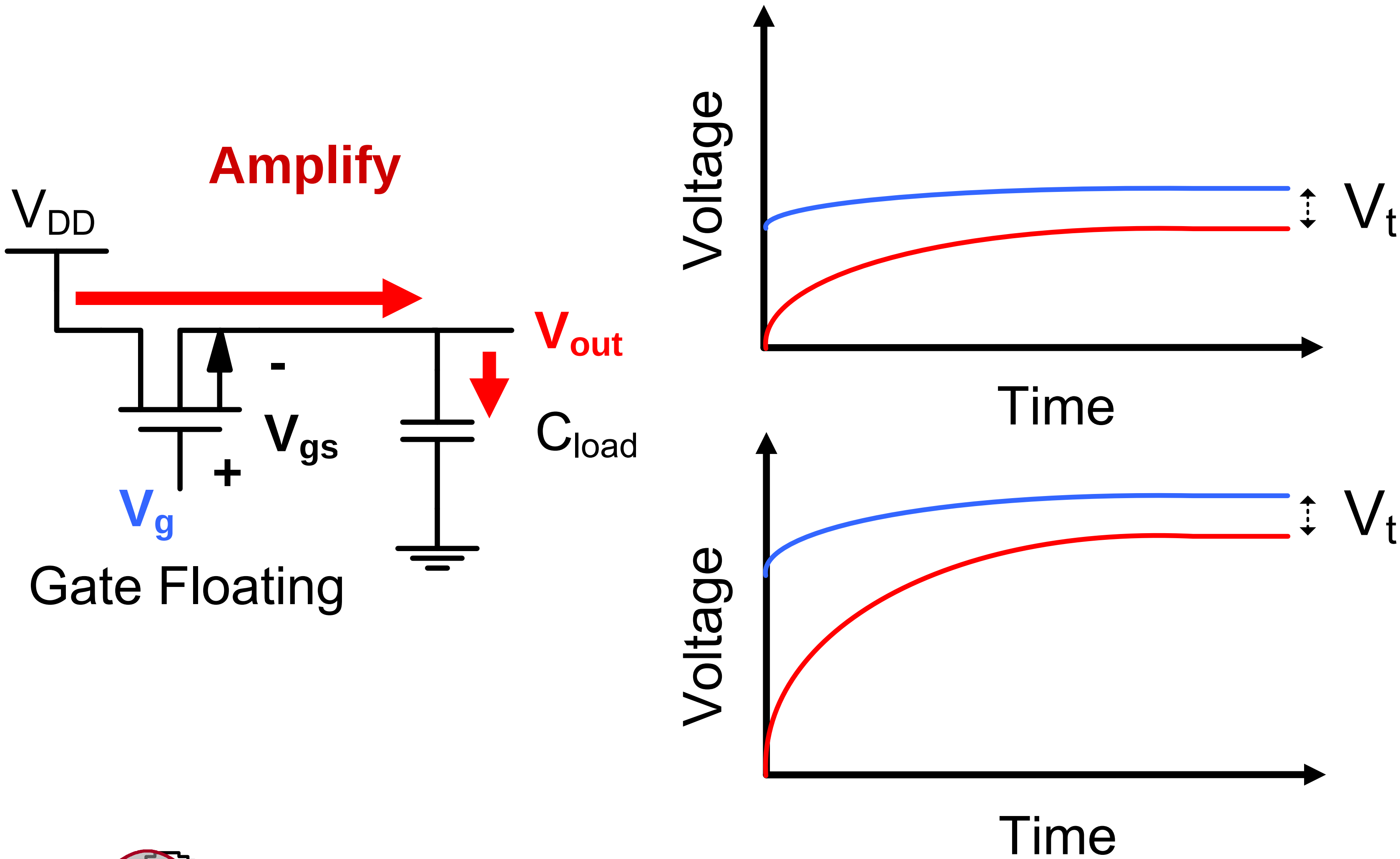


The World's Most Efficient SC Amplifier (?)

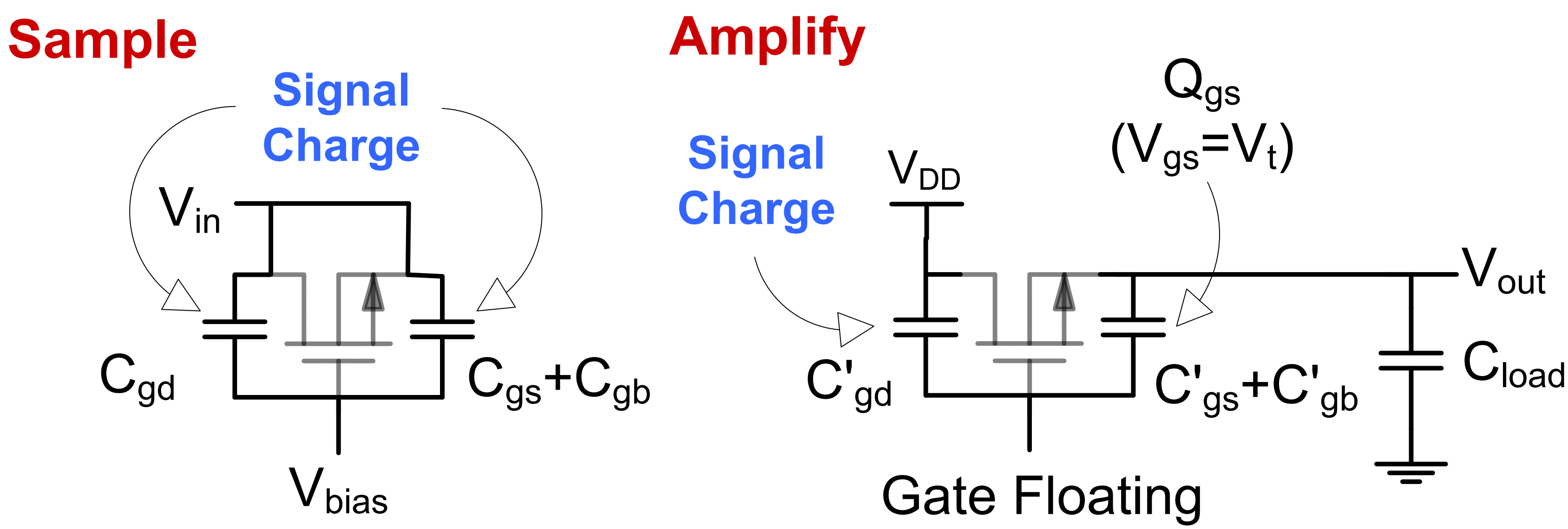


[Hu, Dolev & Murmann, VLSI Symposium 2008]

Settling in Amplify Phase



Amplification Principle



$$\text{Incremental Gain} \cong \frac{C_{gs} + C_{gd} + C_{gb}}{C'_{gd}}$$

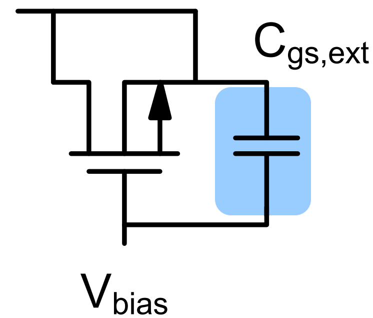
Basic Amplifier Modifications

- Add $C_{gs,ext}$ in parallel to C_{gs} for gain control

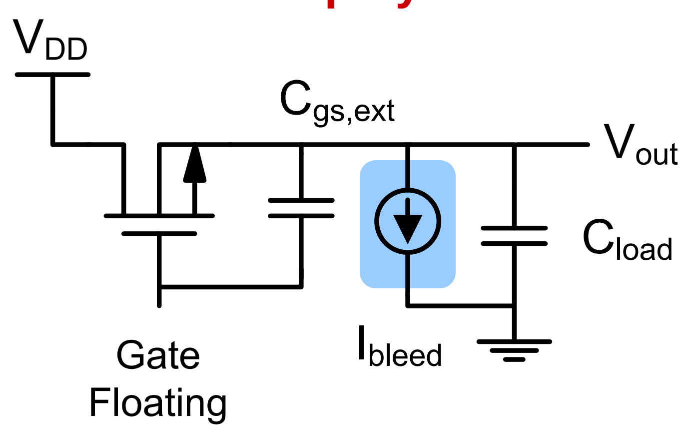
$$G = \frac{C_{gs,ext} + C_{gs} + C_{gd} + C_{gb}}{C'_{gd}}$$

- Add I_{bleed} during amplify phase

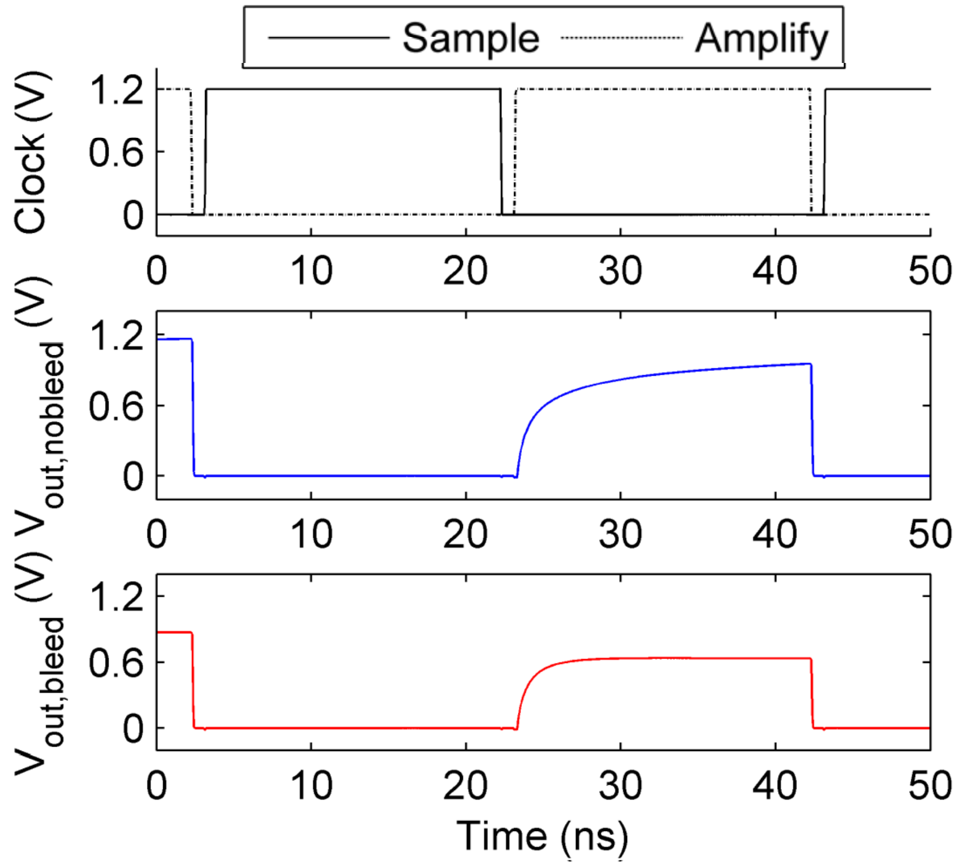
Sample



Amplify

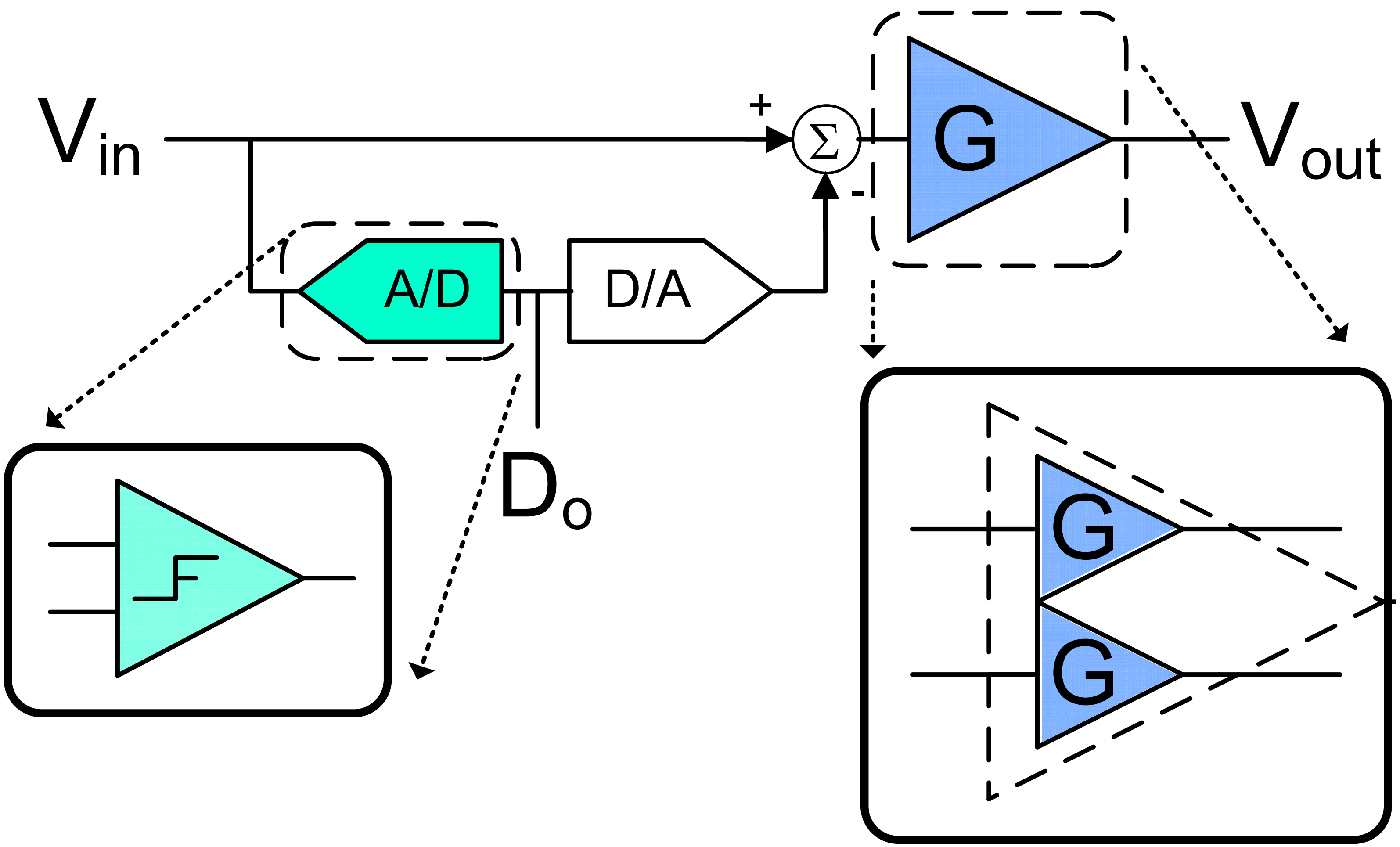


Impact of I_{bleed} (Simulation)

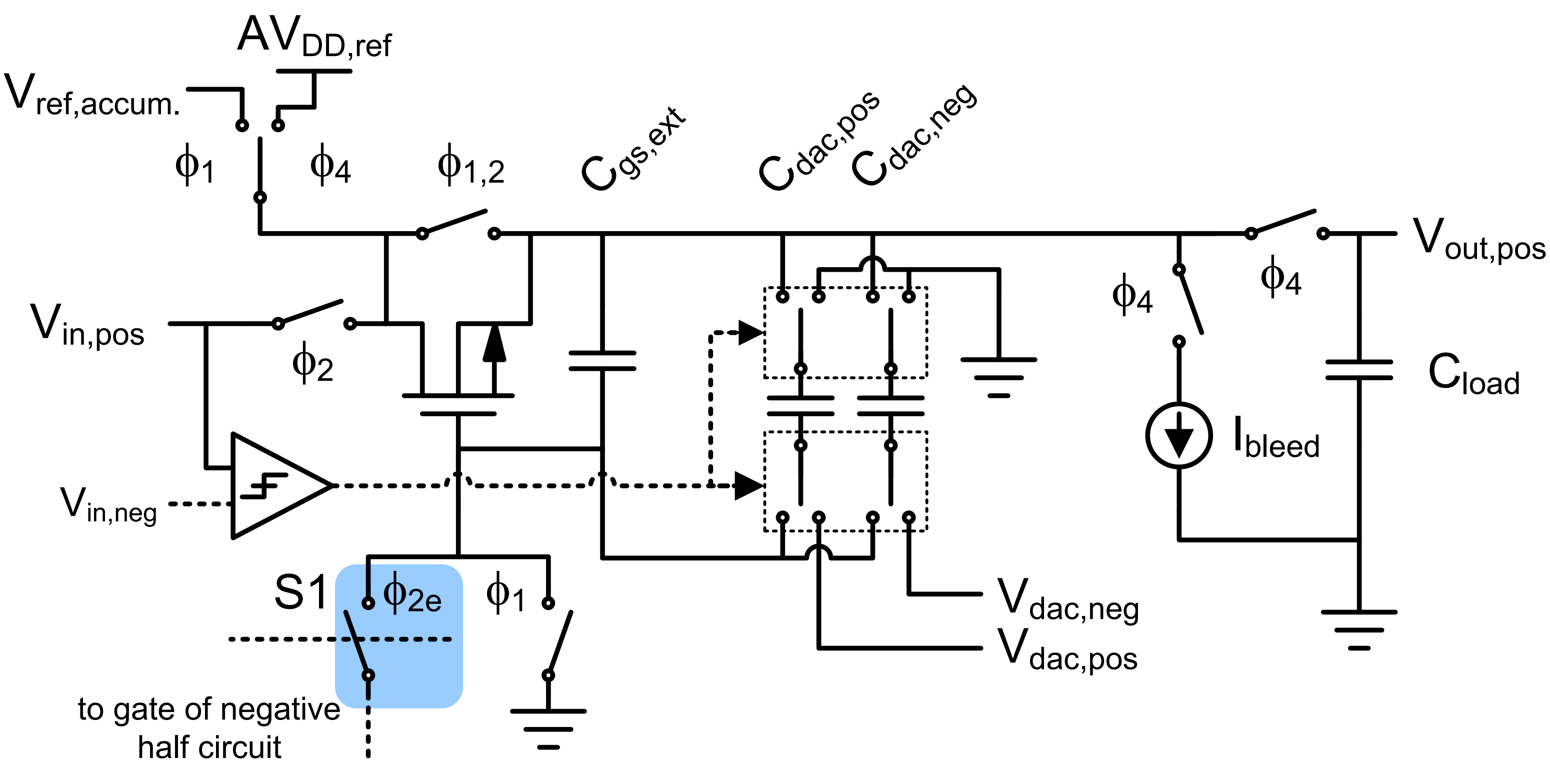


- Bleed current small, about 5μA

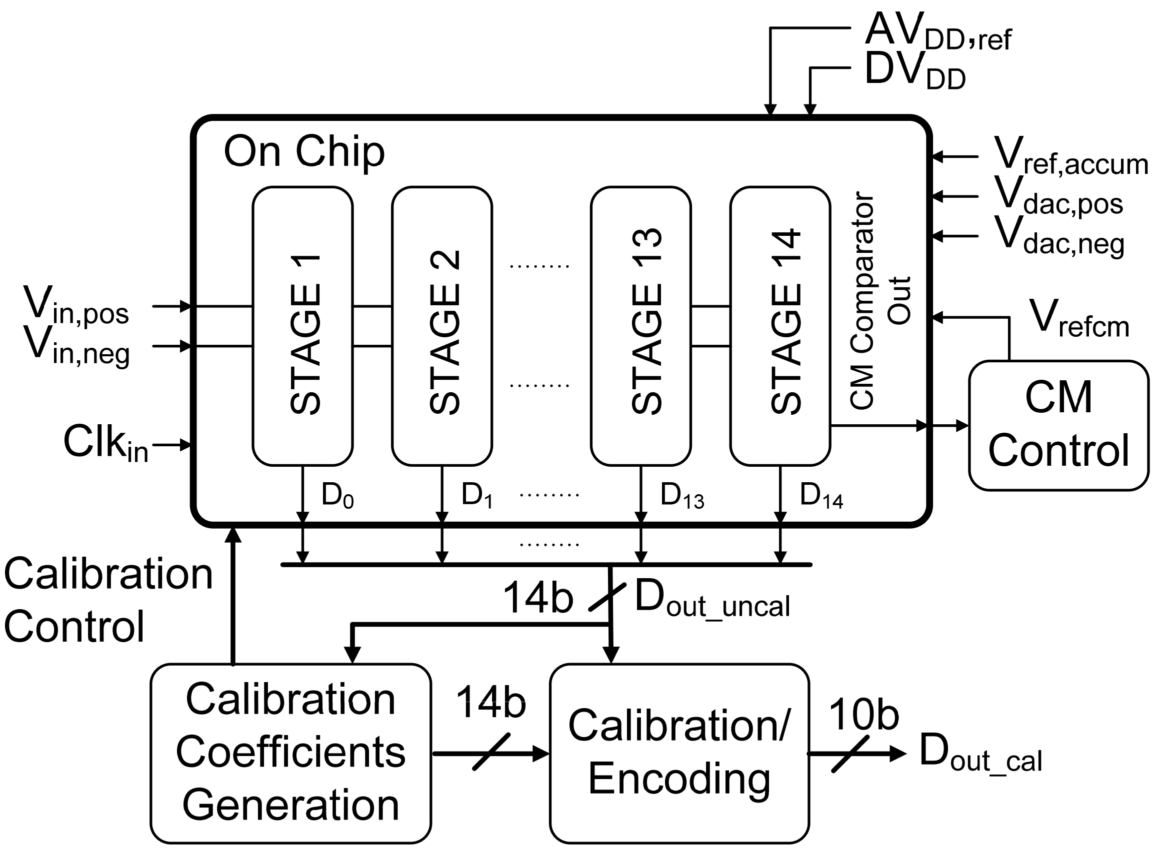
Pseudo-Differential Stage



Stage Schematic

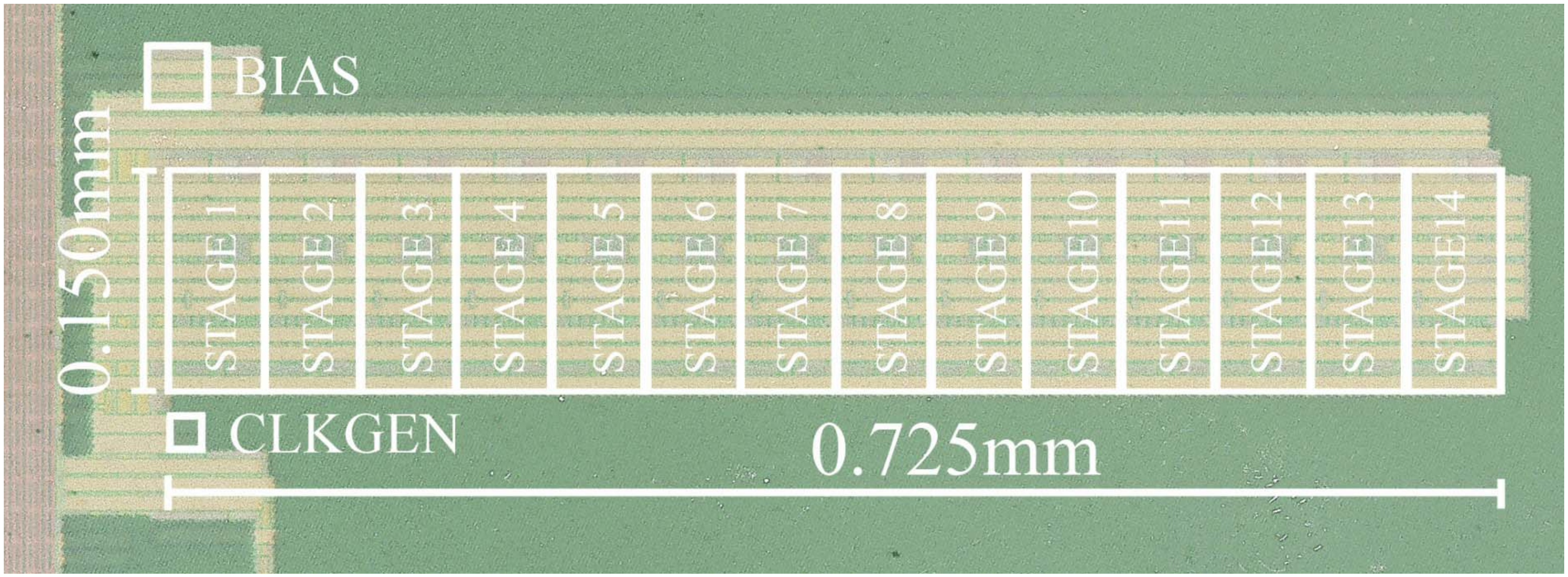


Testchip Architecture



- Target 8-9 bits of resolution
- 1-bit per stage
- Reduced radix (G=1.7) for offset tolerance
- Digital gain calibration [Karanicolas, 1993]
- 14 stages, no scaling
- Calibrated output encoded to 10 bits

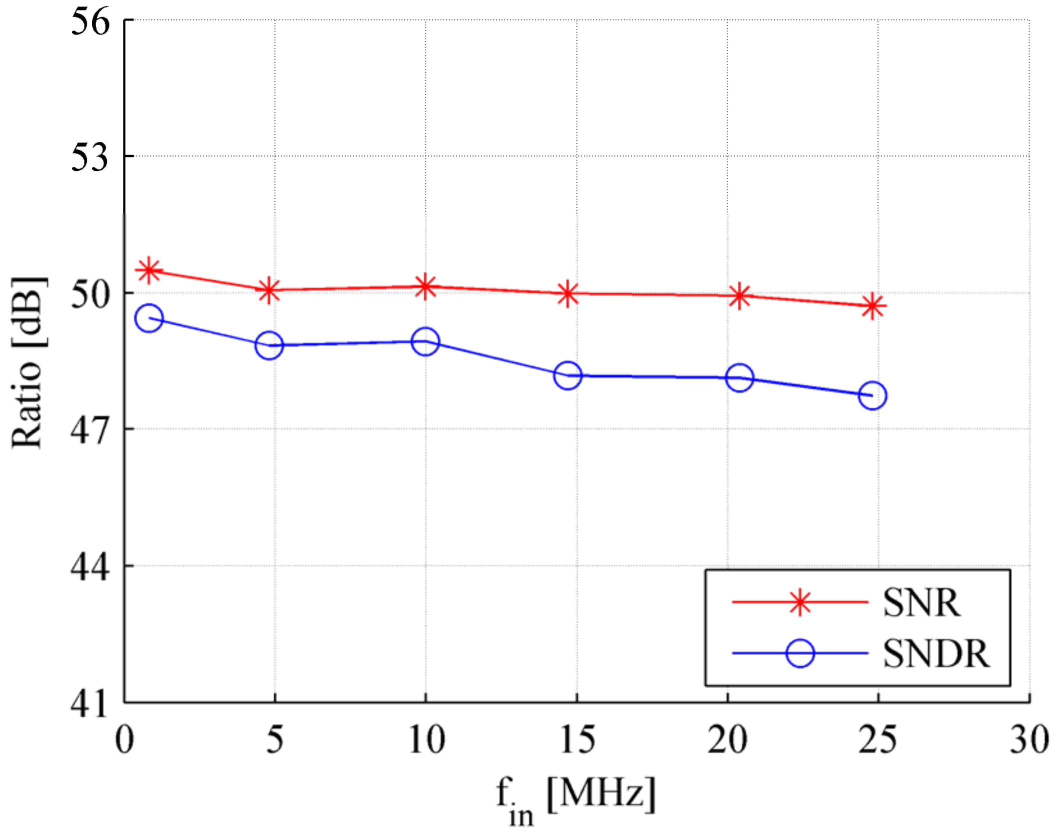
Prototype ADC



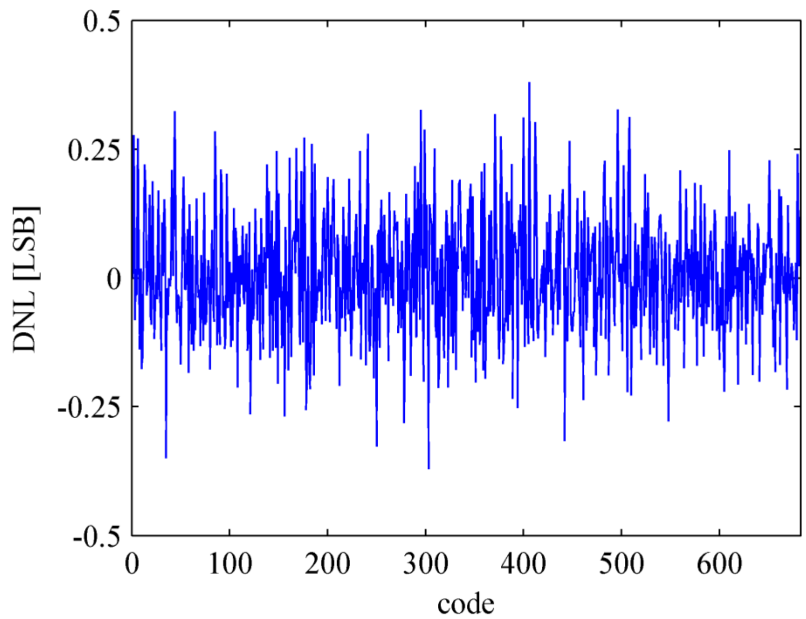
- UMC 90-nm CMOS process
- 0.123mm^2 (excluding off-chip reference generators)
- 9.4 bits (685 levels), f_s = 50MHz

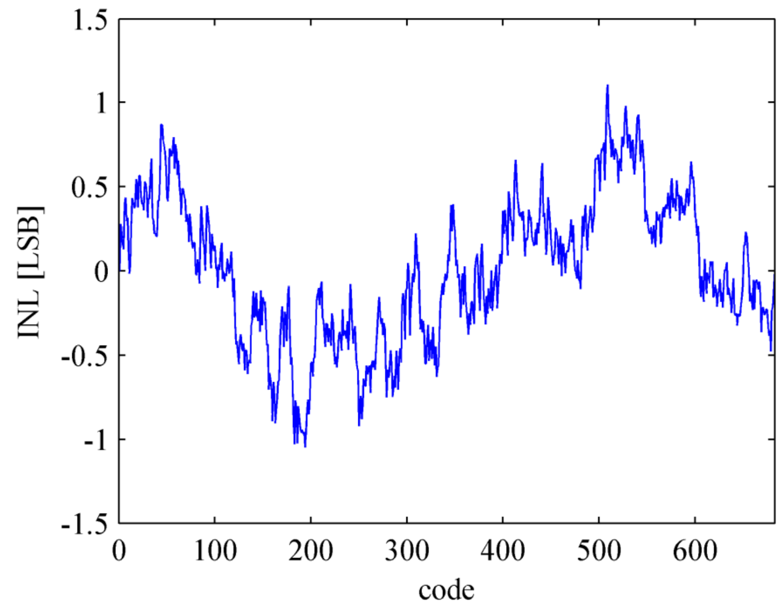
SNDR vs Input Frequency

- f_s = 50 MHz
- At low f_{in}
  - SNDR = 49.4 dB
  - ENOB = 7.9 bits
- SNDR degrades by 1.7 dB at high f_{in}



INL and DNL

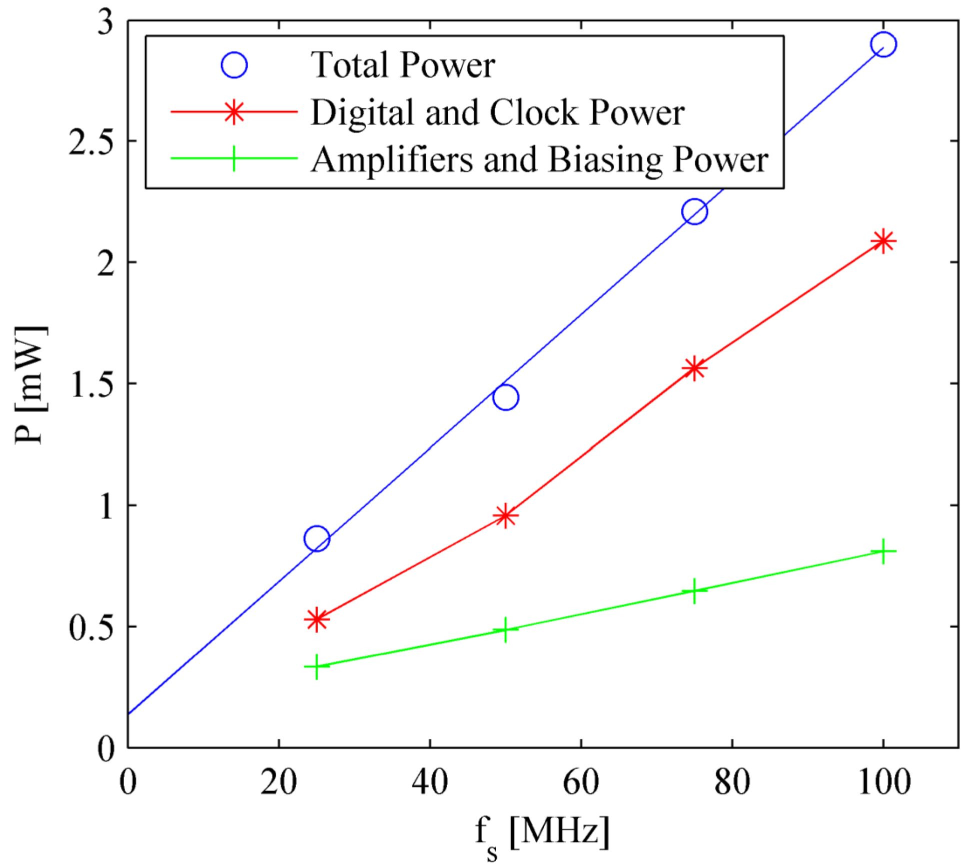




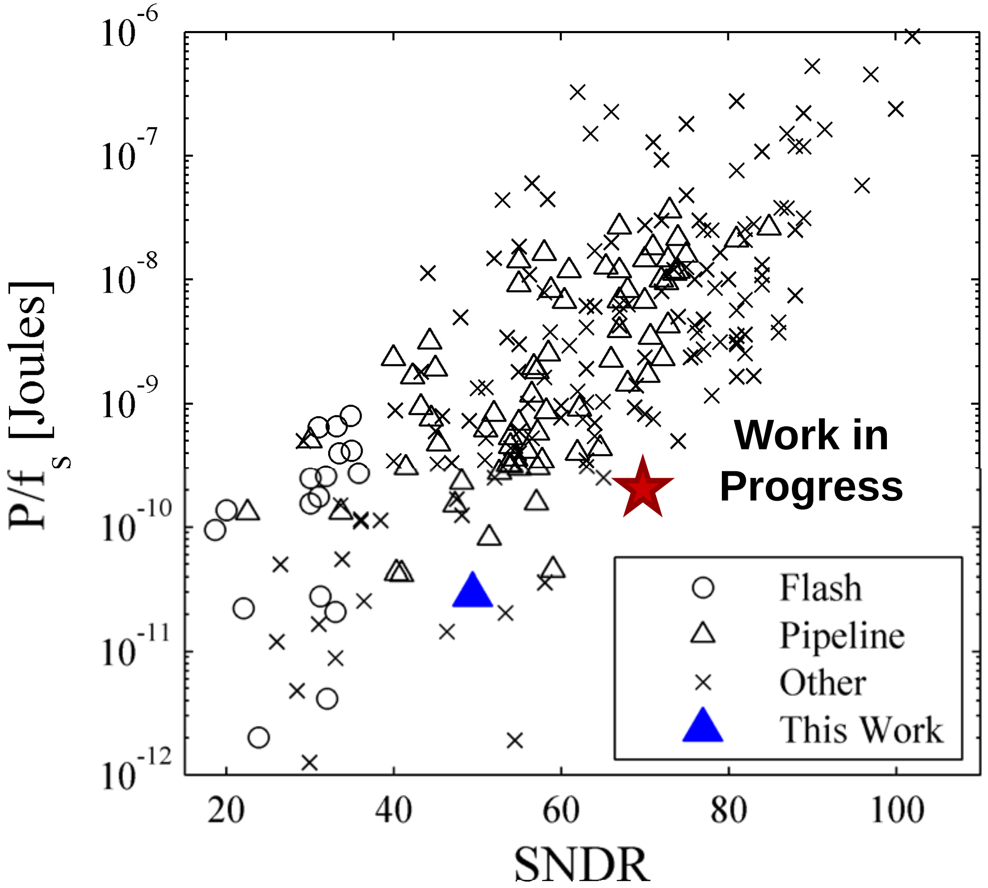
- 9.4 bit resolution (685 levels), f_s = 50 MHz
- DNL = +0.4/-0.4 LSB
- INL = +1.3/-0.9 LSB

Power

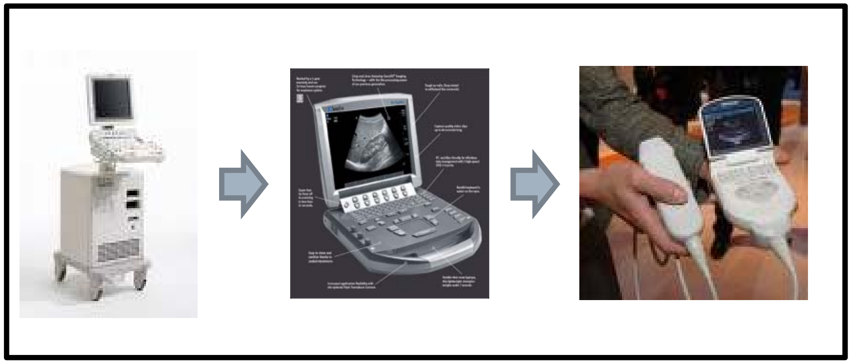
- 1.44 mW at f_s = 50 MHz
  - 0.49 mW amplifiers and biasing
  - 0.95 mW comparators and clocks
- At f_s = 50 MHz, only 9% of power is static

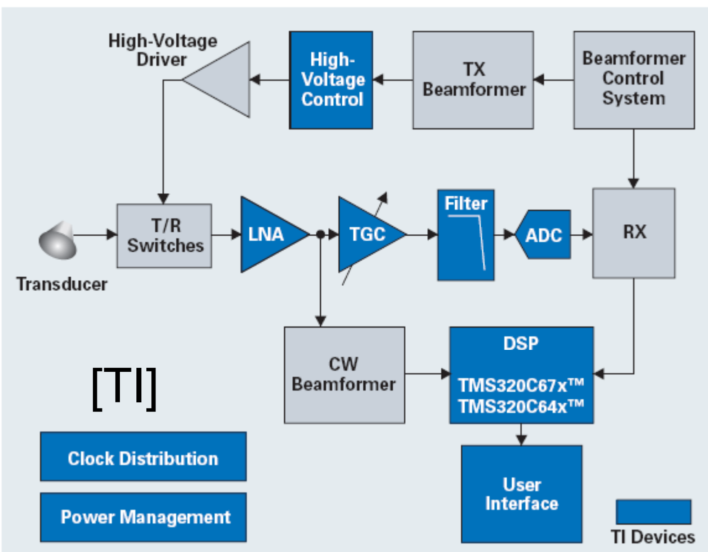


Comparison and Outlook



Driver Application



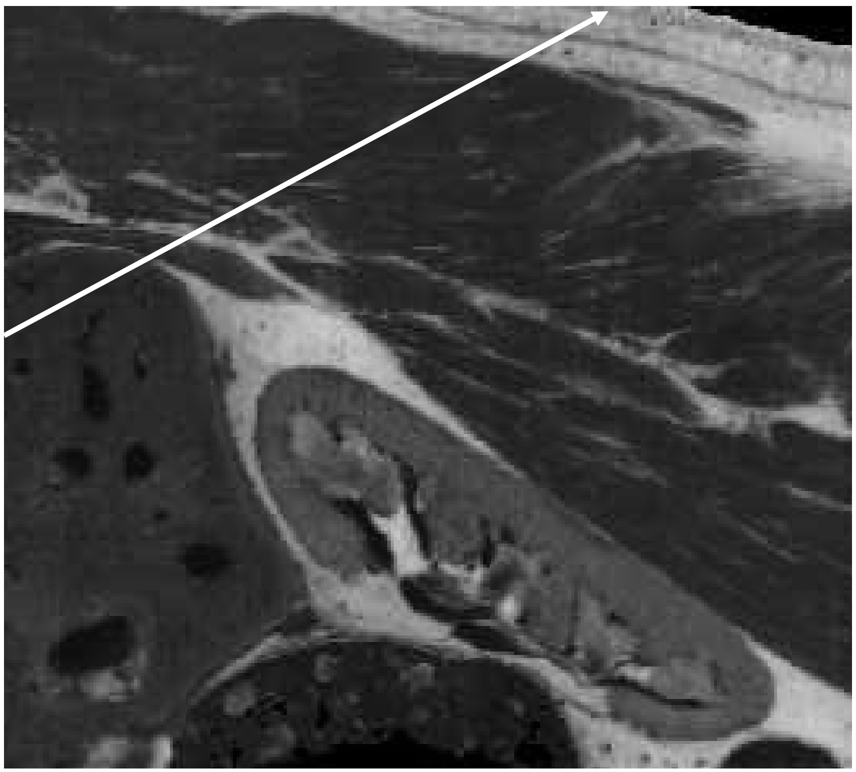


Ultrasound system block diagram.

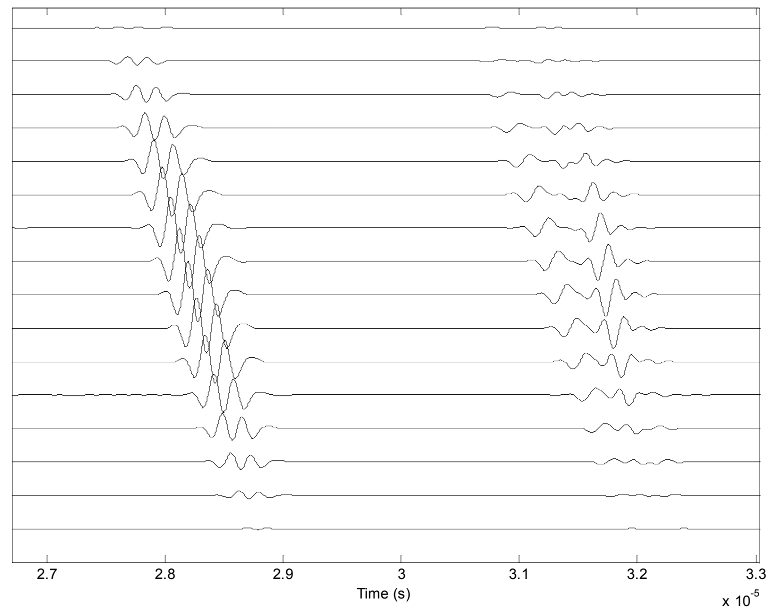
- Medical ultrasound
- Want to implement 64+ high speed ADCs on a single chip
- Approach
  - Minimalistic, digitally assisted pipeline ADC
  - Exploit specific signal and system properties!

Received Signals Are Highly Correlated

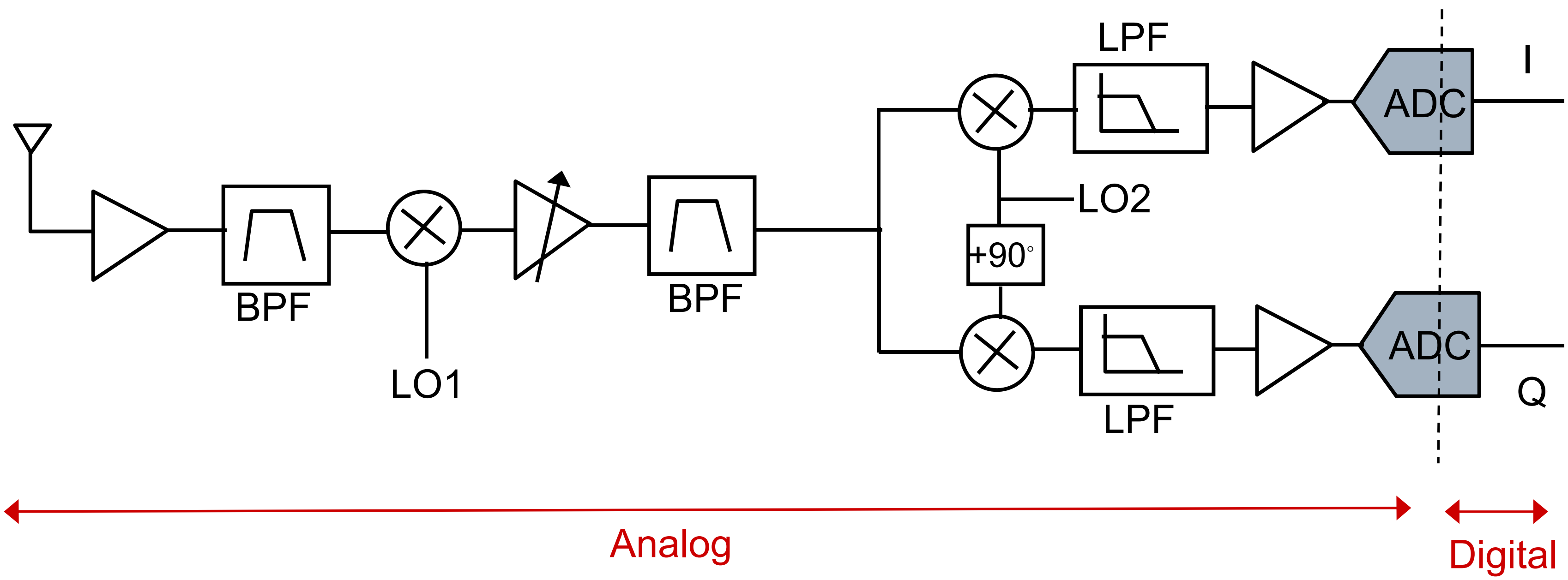
Phantom Image of Kidney



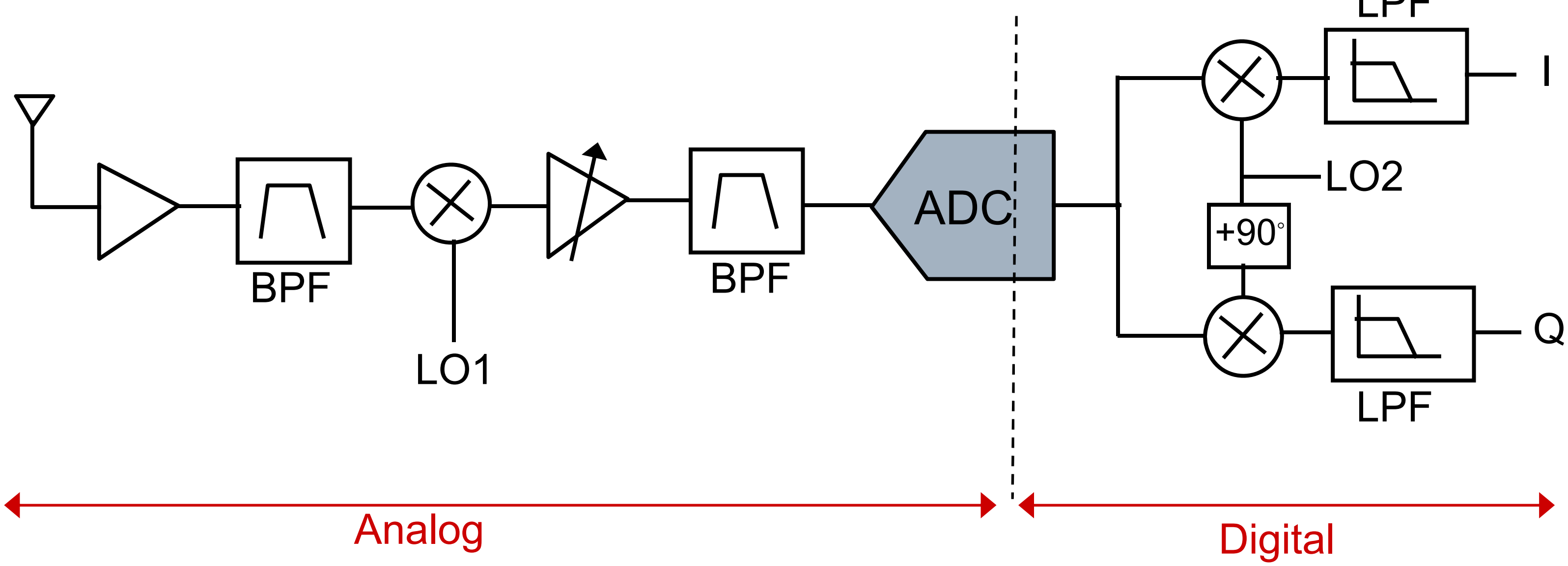
Received Signal Traces



Typical Heterodyne Receiver

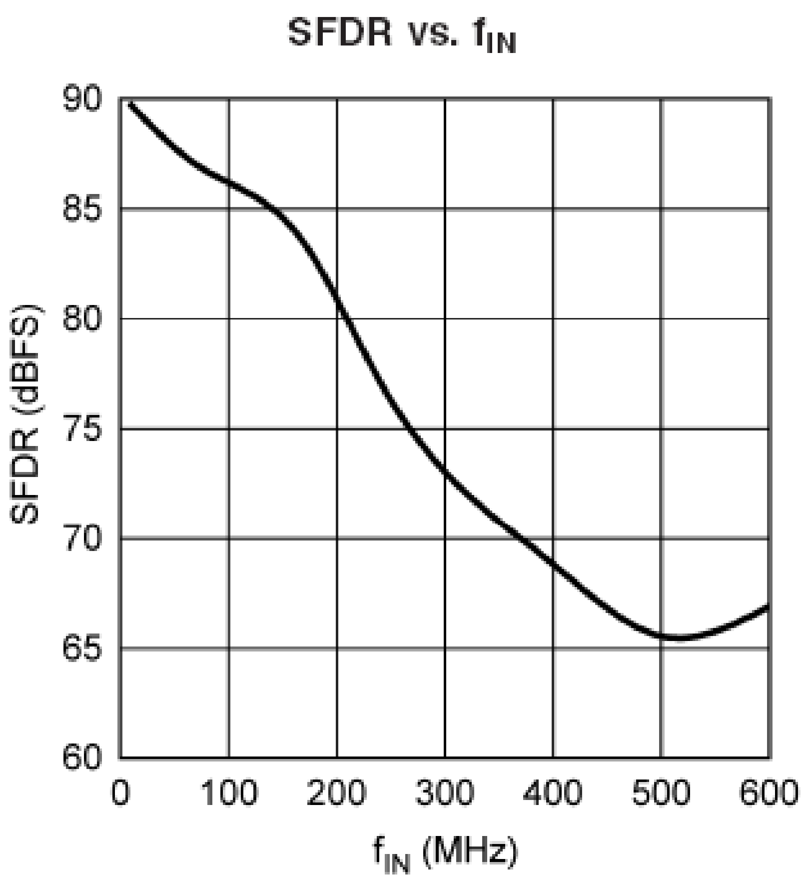


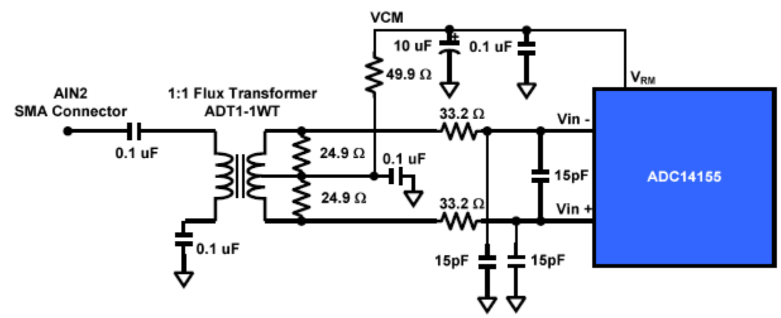
IF Subsampling Receiver



- Need ADC with high linearity at IF input frequencies

SFDR of Typical CMOS ADC

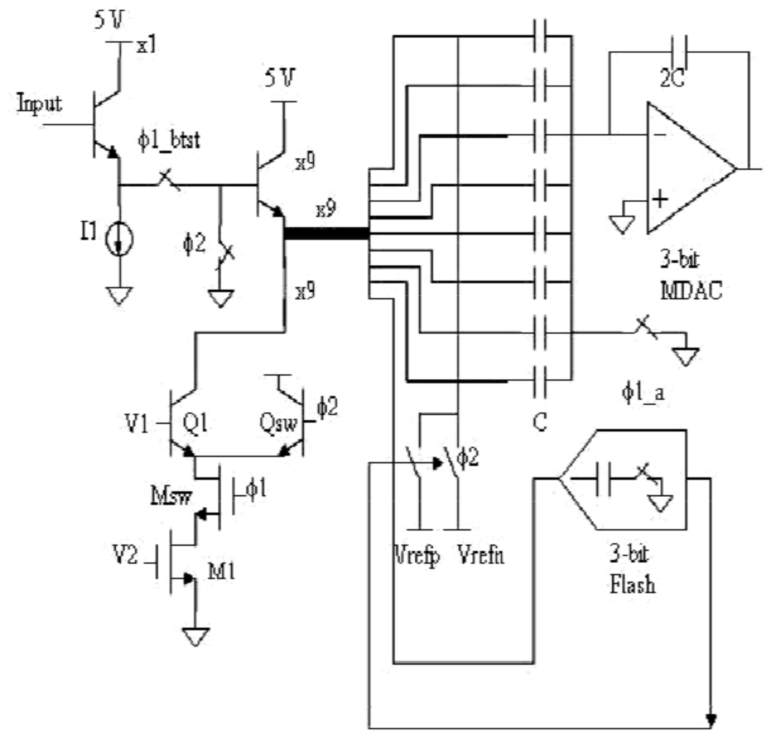




National ADC14155: 14bit, 155 MS/s, 1.1 GHz Bandwidth A/D converter

Achieving High SFDR (1)

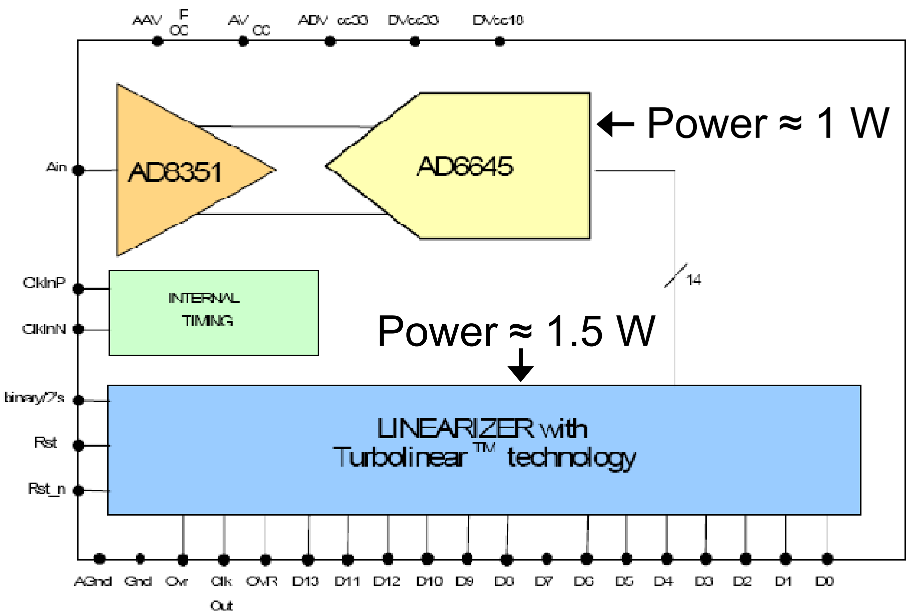
- BiCMOS front-end
  - BJTs used as buffer for linear signal tracking and sampling
  - Can achieve SFDR>90dB up to 4th Nyquist zone at 125MS/s
- $$$

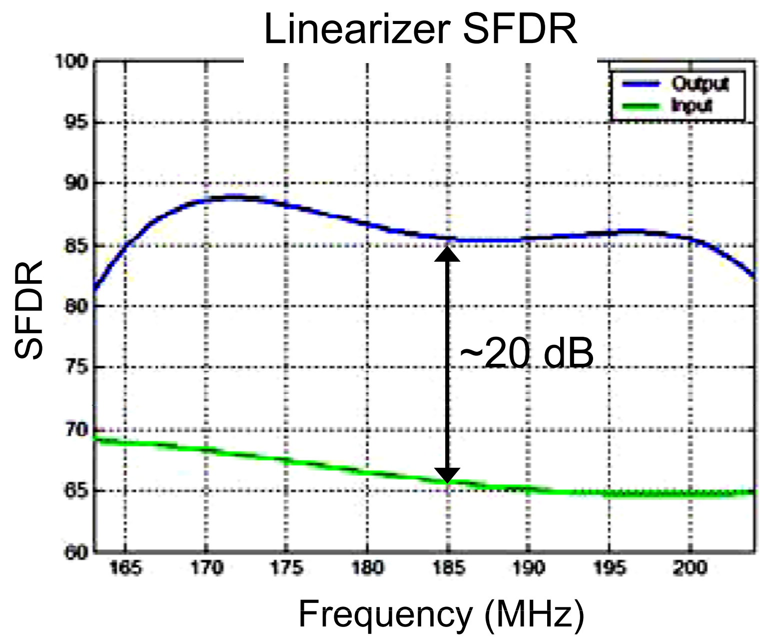


A.M.A. Ali et al. “A 14 bit 125 Ms/s IF/RF Sampling Pipelined A/D Converter,” IEEE CICC, Sep. 2005

Achieving High SFDR (2)

- Compensate nonlinearities by applying inverse nonlinear function to the digital output
  - Roy Batruni, www.optichron.com
- Issue: complexity, power



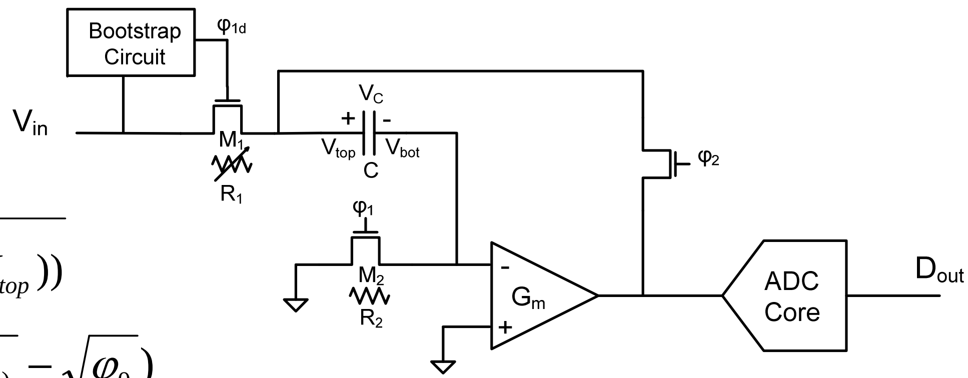


Judicious Modeling

- During tracking mode, the track-and-hold can be modeled as an RC circuit with an input dependent resistance

$$V_{in} = V_C + (R_1 + R_2) C \frac{dV_{out}}{dt}$$

$$\begin{cases} R_1 = R_1(V_{in}) = \dfrac{1}{\mu_n C_{ox} \dfrac{w}{l} (V_{gs} - V_{th}(V_{in}, V_{top}))} \\ V_{th}(V_{in}, V_{top}) = V_{th0} + \gamma \left(\sqrt{\varphi_0 + (V_{in}, V_{top})} - \sqrt{\varphi_0} \right) \end{cases}$$



Flip-around track-and-hold circuit

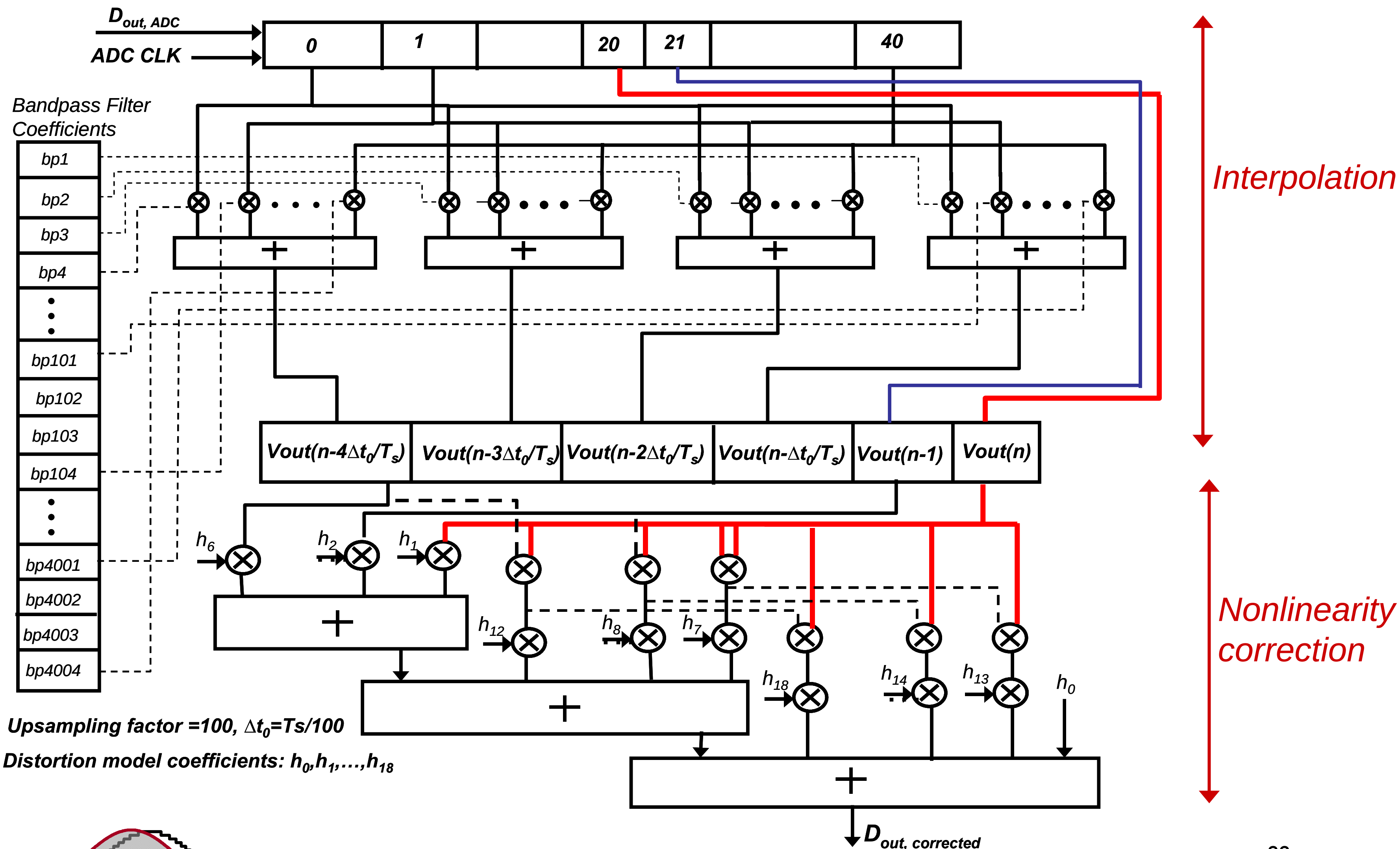
At the sampling instant

$$V_{in}(k) = V_{out}(k) + (a_0 + a_1 V_{out}(k) + a_2 V_{out}{}^2(k) + \ldots) \times \frac{dV_{out}(k)}{dt}$$

nonlinearity *memory*

Nikaeen & Murmann CICC 2008

Digital Processor Diagram



Upsampling factor =100, Δt_0=Ts/100

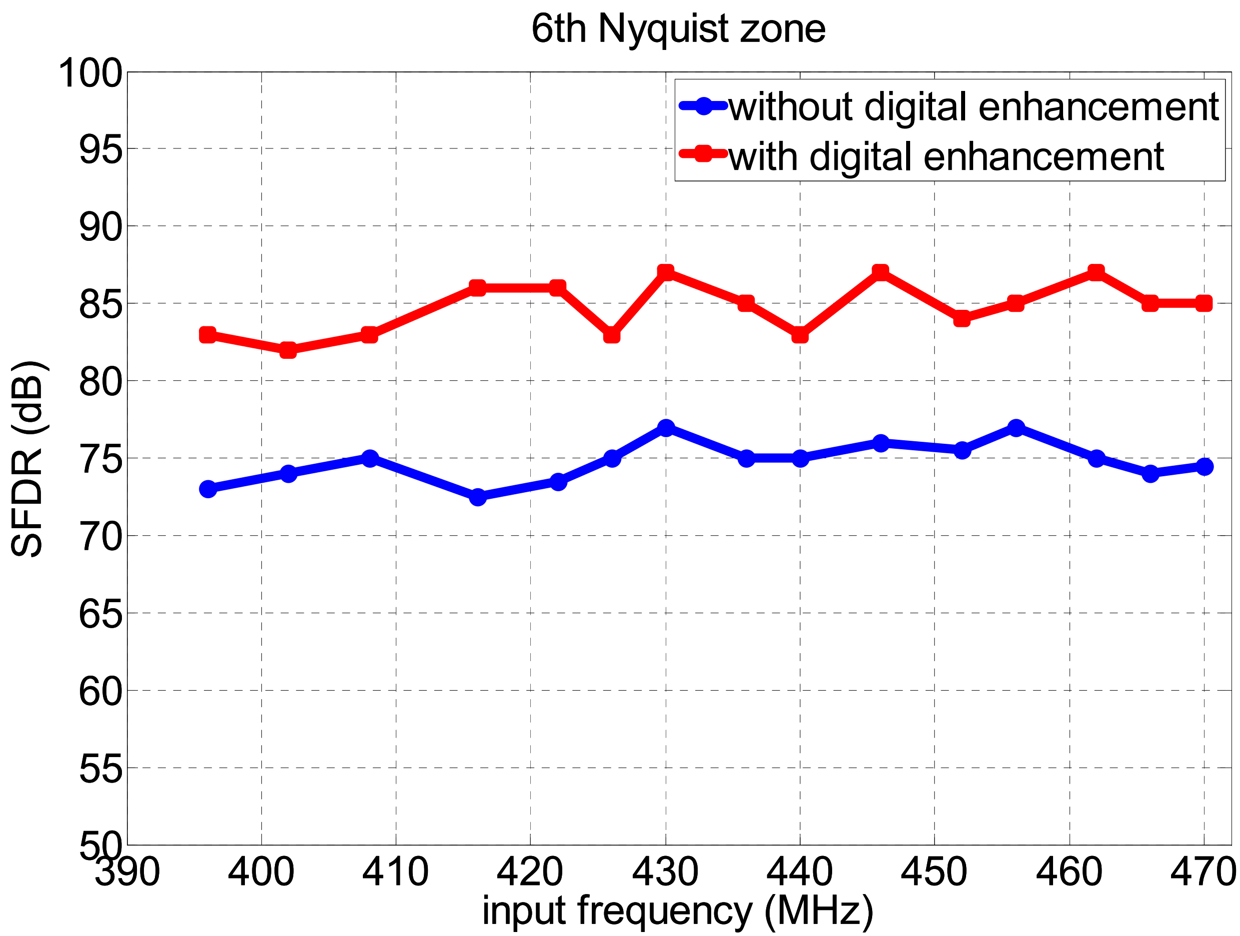
Distortion model coefficients: $h_0, h_1, \ldots, h_{18}$

Hardware Requirements

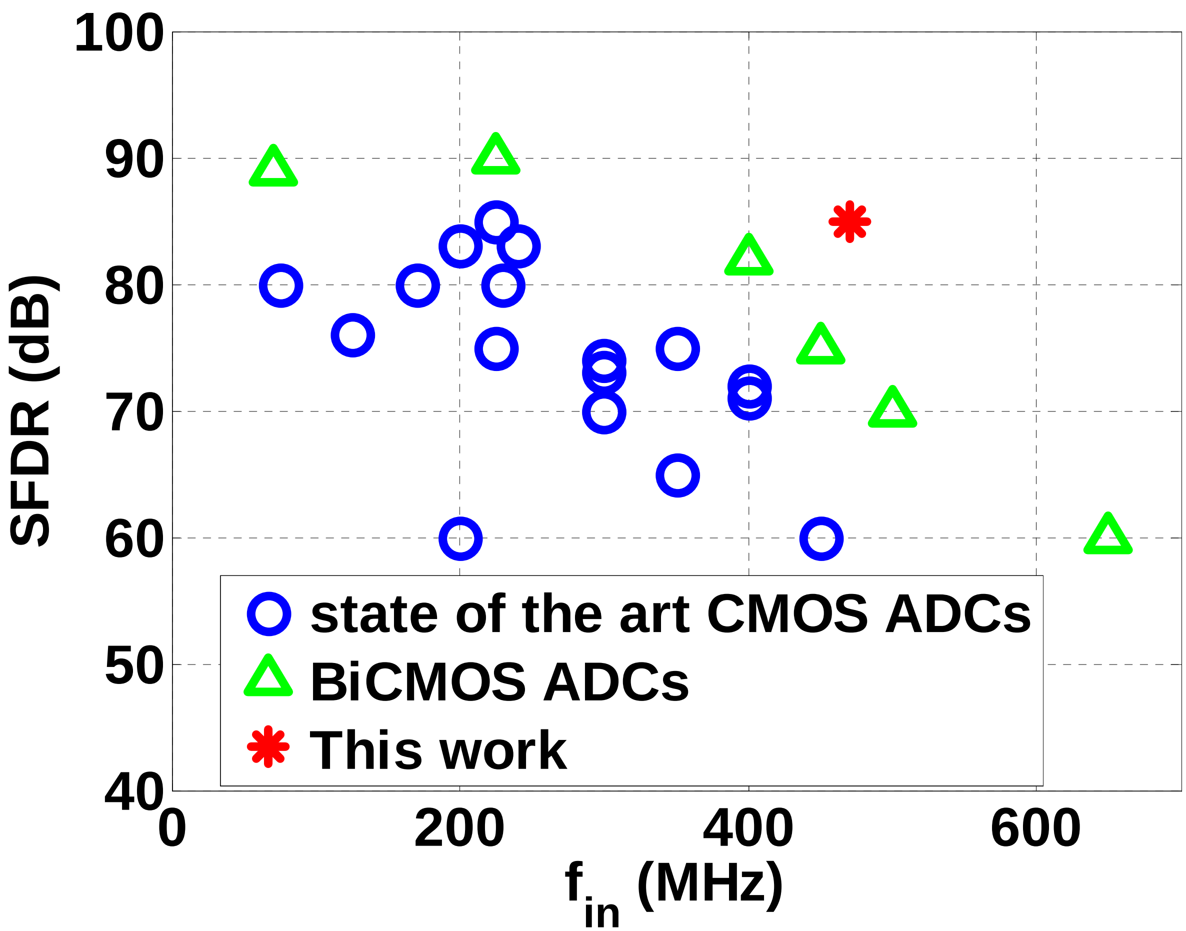
- The algorithm was implemented in Verilog and synthesized using standard CMOS cells in 90nm

Technology	90-nm CMOS
Clock speed	155 MHz
Latency	33 clock cycles
Number of logic cells	61,339
Area	$0.54mm^2$
Power	52 mW
ADC power (ADC14155)	967 mW

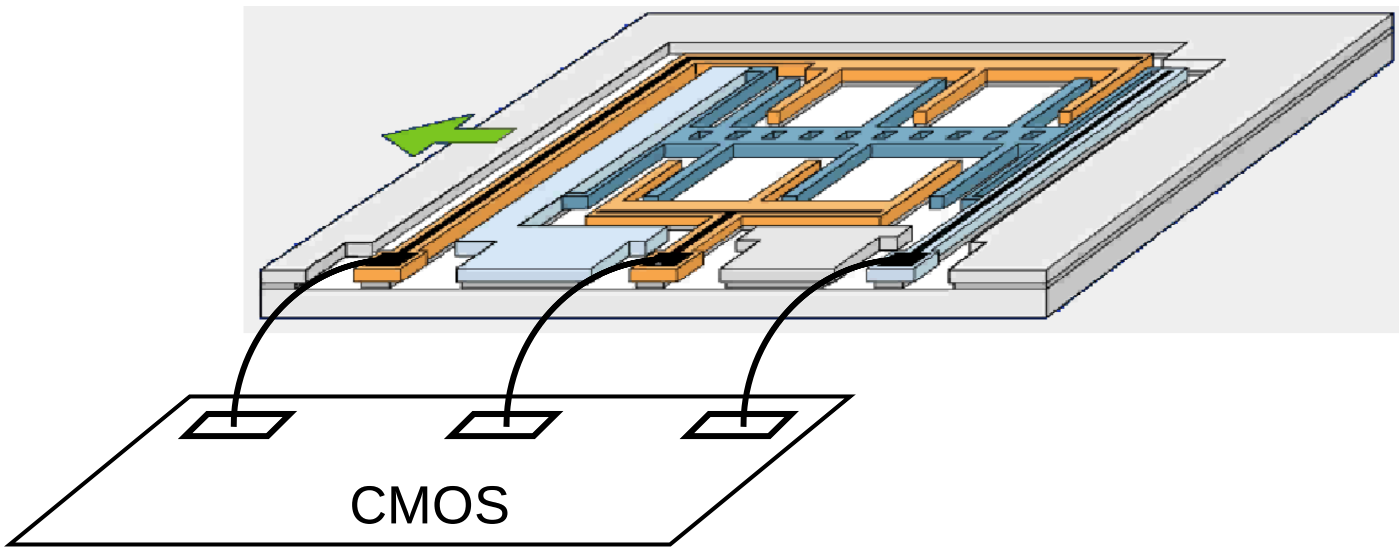
Measured Results



SFDR Comparison

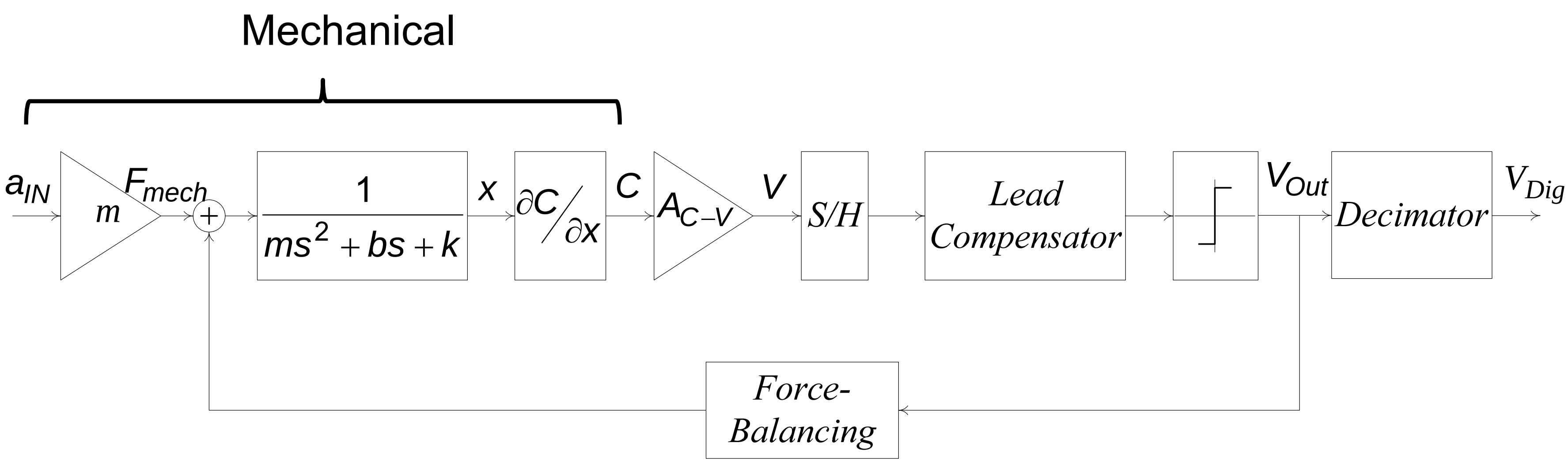


MEMS Accelerometer



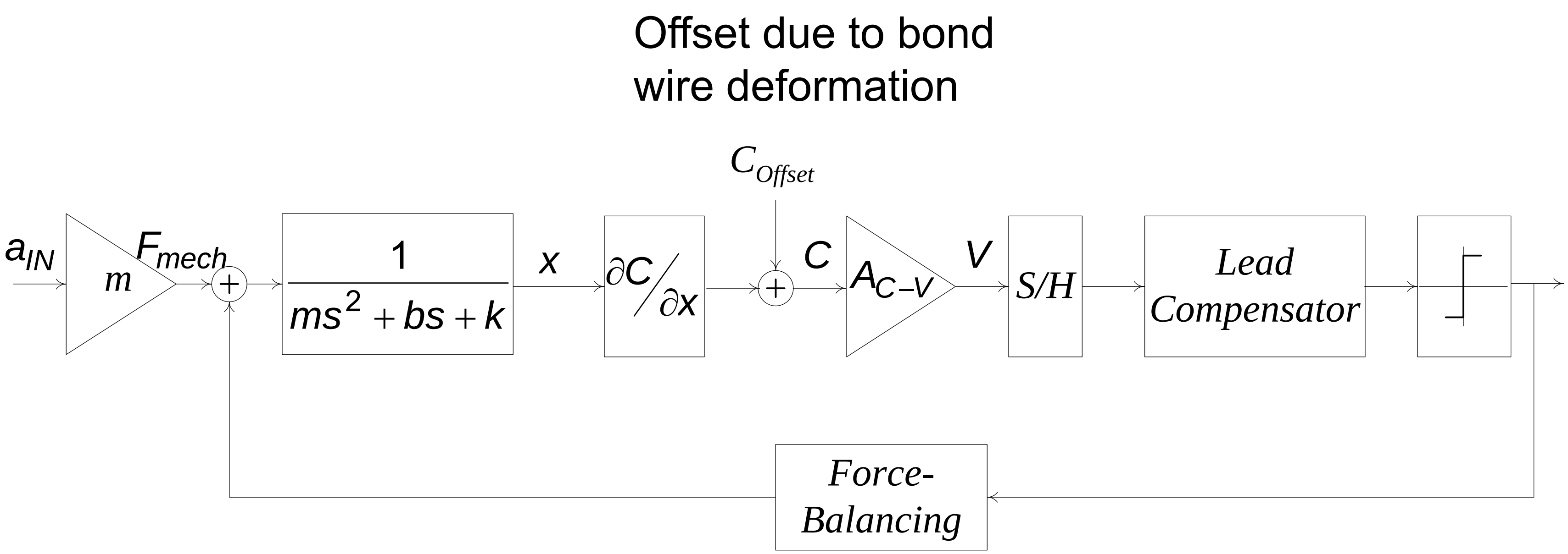
- Capacitance change ~10 fF/g
- Desired resolution ~10 mg for airbags and ESP
  - Must resolve capacitance changes of ~100 aF
- Problem: Drift in parasitic bondwire capacitance

Sigma-Delta Interface



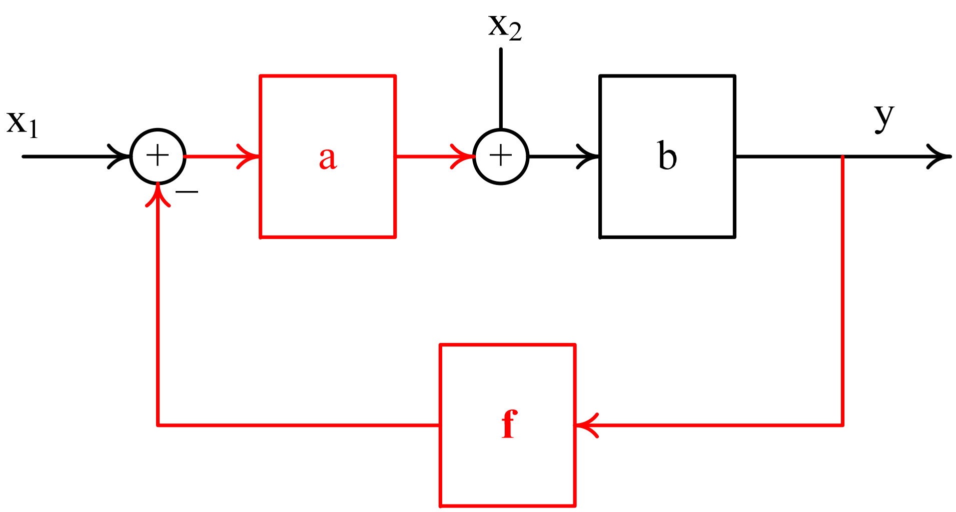
M. Lemkin and B. E. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. Solid-State Circuits*, vol. 34, pp. 456-468, April 1999.

Offset



- Drifts over time
- Indistinguishable from DC acceleration

Linear Feedback System with Two Inputs

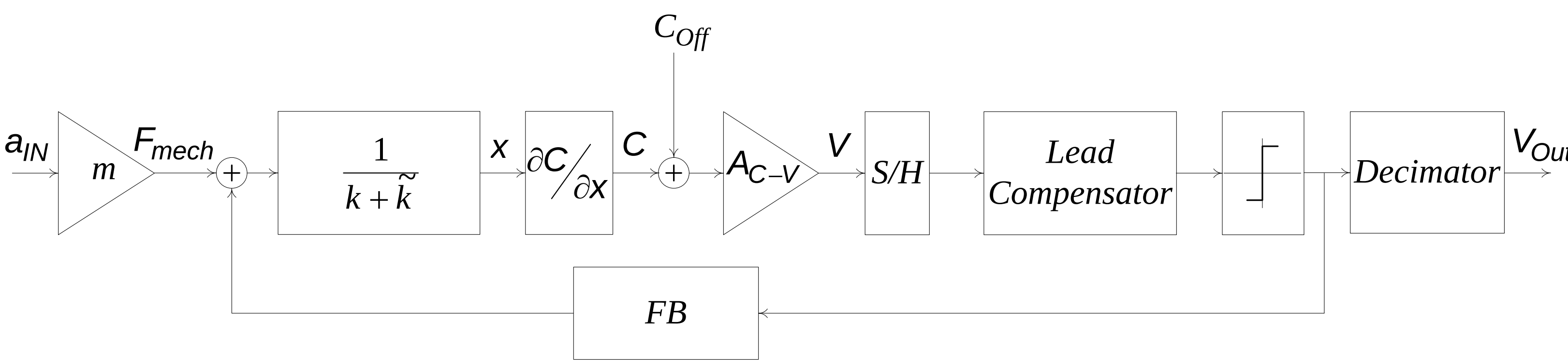


$$y \cong x_1 \cdot \frac{1}{f} + x_2 \cdot \frac{1}{f \cdot a}$$

Spring Constant Modulation

- The output due to C_{off} can be modulated to higher frequencies by modulating k

$$V_{Out} \cong F_{mech} \cdot \frac{1}{FB} + C_{Off} \cdot \frac{k+\tilde{k}}{FB \cdot \frac{\partial C}{\partial x}}$$

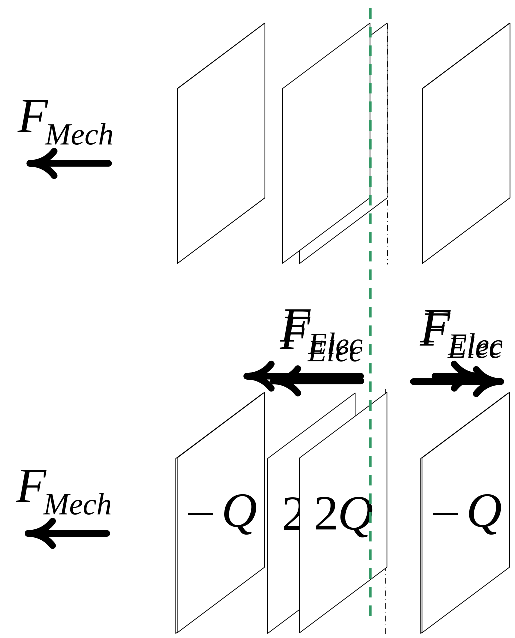


Spring softening effect

No electrostatic force

With electrostatic force

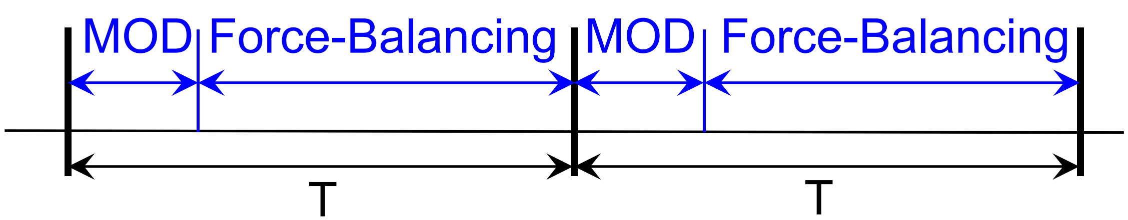
Larger displacement than expected



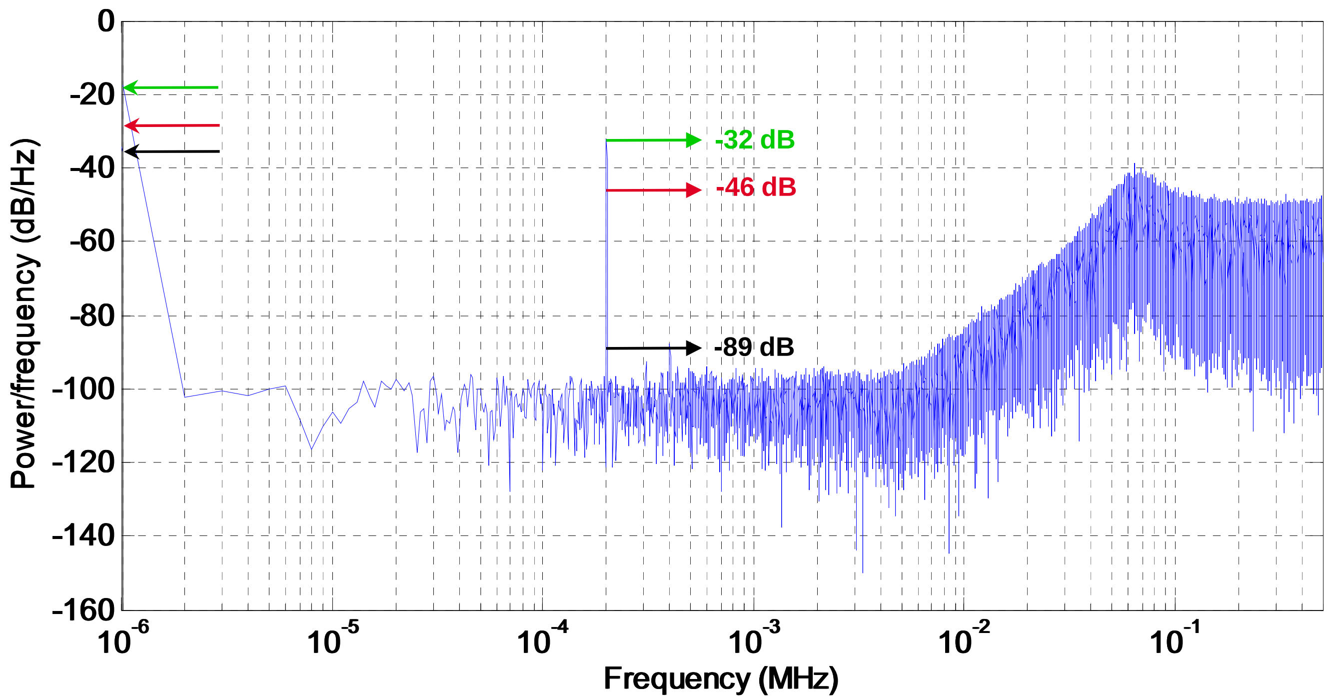
- Can be used to modulate spring constant

Time-Multiplexed Feedback

- Phase 1
  - Spring constant modulation
- Phase 2
  - Sigma-delta force-balancing



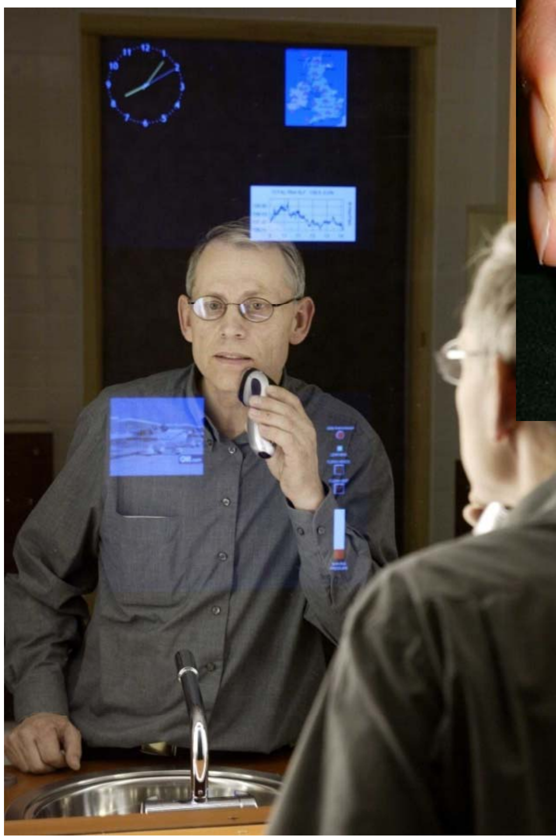
Simulated Output Spectrum



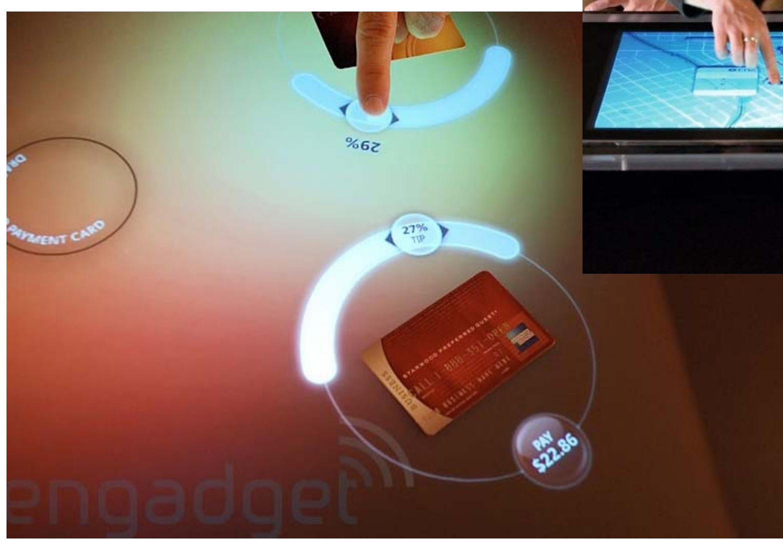
DC Acceleration	Offset Capacitance
9.1 m/s^2	**0 fF**
9.1 m/s^2	**10 fF**
9.1 m/s^2	**50 fF**

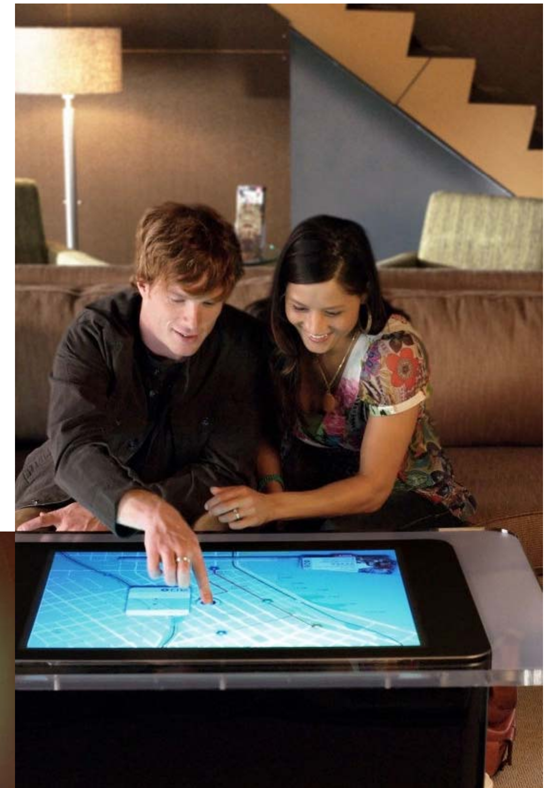
- Currently working on IC prototype

The Future?



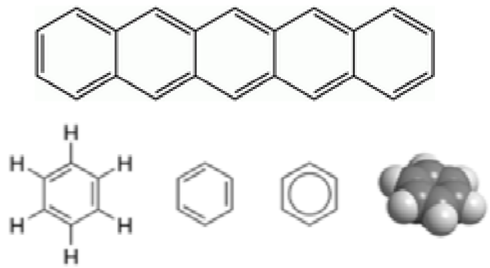

CAMBRIDGE,Mass.--September
17, 2001--E Ink Corporation, the
leading developer of electronic
ink technology for paper-like
displays, today announced the
opening of a flexible
microelectronics facility in
Woburn, Mass. The 9,500
square foot building will house E
Ink's Microelectronics
Technology Group.The group
will develop microelectronics;

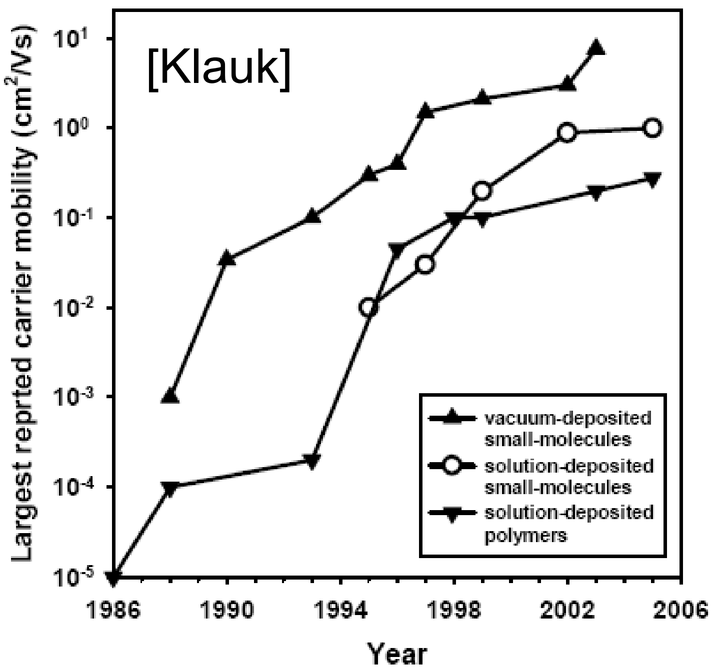

PAYMENT CARD
27% TIP
PAY $22.86
engadget



Organic Semiconductors

Pentacene

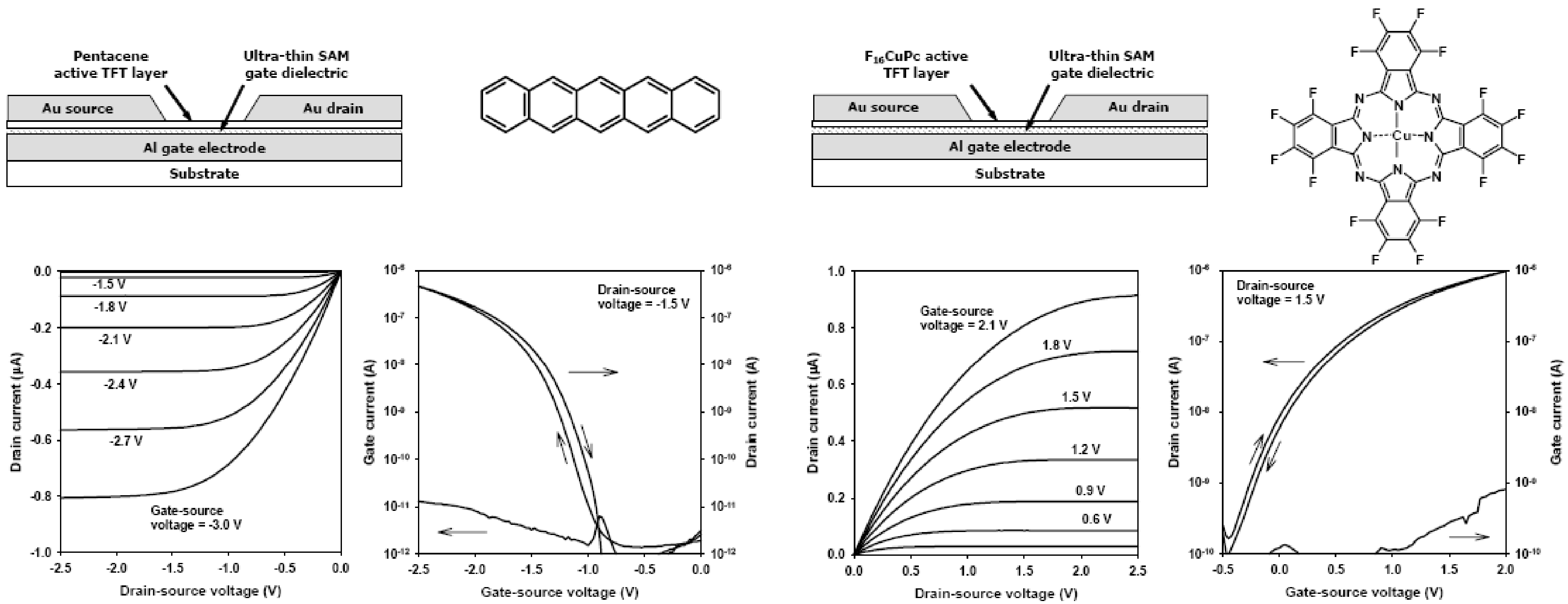




- Mechanically flexible
- Suitable for solution processing
  - <u>Cheap to cover large areas</u>
  - Make disposable devices

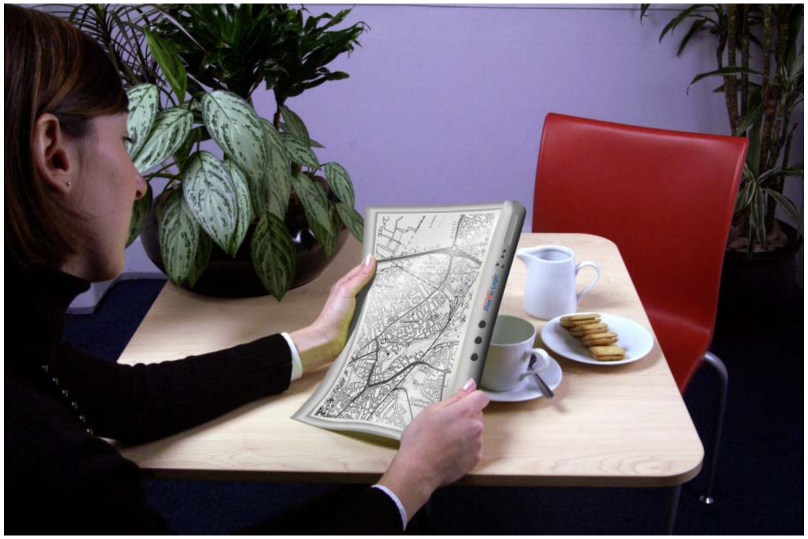
Applied Films

Organic Transistors



[Klauk]

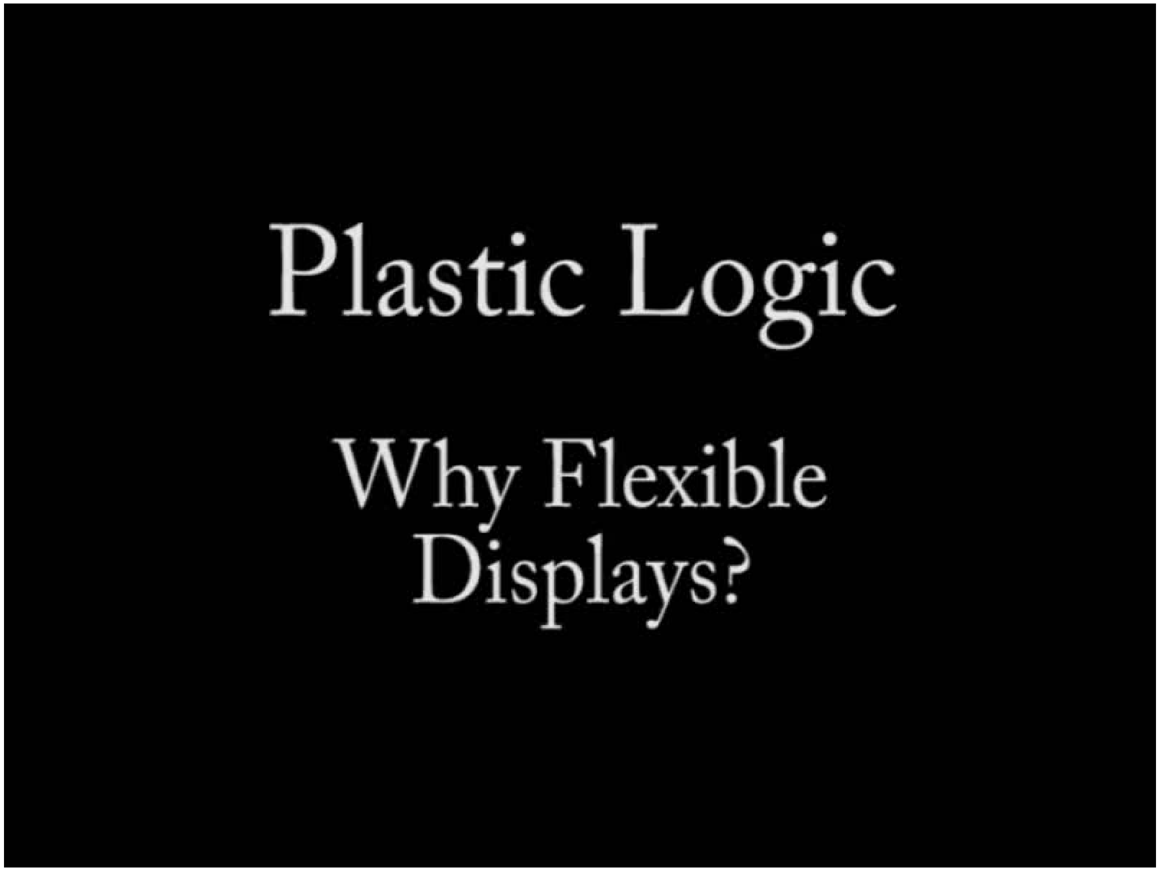
Displays (1)



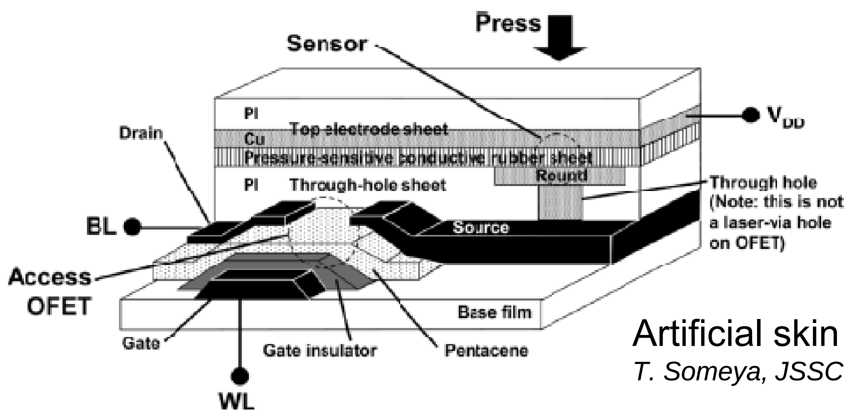
Plastic Logic

Sony's 1,000,000:1 contrast ratio 27-inch OLED HDTV

Displays (2)

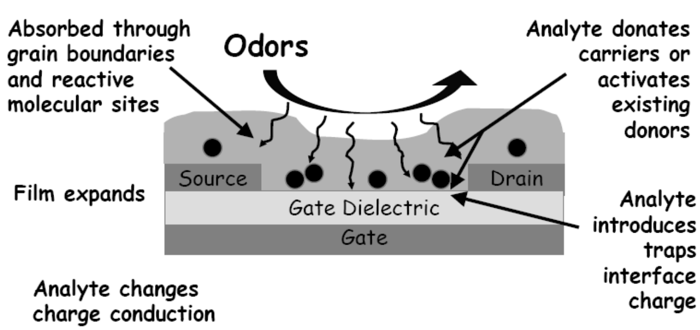


Sensor Applications



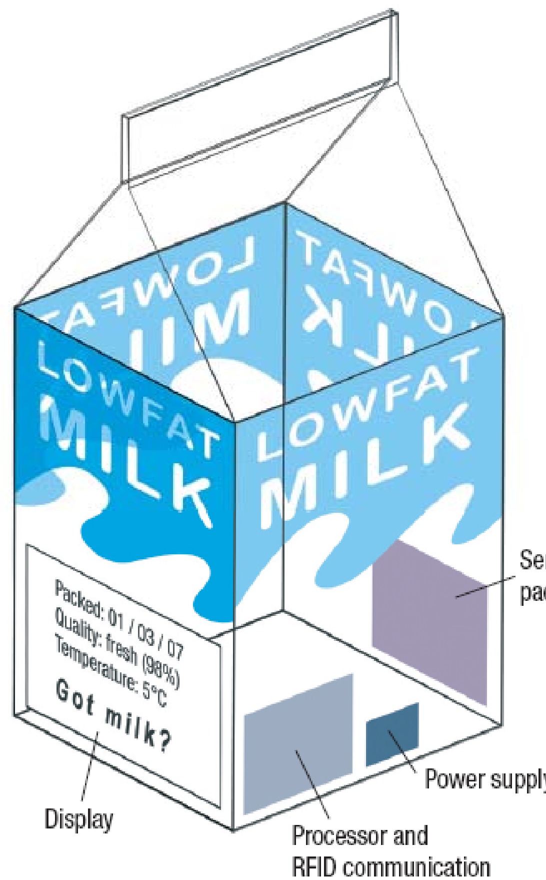
Artificial skin

T. Someya, JSSC 2005

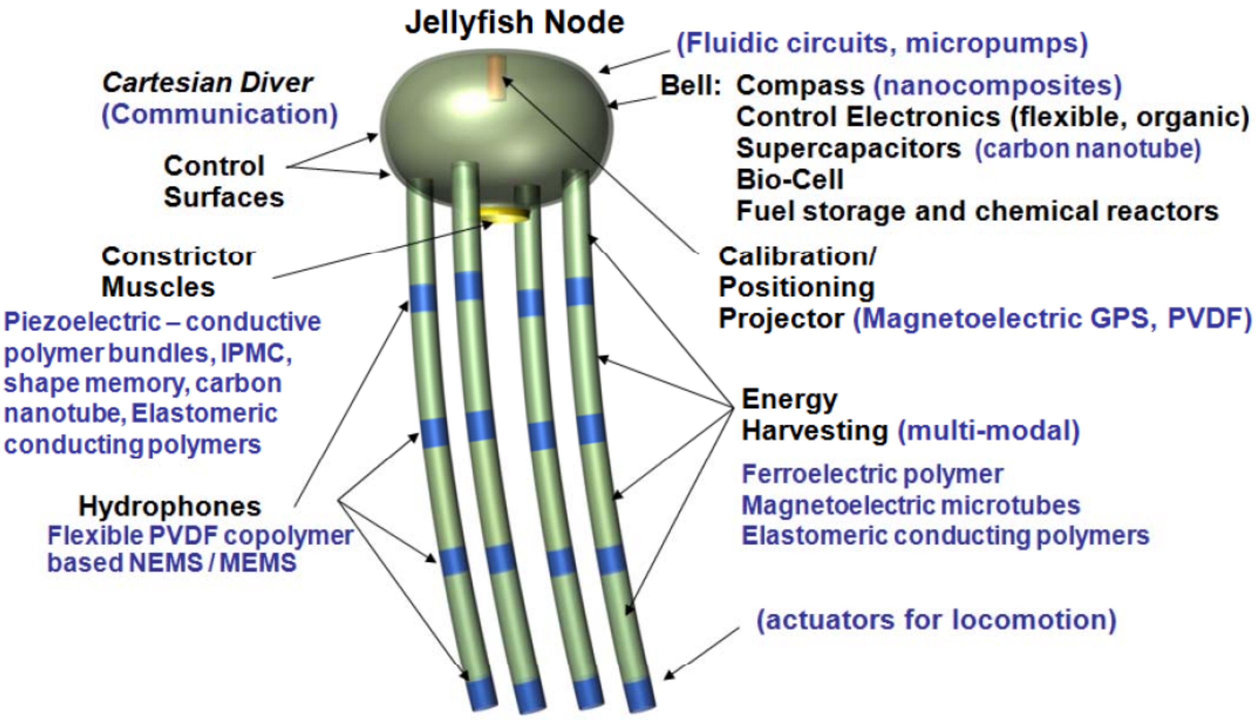


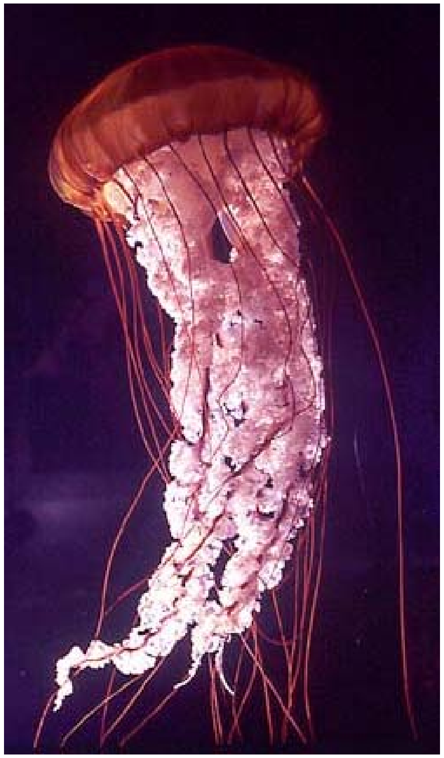
Chemical sensor

V. Subramanian, ISSCC 2006



Jelly Fish Autonomous Node

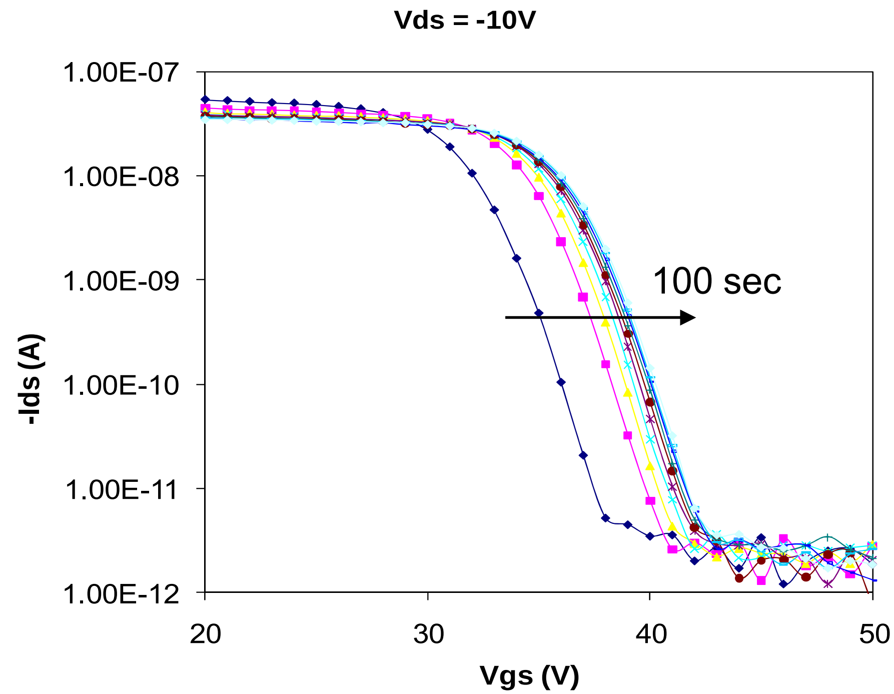




http://muri.mse.vt.edu/

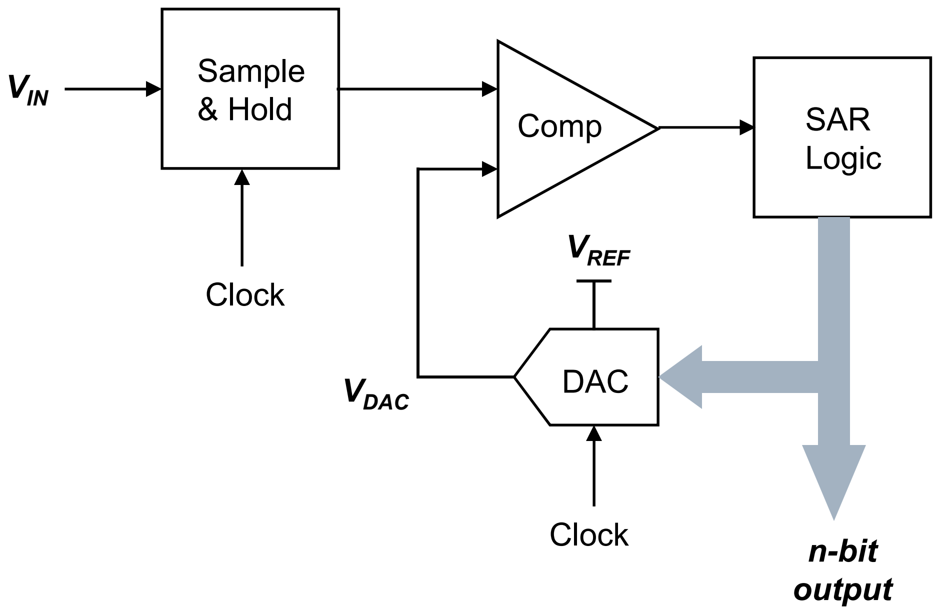
Organic Circuit Design Challenges

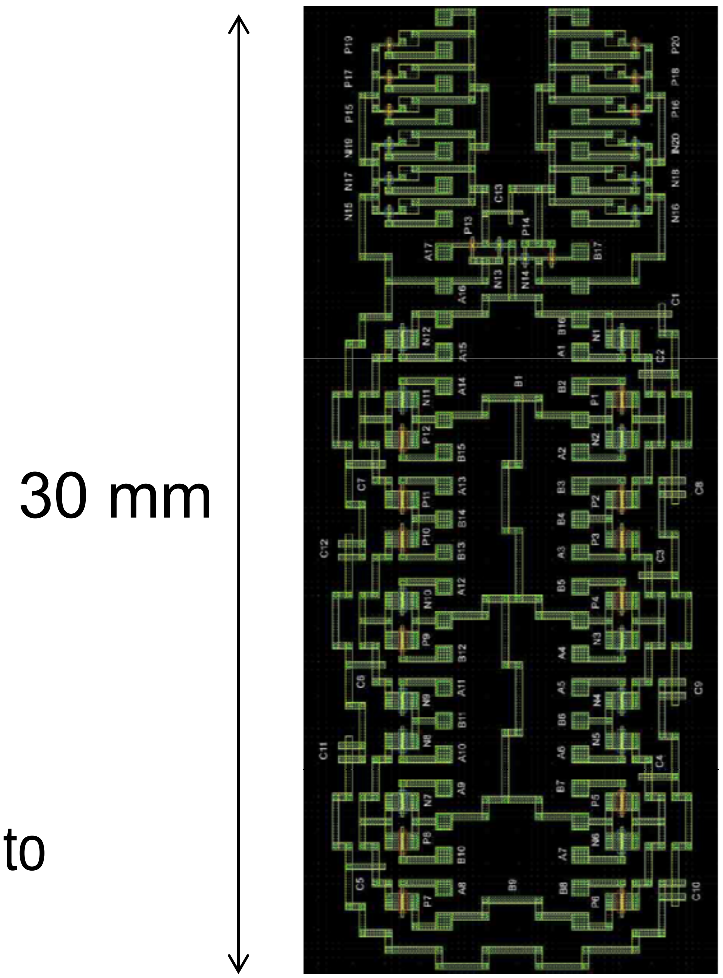
- Poor mobility
- Age degradation
- Bias stress effects
- Device-to-device variations
- Dielectric leakage



- To date, very little work on <u>analog</u> circuits using organic transistors

Work in Progress: ADC using OTFTs





- Leverage experience from Si-CMOS to create a robust OTFTdesign

Summary

- Mixed-signal IC design is no longer business as usual
  - Expect less return from pure "scaling" of decade-old circuits
  - Time to become creative
- Many opportunities for innovation fall into the "cracks" between traditional boundaries of analog & digital, circuit & algorithm, mechanical & electrical partitioning
- Trend toward "More than Moore" will likely bring diversification of device technologies
  - MEMS/NEMS, large area device technologies, novel sensor devices, …

Sponsors

National Semiconductor
The Sight & Sound of Information

Texas Instruments

Analog Devices

NEC

BOSCH

Agilent Technologies

Renesas
Everywhere you imagine.

SONY

LSI

TOSHIBA
Leading Innovation

SRC
Semiconductor Research Corporation

Medtronic
Alleviating Pain · Restoring Health · Extending Life

intel.

Rambus

C2S2

ONR
Revolutionary Research . . . Relevant Results