CMOS RF Power Amplifiers: Nonlinear, Linear, Linearized

David Su

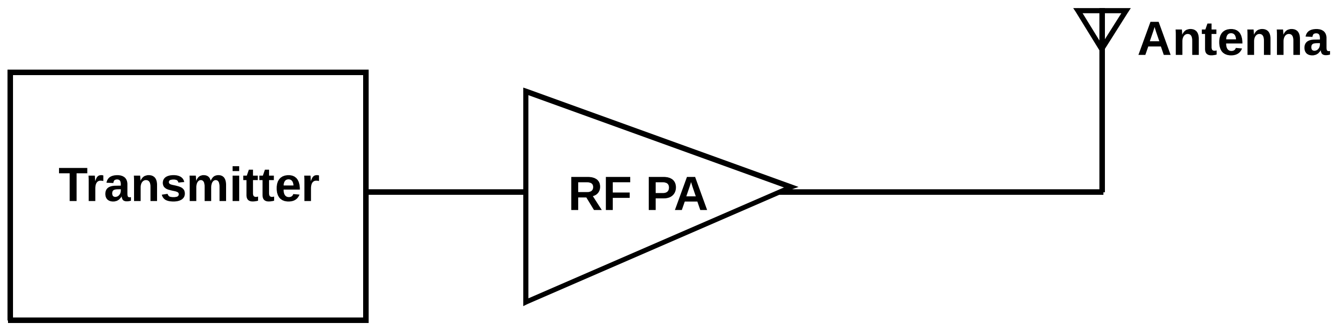
Atheros Communications

Sunnyvale, California

Outline

- Introduction
- Nonlinear Power Amplification
- Linear Power Amplification
- Linearization using Envelope Elimination and Restoration
- Conclusion

RF Power Amplification

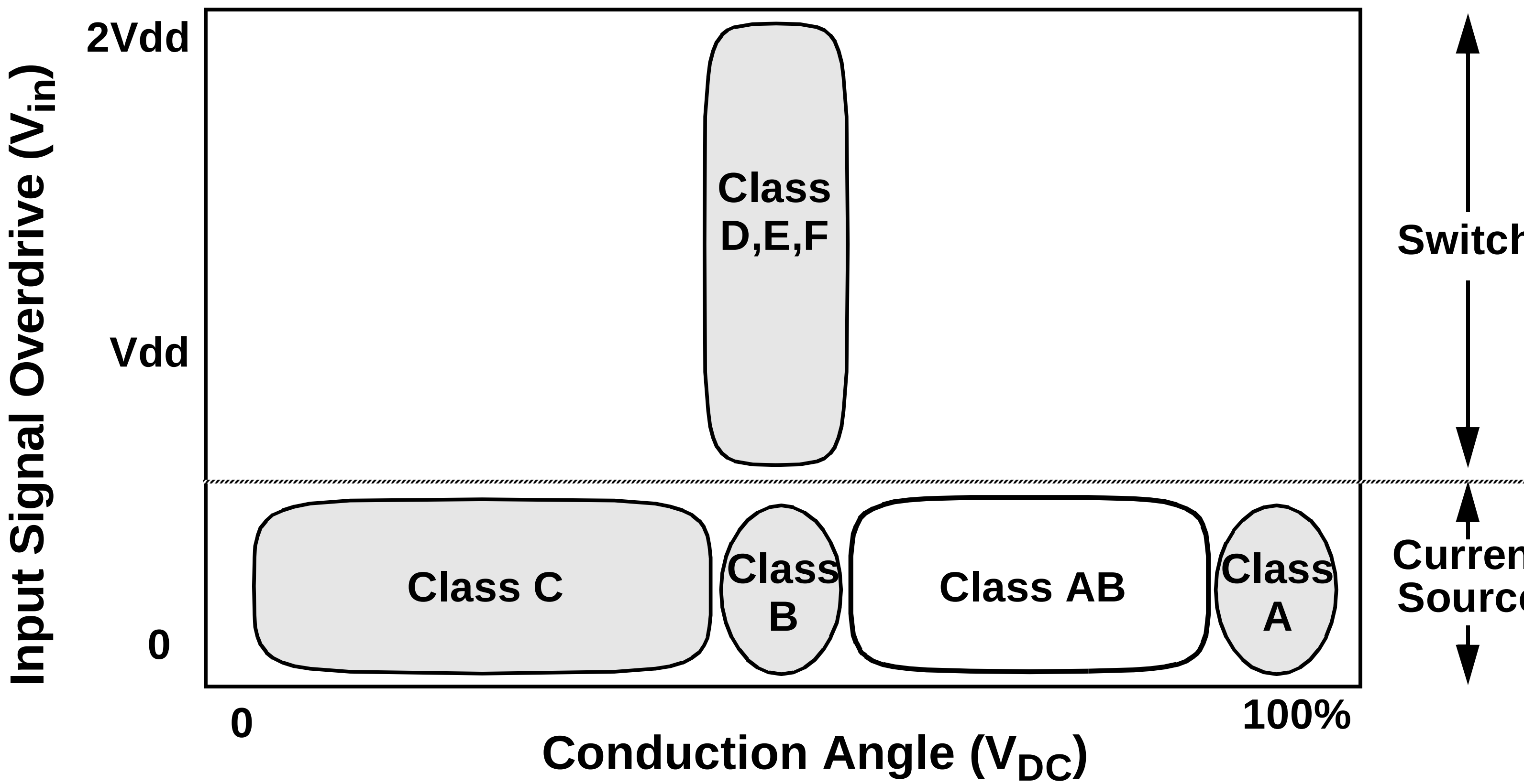


- **Purpose:** Delivers “narrow-band” RF power to a 50-ohm antenna
- **Performance:** Output Power
  Efficiency
  Linearity

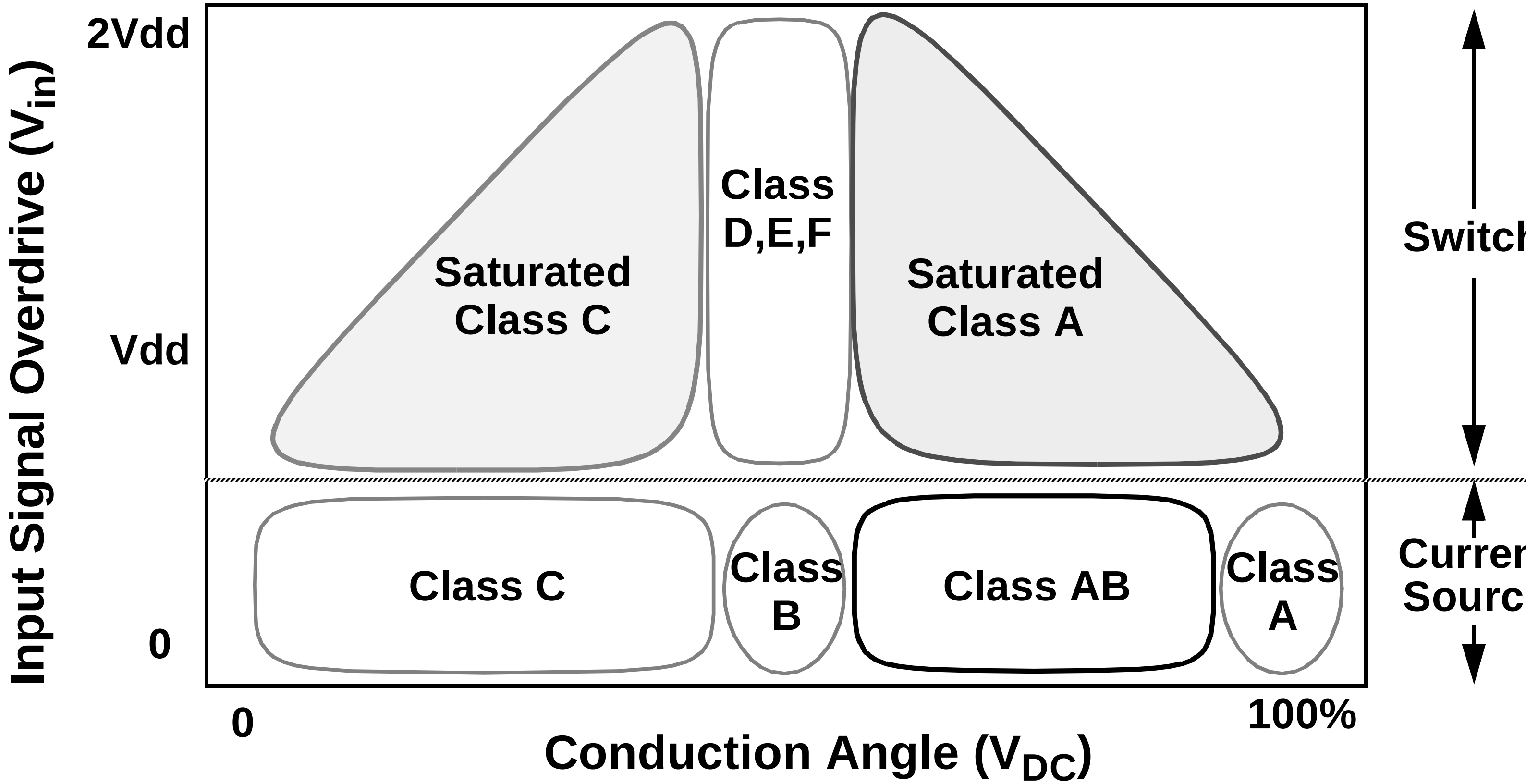
Traditional PA Classification

Class	Modes	Conduction Angle	Output Power	Maximum Efficiency	Gain	Linearity
A	Current Source	100%	moderate	50%	Large	Good
B		50%	moderate	78.5%	Moderate	Moderate
C		< 50%	small	100%	Small	Poor
D	Switch	50%	large	100%	Small	Poor
E		50%	large	100%	Small	Poor
F		50%	large	100%	Small	Poor

PA Classification & Input Drive



Power Amplifier Classification



CMOS for RF Power Amplification

- **Traditional RF PAs use GaAs / Bipolar.**

- **Advantages of CMOS:**

  Low cost, high-yield, high-integration

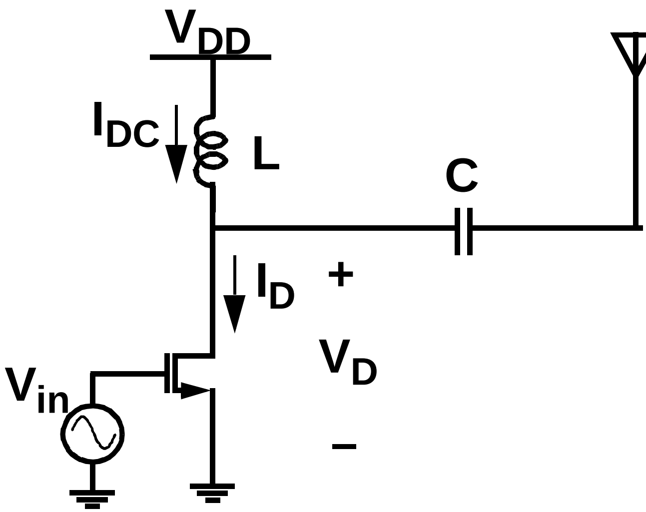
  Efficient switched-mode amplifier

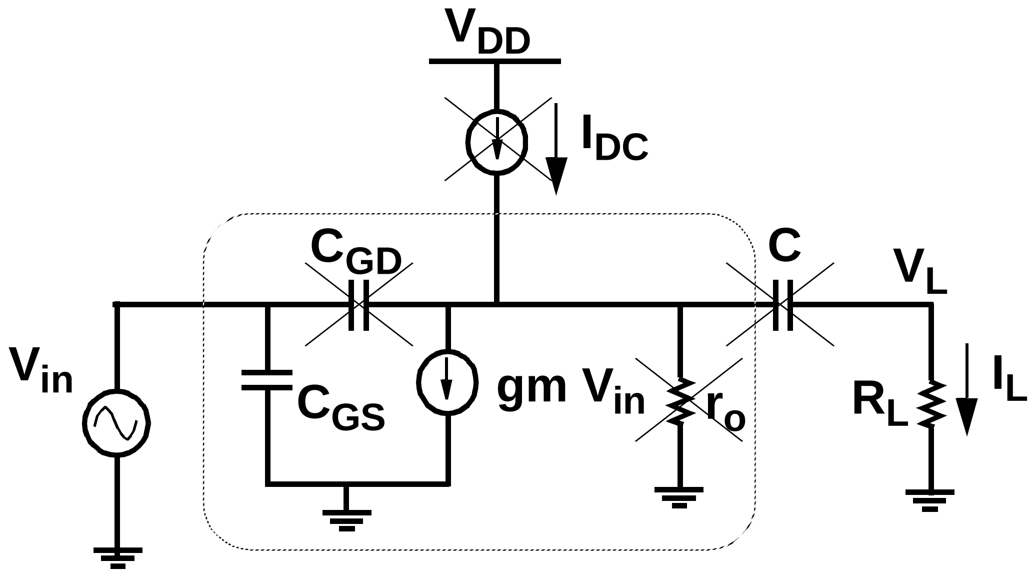
- **Disadvantages of CMOS:**

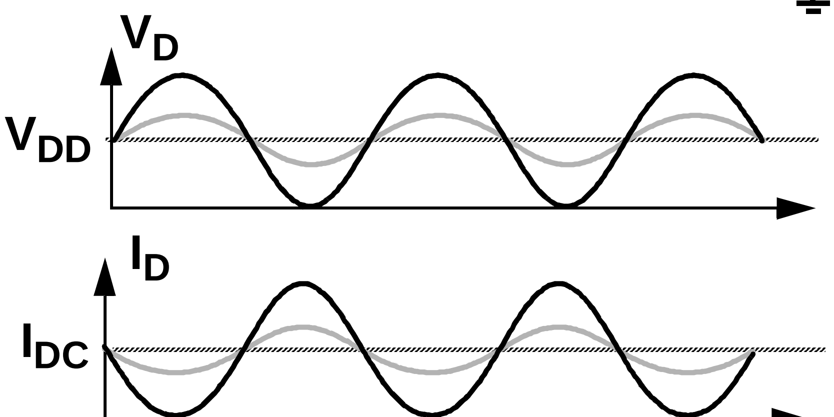
  Low bandwidth

  Low breakdown voltage

Simplified RF Output Stage



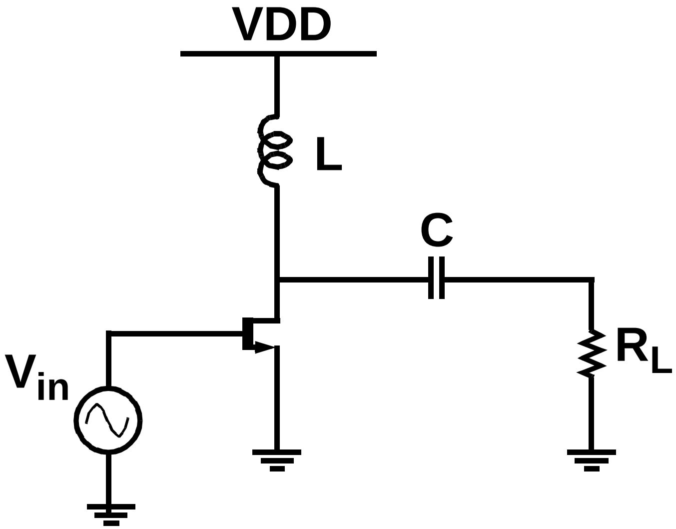


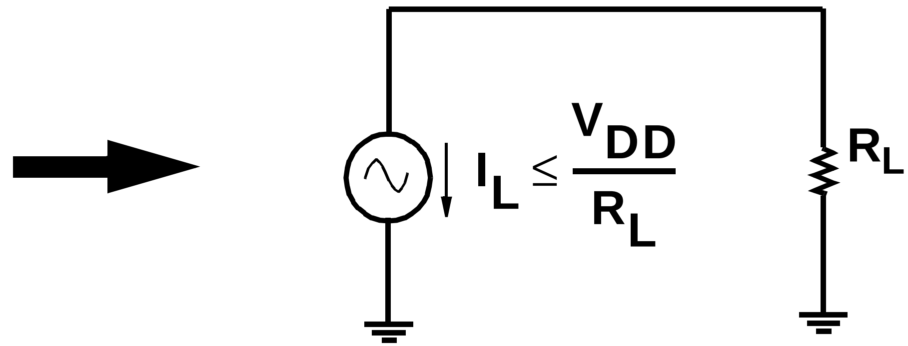


$$I_D = gmV_{in}$$

$$I_L \leq \frac{V_{DD}}{R_L}$$

Class-A (Linear) Operation





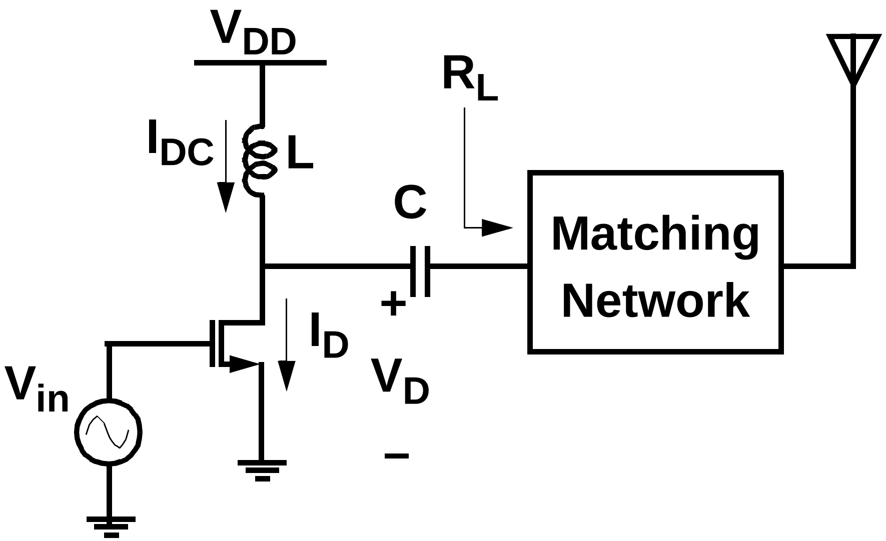
AC Equivalent Model

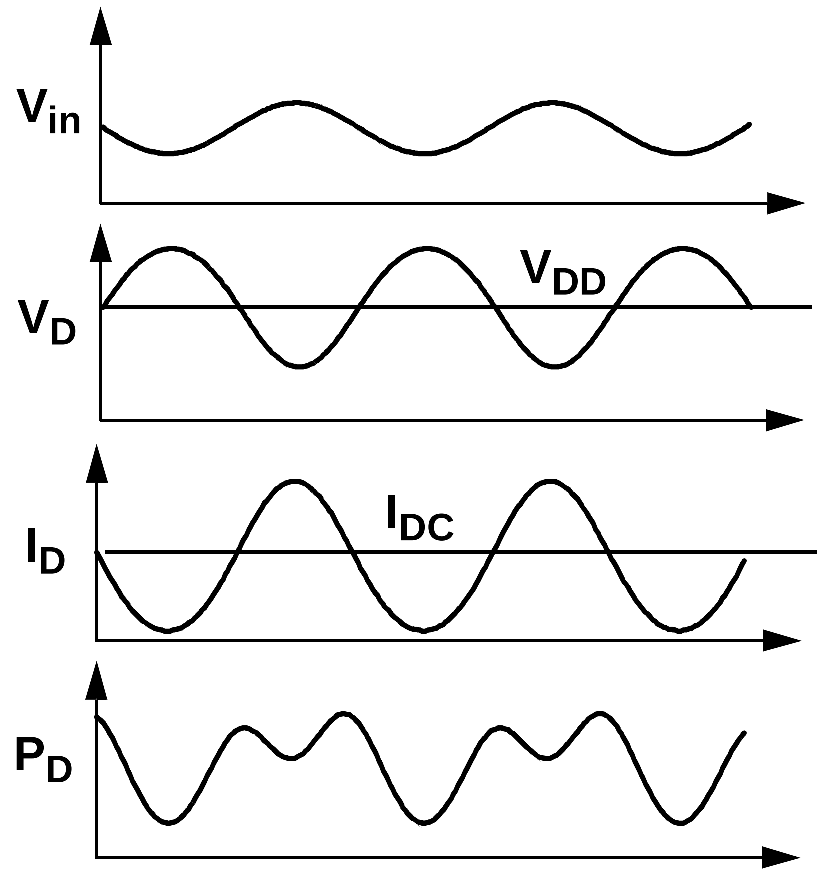
$$P_{out} = \frac{1}{2} I_L^2 R_L \leq \frac{VDD^2}{2R_L}$$

For Pout = 1 W (Class A), R_L = 4.5 Ω @ VDD = 3V
R_L = 3.1 Ω @ VDD = 2.5V

⇒**Needs Impedance Transformation Network → 50 Ω antenna**
⇒**Keep parasitic loss << R_L of 3.1 Ω**

Efficiency of Class A operation





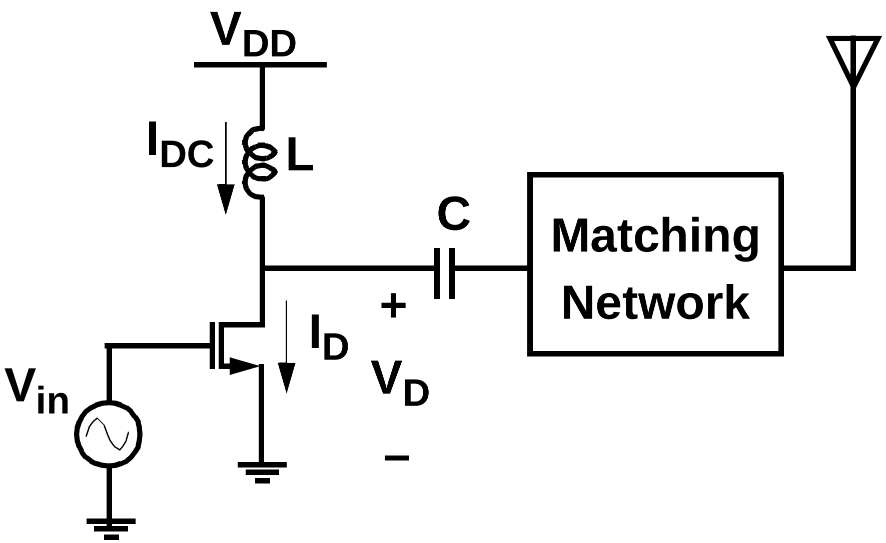
$$Pout \leq \frac{VDD^2}{2R_L}$$

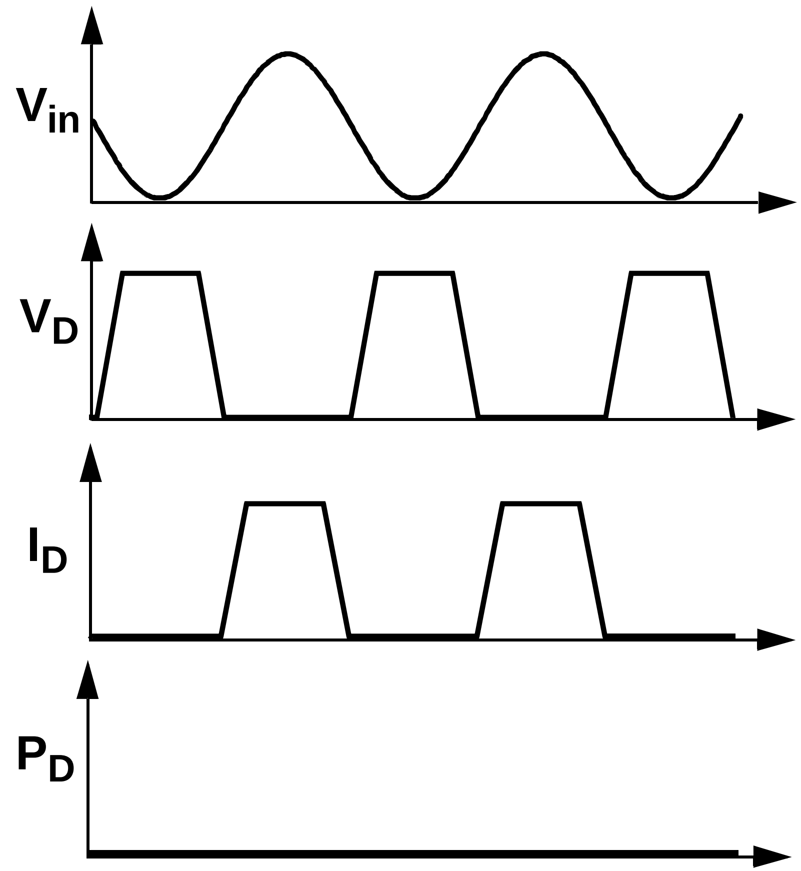
$$Psupply = I_{DC} x V_{DD} = \frac{VDD^2}{R_L}$$

$$Efficiency = \frac{Pout}{Psupply} \leq 50\%$$

$P_D = I_D \times V_D \downarrow \Rightarrow$ **Efficiency** $\uparrow$

Efficiency-Linearity Tradeoff



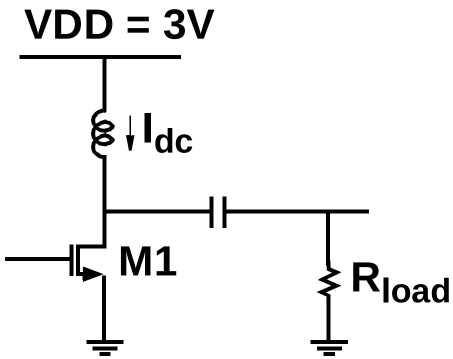


- Large input signal
- Square wave output I_D and V_D
- Non-overlapping I_D and V_D

$$\text{Pout} = \frac{\text{VDD}^2}{R_L}$$

$$P_D = 0 \Rightarrow \textbf{Efficiency} = 100\%$$

Low-Voltage Operation



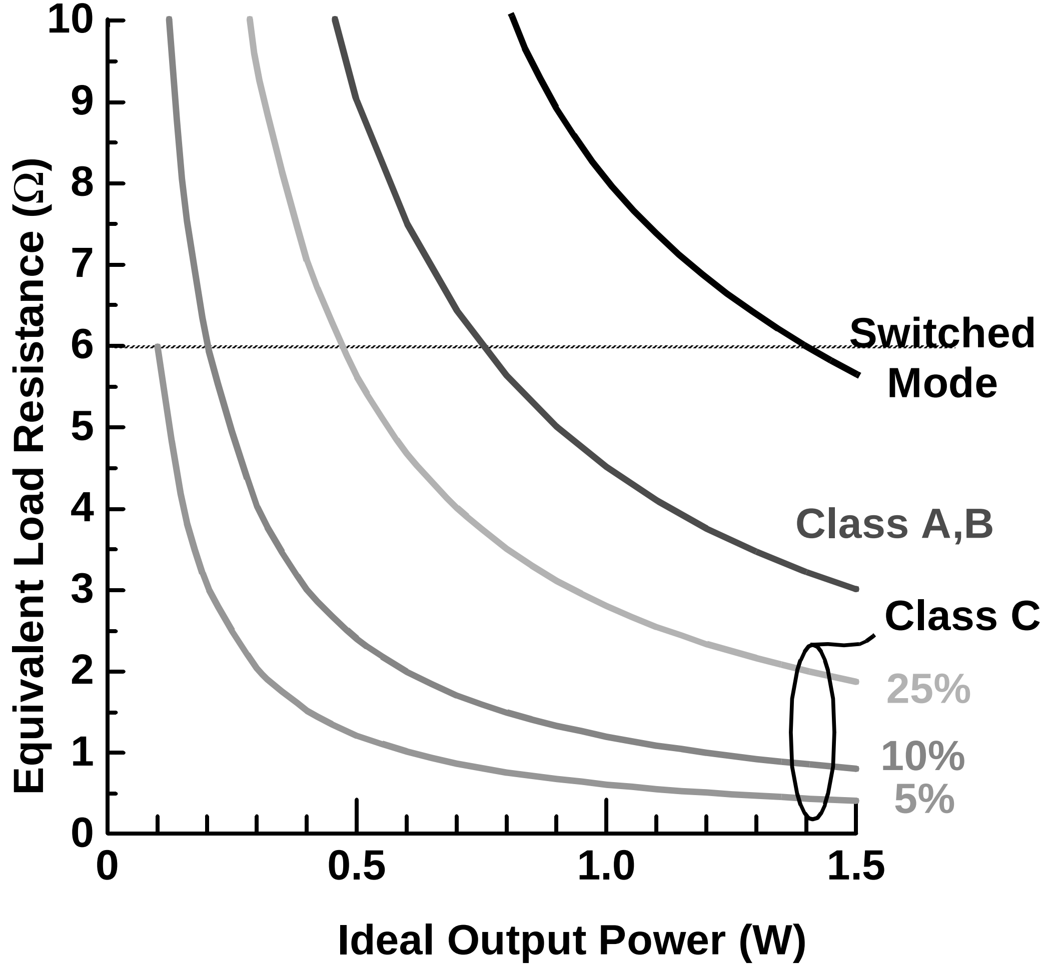
$$Pout \approx \frac{VDD^2}{nR_{load}}$$

$$R_{load} \approx \frac{VDD^2}{nPout}$$

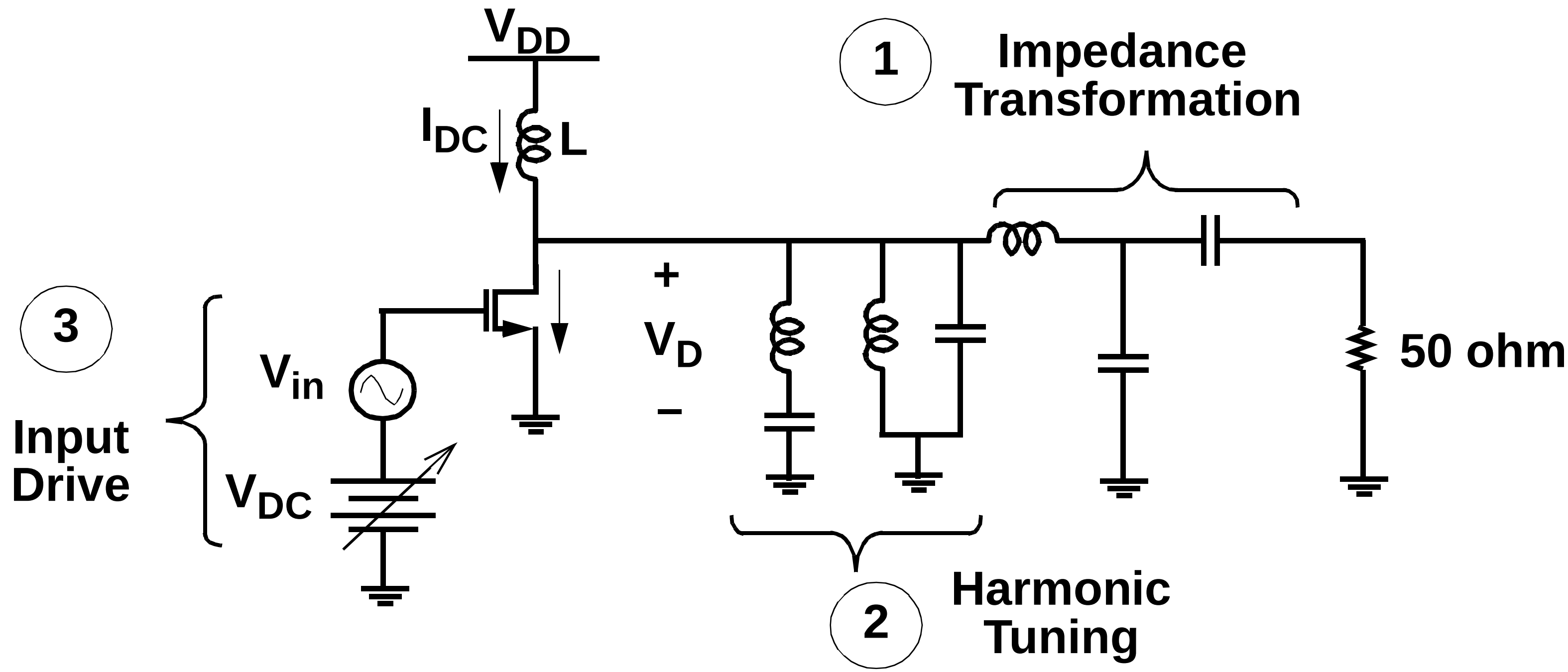
Switched-Mode: $n = 1$

Class A,B: $n = 2$

Class C: $n > 2$



Practical Power Amplifier Design



LOAD PULL Optimization

1. Impedance transformation: Output Power

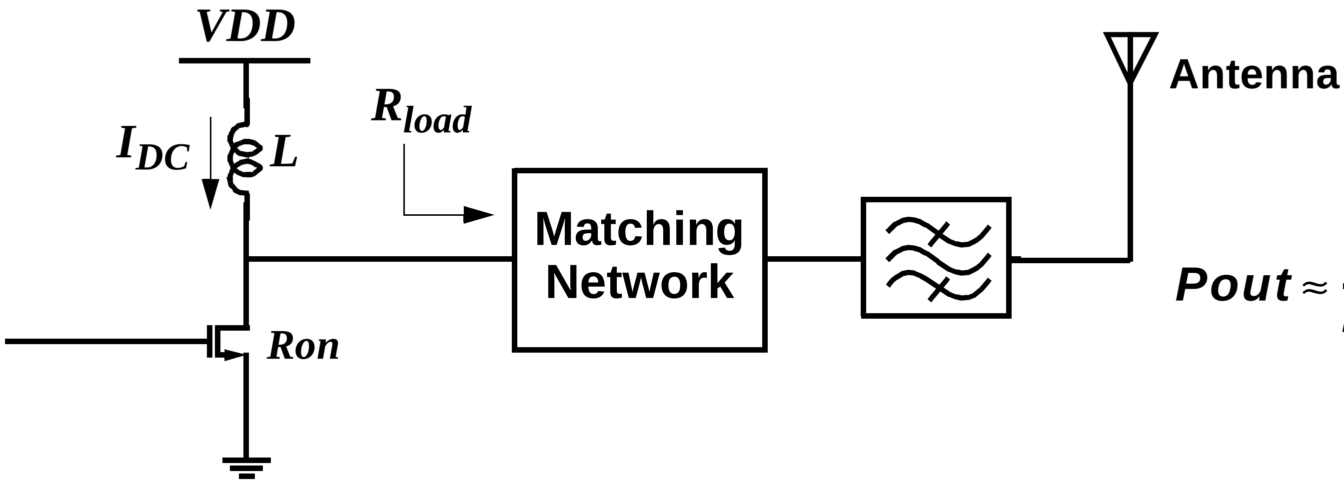
2. Harmonic Tuning: short @ 2fc & open@ 3fc for non-overlap I_D & V_D to maximize efficiency

3. Input drive: VDC -> Conduction Angle; Vin -> current source vs switch

Nonlinear Power Amplifier

- **Hewlett Packard Labs (with W. McFarland)**
- **800-MHz 32dBm AMPS PA with 42 % PAE in 0.8 μm CMOS**

Switched-Mode Design



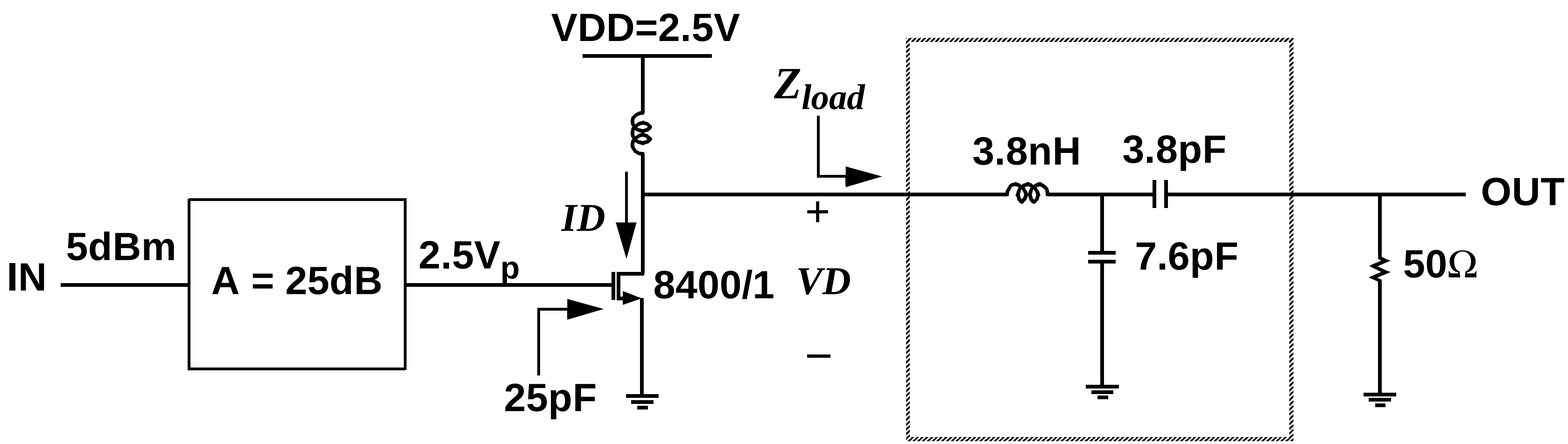
$$Pout \approx \frac{VDD^2}{nR_{load}}$$

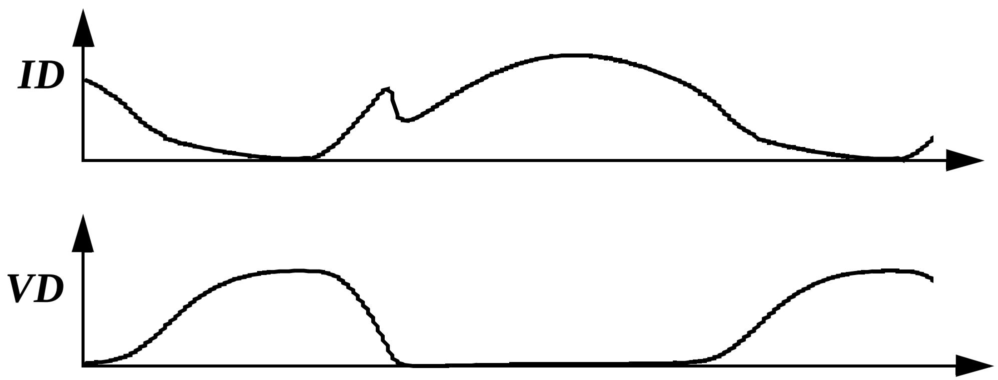
Choose n = 1.5 (assume 67% efficiency due to Ron > 0),
VDD = 2.5V,
For Pout = 1 W,

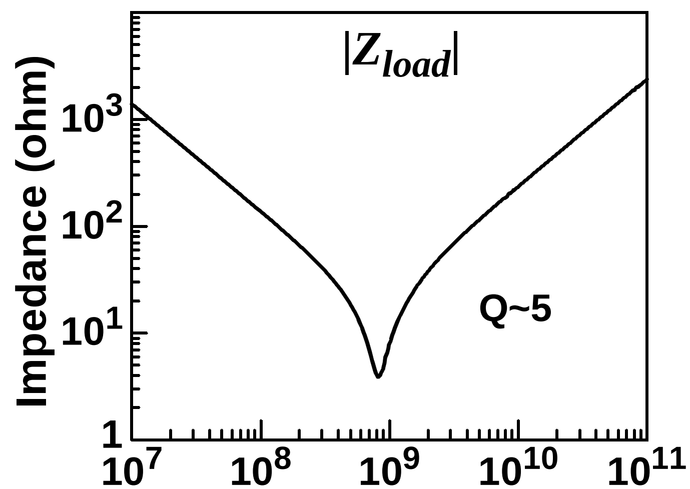
- **R_{load} = 4.2 Ω** [Pout = VDD^2/n R_{load}]
- **I_{DC} = 0.49A** [I_L (peak) = I_{DC} & Pout = 0.5 x I_{DC}^2 x R_{load}]
- **Ron = 1 Ω** [Assume no overlap; P_D = 0.5W = 0.5 x $(2\ IDC)^2$ x Ron]

⇒ **Output transistor sizing: Ron < 1 Ω**

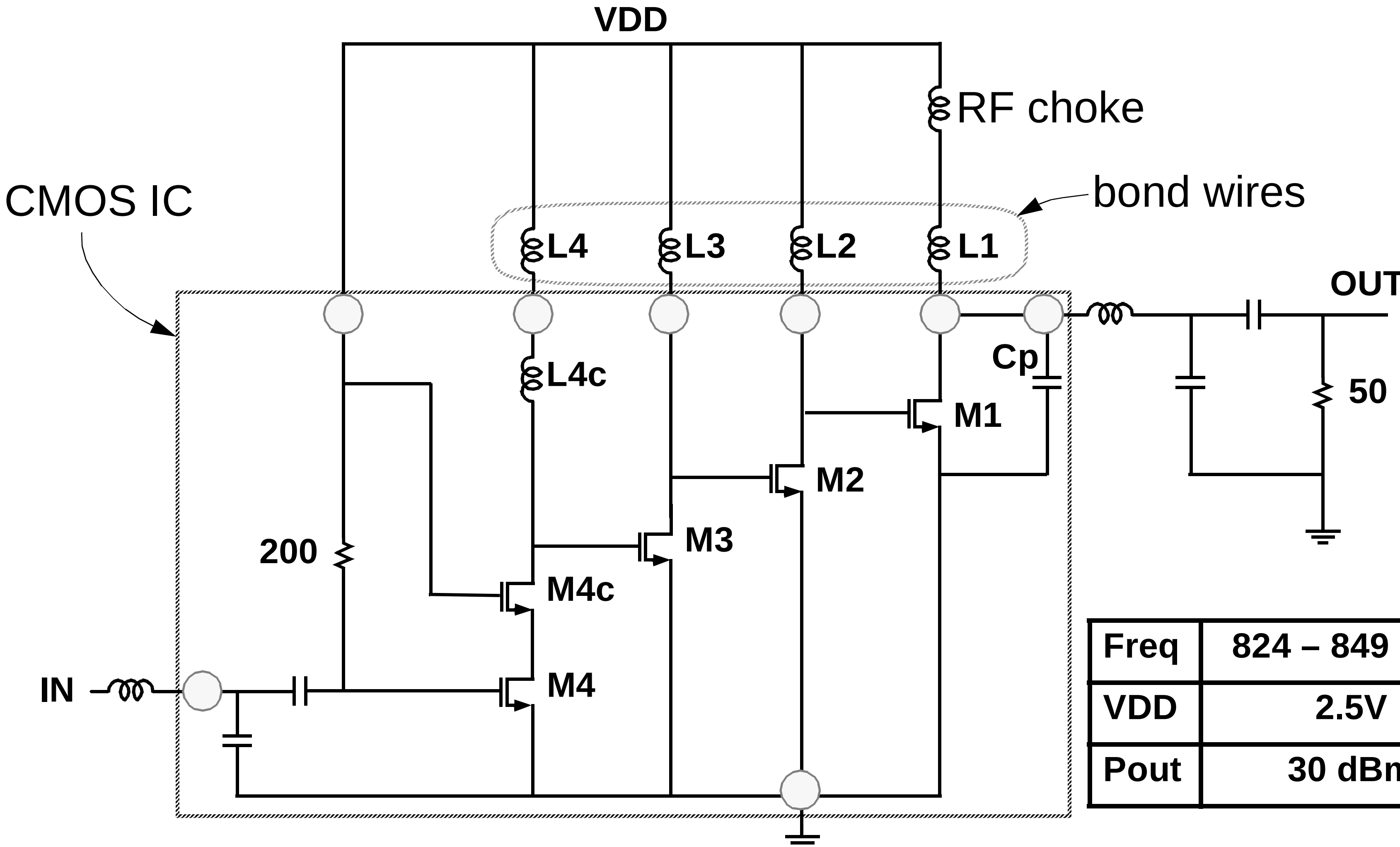
Output Stage Design







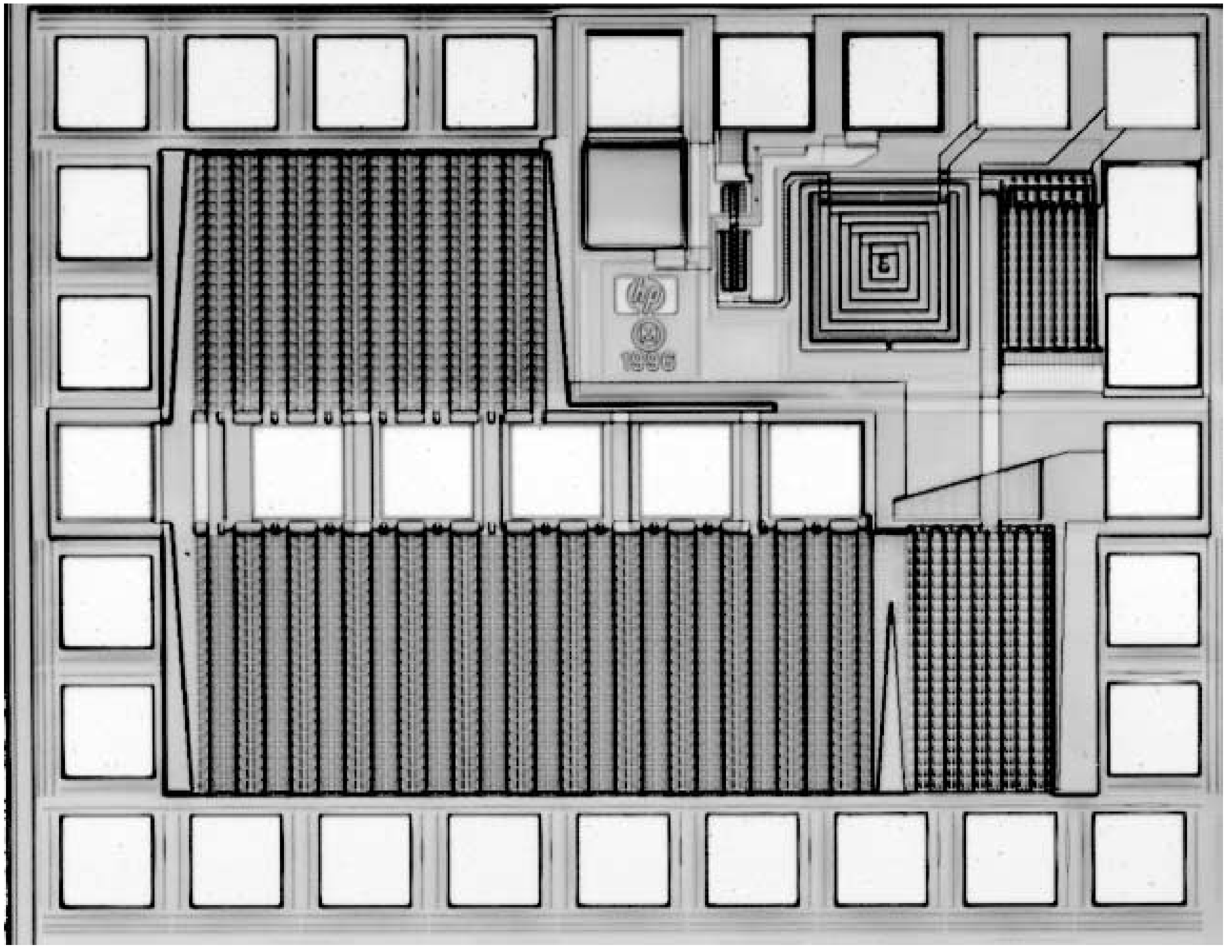
Complete Amplifier



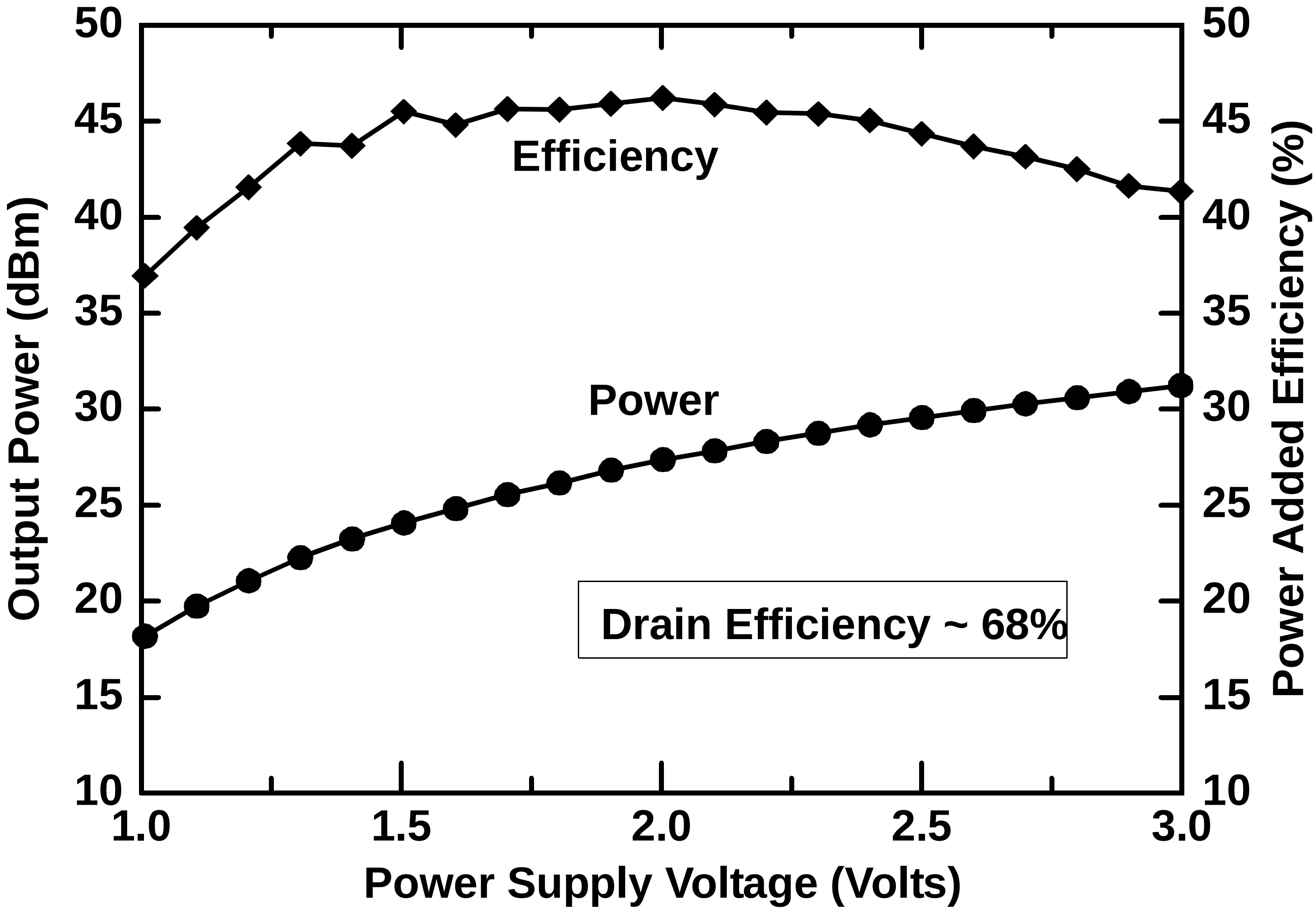
Freq	824 – 849 MHz
VDD	2.5V
Pout	30 dBm

Die Photo

0.8µm CMOS
1.5 mm^2



Measured P_{OUT} and Efficiency



Linear Power Amplifier

- Atheros Communications (with D. Weber et al)
- 5-GHz 18dBm OFDM PA for IEEE 802.11a in 0.25 μm CMOS

Spectral-Efficient Modulation

- **64-QAM (Quadrature Amplitude Modulation)**
  — Large signal to noise ratio > 30dB

- **OFDM (Orthogonal Frequency Division Mux)**
  — Large peak to average power ratio of $\sqrt{52}$ or 17dB

→ Requires High Linearity in PA

Power Amplifier Design

- Large peak to average ratio (PAR) of $\sqrt{52}$ or 17dB
- Signal peaks are infrequent: 0.25dB SNR degradation when PAR reduced to 6dB for 16-QAM*.
- Implications:
  - Poor power efficiency
  - With 6dB PAR, to obtain 40mW (16dBm) requires Psat of ~22dBm or 160mW
  - With 17dB PAR, to obtain 40mW (16dBm) requires Psat of ~33dBm or 2W

*Van Nee & Prasad, OFDM for Wireless Multimedia Communications, Artech House, 2000

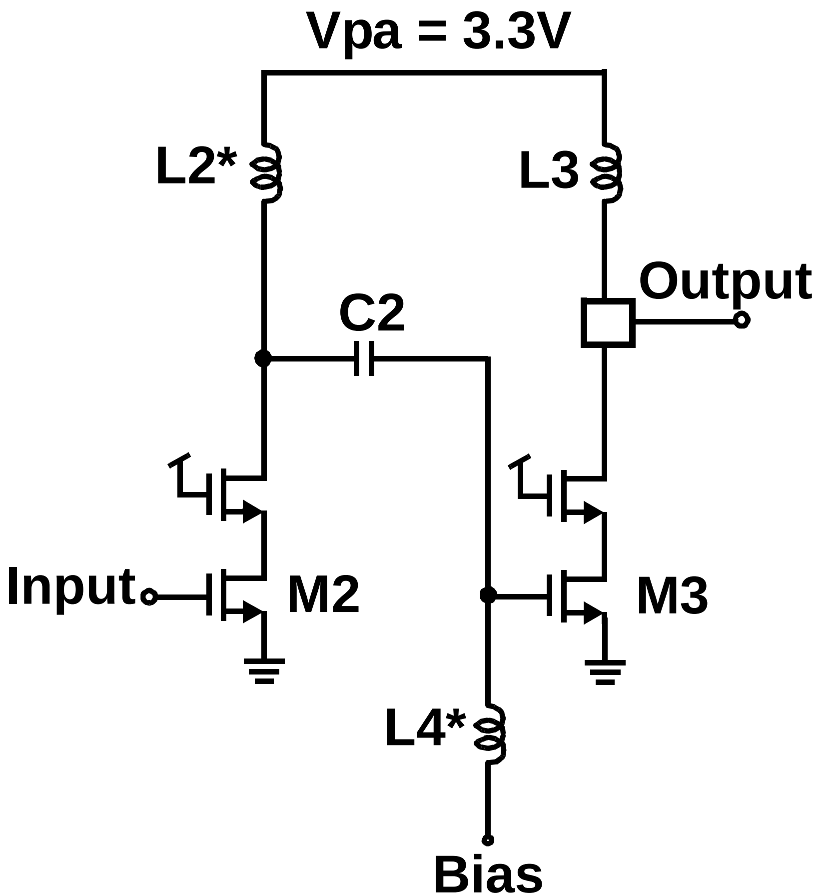
Linear PA makes efficient radios

- **Frequency bandwidth is precious**
  --> Maximize network capacity
- **Energy/bit (battery life)**
  More bits sent per second
  --> PA + the rest of the radio
  are ON for shorter duration

Linear PA Design

- Input load impedance
  - signal dependency
  - cascode
- V_{GS} overdrive
  - dc bias with capacitive level-shift
- Output load impedance
  - impedance matching network
- Stability
  - cascode

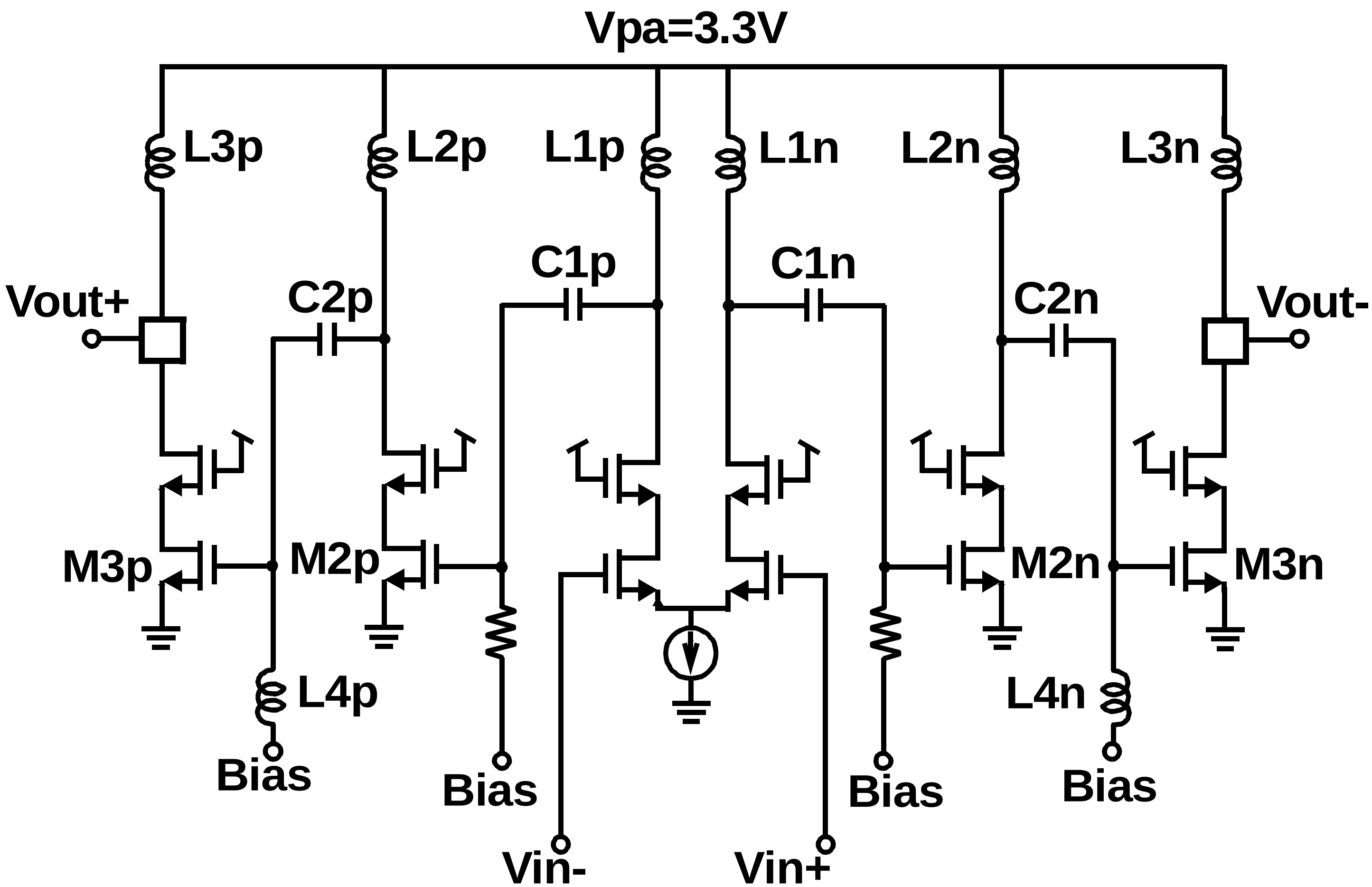
Power Amplifier Topology



- Class A operation
- Cascoded
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
  - Metal-2,3,4,5 stacks
- Inductive loads
- Differential
  - Off-chip balun

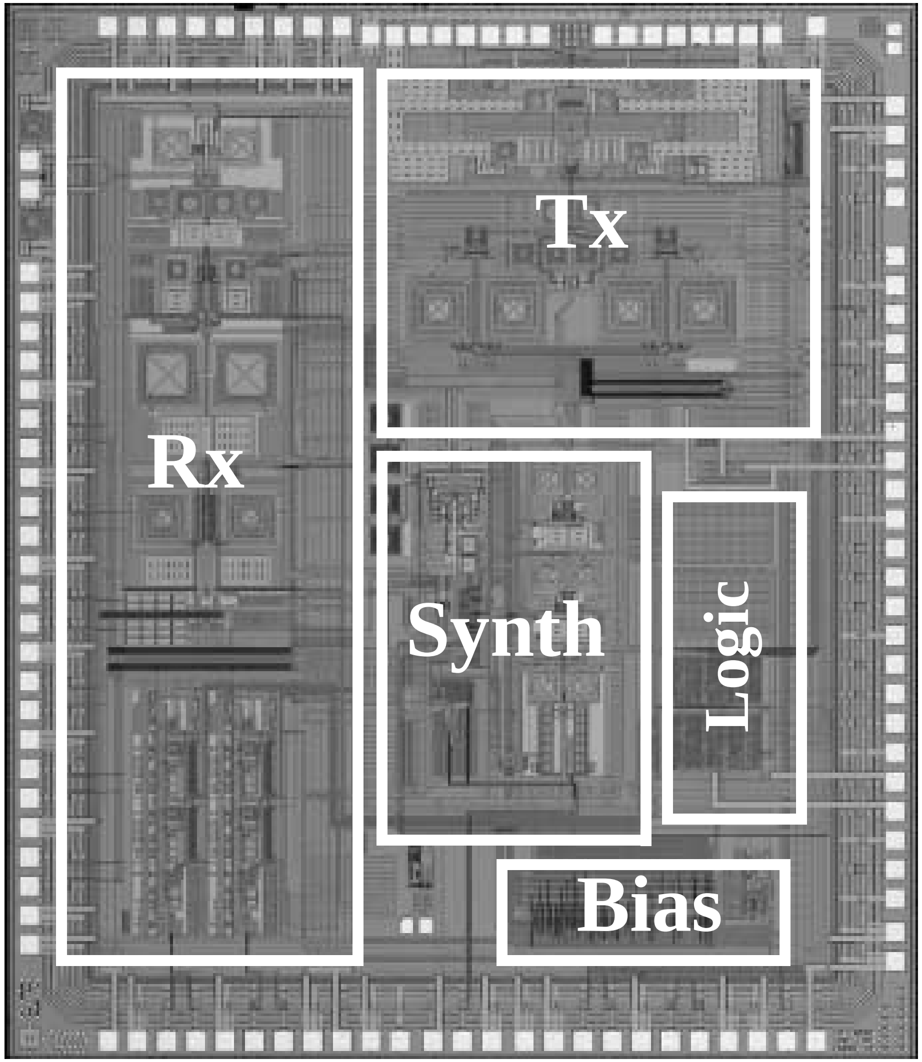
* C.P. Yue and S.S. Wong, IEEE JSSC, May 1998

Power Amplifier Schematic

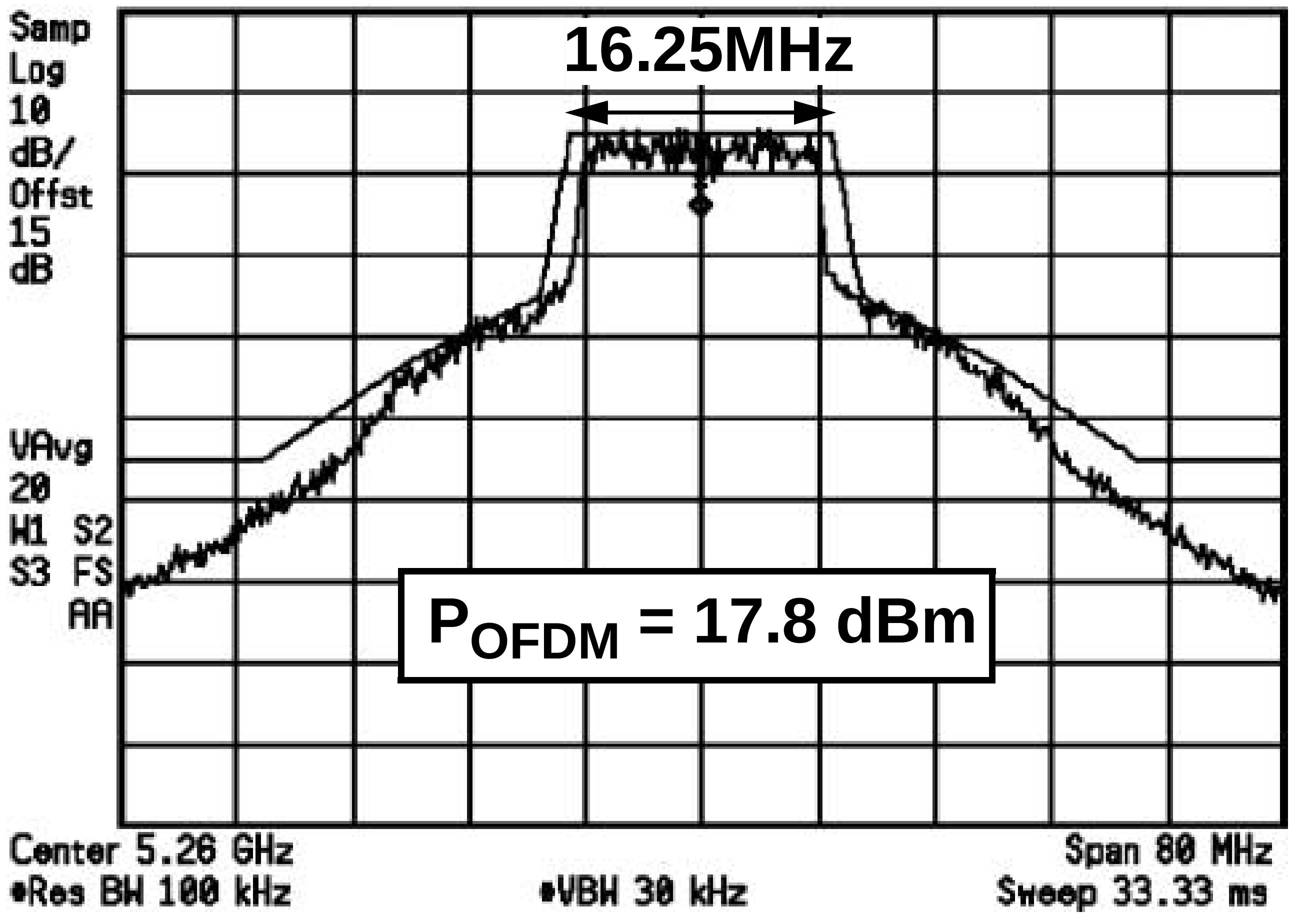


P_{SAT} = 22 dBm

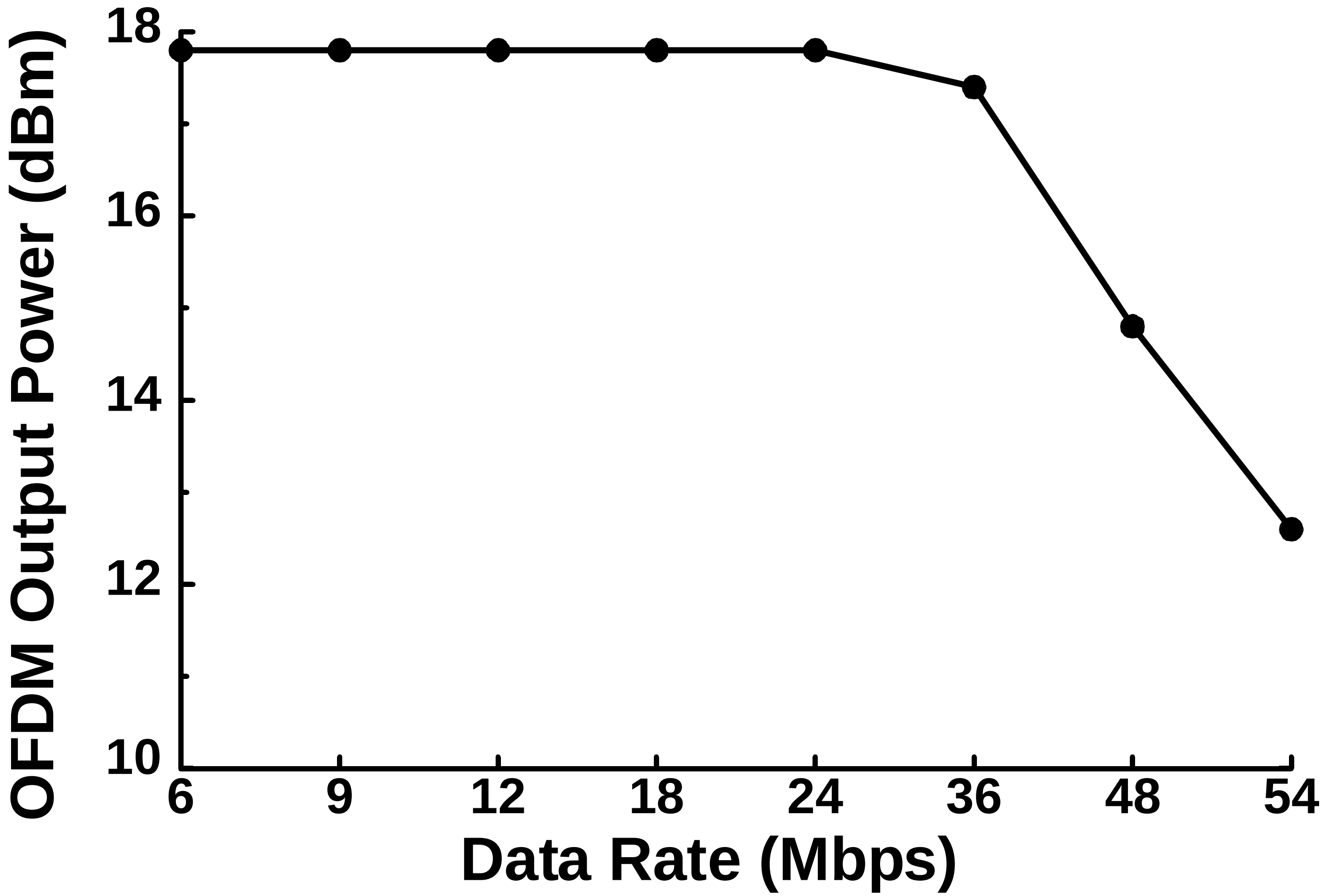
Die Photograph



Measured BPSK OFDM Spectrum



Measured Transmit Output Power



Linearized Power Amplification

- Hewlett Packard Labs
  (with W. McFarland)
- Linearization IC for NADC with efficiency improvement from 36% to 49% using envelope elimination and restoration

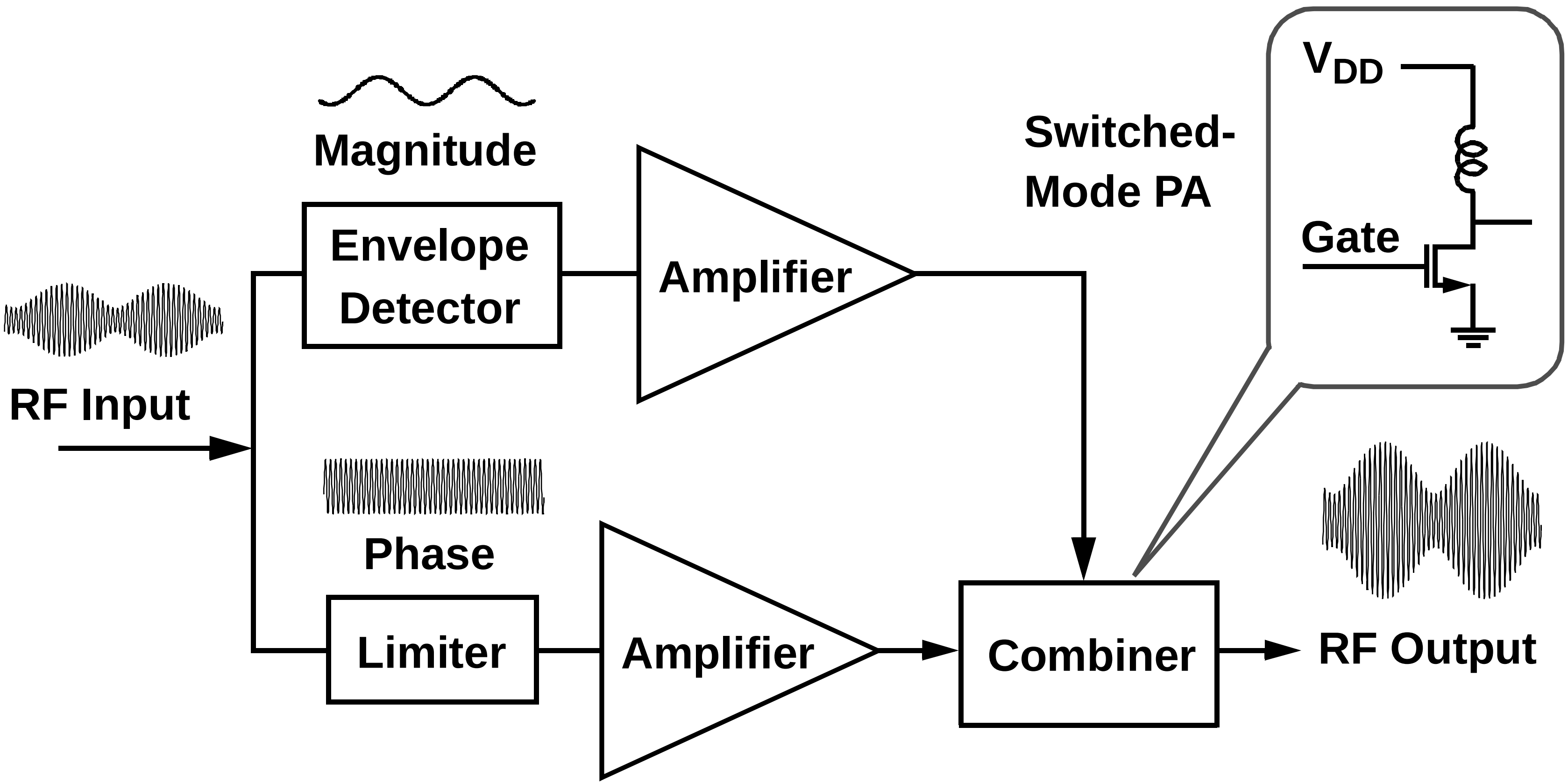
Applying Integration to RF PA

Transistors are *cheap.*

- **LARGE Output Power: Use switched-mode output stage**
- **HIGH Efficiency: Use switched-mode output stage**
- **GOOD Linearity: Use linearization circuits so that the output stage does not need to be linear.**

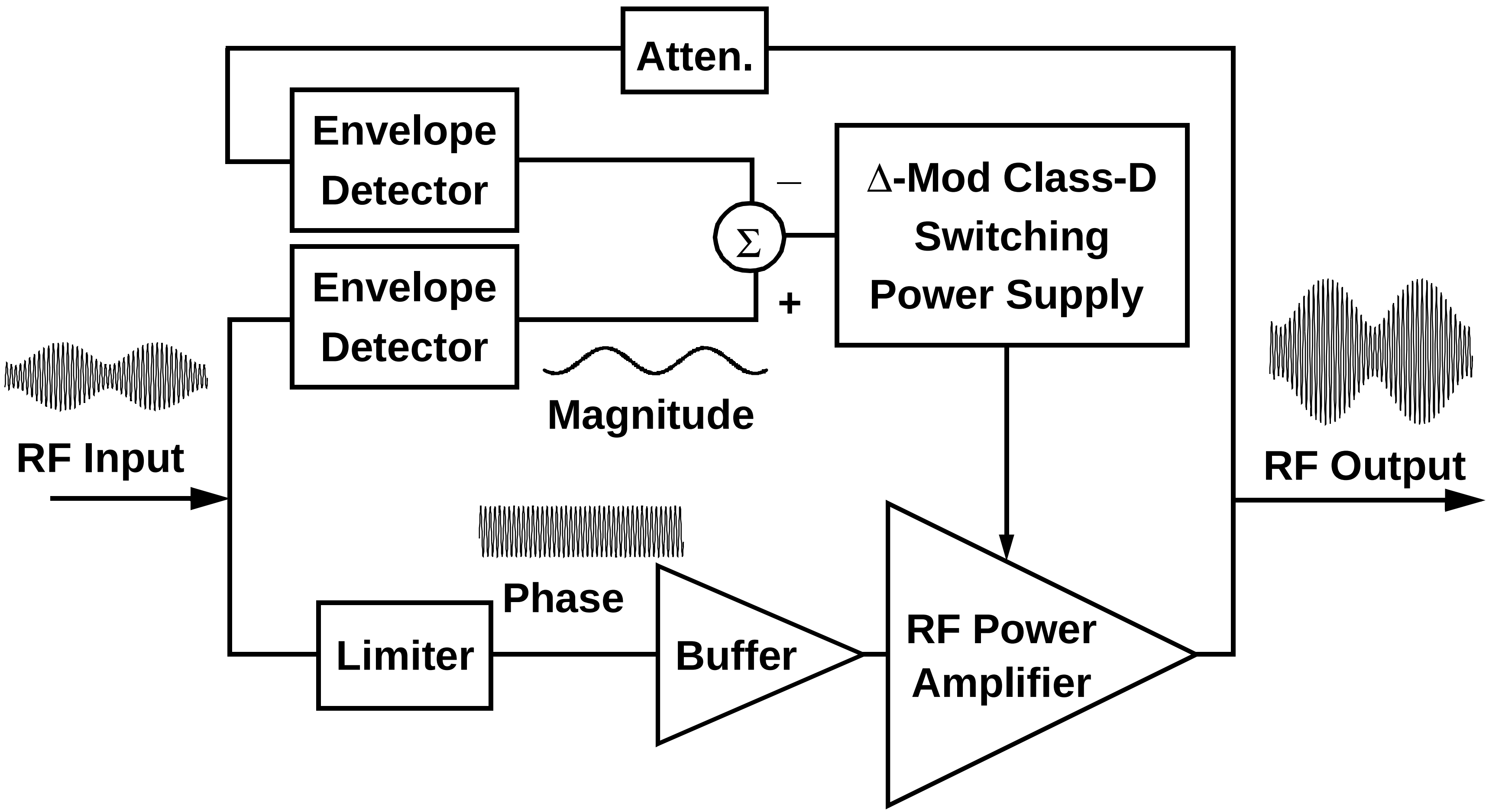
SOLUTION: Switched-mode output stage + linearization.

Envelope Elimination and Restoration

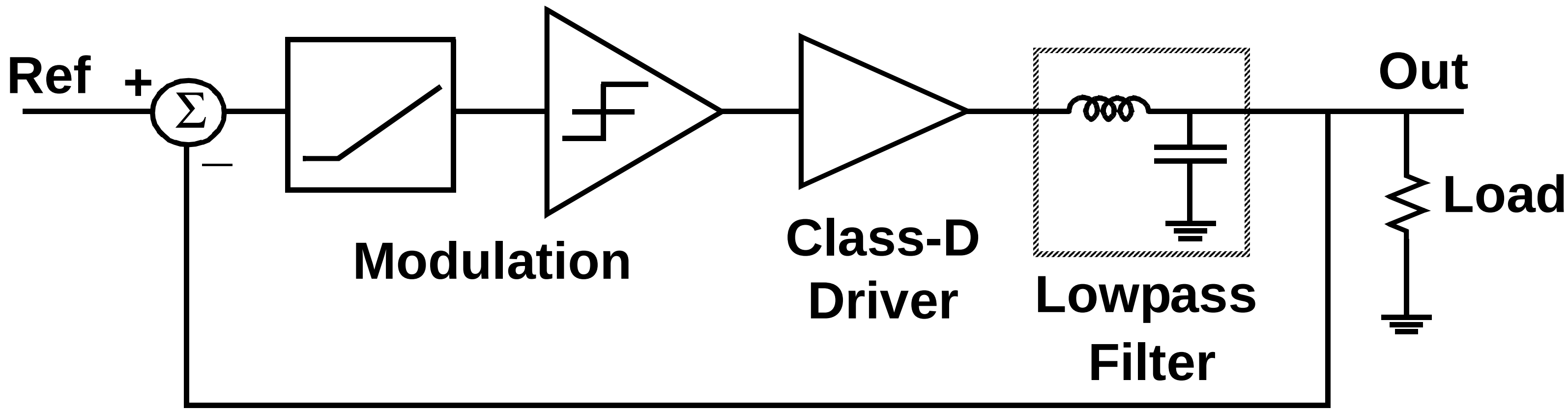


Ref: L. Kahn, Proc IRE, July 1952

Closed-Loop EER Implementation

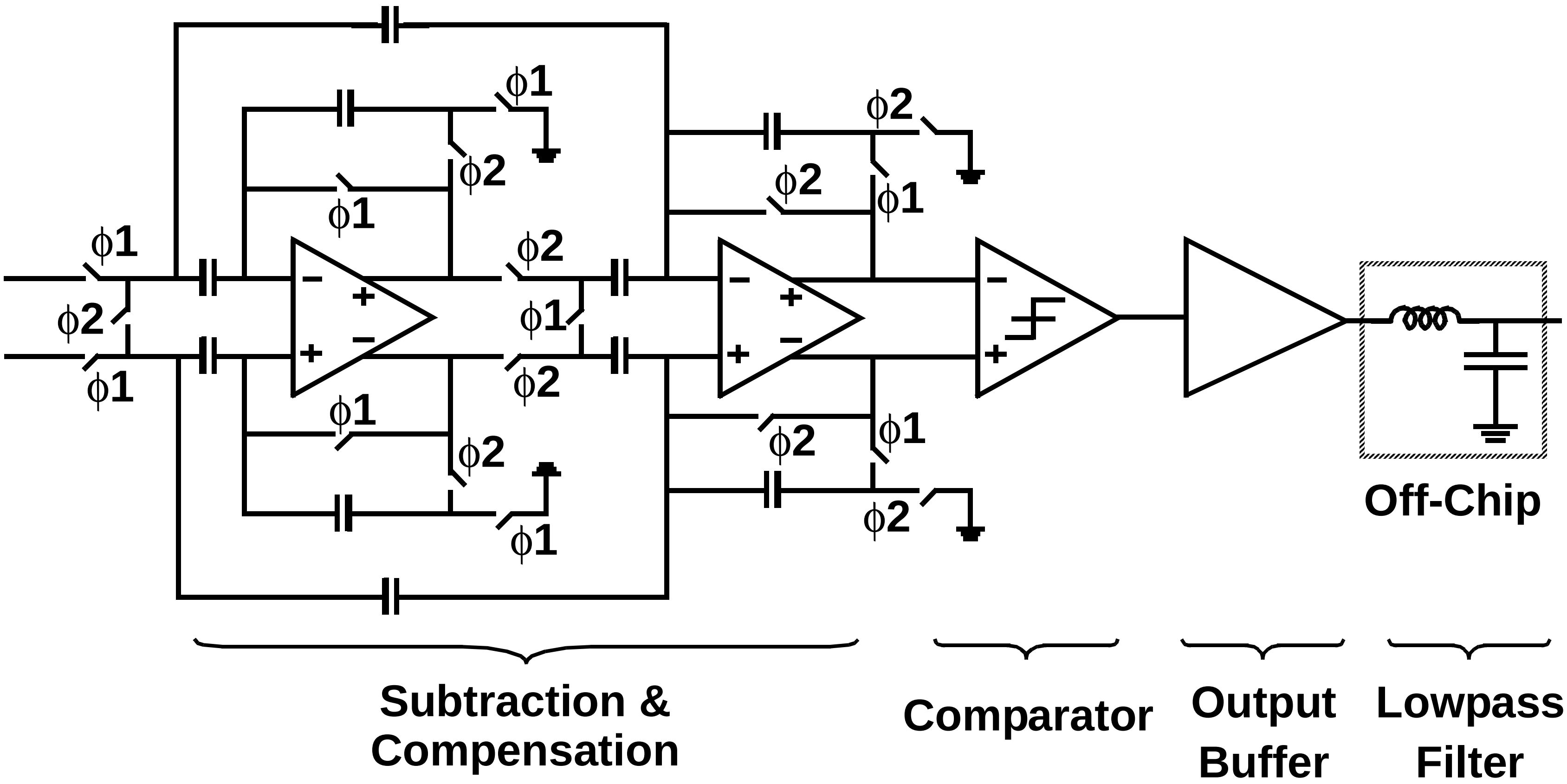


Δ-Modulated Switching Power Supply

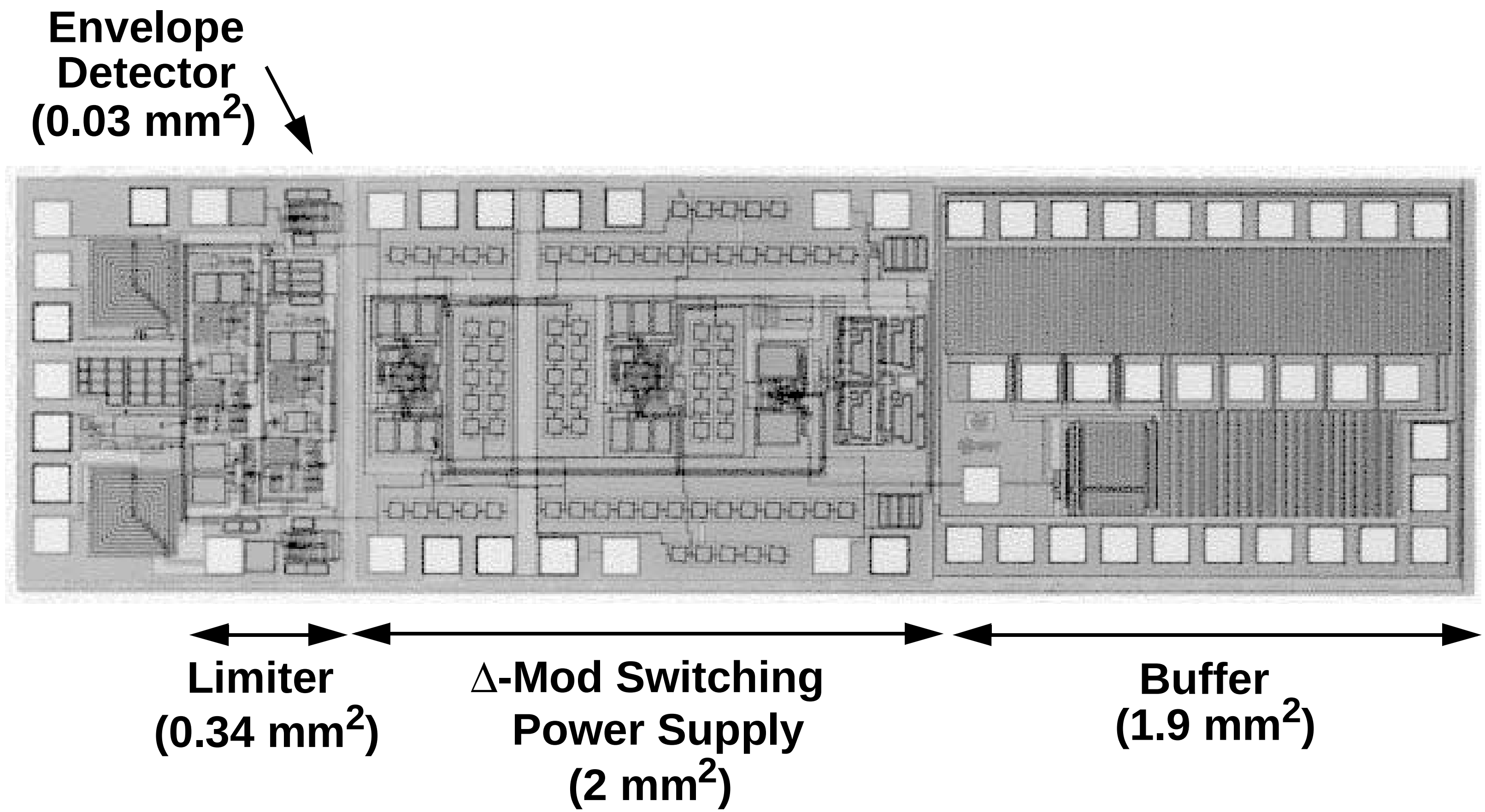


- Closed-loop system
- Modulation to generate a two-level output
  - ⇒ Pulse width modulation vs. Delta modulation
- Efficient Class-D driver

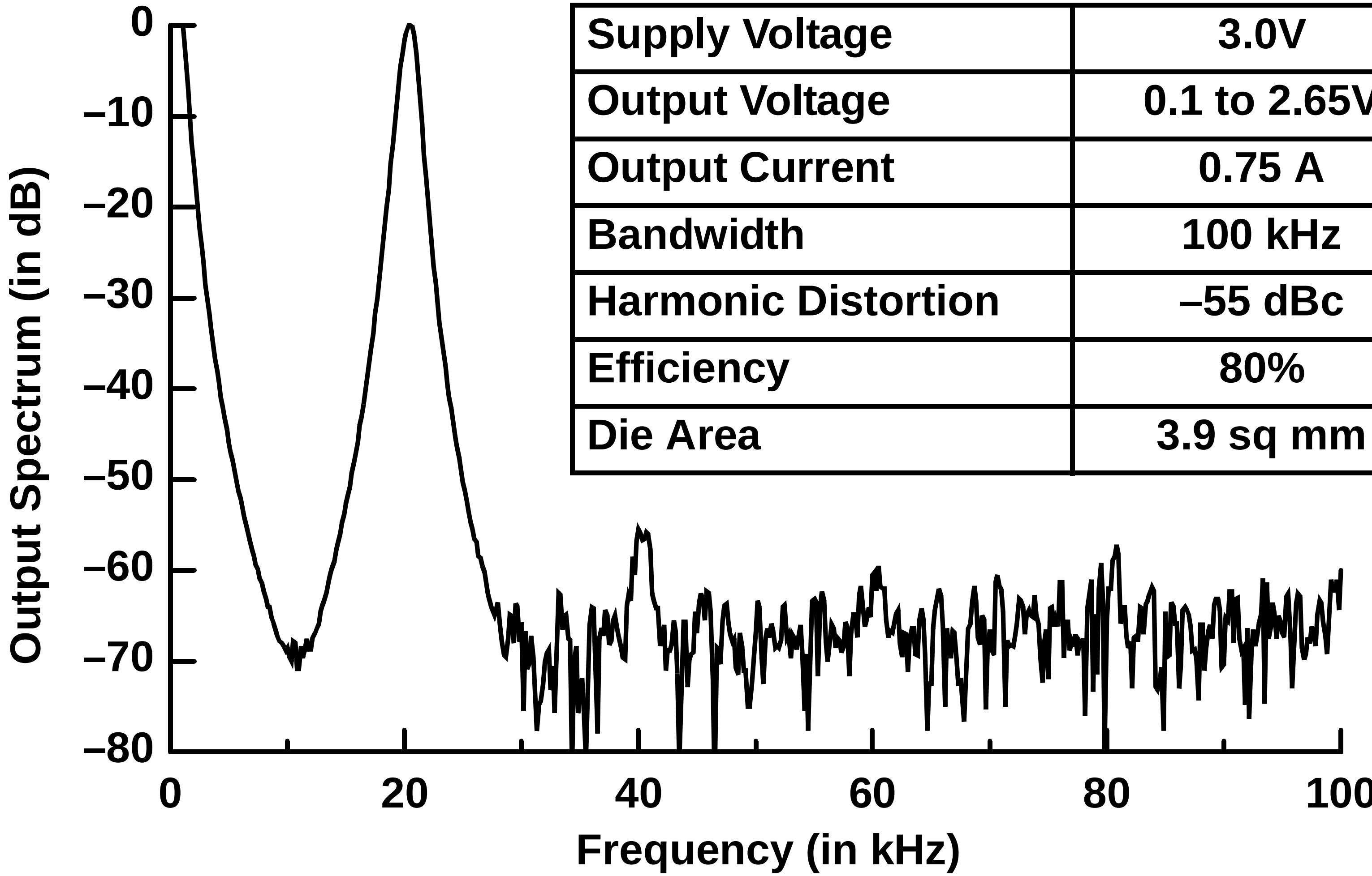
Switched-cap Circuit for Δ Modulation



Die Photograph

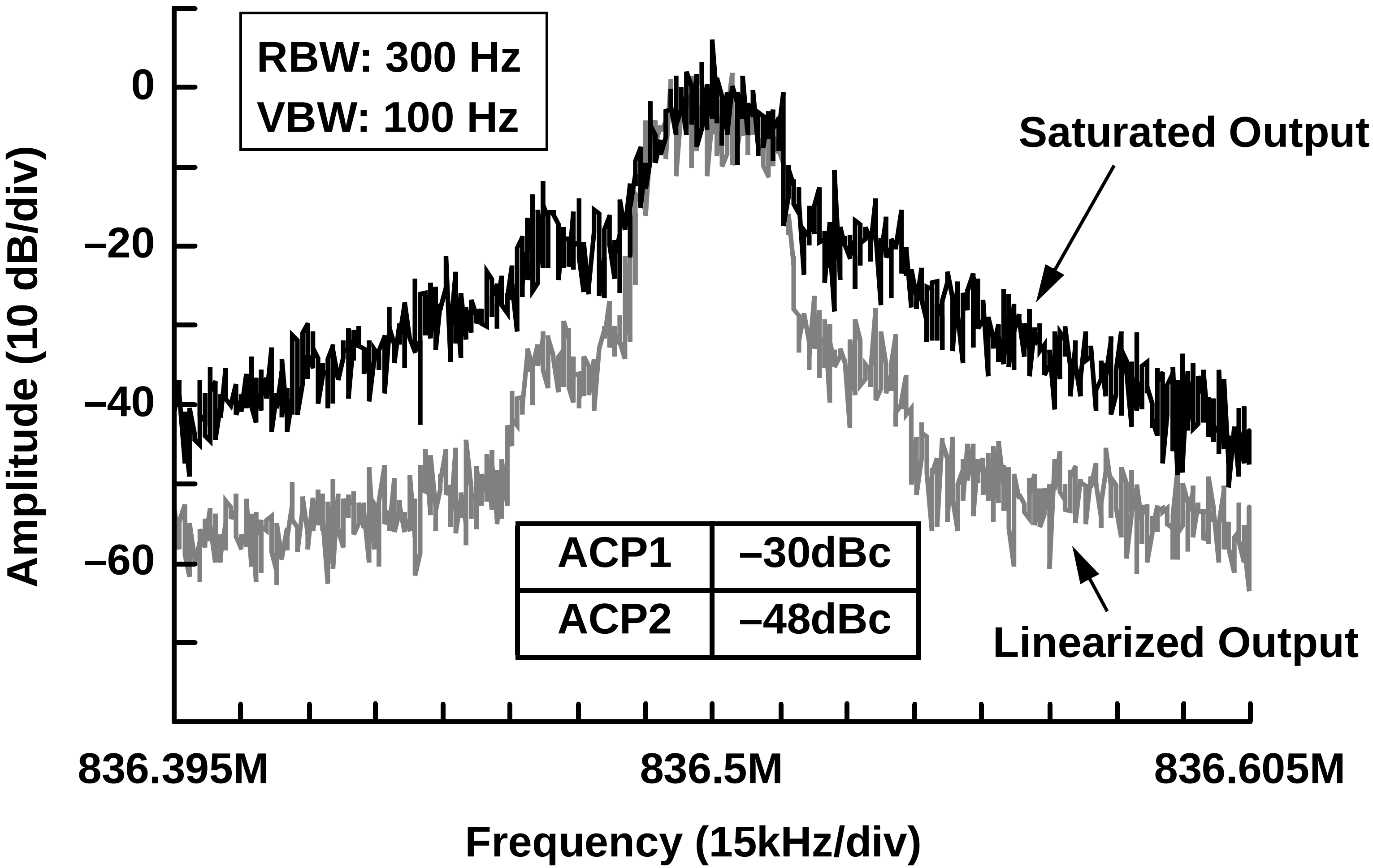


Switching Power Supply

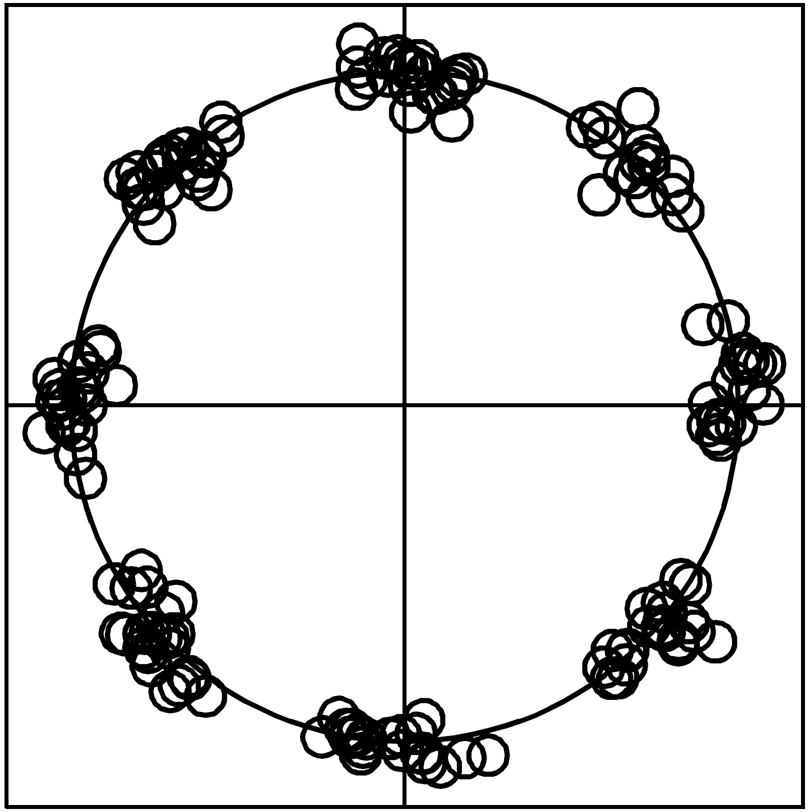


Supply Voltage	3.0V
Output Voltage	0.1 to 2.65V
Output Current	0.75 A
Bandwidth	100 kHz
Harmonic Distortion	–55 dBc
Efficiency	80%
Die Area	3.9 sq mm

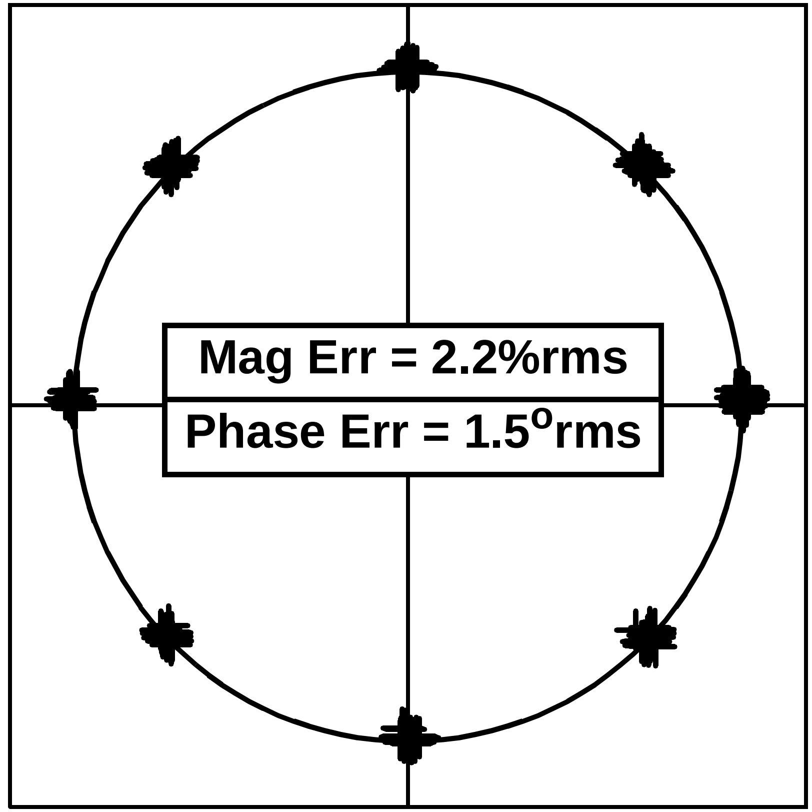
Spectral Mask of CMOS PA



π/4 QPSK Constellation of CMOS PA

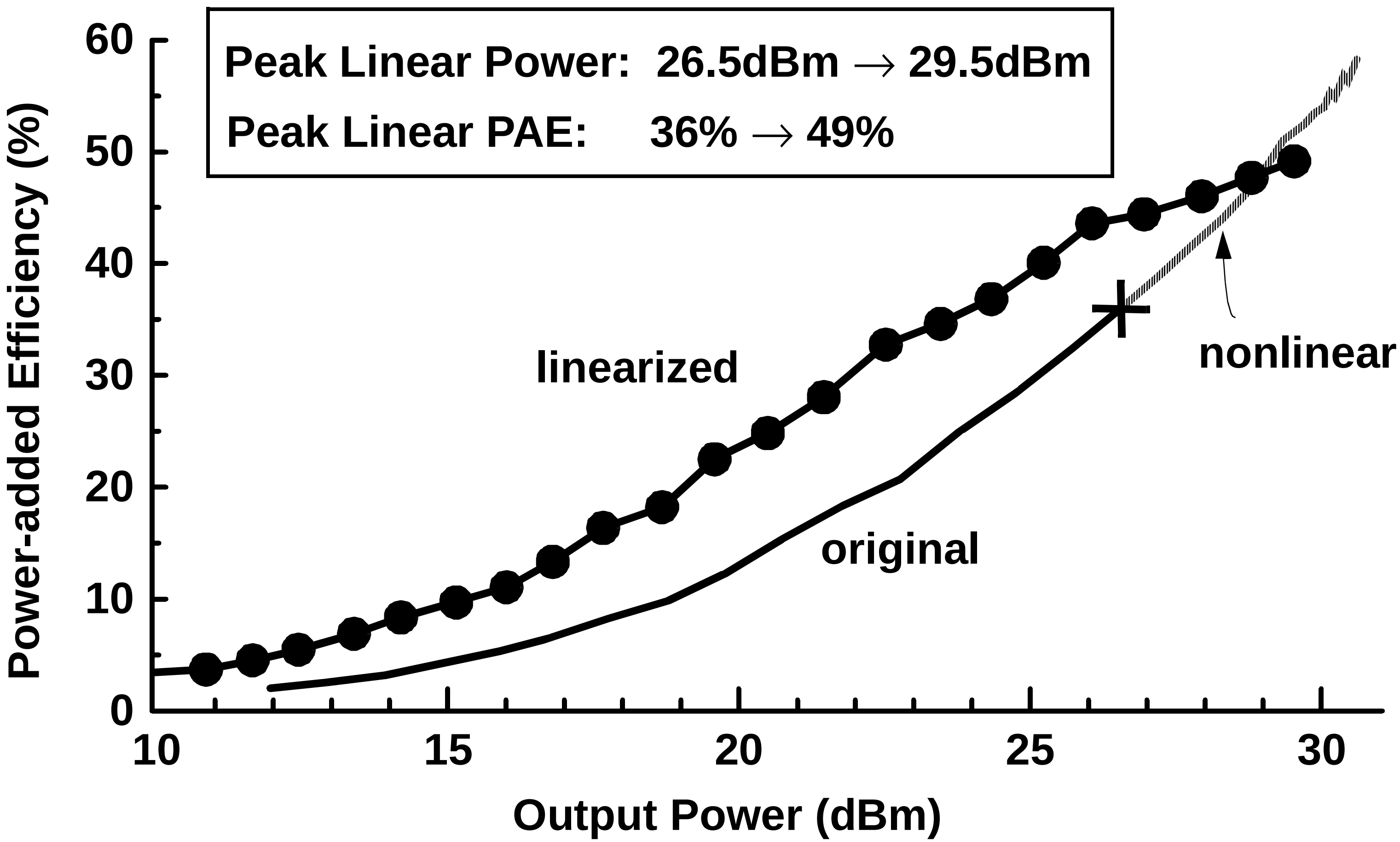


Without Linearization



With Linearization

Efficiency of 4.8-V GaAs PA



Conclusion

- Nonlinear (switched-mode) PA provides
  (+) large output power and high efficiency
  (–) poor linearity
- Linear PA provides
  (+) linearity, spectral efficiency
  (-) poor efficiency
- Linearization using envelope elimination and restoration
  (+) linear RF output + high efficiency
  (-) implementation complexity