A Very Low Power CMOS Mixed-Signal IC for Implantable Pacemaker Applications

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Questions:

(1) What year was the 1st pacemaker introduced?

(2) How many transistors are there in the 1st pacemaker?

(3) How many transistors are there in today's (2004) pacemaker?

Outline

- Overview of Cardiac Pacemaker
- Overview – Sensing
- Overview – Output Therapy System
- Overview – Battery Management System
- Overview – Low Power Logic Design
- Overview – Low Power Memory Design
- Overview (MEMS) – Activity Sensor
- Overview (MEMS) – Magnet Sensor
- Silicon Results

Overview of Cardiac Pacemaker – What is it?

Cardiac Pacemaker System

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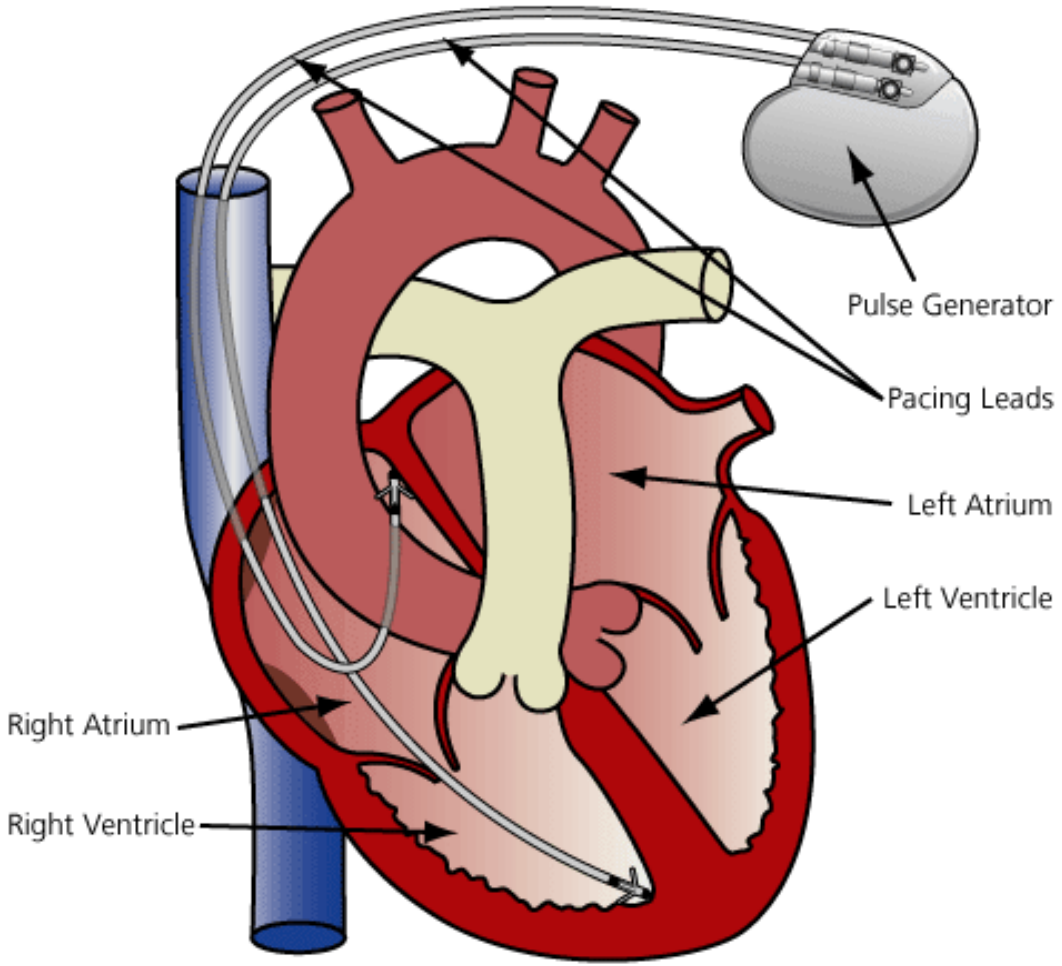
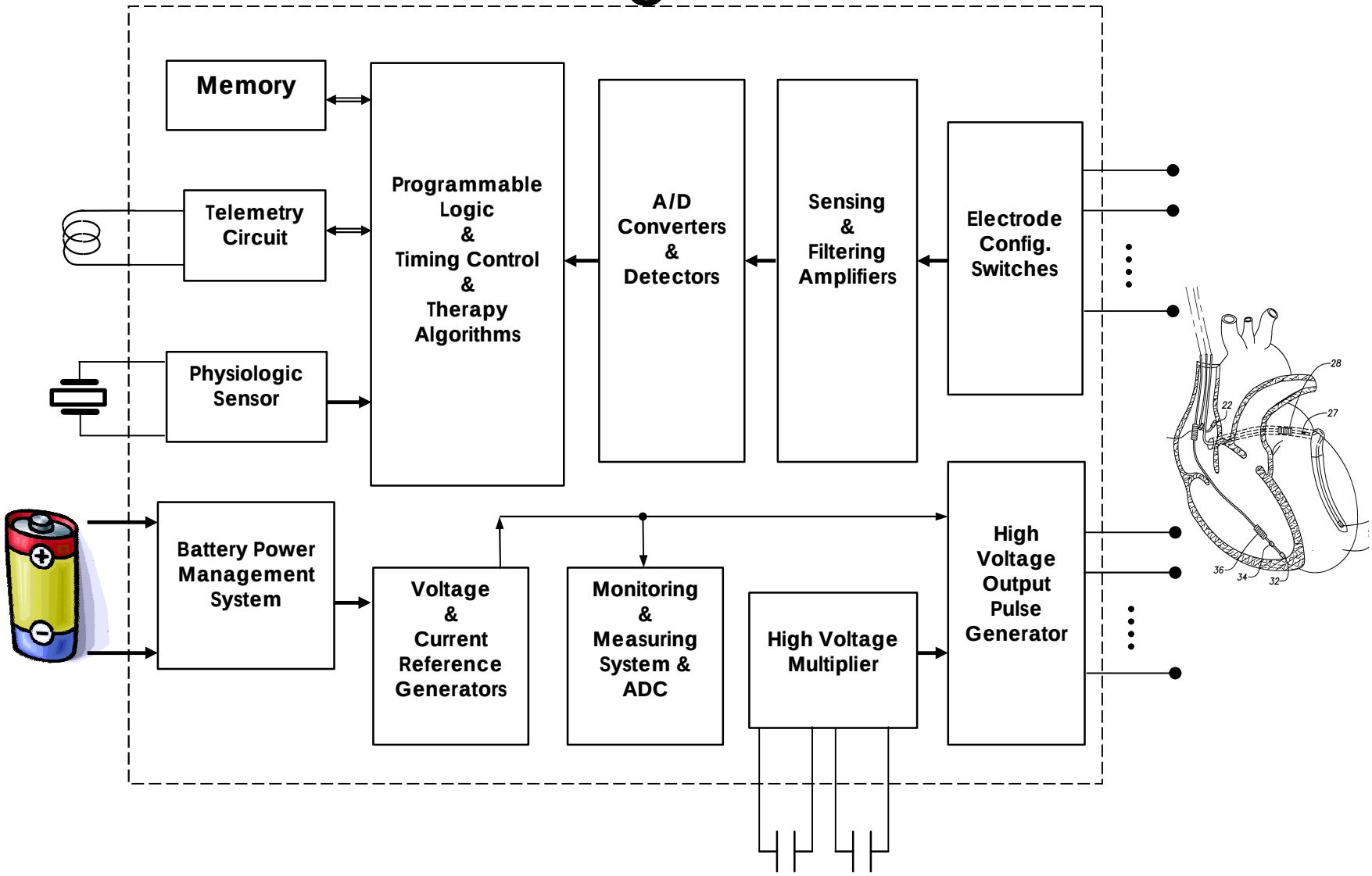


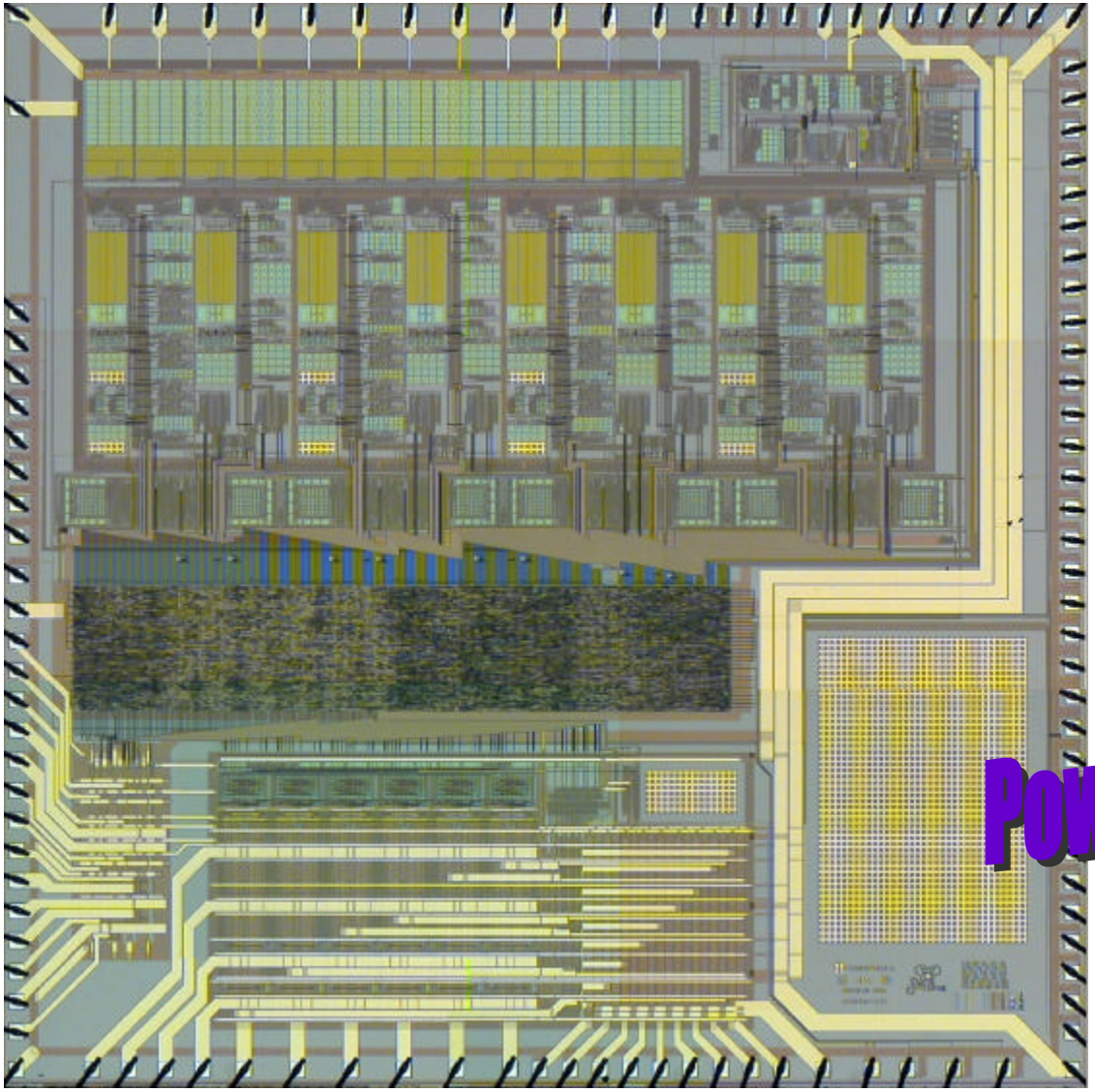
2 inch

Picture of an actual Implantable Pacemaker

Pacemaker – Simplified Block Diagram



Die Photograph

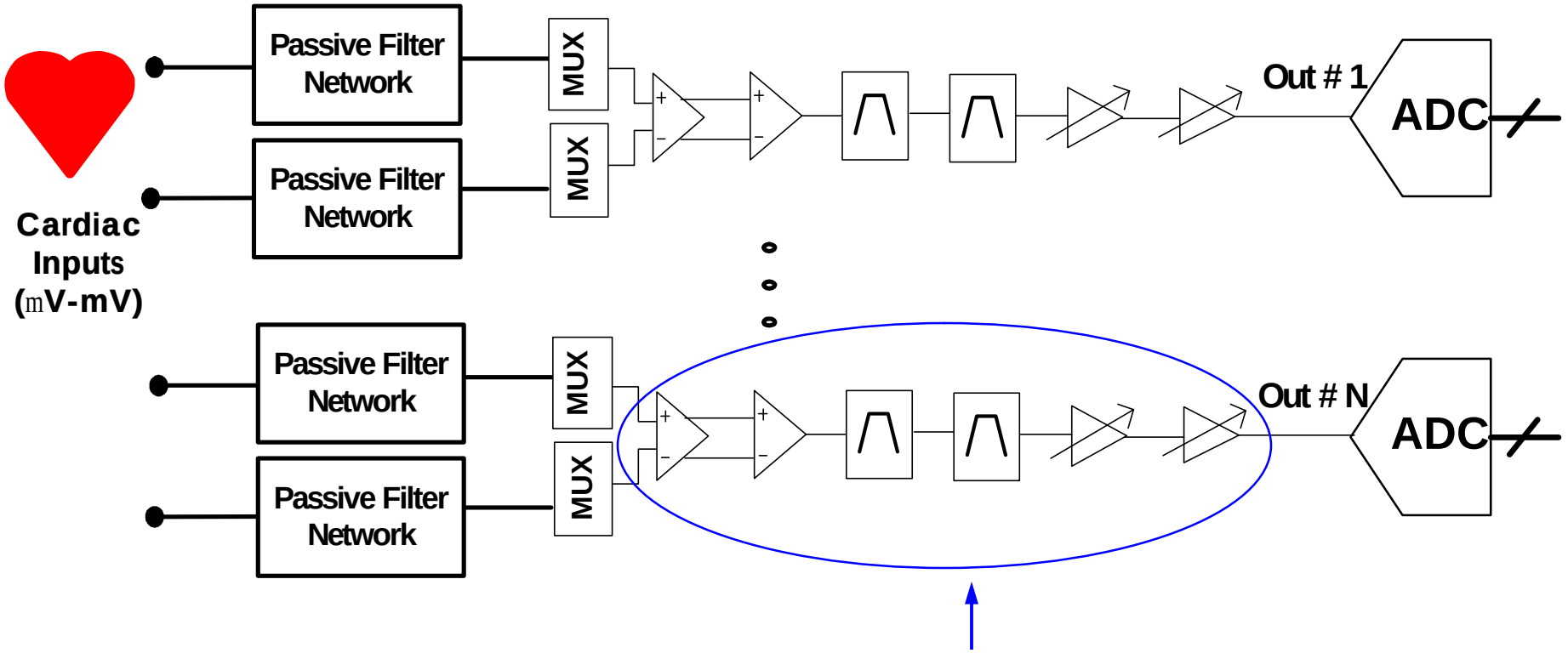


Power ~ 8uW

7000㎛

Overview of Cardiac Pacemaker – Cardiac Sensing System

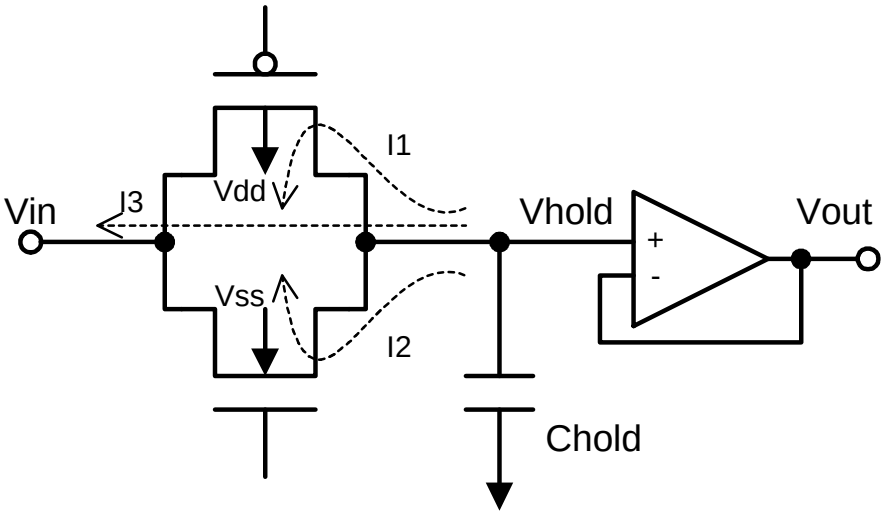
Sensing System Block Diagram



Low Power SC Circuits - Problem

Illustrated by a SC SH amplifier:

- Residual leakage current (~pA) when CMOS switch is off
- Cardiac/Neuro-signals have low frequency content ~0.1Hz
- Signal amplitude of interest ~µV-mV

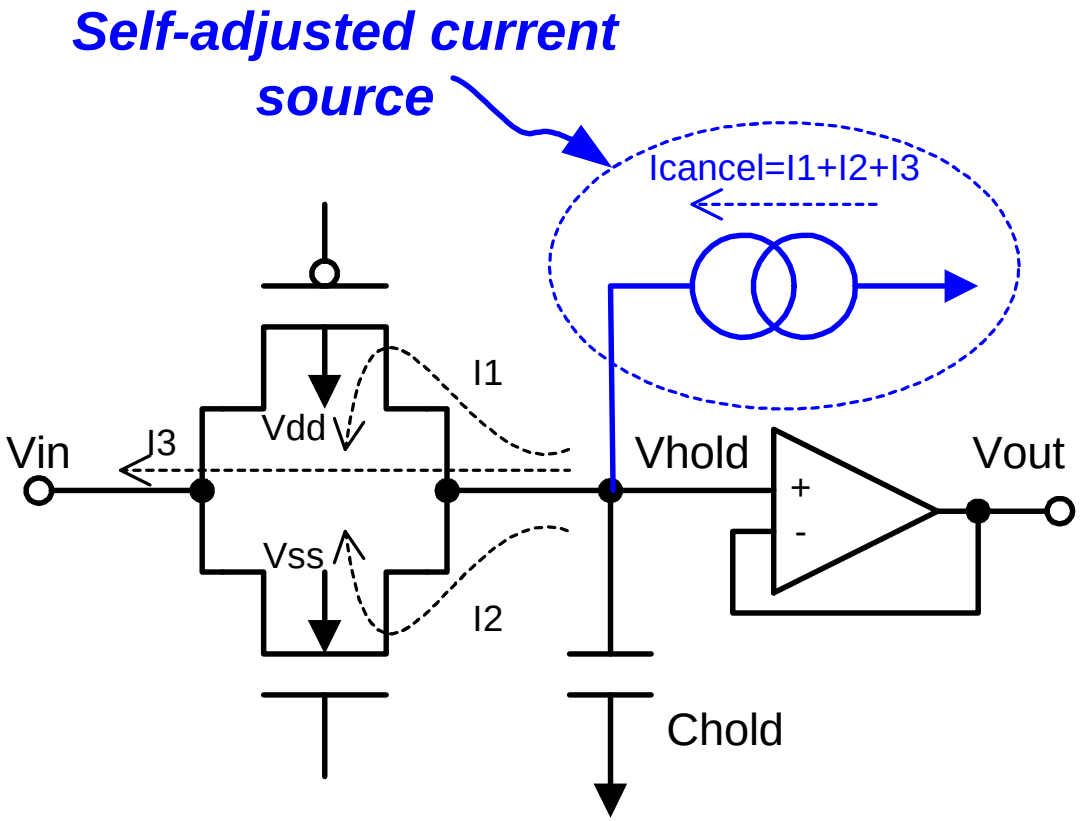


A "Sample-hold Amplifier" used to illustrate the problem

If leakage=1pA, Chold=1pF, hold time=100mS, then

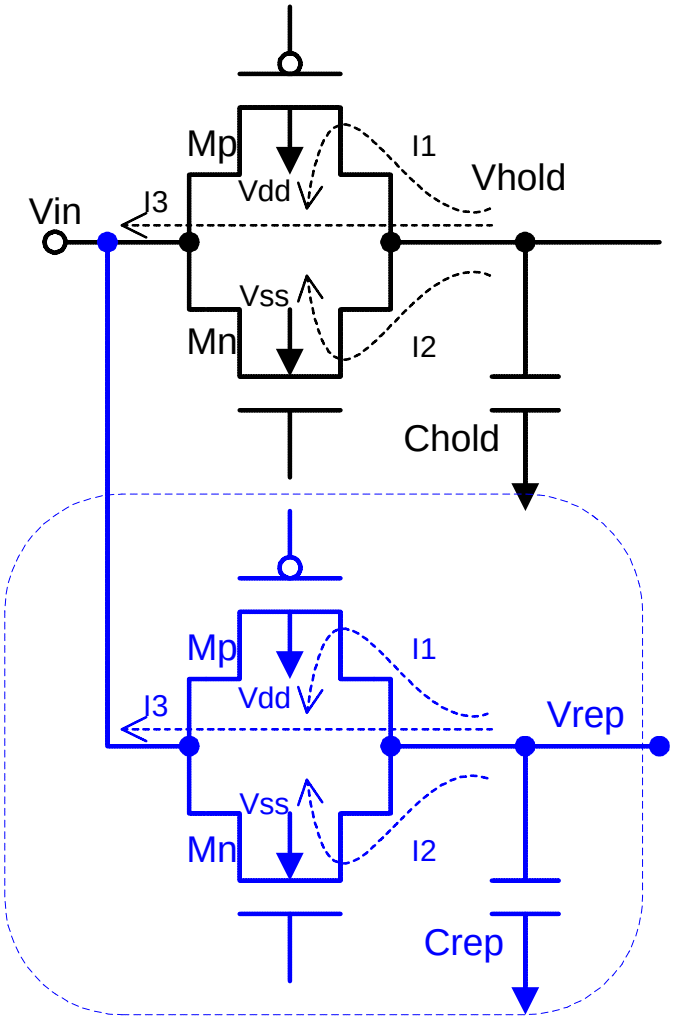
Vout drift = 100mV (Unacceptable)

Leakage Cancellation Technique - Concept



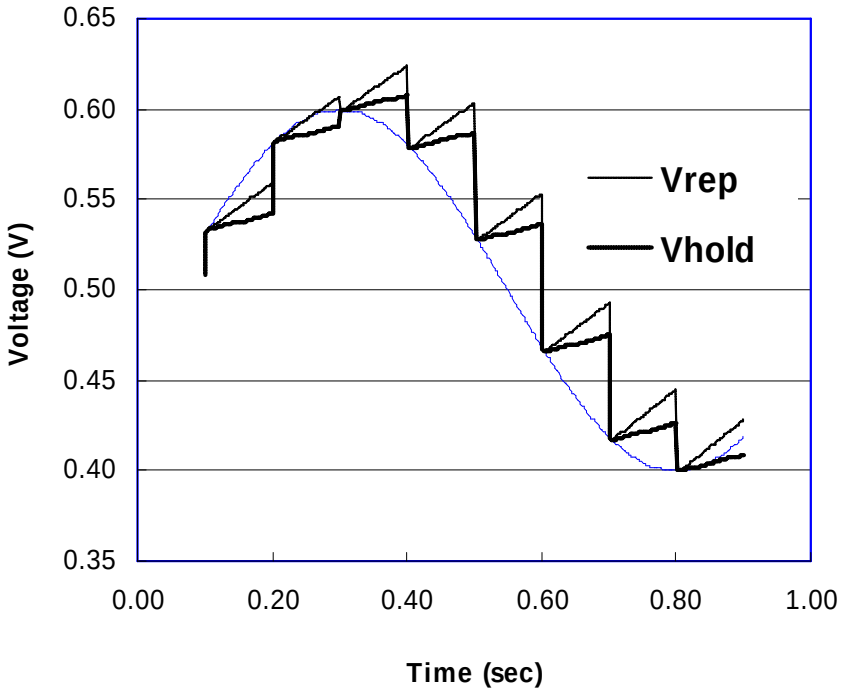
The concept of "Leakage Cancellation Technique"

Leakage Cancellation Technique - Concept



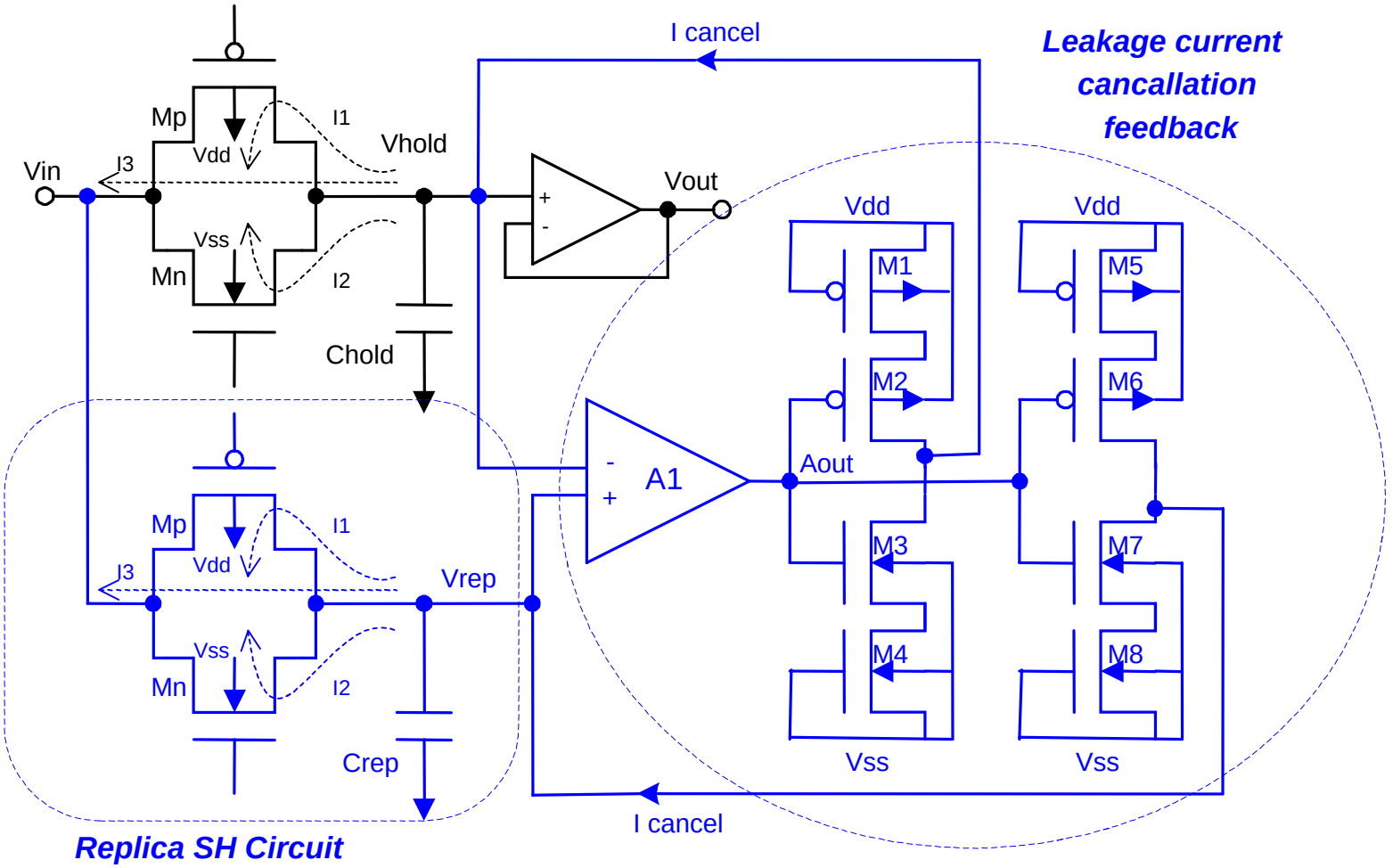
Main SH Circuit

Replica SH Circuit



Introducing the "Replica SH Circuit", with Crep << Chold

Leakage Cancellation Technique - Design



$$\frac{dV_{hold}}{dt} = \frac{I_{delta}}{Chold - Crep} = \frac{f\left(\frac{Aout}{A} + V_{offset}\right)}{Chold - Crep}$$

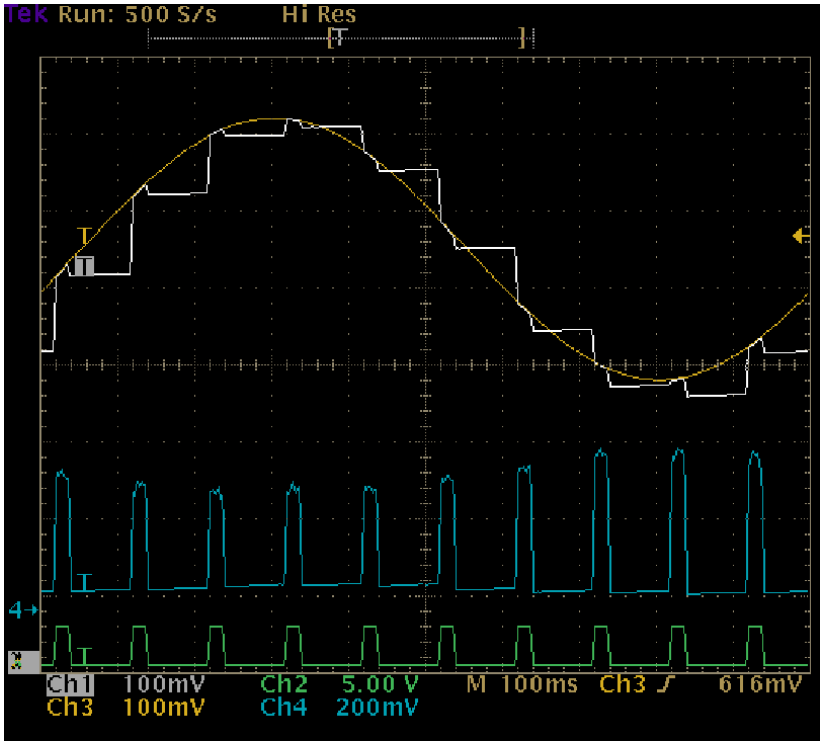
A design example of the "Leakage Cancellation Technique"

Leakage Cancellation Technique - Results

SHA (Original)

1Hz sine input, Fs=10Hz

I leakage ~ 0.1pA total



SHA with Leakage Cancellation

1Hz sine input, Fs=10Hz

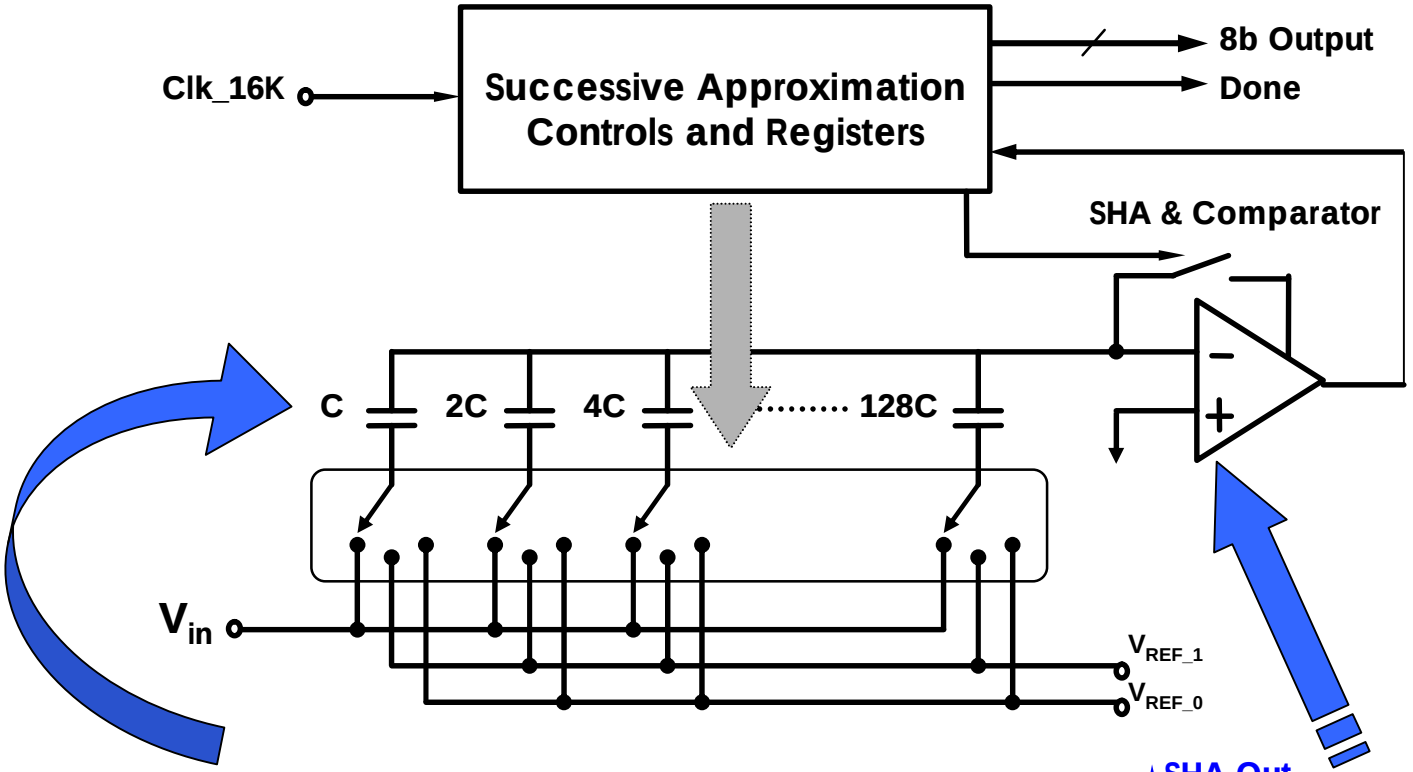
I leakage < 0.01pA (effective)

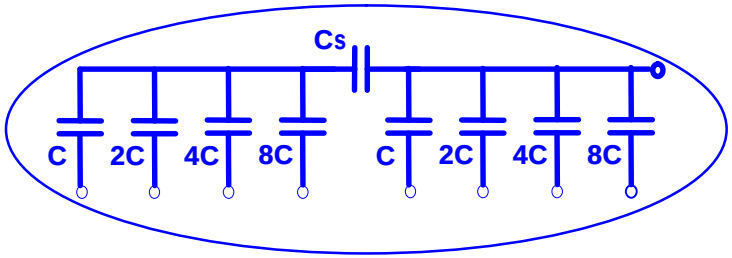
Overview of Cardiac Pacemaker – ADC

8-bit ADC

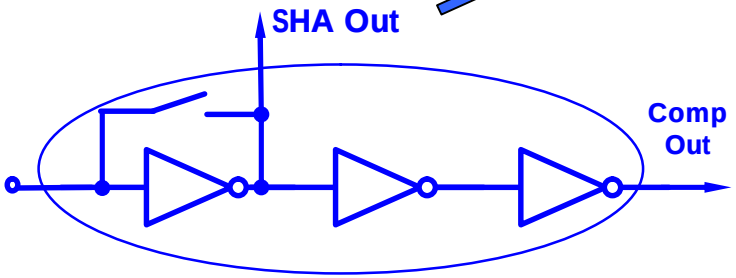
- ADC is used to digitized the cardiac sensing outputs
- Successive Approximation Architecture
- Typical power consumed by:
  - S/H
  - DAC
  - Comparator
- **To minimize power, this ADC:**
  1. **Uses capacitor-array for both DAC and SHA**
  2. **Use an integrated-opamp for both SHA and comparator**

8-bit ADC – Architecture



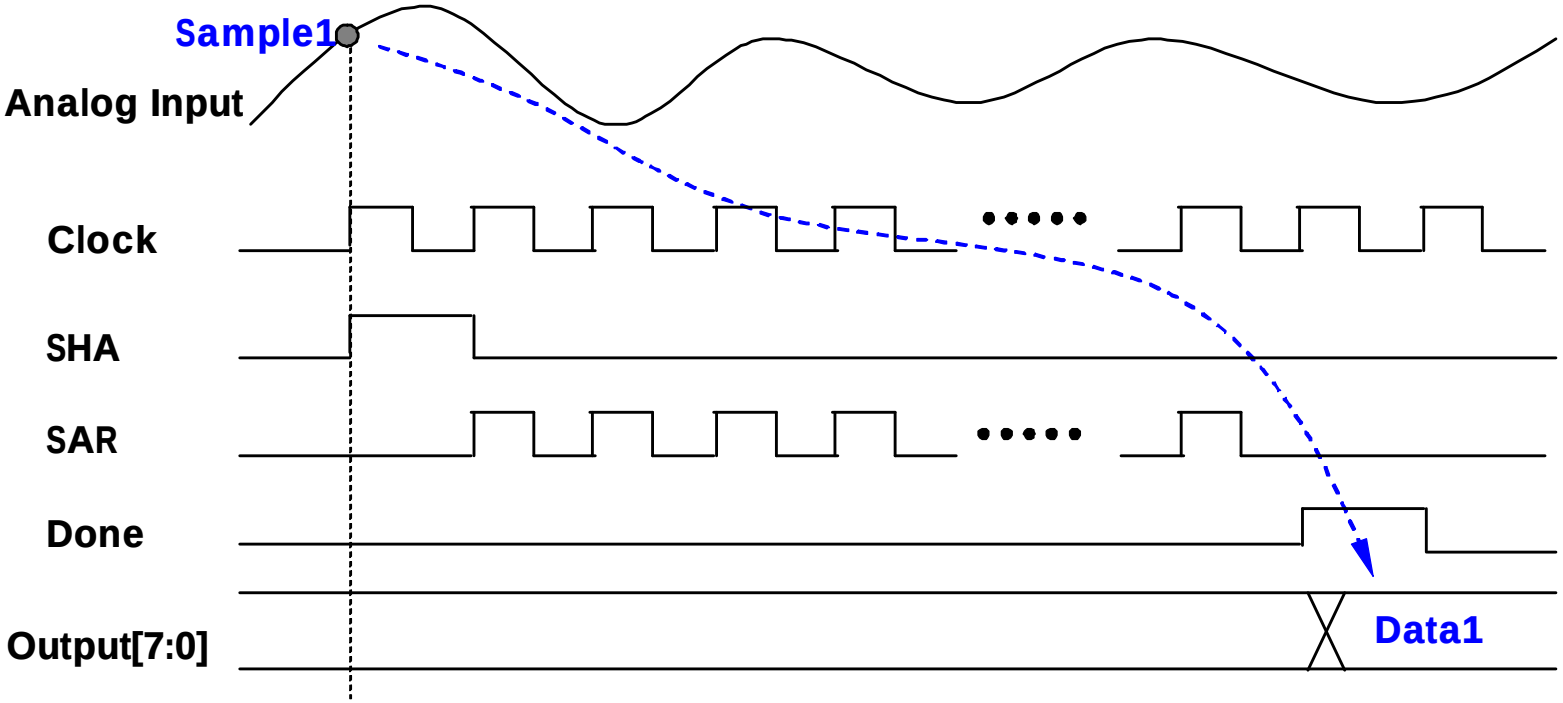


Capacitor array for S/H and DAC

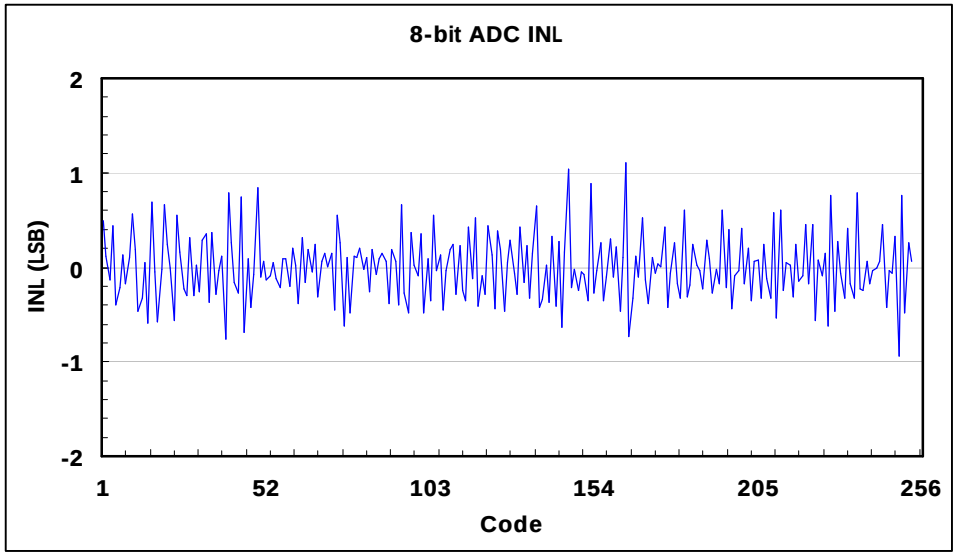


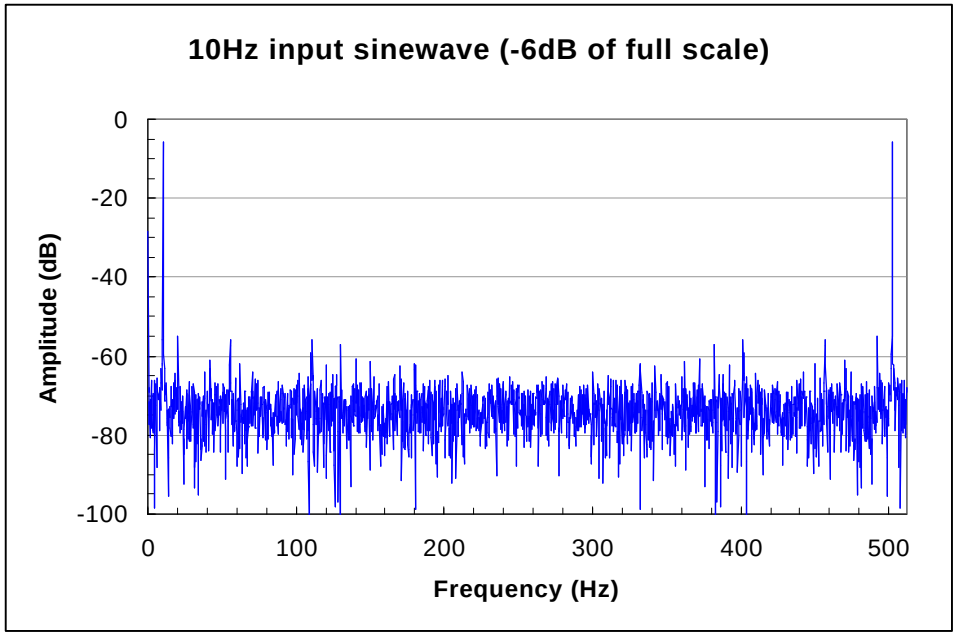
Integrated “S/H-comparator”

8-bit ADC – Timing



8-bit ADC – Measured Results

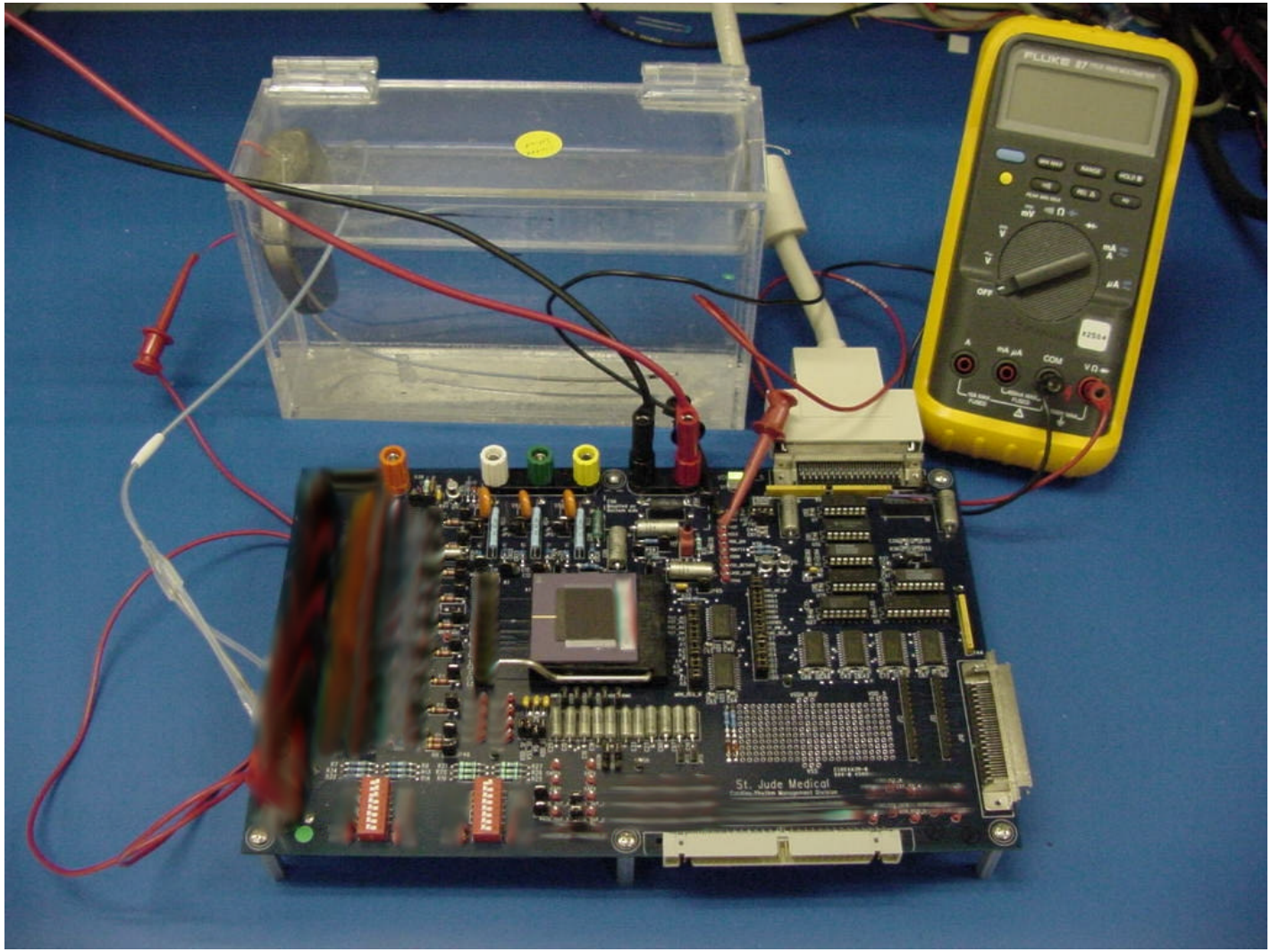




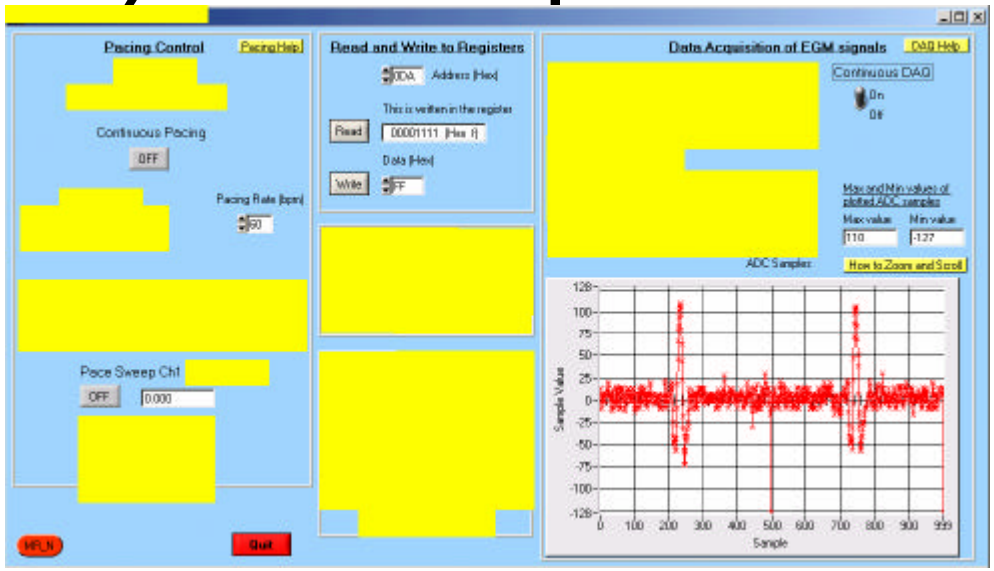
8-bit ADC – Measured Results

Parameter	Value
Resolution	8-bits
Sampling Rate	1 KS/s
Input Voltage Range	500mVpp
INL	< 1.5 LSB
DNL	< 1.5 LSB
SFDR	> 48 dB
Supply Current (On)	~ 150nA @ 2V
Supply Current (Standby)	~ 20nA
Gain error	< ±10% FS
DC offset error	< 3 LSB

Complete Sensing System – Measurement Setup



Complete Sensing System (SC Filters and ADC) – Example ECG Results



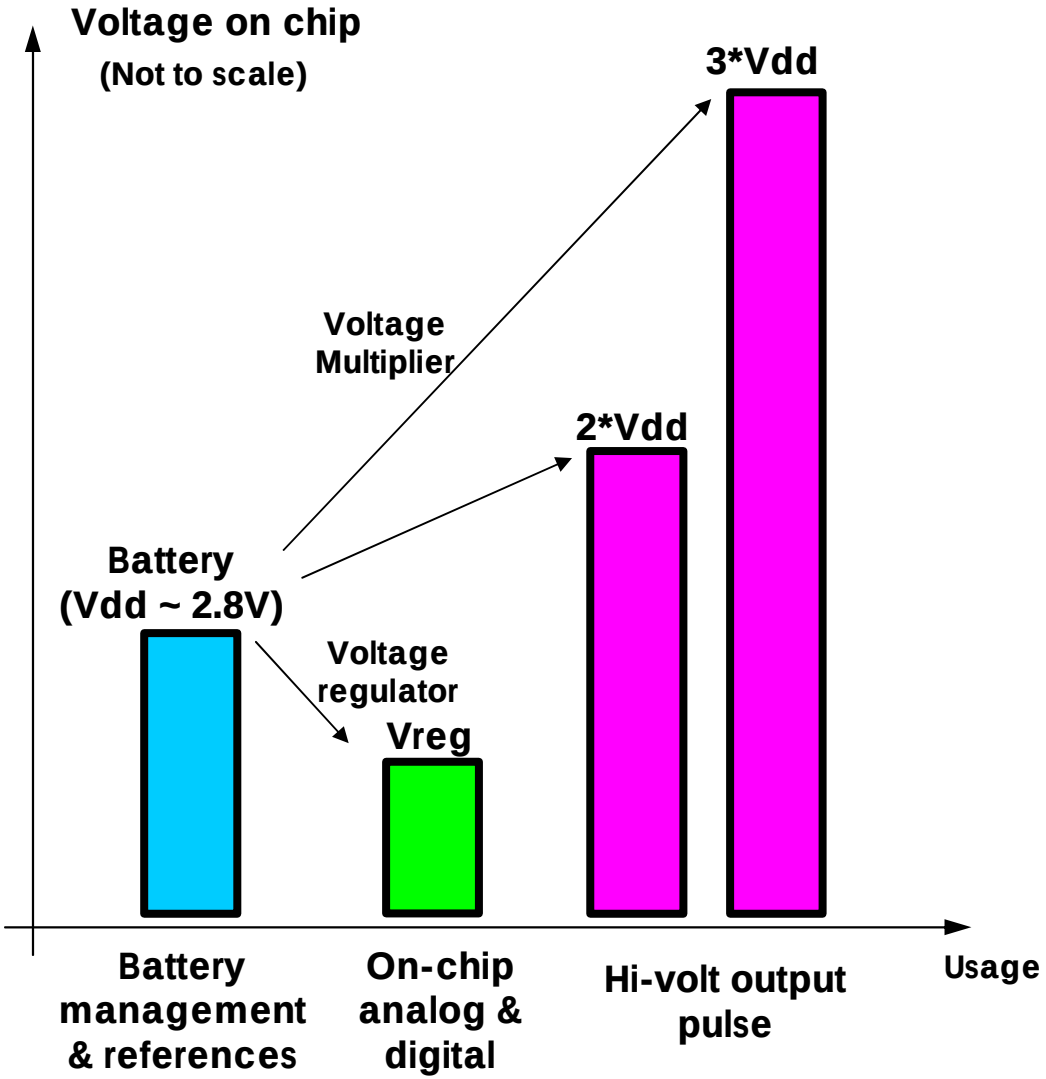
An example ADC output of Electrocardiogram (ECG) processed by different SC filters.

Overview of Cardiac Pacemaker – Output Therapy System

High Voltage Output System

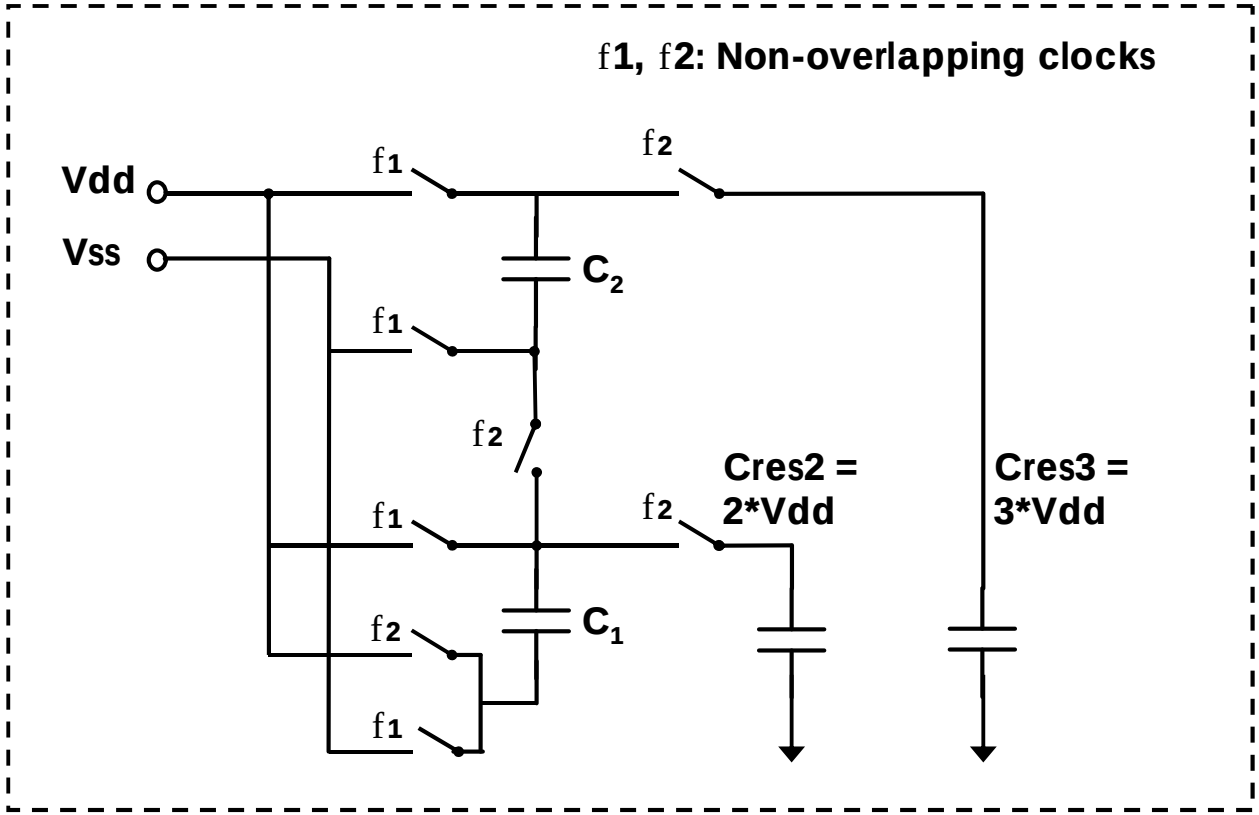
- To stimulate the heart muscle (e.g. initiate a heart beat), a high-voltage output pulse is delivered to the heart through the pacing leads.
- Multiplying the battery voltage is needed to generate the necessary high voltage.
  - **A Voltage Multiplier Circuit is used**
- The amplitude and pulse width of the high-voltage output pulse is customized for the patients.
  - **A High Voltage DAC is used**

High Voltage Multiplier



Voltage Multipliers and Regulators for the complete IC

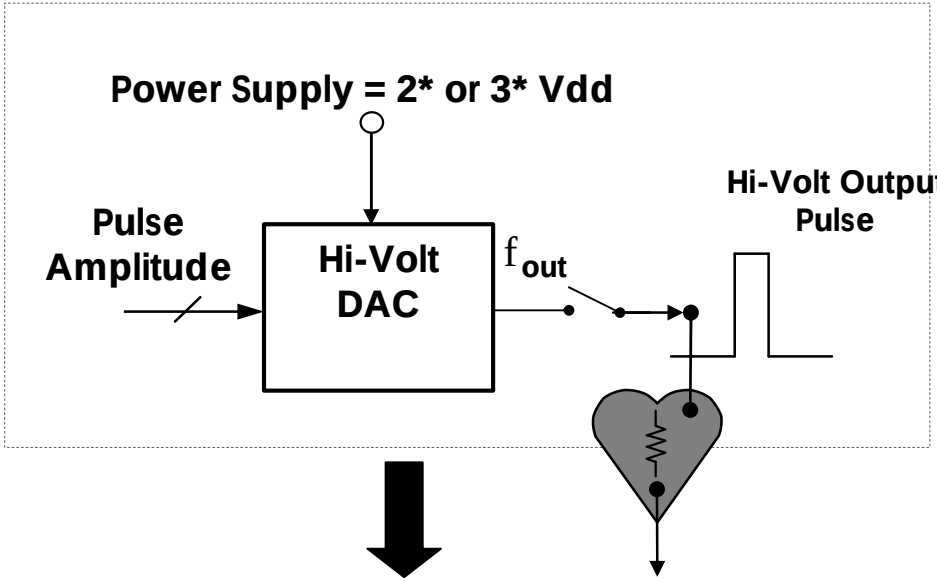
Capacitive Voltage Multiplier – Design



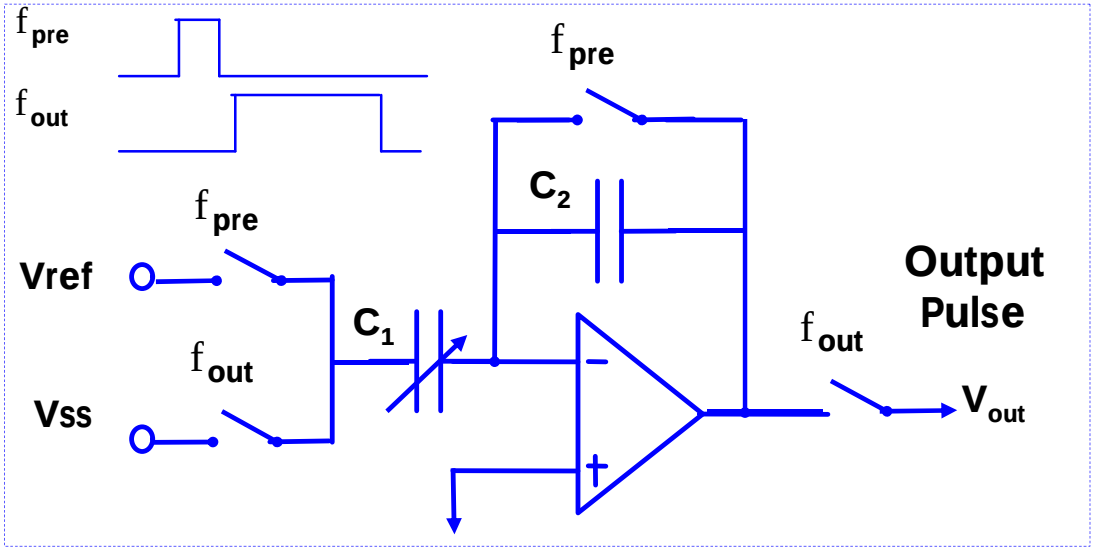
Capacitive 2X and 3X voltage multiplier

High-Voltage DAC – Design

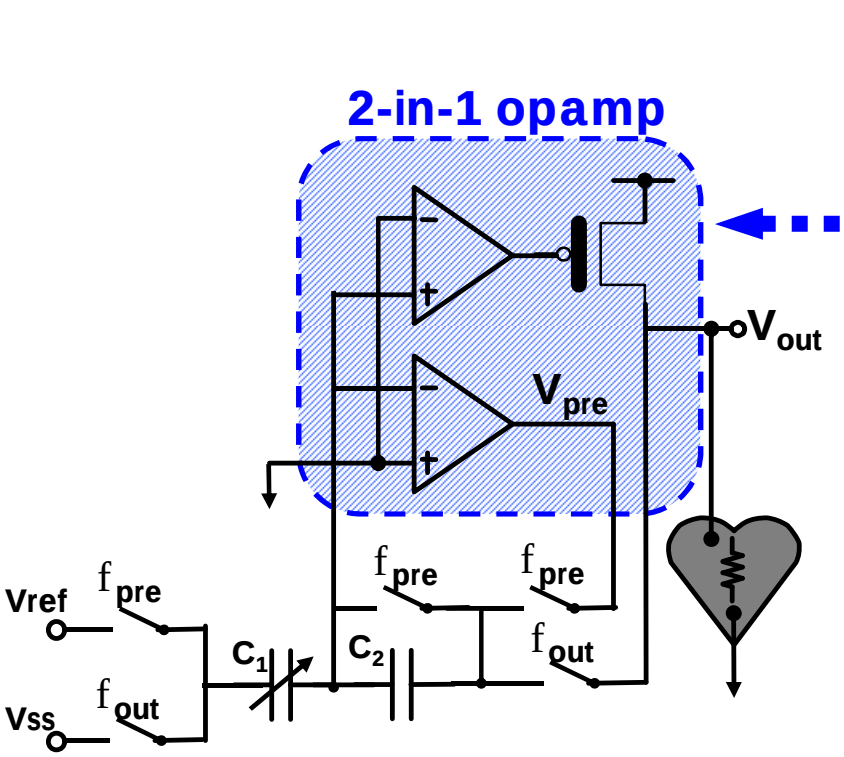
Hi-Voltage Output Pulse Generator: Equivalent model

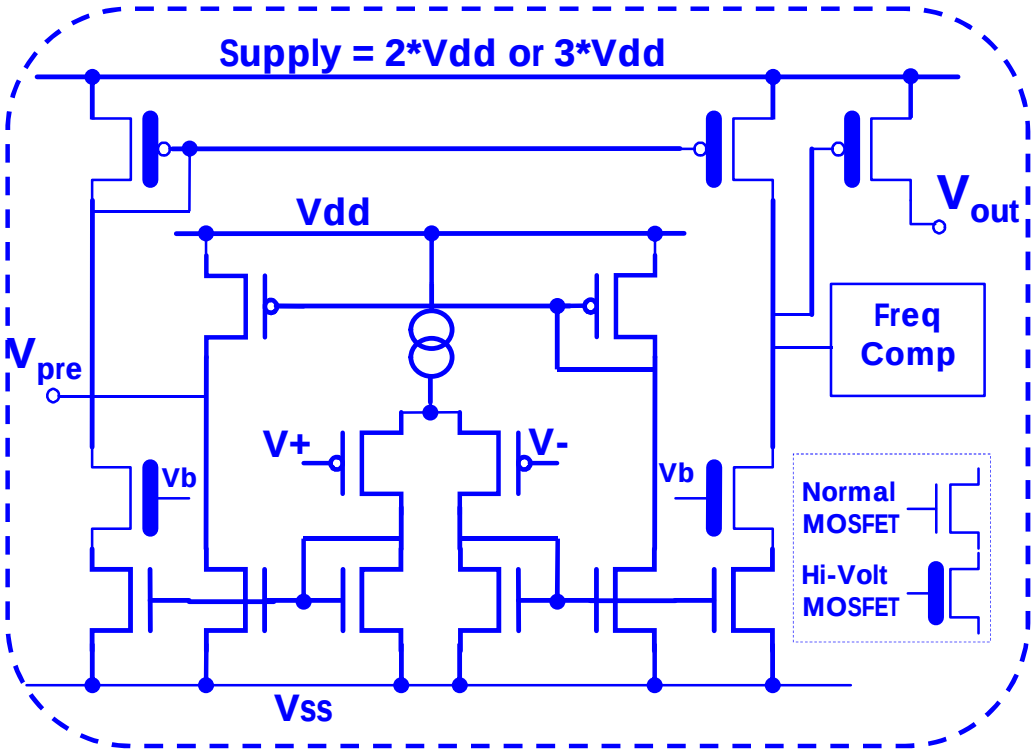


Hi-Voltage Output Pulse Generator: Switched-Cap DAC



High-Voltage DAC – Design

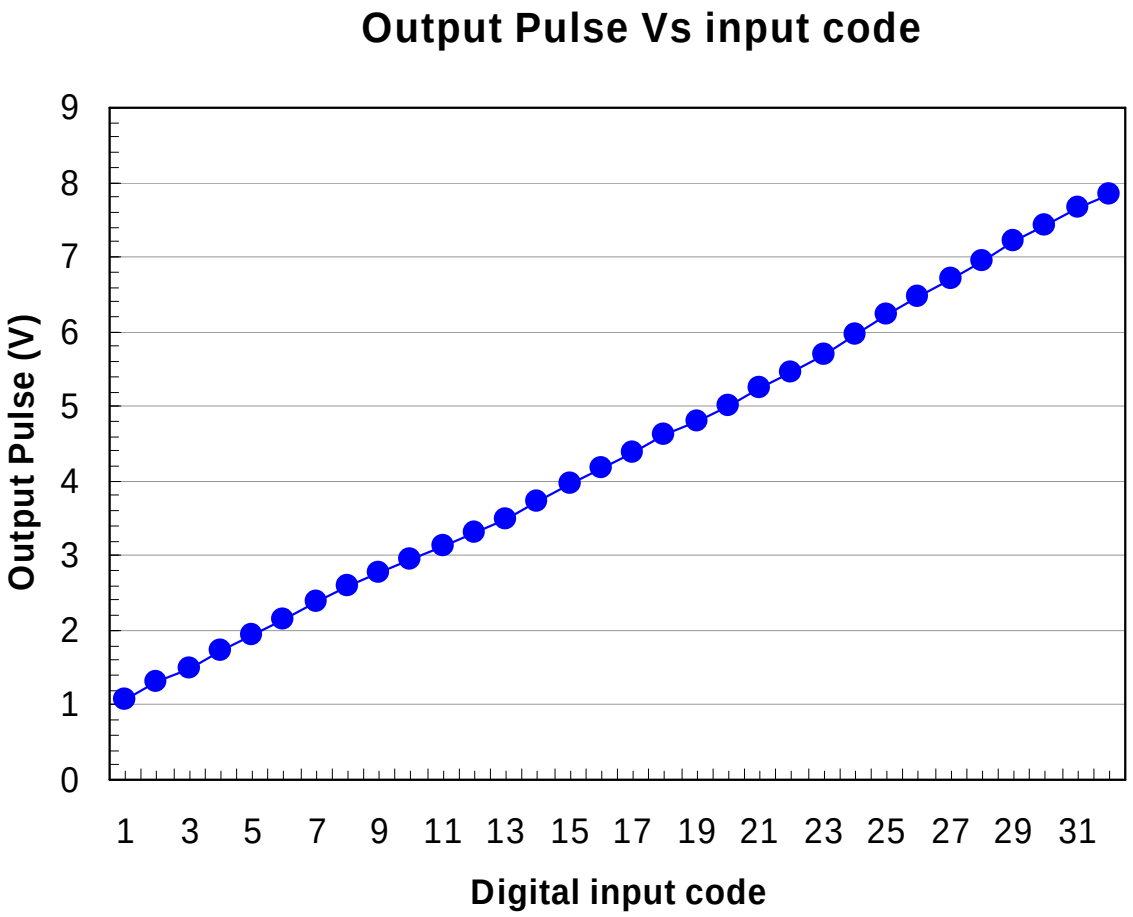




High-Voltage DAC utilizing 2-in-1 opamp

2-in-1 (HV/LV) CMOS opamp

High-Voltage DAC – Measured Results



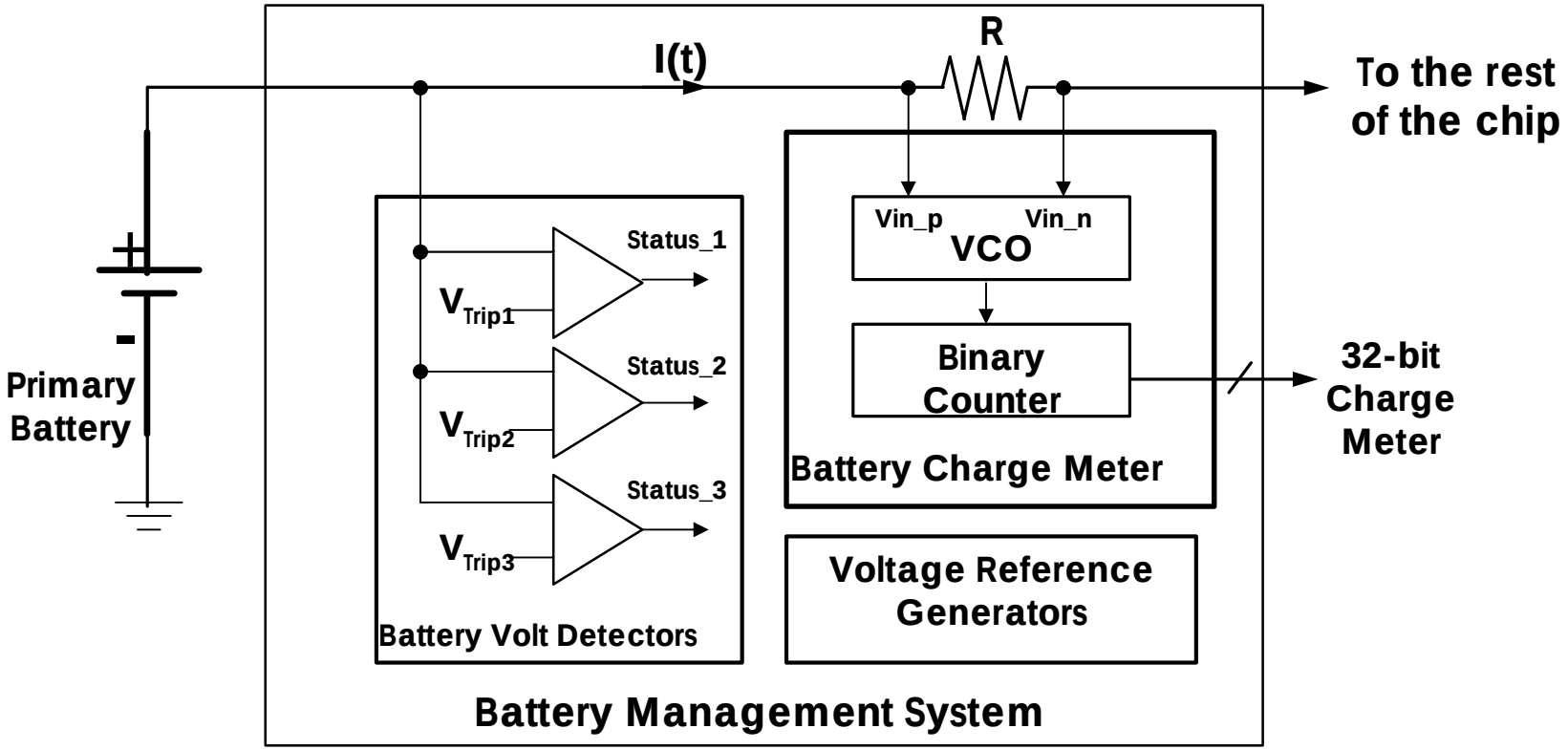
Linearity of Output Pulse Amplitude

Overview of Cardiac Pacemaker – Battery Management System

Battery Management System

- A primary battery (~2.8V) is typically used for a 5-10 years of device life time.
- Battery status must be accurately monitored to guarantee reliable operations.
- The status of the battery is determined by measuring its output voltage. However, it may NOT be very accurate due to the flat output voltage characteristics.
- **To enhance accuracy:**
  - **A Battery Charge monitoring circuit (Battery Charge Meter) is proposed.**

Battery Management System – Block Diagram



Battery Charge Meter:

- Low offset, high linearity VCO
- Continuously monitors 0.5μA-100μA of current
- Very low power consumption

Battery Management System – Battery Charge Meter

- VCO output frequency:

$$Freq_{VCO} = K_{VCO} \times I(t) \times R$$

- The output of the counter:

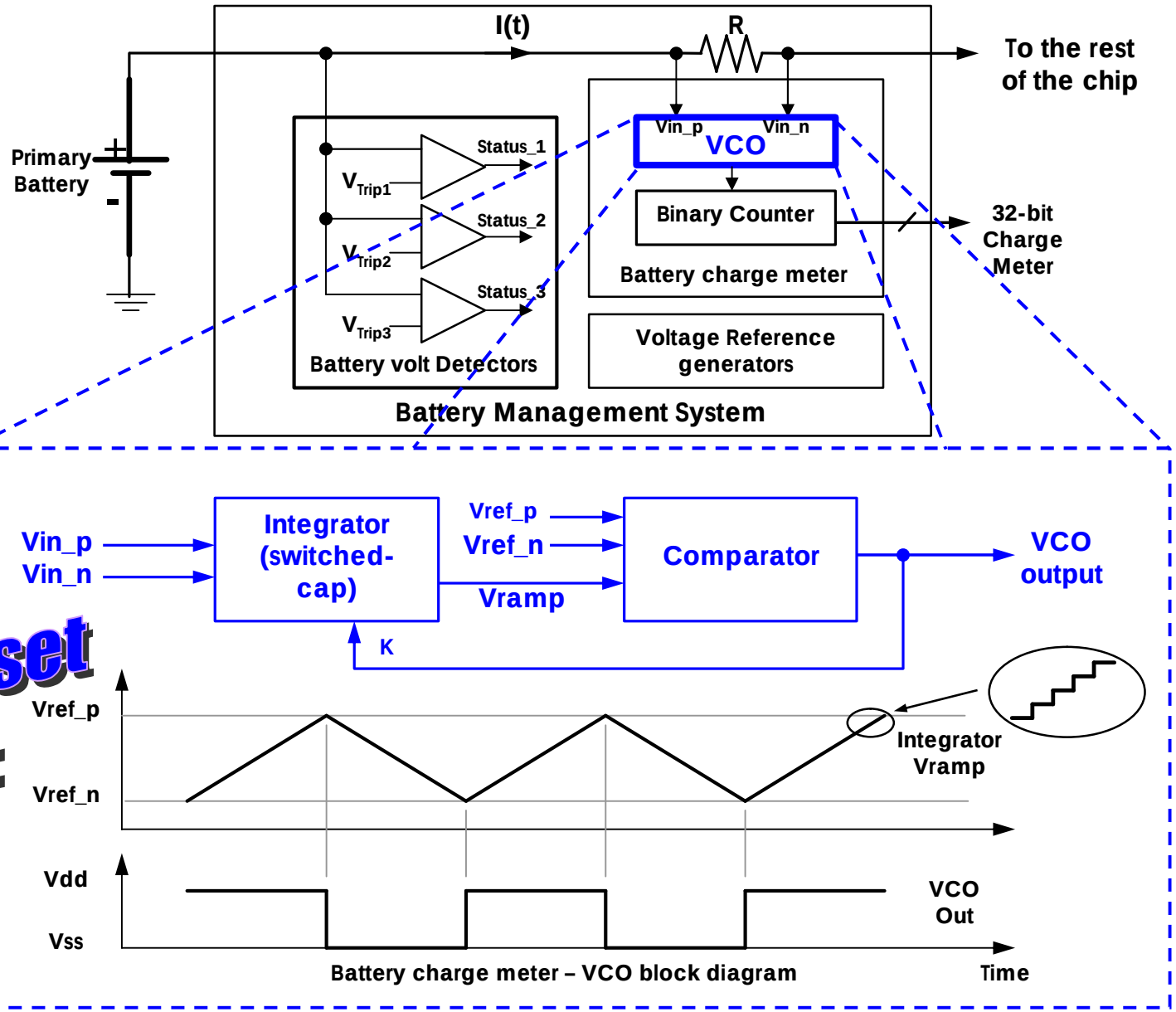
$$Count = \int Freq_{VCO} \cdot dt = \int K_{VCO} \times I(t) \times R \cdot dt$$

- Re-arrange to give:

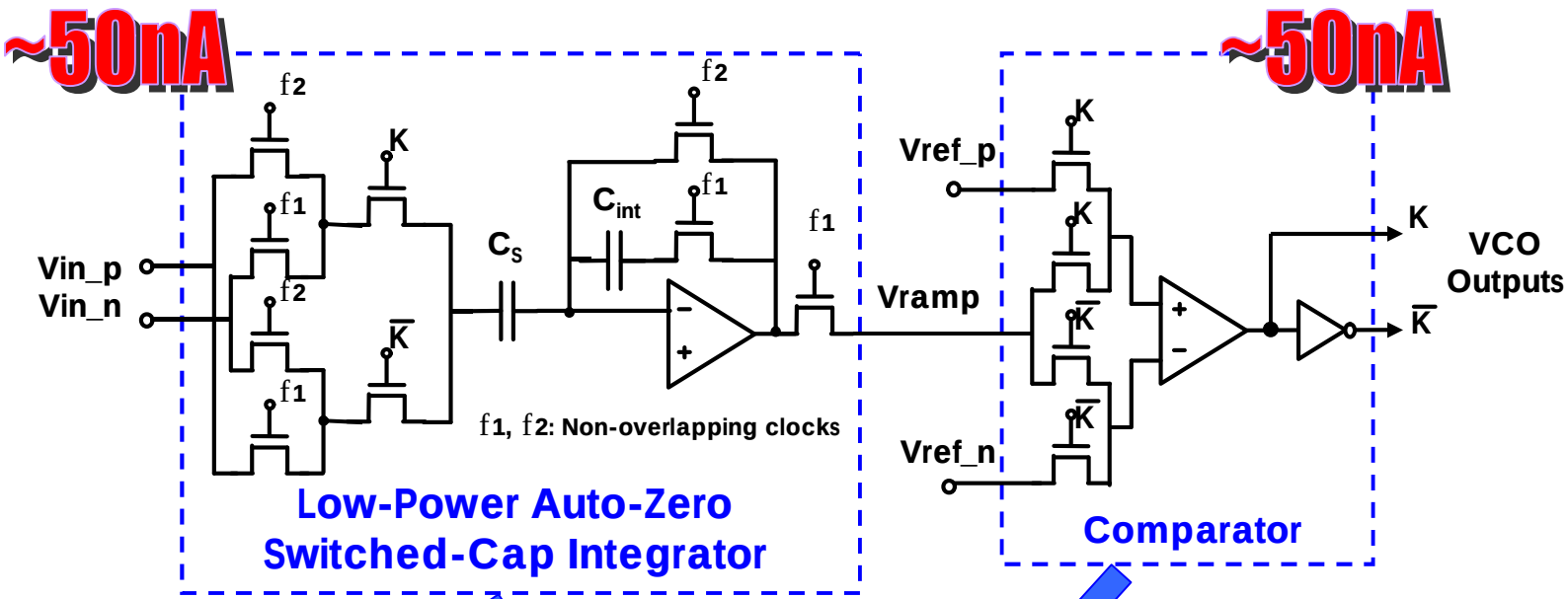
$$Q = Charge = \int I(t) \cdot dt = \frac{Count}{K_{VCO} \times R}$$

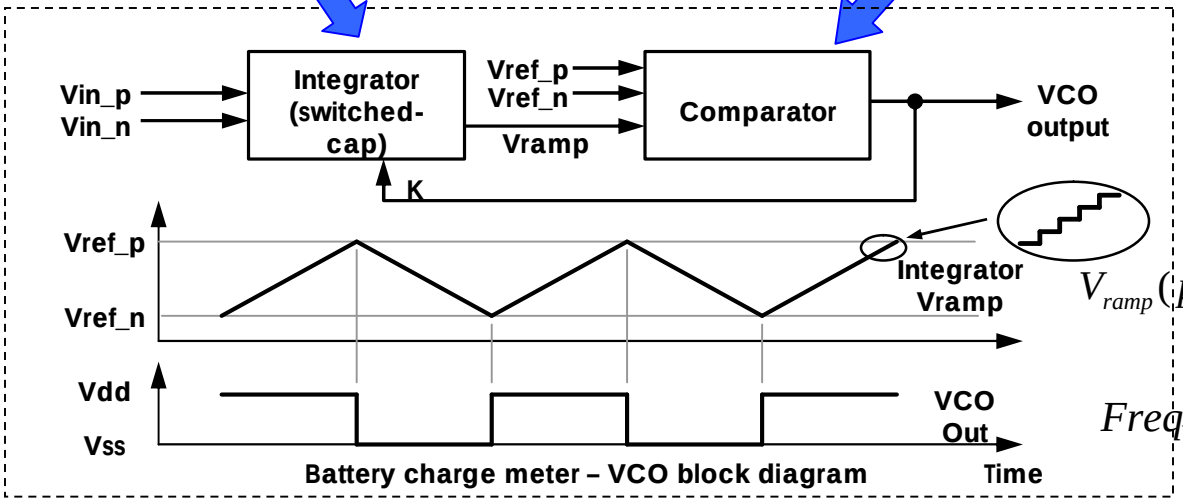
- Knowing "*Count*, K_{VCO} and *R*", the total charge depleted from the battery can be accurately calculated.

Battery Charge Meter - Design



Battery Charge Meter – VCO Design

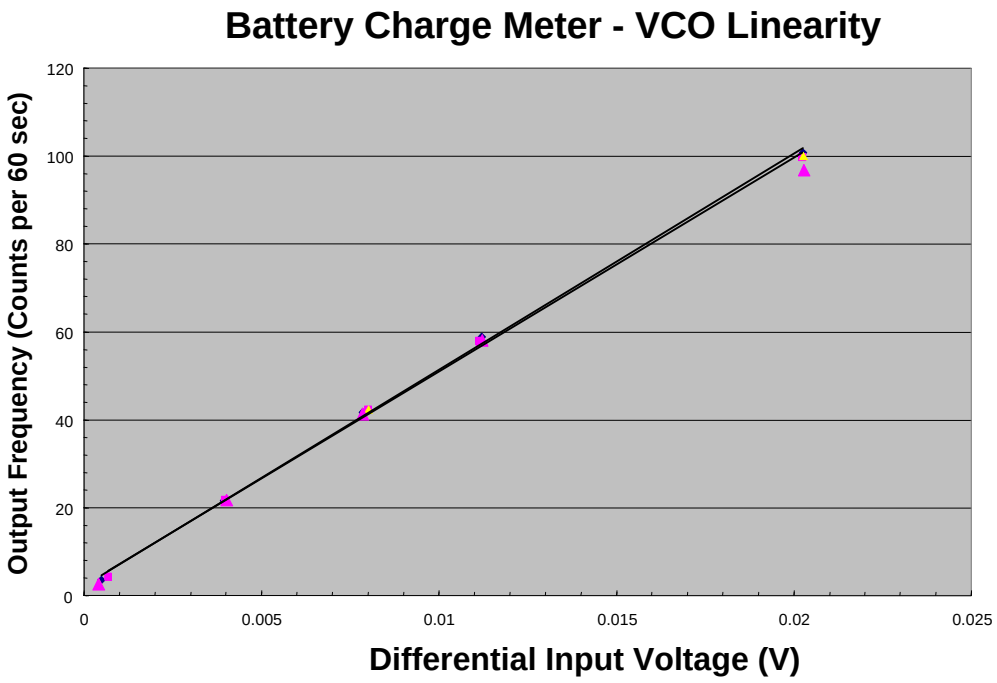




$$V_{ramp}(per\_step) = \frac{(V_{in\_p} - V_{in\_n}) \times C_s}{C_{\text{int}}}$$

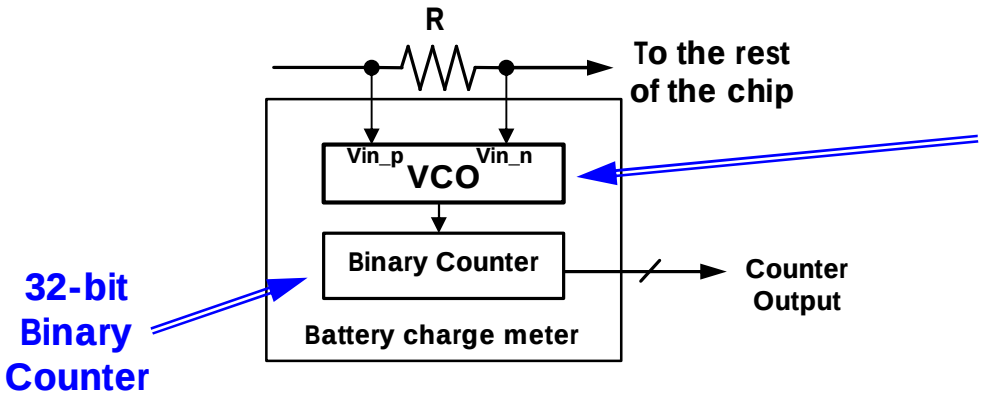
$$Freq_{VCO} = \frac{(V_{in\_p} - V_{in\_n}) \times F_s \times C_s}{2(V_{ref\_p} - V_{ref\_n}) \times C_{\text{int}}}$$

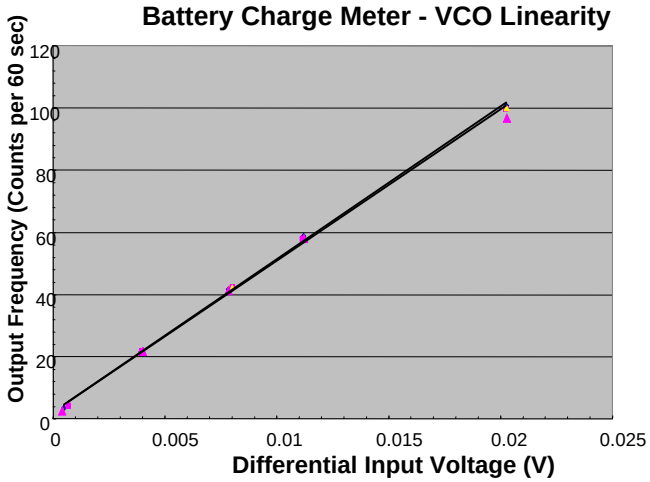
Battery Charge Meter – Measured Results



Parameter	Value
Input Range	0mV - 50mV
VCO Gain	80 Hz/V
Input Offset Error	< 150µV
Sampling Rate	8 KHz
Supply Current (On)	~ 100nA @ 2.8V
Supply Current (Standby)	< 10nA

Battery Charge Meter – Measured Results





Now, we have:

- Kvco = 80Hz/V, R = 500Ω and assume a 1A-h battery

$$Q = Ch\arg e = \int I(t)\cdot dt = \frac{Count}{K_{VCO} \times R}$$

- At the end of battery life, the counter output will reach:

144,000,000 counts

(It is also independent of the battery output voltage!)

Overview of Cardiac Pacemaker – Low Power Logic Design

by:

Raymond Okamoto

Raymond Okamoto received his B.S. ECE from U.C. Santa Barbara. He has 15+ years in both hardware and software designs. He has previous worked for ArgoSystems, Trimble Navigation, Intel and Mentor Graphics. He has designed both GPS and networking ASICs as well as other hardware systems. He joined St Jude Medical in 2003.

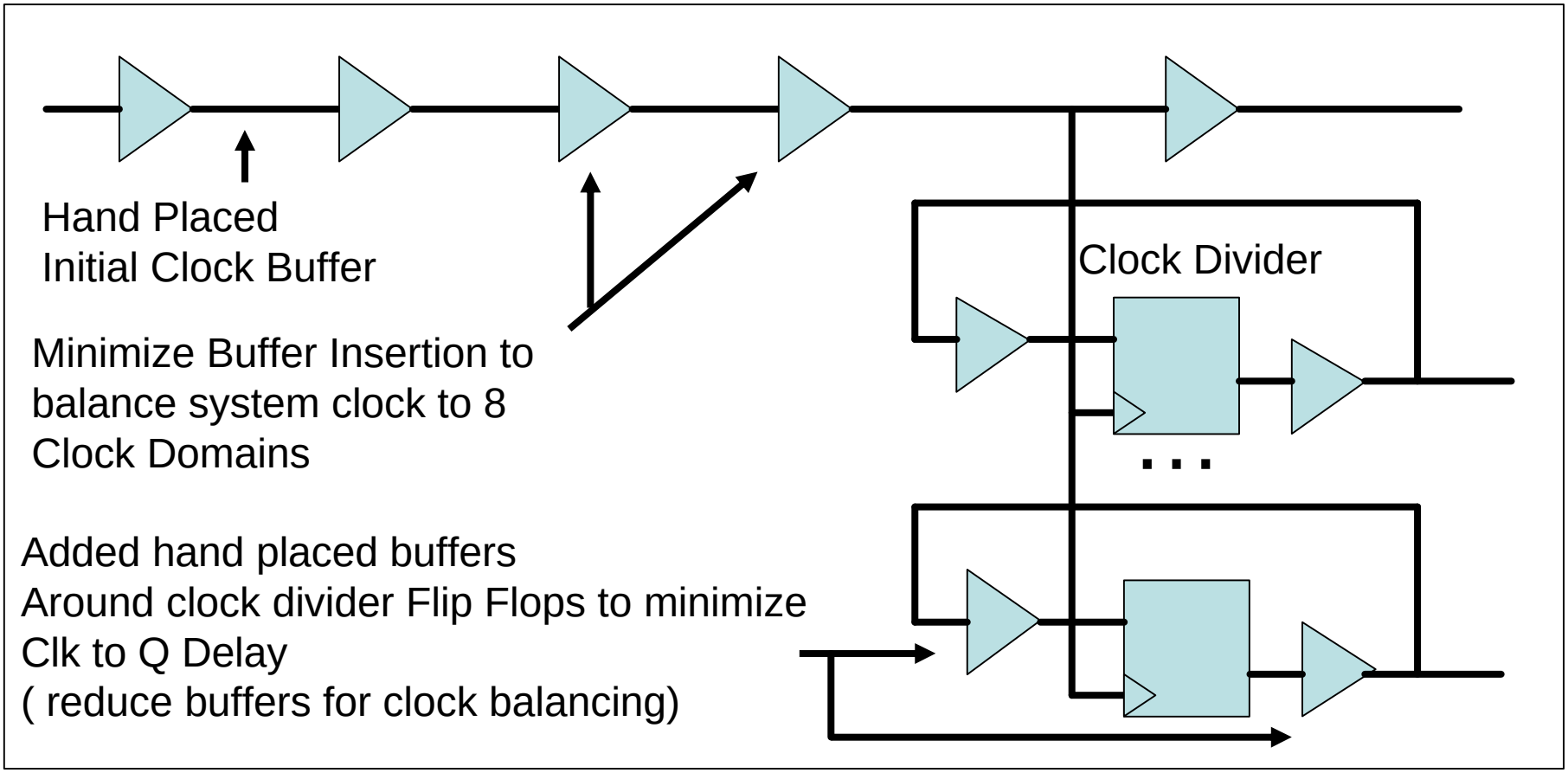
Programmable Logic, Timing Control and Therapy Algorithms

- CPU Configuration Registers
- Timing and control for Analog Functions
- Finite State Machine under CPU control for Therapy Algorithms
- Hardware Control Finite State Machine in backup (fail safe) mode to delivery therapy
- RTL to GDSII design flow
- Low Power Design (nW)

Digital Core Lower Power Techniques

- Minimize Voltage
  - Trade off custom low power library vs standard library
  - Backend Flow with multiple power
- Minimize Clock Frequency
  - Gated Clock Design
  - Review of minimum clock frequency required
- Minimize Capacitance (Logic Area)
  - Design for minimum logic at the RTL level
  - Reduce clock domains (trade off with min clock frequency)
- Customize Clock Synthesis Tool for low power vs high speed trees

Clock Tree Synthesis
Custom Approach to minimize buffer insertion



5 : 1 Aspect Ratio for Digital Core

Overview of Cardiac Pacemaker – Low Power Memory Design

by:

Joseph Ahn

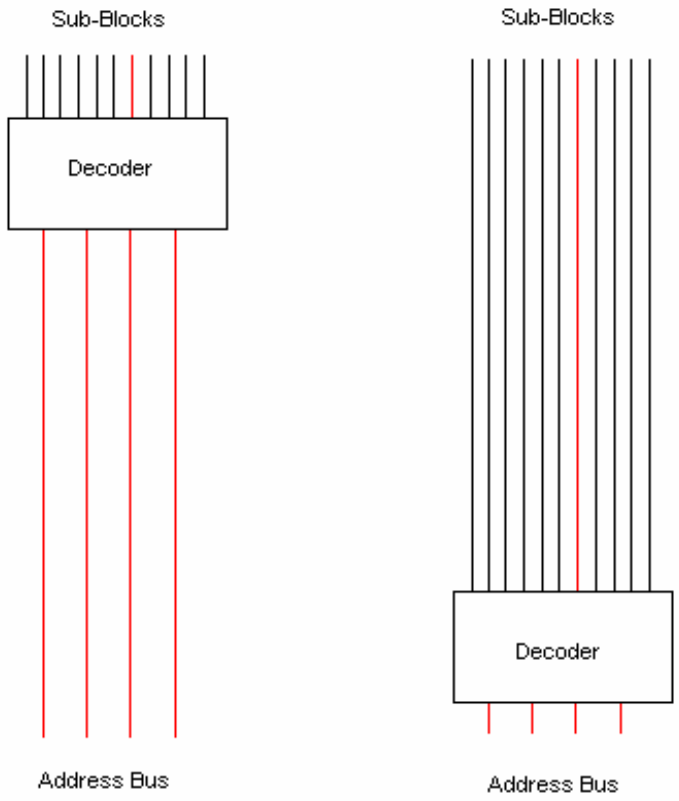
Joe Ahn received his B.S. and M.S. EE from Lehigh University. He has 11+ years in hardware design. He has previous worked for Virtual Silicon Technology, C-Cube Microsysytems and Aspec Technology. He has designed various components including SRAM's, ROM's, datapath blocks, I/O's and standard cells. He joined St Jude Medical in 2002.

Ultra-Low Power SRAM for Pacemakers and ICD's

- The three components of power
- Capacitance
  - Reduce switching of high capacitive nodes
- Voltage
  - Reduce the voltage swing
- Frequency
  - Lower operating frequency

Reduce switching of high capacitive nodes

- Smaller subsections
- Shorter word-lines and bit-lines
- Disable inactive circuitry
- Local decoders vs. global decoders



Reduce the voltage swing

- Partial voltage swings
- Low power sense amp
- Special manufacturing processes
  - Lower operating voltage
  - Leakage current
  - High Vt devices

Lower operating frequency

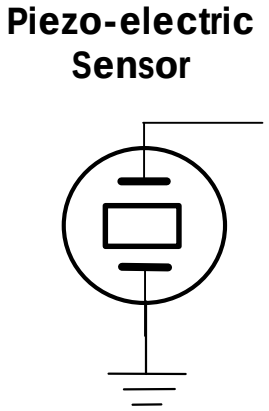
- Lower operating frequency

Overview of Cardiac Pacemaker – MEMS Activity Sensor

Patient Activity Sensor

- Patient activity sensor is used to:
  - Sense patient's body movements, and to determine the appropriate pacing rates for correct therapy.
  - An "Accelerometer Sensor" is placed inside the device.
  - Be able to differentiate between patient movements from surrounding noise (eg vehicle vibration, vacuum cleaner)

Activity Sensor Interface Circuit



- It generates a charge/voltage proportional to the patient's acceleration.
- The VCO generates an output signal whose frequency is proportional to the voltage sensed at the input. The number of cycles of the VCO output is proportional to the average patient physical accelerations.
- Low power consumption ~ 40nA

Overview of Cardiac Pacemaker – MEMS Magnet Sensor

Magnet Detection Sensor

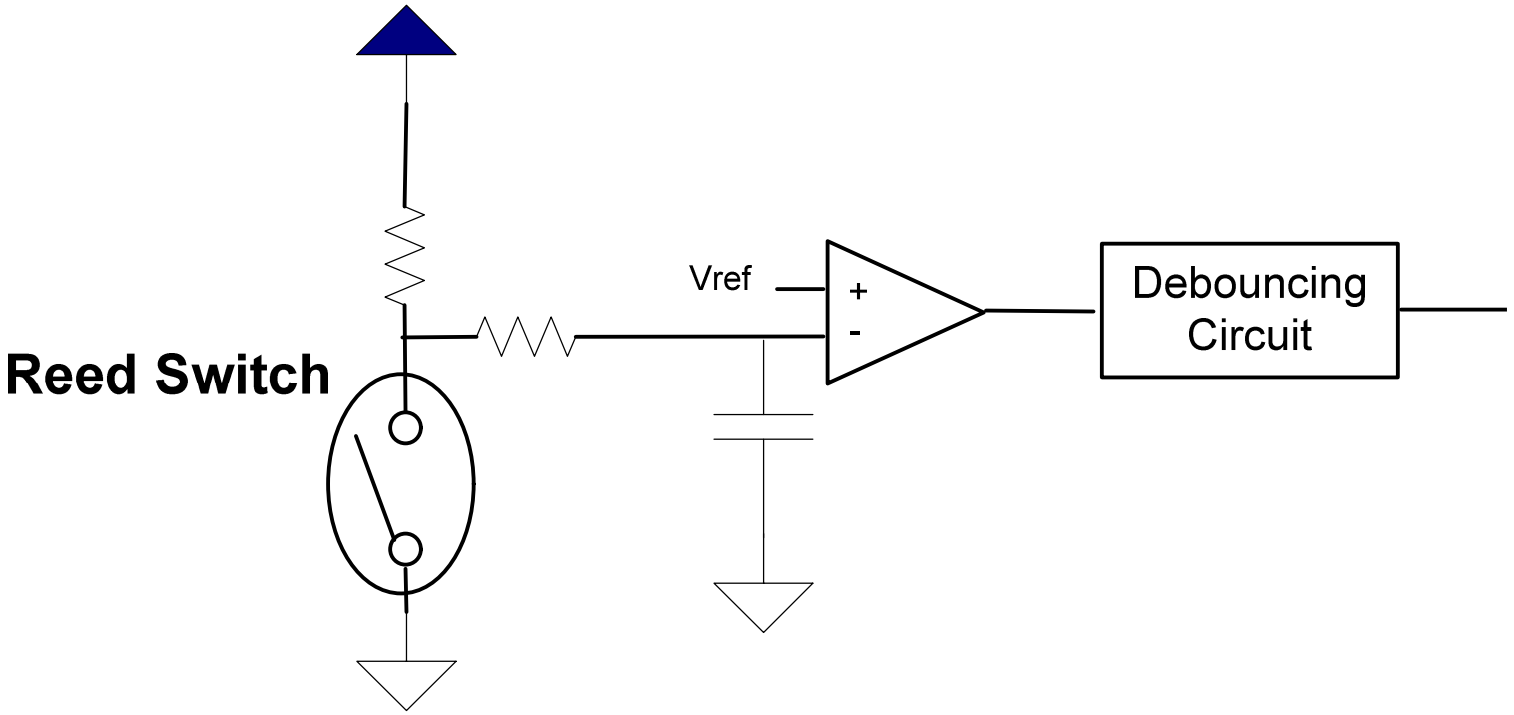
- A magnet detector can be used to:
  - Open the telemetry channel
  - Disable the device
  - Put the device into a special operating mode, e.g. in emergency

Magnet Detection Sensor

Two types of magnetic sensors are typically used:

1. Reed Switch
2. Giant Magneto Resistive (GMR) Sensor

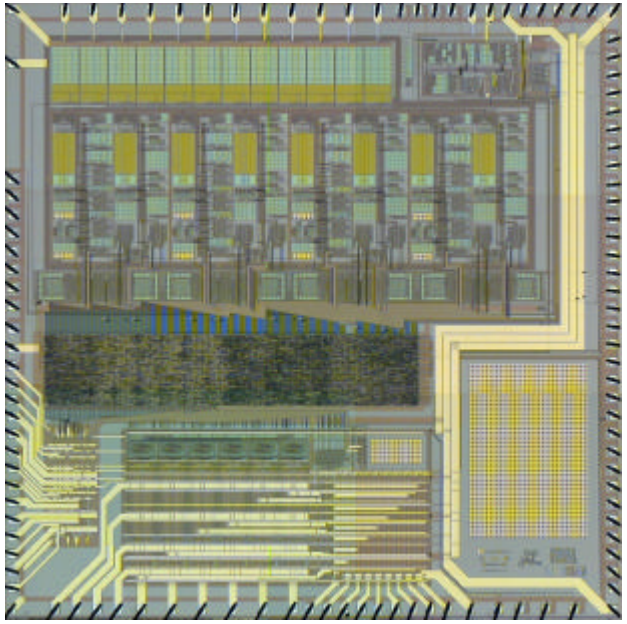
Reed Switch Interface Circuit



- Low pass filter
- Debouncing circuit to filter out glitches
- Very low power consumption ~ 20nA

Overview of Cardiac Pacemaker – Silicon Results

Silicon Results



Parameter	Value
Supply Voltage	2.0V – 2.8V
Power Consumption	~ 8mW
Die Size	7mm x 7mm