A Baseband Mixed-Signal Receiver for 1Gbps Wireless Communications at 60GHz

Berkeley Wireless
Research Center

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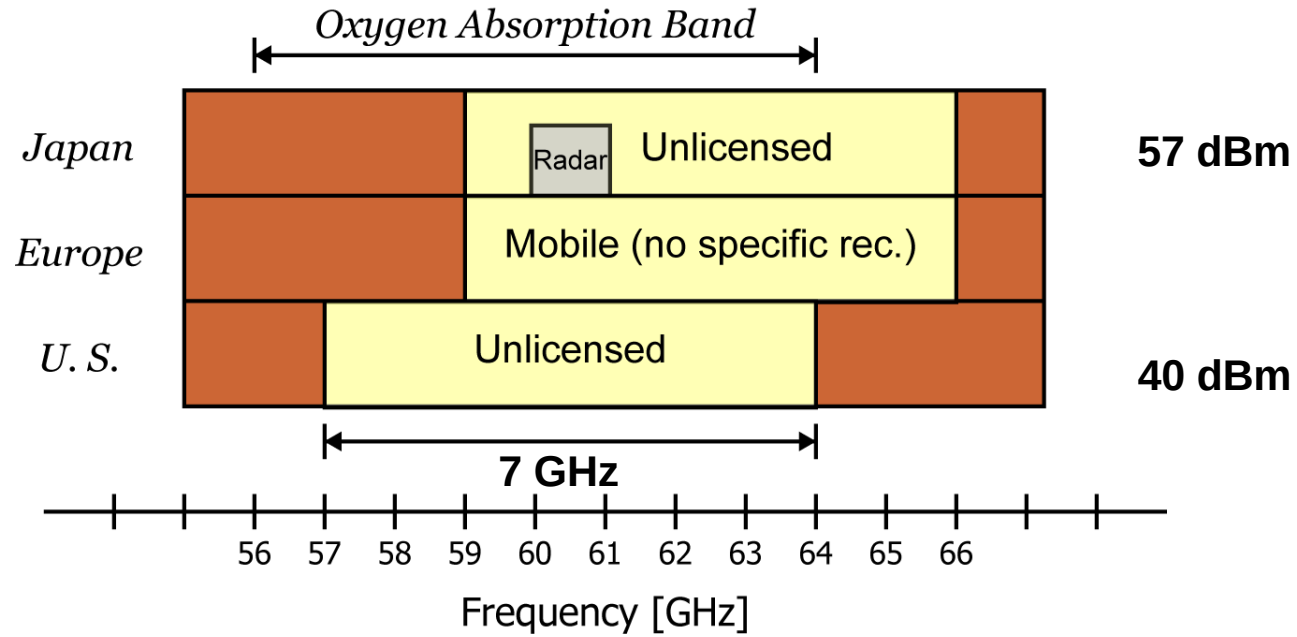
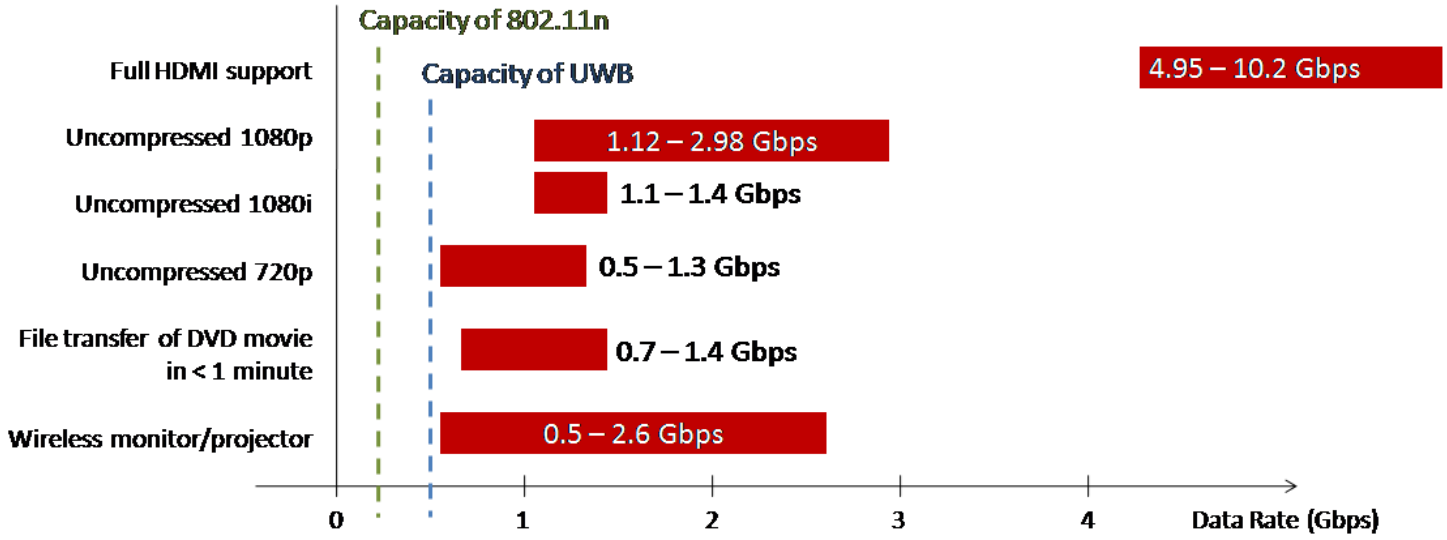
Apr. 16, 2009

The 60GHz Opportunity



- Unprecedented amount of unlicensed spectrum
- Few regulatory specifications
- Small wavelength allows for multi-antenna approach

Wireless HD Video Requirements



- Uncompressed in-home HD media distribution
- Fast transfer/sync of media to a portable device
- Wireless PC display

60GHz High-speed Link: Key Channel and Circuit Challenges

- Friis Transmission equation: Loss increases with f_c

$$L = \frac{P_{RX}}{P_{TX}} = \frac{G_{TX} G_{RX} c^2}{f_c^{\,2} (4\pi d)^2}$$

- Power-handling, linearity, and noise performance of CMOS circuits at 60GHz
- Multipath channel issues
  - Specular, (moderately) reflective channel
- Baseband analog interface bottleneck
  - High-speed link ➔ high-speed, high-resolution ADC/DAC?

Research Proposal

- Problem
  - Given 60GHz circuit and channel limitations, how do we design the baseband system and architecture for a power-efficient, high-data rate 60GHz wireless link?
- Approaches
  - Utilize beam-forming to combat channel loss and multipath
  - Identify modulation format most amenable to 60GHz RF circuits
  - Identify baseband architectures that allow for power-efficient, high data-rate baseband circuits
- Goals
  - Ease performance requirements on 60GHz RF circuits
  - Enable a low-complexity baseband architecture

Presentation Outline

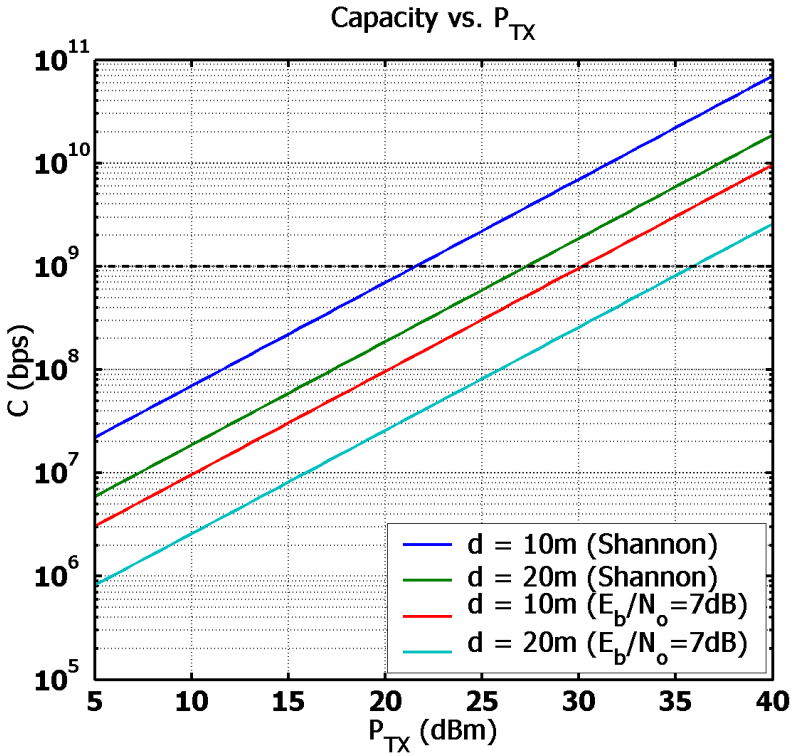
- Overview of 60GHz channel and beamforming
- Modulation scheme considerations
- Baseband architecture exploration and proposed system prototype
- Low-power, high-speed mixed-signal circuits
- Measurement results
- Conclusions

Shannon (and Some Practical) Limits

- Shannon AWGN capacity limited by received power

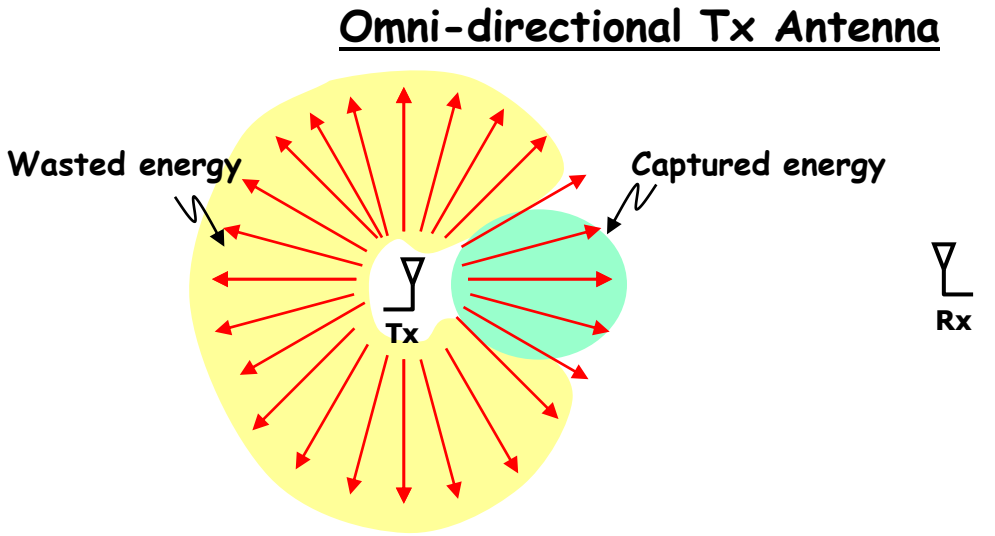
$$C_{BW\to\infty} \approx 1.44 \frac{P_{RX}}{N_o}$$

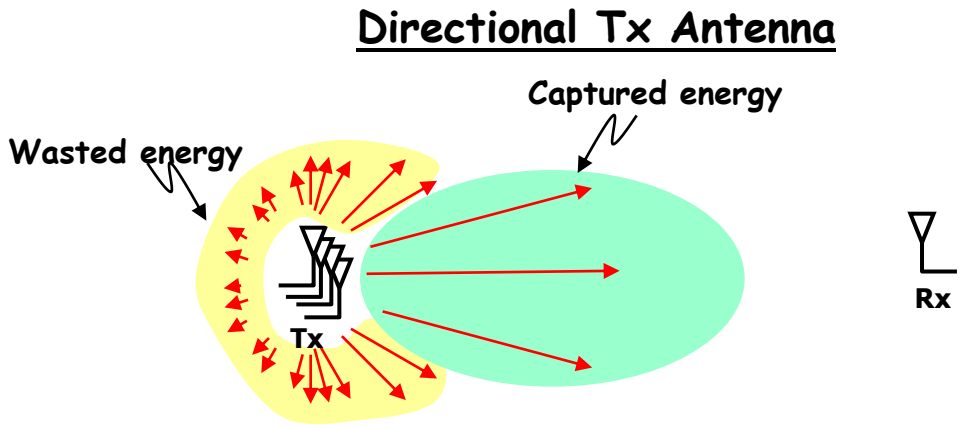
  - E_b/N_o=7dB for reliable communications
- Assumptions:
  - NF_{RX}=10dB
  - Link distance = 10m
  - 10dB other losses
  - Omni-directional antenna (G = 0dB)



Omni-directional antenna can't provide 1Gbps

Beamforming and Antenna Gain

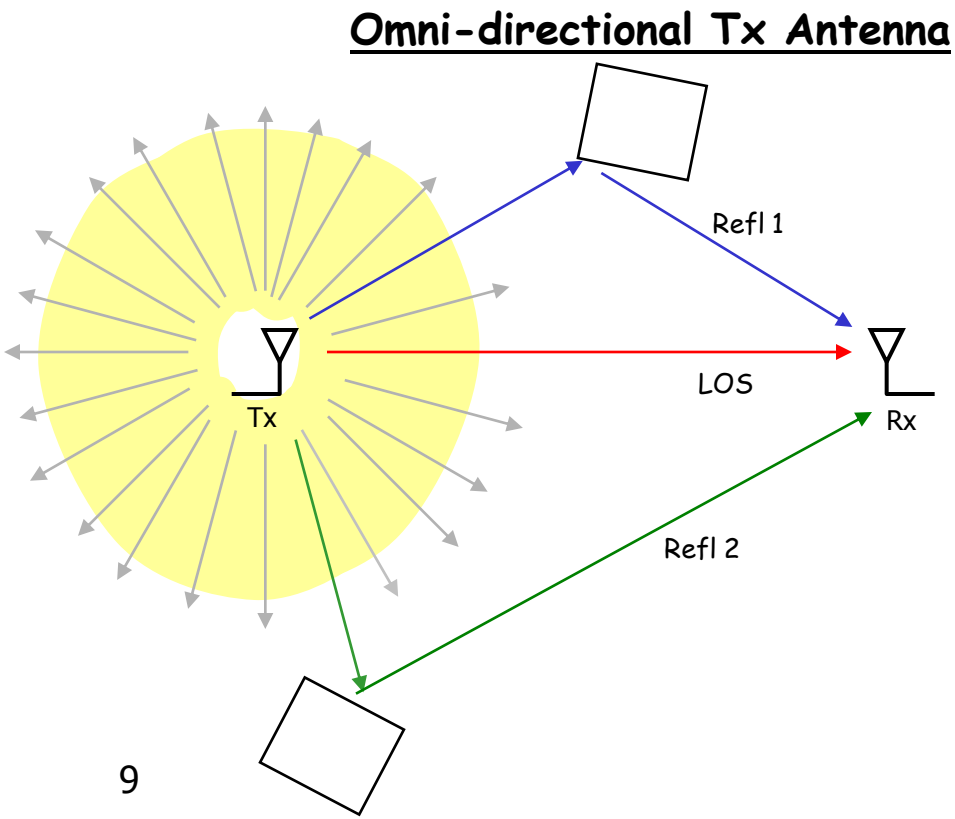


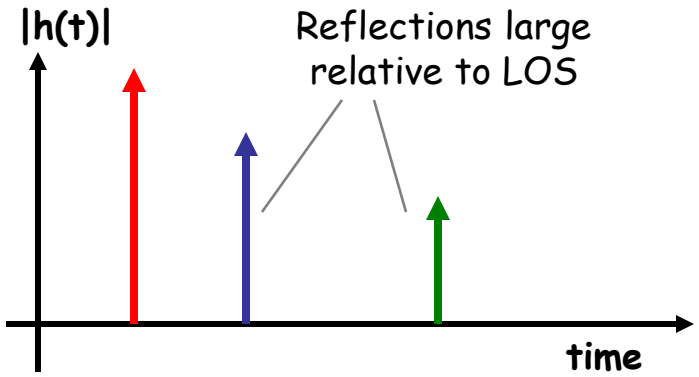


- Omni-directional antenna inefficient
- Antenna array forms narrow, steerable beam
- Increases antenna gain

Antenna Patterns and Multipath

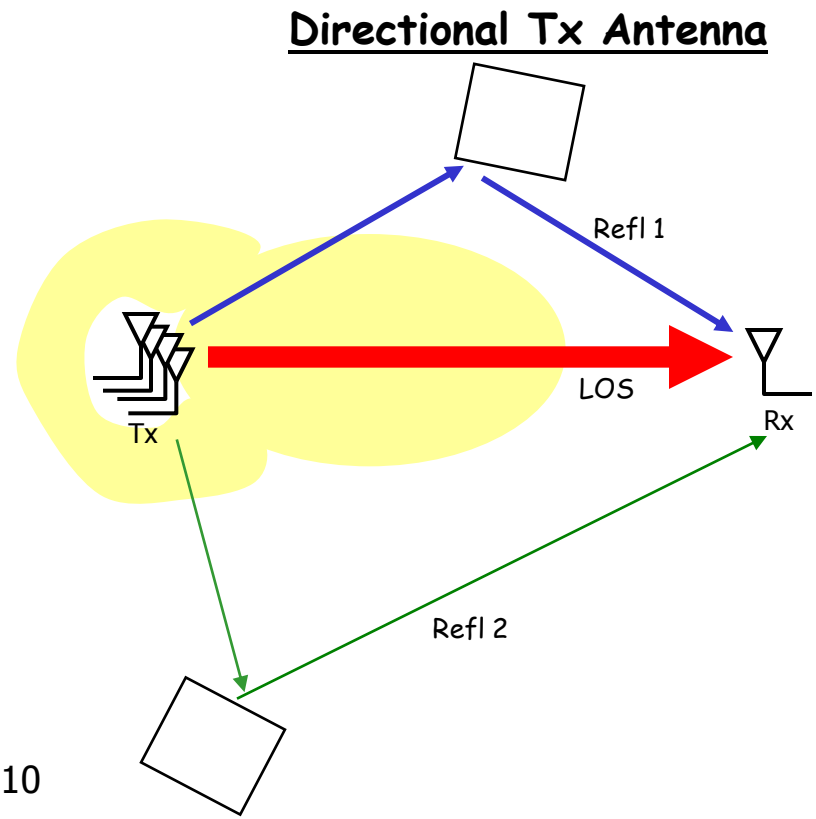
- Multipath caused by reflections off obstacles in space
- Omni-directional antenna can have poor multipath profile

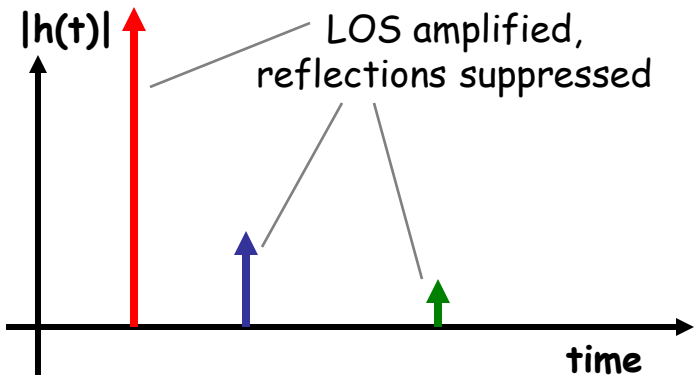




Antenna Patterns and Multipath

- Directional antenna restricts the spatial extent of signal to the LOS path
- Reduces reflections, improving multipath profile





60 GHz Channel Spatial Properties

- Specular, moderately reflective channel
  - Building materials poor reflectors at 60GHz
- "Typical" 60GHz indoor channel properties: [1]
  - Omni-antenna w/ LOS: T_{RMS} ~ 25ns, K_{Rician} ~ 0-5dB
  - 30° horn w/ LOS: T_{RMS} ~ 5ns, K_{Rician} ~ 10-15dB
  - $K_{Rician} = P_{LOS}/\Sigma P_{Multipath}$

Antenna directivity reduces **multipath fading** problem to **constrained ISI** problem

[1] M. Williamson, et al, "Investigating the effects of antenna directivity on wireless indoor communication at 6O GHz," PIMRC 1997

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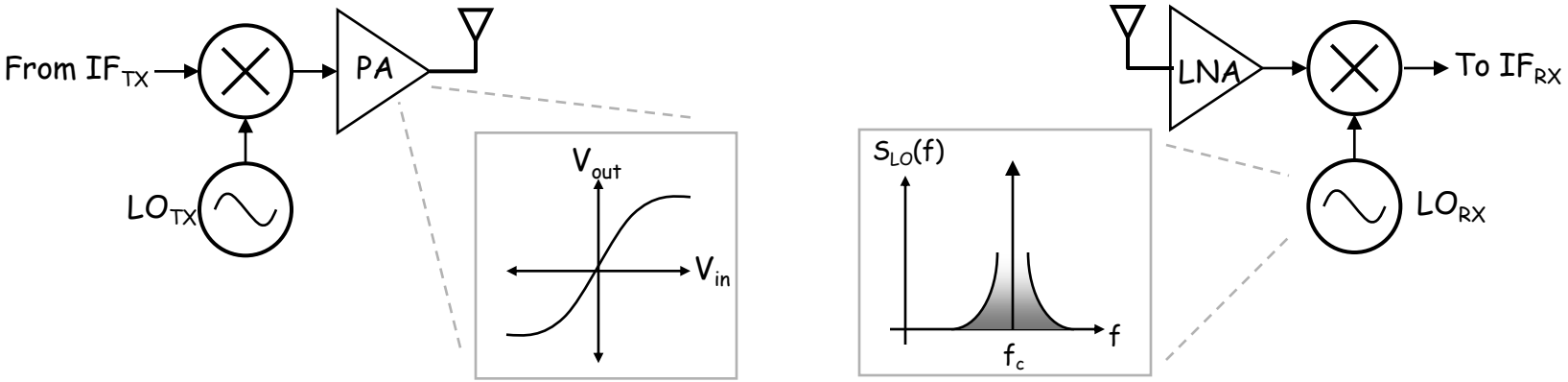
Modulation Scheme: RF Limitations

- 60GHz CMOS PA will have limited P_{1dB} point
  - Tx power constraint while targeting 1Gbps
  - Must use low PAR signal for efficient PA utilization
- 60GHz CMOS VCO's have poor phase noise
  - -85dBc/Hz @ 1MHz offset typical (ISSCC 2004)
  - Modulation must be insensitive to phase noise



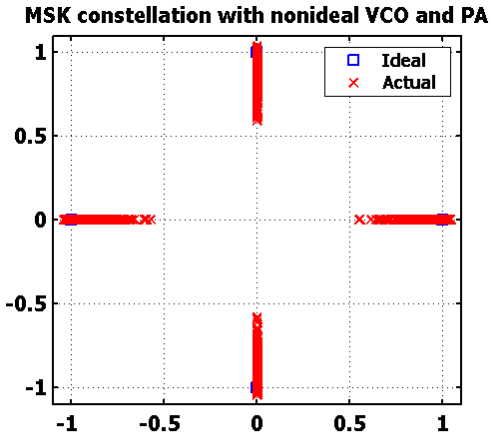
Modulation Scheme: Comparisons

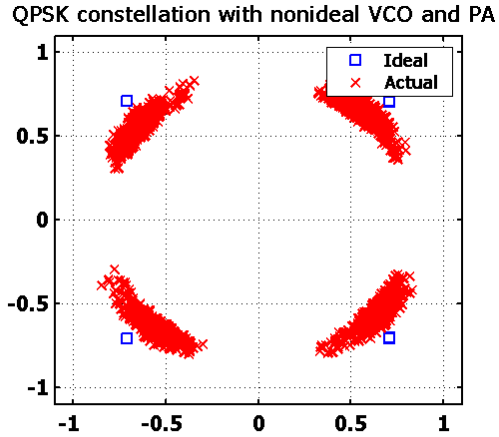
Modulation	OFDM-QPSK	High-order modulation (16-QAM)	Single-carrier QPSK	Constant Envelope (MSK)
SNR_{req} (BER=10^{-3})	7dB	12dB	7dB	7dB
PAR_{TX}	~10dB	~5.5dB	~3dB	0dB
PA linearity req't	High	High	Moderate	Low
Sensitivity to Phase Noise	High (ICI)	High (Symbol Jitter)	Moderate	Low
Complexity of Multipath Mitigation Techniques	Moderate (FFT)	High (Equalizer)	High (Equalizer)	High (Equalizer)

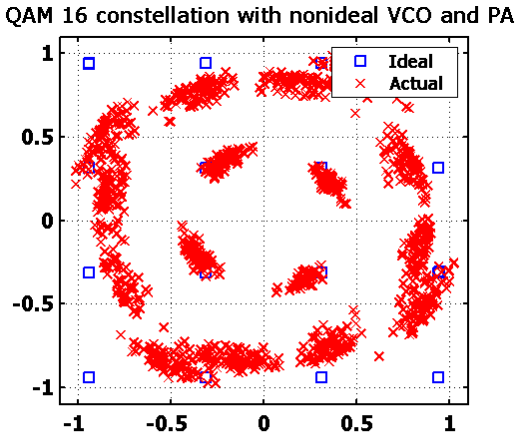
Beamforming to combat multipath.

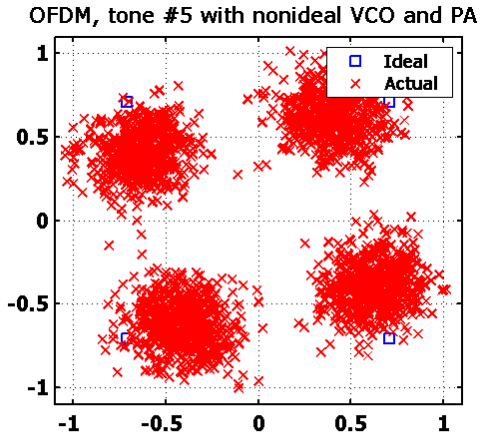
Simple modulation (MSK) for feasible CMOS RF circuits.

Example: PA and VCO nonidealities









Constellation observed at TX output

- No thermal noise

Simulation conditions:

- $P_{TX}=P_{1dB}$
- SSPA AM/AM, AM/PM model [1]
- Lorentzian PN spectrum
  - f_{3dB}=1MHz
  - -85dBc/Hz @ 1MHz

Simulation Results:

- MSK: SNR = 24dB
- SC-QPSK: SNR = 16dB
- OFDM: SNR = 9.5dB

[1] C. Rapp, "Effects of HPA-Nonlinearity…", Proc. 2nd European Conf. on Satellite Comm, 10/91.

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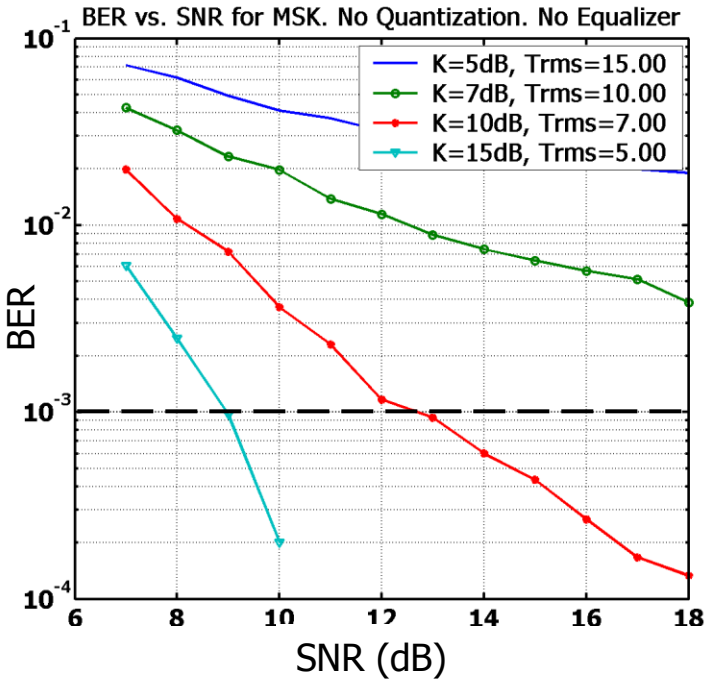
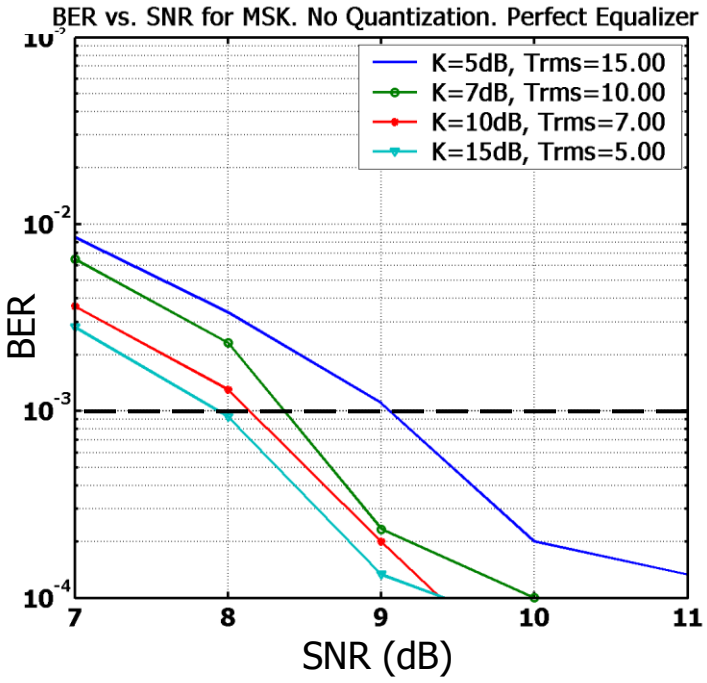
Baseband Architecture Considerations

- Channel equalization still necessary
- DFE well-suited to cancel post-cursor multipath





Note: For all BER plots, 20 instantiations of channel with 3 ksym/inst. used

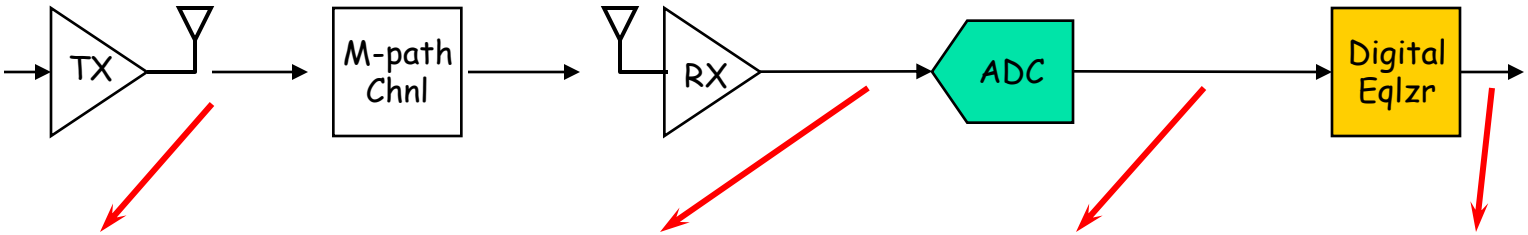
Baseband Architecture Considerations

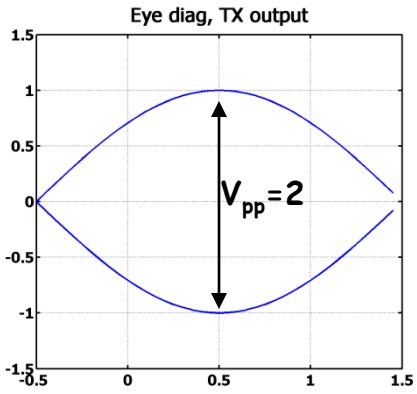
- Targeting 1 Gbps with "simple" modulation scheme
  - Must use low-order constellation, high baud rate
- Fast baud rate (1Gsym/s) ➔ high-speed ADCs, VGAs
- Desire baseband architectures that:
  - Minimize ADC resolution
  - Minimize required ADC oversampling ratio
  - Incurs minimal SNR loss from above simplifications
  - Adaptable, robust to channel variations

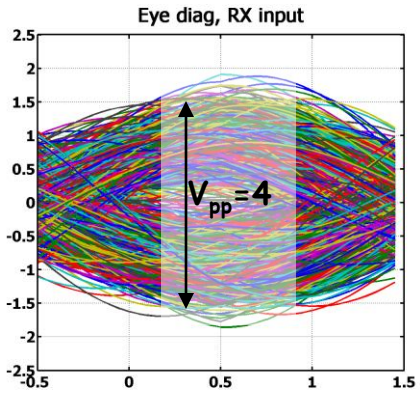
Re-think "traditional" partitioning of analog and digital subsystems!

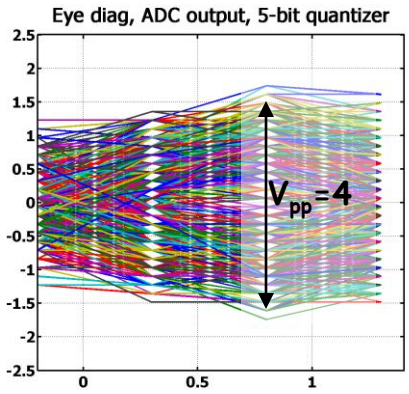
Digital Equalization

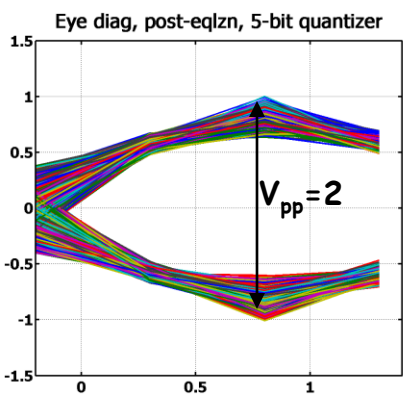
- Multipath increases PAR → additional ADC bits req'd







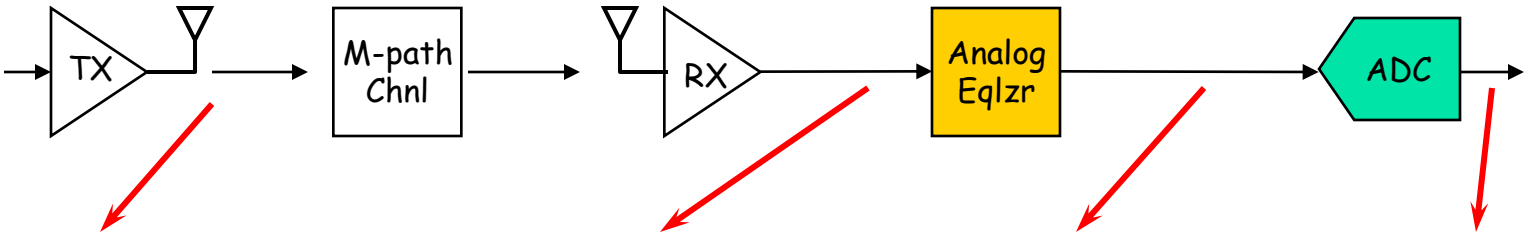


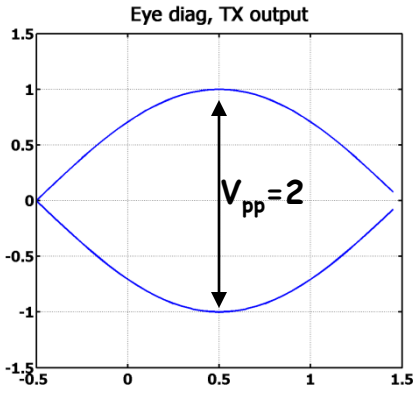


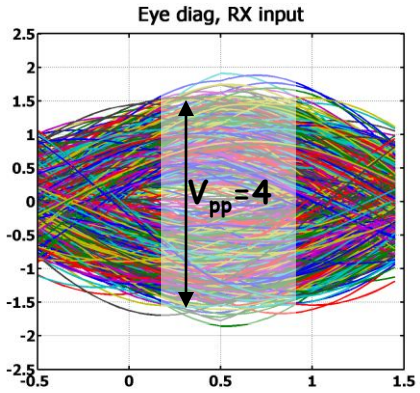
Note: Normalized amplitudes. Channel gain = 1

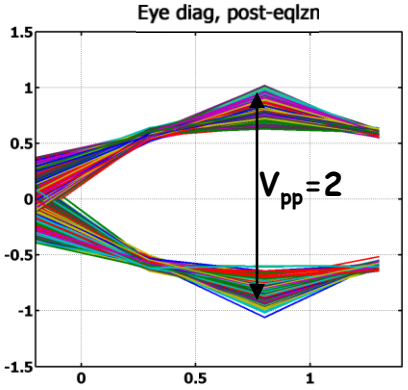
Mixed-Signal Equalization

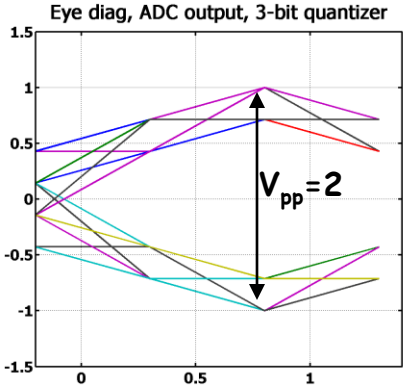
- Mixed-signal equalizer conditions input prior to ADC.
- Fewer ADC bits required





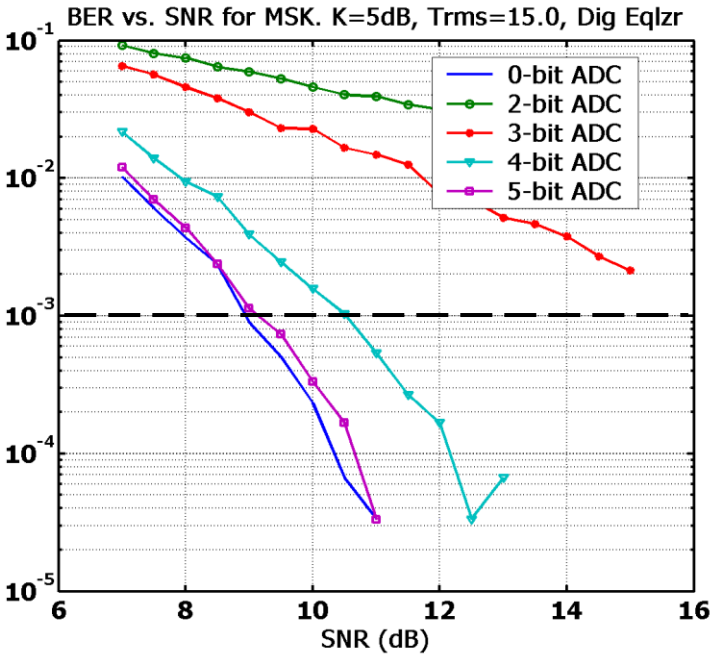


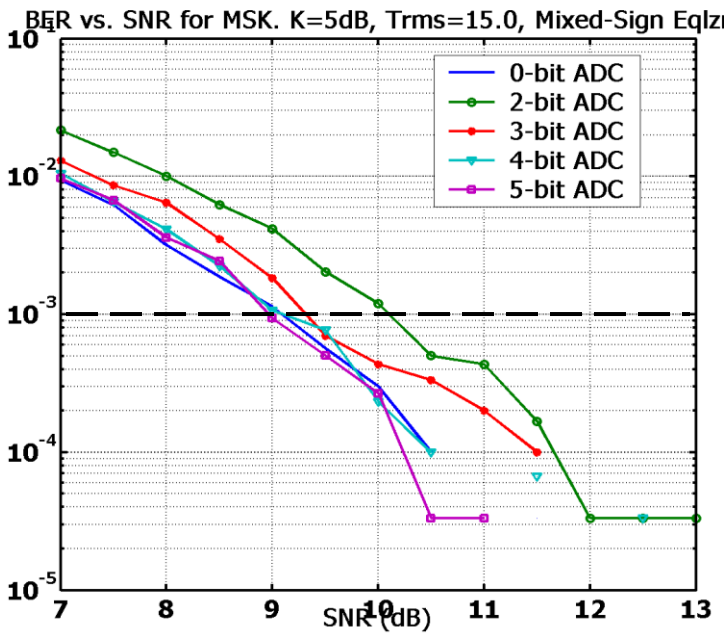




Note: Normalized amplitudes. Channel gain = 1

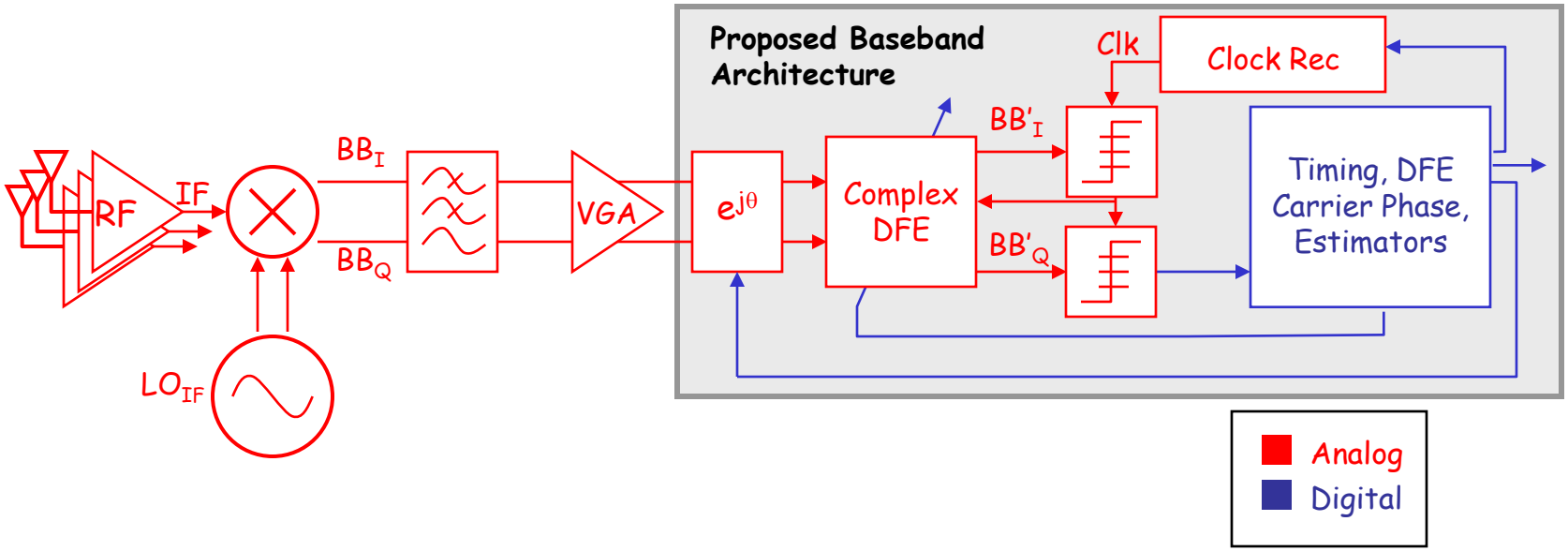
Comparison: Digital vs. Mixed-signal DFE





- Mixed-signal equalizer requires ~2 fewer ADC bits
  - PAR reduction
  - Quantization effects in digital circuits

"Hybrid-Analog" Receiver Architecture



- Synchronization in "hybrid-analog" architecture
  - ESTIMATE parameter error in digital domain
  - CORRECT for parameter error in analog domain
- Greatly simplifies requirements on power-hungry interface ckts (i.e. ADC, VGA)
  - Additional analog hardware is relatively simple

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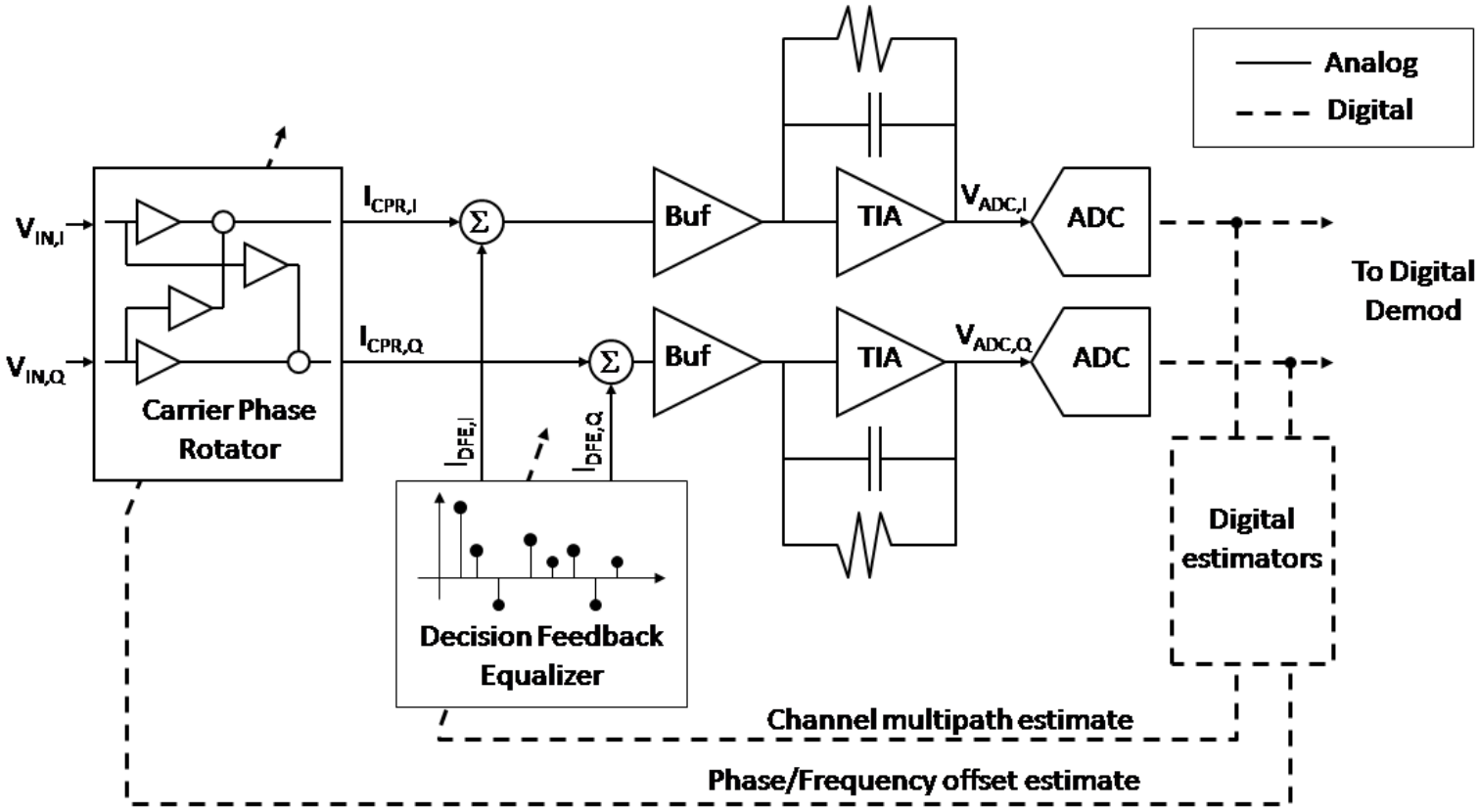
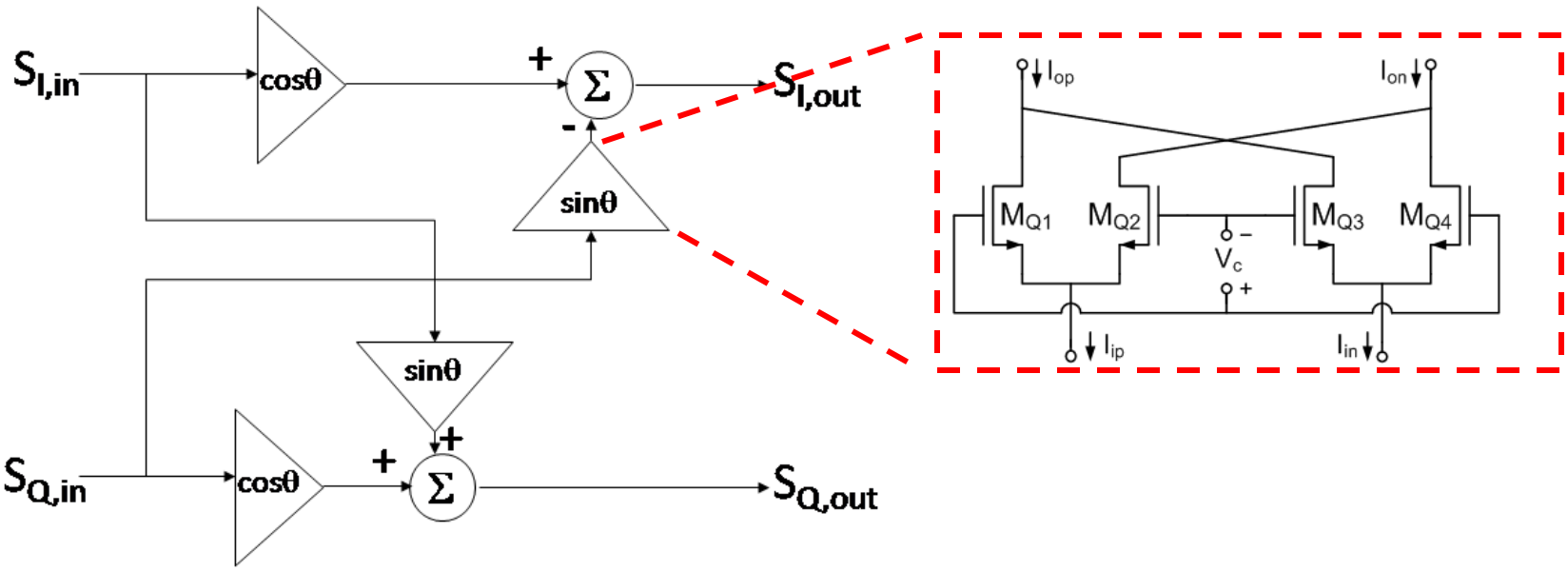
Detailed Circuit architecture



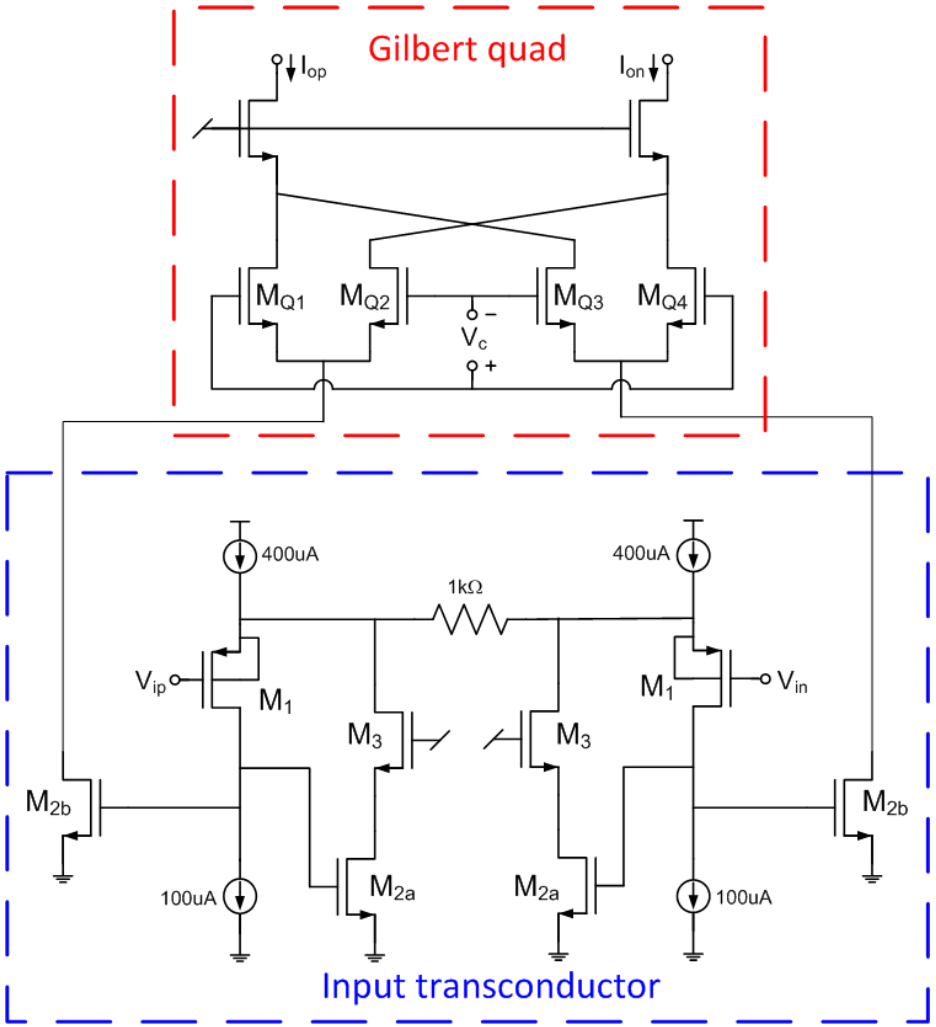
Carrier Phase Rotator

- Implemented as a vector multiplier
- Gilbert Quad is a current-domain multiplier
  - Weak-inversion MOS functions like translinear BJT



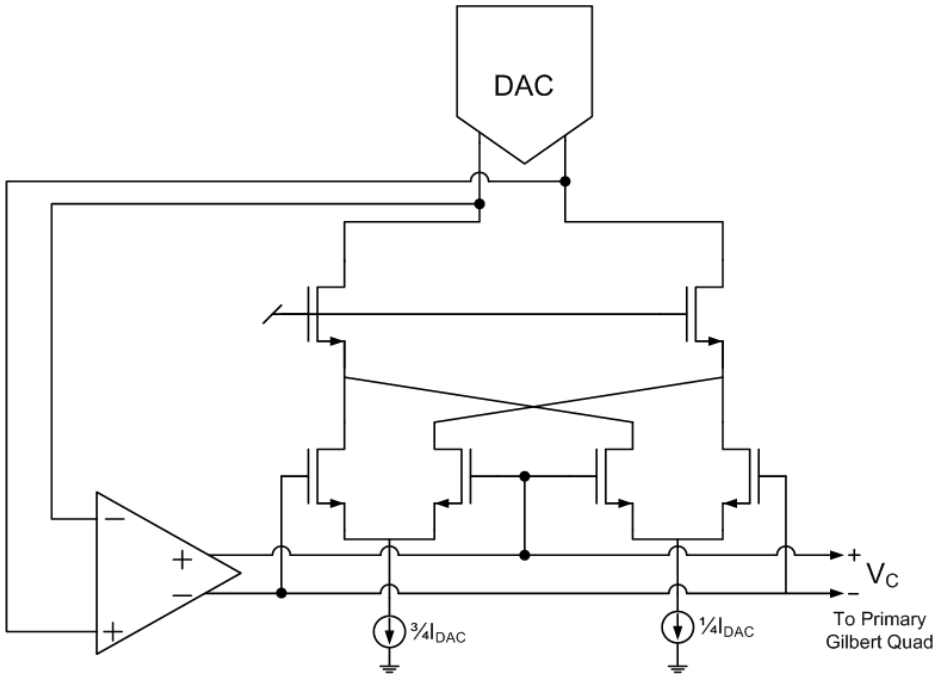
Carrier Phase Rotator Schematic

- Input transconductor uses local feedback
- Gilbert quad performs multiplication by cosθ, sinθ
- Control of V_c required to obtain θ



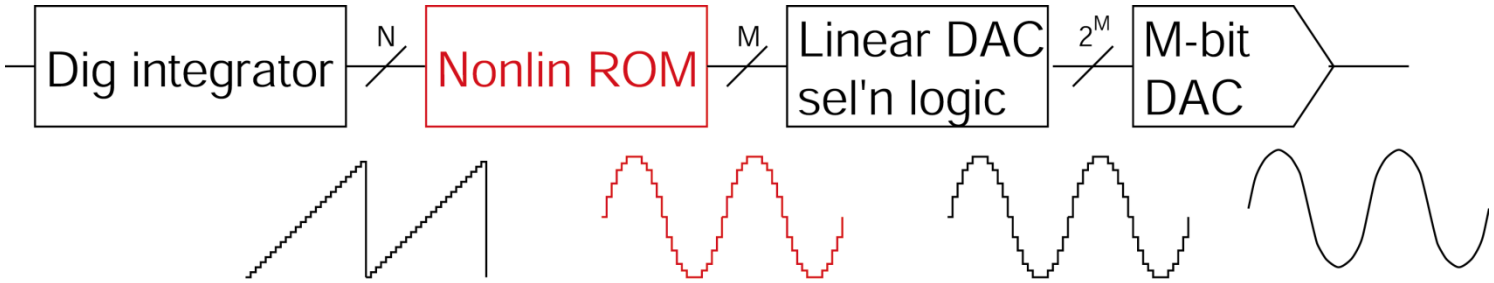
Carrier Rotation Tuning Circuit

- Replica tuning circuit used to generate V_c
- Can use feedback techniques for high accuracy θ tuning
- Rotation angle is due to TX/RX LO mismatch
  - 100ppm crystal ➔ 6MHz BW

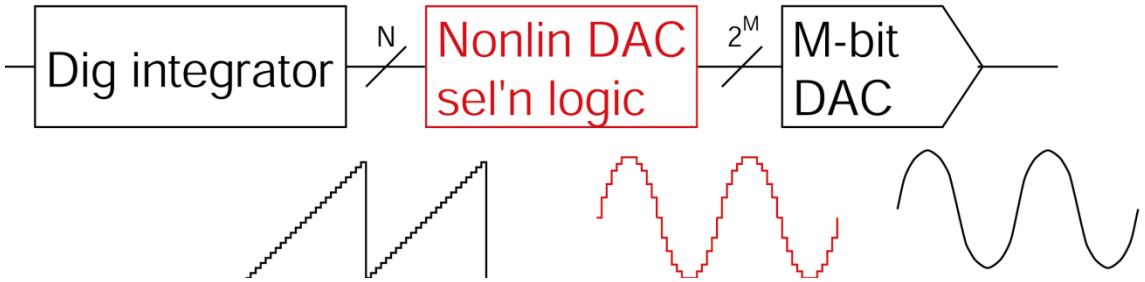


Mixed-signal DDFS

- VGA's require gain of sinϕ, cosϕ
- Traditional DDFS have power-ineffecient ROM table



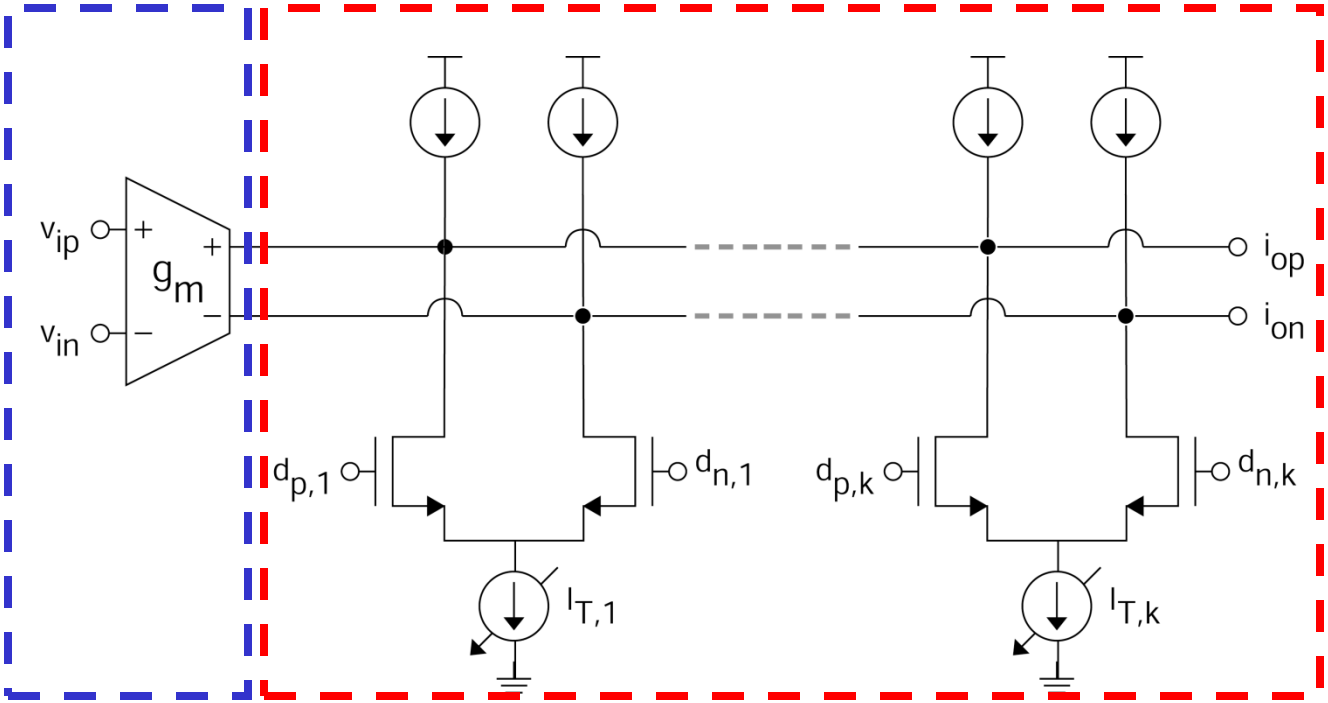
- Can embed trig. operation in DAC element selection logic (*)



(*) see also S. Mortezapour, JSSC 10/99

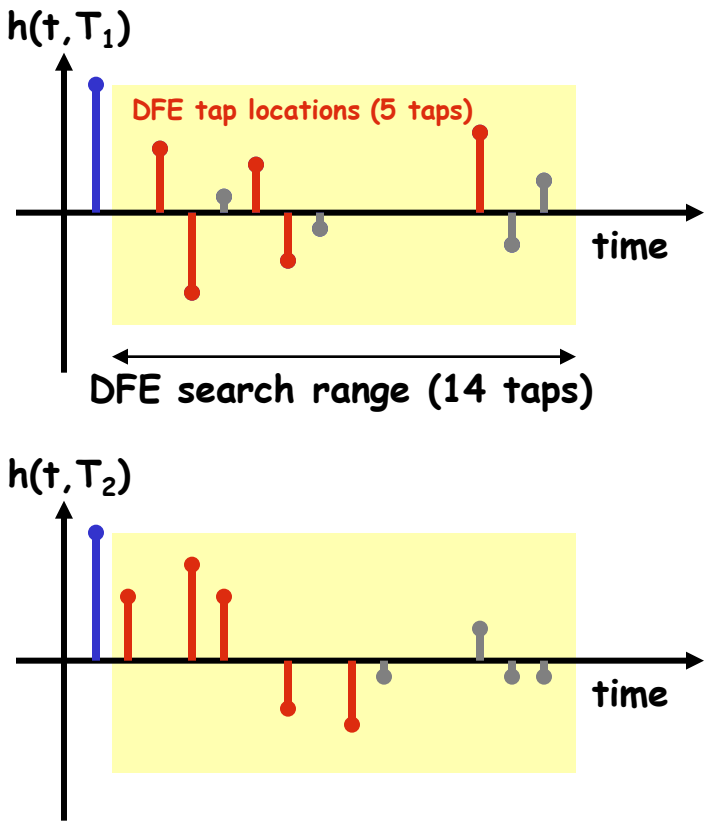
Analog DFE—Current-switching pairs

- Weighted subtraction of past decisions
  - Diff pair fully switches current
  - Each tap current is digitally controlled

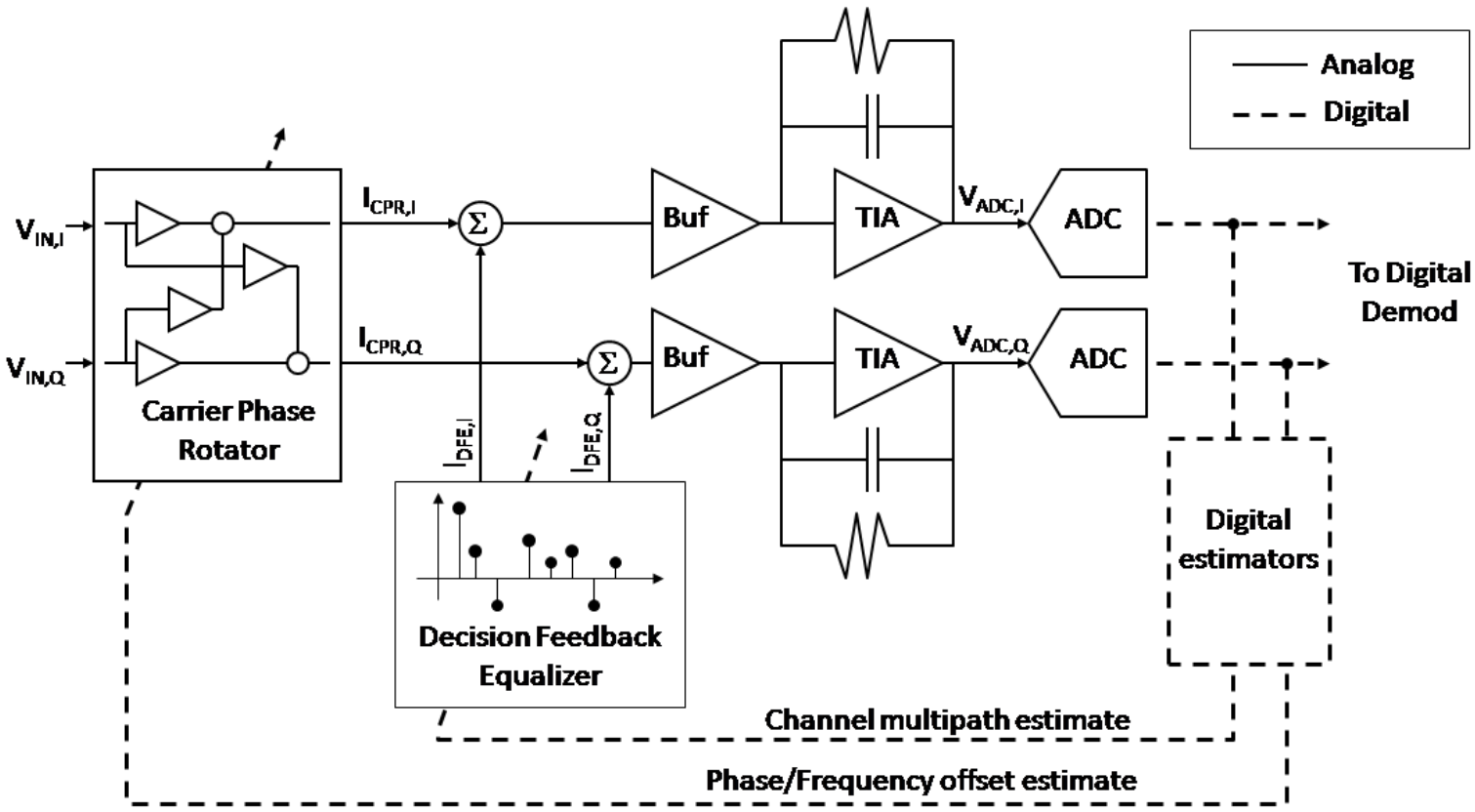


Adaptive DFE Tap Allocation

- 60GHz channel has "sparse" multipath reflections
- Adding more DFE taps adverse effects on equalization process
- Better to adaptively allocate fixed number of taps over DFE correction range

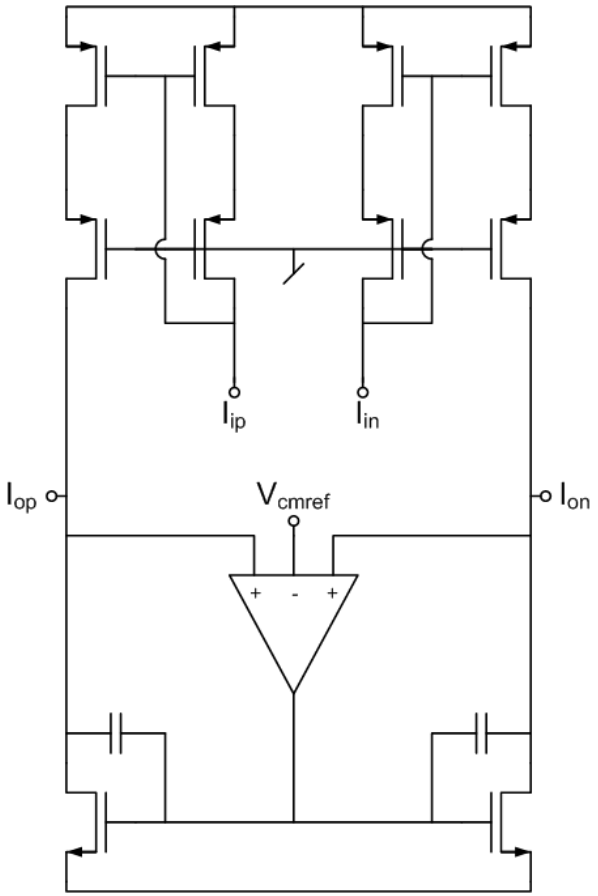


Detailed Circuit architecture



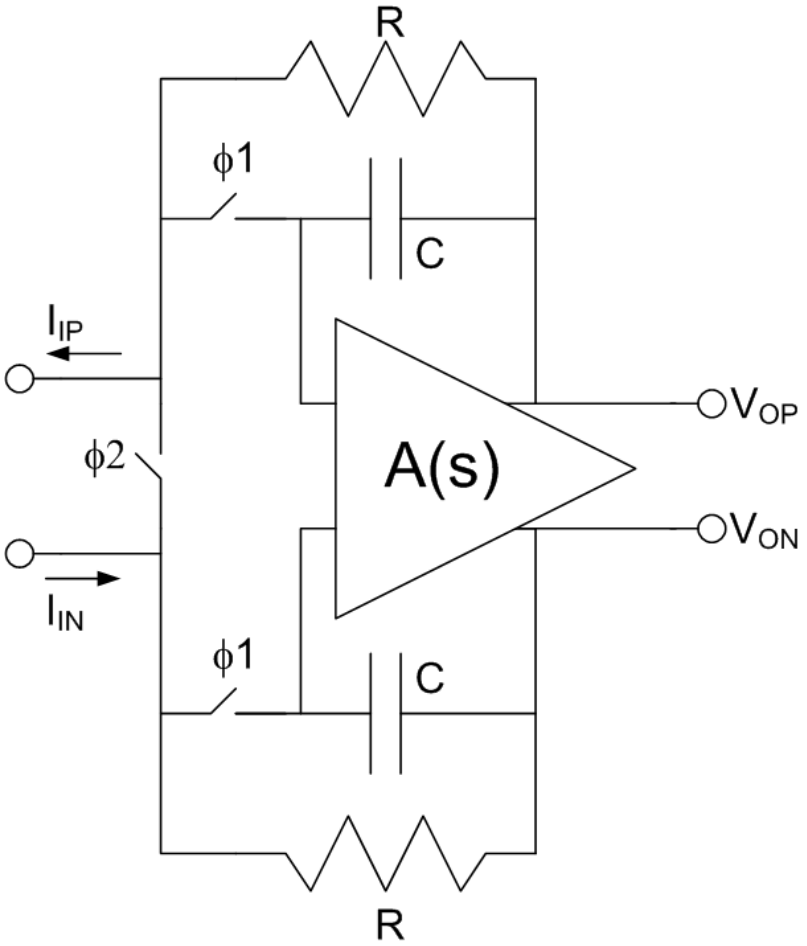
Current-Mode Buffer

- CPR and DFE present large capacitive load
  - Buffer has low Z_{in}
- Subsequent high-speed stage (THTIA) sensitive to capacitance
  - Buffer has high Z_{out}
- Feedback used for output common-mode control

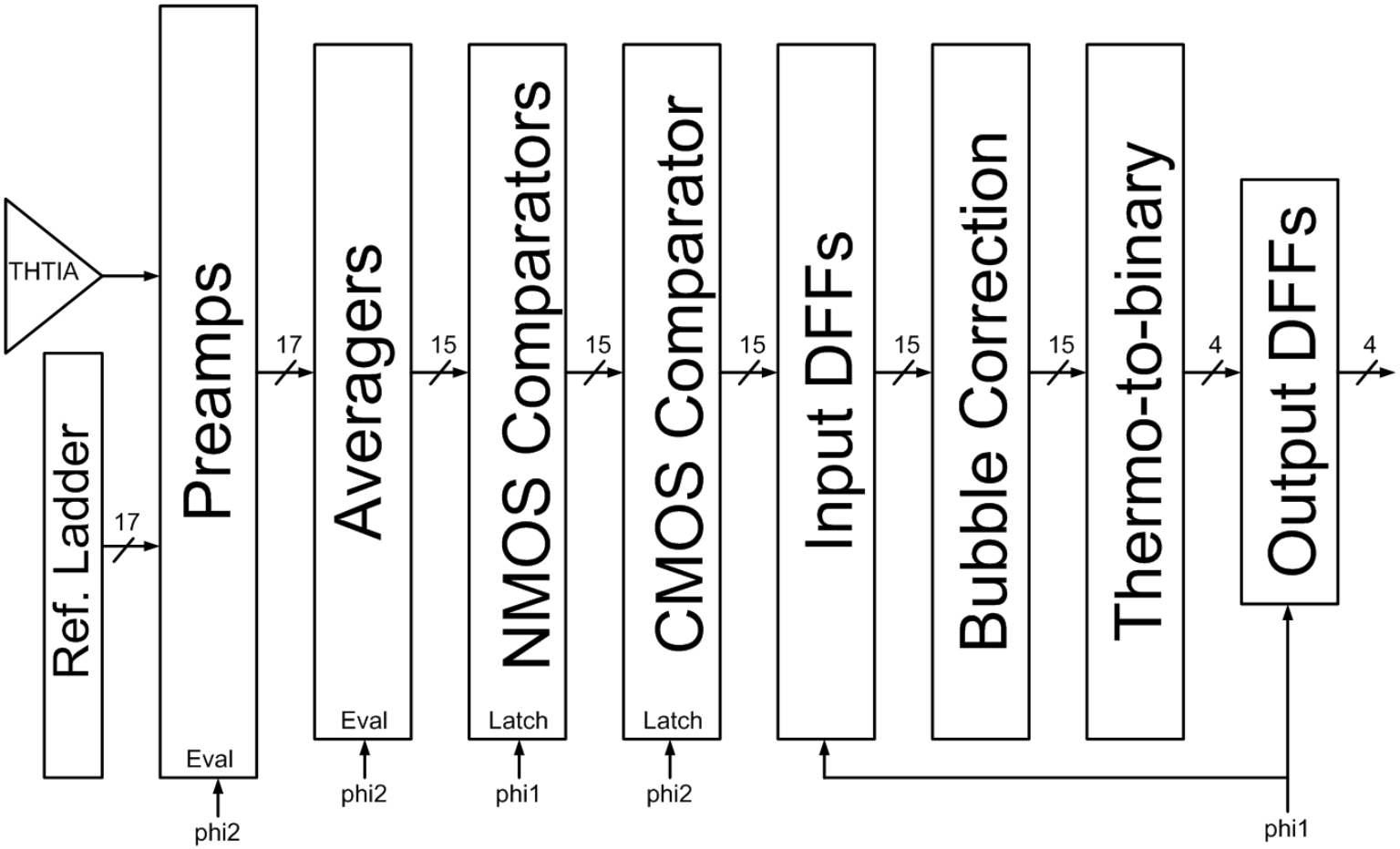


Track-and-hold Transimpedance Amplifier (THTIA)

- During phi1, circuit is a transimpedance amp
- During phi2, output voltage is held across C
- Feedback factor ~ 1
  - Enables high-speed operation

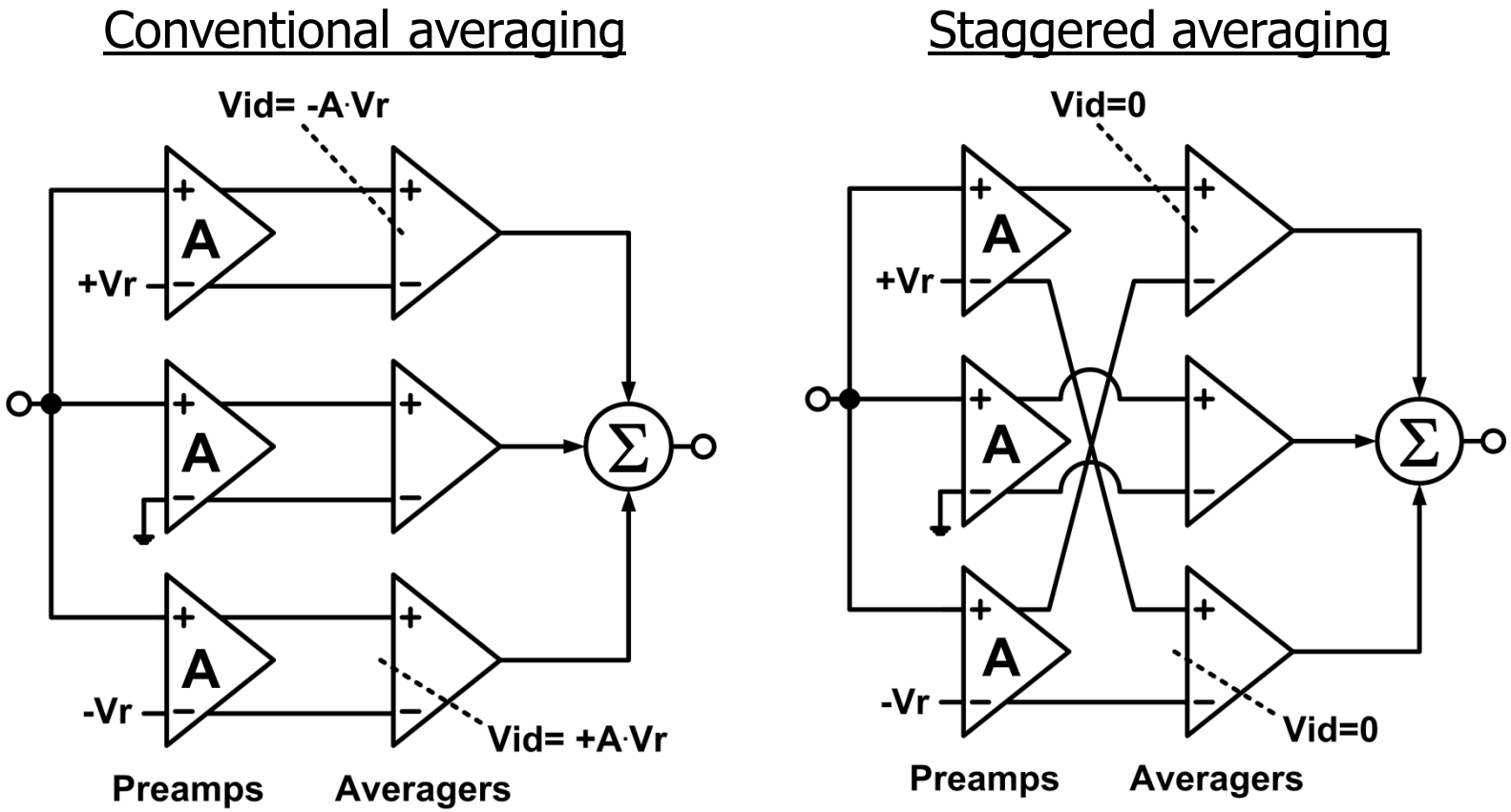


4-bit, 2Gs/s Flash ADC architecture



Flash ADC—Active Averaging

- Staggered active averaging decouples preamp gain and averager input range



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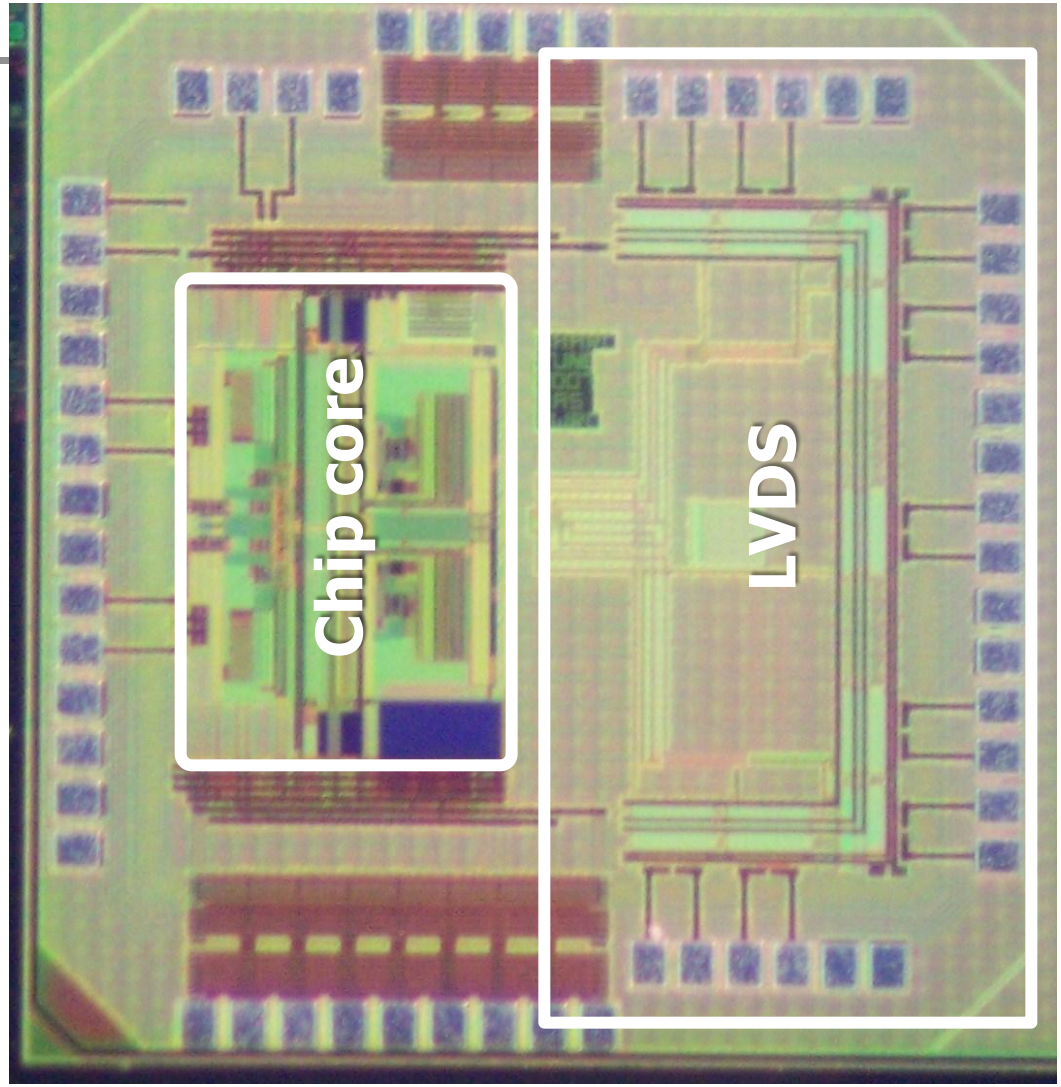
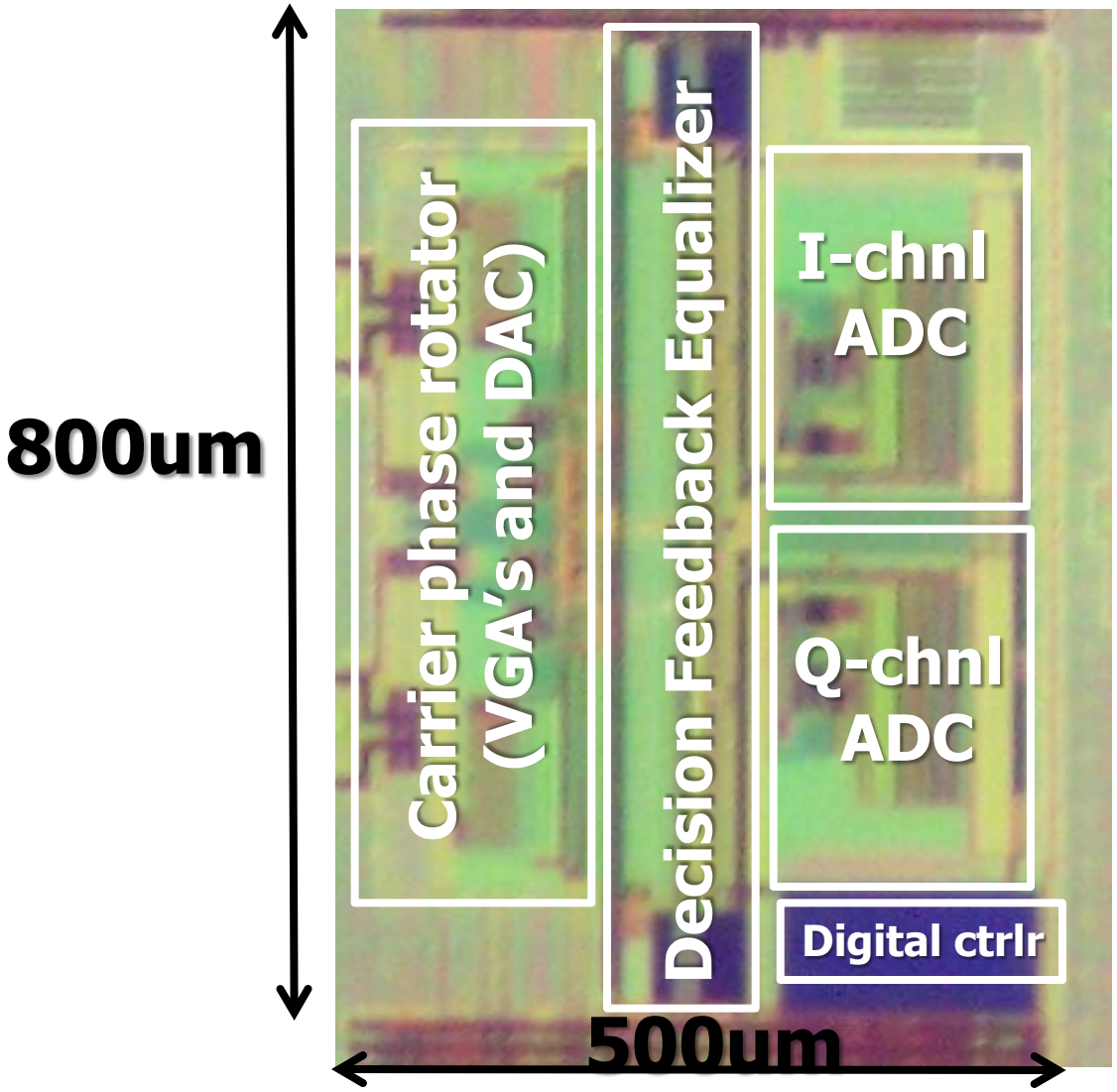
SHARC chip

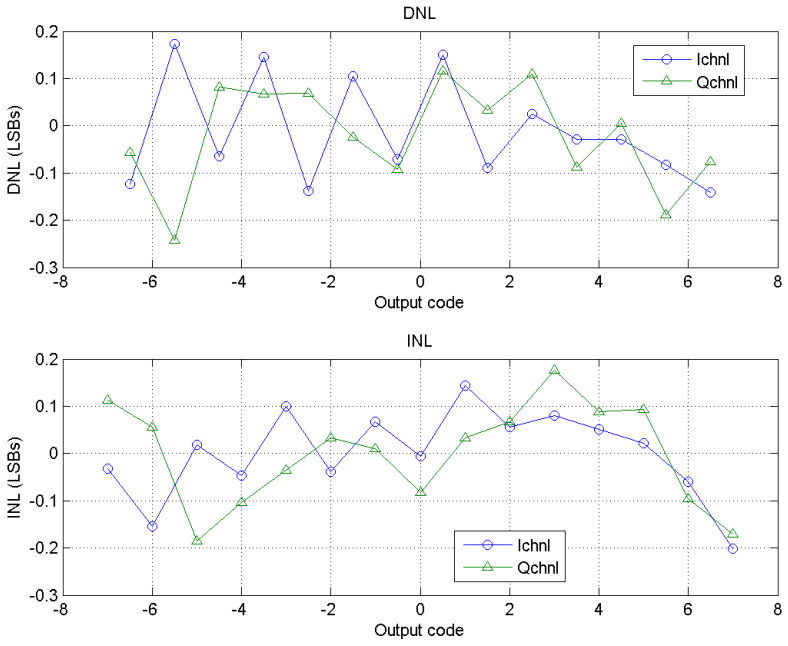
- 1.5mm x 1.55mm (pad-limited)
- Chip includes:
  - Two 2Gs/s, 4-bit ADCs
  - Carrier phase rotator (4x VGA's and 2x DDFS DAC's)
  - One 1Gs/s, 16-tap I/Q DFE
  - 9 LVDS output pairs
  - Digital controller

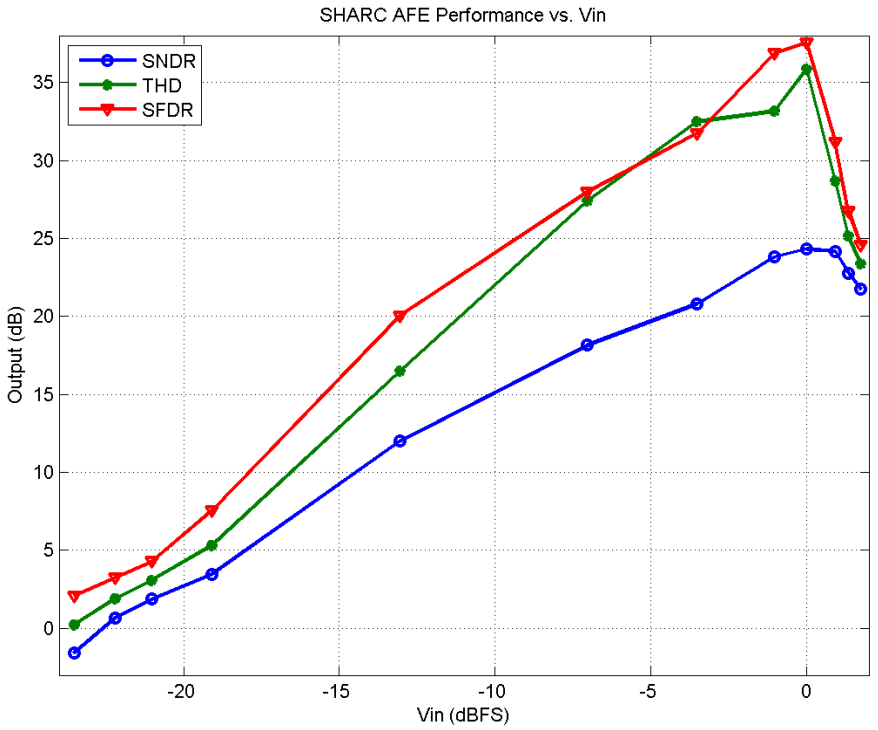


SHARC chip (zoomed in)



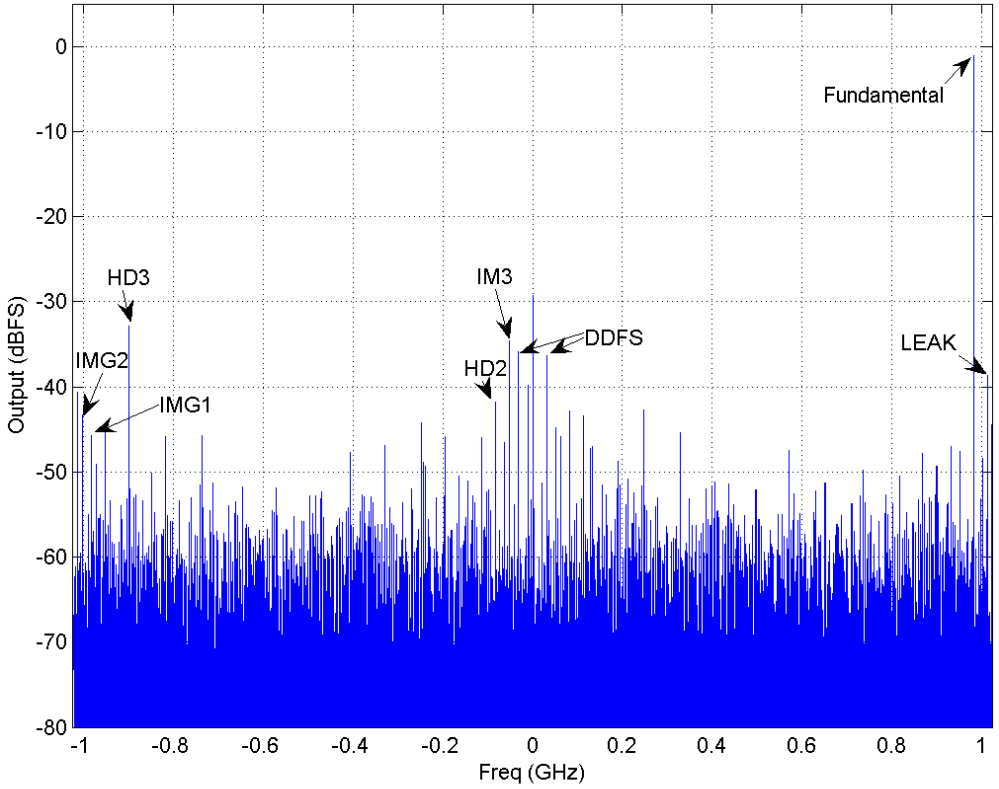
Measured Results (ADC)





- Nyquist-rate testing (F_{sig}=1GHz, F_{clk}=2.048GHz)
- 24.7dB peak SNDR, 35.5dB THD, 44dB IMD3
- INL and DNL less than +/- 0.2LSB

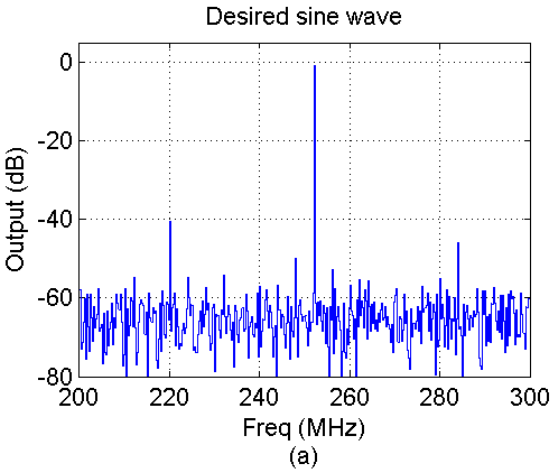
Measured Results (CPR)

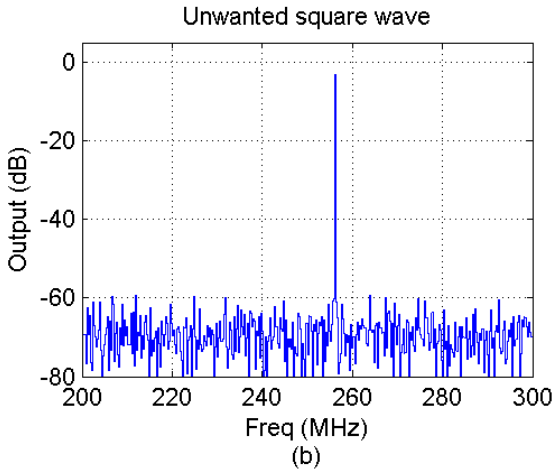


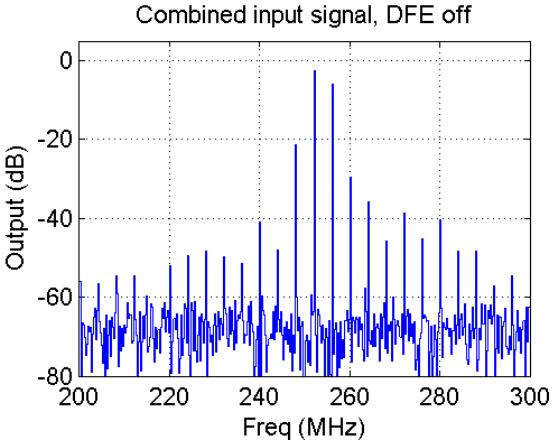
- Quadrature input:
  - F_{IN} = 1014MHz
  - F_{DDFS} = -31MHz
- Image tones < -42dBc
- Leakage tone < -37dBc
- Quadrature matching: 0.1dB, 0.7^{o}

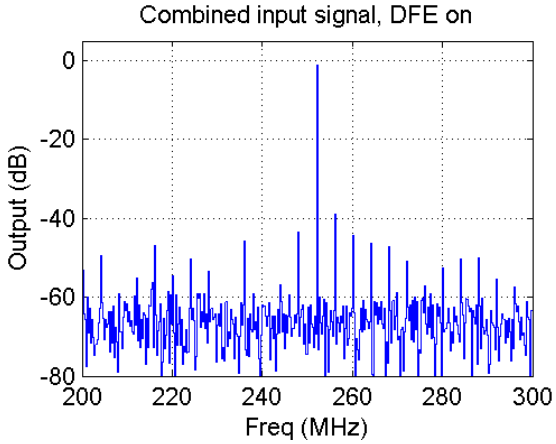
Measured Results (DFE)

- Input signal: (Desired) sine wave and (unwanted) square wave
- With DFE off:
  - ADC clips
  - Heavy IMD (-19dB)
- With DFE on:
  - 33dB cancellation of square wave
  - IMD < -42dB









Performance Summary

Technology		90nm 9M1P Digital CMOS	
Package		Chip on board	
ADC	Sample Rate	2 Gs/s	
	Peak SNDR	24.8dB	
	SFDR	38dB	
	IMD3	-40dB	
CPR	DDFS clock speed	500MHz	
	DDFS resolution	8 bits (1.4°)	
	Image tones	< -37dB	
	I/Q matching	< 0.1dB, < 0.7°	
DFE	Clock speed	1GHz	
	INL/DNL	< 0.06 LSB	
	Linearity	>40dB	
Power	CPR	11mW	Total : 55mW
	DFE	14mW	
	THTIA	2 @ 5mW	
	ADC	2 @ 10mW	

- Dynamic range comparable to 6-bit systems
  - Compare to: 110mW for two 6-b, 2Gs/s 90nm ADC [VLSI 2007]
- Full carrier sync and DFE functionality

Conclusion

- An analysis of modulation schemes appropriate for use with a 1Gbps, 60GHz all-CMOS receiver
- The design of a mixed-signal baseband receiver architecture to reduce overall power dissipation and complexity
- A full analysis and simulation of the proposed receiver architecture
- The design and implementation of the proposed receiver in a 90nm digital CMOS process

Acknowledgements

- BWRC member companies
- TSMC for providing silicon fabrication
- DARPA TEAM program
- NSF Infrastructre Grant
- Faculty, students and staff at the BWRC