IEEE SCV Signal Processing Society

Date: Feb 12th 2007
Title: A/D and D/A Converters with Integrated High-speed Compression
Speaker: Al Wegener, CTO, Samplify Systems, Inc

Location: National Semiconductor (north end of Building E - see maps on the Chapter web site *http://www.ewh.ieee.org/r6/scv/sps/*), 2900 Semiconductor Dr., Santa Clara, CA 95051 (Near the intersection of Lawrence and Central Expressway);

Directions: Take 101 to Lawrence Expressway. Head south on Lawrence to Kifer (past Central). Turn right on Kifer. Turn right on Semiconductor Dr. and drive all the way back to north end to Buldg E. Entrance is on the West side of the building.

Time: 6:30pm: Fast Food & drinks ($1 Donation Recommended towards Refreshments)
7:00pm: Announcement
7:05pm: Talks starts

Abstract:
Various compression methods have become integral components of computer systems (WinZIP), audio distribution (MP3), and video processing (MPEG, H.264). However, effective and efficient compression techniques for high-speed A/D and D/A converters have not been available. This talk describes the Samplify series of algorithms, which provides both lossless and lossy compression of bandlimited, sampled data acquired by A/D converters, or provided to D/A converters, and then further processed by FPGAs or ASICs. Samplify provides a lossless compression mode whose compressed data rate varies, depending on the redundancy present in the signal. Samplify also offers two complementary lossy compression modes, in which users select either a desired compression ratio (such as 2.05:1 or 3.68:1) or a desired dynamic range (such as 65.5 dB). Examples using common, bandlimited signals demonstrate the rate-distortion tradeoffs enabled by the Samplify algorithms. Improved compression ratios can be achieved by combining a training phase, in which the signal's characteristics are discovered, with a compression phase. The Samplify algorithms require a modest amount of FPGA resources and operate at up to 200 Msamp/sec. Higher sample rates are achieved by instantiating parallel compression and decompression blocks.

Biography:
Al Wegener, is the founder and CTO of Samplify Systems, a venture-funded start-up whose patented compression solutions reduce bandwidth and storage bottlenecks in sampled data systems. Mr. Wegener is a DSP engineer, technical manager, and inventor with more than 25 years of experience in defense electronics, professional and consumer audio, and wireless applications. Mr. Wegener founded Samplify Systems to bring the benefits of high-speed lossless and lossy compression to signal processing systems at sampling rates above 10 Msamp/sec, where no effective compression solutions were previously available. Prior to Samplify Systems' first venture funding, Mr. Wegener was the technical manager of Texas Instruments' Palo Alto ASIC design center (formerly Graychip), where he was the project lead and chip evangelist for the GC1115 crest factor reduction processor. Mr. Wegener holds a BSEE from Bucknell University and an MSCS from Stanford University. Mr. Wegener holds nine issued U. S. patents and is named on seven additional, pending Samplify Systems patents.