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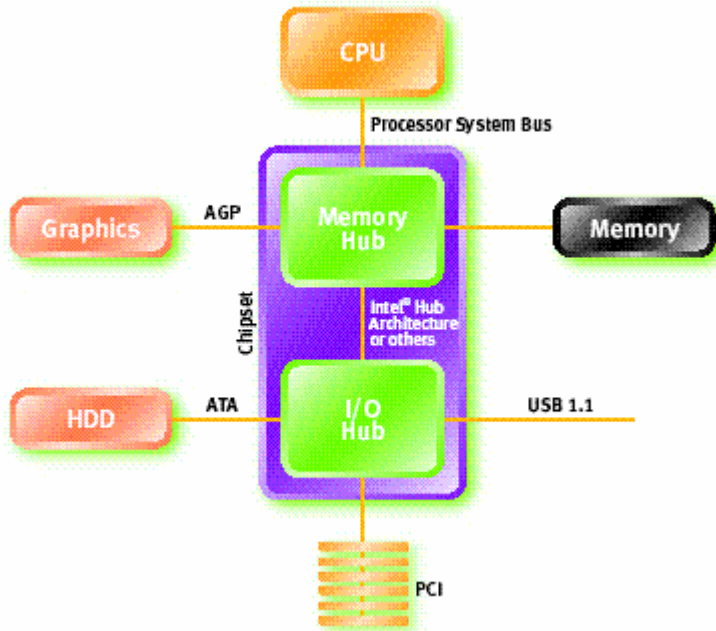
"Overview of Significant Changes in Computer Architecture and
Tackling the Challenges of High Speed Digital Interfaces"

...with a Focus on PCI and Memory

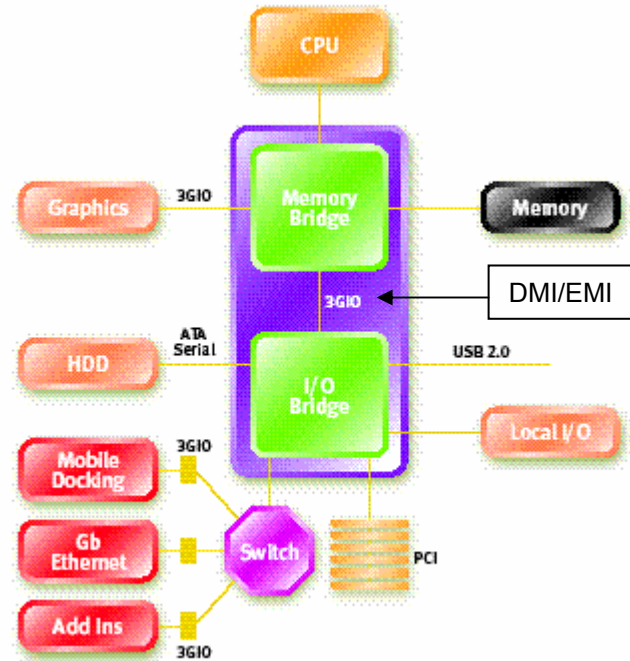
Agenda

- Changes in chipsets
- Intro to current/new interfaces
- Commonalties in interconnects (serial/parallel)
- Tool lifecycle
- PCI Express (including new tools)
- Fully Buffered DIMM (including new tools)

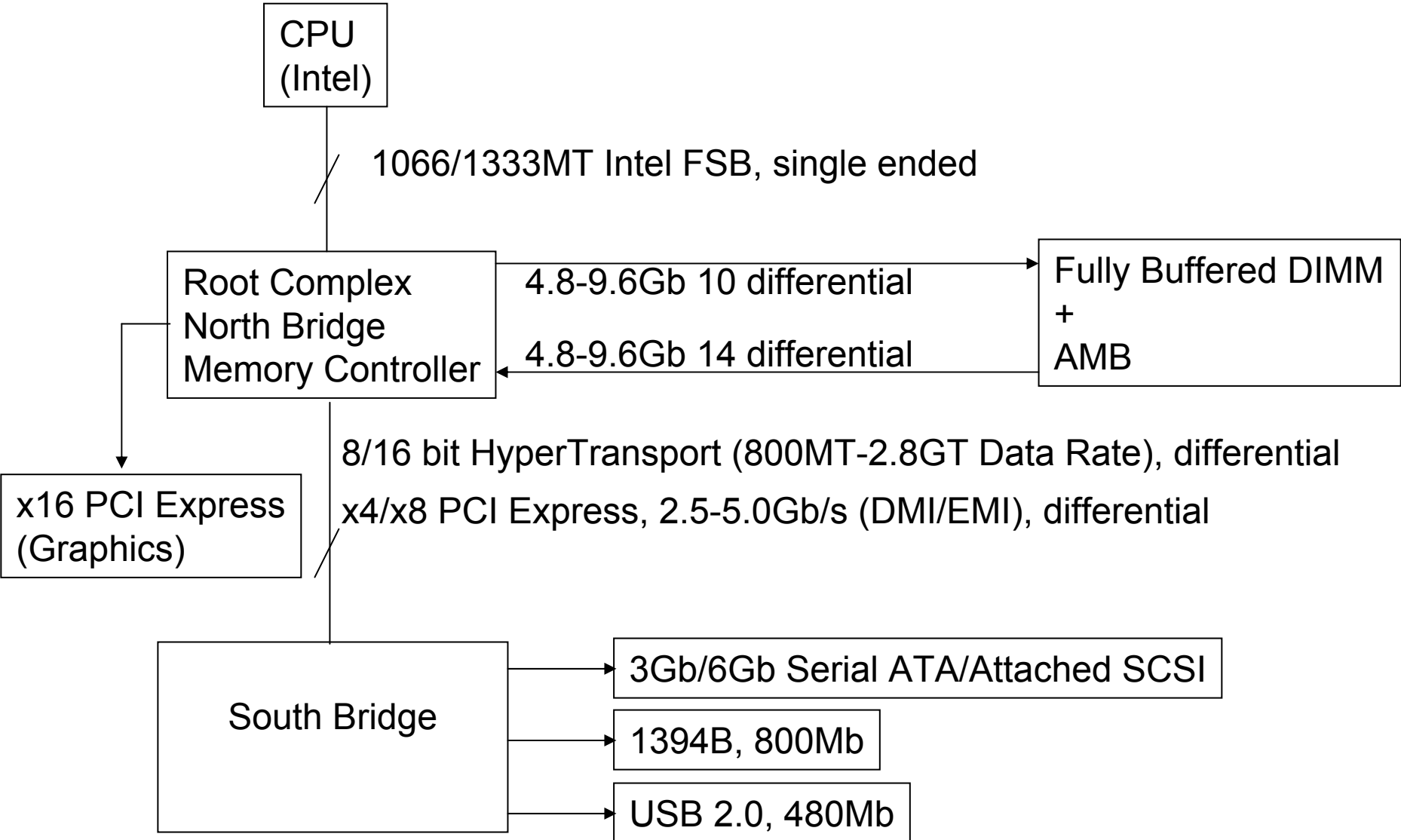
Computer System Topologies

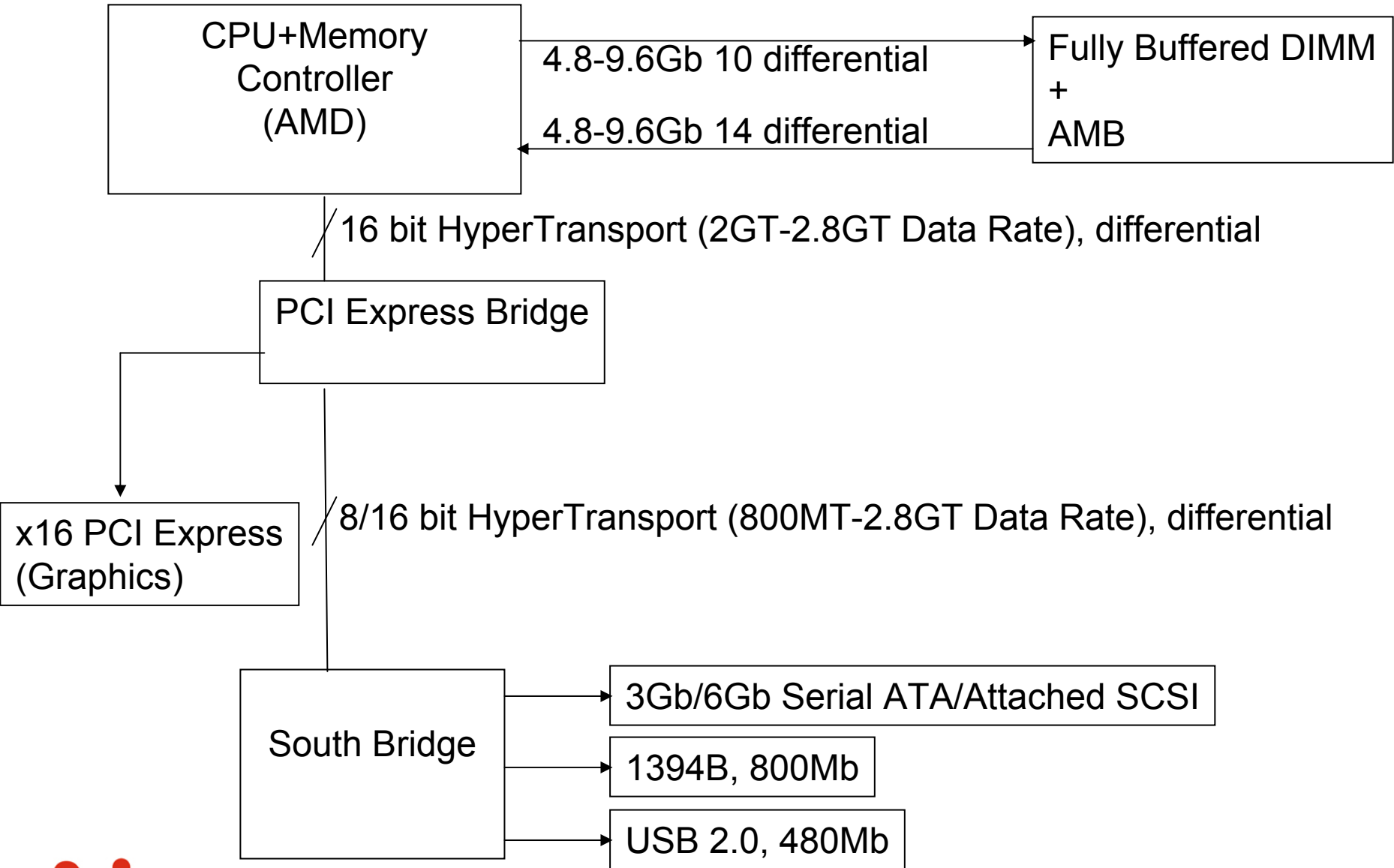


Mid 90's



Circa 2002





Digital Technologies in the Bay Area

- Serial ATA/Attached SCSI
- Fully Buffered DIMM
- PCI Express
- PCI-X 2.0
- Hypertransport
- Intel FSB
- DDR I/II/III
- USB 2.0/Firewire 1394B
- Infiniband 1x, 4x, 12x
- FibreChannel 4Gb/s, 6/8Gb/s, 10Gb/s
- 1Gb/s, XAUI 10Gb/s Ethernet over copper
- Advanced TCA
- SPI 4.2
- Serial Rapid I/O
- Digital Video Interface
- High Definition Multimedia Interface



Transitions and Commonalities in Interconnect Technology

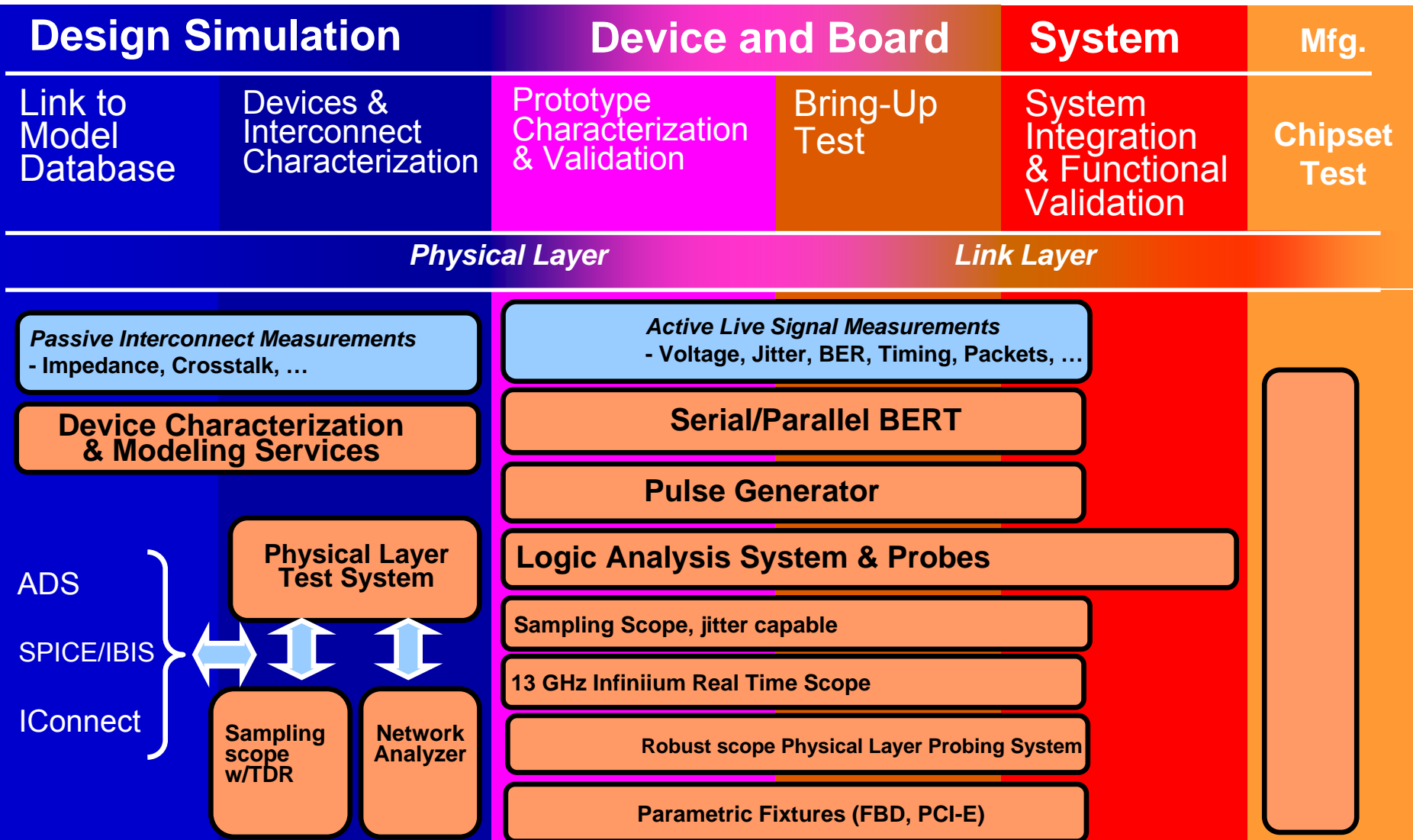
High Speed Serial

- Differential Signaling
- Embedded Clock, CDR
- Spread Spectrum, EMI Reduction
- Reduced Pin/Signal Count
- Packet Based Transactions
- Improved Quality of Service

High Speed Parallel

- Differential (e.g. FBDIMM, HyperTransport)
- Single Ended (e.g. DDR2, DDR3, Legacy Intel FSB)
- Clk rates increased (multi-gigabit)
- Reduced slot count (e.g. PCI-X, DDR3)
- Improved Quality of Service, ECC
- Reduced Pin/Signal Count

Lifecycle Tools for Multi-Gigabit Designs

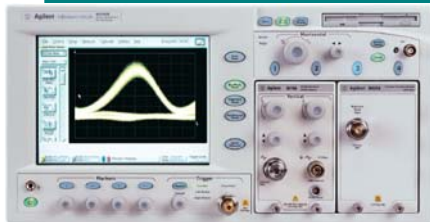
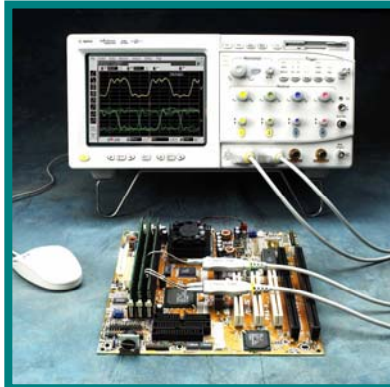
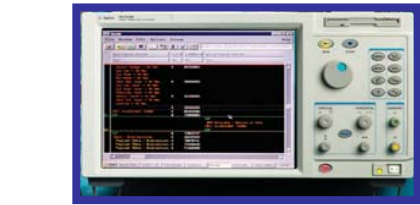
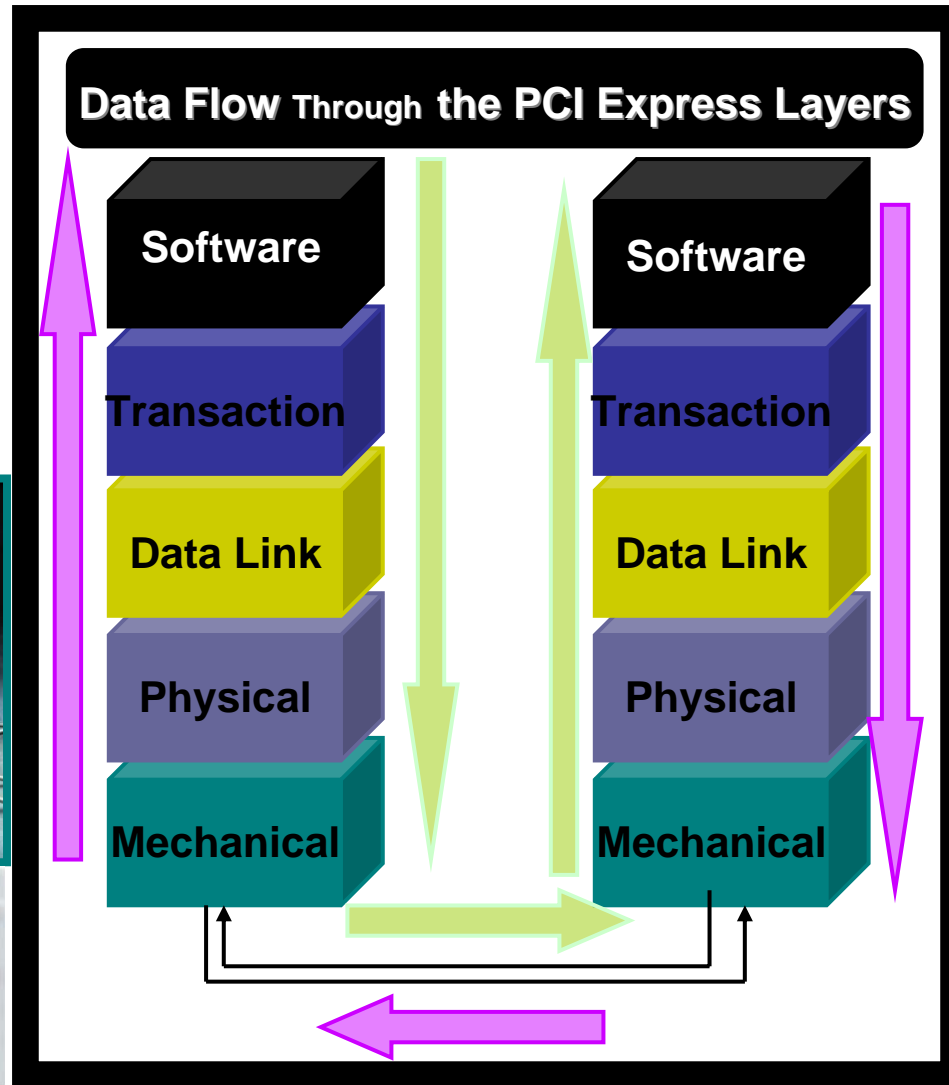


PCI Express Validation Methodologies

Rohit Bhasin
Agilent Technologies

Presented at PCI-SIG
Developers Conference
June 2004

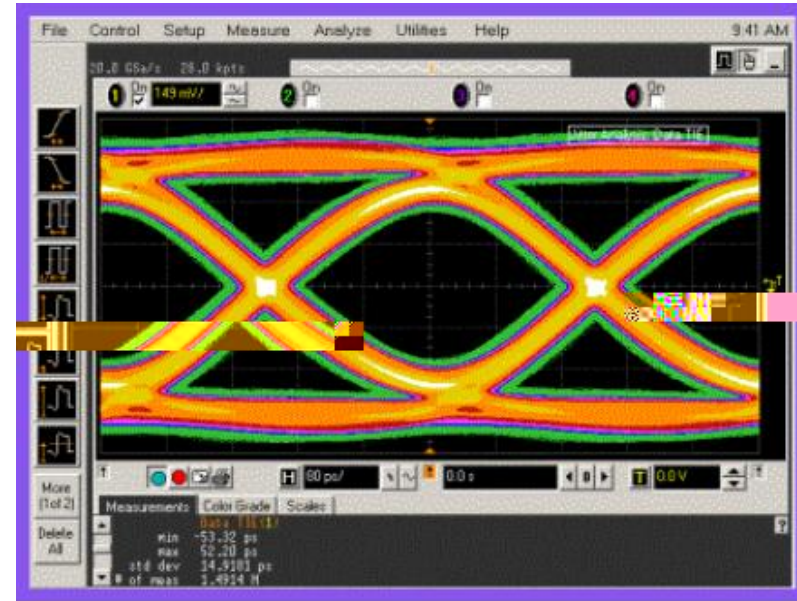
PCI Express Debug Challenges



PCI Express Validation Steps

Signal Integrity - Verify the 2.5/5.0 Gb design

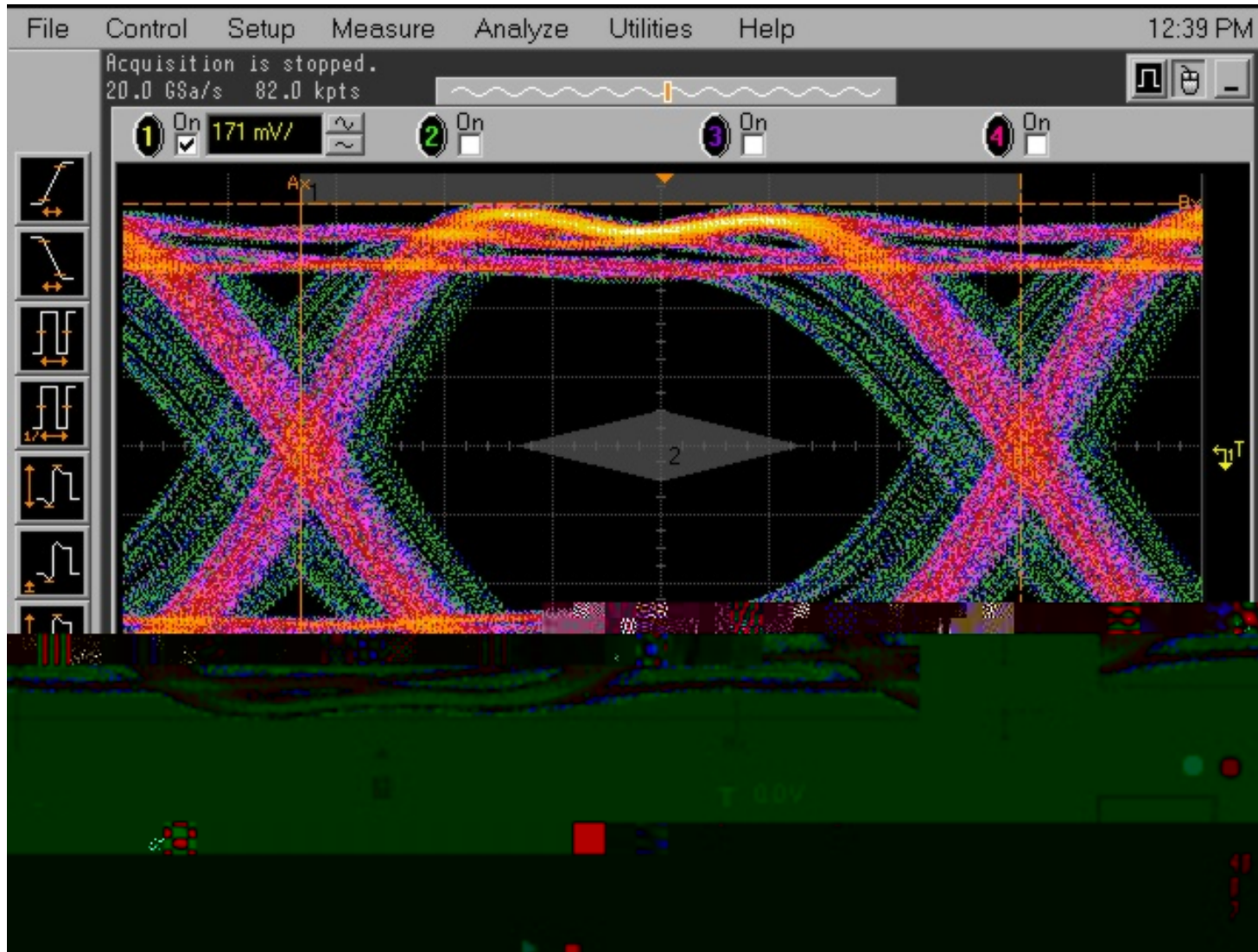
- Eye Measurements
- Capture waveforms
- Measurement on parameters (jitter analysis, mask test, etc.)
- Board and Component characterization
- BERT



Serial Data Analysis Toolkit

- Clock recovery and serial data analysis for high-speed serial data signals
- Masks for PCI Express, Serial ATA/Attached SCSI, Fibre Channel, and XAUI
- Real-time eye diagram display
- Time interval error (TIE) jitter measurement
- First-order or second-order PLL clock recovery, and PCI Express clock recovery (provided by PCI-SIG)

An example using the Serial Data Tool

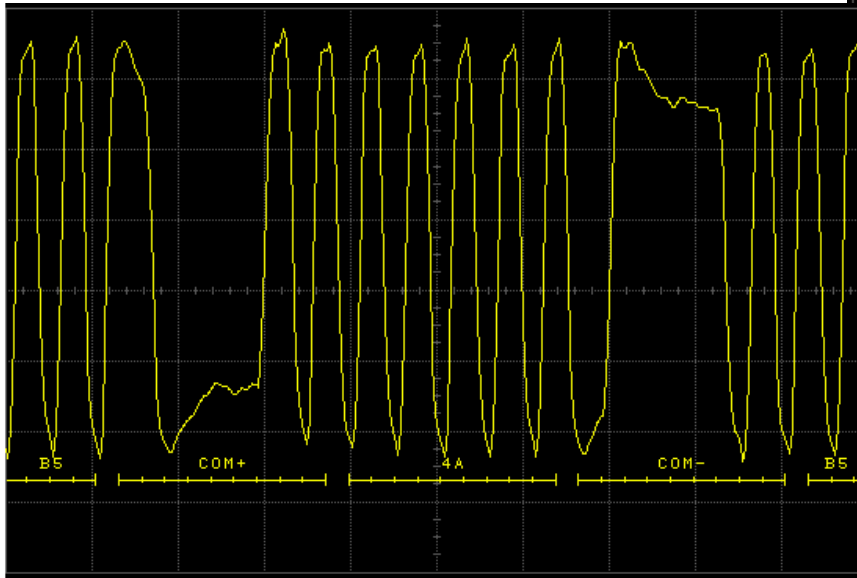
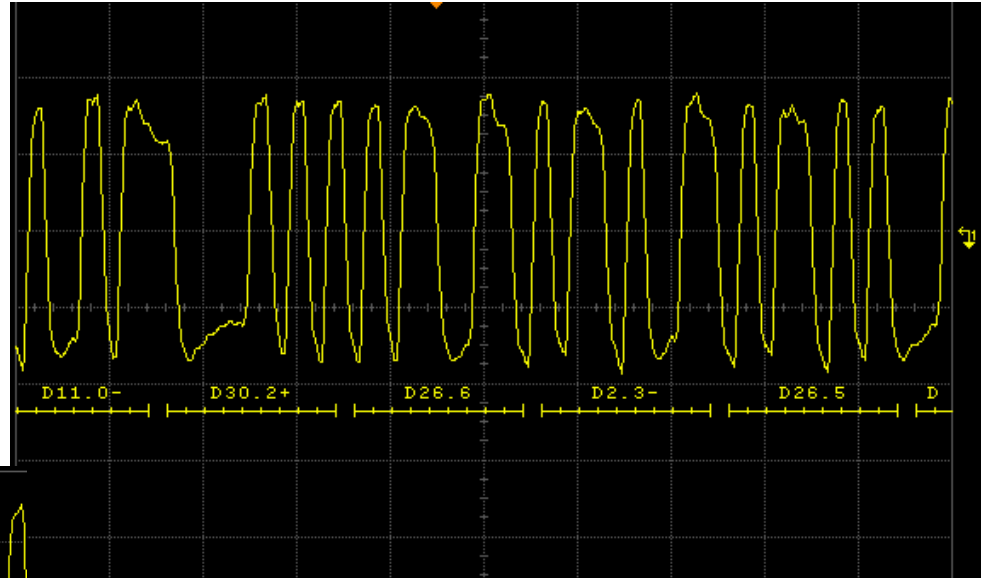


Features and Capabilities

- 8b/10b decoding
- 8b/10b search
- 8b/10b trigger
- Real time eye mask violation unfolding

8b/10b Decoding

Symbols in the serial data stream can be decoded and displayed as hex or decimal values, or as labels



Search and trigger

Display only those acquisitions where the specified sequence of symbols is found

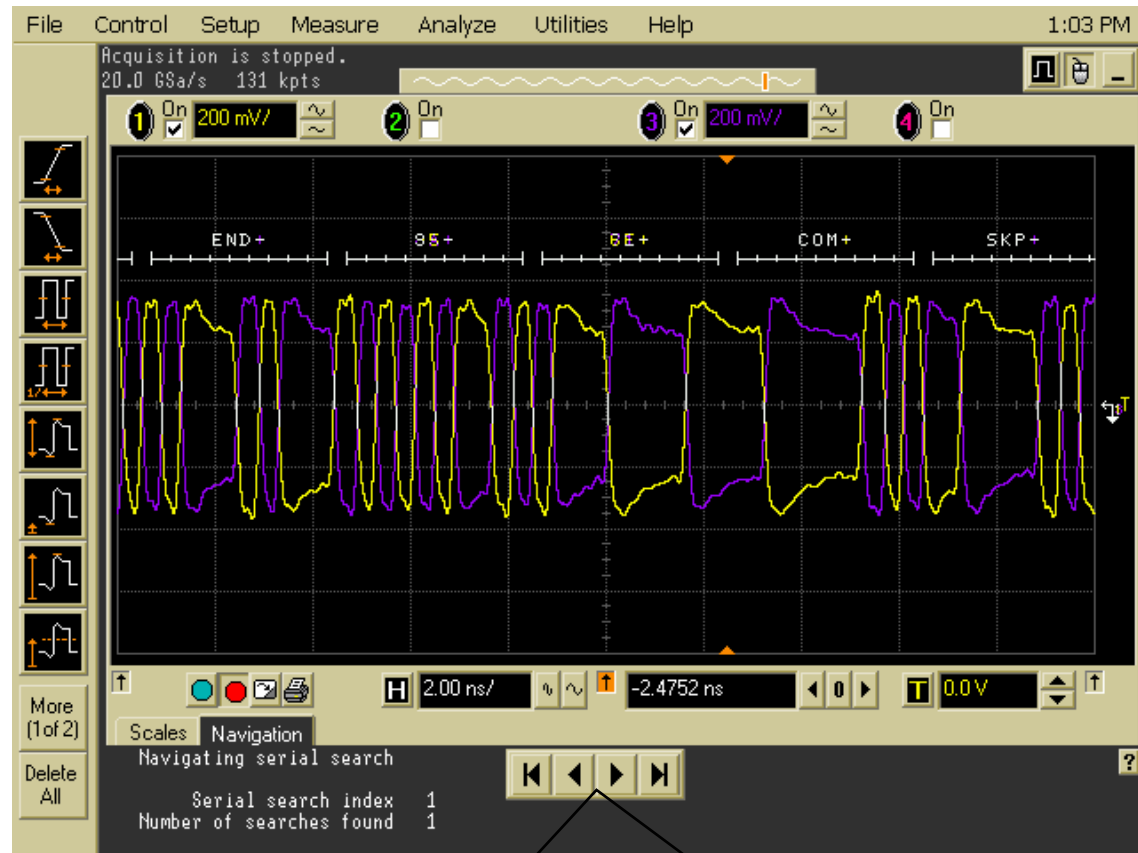
Stop acquisition when pattern is found

Specify up to 4 symbols in sequence

The image shows a 'Serial Setup' dialog box with the following settings:

- Decode Standard: PCI Express
- Display Format: Label (selected), Hexadecimal, 10 Bit, Decimal
- Enable Searching:
- Search Source: Channel 1
- Trigger On Search:
- Stop On Trigger:
- Immediately Followed By...: Find 95, Then 6E, Then CDM, Then SKP
- Symbol 2 Data: A 16x16 grid for specifying symbol sequences. The cell at row 6, column D contains a checkmark.
- Symbol 2 Control: SKP, FTS, SDP, IDL, K28.4, COM, K28.6, K28.7, PAD, STP, END, EDB. All are unchecked.
- Invalid Codes:
- Buttons: Check All, Uncheck All, Close, Help, Don't Care

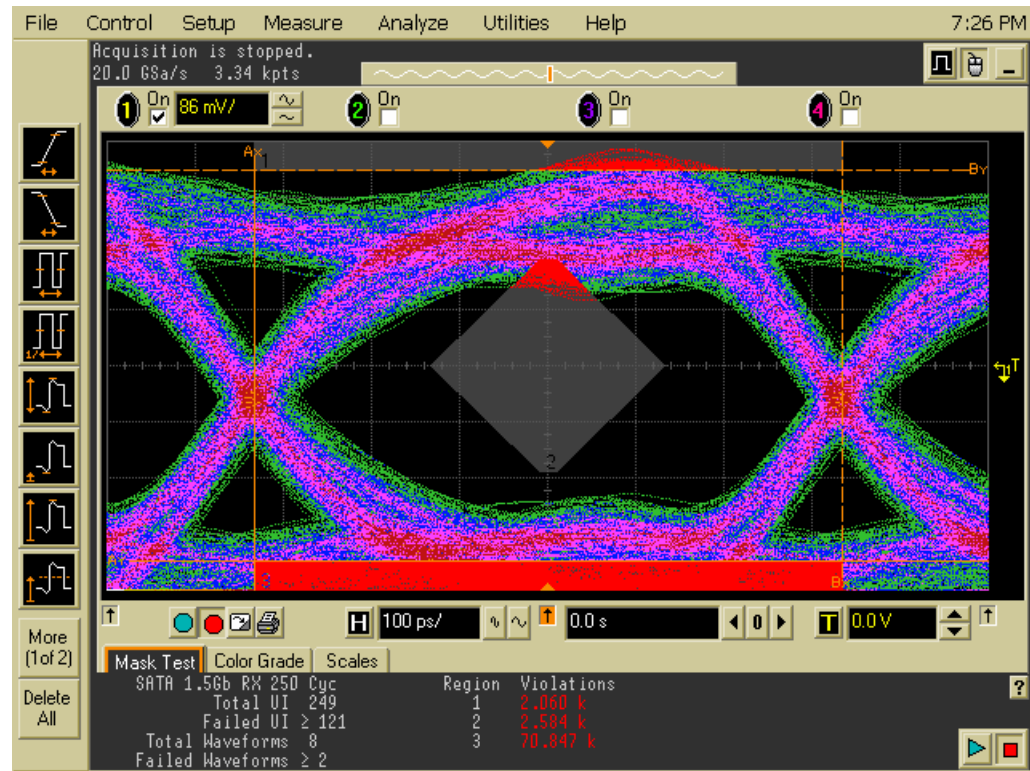
Search Navigation



Navigate to all the instances of the specified sequence of symbols using the arrow keys

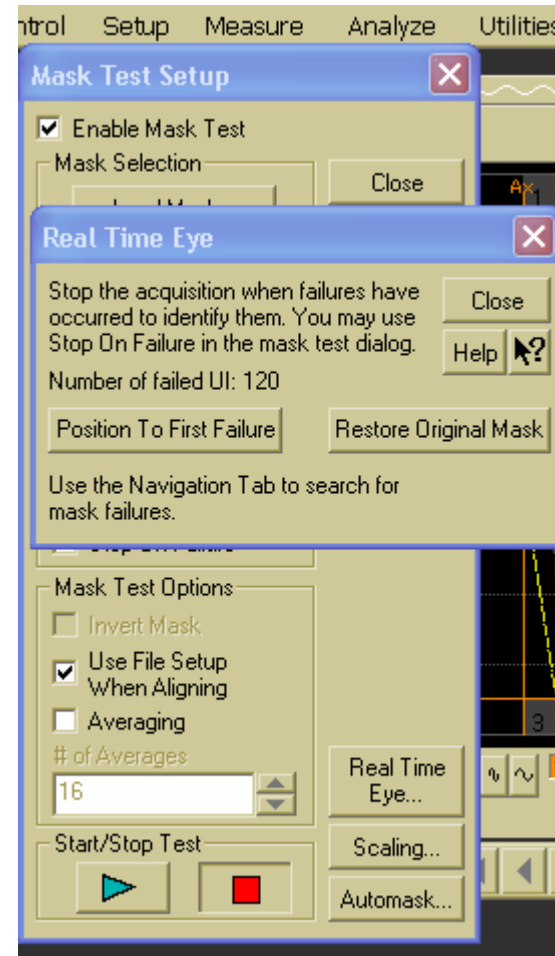
Locating mask violations and failures

The real-time eye combined with the PCI Express mask test indicates there were multiple violations. But how do you gain insight into the individual violations by looking at the composite eye?

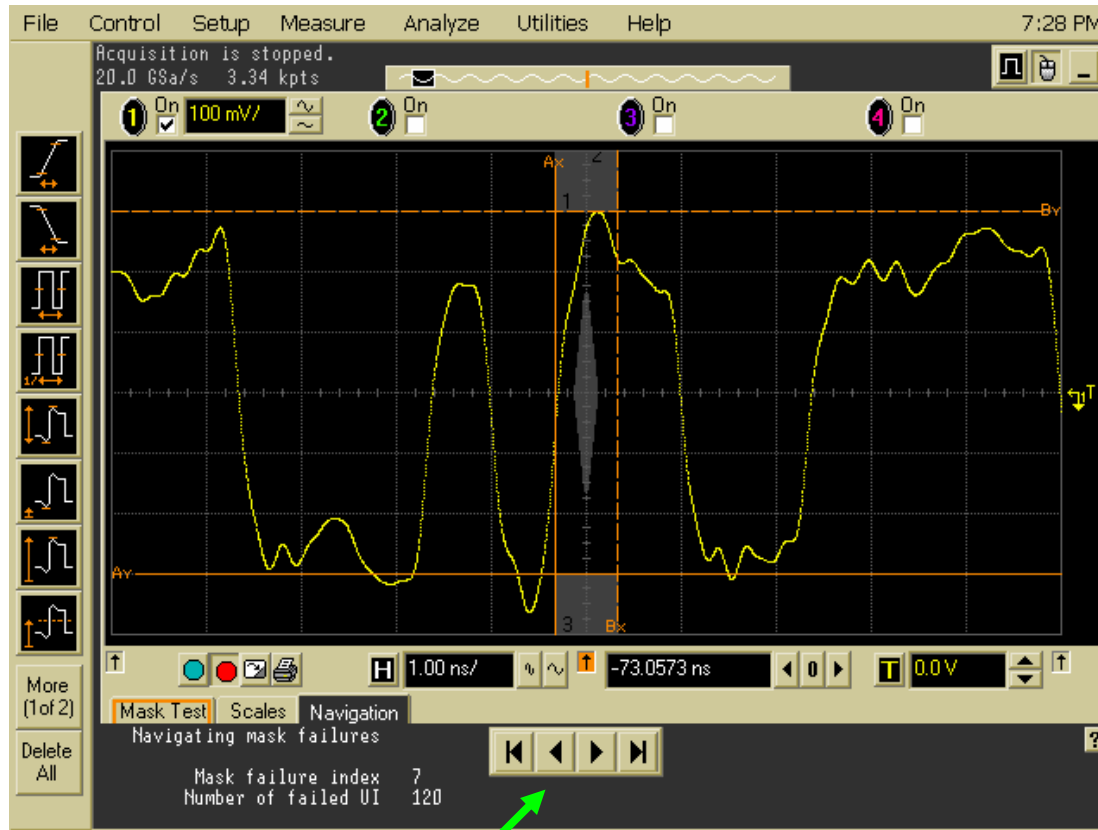


Locating mask violations

Using the controls, we can instruct the scope to go to the first violation in the serial data stream.

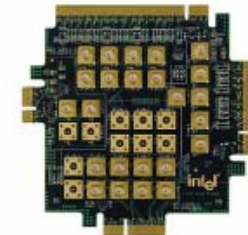
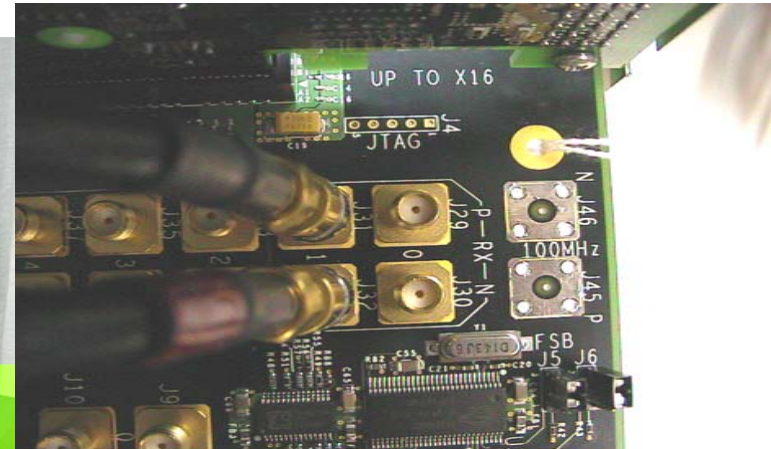


Locating mask violations

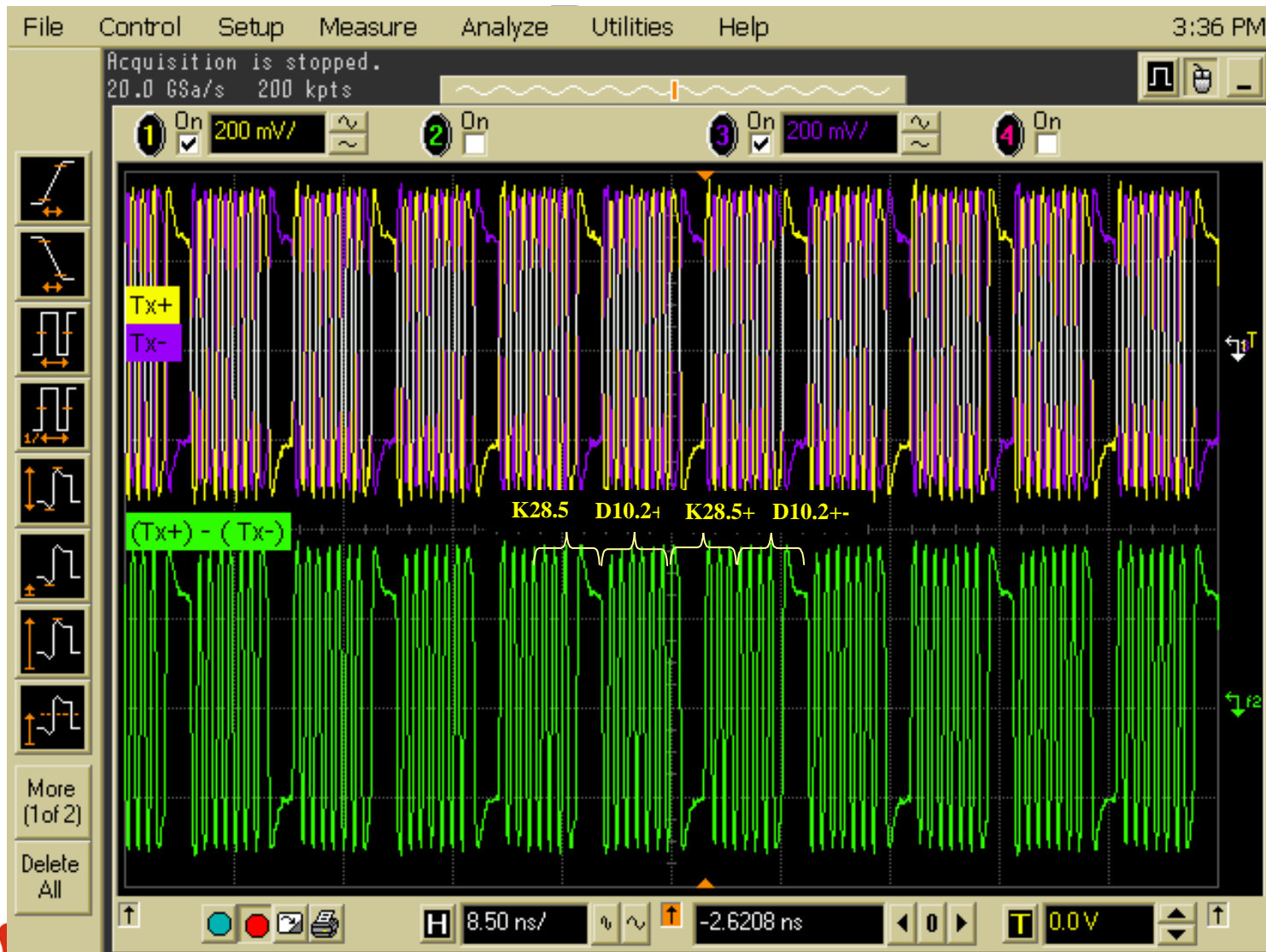


You can use the arrow keys to view each violation individually.

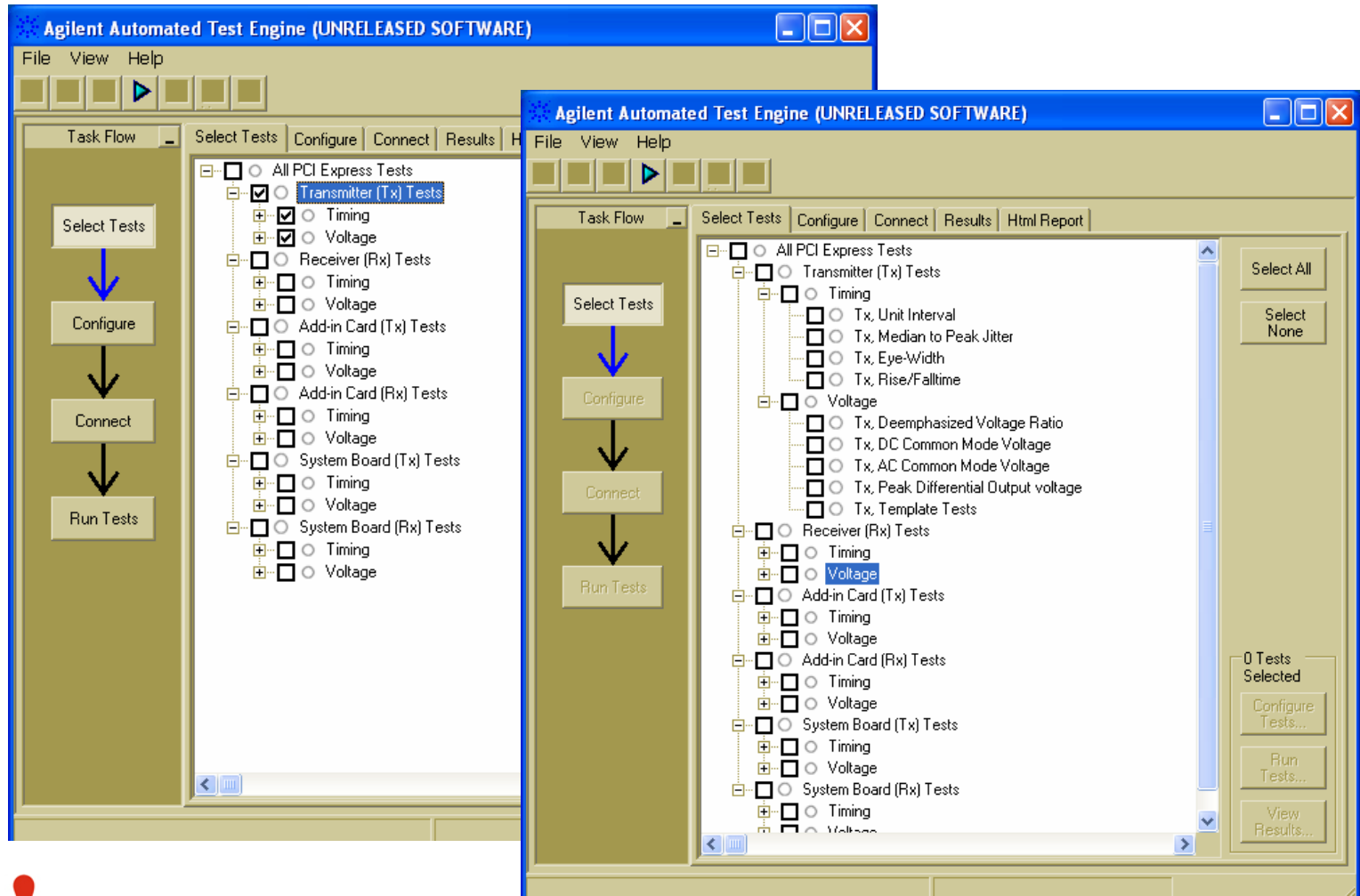
PCI Express Compliance Test Setup (add-in card)



PCI Express TS-1 Compliance Test



PCI Express Compliance and Validation Tool Suite



PCI Express Compliance Report Showing Marginal Performance Analysis



PCI Express Compliance Report

Pass	Test Name	Spec Range
------	-----------	------------

Overall Result: FAIL (3 of 35 Tests Failed)

Test Configuration Details	
Test Date	Jan 27, 2004, 21:04:30
Instrument ID	Agilent Technologies,54855A,No Serial,A.03.18,001,EZJ,SDA
Probe ID	1134A
Serial Number	Jan 27, 2004, 21:04:30
Calibration Status	All Passed

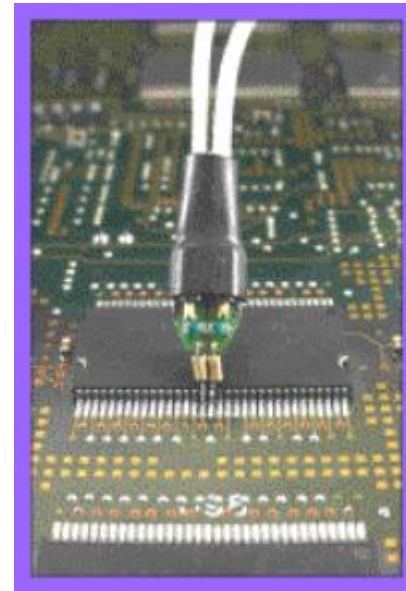
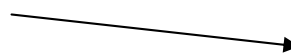
Summary of Results

Margin Thresholds	
Warning	<=3%
Critical	<=0%

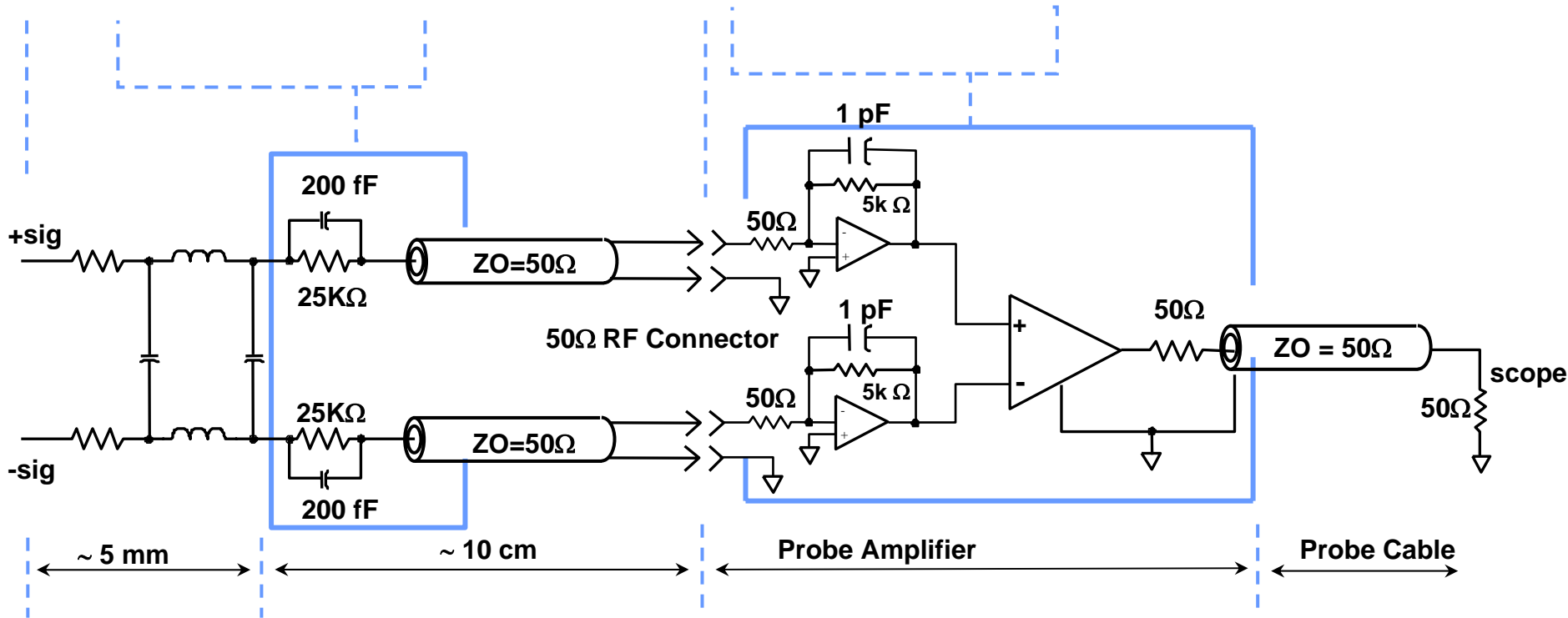
PCI Express Validation Steps

Signal Integrity - Verify the 2.5/5.0 Gb design

- Probing



New Probe Architectures



Making Good Connections (Gen 1)

Flexibility Probe Systems

- Browser probe head
- Solder-in probe head
- Socketed probe head
- SMA probe head
- Differential and single-ended

Probing in confined spaces

10 cm solder-in probe head

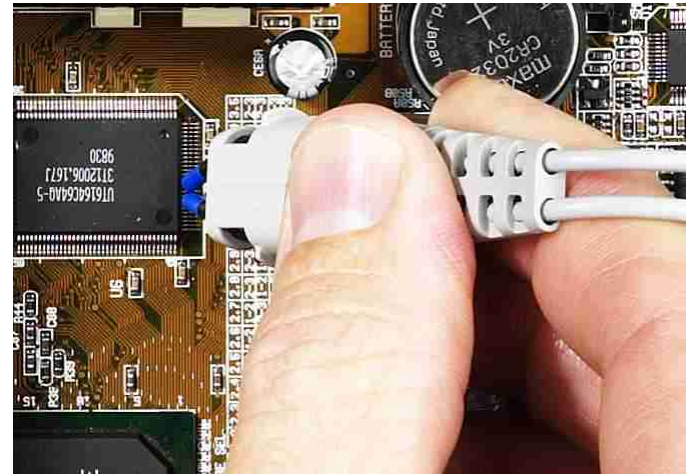
10 cm socketed probe head

Differential browsing probe head

Browser Probe

Characteristics:

- 6 GHz BW
- Most versatile for hand-held probing
- Z-Axis compression enhances connection
- Adjustable tip spans
- Ergonomic sleeve
- Replaceable damping resistor tips
- Can be used with probe stand holder



Solder-in Probe (Gen 1)

Characteristics:

- 8 GHz BW
- Use for high bandwidth connection
- Least space requirement
- Replaceable damping resistors (8 mil)

Socketed Probe

Characteristics:

- 7 GHz BW
- Semi-permanent attachment
- Move between multiple test points
- Adapter for standard headers
- Standard axial lead resistors (20 mil)
- Same resistors support Logic Analyzer
Flying Lead Set

Differential SMA Probe



Characteristics:

- 50-Ohm Input Impedance
- 7 GHz BW
- Span-adjustable semi-rigid coax
- High common-mode rejection
- Cable loss compensation
- Cost effective adapter for existing probe amp
- Can apply DC offset bias

12 GHz Active Probes (Gen 2)

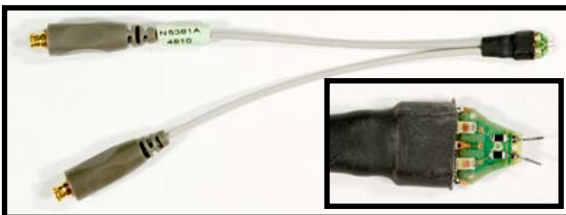
Probe Amplifiers	
Specified Bandwidth	12 GHz
Characterized Probe Tips	Yes
Noise Referred to Input	2.5 mV rms
Attenuation	3.45:1
Diff Dynamic Range	3.3 V p-p
DC Offset Range	+/- 16 V
Maximum Voltage	+/- 30 V



Offers excellent bandwidth, characterized performance for various probe tips, low noise, low attenuation, good dynamic range and small size



12 GHz Differential SMA Adapter Probe Head



12 GHz Differential Solder-in Probe Head: 210 fF input capacitance, 50 kOhm input resistance, 4" reach, 2 mm probe head size at taper, 0.2-3.3 mm lead span



12 GHz Differential Browser: 210 fF input C, 50 kOhm input R, 0.2-3.3 mm lead span

- Logic Layer PCI-E probing
- DLLP and TLP debug

Tools for PCI-Express Logic Layer debug

Packet
Analysis Probe



Logic Analyzer



Config./OS

Software

Transaction

Data Link

Physical

Mechanical

PCI Express Packet Analysis Probe



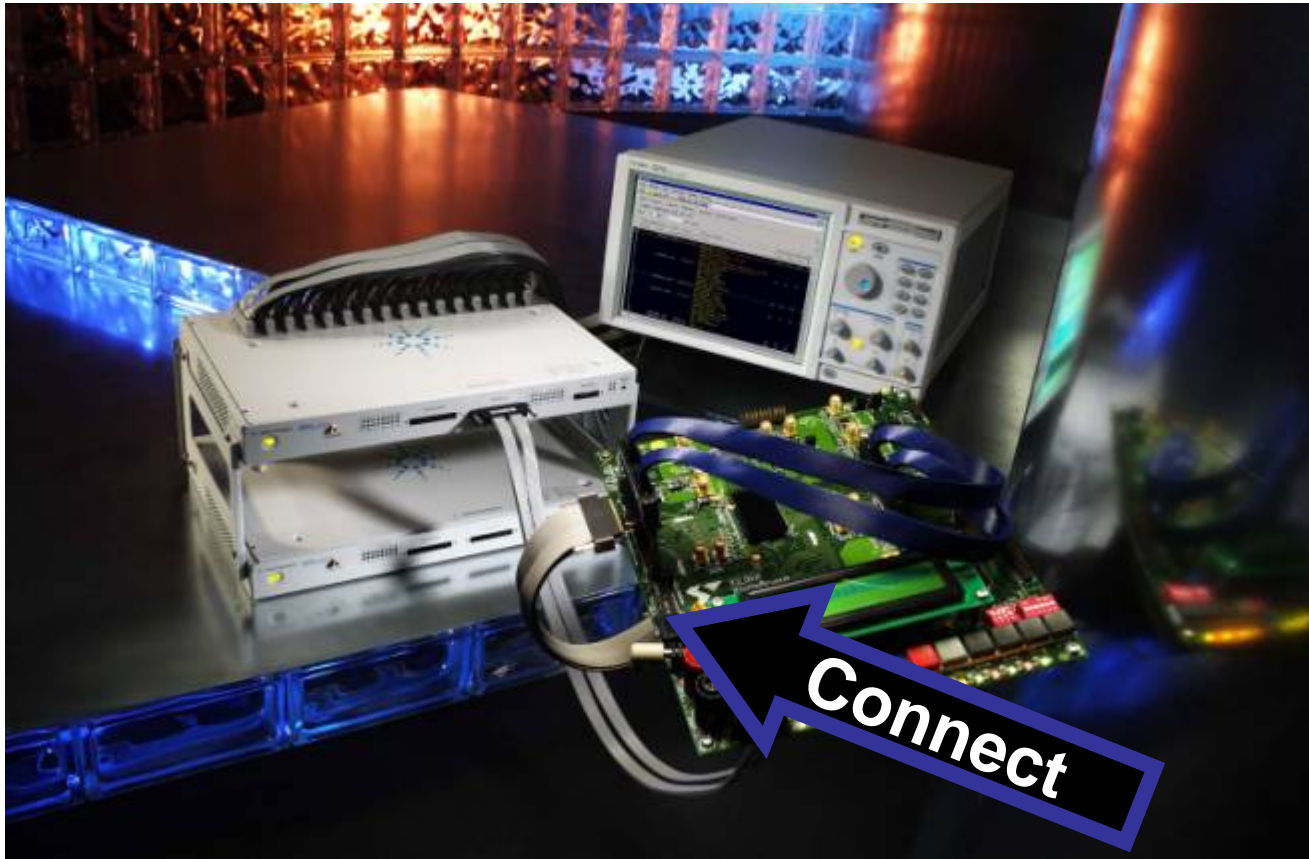
Digital Validation for PCI Express

- Logic Analysis Value Proposition



- Probing
 - Non Intrusive passive observation of data flow
 - Validation of Add-in Cards Chip-to-Chip Architectures
- Packet Analysis and Display
 - Dedicated Packet Triggering in LA
 - Dedicated FPGA Hardware Pattern Recognizers in Probe
 - Software Decode Tool runs on LA
- Full System Validation
 - Cross-Bus Analysis (Time Correlated)
 - Cross-triggering correlation between scope and analyzer

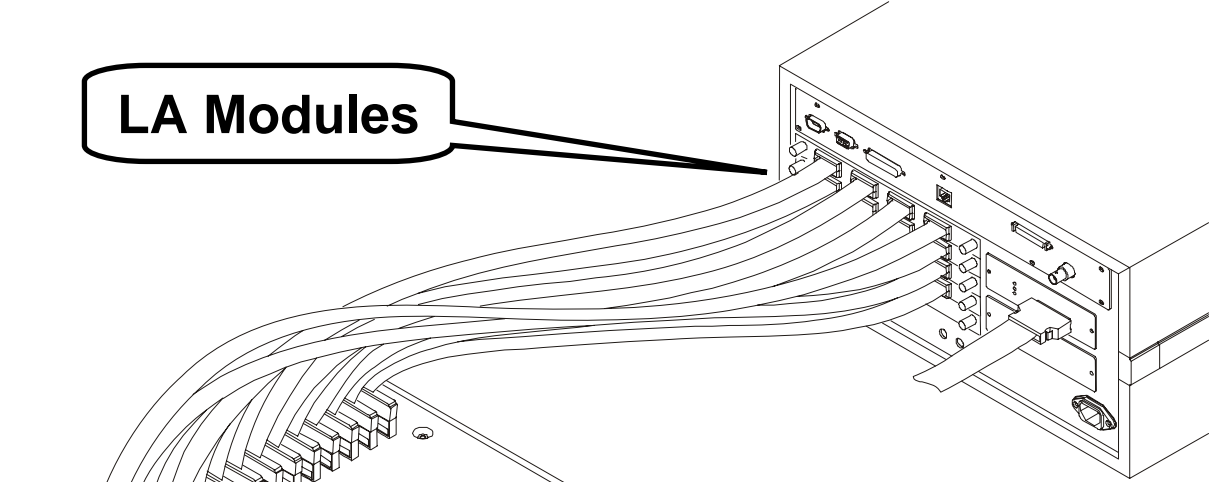
Logic Analysis PCI Express Connection



PCI Express Packet Analysis Probe Slot Interposer Solution

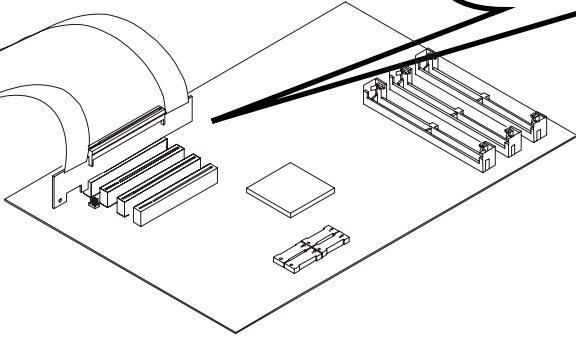


LA Modules



n4220e02

Slot Interposer



Packet Analysis Probe
19" x 12" x 1.5" Form Factor (1U thick)

PCI Express Packet Analysis Probe Midbus Footprint Solution

LA Modules

n4220e03
**Soft Touch
Technology**
PCI Express Footprint

Packet Analysis Probe
19" x 12" x 1.5" Form
Factor (1U thick)

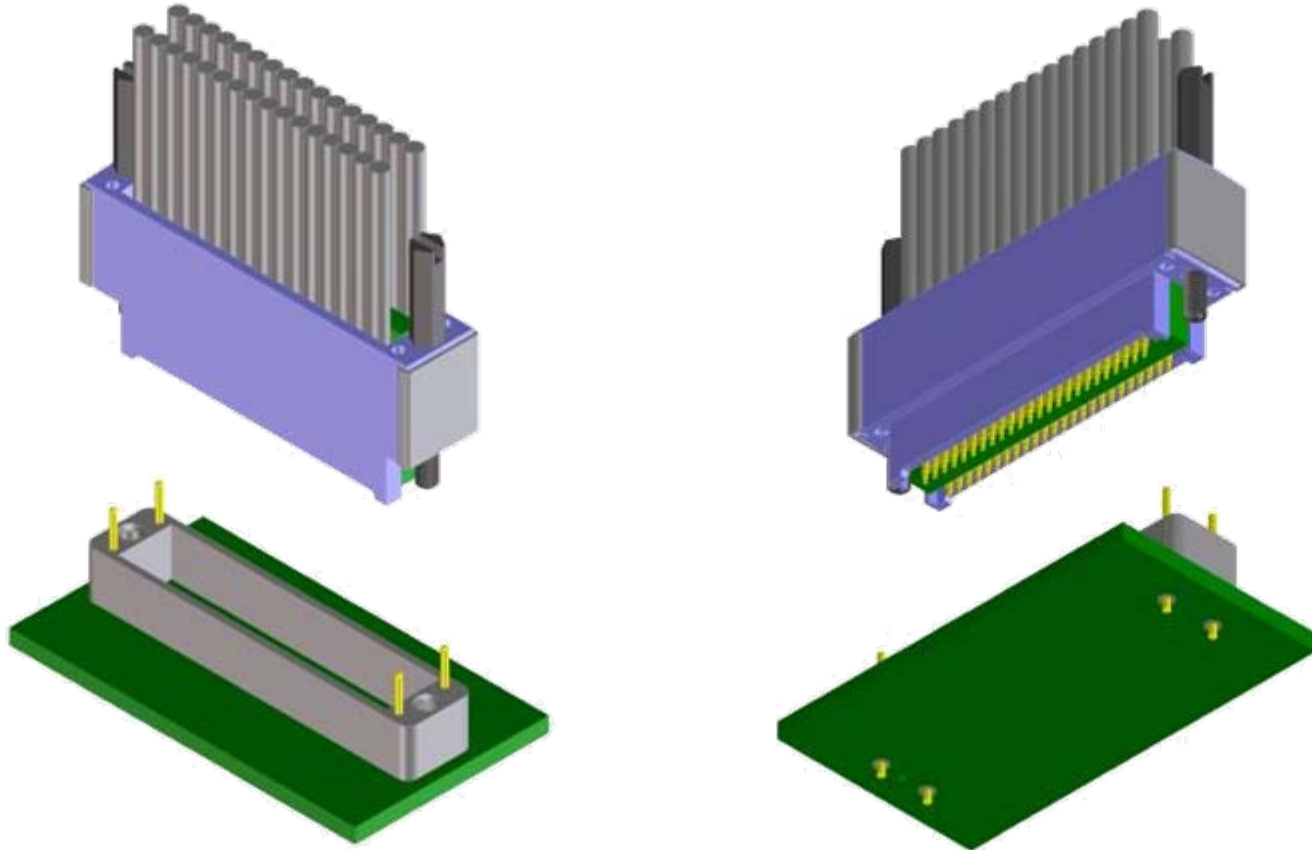
Connect: Low Intrusion is a must



- Types of connection
 - Chip-to-Chip Link – PCI Express FOOTPRINT (Soft Touch TECHNOLOGY)
 - Card Edge
 - Slot connector/interposer



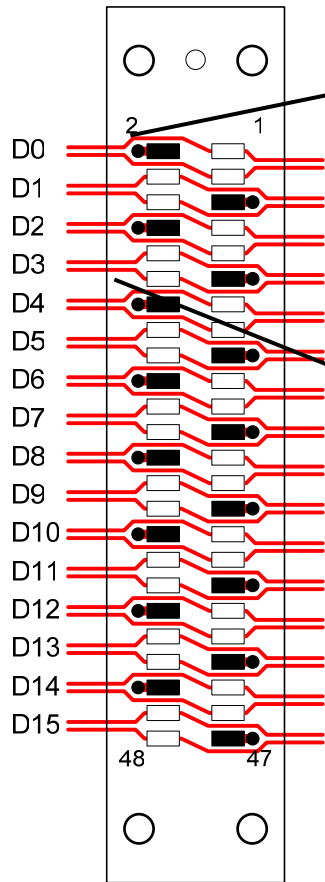
Midbus Probe



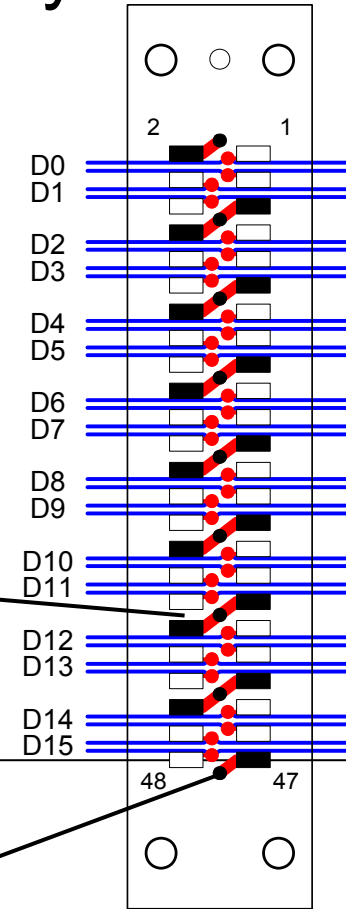
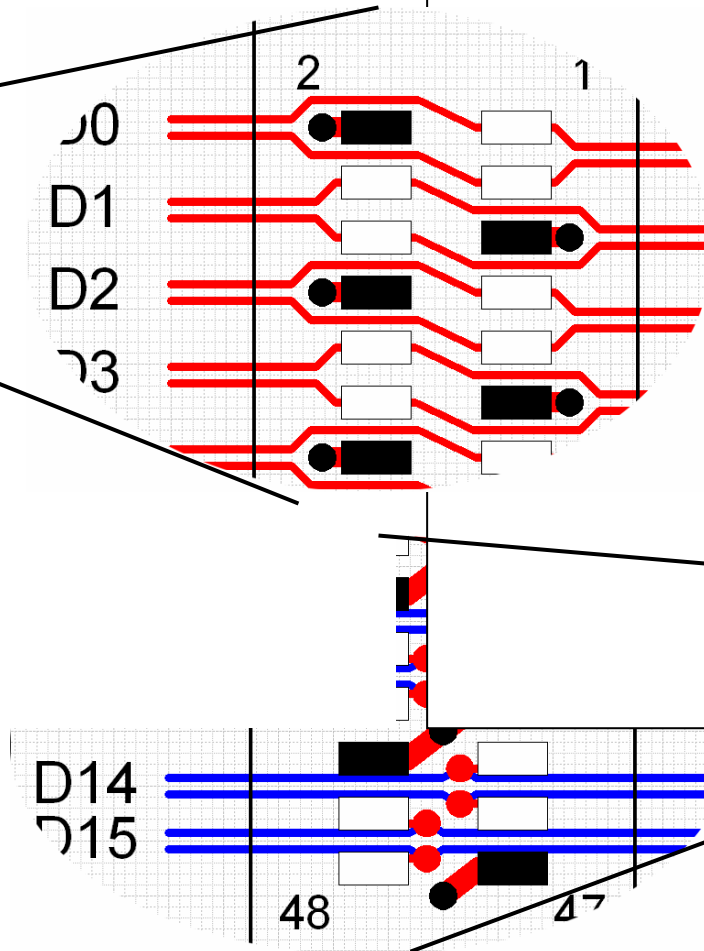
Mid-Bus Footprint Routing



Top Layer Routing



Inner Layer Routing



Mid-Bus Connector Layout



**Additional
x16
Layouts
Supported** →

one direction of x16:	other direction of x16:	both directions of x8:
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
15	15	15

**Additional
Layouts
Supported** →

both direction of 2 x4:	both direction of 2 x2:	both direction of 2 x1:
0	0	0
1	1	nc
2	nc	nc
3	nc	nc
0	0	0
1	1	nc
2	nc	nc
3	nc	nc

- Signal Pair Polarity can be reversed
- Entire Link Lane assignment can be reversed

Connect: Flying Lead Set



Logic Analysis PCI Express Validation Steps



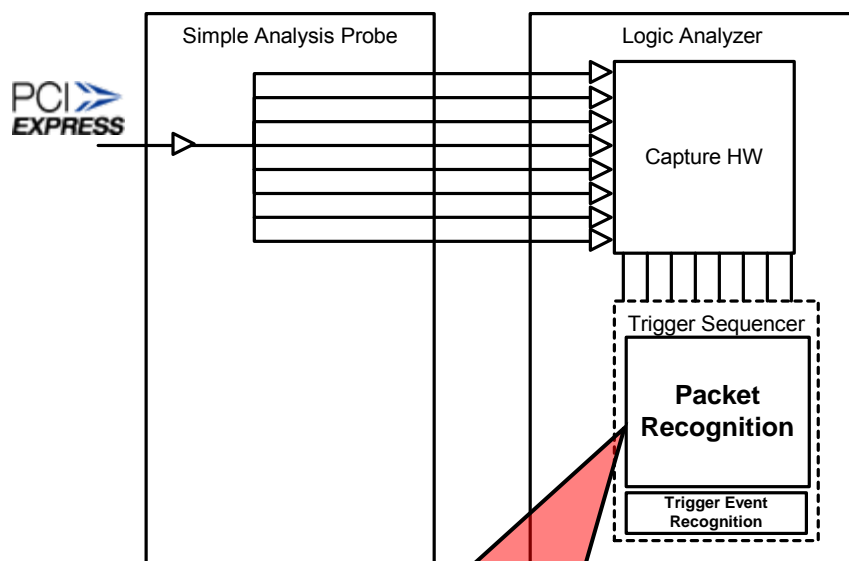
Acquire



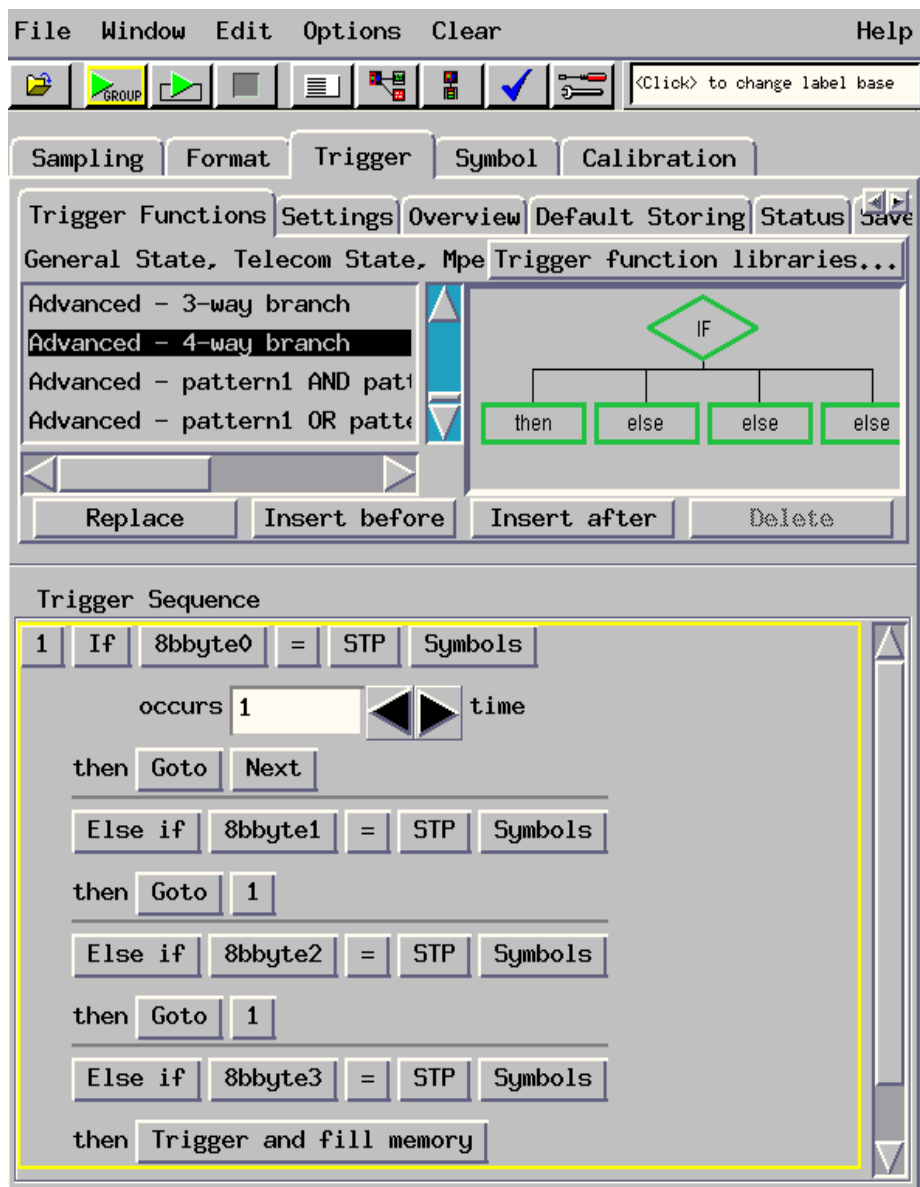
Acquire: PCI Express Traditional LA



- Traditional Serial Analysis Probes

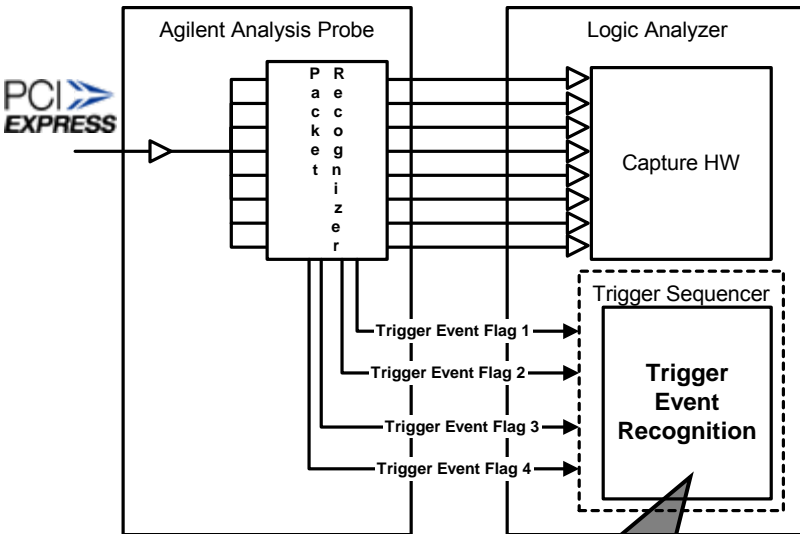


**Packet Recognition
Consumes MOST of the
Trigger Sequencer Resources**

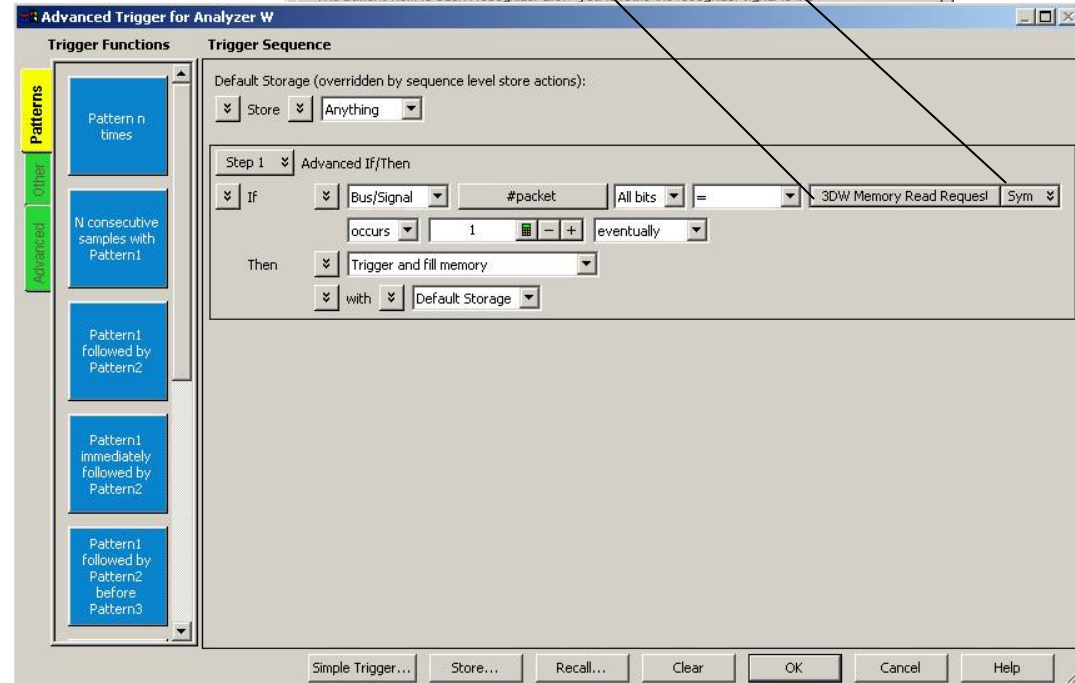
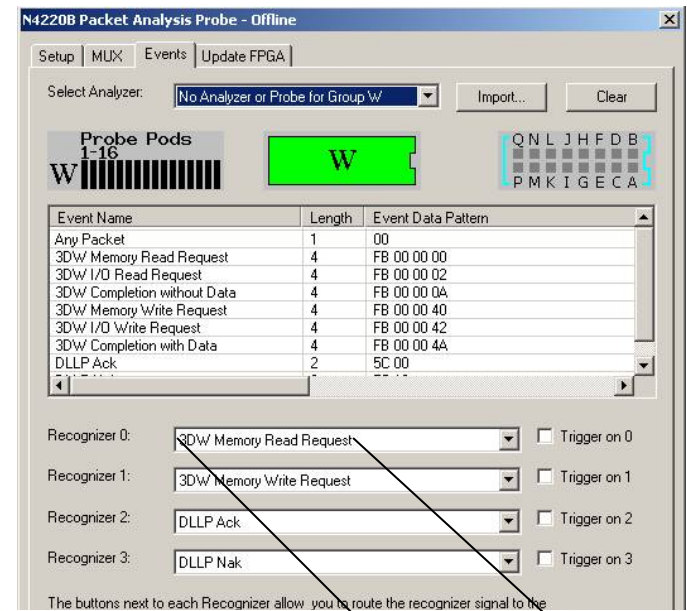


Acquire: PCI Express Packet Recognition

- PCI Express Packet Analysis Probe



Full Trigger Resources Available for Complex Triggering



PCI Express Packet Recognition



- *Enhanced Trigger Capability Through Packet Recognition*
 - 8 Header Recognizers will exist in the Analysis Probe (4 Tx/4 Rx)
 - Implemented in h/w, includes GUI
 - 24 Bytes in each Header Recognizer (Recognition into Data Portion)
 - Recognizers send simple event notification back to Logic Analyzer
 - Full, Robust Logic Analyzer Sequencing will be available on event notification bits.

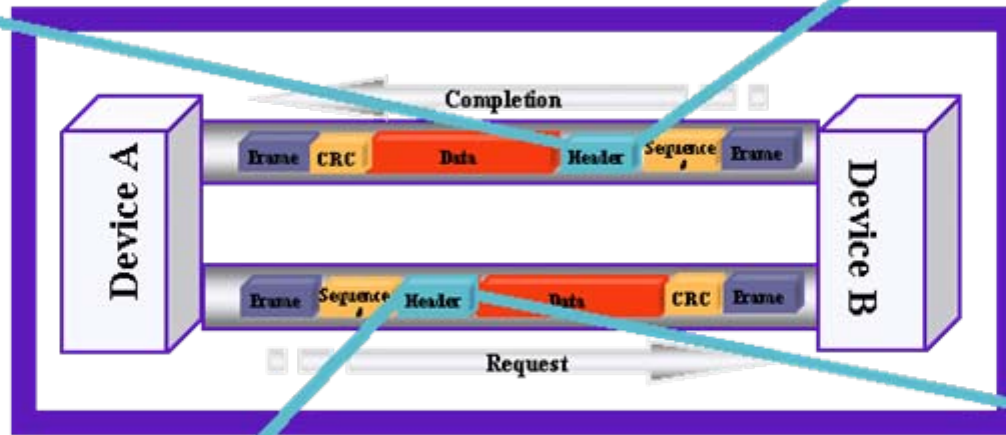
Recognizer 0:	<input type="text" value="3D/W Memory Read Request"/>	<input type="checkbox"/> Trigger on 0
Recognizer 1:	<input type="text" value="3D/W Memory Write Request"/>	<input type="checkbox"/> Trigger on 1
Recognizer 2:	<input type="text" value="DLLP Ack"/>	<input type="checkbox"/> Trigger on 2
Recognizer 3:	<input type="text" value="DLLP Nak"/>	<input type="checkbox"/> Trigger on 3

Logic layer Validation Challenges

“Read” & “Write” Cycles replaced by Packets

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0 >	R	Fmt x 0			Type				R	TC	Reserved				T	E	P	Attr	R	Length												
Byte 4 >	Completer ID								Compl. Status				Byte Count																			
Byte 8 >	Requester ID								Tag								R	Lower Address														

Completion Header Format

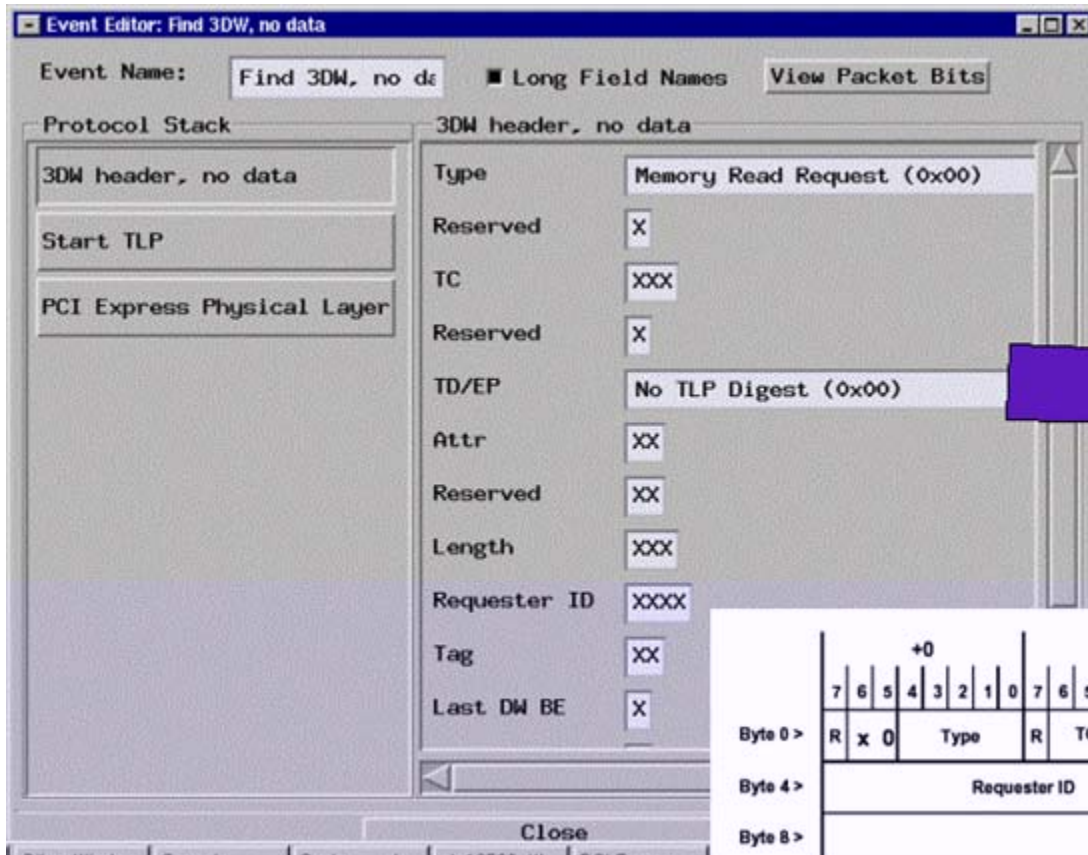


	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0 >	R	Fmt x 1			Type				R	TC	Reserved				T	E	P	Attr	R	Length												
Byte 4 >	Requester ID								Tag								Last DW BE				1st DW BE											
Byte 8 >	Address[63:32]																															
Byte 12 >	Address[31:2]																R															

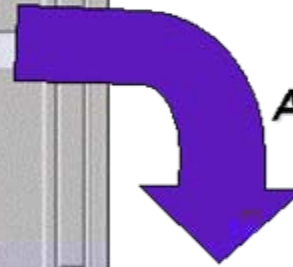
Requester Header Format
For 64-bit addressing of memory

Validation Steps

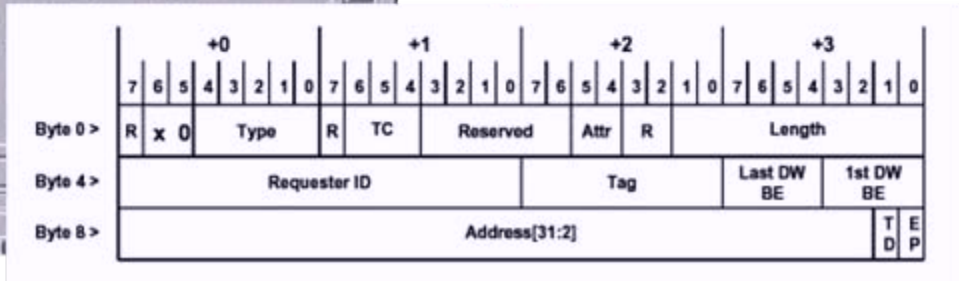
Defining a Packet



*Describe your trigger
At Packet Level*



*Analyzer handles bit
order, 10B/8B,
scrambling, etc.*



Logic Analysis PCI Express Validation Steps

PCI
EXPRESS



Display: Packet Decode



Packet Decode	Bad CRC	Lane Data	Ch
-10	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-9	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-8	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-7	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-6	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-5	00	4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A 4A	D10.2 D10.2 D10.2
-4	00	BC BC BC BC BC BC BC BC BC BC BC BC	K28.5 K28.5 K28.5
-3	00	1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	K28.0 K28.0 K28.0
-2	00	1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	K28.0 K28.0 K28.0
-1	00	1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C 1C	K28.0 K28.0 K28.0
0 Start TLP = STP *****	00	FB 00 00 00 00 00 00 00 00 00 00 00	K27.7 D00.0 D00.0
0.1	Reserved = 0 Hex		
0.2	TLP Sequence Number = 000 Hex		
0.3	Reserved1 = 0 Hex		
0.4	Fmt = 3DV header, no data		
0.5	Type = Memory Read Request		
0.6	Reserved2 = 0 Hex		
0.7	TC = TCO		
0.8	Reserved3 = 0 Hex		
0.9	TD = TLP Digest Not Present		
0.10	EP = TLP Not Poisoned		
0.11	Attributes = Default Ordering, Default		
0.12	Reserved4 = 0 Hex		
0.13	Length = 000 Hex		
0.14	Requester ID = 0000 Hex		
0.15	Tag = 00 Hex		
0.16	Last DW Byte Enable = 0 Hex		
0.17	First DW Byte Enable = 0 Hex		
0.18	Address[31:2] = 0000 0000 Hex		
0.19	Reserved5 = 0 Hex		
0.20	LCRC = c779 bbd1 Hex (GOOD)		
1 End TLP = END -----	00	79 BB D1 FD F7 F7 F7 F7 F7 F7	D25.3 D27.5 D17.5
2 Start TLP = STP *****	00	FB 00 00 01 00 00 00 00 00 00 00	K27.7 D00.0 D00.0
2.1	Reserved = 0 Hex		
2.2	TLP Sequence Number = 000 Hex		
2.3	Reserved1 = 0 Hex		
2.4	Fmt = 3DV header, no data		
2.5	Type = Memory Read Request-Locked		
2.6	Reserved2 = 0 Hex		
2.7	TC = TCO		
2.8	Reserved3 = 0 Hex		
2.9	TD = TLP Digest Not Present		
2.10	EP = TLP Not Poisoned		

Packet Decode / Display (TLP)

K/D	Time	Packet Decode	Data0	Data1	Data2
Binary	Absolute	Text	Hex	Hex	Hex
1000	0 s	Start TLP	FB	00	00
		Reserved = 00 Hex Packet Sequence Number = 00 Hex Reserved = 0 Binary Global Format = 00 Binary (3DW header, no data) Type = 04 Hex (Configuration Read Type 0)			
0000	20,000 ns	Reserved = 0 Binary TC = 000 Binary Reserved = 00 Hex Attr = 00 Binary Reserved = 00 Binary Length = 000 Hex Requester ID = 0000 Hex	00	00	00
0000	40,000 ns	Tag = 00 Hex	00	00	00
		Last DW BE = 0 Hex First DW BE = 0 Hex Bus Number = 00 Hex			
0000	60,000 ns	Device Number = 00 Hex Function Number = 0 Hex Reserved = 0 Hex Ext. Reg Address = 0 Hex Register Address = 00 Hex TLP Digest = 0 Binary EP = 0 Binary 32b CRC: 0x00000000	00	00	00
0001	80,000 ns	End	00	00	00
1000	100,000 ns	Start TLP	FB	00	00

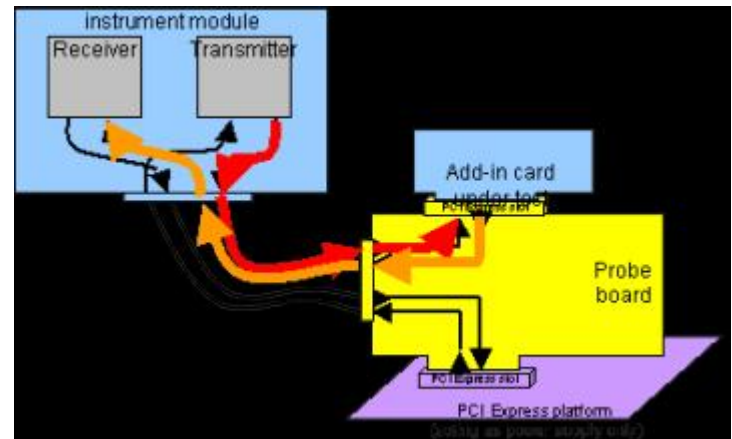
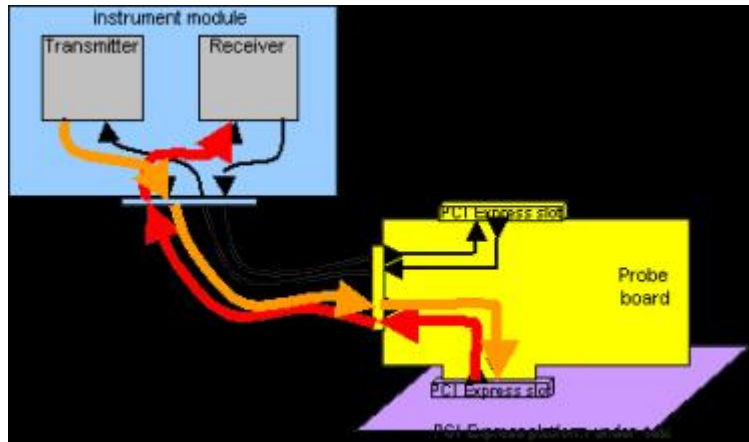
Packet Decode / Display (DLLP)

K/D	Time	Packet Decode	Data0	Data1	Data2
Binary	Absolute	Text	Hex	Hex	Hex
1000	10,340 us	Start DLLP Type = 1 Hex (Nak) Must be zero = 0 Hex Reserved = 00 Hex Reserved = 00 Hex	5C	10	00
0001	10,360 us	End AckNak_Seq_Num = 01 Hex 16b CRC: 0x0000	01	00	00
1000	10,380 us	Start DLLP Type = 2 Hex (PM) PM = 0 Hex (PM_Enter_L1) Reserved = 00 Hex Reserved = 00 Hex	5C	20	00
0001	10,400 us	End Reserved = 00 Hex 16b CRC: 0x0000	00	00	00
1000	10,420 us	Start DLLP Type = 2 Hex (PM) PM = 1 Hex (PM_Enter_L2) Reserved = 00 Hex Reserved = 00 Hex	5C	21	00
0001	10,440 us	End Reserved = 00 Hex 16b CRC: 0x0000	00	00	00
1000	10,460 us	Start DLLP Type = 2 Hex (PM) PM = 2 Hex (PM_Active_State_Request_LOs)	5C	22	00

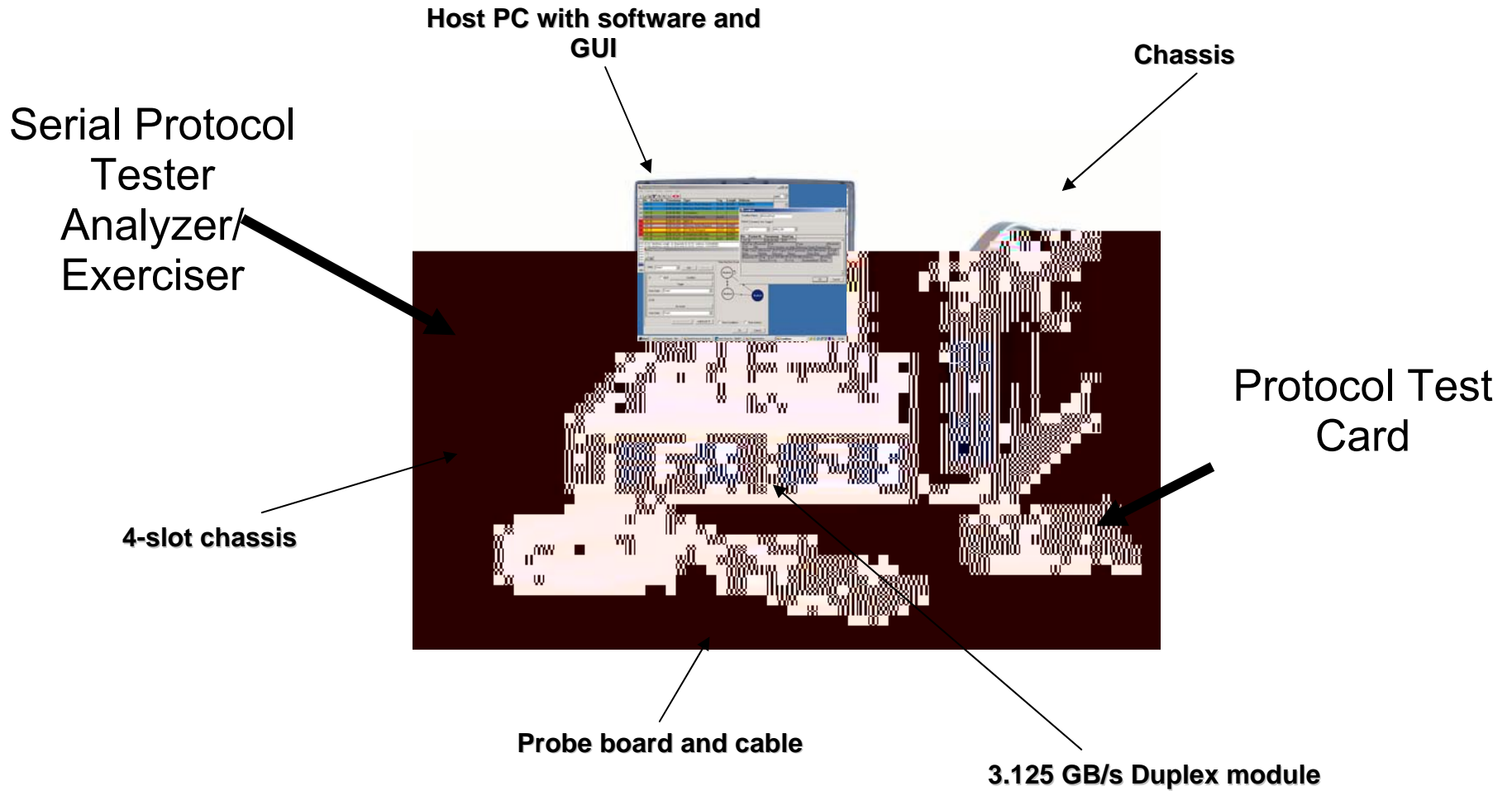
Protocol Verification Challenges

Protocol Variations / Maximum Load

- Maintain system stability over different configurations
 - What happens if the link is fully populated with packets?
 - Does my system still work if an add-in card is inserted that implements the protocol differently?
 - How can I tell if my design is protocol compliant?



Serial Protocol Tester and Protocol Test Card



GUI Protocol Analyzer

Color coded transaction types allow easy recognition of various transactions.

Tabular view with configurable columns.

Packets with errors are highlighted with special colors.

Expand/collapse individual packets to get more details

Tooltips for each field provide more detailed information as needed

Context sensitive field decoding

Transaction view pane provides alternate view of traffic (e.g. textual, statistical, etc.)

Agilent E2960A Protocol Analyzer for PCI Express

Dir.	Packet N	Timestamp	StartTag	Sequence	Type	Length	Tag	Completer	Req	Data
↑	24	4544	SDP		UpdateFC-NP					
↑	25	4740	STP	0x0002	Completion with data	0x0001	0x03	0x0100		0x00000100
↓	26	5740	STP	0x0004	Config Read Type 0	0x0001	0x04	0x0100	13	
		StartTag	Sequence Number	Fmt	Type	Traffic Class	TLP Digest	TLP poisoned	Attr	Length
		STP	0x0004	3DW header, no data	Config Read Type 0	000b	Absent	false	00b	0x0001
		Requester ID	Tag	Last DW BE	First DW BE	Completer ID	Ext. Reg. Number	Register Number	LCRC	EndTag
		0x0030	0x04	0000b	1111b	0x0100	0	13	0x280FD52D	END
↑	27	5780	COM		Skip Ordered Set					
↓	28	5820	SDP	0x0002	Ack					
↑	29	6228	SDP	0x0004	Ack					
↑	30	6300	SDP		0xEB					
↑	31	6340	SDP		UpdateFC-NP					
↑	32	6436	STP	0x0003	Completion with data	0x0001	0x04	0x0100		
		StartTag	Sequence Number	Fmt	Type	Traffic Class	TLP Digest	TLP poisoned	Attr	Length
		STP	0x0003	3DW header, with data	Completion with data	000b	Absent	false	00b	0x0001
		Completer ID	Completion Status	BCM	Byte Count	Requester ID	Tag	Lower Address	Data	LCRC
		0x0100	0C (Successful Completion)	0b	0x0004	0x0030	0x04	0x00	0x40000000	0x39A3755D
		EndTag								
		END								
↓	33	7412	COM		Skip Ordered Set					
↓	34	7460	SDP	0x0003	Ack					

Type: Invalid Value Reserved: Reserved not 0

Transactions

- 44: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x00000100
- 2198: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x06011000
- 4044: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x00000100
- 5740: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x40000000
- 7492: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x0150C2DB
- 9188: CfgRead0, Length: 0x0001, Requester ID: 0x00000030, Length: 0x0001, Completion Status: 000b, Data: 0x05600000

Protocol Analyzer Trigger Setup

The screenshot displays the 'Trigger Setup (Offline)' window, which is used for configuring triggers in a protocol analyzer. The window is divided into two main sections: configuration on the left and a visualization on the right.

Configuration Section:

- State:** A dropdown menu is set to 'Start', with 'Add...' and 'Rem' buttons.
- IF Rule:** A rule is defined with the condition 'IF NOT TRUE' and the action 'StoreUpstream,StoreDownstream'. Below this, there are two more rules using 'Counter1' and 'Counter2' with various logical operators (AND, OR, NOT).
- ELSE IF Rule:** A rule is defined with the condition 'ELSE IF NOT TRUE' and the action 'StoreUpstream,StoreDownstream'. Below this, there is another rule with the condition 'IF TRUE AND Counter1' and the action 'StoreUpstream,StoreDownstream'.
- Goto State:** A dropdown menu is set to 'State2' for the first rule and 'Start' for the second rule.

Trigger Visualization Section:

- The diagram shows three states: 'Start', 'State2', and 'State3'.
- Start State:** A self-loop arrow labeled 'ELSE IF TRUE StoreUpstream,StoreDownstream'.
- Start to State2:** A transition arrow labeled 'IF NOT TRUE AND Counter1 OR Counter2 AND NOT Counter2 StoreUpstream,StoreDownstream'.
- State2 to State3:** A transition arrow labeled 'IF TRUE AND Counter1 StoreUpstream,StoreDownstream'.
- State3:** A self-loop arrow labeled 'IF TRUE StoreUpstream,S'.

At the bottom of the window, there are checkboxes for 'Show Conditions' and 'Show Actions', both of which are checked. The 'OK', 'Apply', and 'Close' buttons are located at the bottom right.

Exerciser GUI

The screenshot displays the 'Protocol Exerciser for PCI Express - Untitled1 (Offline)' application. The main window is titled 'Request' and is divided into several sections:

- Navigation:** Shows 'Exercisers' and 'Untitled1 (Offline)'.
- Request Overview:** A table showing a single packet configuration.
- General Behaviors:** A list of checkboxes for 'automatic TAG generation', 'TLP digest present', and 'TLP poisoned'.
- Request Details:** A detailed view of the selected packet with fields for Dir, Type, Address, Data, StartTag, Sequence Number, and Fmt*.
- Request Parameters:** A table of parameters including Type*, Traffic Class*, TLP Digest, TLP poisoned*, Attr*, Length, Requester ID*, Tag, Last DW BE*, First DW BE*, Address*, LCRC, and EndTag.
- Request Type Selection:** A list of options: Single Packet Memory (selected), Data Generator, Internal Memory, and Compose With Internal Memory.
- Virtual Channel:** A section with a 'Request' button and a 'Completion' button.
- Status Bar:** Shows 'default setup created', 'Session: offline', and 'Exerciser: offline'.

Dir.	Type	Address	Data
↑	Memo	0x000000	write

StartTag	Sequence Number	Fmt*
auto generated	3DW header, no data	

Type*	Traffic Class*	TLP Digest	TLP poisoned*
Memory Read	000b	Absent	false

Attr*	Length	Requester ID*	Tag
00b	1 DW	0x0000	auto generated

Last DW BE*	First DW BE*	Address*	LCRC	EndTag
0000b	0000b	0x00000000	correct	END

Request Type Selection:

- Single Packet Memory
- Data Generator
- Internal Memory
- Compose With Internal Memory

Virtual Channel:

Request

Completion

Status Bar: default setup created | Session: offline | Exerciser: offline

Protocol Test Card for PCI Express Compliance Testing

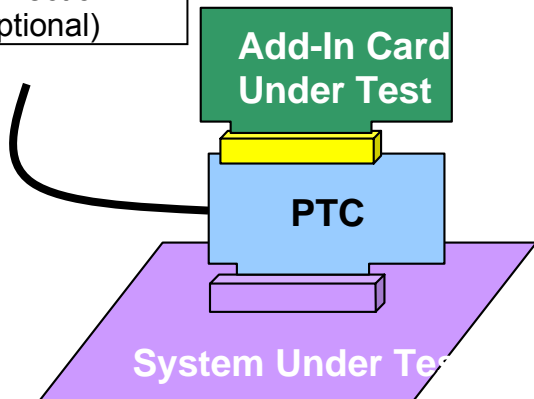
Log	01:00:00:00:00:00	Received TLP with invalid CRC
Log	01:00:00:00:00:00	CRC discard the TLP, free any storage associated with it, schedule a NAK DLP for transmission if one is not already scheduled and report an error associated with the TLP.
Log	01:00:00:00:00:00	
Log	01:00:00:00:00:00	Received TLP with invalid CRC
Log	01:00:00:00:00:00	Discard TLP, free any storage associated with it, schedule a NAK DLP for transmission if one is not already scheduled and report an error associated with the TLP.
Log	01:00:00:00:00:00	
Log	01:00:00:00:00:00	Received TLP with invalid CRC
Log	01:00:00:00:00:00	Discard TLP, free any storage associated with it, schedule a NAK DLP for transmission if one is not already scheduled and report an error associated with the TLP.
Log	01:00:00:00:00:00	
Log	01:00:00:00:00:00	Received TLP with invalid CRC
Log	01:00:00:00:00:00	Discard TLP, free any storage associated with it, schedule a NAK DLP for transmission if one is not already scheduled and report an error associated with the TLP.
Log	01:00:00:00:00:00	



Collaboration and joint development with Intel

- **Cost-effective compliance solution**
- **Easy-to-use**
 - **GUI/push-button solution**
 - **Pre-programmed tests**
 - No programming effort**
 - **Pass/Failed report**
- **Improves design quality, compliance and accelerates time to market**

Serial Protocol Tester – Analyzer connection (optional)



PTC GUI – main view

Agilent E2969A Protocol Test Card for PCI Express - Compliance Test Suite

File View Tests Help

Execute Status Name Description

Execute	Status	Name	Description
<input checked="" type="checkbox"/>	PASSED	DLL.5.3#2	Discard TLP on bad LCRC, send NAK
<input type="checkbox"/>	n/a	DLL.5.2#15	If a normal TLP (one with END framing symbol) is received and its LCRC doesn't match calculated CRC, discard the TLP, free any storage associated with it, schedule a NAK DLLP for transmission if one is not already scheduled and report an error associated with the Port.
<input type="checkbox"/>	n/a	DLL.5.3#3.1	
<input type="checkbox"/>	n/a	DLL.5.2#2	
<input type="checkbox"/>	n/a	DLL.5.3#3.2	
<input type="checkbox"/>	n/a	DLL.5.2#1	Retransmit TLP on NAK
<input type="checkbox"/>	n/a	DLL.5.2#1.2	Retransmit TLP until REPLAY_NUM overflow
<input type="checkbox"/>	n/a	DLL.5.2#10	Ensure correct TLP order in replay
<input type="checkbox"/>	n/a	DLL.5.2#1.2	Start REPLAY upon REPLAY_TIMER expiring
<input type="checkbox"/>	n/a	DLL.4.1#2	All reserved fields must be 0
<input type="checkbox"/>	n/a	DLL.5.2#16	DLLP with undefined encoding shall be dropped
<input type="checkbox"/>	n/a	DLL.5.2#17	Report error on wrong sequence via ACK

Fully Buffered DIMM Overview

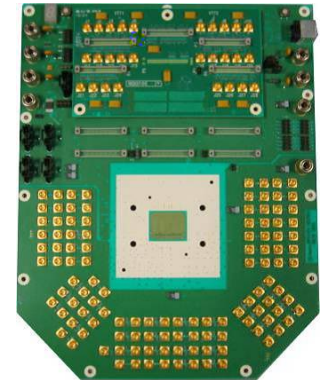
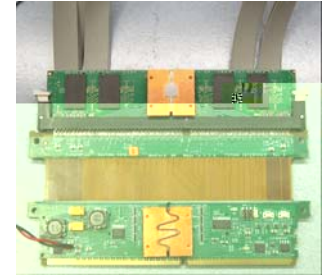
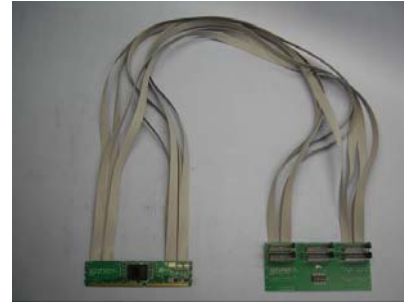
PHY and Logic Probing Overview

Rohit Bhasin

Senior Technical Sales Engineer

Digital Verification and Design Validation Solutions

Agilent Technologies

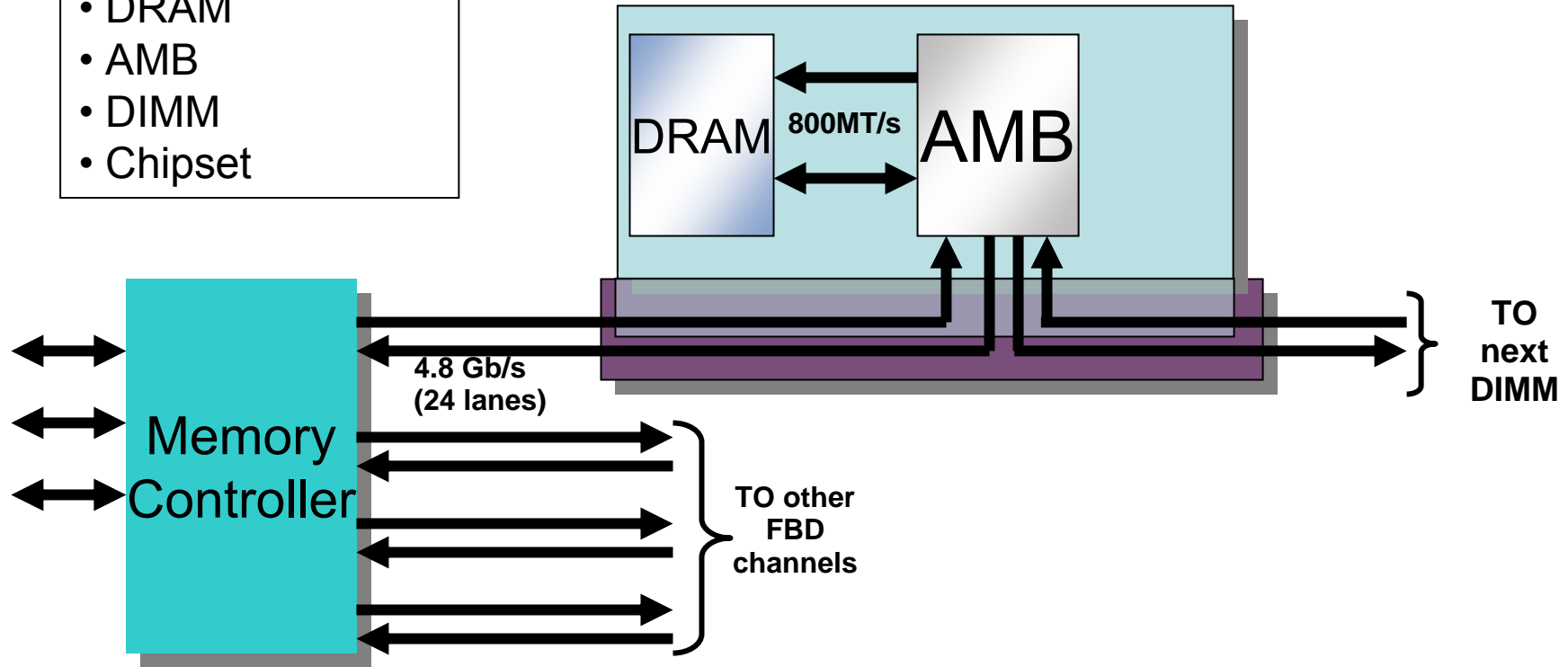


What is Fully Buffered DIMM?

FSB, PCI-X, PCI-E, SATA, etc.

People doing FBD:

- DRAM
- AMB
- DIMM
- Chipset



DRAM IO [Mb/s]	533	667	800	1.066	1.333	1.600
AMB IO [Gb/s]	3.2	4.0	4.8	6.4	8.0	9.6

Routing Comparison

Direct DDR2 Registered DIMMs:

1 Channel, 2 Routing Layers with 3rd layer required for power

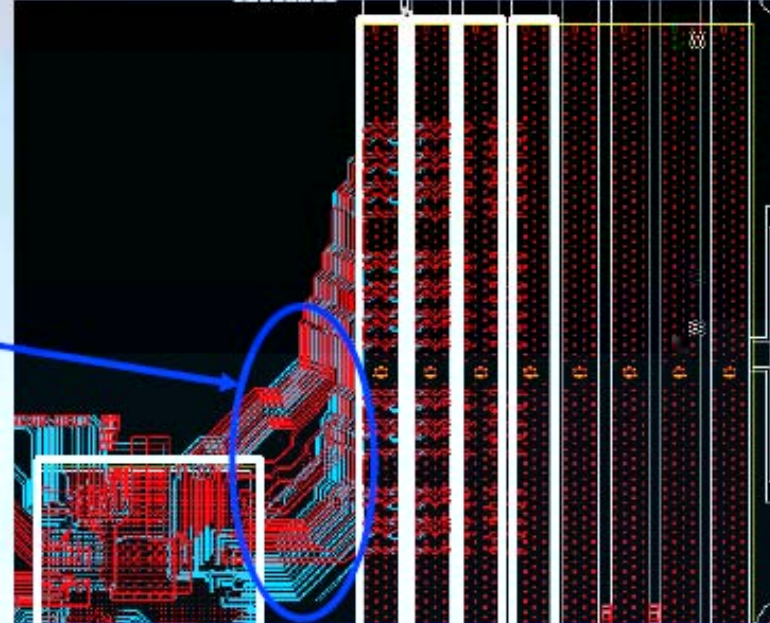


Serpentine routing is complicated and uses up a lot of board area

Fewer signals and no trace length matching minimizes board area

FB-DIMMs:

2 Channels, 2 Routing Layers (includes power delivery)

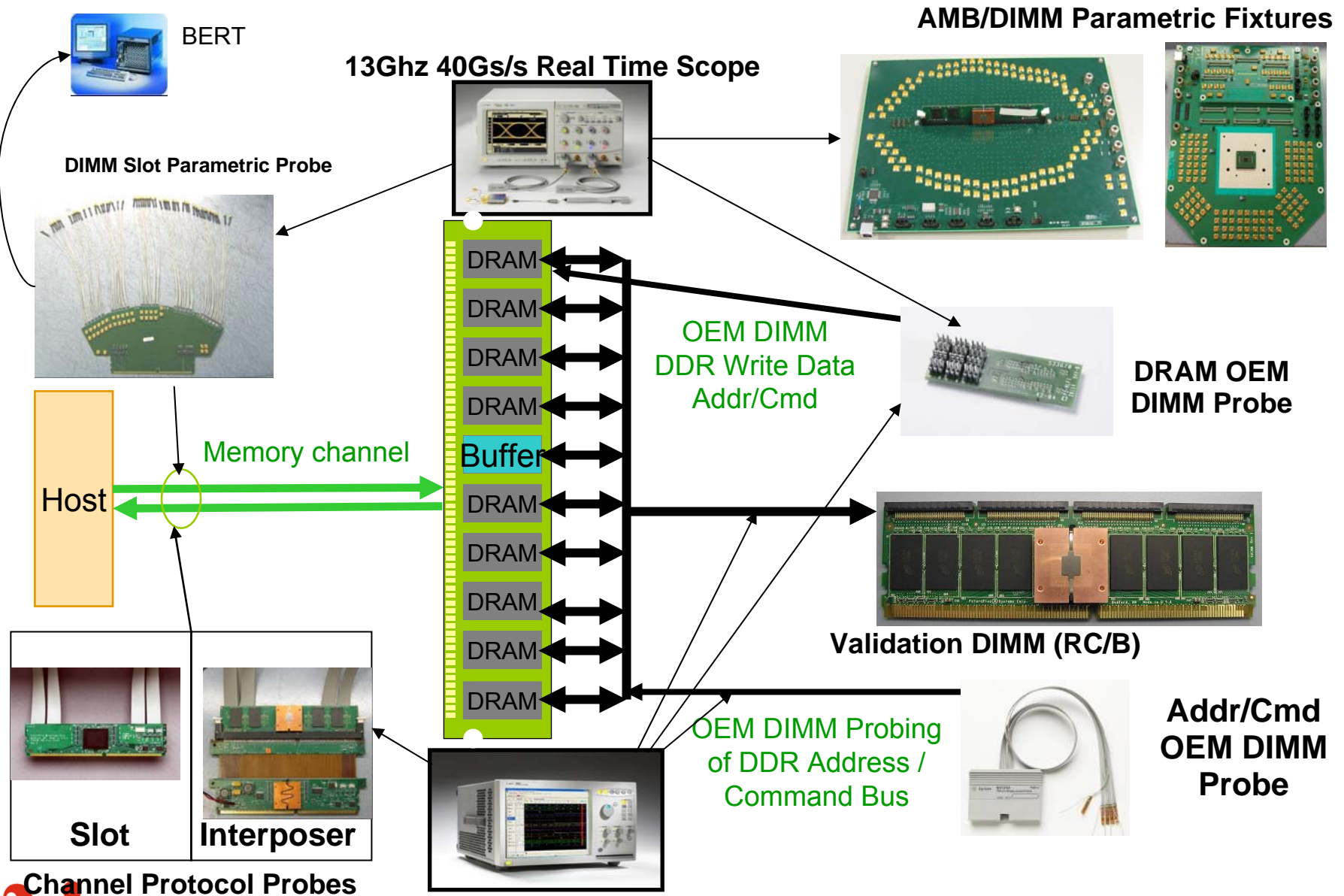


FB-DIMM: Fewer Layers, Less Routing Area

Developed by

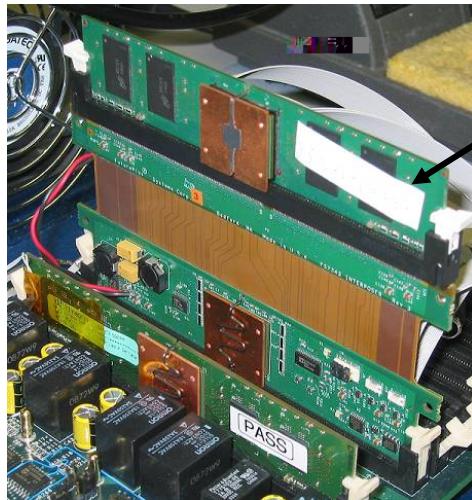
Form

FBD Measurement Points and Validation Components



High Speed Channel Probes

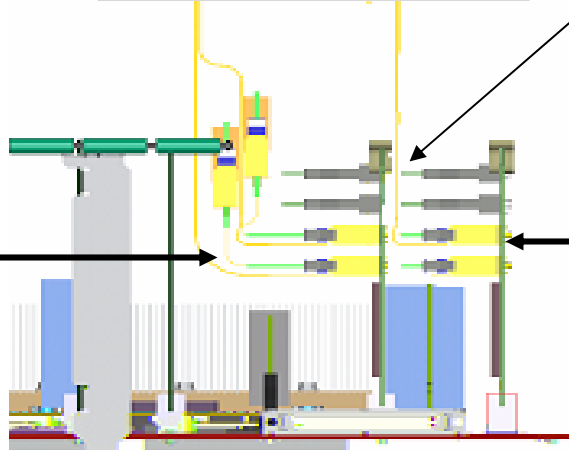
Interposer Probe allows all DIMM slots to be populated



FB-DIMM



Slot Probe fits anywhere a Jedec DIMM will fit and works in systems with suspect timing



Interposer Channel Probe

- Does not consume a slot
- Adjustable orientation of interposed DIMM for maximum installation flexibility
- Supports probing of 2 channels in adjacent slots
- Full SB/NB protocol analysis

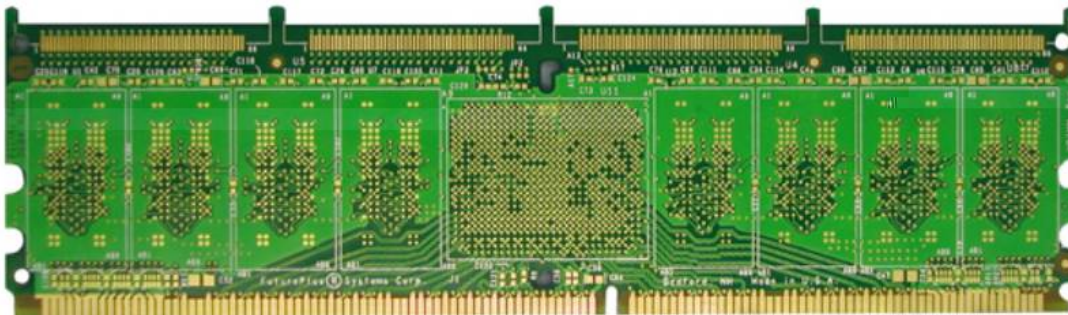
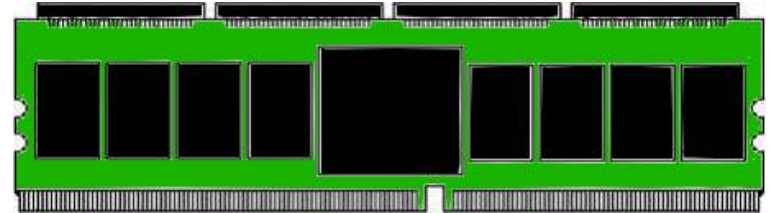
Slot Channel Probe

- Same size as standard FB DIMM to fit in crowded systems
- High Speed channel layout identical to standard DIMM for operation in marginal systems
- Full SB/NB protocol analysis

Complete Pre-AMB Probing

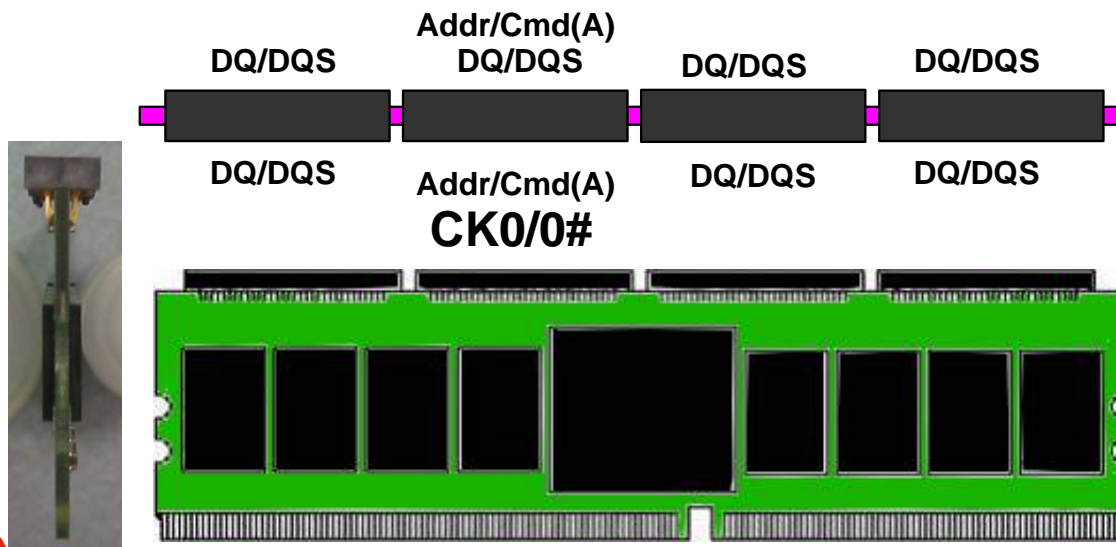
Logic Analyzer Probing for Instrumented DIMMs

- RC/B Validation DIMM
 - Fast connection to all post-register signals (Addr/Cmd/DQ)
 - Support to DDR800+ Speeds
 - Supports all Jedec AMBs and x8 DRAMS
 - RC/A,C,D,G,H,I support planned if demand warrants



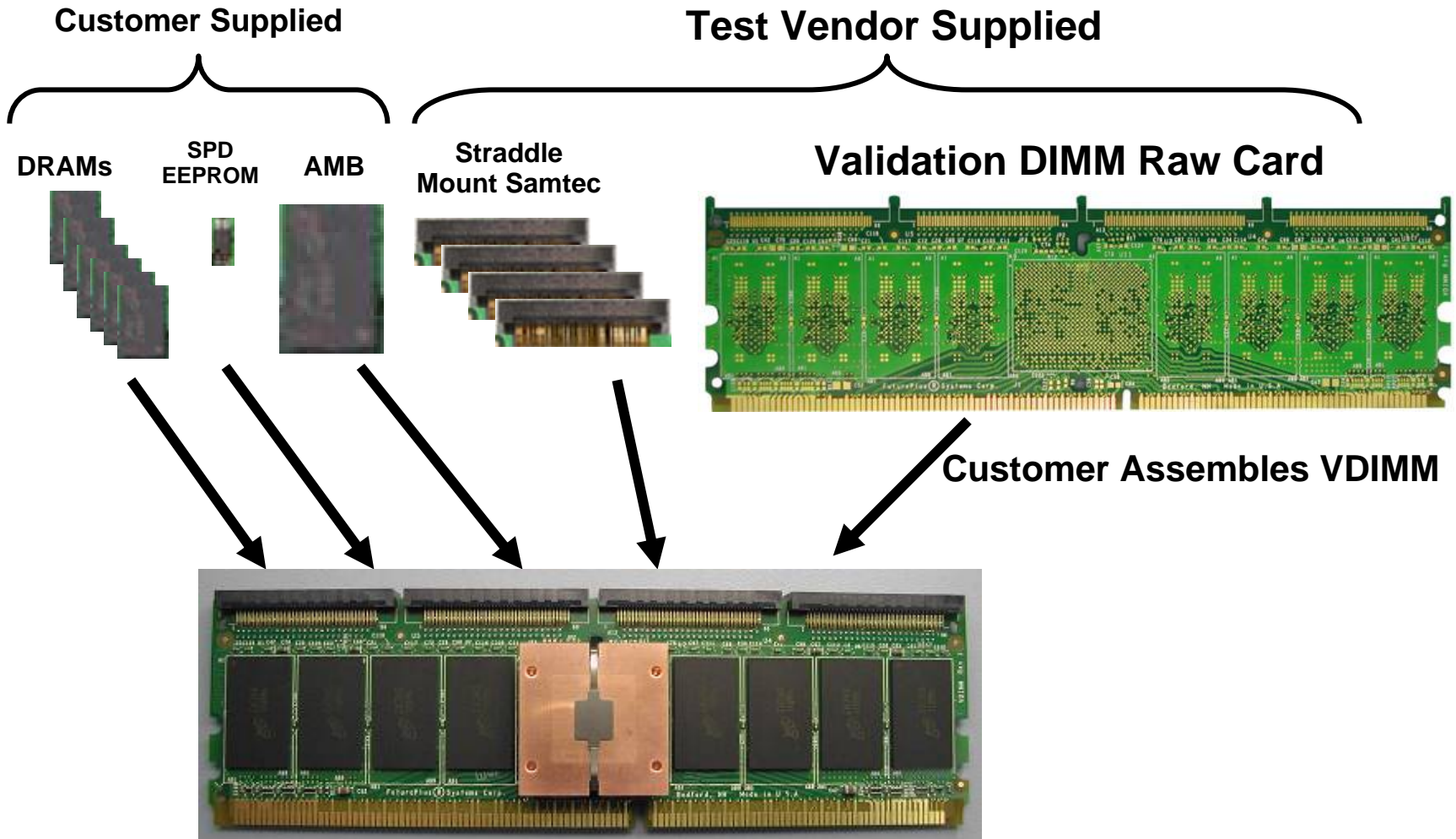
Validation DIMM (Pre-AMB)

- Functional and signal integrity validation of addr/cmd and data
- Adds 2 layers to DIMM reference design for embedded probing resistors to eliminate stub loading from routing to logic analysis connectors.
- Validation DIMM for each raw card type
- Straddle mount connector topology minimizes loading and allows probing of adjacent slots and system with limited vertical clearance.
- Supports all DDR2 DRAMs and AMB components



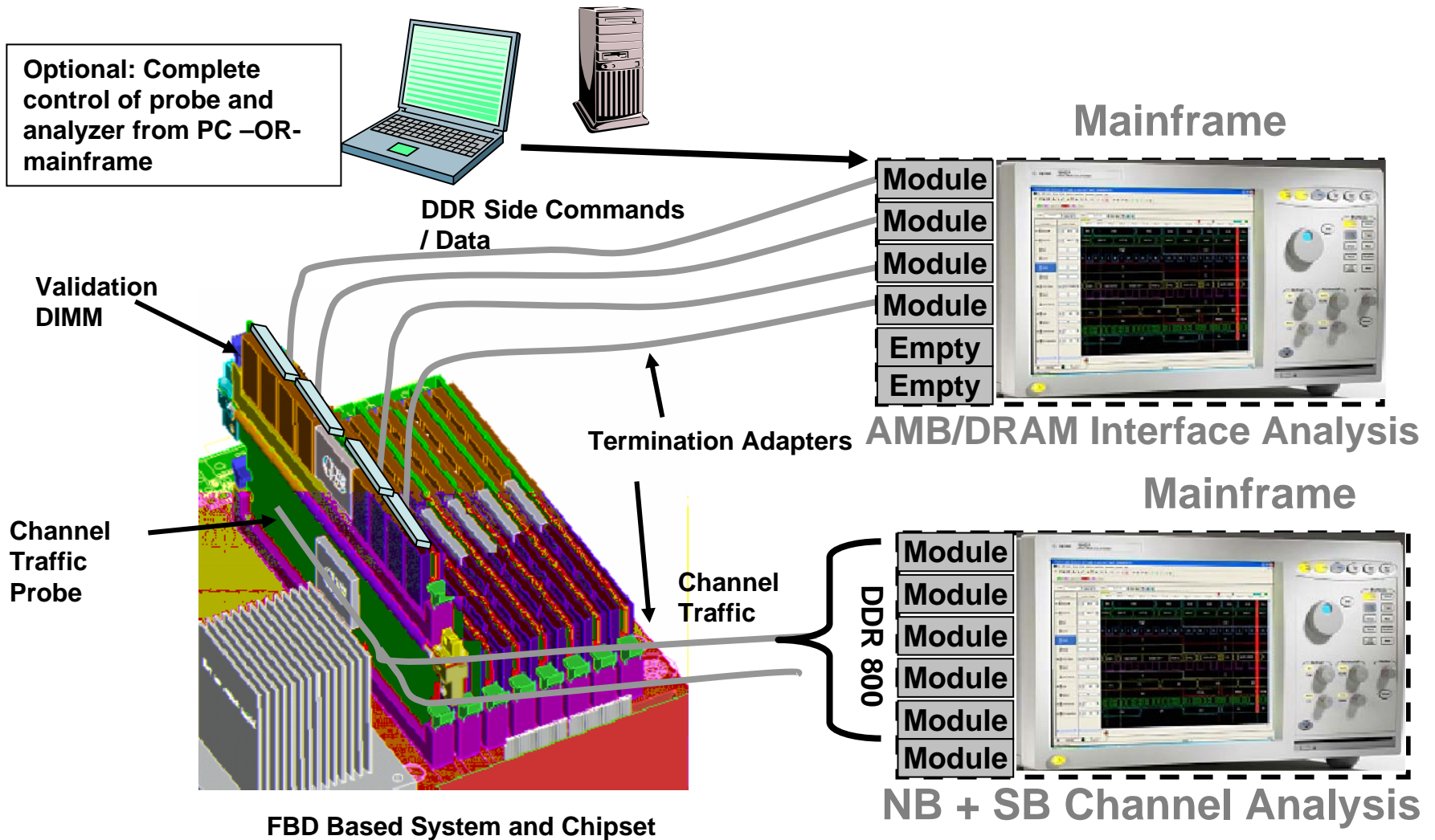
Signals	Count
CK0/CK0#	1
Addr/Cmd	28
DQ	72
DQS	18
DQS#	17
TOTAL	136

VDIMM Configuration (Pre-AMB)



Assembled VDIMM with custom combination of AMB and DRAM

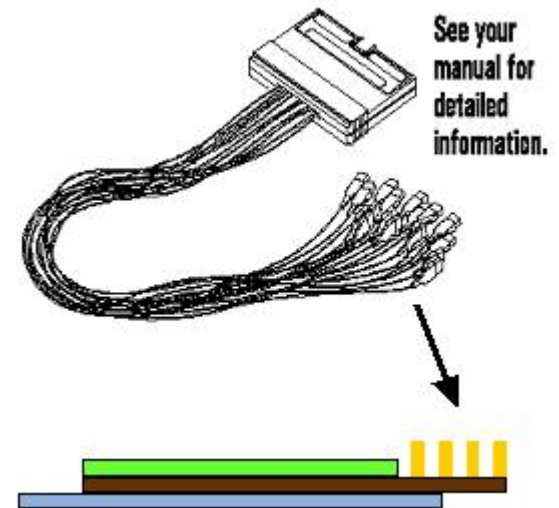
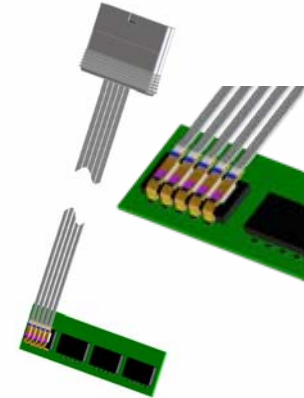
Looking at Channel & AMB/DRAM traffic concurrently



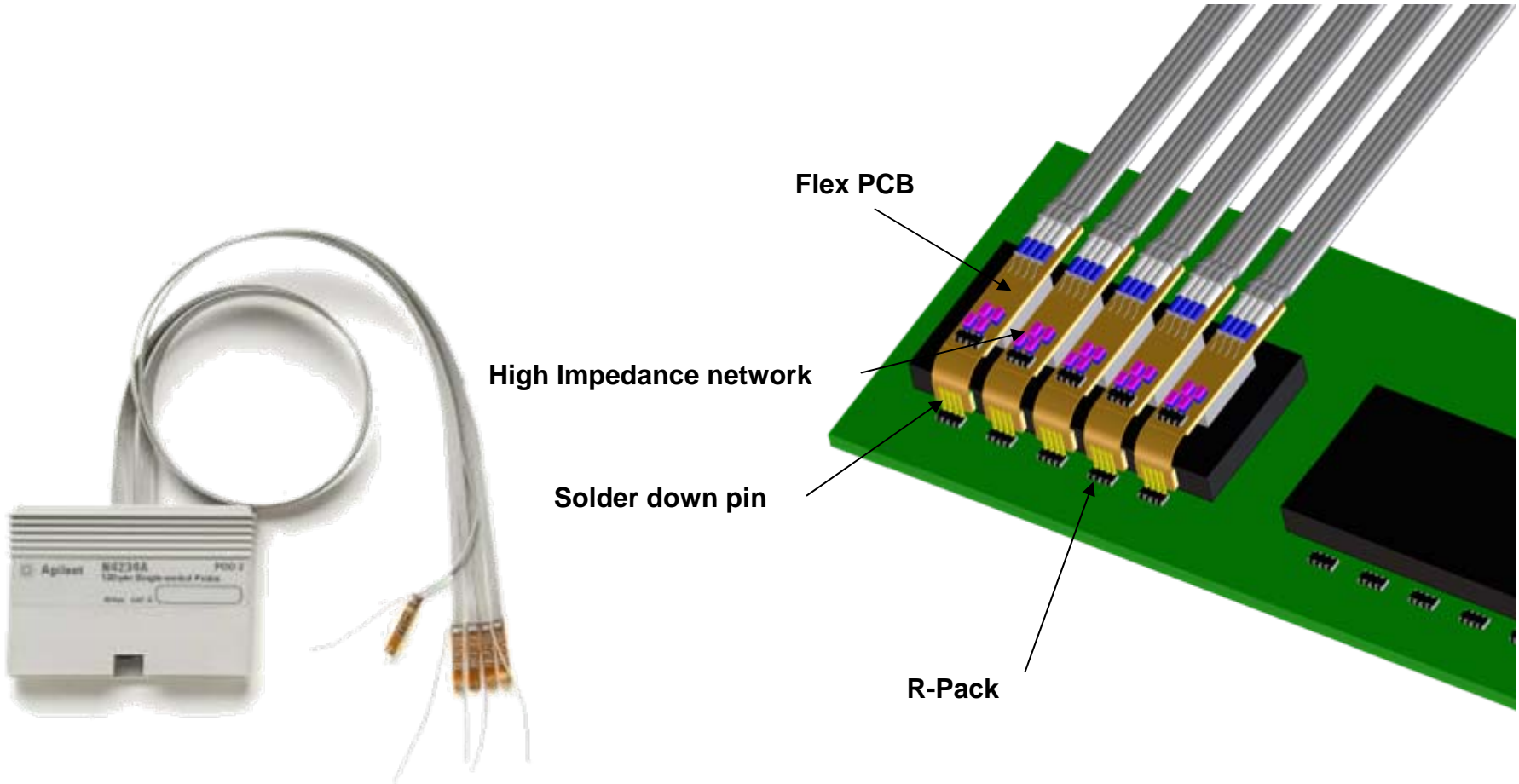
Complete Post-AMB Probing

Logic Analyzer Probing for OEM DIMMS

- RPACK Probe
 - Probing of FBD Addr/Cmd Bus to DDR1067
 - Supports all FBD Raw Cards
 - Supports DDR1/DDR2 DIMM and SODIMM
- DDR2 Probe
 - Probes DDR2 BGA packages
 - DQ/DQS/CK for x4 and x8 DDR2 DRAMs
 - Supports all FBD Raw Cards
 - Supports DIMM, SODIMM and embedded DDR2
 - Scope probing may be possible

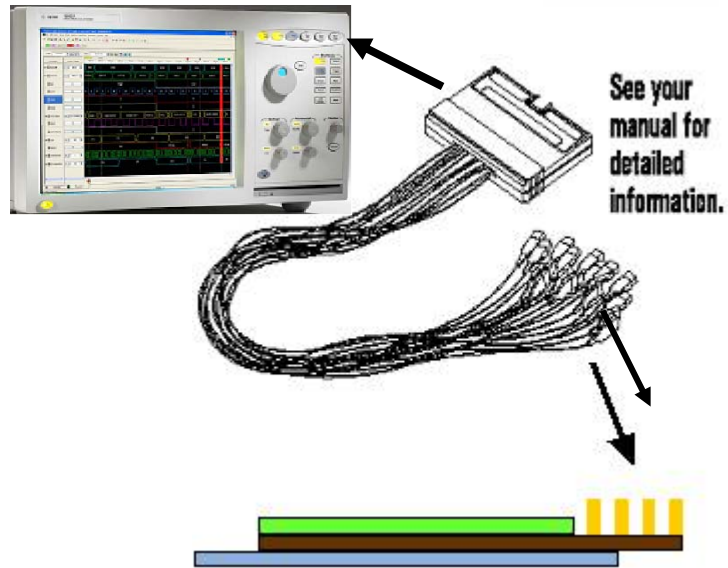
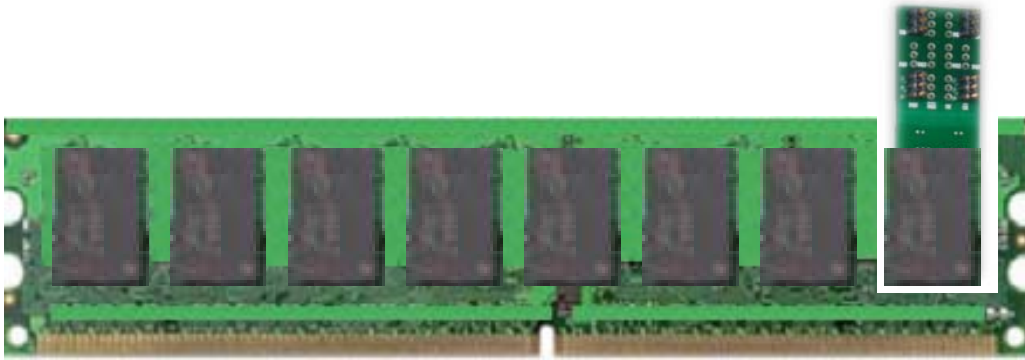
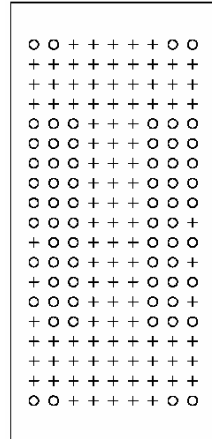


OEM DIMM Probe (RPACK)



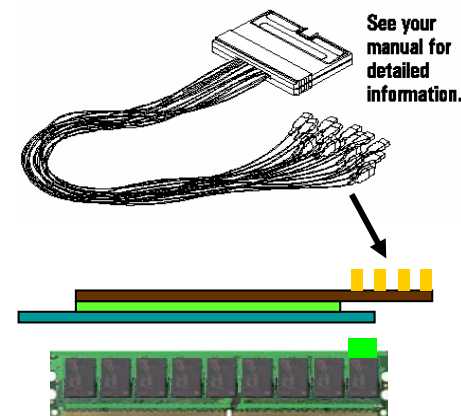
OEM DIMM Probe (DRAM)

- 0.8mm micro-BGA probe of DQ/DQS using flying lead probes
- Embedded tip resistors isolate probe from bus
- Functional and signal integrity validation (EyeScan/scope)
- Supports DDR2 common footprint (x4/x8)



Complete Pre and Post-AMB Probing

Logic Analyzer Probing for Instrumented and OEM DIMMS



RC/B Validation DIMM

- RC/B based - most commonly used DIMM
- Uses actual RC/B layout for accurate results
- Compact design minimizes loading
- Straddle mount analyzer connections for zero increase in DIMM thickness
- Right angle probes fits in tight server systems

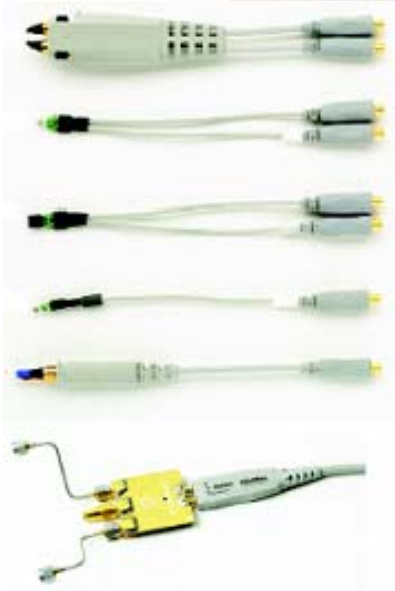
RPACK Probe

- Probing of FBD Addr/Cmd Bus to DDR1067
- Supports all FBD Raw Cards
- Supports DDR1/DDR2 DIMM and SODIMM

DDR2 Probe

- Probes DDR2 BGA packages
- DQ/DQS/CK for x4 and x8 DDR2 DRAMs
- Supports all FBD Raw Cards
- Supports DIMM, SODIMM and embedded DDR2
- Analog scope connection with high bandwidth probes

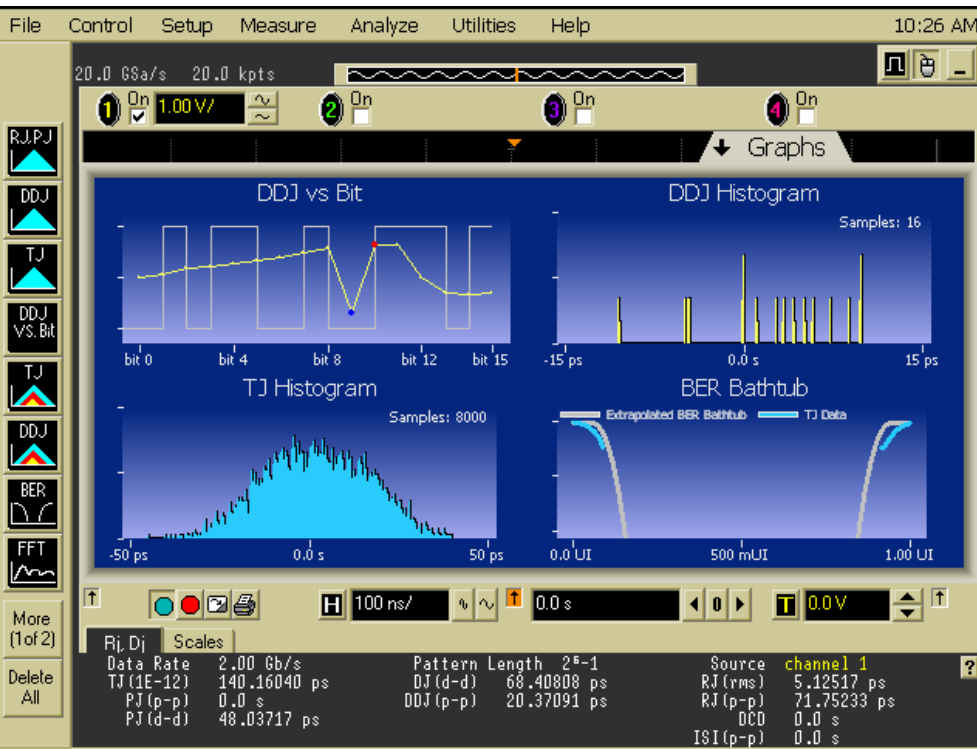
FBD Requires Bandwidth



- **Recommended - 13 Ghz Real Time Scope with very high bandwidth probes or FBD parametric fixtures provide bandwidth required for 4.8Gb FBD measurements**

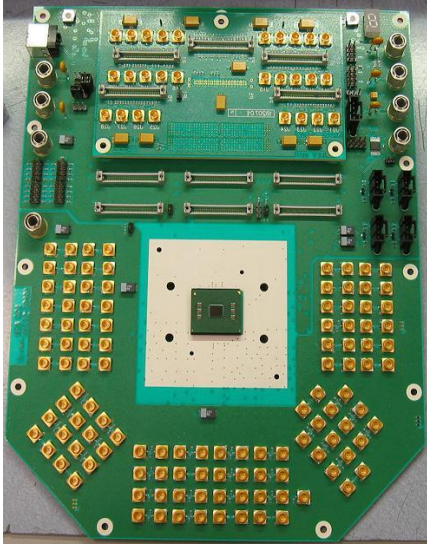


Comprehensive Data Analysis



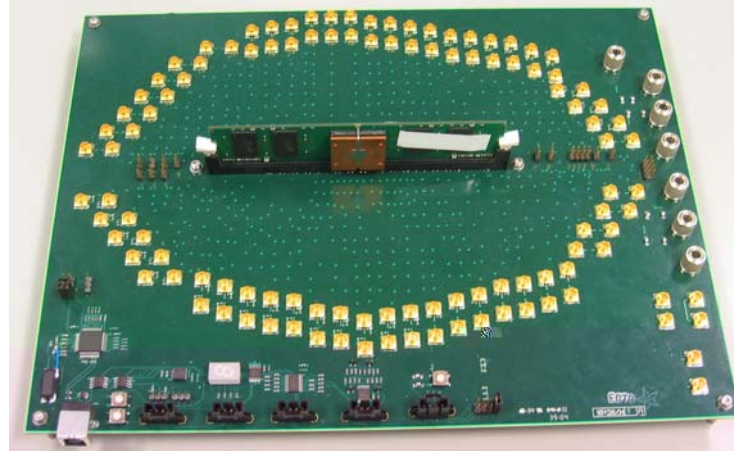
- Complete Jitter Analysis
 - RJ/DJ (ISI,DCD, Periodic jitter) separation
 - Jitter histograms
 - Spectral analysis
 - Traceable to individual bits
 - Bathub BER analysis
- FBD Mask and Compliance Test
 - Real Time Eye
 - Eye unfolding identifies failure pattern
 - Fixture control and compliance test suite integration

Graduated Physical Layer Parametric Test



AMB Parametric Test

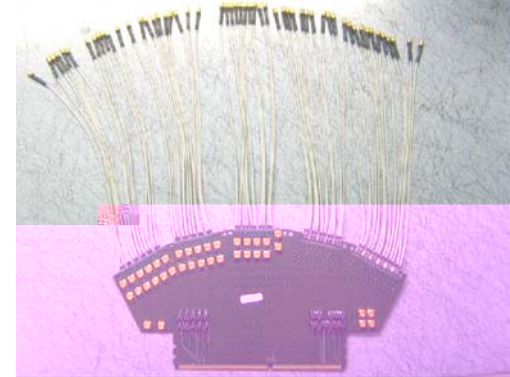
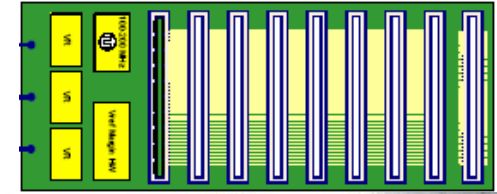
- AMB Die and Package focus
- Jedec Tx/Rx, BERT, Return Loss, etc.
- Package modeling



DIMM Parametric Test

- Adds DIMM and connector to test environment
- DIMM and connector impact on Channel specification
- Supports all Raw Cards
- Simplifies failure analysis

Characterized with S-parameters for de-embedding fixture impact



N4238A Slot Parametric Probe

- Adds MB and second connector to test environment
- System channel SI performance
- Supports any FBD channel
- Simplifies failure analysis

• Anyone awake? 😊

Summary and take aways...

- Serial Links ramping up to 5-6Gb (per lane), probably higher
- Parallel signaling ramping up to 9.6Gb (e.g. FBD)
- Equipment out there to help you design any interface you want!
Scope, LA's can also be used as a general purpose debug tool
(for proprietary interfaces)
- Probing is KEY (both at PHY and logic/protocol layers, don't think you can use a conventional probe to look at multi-gigabit signaling)
- Use the automated tools that are available to help you validate your interfaces
(i.e. Automated mask testing on scope, predefined DDR IA's, etc)