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Agilent Technologies

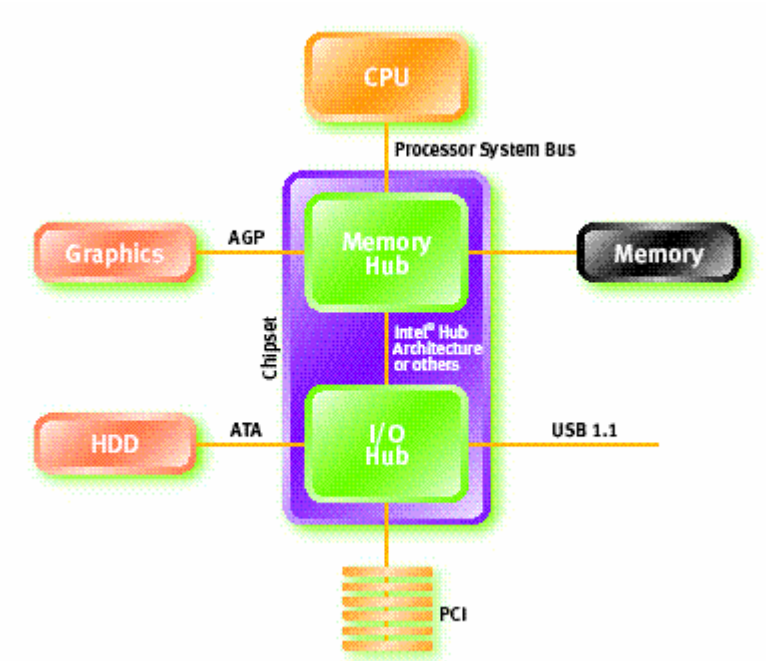
"Overview of Significant Changes in Computer Architecture and Tackling the Challenges of High Speed Digital Interfaces"

…with a Focus on PCI and Memory

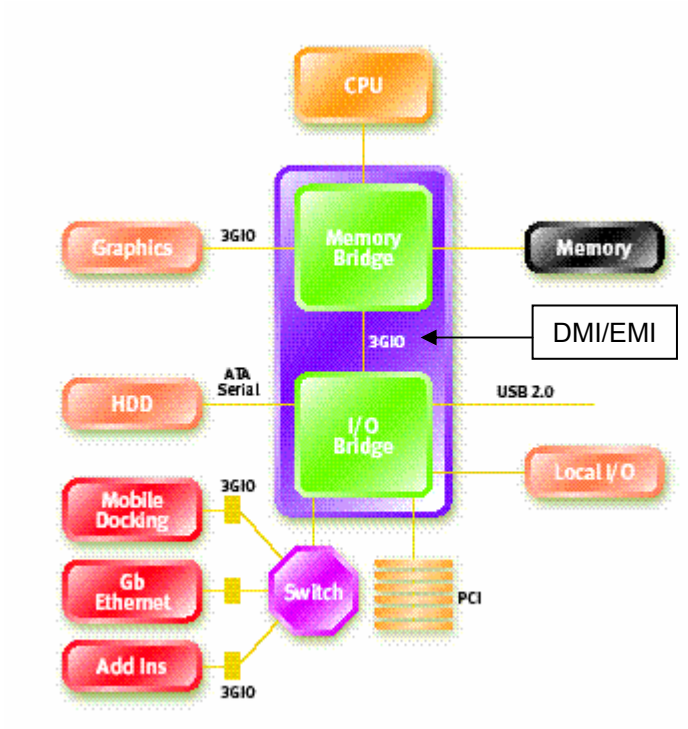
Agenda

- Changes in chipsets
- Intro to current/new interfaces
- Commonalties in interconnects (serial/parallel)
- Tool lifecycle
- PCI Express (including new tools)
- Fully Buffered DIMM (including new tools)

Computer System Topologies



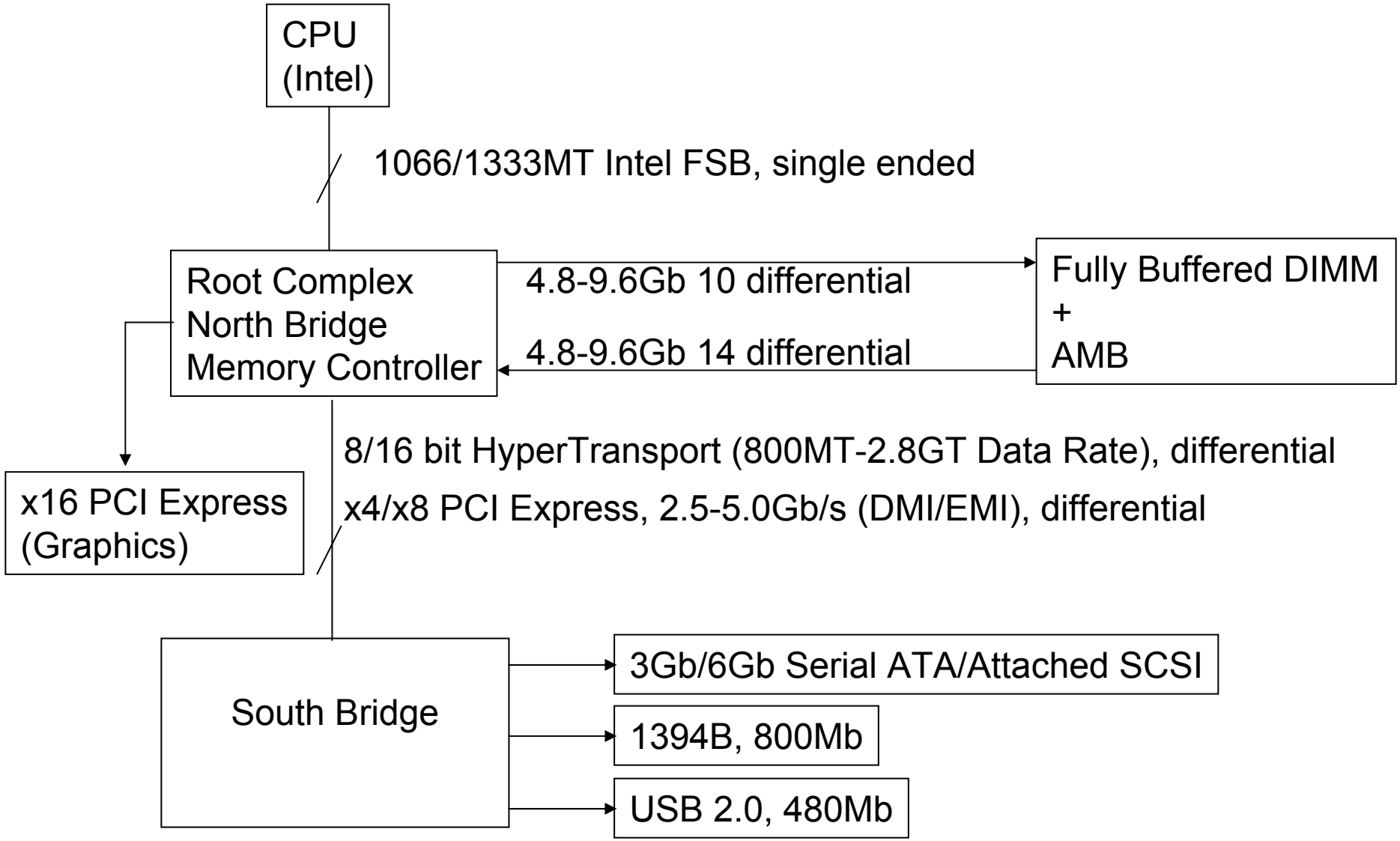
Mid 90's



Circa 2002

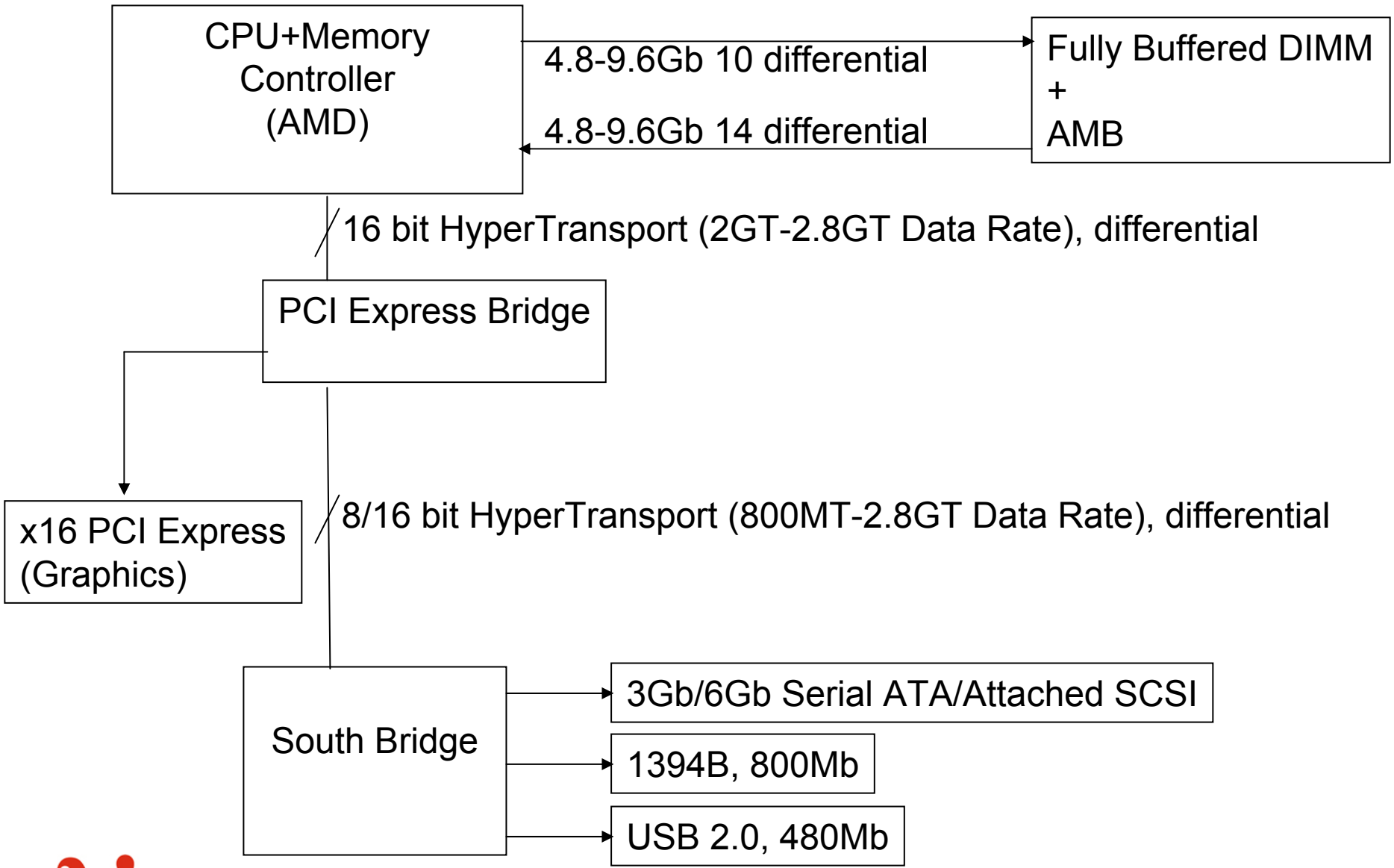
2005-2007 Based

Intel Based



AMD Based

2005-2007 Based



Created by Rohit Bhasin

Digital Technologies in the Bay Area

- Serial ATA/Attached SCSI
- Fully Buffered DIMM
- PCI Express
- PCI-X 2.0
- Hypertransport
- Intel FSB
- DDR I/II/III
- USB 2.0/Firewire 1394B
- Infiniband 1x, 4x, 12x
- FibreChannel 4Gb/s, 6/8Gb/s, 10Gb/s
- 1Gb/s, XAUI 10Gb/s Ethernet over copper
- Advanced TCA
- SPI 4.2
- Serial Rapid I/O
- Digital Video Interface
- High Definition Multimedia Interface

Transitions and Commonalities in Interconnect Technology

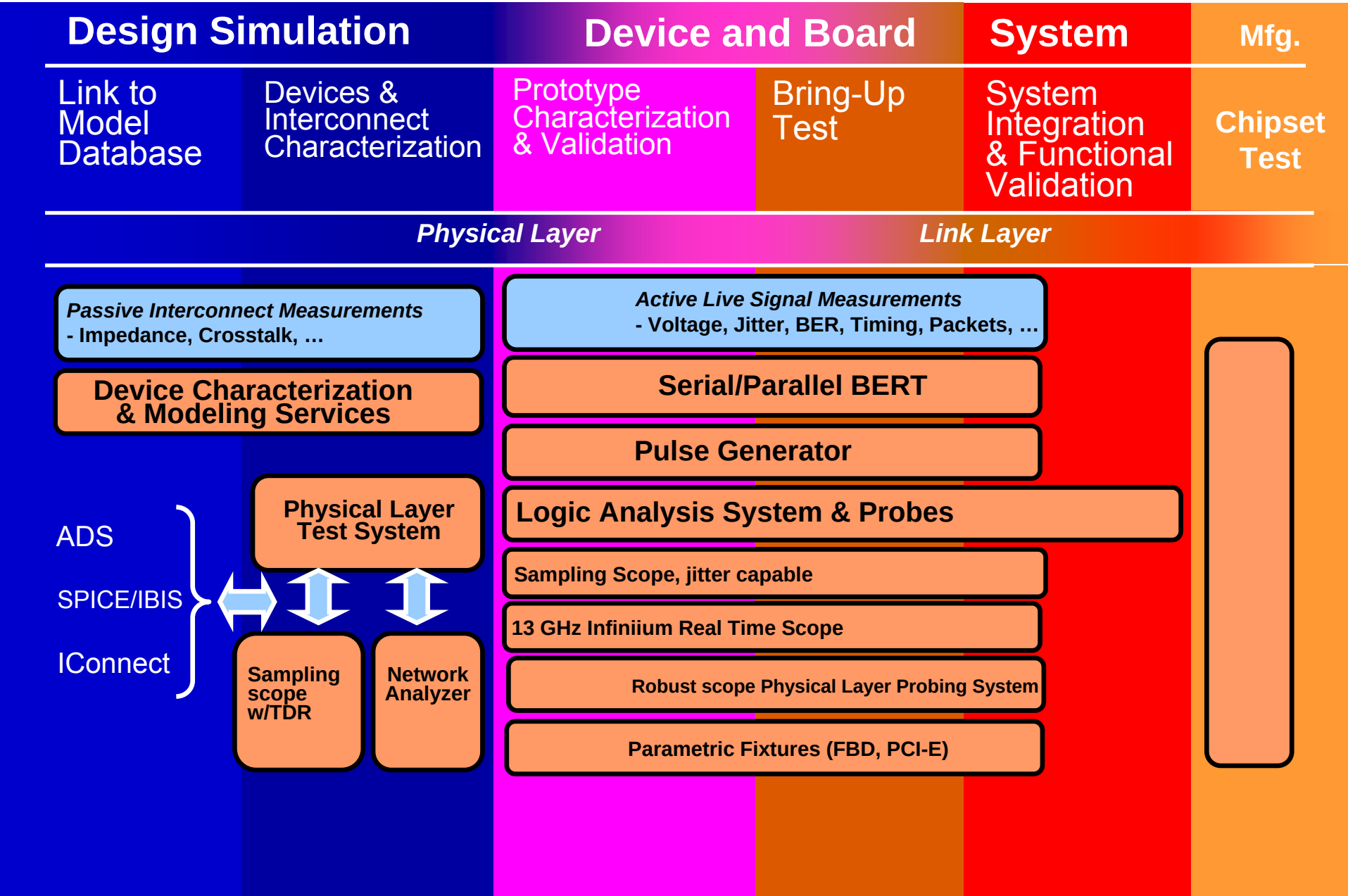
High Speed Serial

- Differential Signaling
- Embedded Clock, CDR
- Spread Spectrum, EMI Reduction
- Reduced Pin/Signal Count
- Packet Based Transactions
- Improved Quality of Service

High Speed Parallel

- Differential (e.g. FBDIMM, HyperTransport)
- Single Ended (e.g. DDR2, DDR3, Legacy Intel FSB)
- Clk rates increased (multi-gigabit)
- Reduced slot count (e.g. PCI-X, DDR3)
- Improved Quality of Service, ECC
- Reduced Pin/Signal Count

Lifecycle Tools for Multi-Gigabit Designs



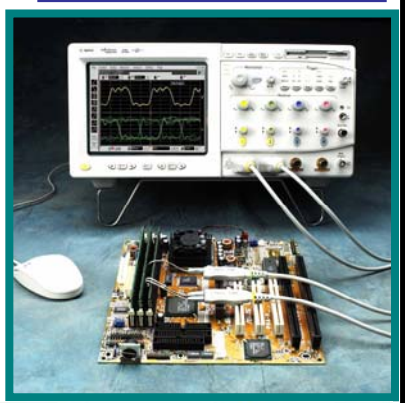
PCI Express Validation Methodologies

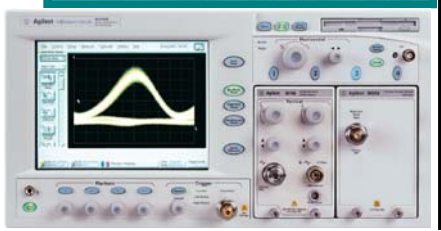
Rohit Bhasin

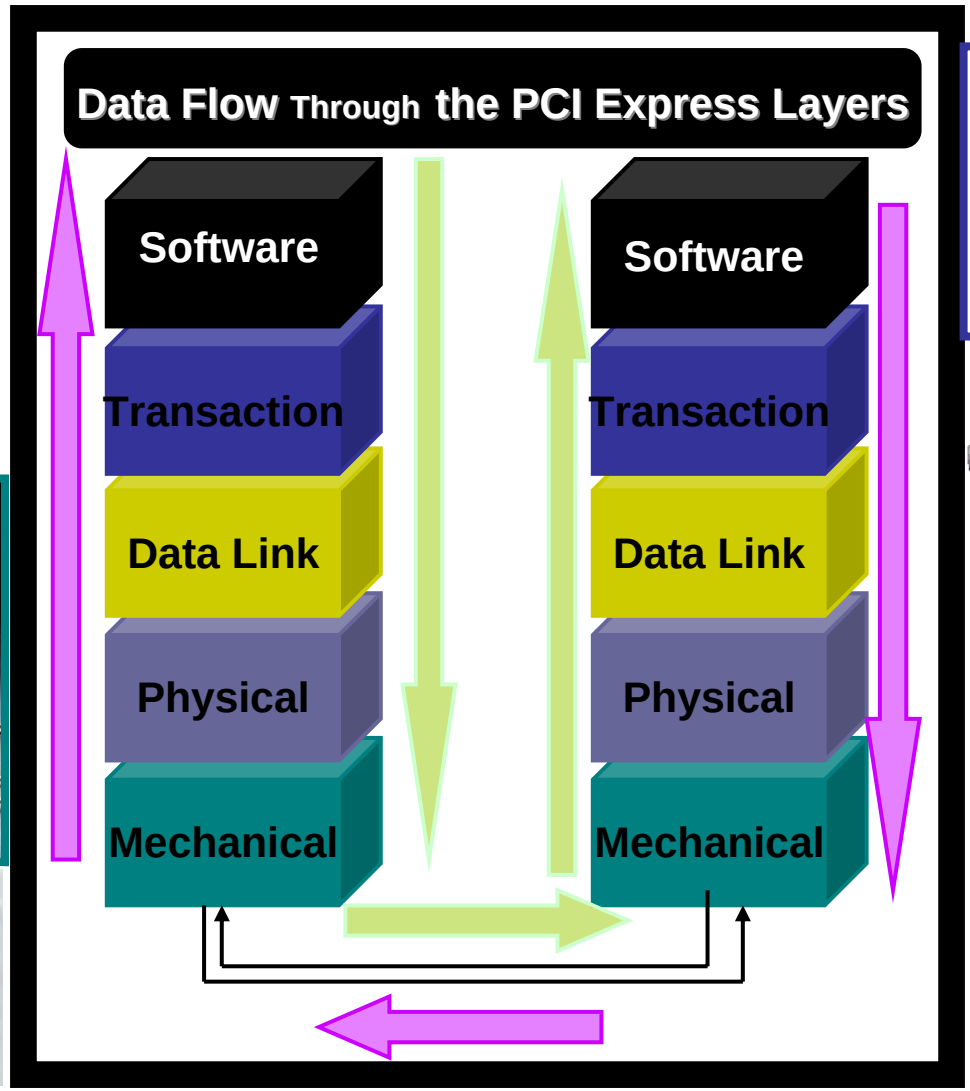
Agilent Technologies

Presented at PCI-SIG
Developers Conference
June 2004

PCI Express Debug Challenges







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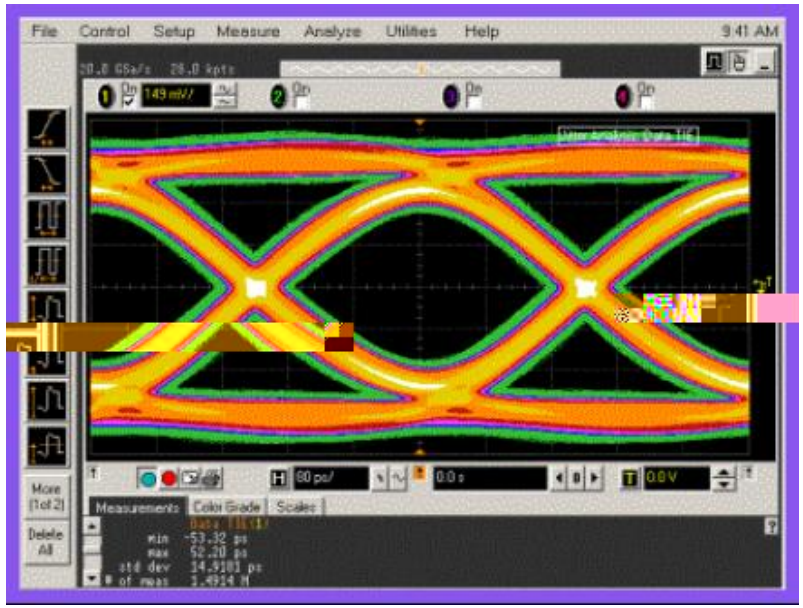
PCI Express Validation Steps

Signal Integrity - Verify the 2.5/5.0 Gb design

- Eye Measurements
- Capture waveforms
- Measurement on parameters (jitter analysis, mask test, etc.)
- Board and Component characterization
- BERT



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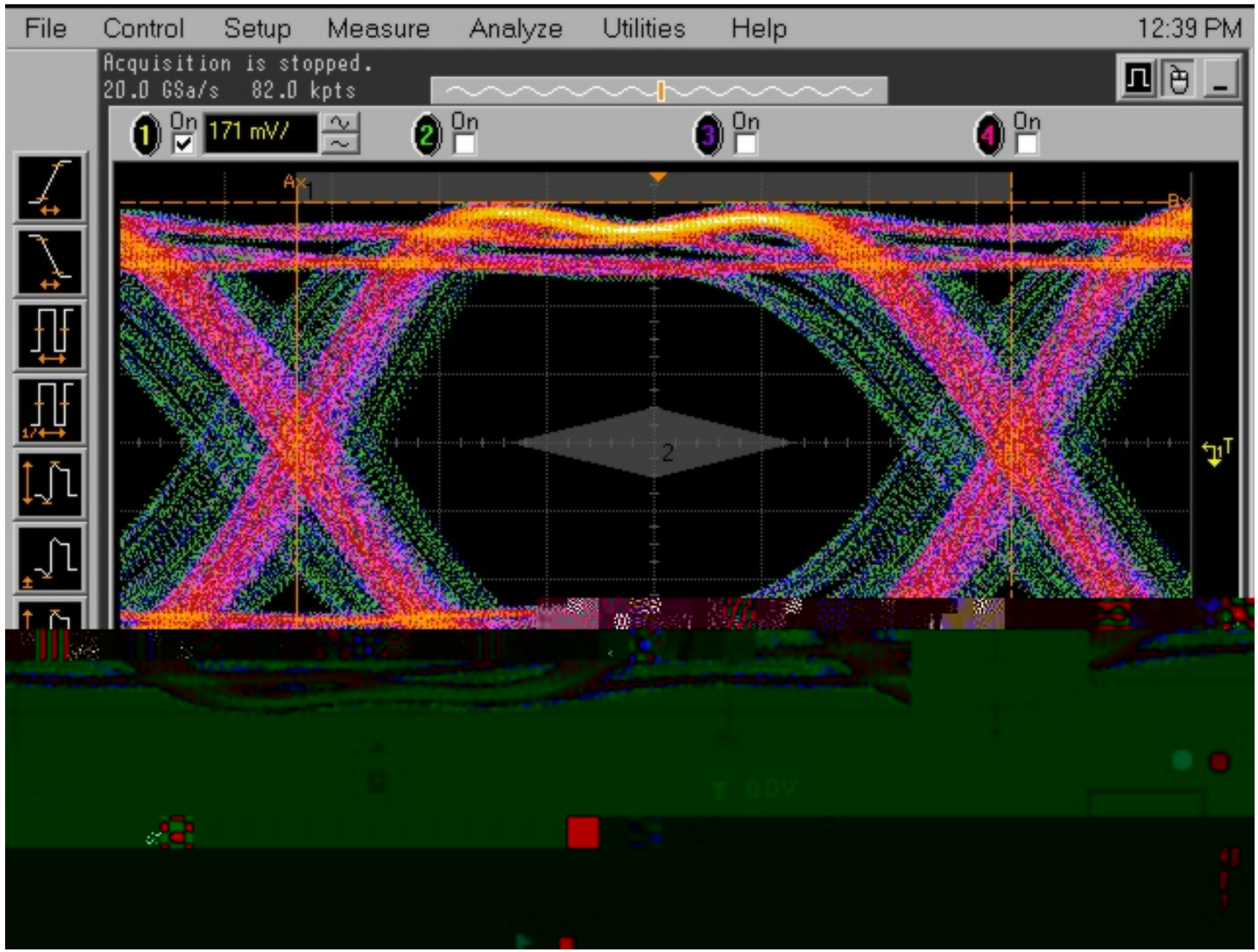
Serial Data Analysis Toolkit

- Clock recovery and serial data analysis for high-speed serial data signals
- Masks for PCI Express, Serial ATA/Attached SCSI, Fibre Channel, and XAUI
- Real-time eye diagram display
- Time interval error (TIE) jitter measurement
- First-order or second-order PLL clock recovery, and PCI Express clock recovery (provided by PCI-SIG)

An example using the Serial Data Tool

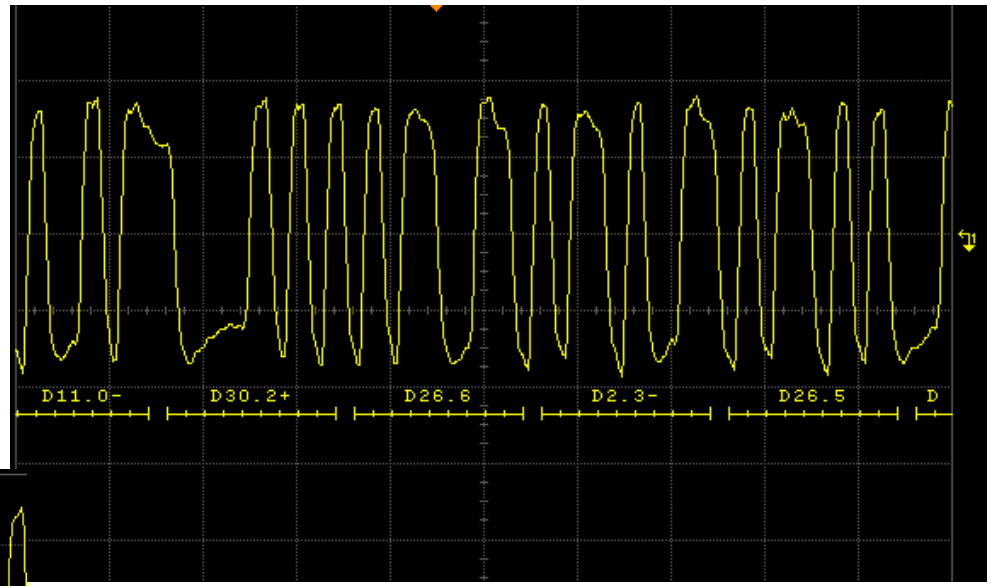


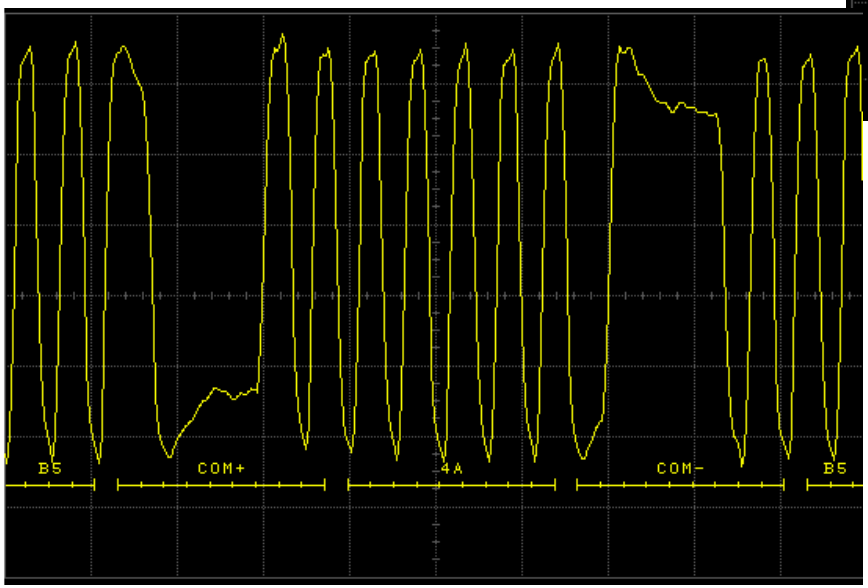
Features and Capabilities

- 8b/10b decoding
- 8b/10b search
- 8b/10b trigger
- Real time eye mask violation unfolding

8b/10b Decoding

Symbols in the serial data stream can be decoded and displayed as hex or decimal values, or as labels

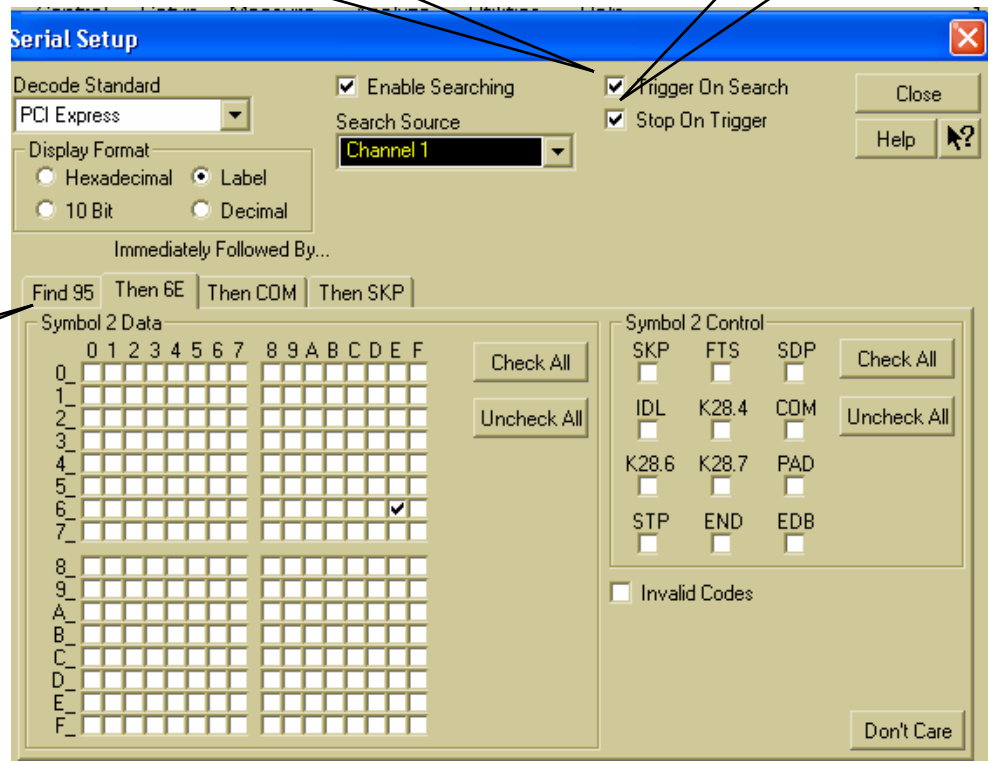




Search and trigger

Display only those acquisitions where the specified sequence of symbols is found

Stop acquisition when pattern is found



Specify up to 4 symbols in sequence

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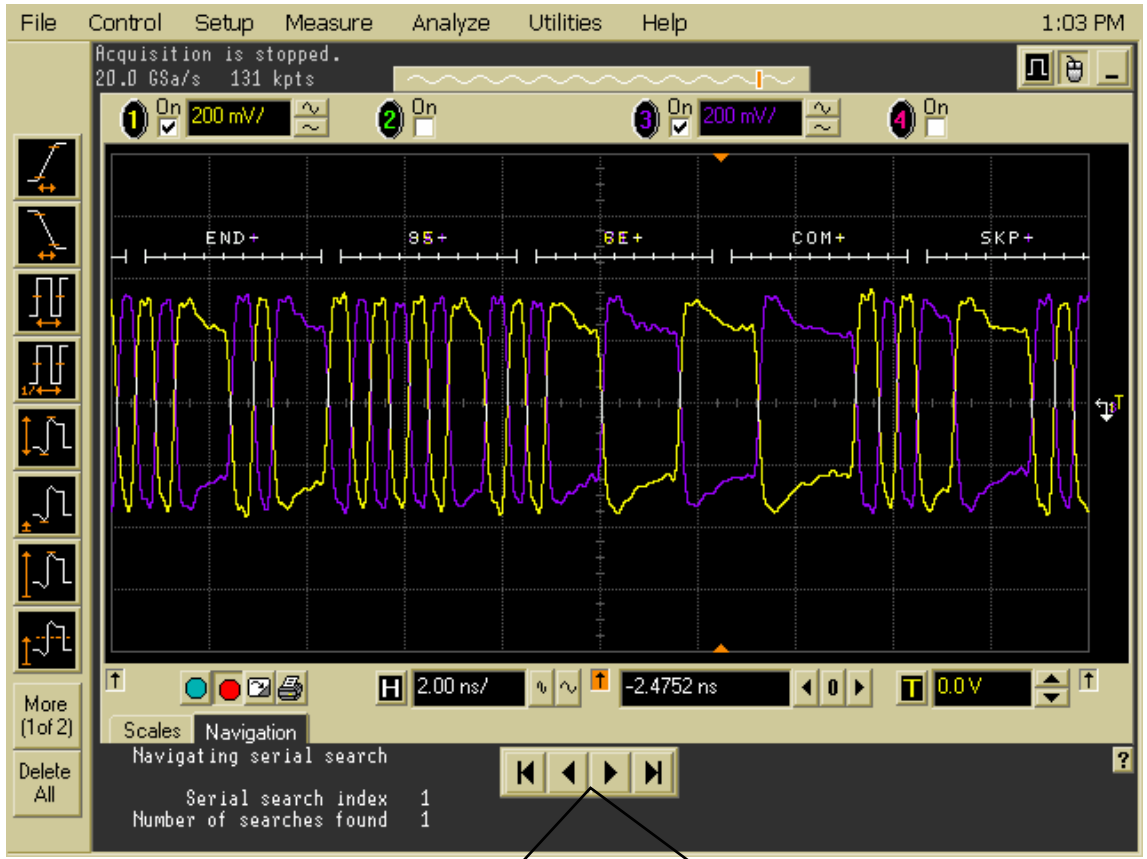
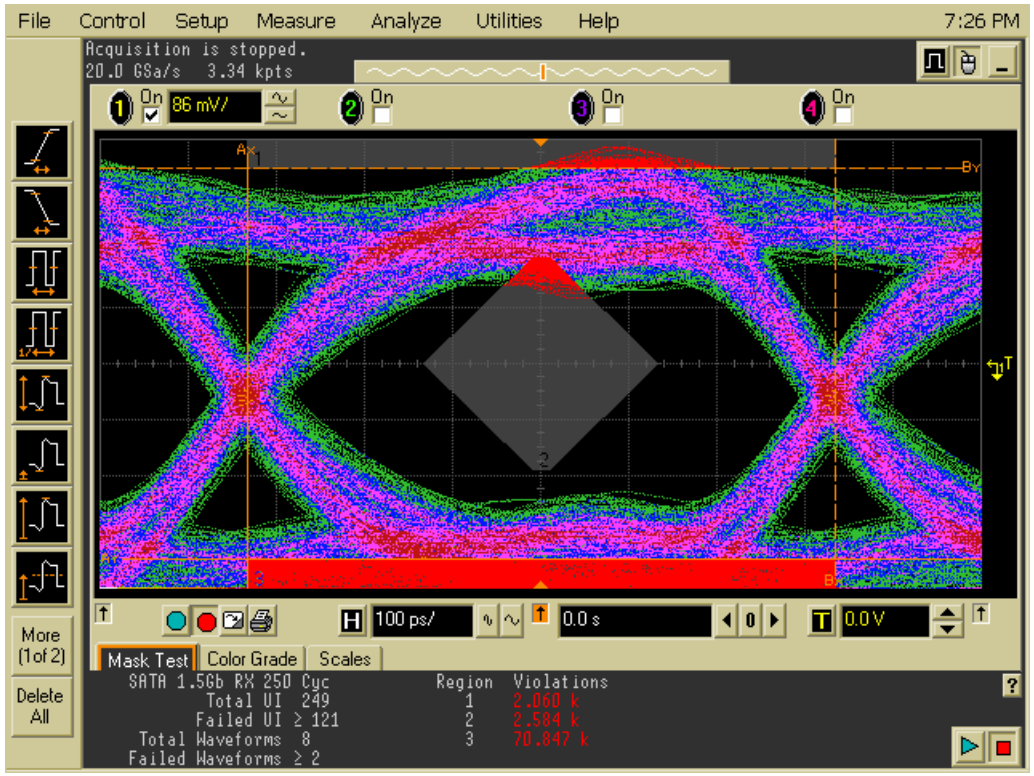
Search Navigation



Navigate to all the instances of the specified sequence of symbols using the arrow keys

Locating mask violations and failures

The real-time eye combined with the PCI Express mask test indicates there were multiple violations. But how do you gain insight into the individual violations by looking at the composite eye?



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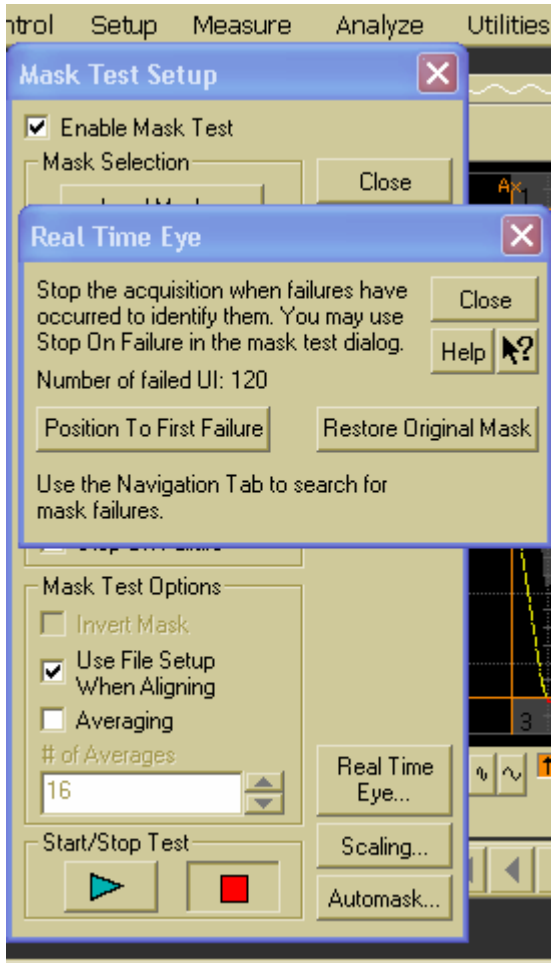
Locating mask violations

Using the controls, we can instruct the scope to go to the first violation in the serial data stream.



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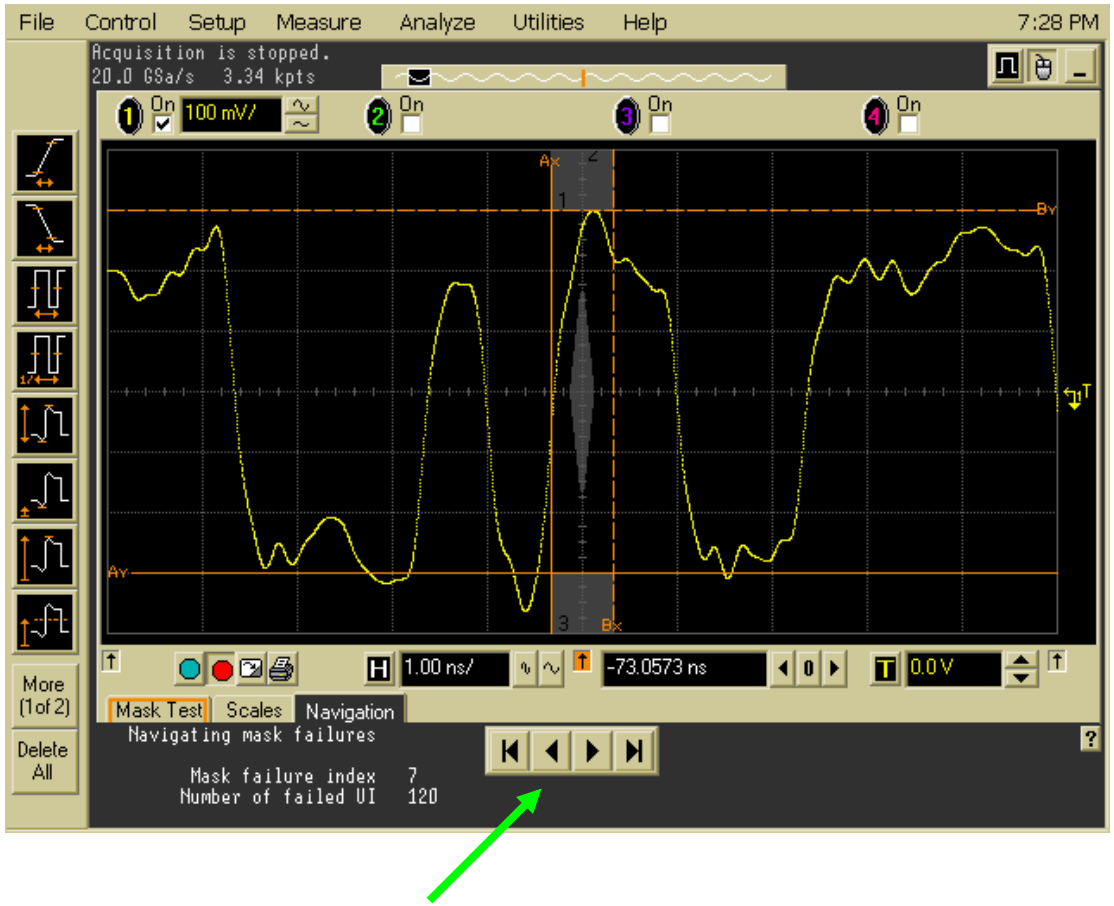
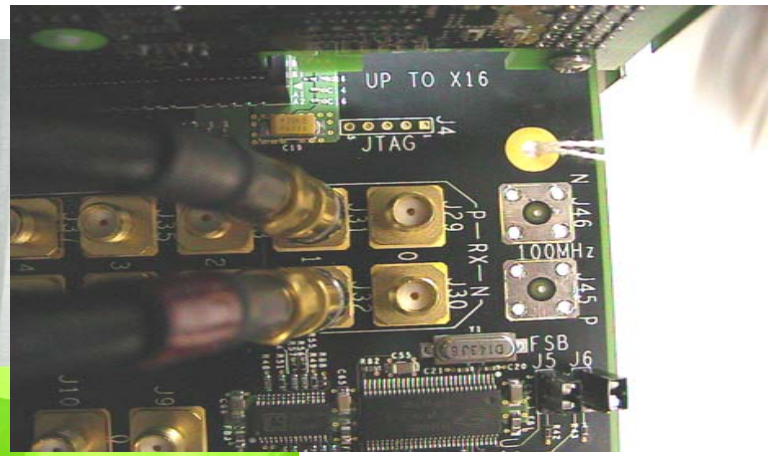
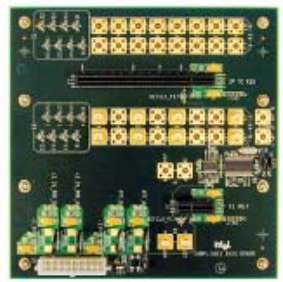
Locating mask violations



You can use the arrow keys to view each violation individually.

PCI Express Compliance Test Setup (add-in card)





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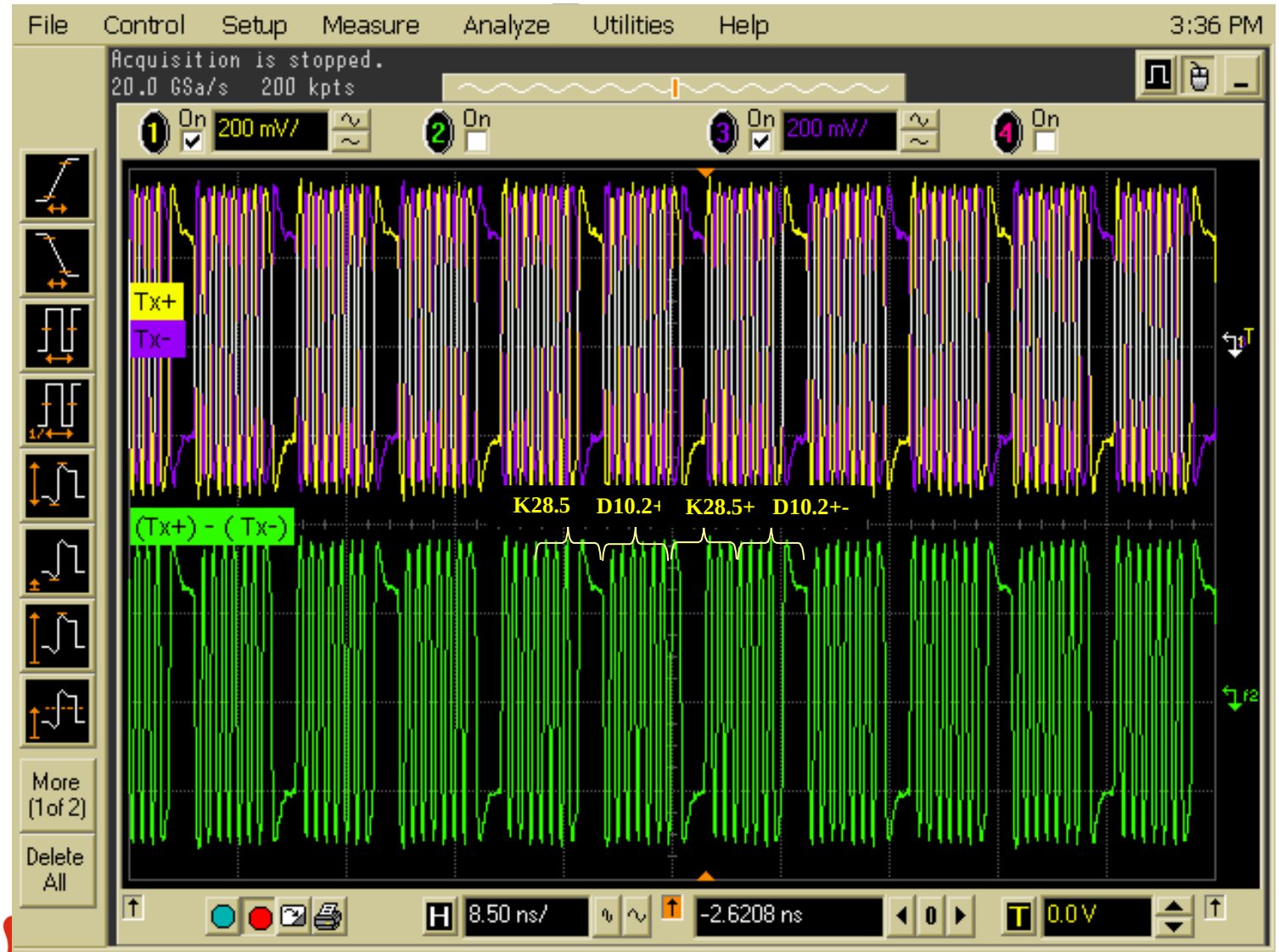
PCI Express TS-1 Compliance Test



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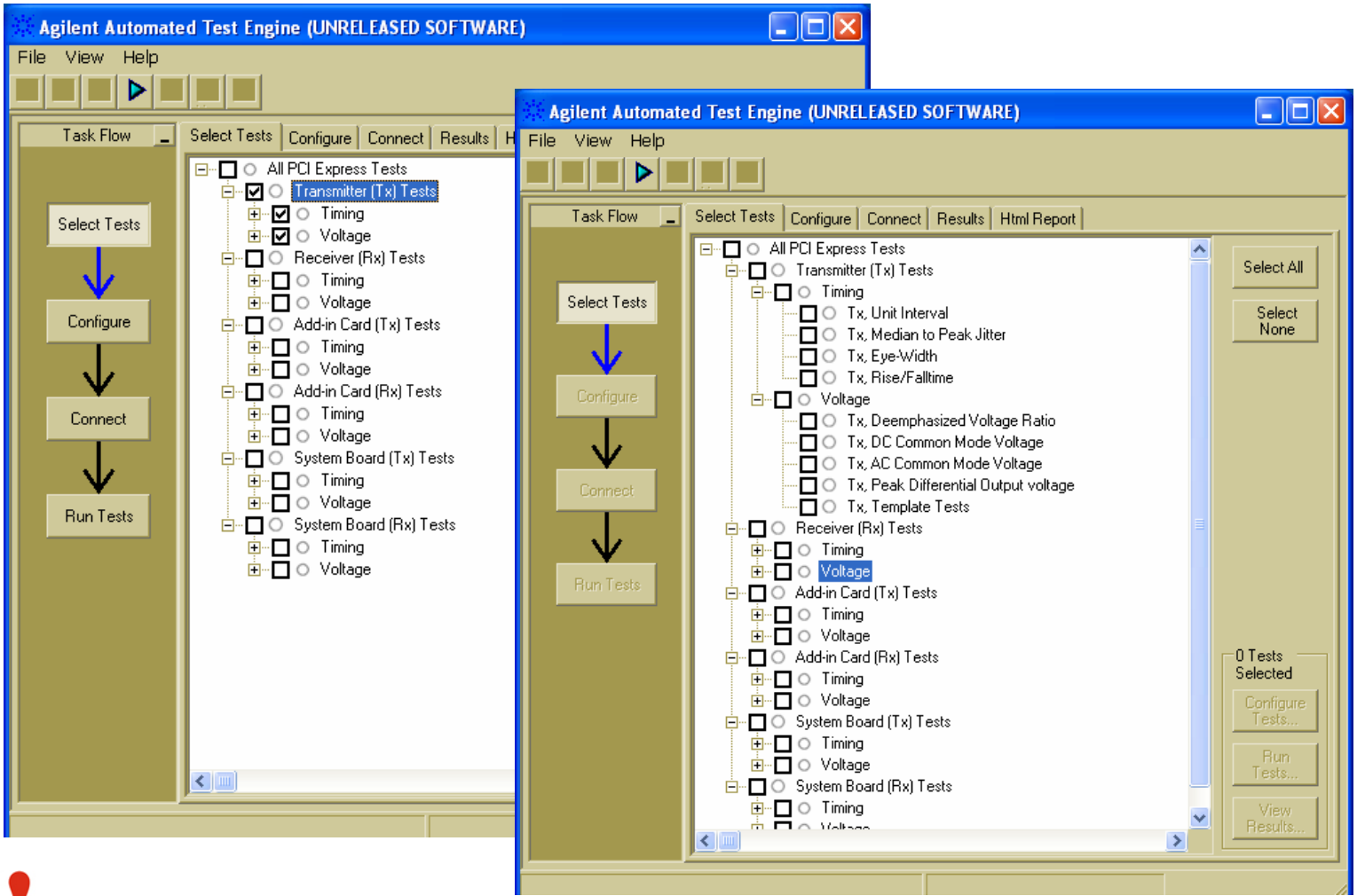
PCI Express Compliance and Validation Tool Suite



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PCI Express Compliance Report Showing Marginal Performance Analysis

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PCI Express Compliance Report

Overall Result: FAIL (3 of 35 Tests Failed)

Test Configuration Details	
Test Date	Jan 27, 2004, 21:04:30
Instrument ID	Agilent Technologies,54855A,No Serial,A.03.18,001,EZJ,SDA
Probe ID	1134A
Serial Number	Jan 27, 2004, 21:04:30
Calibration Status	All Passed

Summary of Results

Margin Thresholds	
Warning	<=3%
Critical	<=0%

Pass	Test Name	Spec Range

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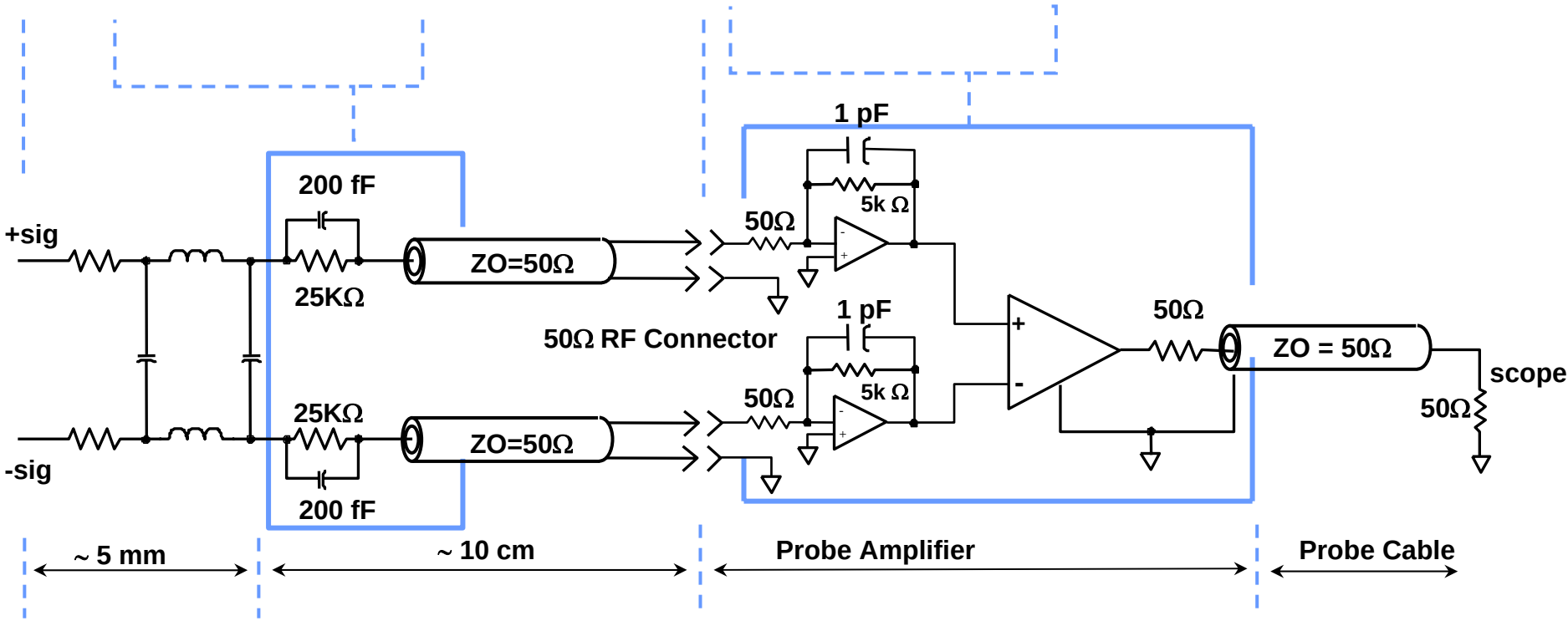
PCI Express Validation Steps

Signal Integrity - Verify the 2.5/5.0 Gb design

- Probing

New Probe Architectures



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Making Good Connections (Gen 1)

Flexibility Probe Systems

- Browser probe head
- Solder-in probe head
- Socketed probe head
- SMA probe head
- Differential and single-ended

Probing in confined spaces

10 cm solder-in probe head

10 cm socketed probe head

Differential browsing probe head

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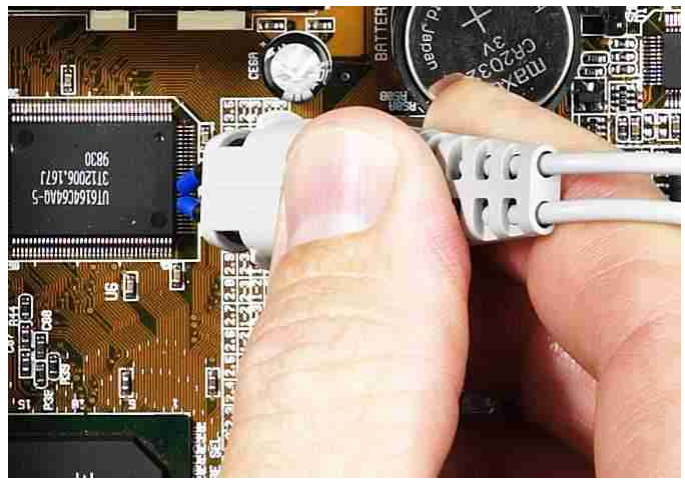
Browser Probe

Characteristics:

- 6 GHz BW
- Most versatile for hand-held probing
- Z-Axis compression enhances connection
- Adjustable tip spans
- Ergonomic sleeve
- Replaceable damping resistor tips
- Can be used with probe stand holder



Solder-in Probe (Gen 1)

Characteristics:

- 8 GHz BW
- Use for high bandwidth connection
- Least space requirement
- Replaceable damping resistors (8 mil)

Socketed Probe

Characteristics:

- 7 GHz BW
- Semi-permanent attachment
- Move between multiple test points
- Adapter for standard headers
- Standard axial lead resistors (20 mil)
- Same resistors support Logic Analyzer Flying Lead Set

Differential SMA Probe

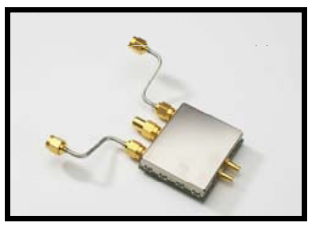
Characteristics:

- 50-Ohm Input Impedance
- 7 GHz BW
- Span-adjustable semi-rigid coax
- High common-mode rejection
- Cable loss compensation
- Cost effective adapter for existing probe amp
- Can apply DC offset bias

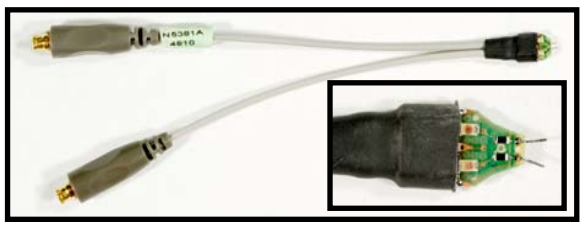
12 Ghz Active Probes (Gen 2)

Probe Amplifiers	
Specified Bandwidth	12 GHz
Characterized Probe Tips	Yes
Noise Referred to Input	2.5 mV rms
Attenuation	3.45:1
Diff Dynamic Range	3.3 V p-p
DC Offset Range	+/- 16 V
Maximum Voltage	+/- 30 V

Offers excellent bandwidth, characterized performance for various probe tips, low noise, low attenuation, good dynamic range and small size



12 GHz Differential SMA Adapter Probe Head



12 GHz Differential Solder-in Probe Head: 210 fF input capacitance, 50 kOhm input resistance, 4” reach, 2 mm probe head size at taper, 0.2-3.3 mm lead span

12 GHz Differential Browser:
210 fF input C, 50 kOhm input R, 0.2-3.3 mm lead span

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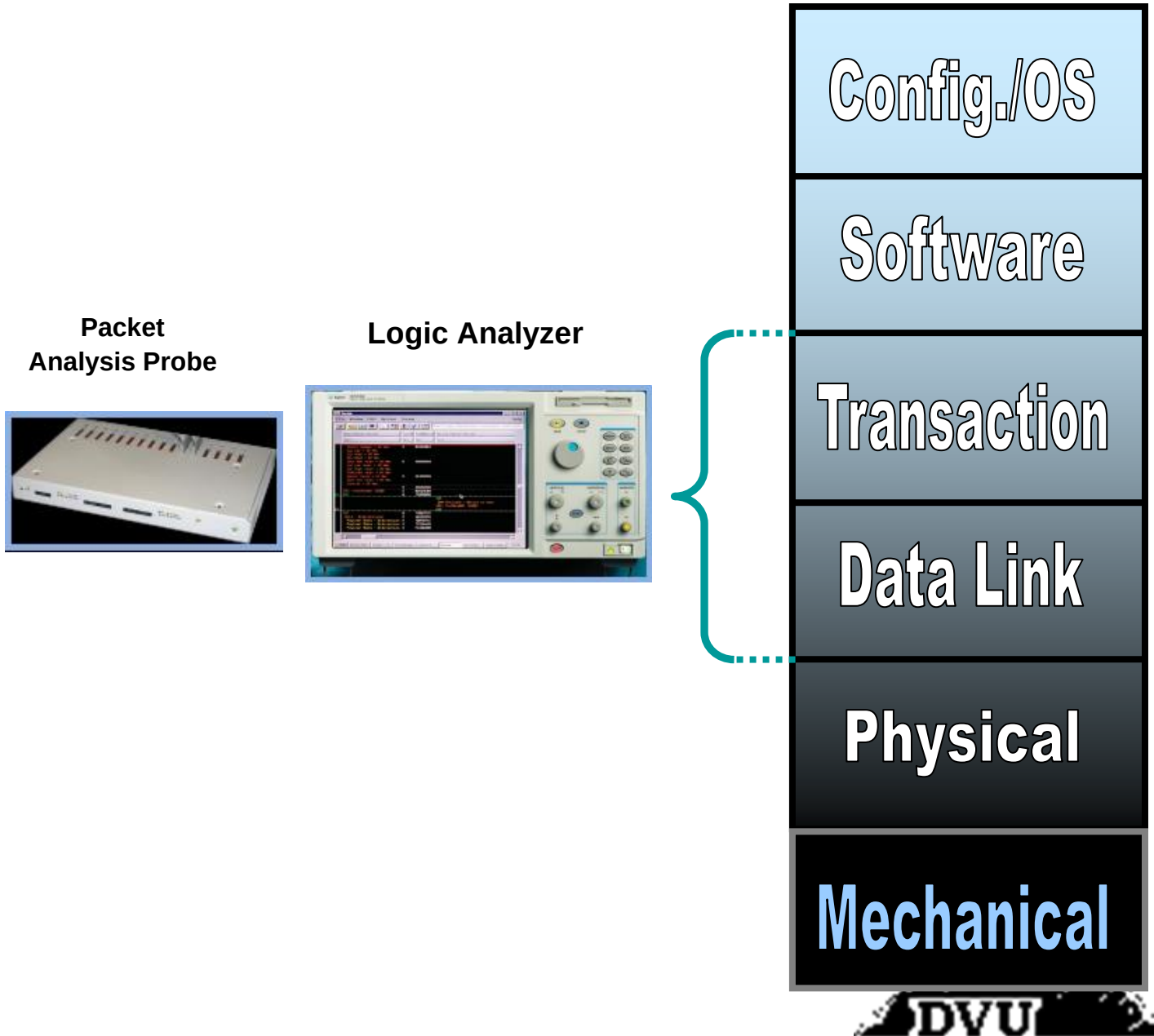
- Logic Layer PCI-E probing
- DLLP and TLP debug

Tools for PCI-Express Logic Layer debug



PCI Express Packet Analysis Probe

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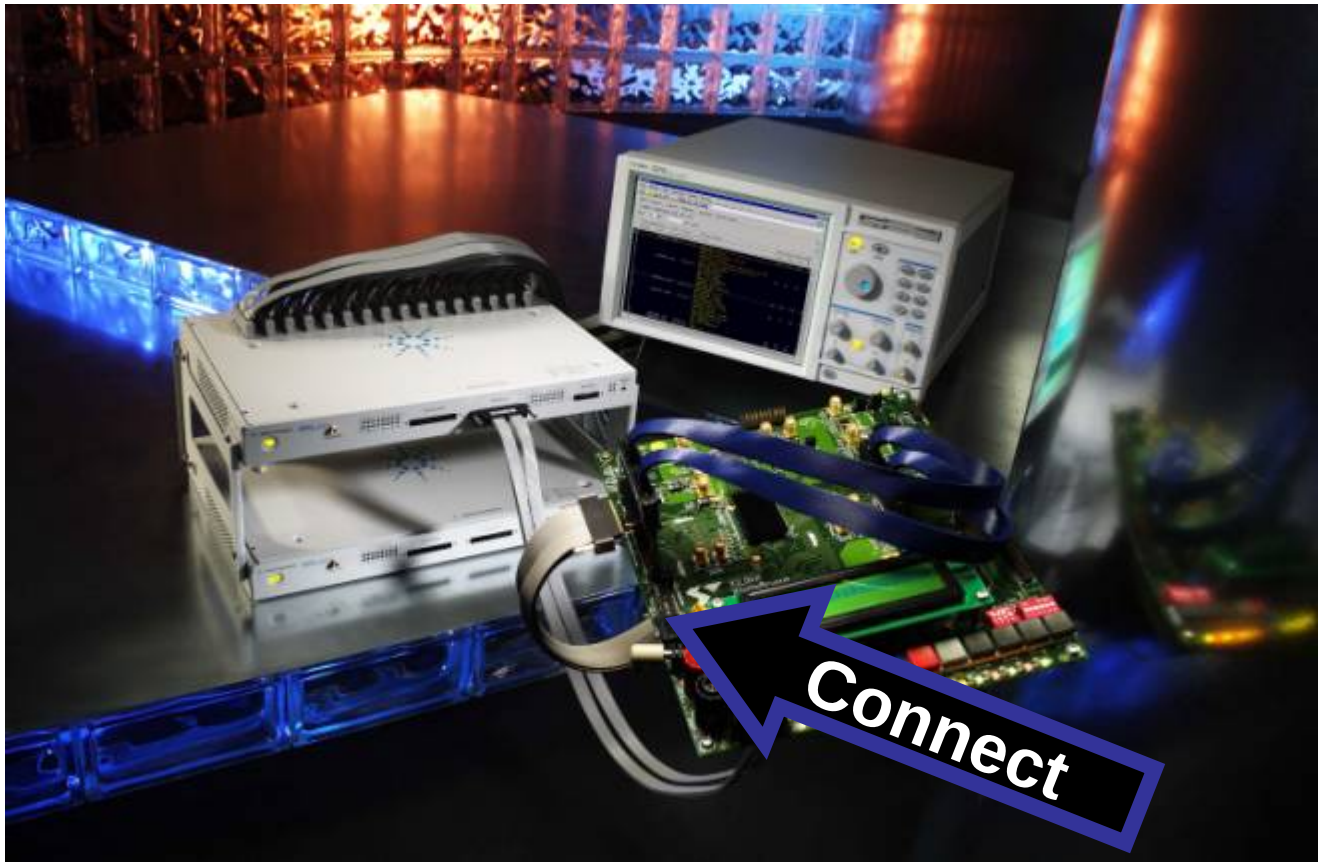
Digital Validation for PCI Express - Logic Analysis Value Proposition

- Probing
  - Non Intrusive passive observation of data flow
  - Validation of Add-in Cards Chip-to-Chip Architectures
- Packet Analysis and Display
  - Dedicated Packet Triggering in LA
  - Dedicated FPGA Hardware Pattern Recognizers in Probe
  - Software Decode Tool runs on LA
- Full System Validation
  - Cross-Bus Analysis (Time Correlated)
  - Cross-triggering correlation between scope and analyzer

Logic Analysis
PCI Express Connection



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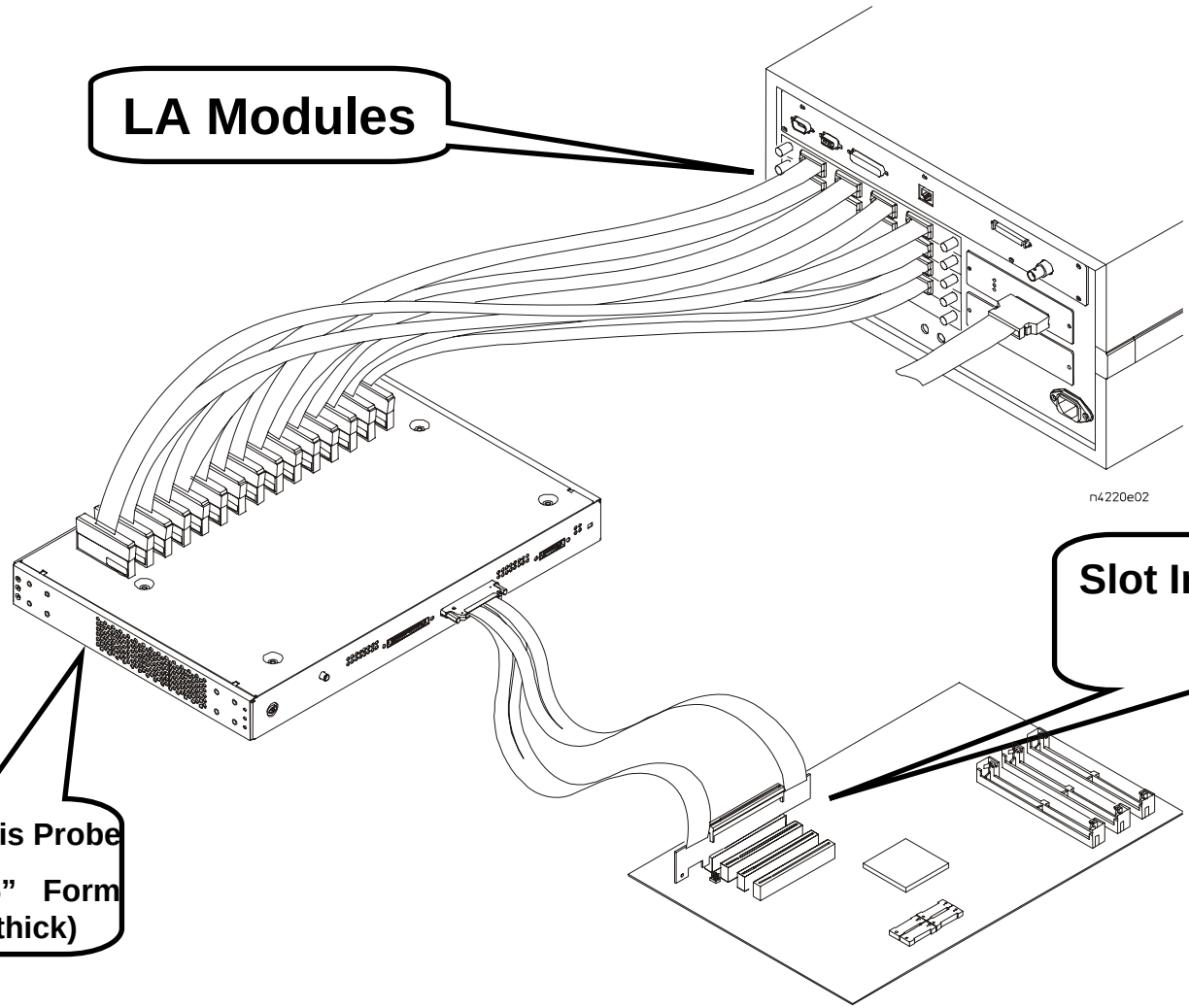
PCI Express Packet Analysis Probe Slot Interposer Solution



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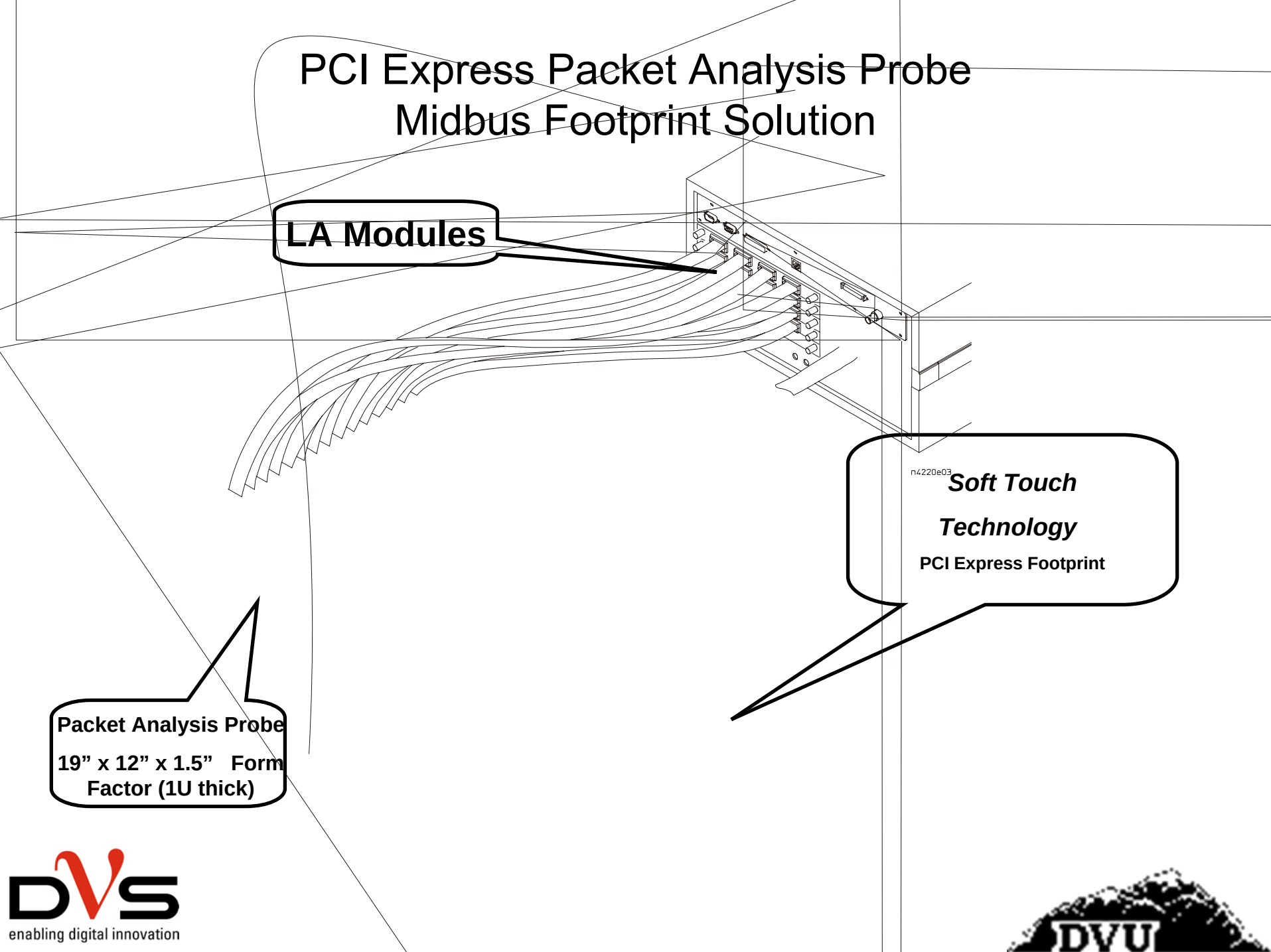
PCI Express Packet Analysis Probe
Midbus Footprint Solution



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Connect: Low Intrusion is a must

- Types of connection
  - Chip-to-Chip Link – PCI Express FOOTPRINT (Soft Touch TECHNOLOGY)
  - Card Edge
    - Slot connector/interposer

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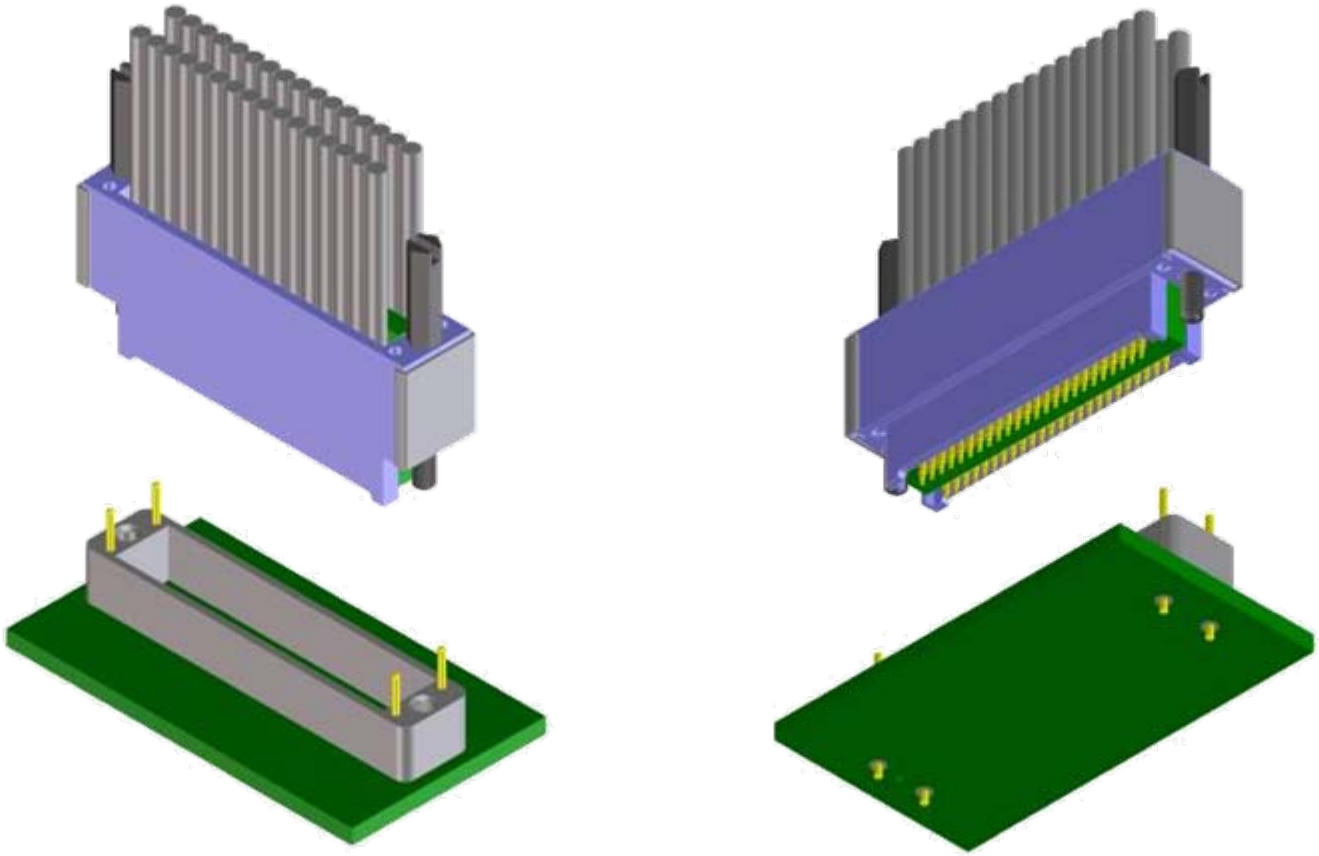
Midbus Probe



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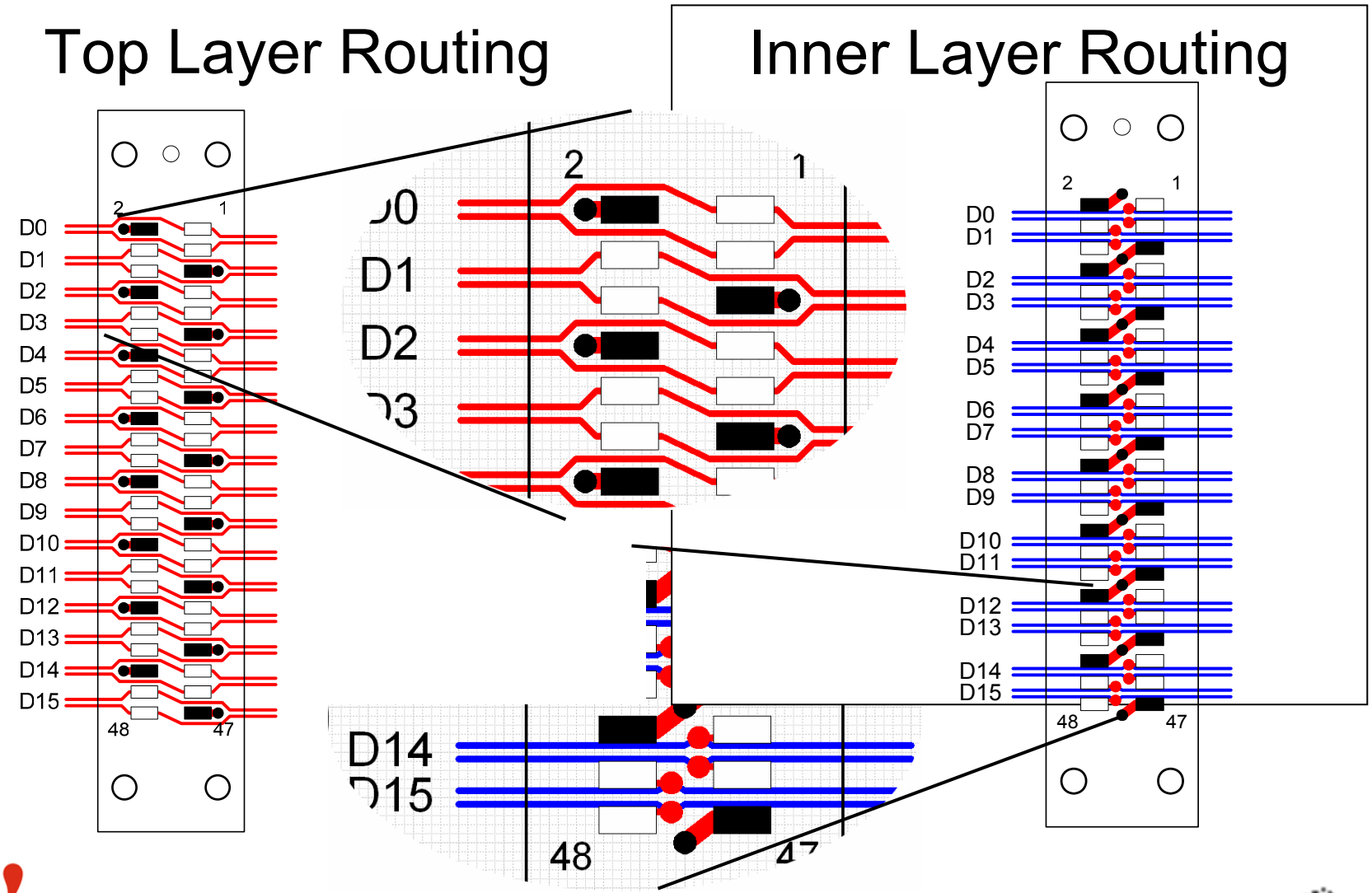
Mid-Bus Footprint Routing



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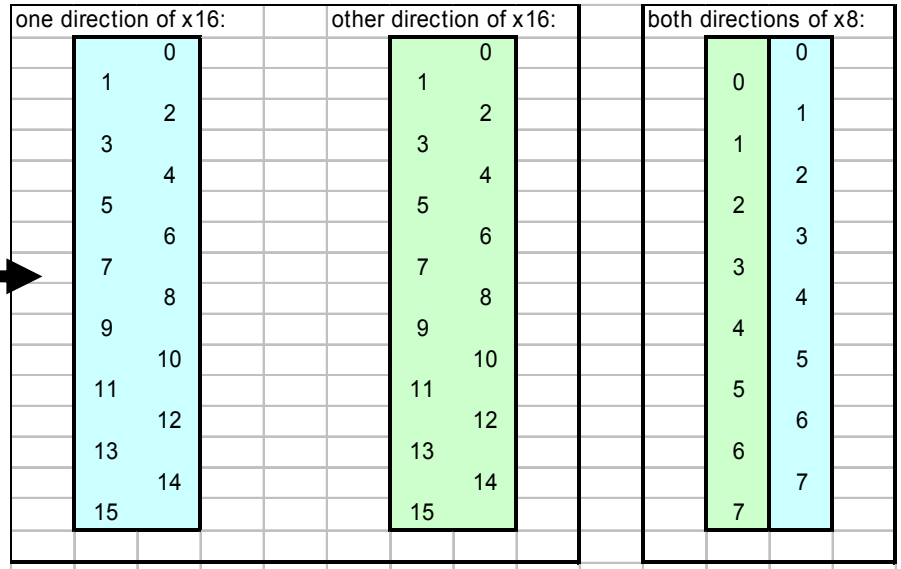
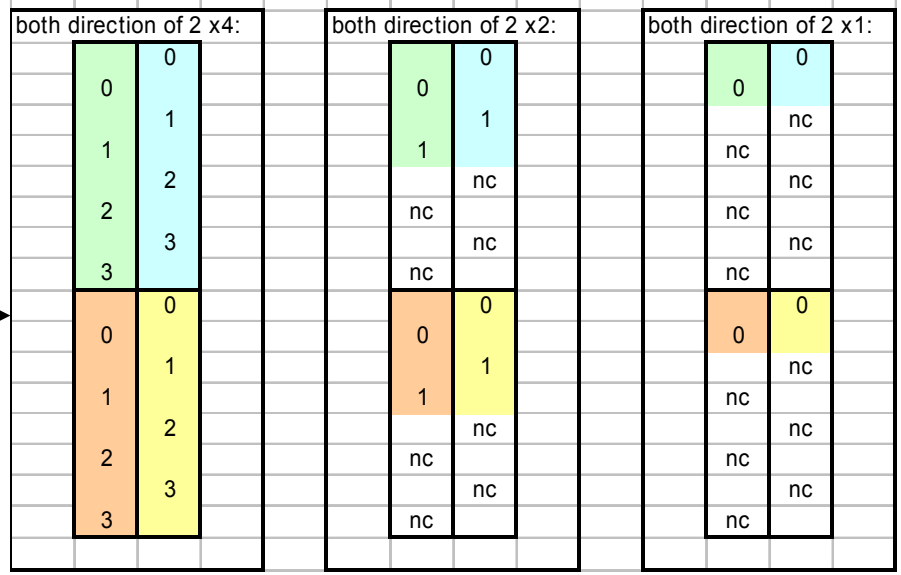
Mid-Bus Connector Layout

Additional x16 Layouts Supported



Additional Layouts Supported



- **Signal Pair Polarity can be reversed**
- **Entire Link Lane assignment can be reversed**

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Connect: Flying Lead Set

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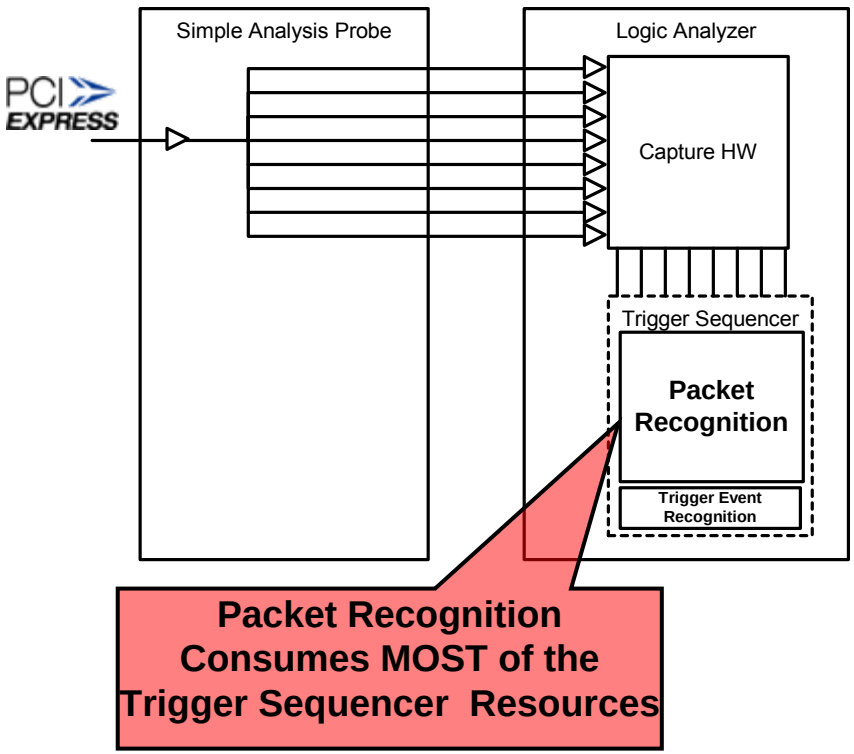
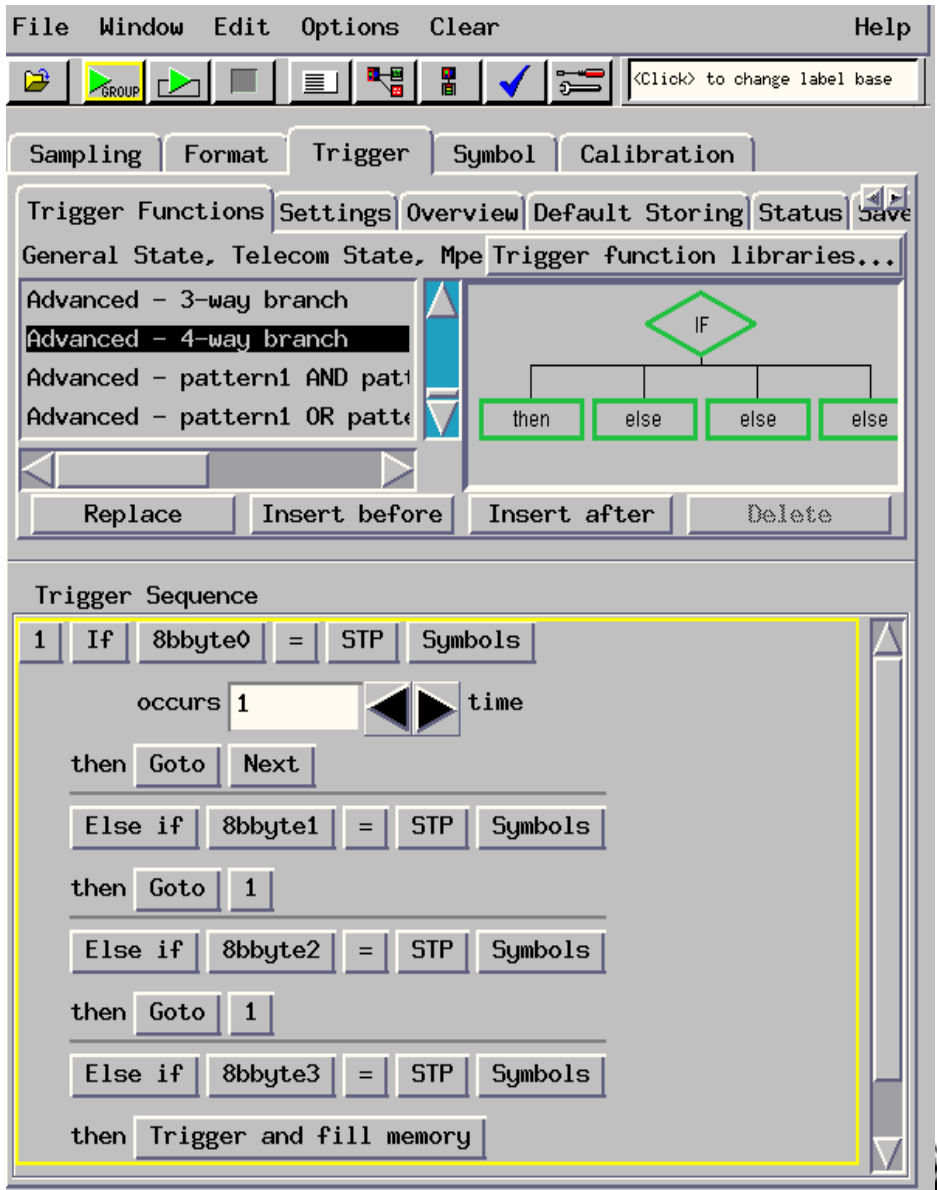
Logic Analysis
PCI Express Validation Steps

Acquire: PCI Express Traditional LA

- Traditional Serial Analysis Probes





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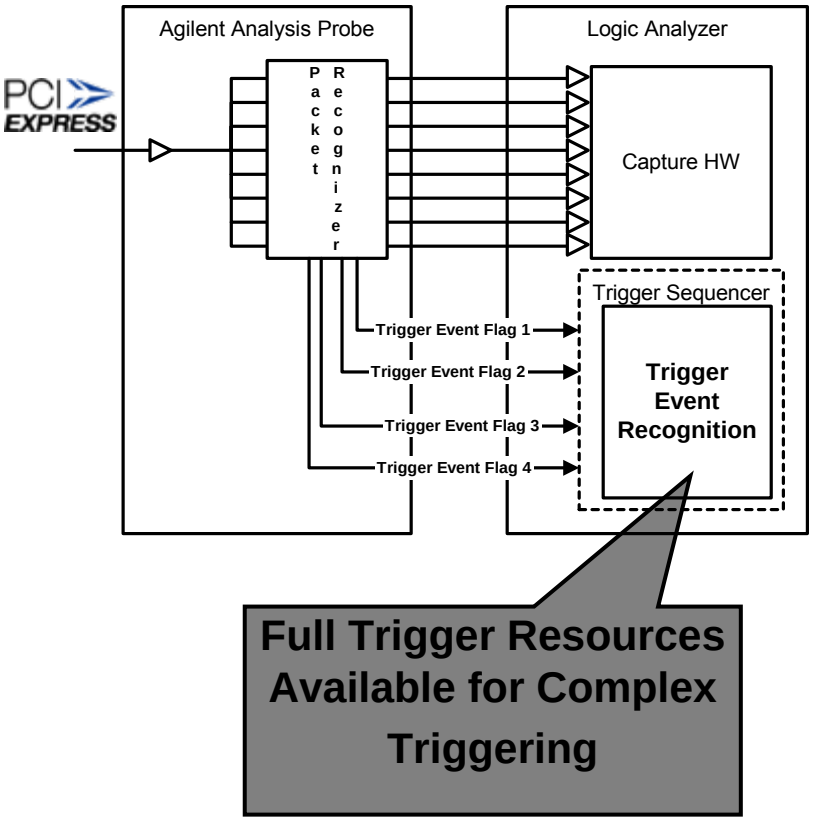
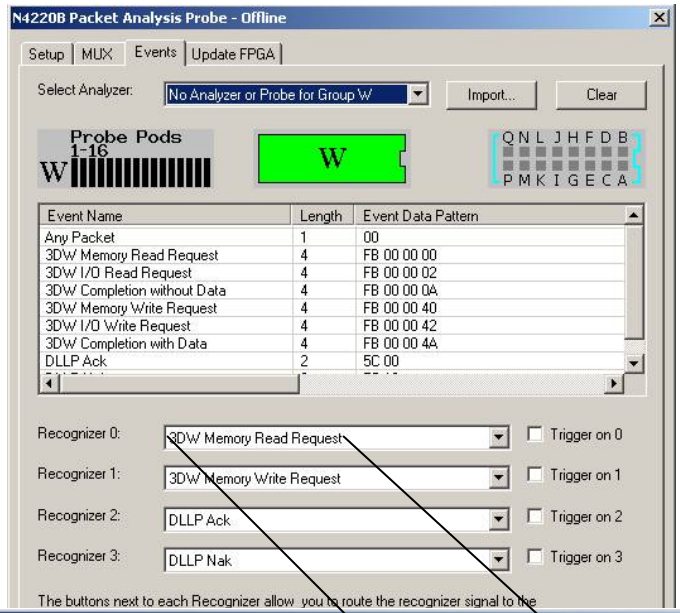
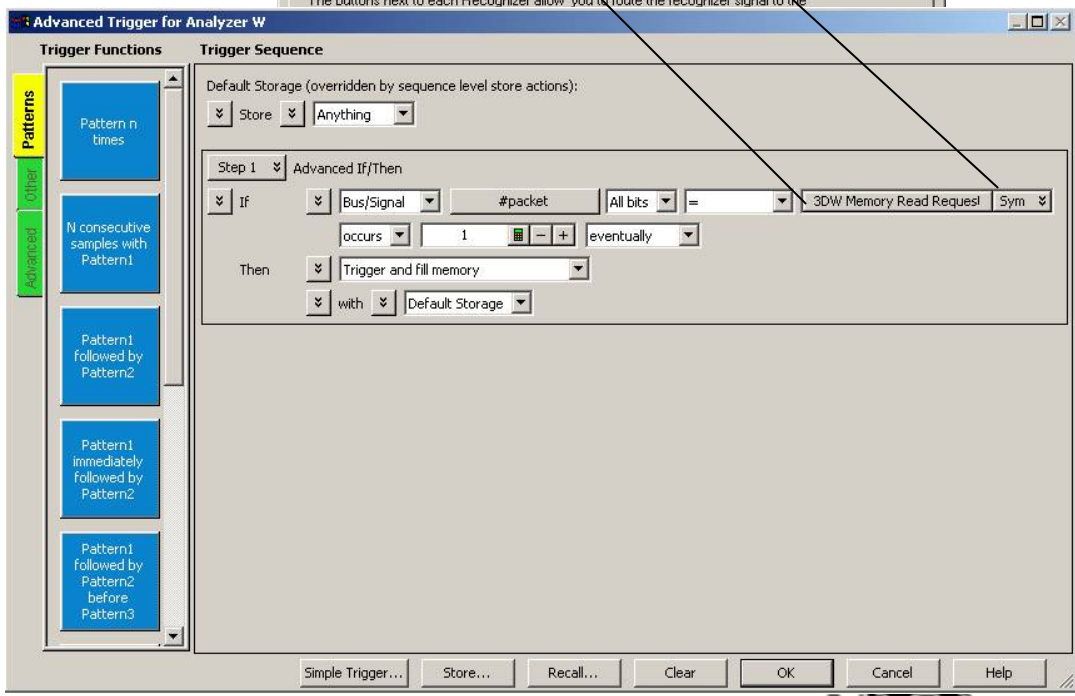
Acquire: PCI Express Packet Recognition

- PCI Express Packet Analysis Probe







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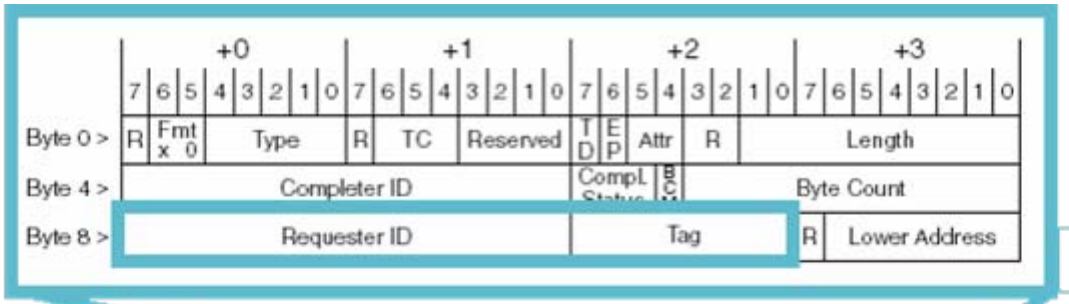
PCI Express Packet Recognition

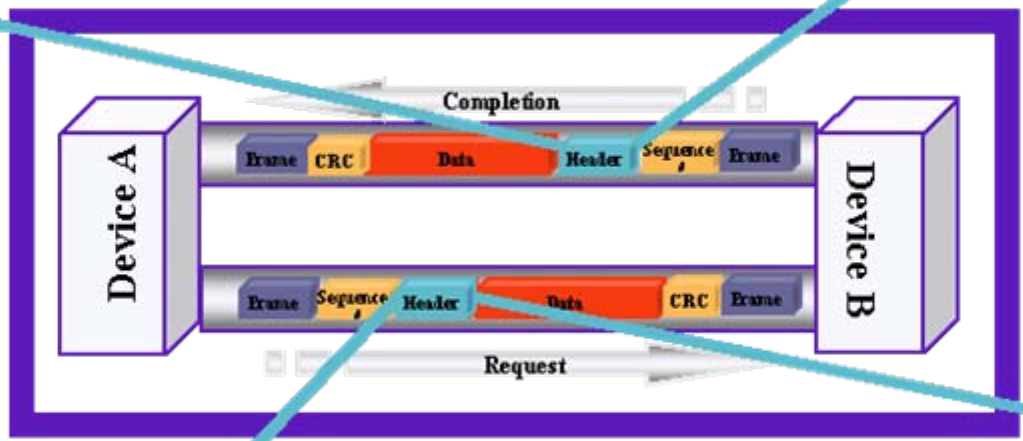
- *Enhanced Trigger Capability Through Packet Recognition*
  - 8 Header Recognizers will exist in the Analysis Probe (4 Tx/4 Rx)
    - Implemented in h/w, includes GUI
      - 24 Bytes in each Header Recognizer (Recognition into Data Portion)
      - Recognizers send simple event notification back to Logic Analyzer
  - Full, Robust Logic Analyzer Sequencing will be available on event notification bits.

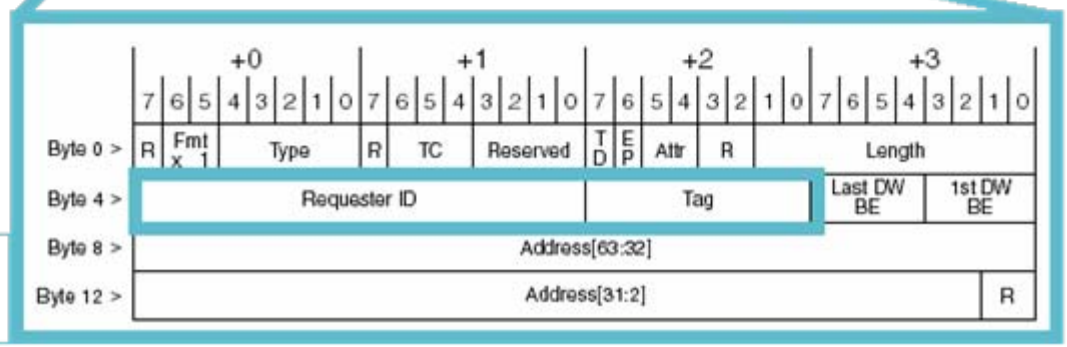
Logic layer Validation Challenges

“Read” & “Write” Cycles replaced by Packets



Completion Header Format





Requester Header Format
For 64-bit addressing of memory

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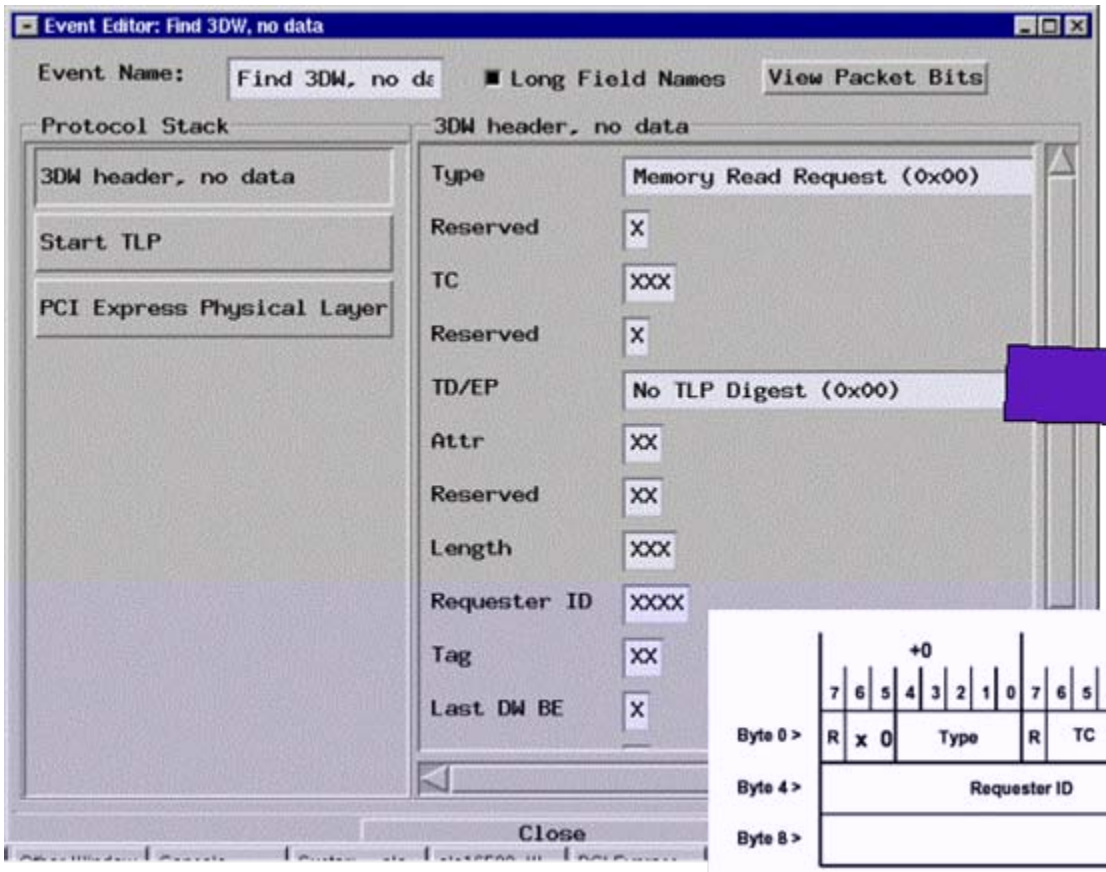
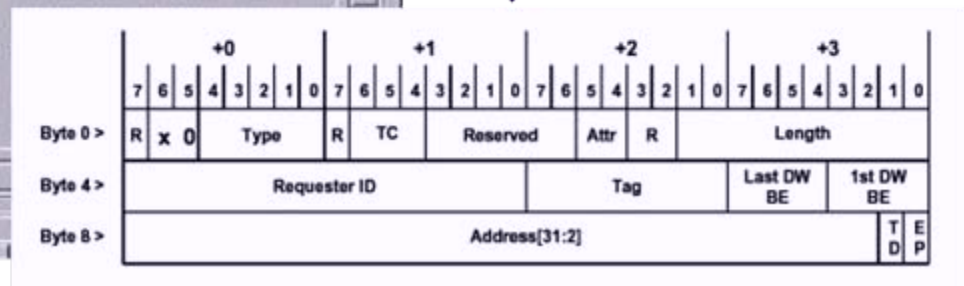
Validation Steps

Defining a Packet



Describe your trigger At Packet Level

Analyzer handles bit order, 10B/8B, scrambling, etc.



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Logic Analysis
PCI Express Validation Steps

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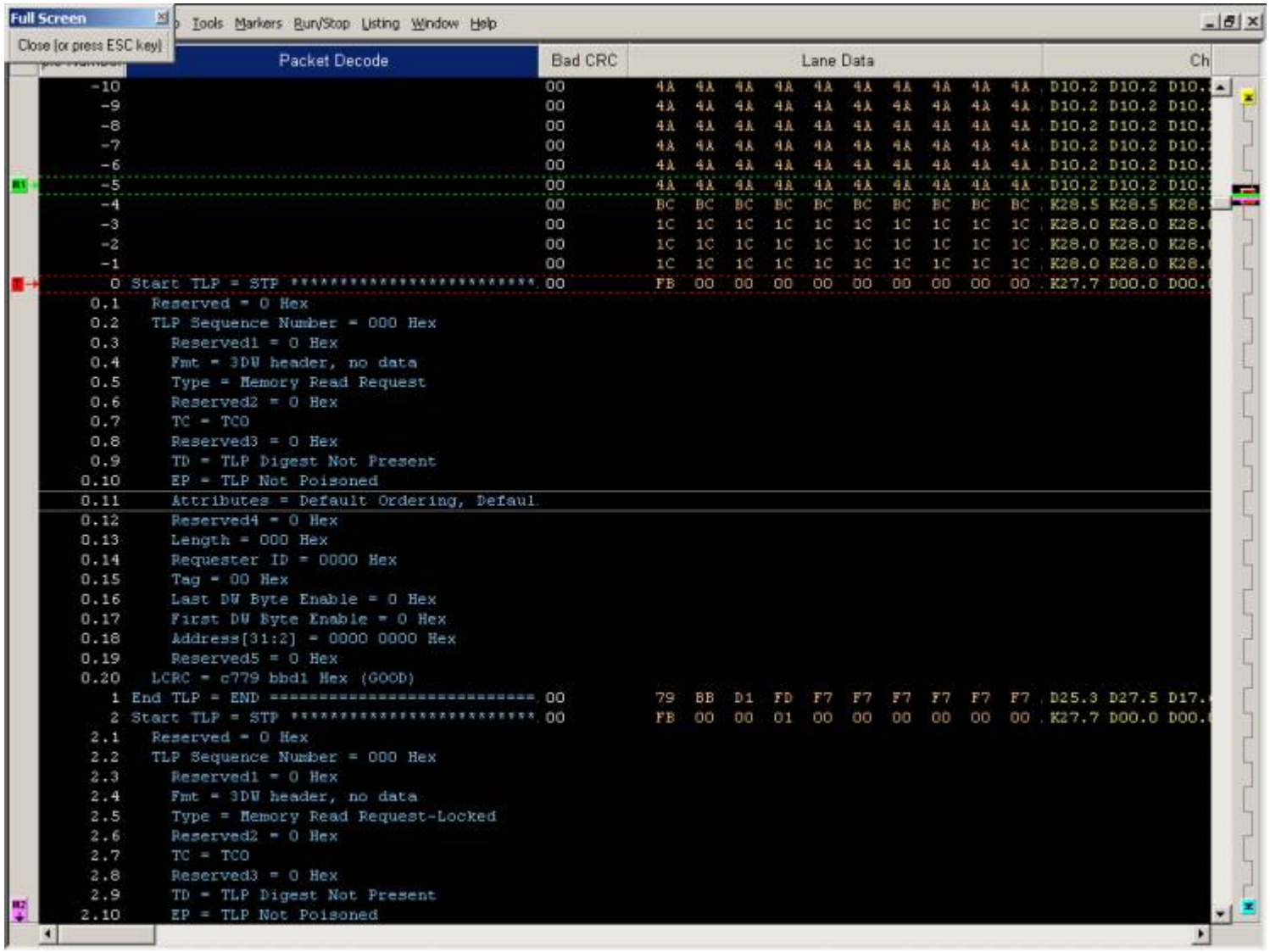
Display: Packet Decode



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Packet Decode / Display (TLP)

K/D	Time	Packet Decode	Data0	Data1	Data2
Binary	Absolute	Text	Hex	Hex	Hex
1000	0 s	Start TLP	FB	00	00
		Reserved = 00 Hex			
		Packet Sequence Number = 00 Hex			
		Reserved = 0 Binary			
		Global Format = 00 Binary (3DW header, no data)			
		Type = 04 Hex (Configuration Read Type 0)			
0000	20.000 ns	Reserved = 0 Binary	00	00	00
		TC = 000 Binary			
		Reserved = 00 Hex			
		Attr = 00 Binary			
		Reserved = 00 Binary			
		Length = 000 Hex			
		Requester ID = 0000 Hex			
0000	40.000 ns	Tag = 00 Hex	00	00	00
		Last DW BE = 0 Hex			
		First DW BE = 0 Hex			
		Bus Number = 00 Hex			
0000	60.000 ns	Device Number = 00 Hex	00	00	00
		Function Number = 0 Hex			
		Reserved = 0 Hex			
		Ext. Reg Address = 0 Hex			
		Register Address = 00 Hex			
		TLP Digest = 0 Binary			
		EP = 0 Binary			
		32b CRC: 0x00000000			
0001	80.000 ns	End	00	00	00
1000	100.000 ns	Start TLP	FB	00	00

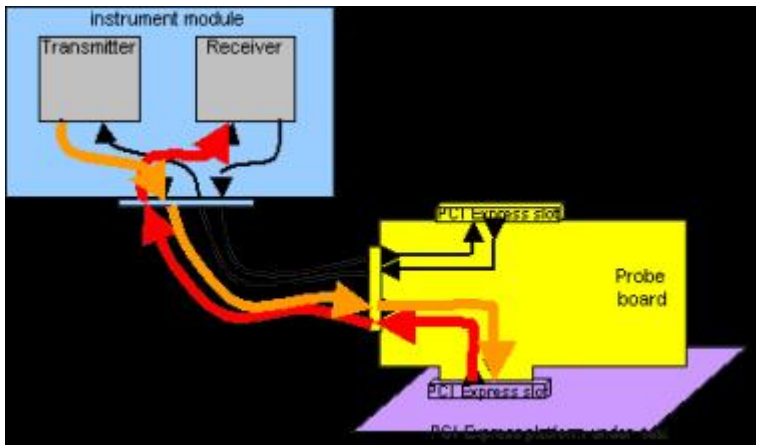
Packet Decode / Display (DLLP)

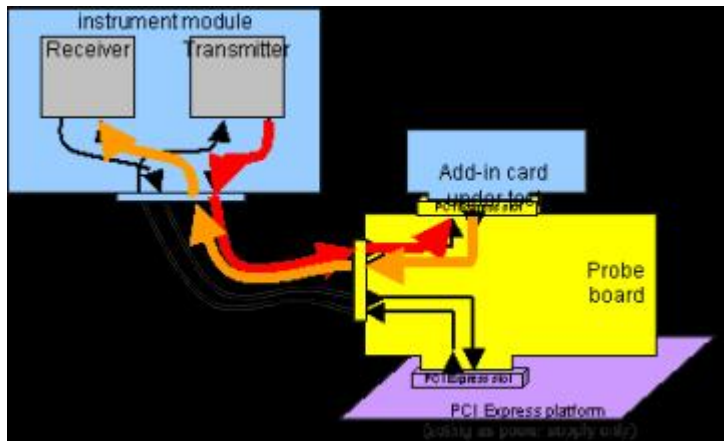
K/D Binary	Time Absolute	Packet Decode Text	Data0 Hex	Data1 Hex	Data2 Hex
1000	10.340 us	Start DLLP	5C	10	00
		Type = 1 Hex (Nak)			
		Must be zero = 0 Hex			
		Reserved = 00 Hex			
		Reserved = 00 Hex			
0001	10.360 us	End	01	00	00
		AckNak_Seq_Num = 01 Hex			
		16b CRC: 0x0000			
1000	10.380 us	Start DLLP	5C	20	00
		Type = 2 Hex (PM)			
		PM = 0 Hex (PM_Enter_L1)			
		Reserved = 00 Hex			
		Reserved = 00 Hex			
0001	10.400 us	End	00	00	00
		Reserved = 00 Hex			
		16b CRC: 0x0000			
1000	10.420 us	Start DLLP	5C	21	00
		Type = 2 Hex (PM)			
		PM = 1 Hex (PM_Enter_L2)			
		Reserved = 00 Hex			
		Reserved = 00 Hex			
0001	10.440 us	End	00	00	00
		Reserved = 00 Hex			
		16b CRC: 0x0000			
1000	10.460 us	Start DLLP	5C	22	00
		Type = 2 Hex (PM)			
		PM = 2 Hex (PM_Active_State_Request_L0s)			

Protocol Verification Challenges

Protocol Variations / Maximum Load

- Maintain system stability over different configurations
  - What happens if the link is fully populated with packets?
  - Does my system still work if an add-in card is inserted that implements the protocol differently?
  - How can I tell if my design is protocol compliant?





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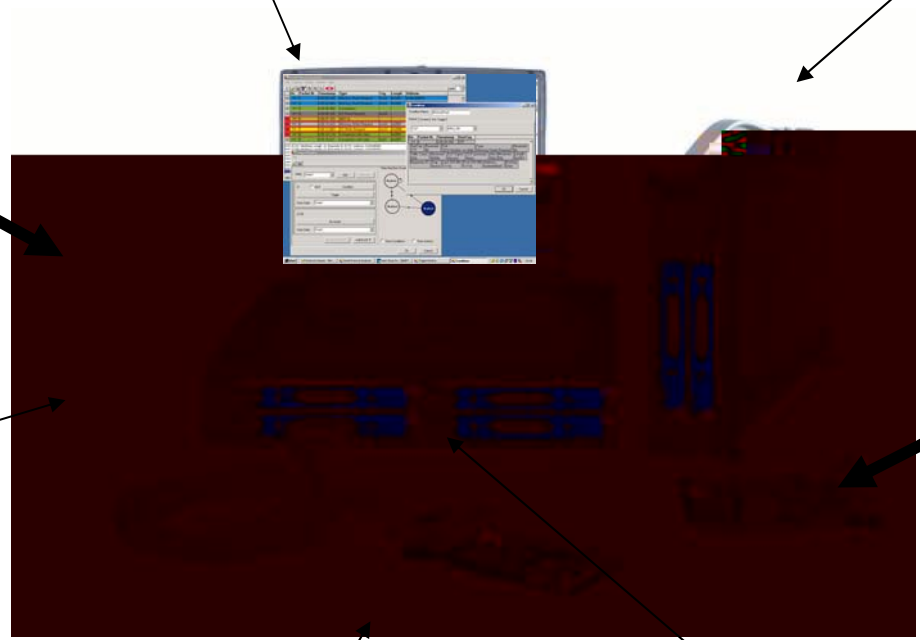
Serial Protocol Tester and Protocol Test Card



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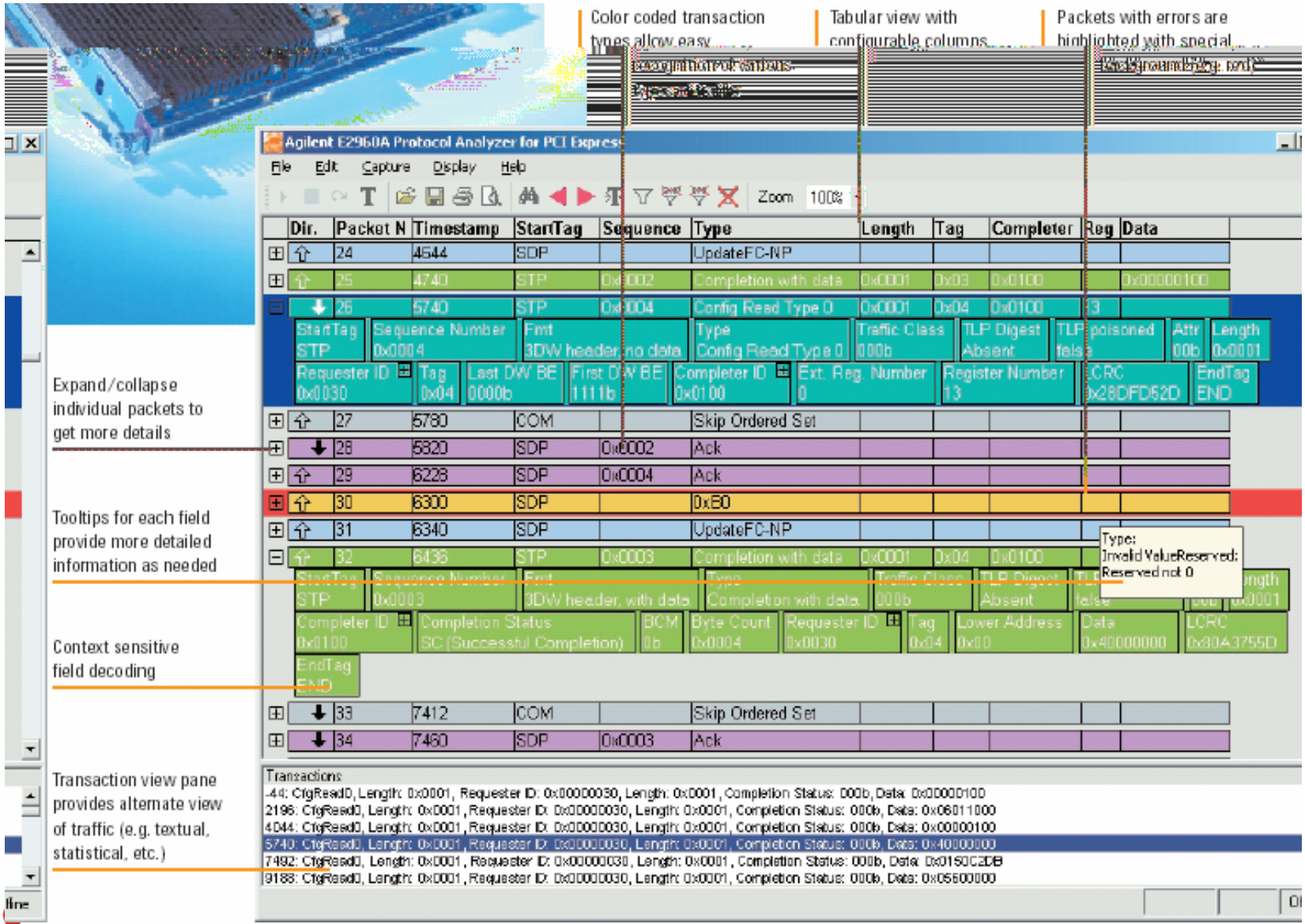
GUI Protocol Analyzer



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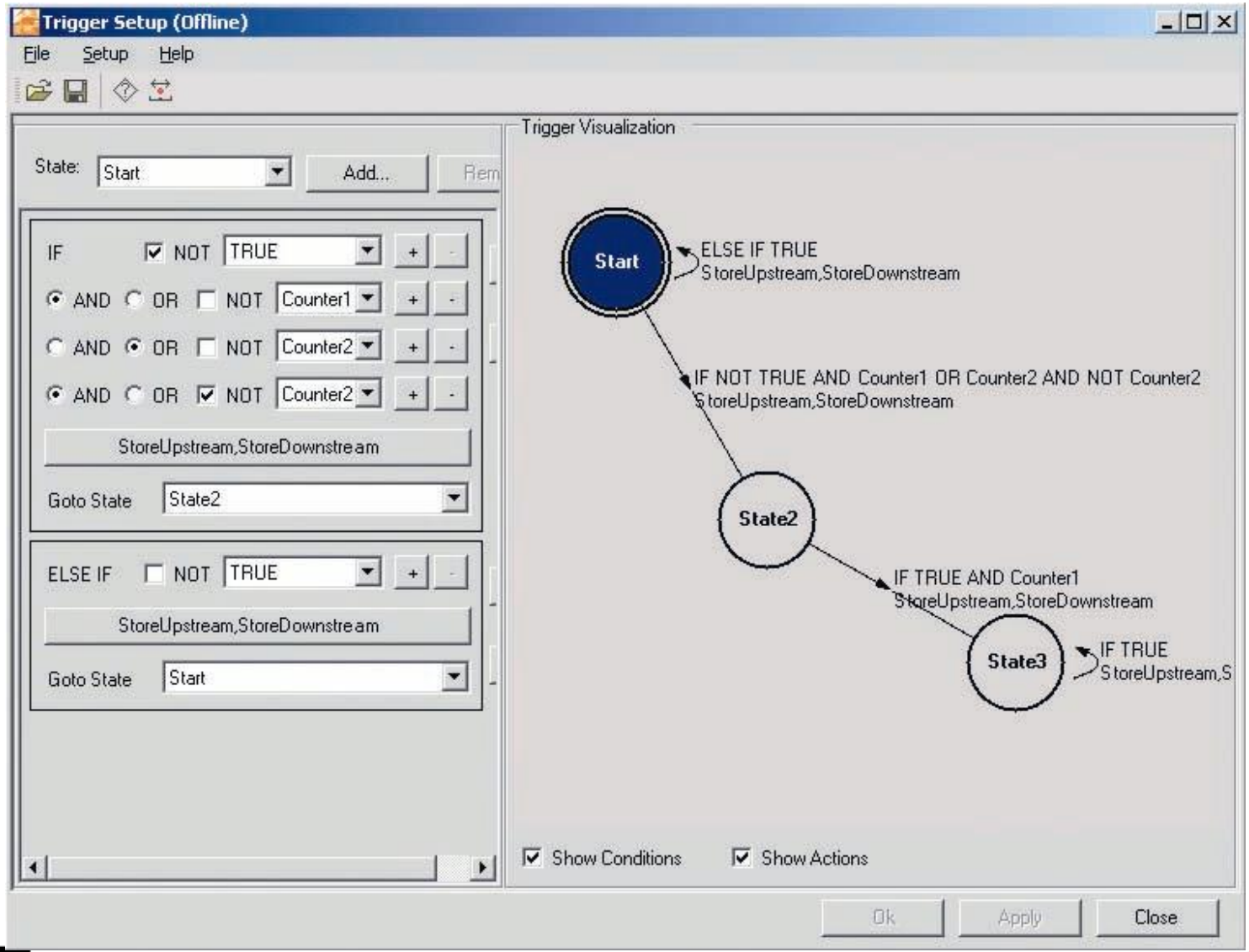
Protocol Analyzer Trigger Setup



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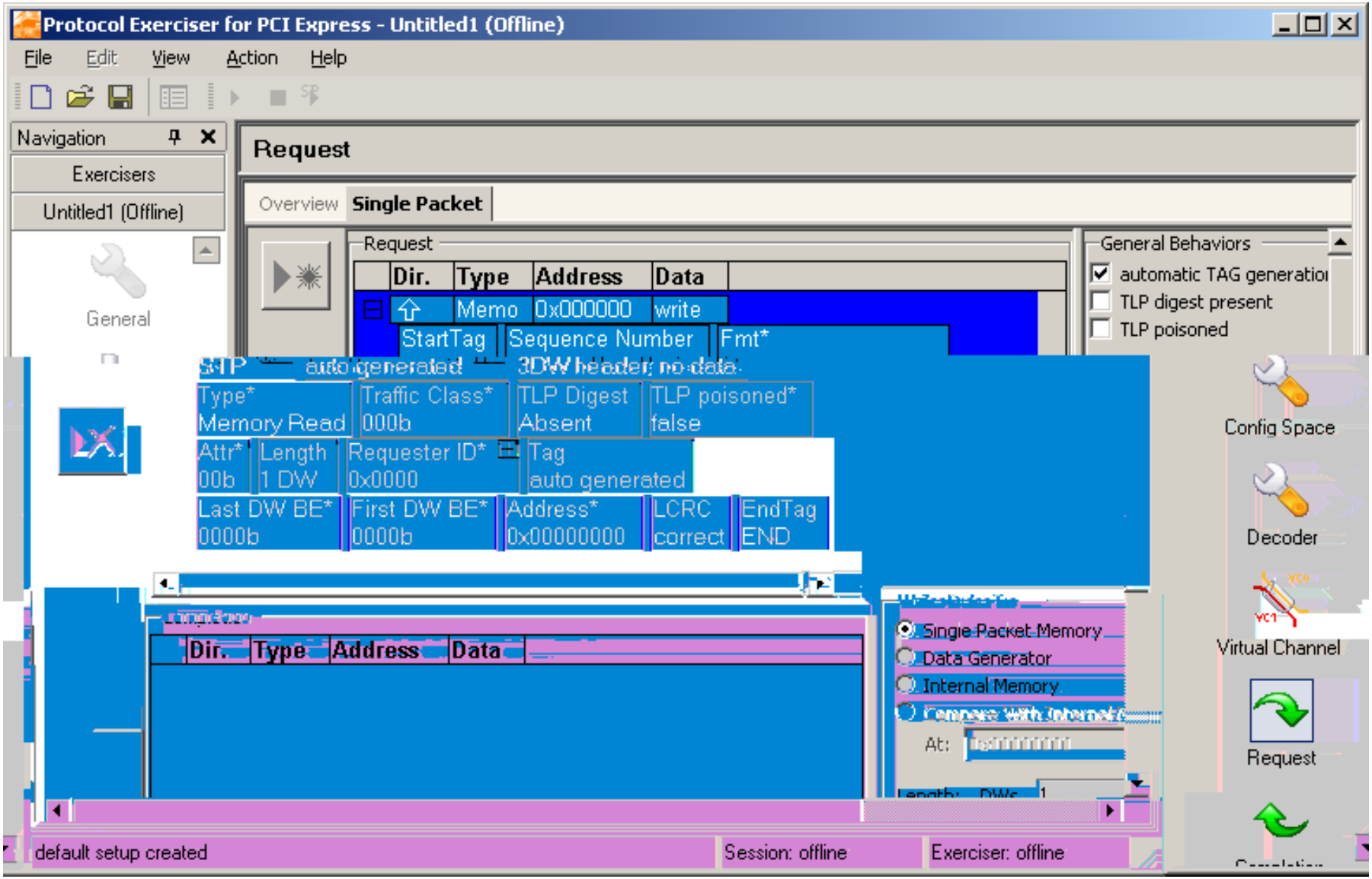
Exerciser GUI



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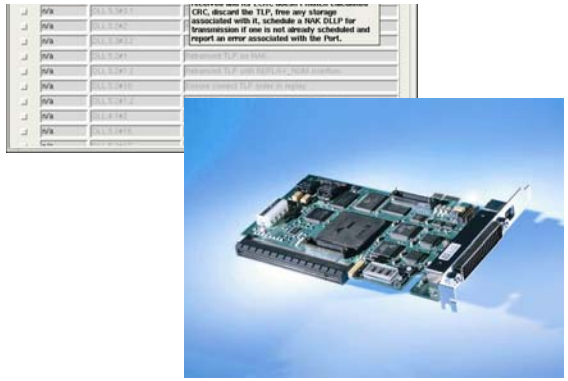
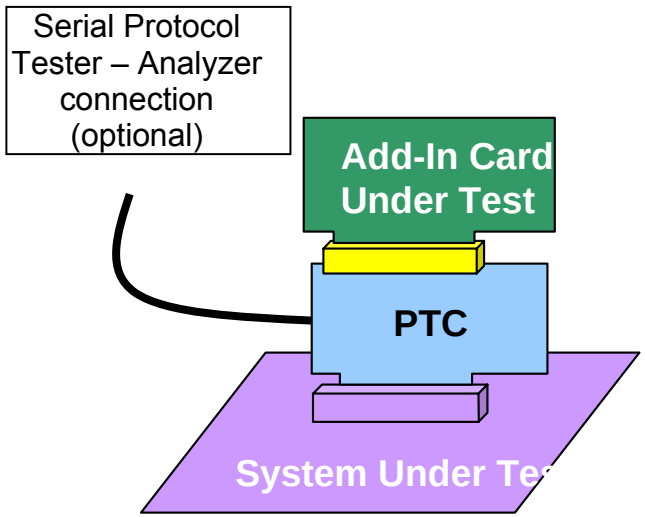
Protocol Test Card for PCI Express Compliance Testing



Collaboration and joint development with Intel

- **Cost-effective compliance solution**
- **Easy-to-use**
  - **GUI/push-button solution**
  - **Pre-programmed tests**
    No programming effort
  - **Pass/Failed report**
- **Improves design quality, compliance and accelerates time to market**



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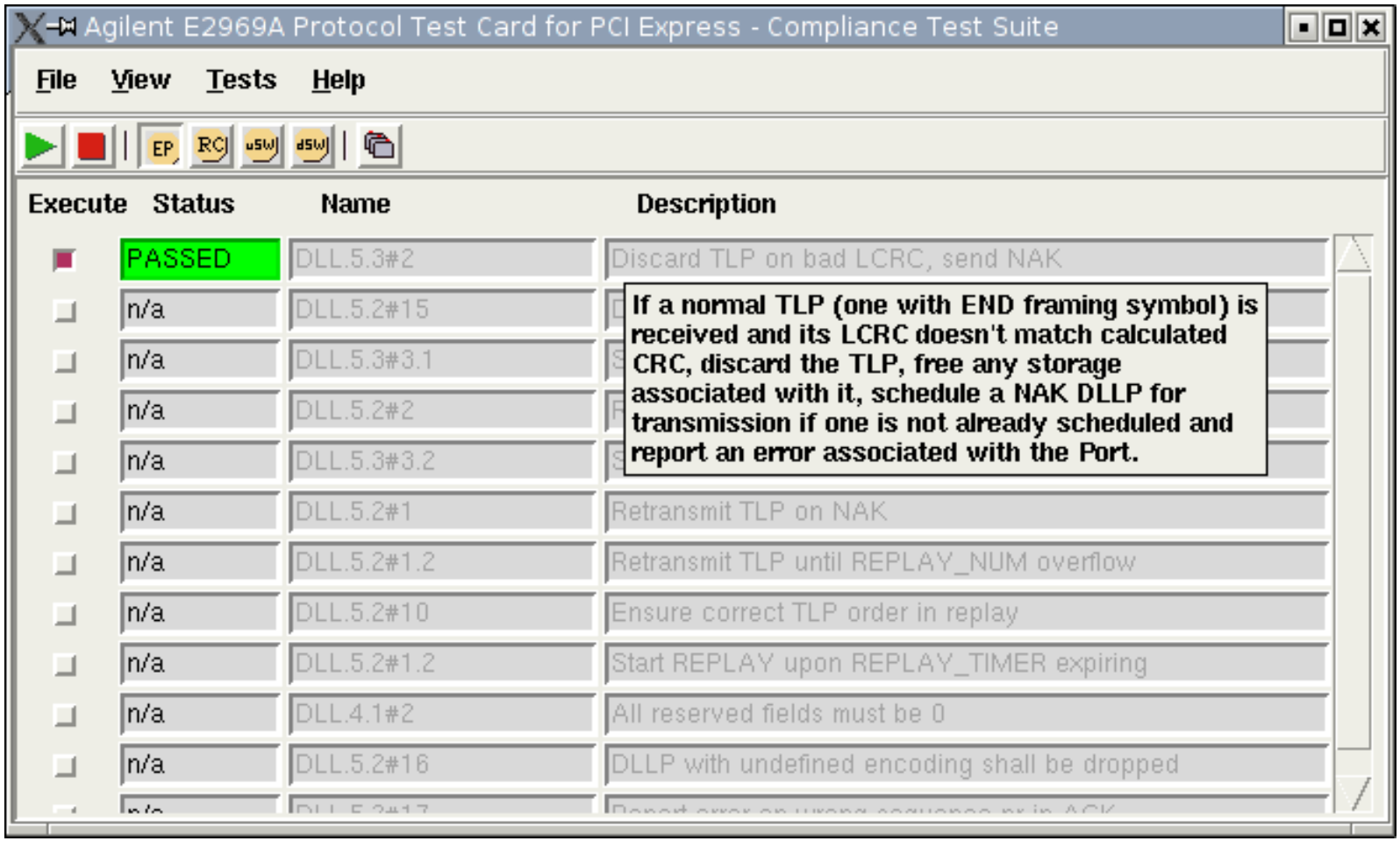
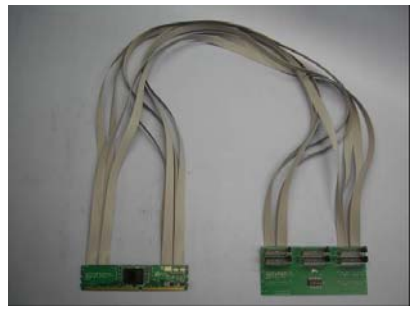
PTC GUI – main view

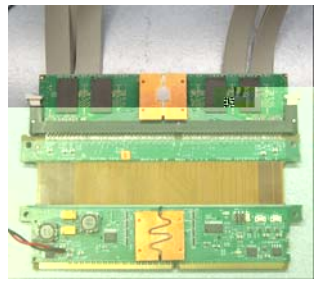


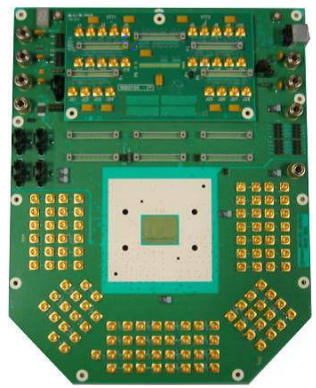
Fully Buffered DIMM Overview

PHY and Logic Probing Overview

Rohit Bhasin
Senior Technical Sales Engineer
Digital Verification and Design Validation Solutions
Agilent Technologies







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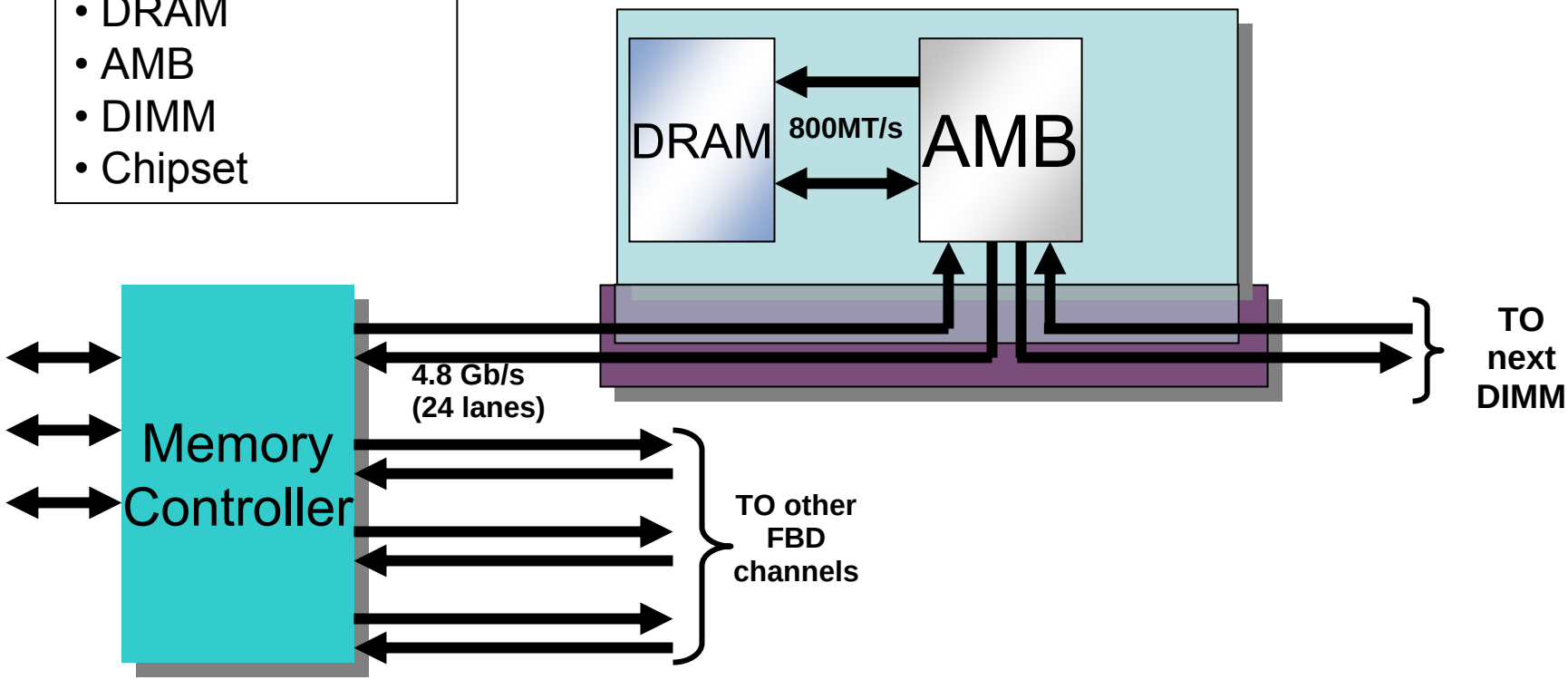
What is Fully Buffered DIMM?

People doing FBD:
- DRAM
- AMB
- DIMM
- Chipset

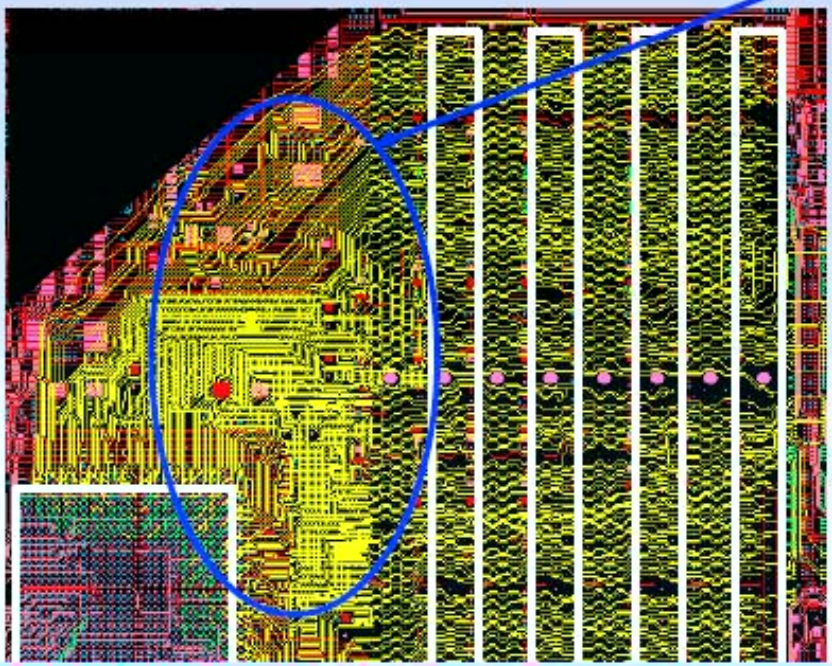


FSB, PCI-X, PCI-E, SATA, etc.

DRAM IO [Mb/s]	533	667	800	1.066	1.333	1.600
AMB IO [Gb/s]	3.2	4.0	4.8	6.4	8.0	9.6

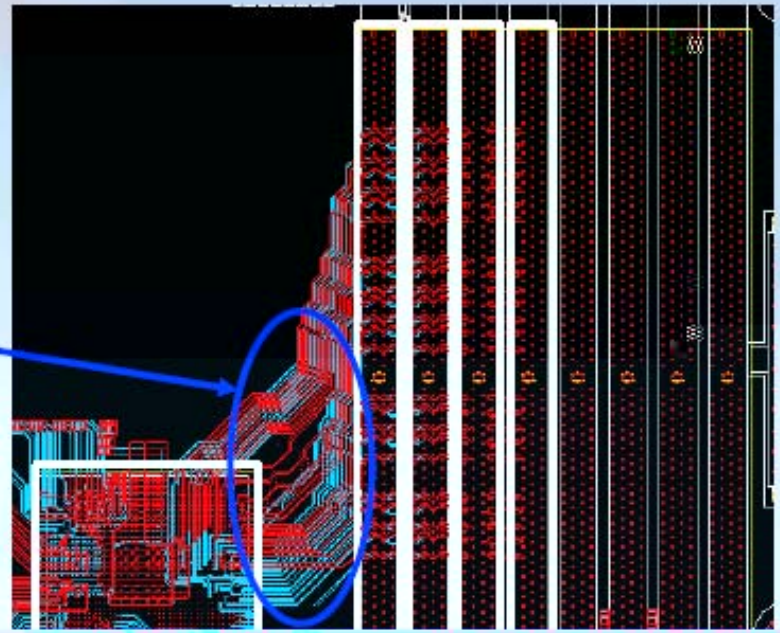
Routing Comparison

Direct DDR2 Registered DIMMs:
1 Channel, 2 Routing Layers with 3rd layer required for power



Serpentine routing is complicated and uses up a lot of board area

FB-DIMMs:
2 Channels, 2 Routing Layers (*includes* power delivery)



Fewer signals and no trace length matching minimizes board area

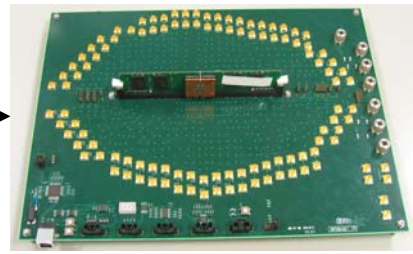
FB-DIMM: Fewer Layers, Less Routing Area

FBD Measurement Points and Validation Components

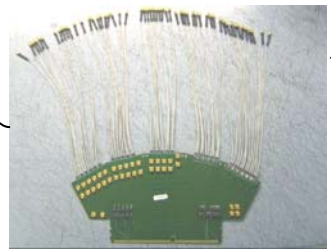
BERT

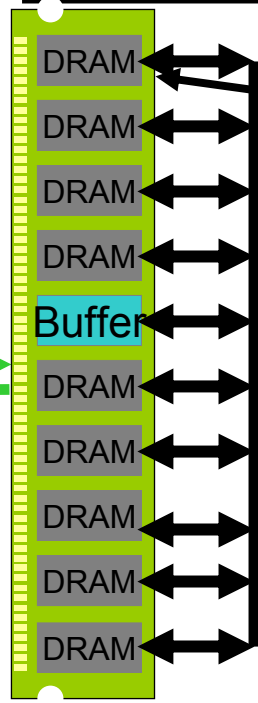
13Ghz 40Gs/s Real Time Scope

AMB/DIMM Parametric Fixtures

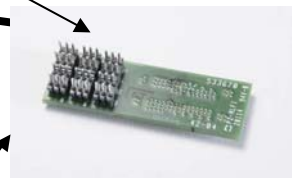


DIMM Slot Parametric Probe





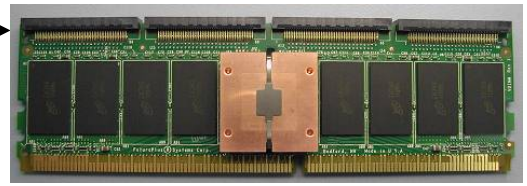
OEM DIMM
DDR Write Data
Addr/Cmd



DRAM OEM
DIMM Probe

Host

Memory channel

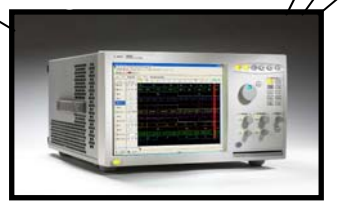


Validation DIMM (RC/B)

Slot

Interposer

Channel Protocol Probes



Logic Analyzer

OEM DIMM Probing
of DDR Address /
Command Bus

Addr/Cmd
OEM DIMM
Probe

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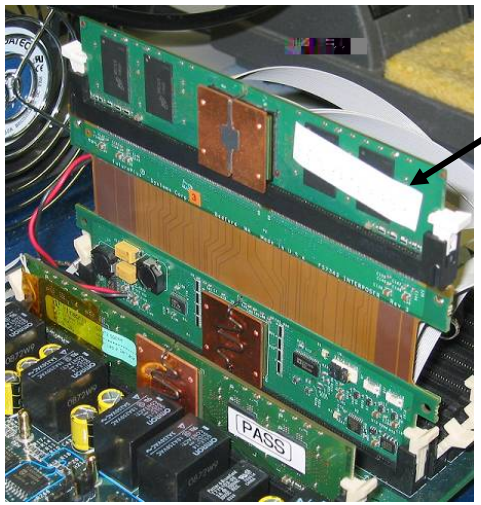
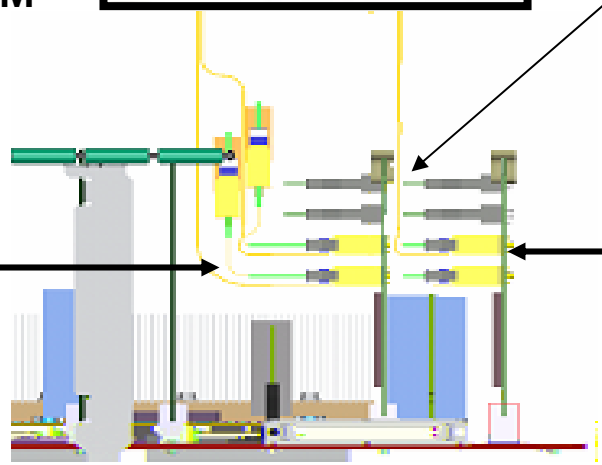
High Speed Channel Probes

Interposer Probe allows all DIMM slots to be populated



FB-DIMM



Slot Probe fits anywhere a Jedec DIMM will fit and works in systems with suspect timing

Interposer Channel Probe

- Does not consume a slot
- Adjustable orientation of interposed DIMM for maximum installation flexibility
- Supports probing of 2 channels in adjacent slots
- Full SB/NB protocol analysis

Slot Channel Probe

- Same size as standard FB DIMM to fit in crowded systems
- High Speed channel layout identical to standard DIMM for operation in marginal systems
- Full SB/NB protocol analysis

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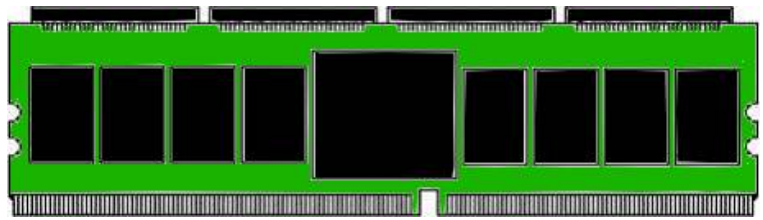
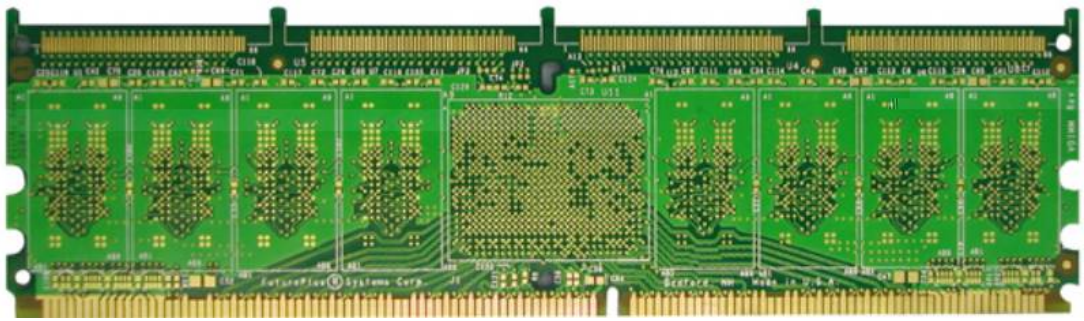
Complete Pre-AMB Probing

Logic Analyzer Probing for Instrumented DIMMs

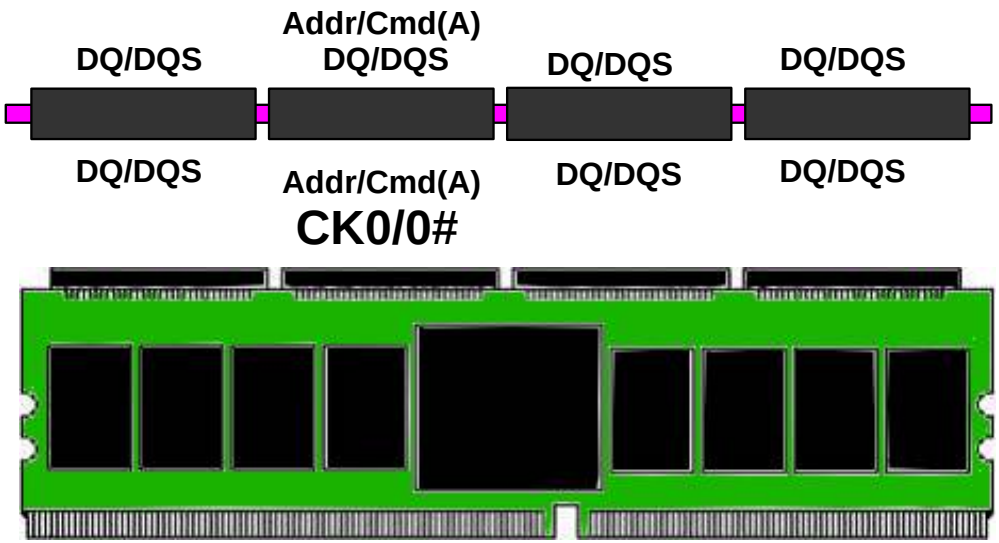
- RC/B Validation DIMM
  - Fast connection to all post-register signals (Addr/Cmd/DQ)
  - Support to DDR800+ Speeds
  - Supports all Jedec AMBs and x8 DRAMS
  - RC/A,C,D,G,H,I support planned if demand warrants





Validation DIMM (Pre-AMB)

- Functional and signal integrity validation of addr/cmd and data
- Adds 2 layers to DIMM reference design for embedded probing resistors to eliminate stub loading from for routing to logic analysis connectors.
- Validation DIMM for each raw card type
- Straddle mount connector topology minimizes loading and allows probing of adjacent slots and system with limited vertical clearance.
- Supports all DDR2 DRAMs and AMB components



Signals	Count
CK0/CK0#	1
Addr/Cmd	28
DQ	72
DQS	18
DQS#	17
TOTAL	136

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VDIMM Configuration (Pre-AMB)

Customer Supplied

Test Vendor Supplied

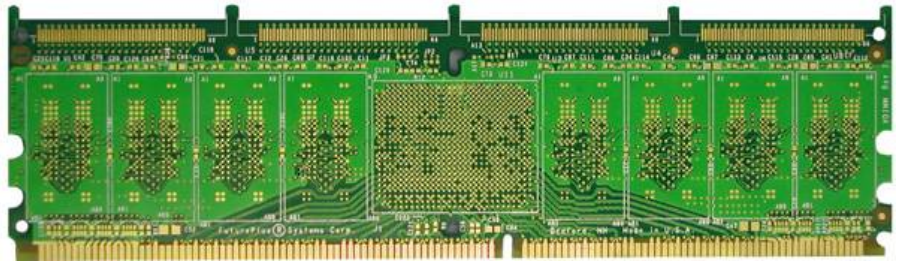
DRAMs

SPD EEPROM

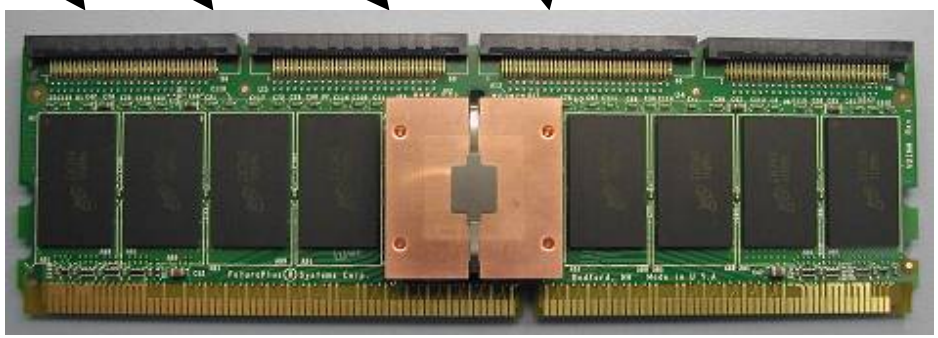
AMB

Straddle Mount Samtec

Validation DIMM Raw Card



Customer Assembles VDIMM



Assembled VDIMM with custom combination of AMB and DRAM

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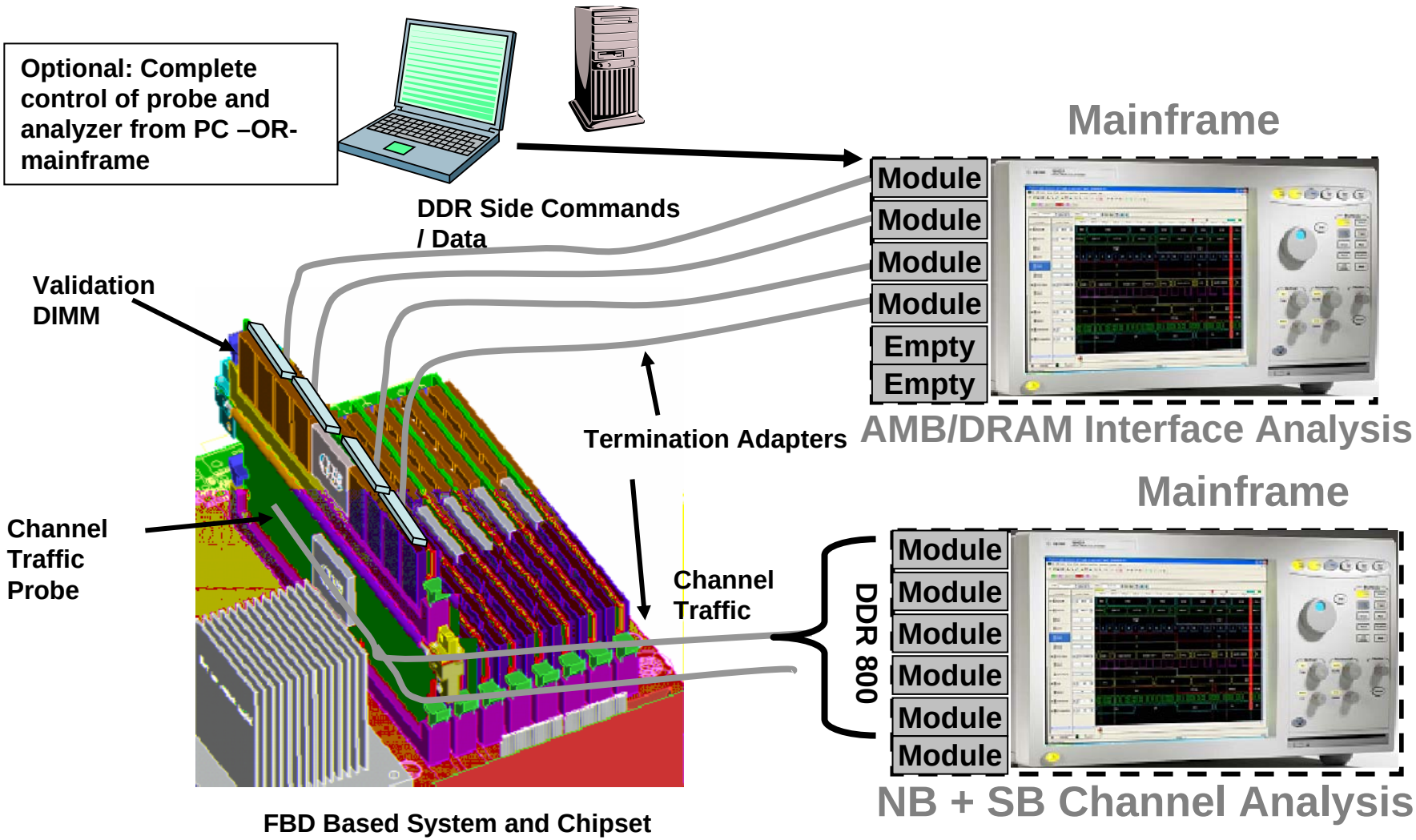
Looking at Channel & AMB/DRAM traffic concurrently



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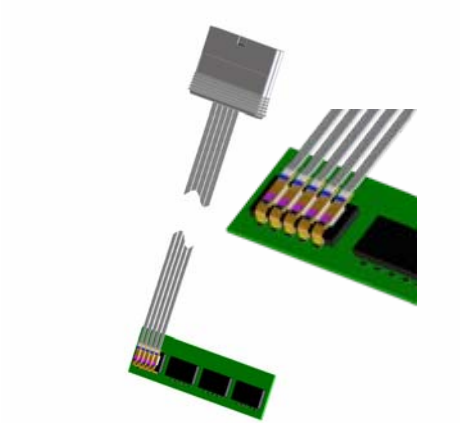
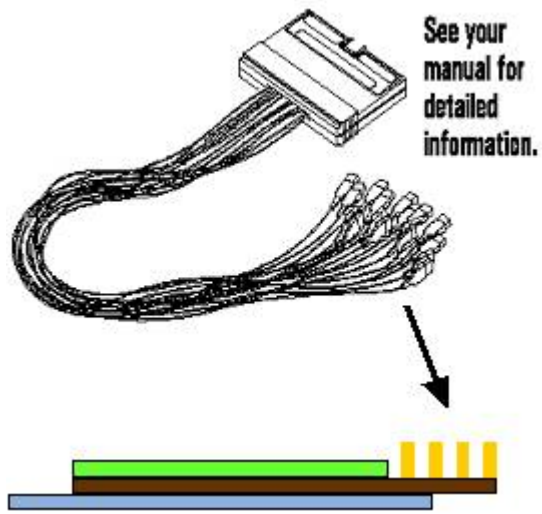
Complete Post-AMB Probing

Logic Analyzer Probing for OEM DIMMS

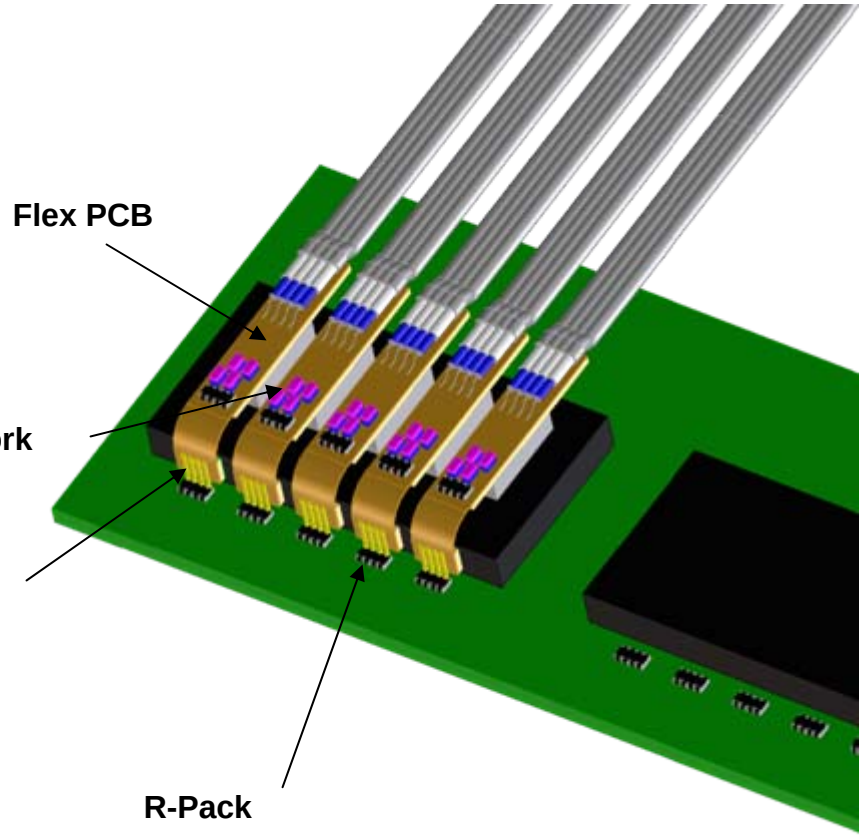
- RPACK Probe
  - Probing of FBD Addr/Cmd Bus to DDR1067
  - Supports all FBD Raw Cards
  - Supports DDR1/DDR2 DIMM and SODIMM



- DDR2 Probe
  - Probes DDR2 BGA packages
  - DQ/DQS/CK for x4 and x8 DDR2 DRAMs
  - Supports all FBD Raw Cards
  - Supports DIMM, SODIMM and embedded DDR2
  - Scope probing may be possible



OEM DIMM Probe (RPACK)



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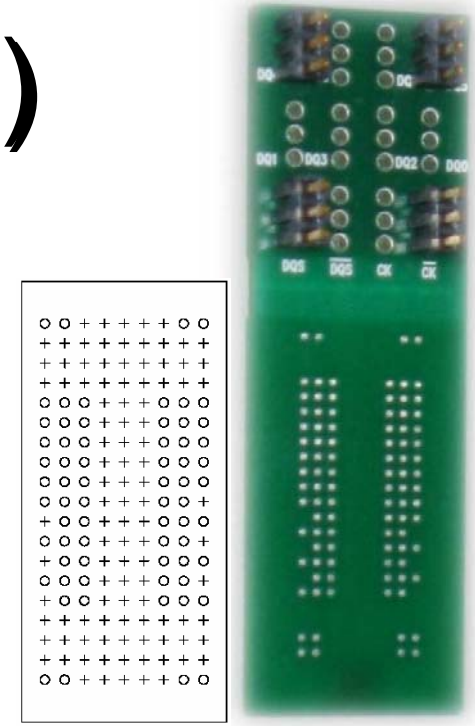
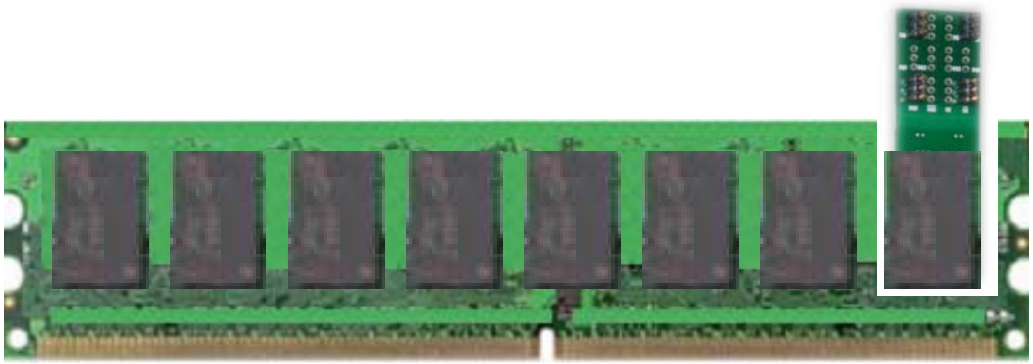
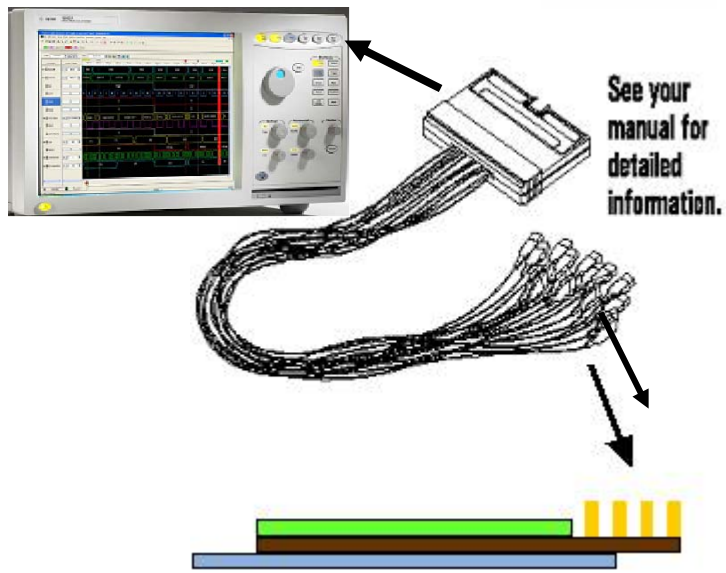
OEM DIMM Probe (DRAM)

- 0.8mm micro-BGA probe of DQ/DQS using flying lead probes
- Embedded tip resistors isolate probe from bus
- Functional and signal integrity validation (EyeScan/scope)
- Supports DDR2 common footprint (x4/x8)







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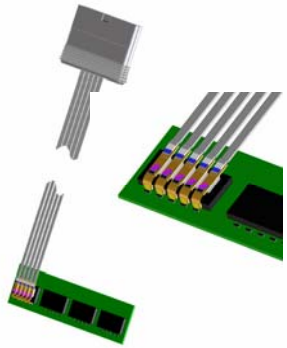
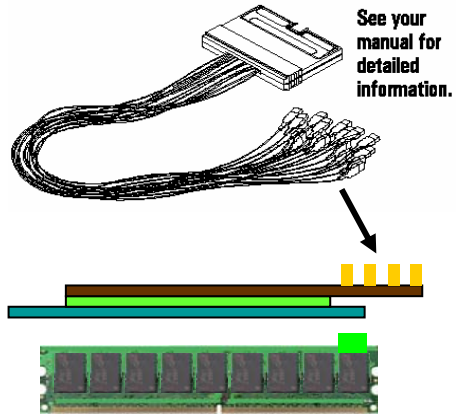
Complete Pre and Post-AMB Probing

Logic Analyzer Probing for Instrumented and OEM DIMMS





RC/B Validation DIMM

- **RC/B based - most commonly used DIMM**
- **Uses actual RC/B layout for accurate results**
- **Compact design minimizes loading**
- **Straddle mount analyzer connections for zero increase in DIMM thickness**
- **Right angle probes fits in tight server systems**

RPACK Probe

- **Probing of FBD Addr/Cmd Bus to DDR1067**
- **Supports all FBD Raw Cards**
- **Supports DDR1/DDR2 DIMM and SODIMM**

DDR2 Probe

- **Probes DDR2 BGA packages**
- **DQ/DQS/CK for x4 and x8 DDR2 DRAMs**
- **Supports all FBD Raw Cards**
- **Supports DIMM, SODIMM and embedded DDR2**
- **Analog scope connection with high bandwidth probes**

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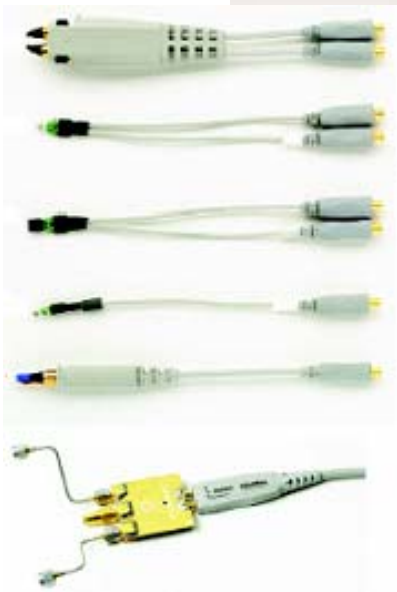
FBD Requires Bandwidth



- **Recommended - 13 Ghz Real Time Scope with very high bandwidth probes or FBD parametric fixtures provide bandwidth required for 4.8Gb FBD measurements**

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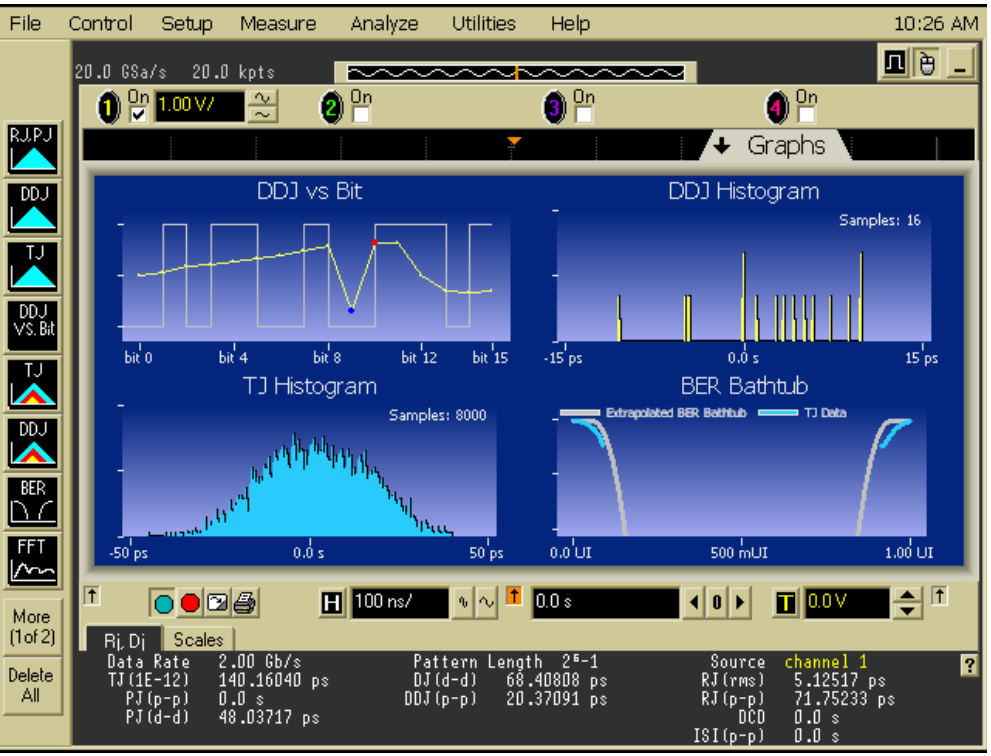
Comprehensive Data Analysis



- Complete Jitter Analysis
  - **RJ/DJ (ISI,DCD, Periodic jitter) separation**
  - **Jitter histograms**
  - **Spectral analysis**
  - **Traceable to individual bits**
  - **Bathtub BER analysis**
    - FBD Mask and Compliance Test
      - **Real Time Eye**
      - **Eye unfolding identifies failure pattern**
      - **Fixture control and compliance test suite integration**

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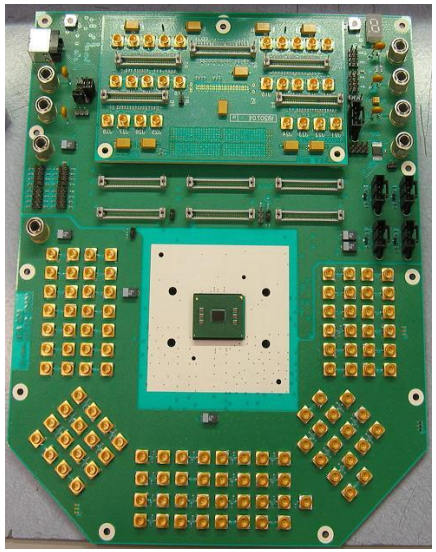
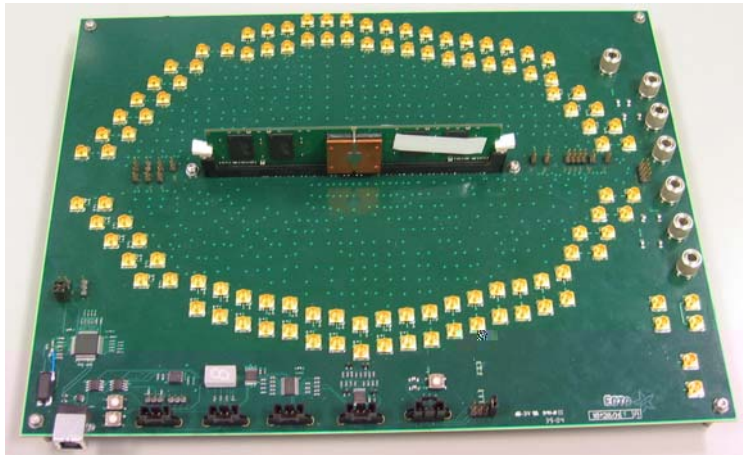
Graduated Physical Layer Parametric Test

Characterized with S-parameters for de-embedding fixture impact



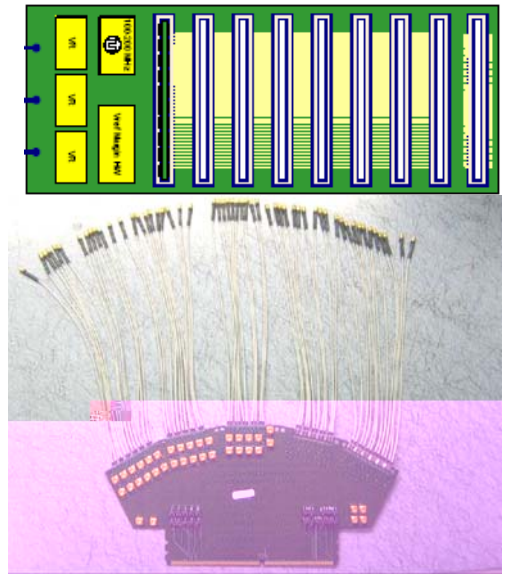
AMB Parametric Test

- AMB Die and Package focus
- Jedec Tx/Rx, BERT, Return Loss, etc.
- Package modeling



DIMM Parametric Test

- Adds DIMM and connector to test environment
- DIMM and connector impact on Channel specification
- Supports all Raw Cards
- Simplifies failure analysis



N4238A Slot Parametric Probe

- Adds MB and second connector to test environment
- System channel SI performance
- Supports any FBD channel
- Simplifies failure analysis

DVS enabling digital innovation

CTC test scripts work across all fixtures

DVU

- Anyone awake? ☺

Summary and take aways…

• Serial Links ramping up to 5-6Gb (per lane), probably higher
• Parallel signaling ramping up to 9.6Gb (e.g. FBD)

• Equipment out there to help you design any interface you want!
Scope, LA's can also be used as a general purpose debug tool
(for proprietary interfaces)

• Probing is KEY (both at PHY and logic/protocol layers, don't think you can use a conventional probe to look at multi-gigabit signaling

• Use the automated tools that are available to help you validate your interfaces (i.e. Automated mask testing on scope, predefined DDR IA's, etc)