Trends and Challenges in VLSI Technology Scaling Towards 100nm

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September 2001

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Agenda

- VLSI Technology Trends
  - Frequency and power trends
- Scaling Challenges
  - Transistor scaling
  - Interconnect scaling
  - Capacitive and inductive coupling
  - Leakage
- Summary

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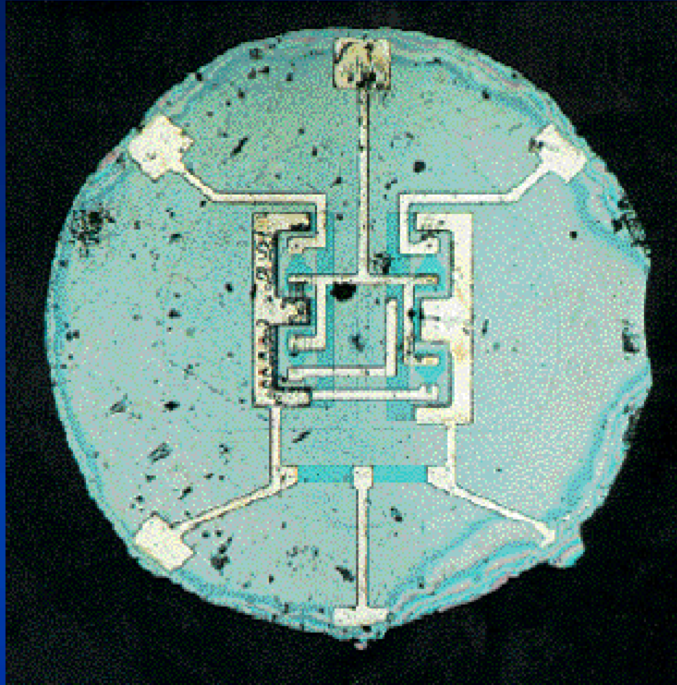
Process Technology Evolution



1961
First Planar Integrated Circuit
Two transistors

2001
Pentium® 4 Processor
42 million transistors

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Moore's Law - 1965

The experts look ahead

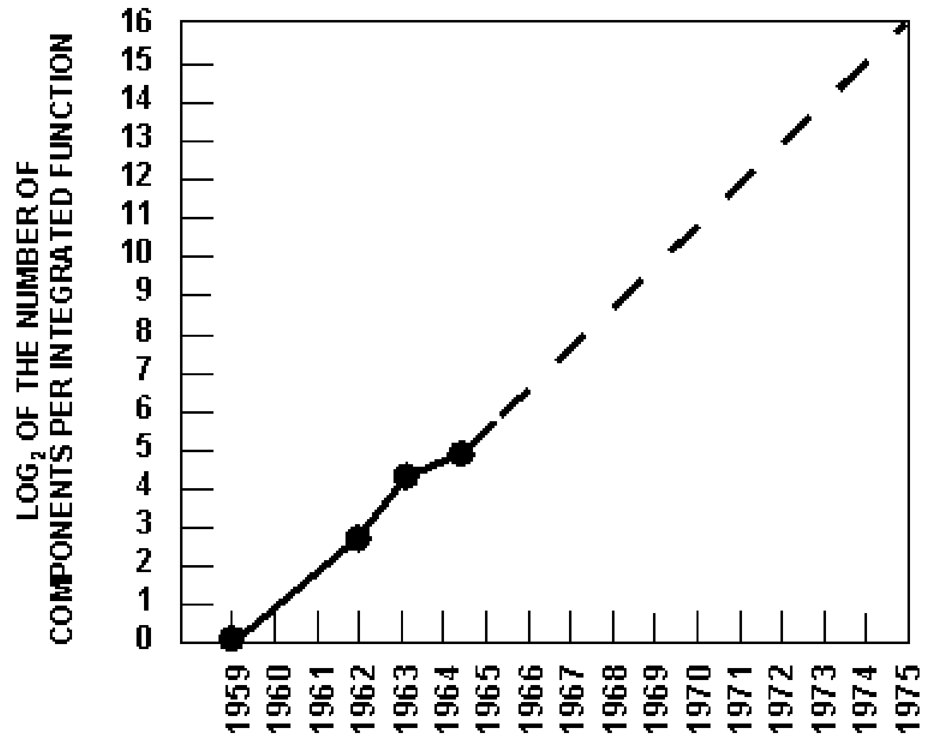
Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965



Electronics, April 1965

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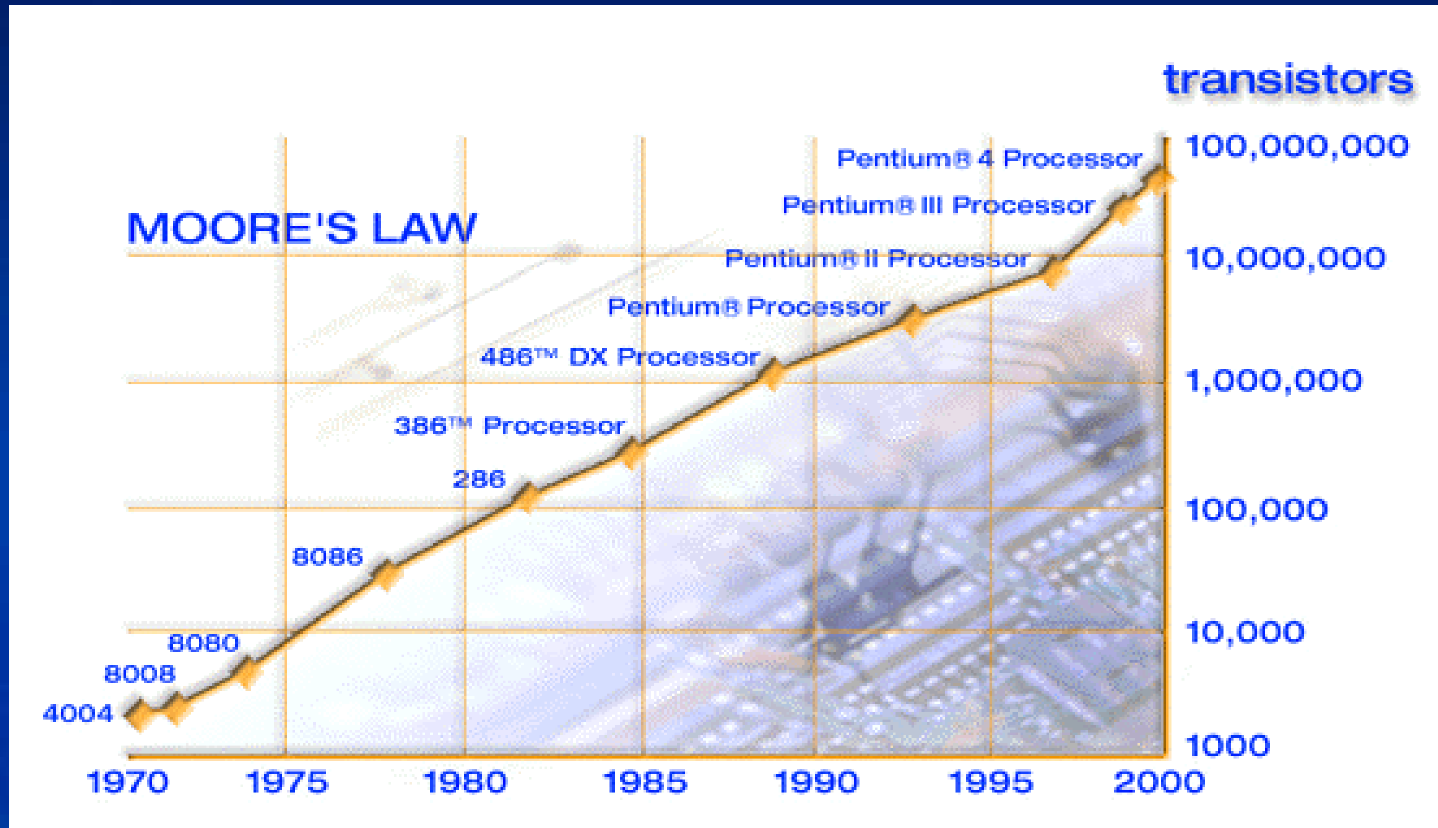
Moore's Law - Today



- Number of transistors per integrated circuit doubles every two years

SIA Technology Roadmap

Characteristic	1999	2001	2004	2008
Process Technology [nm]	180	130	90	60
Logic Transistors [mil]	23.8	47.6	135	539
Across-chip Clock Speed [MHz]	1200	1600	2000	2655
Die area [sq. mm]	340	340	390	468
Wiring Levels	6	7	8	9

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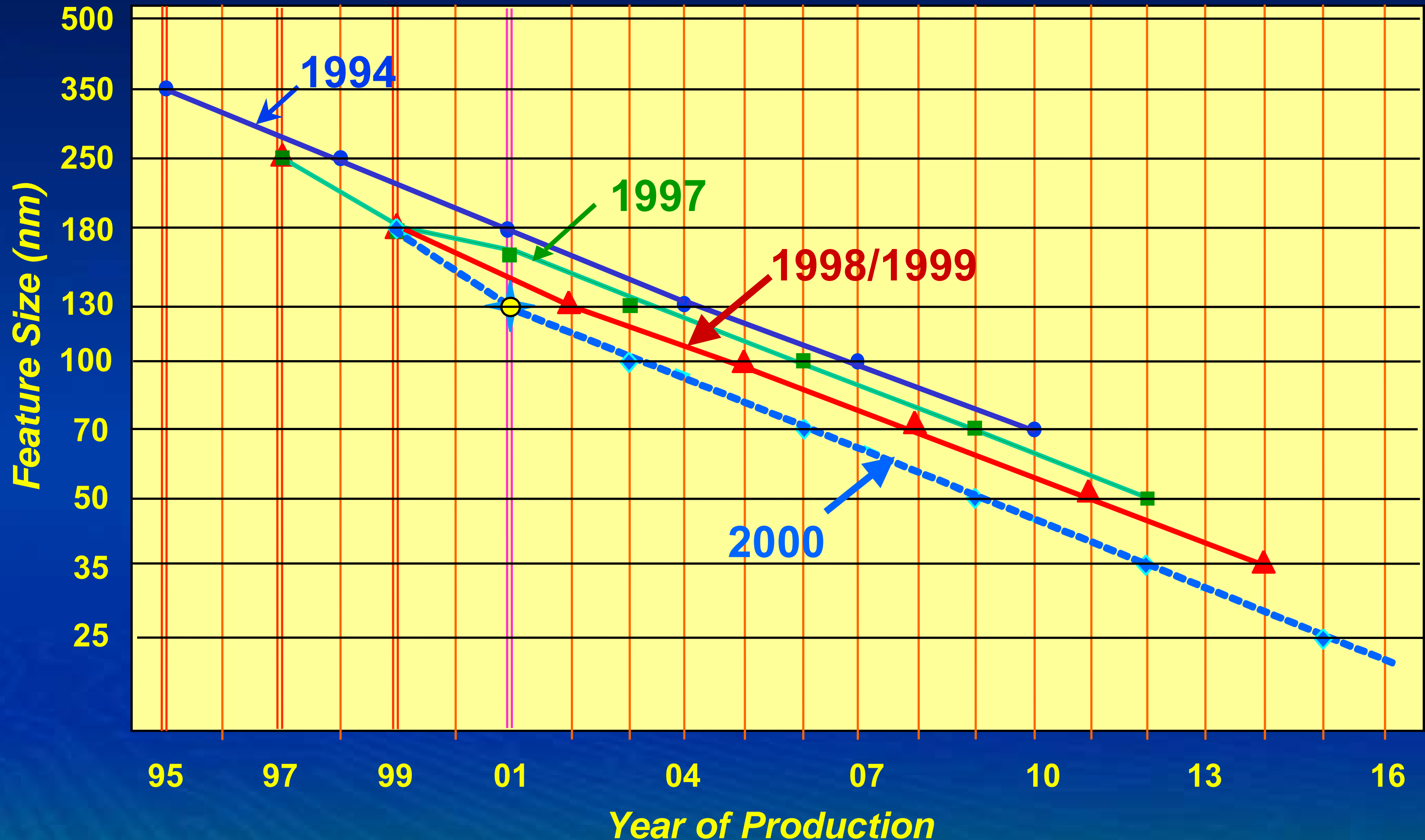
ITRS Roadmap Acceleration Continues



ITRS 2000 Update Review – December 2000

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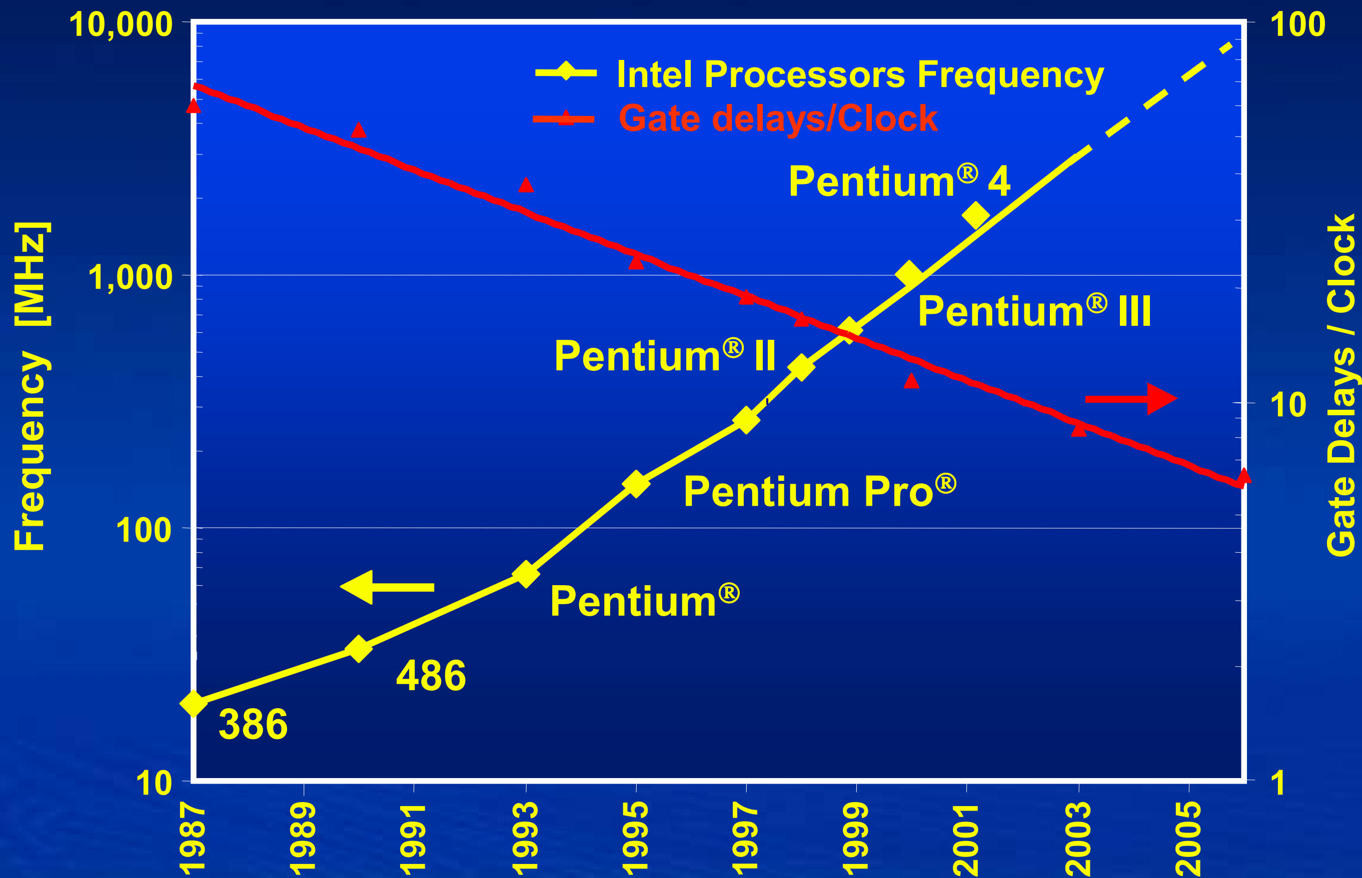
Processor Frequency Trend



- Frequency doubles each generation
- Number of gates per clock reduces by 25%

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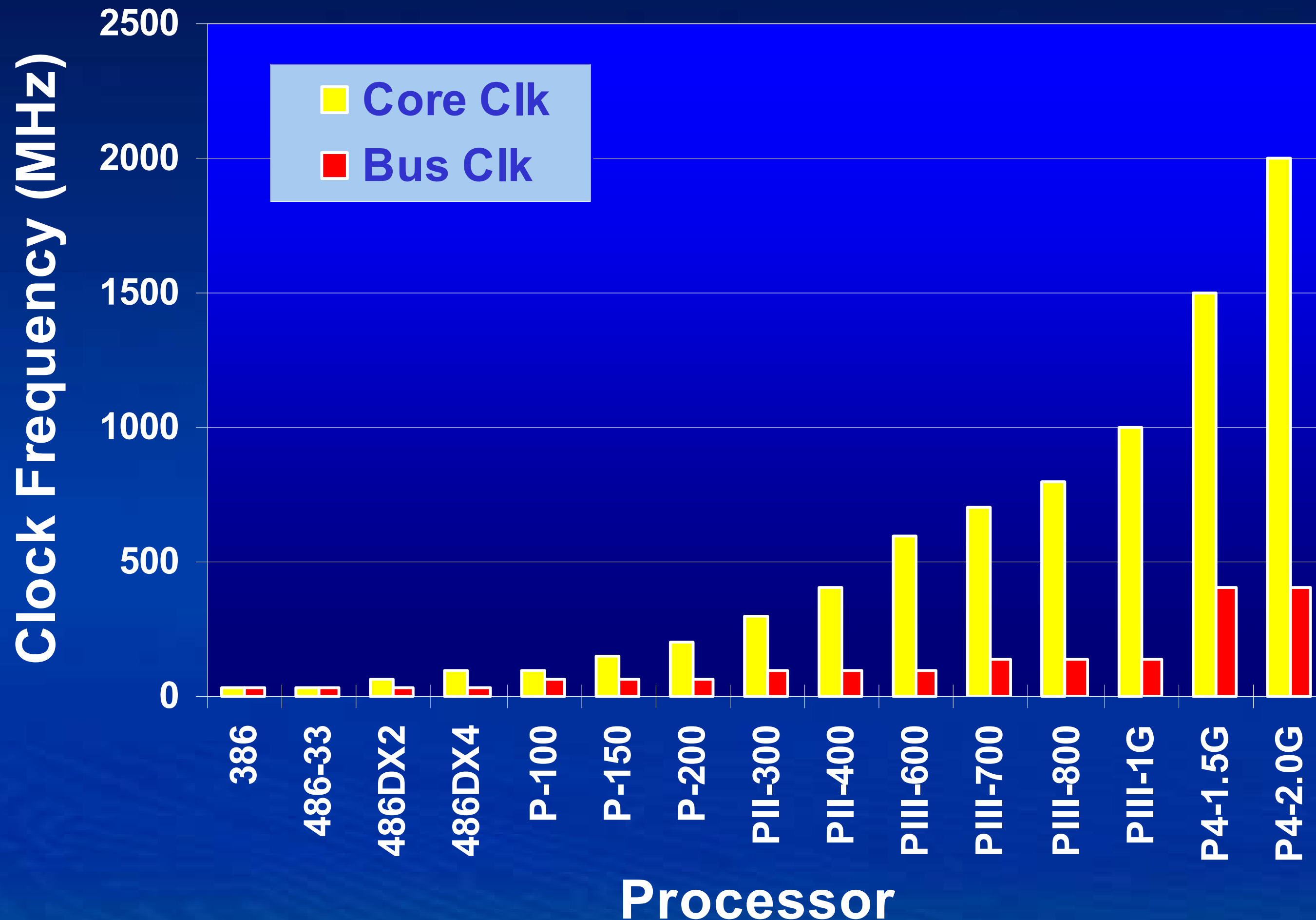
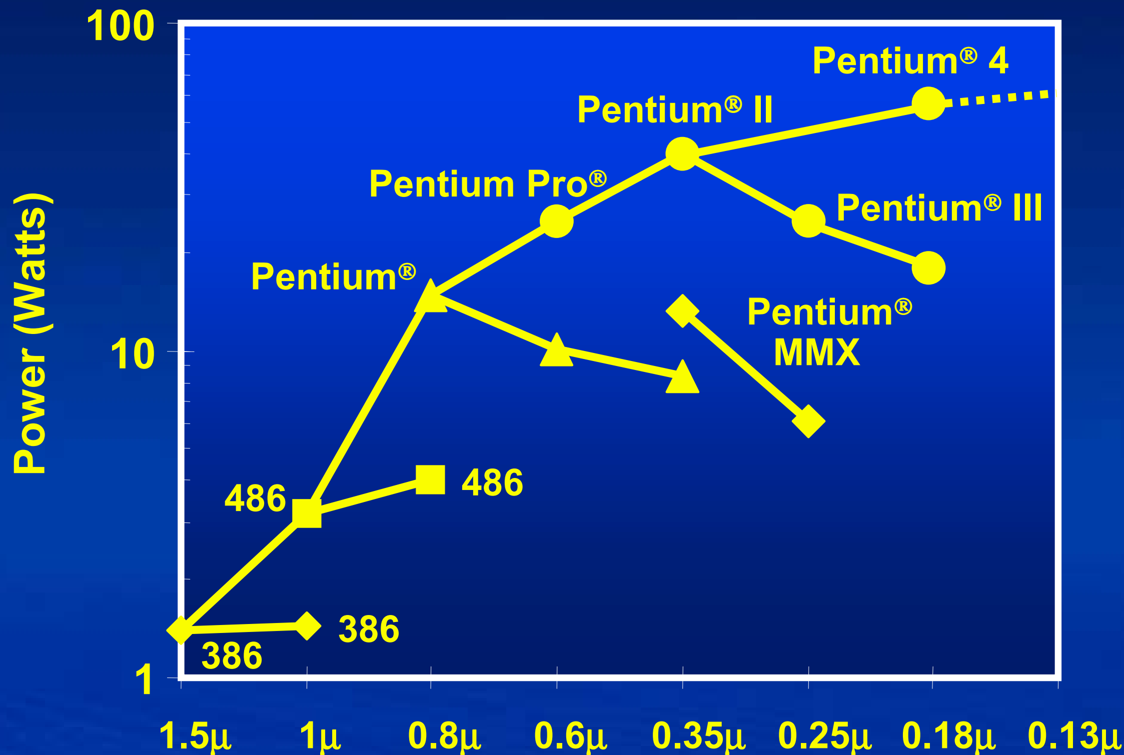
Processor Core Vs. Bus Clock



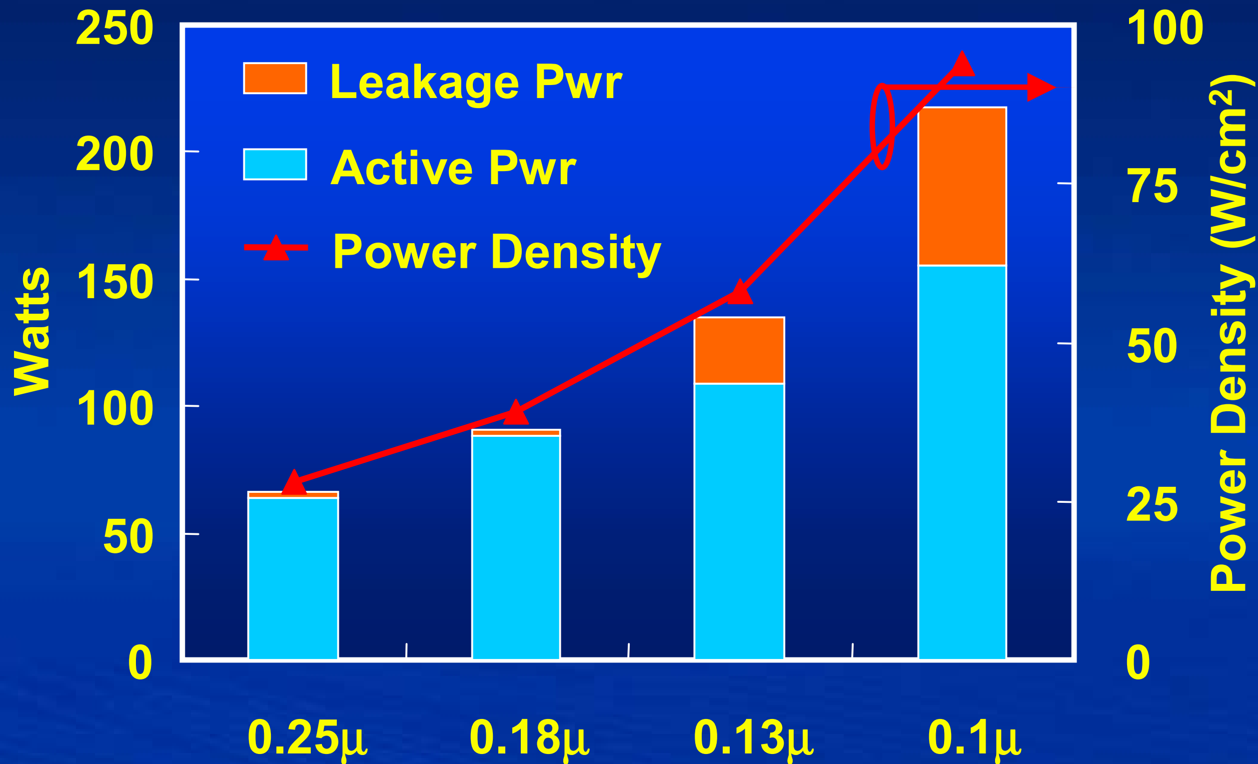
Bus frequency is not keeping up with the processor core

Processor Power Trend



- Lead processor power increases every generation
- Compactions provide higher performance at lower power

Power Density Trend



- Assumptions: 15mm die, 1.5x frequency increase per generation

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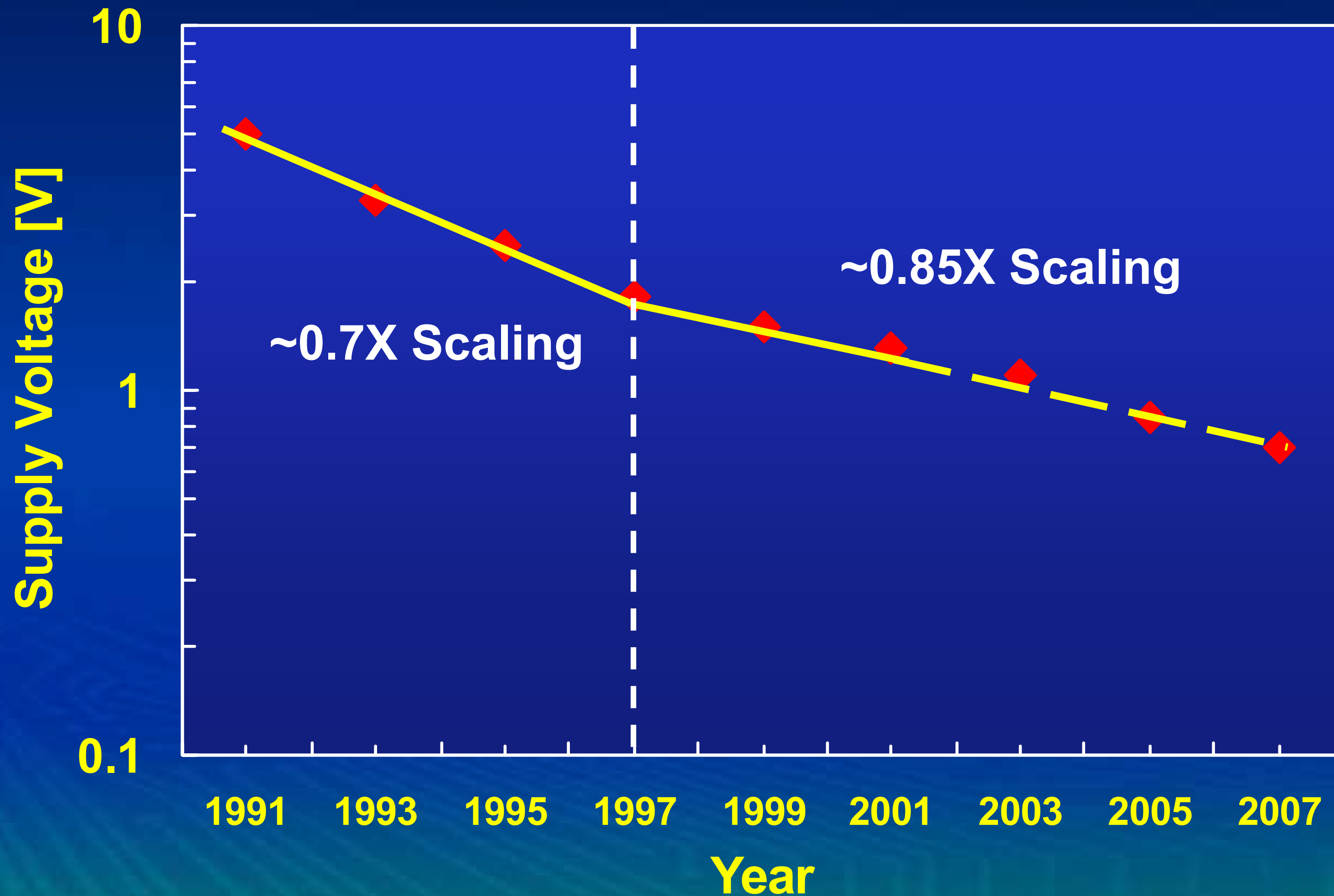
Voltage Scaling



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Transistor Physical Gate Length

1
0.1
0.01
Micron

0.5um
0.35um
0.25um
0.18um
0.13um
90nm
65nm
45nm
Technology Node

0.2um
130nm
70nm
50nm
30nm
20nm
Transistor Physical Gate Length

1991 1993 1995 1997 1999 2001 2003 2005 2007 2009
Year

Source: Robert Chau, 6/2001

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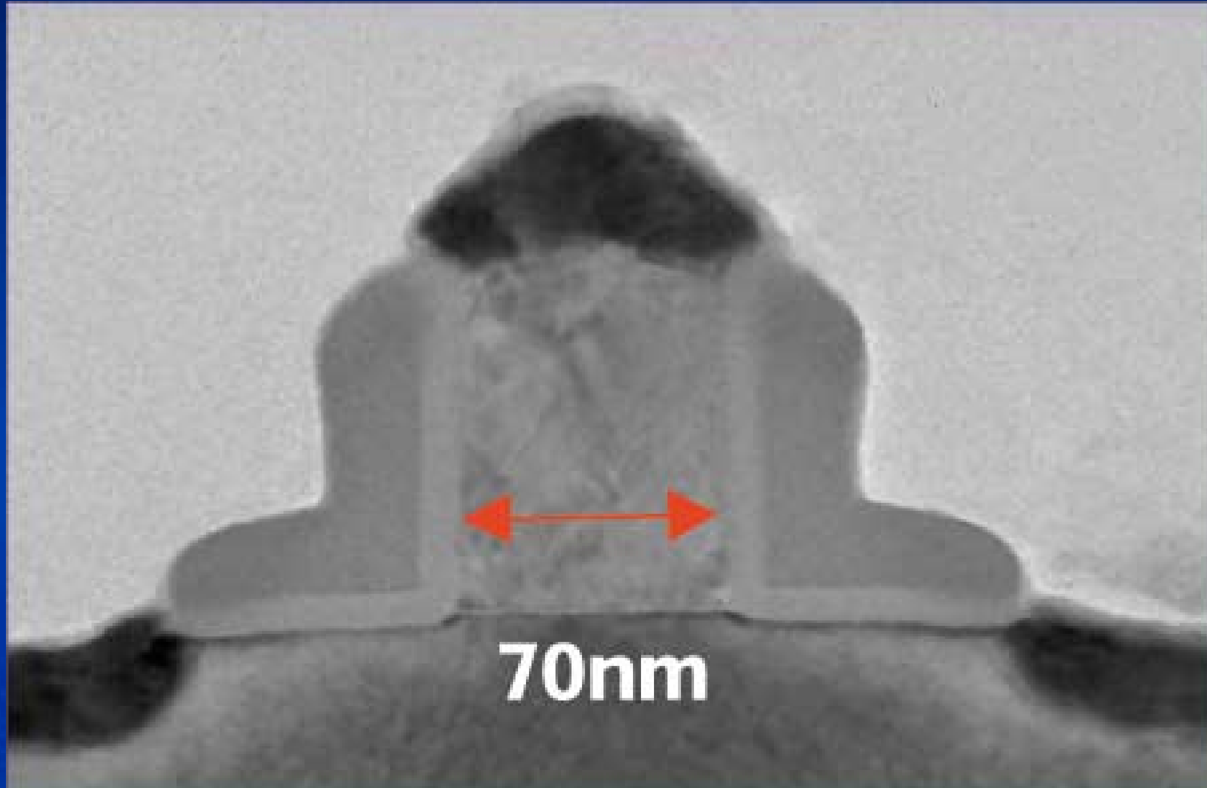
0.13µm Process Technology



70nm Lgate NMOS transistor – in production today

Source: S. Tyagi, et.al., IEDM 2000

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Transistor Physical Gate Length

Micron

1
0.1
0.01

0.5um
0.35um
0.25um
0.18um
0.13um
90nm
65nm
45nm

Technology Node

0.2um
130nm
70nm
50nm
30nm
20nm

Transistor Physical Gate Length

1991 1993 1995 1997 1999 2001 2003 2005 2007 2009

Year

Source: Robert Chau, 6/2001

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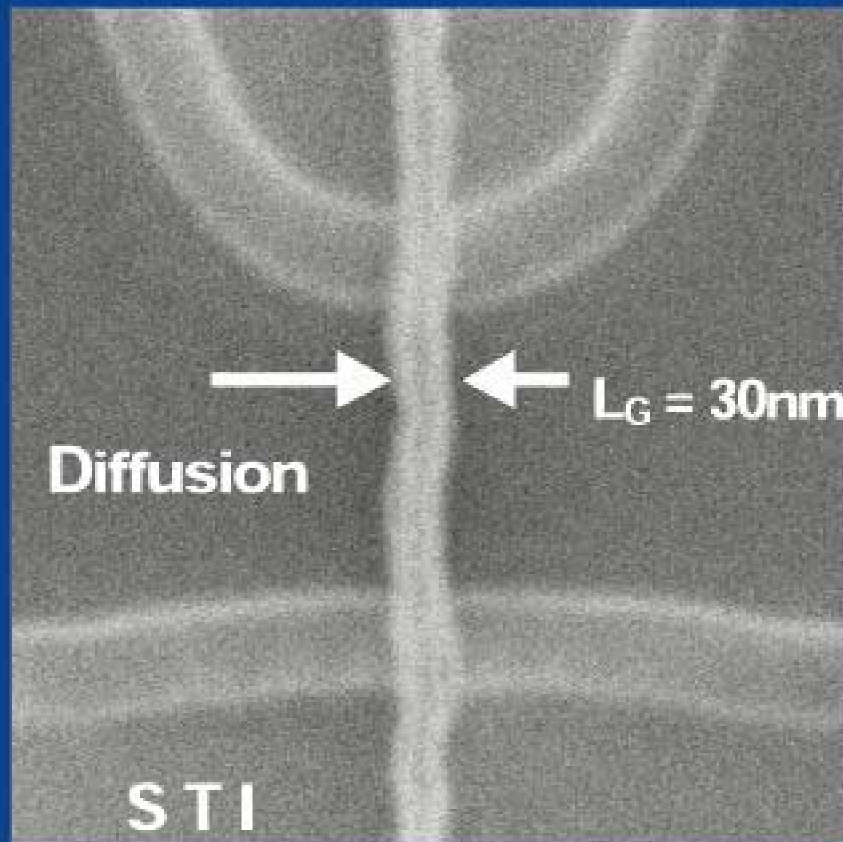
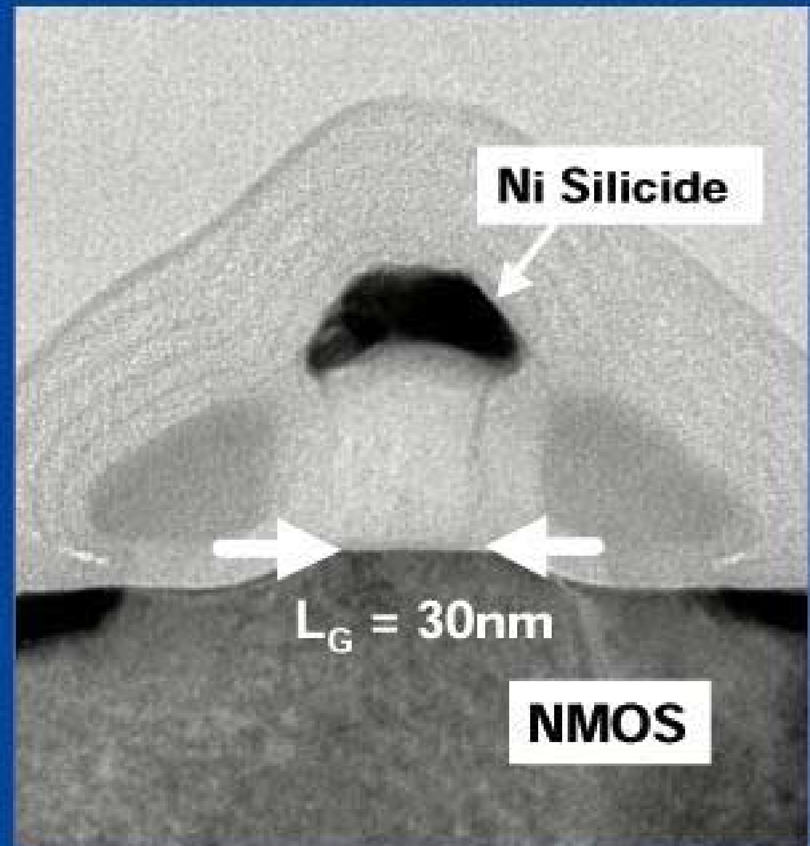
30nm Physical Gate Length Transistor





For the 65nm technology node – production 2005

Source: R. Chau, et.al., IEDM 2000

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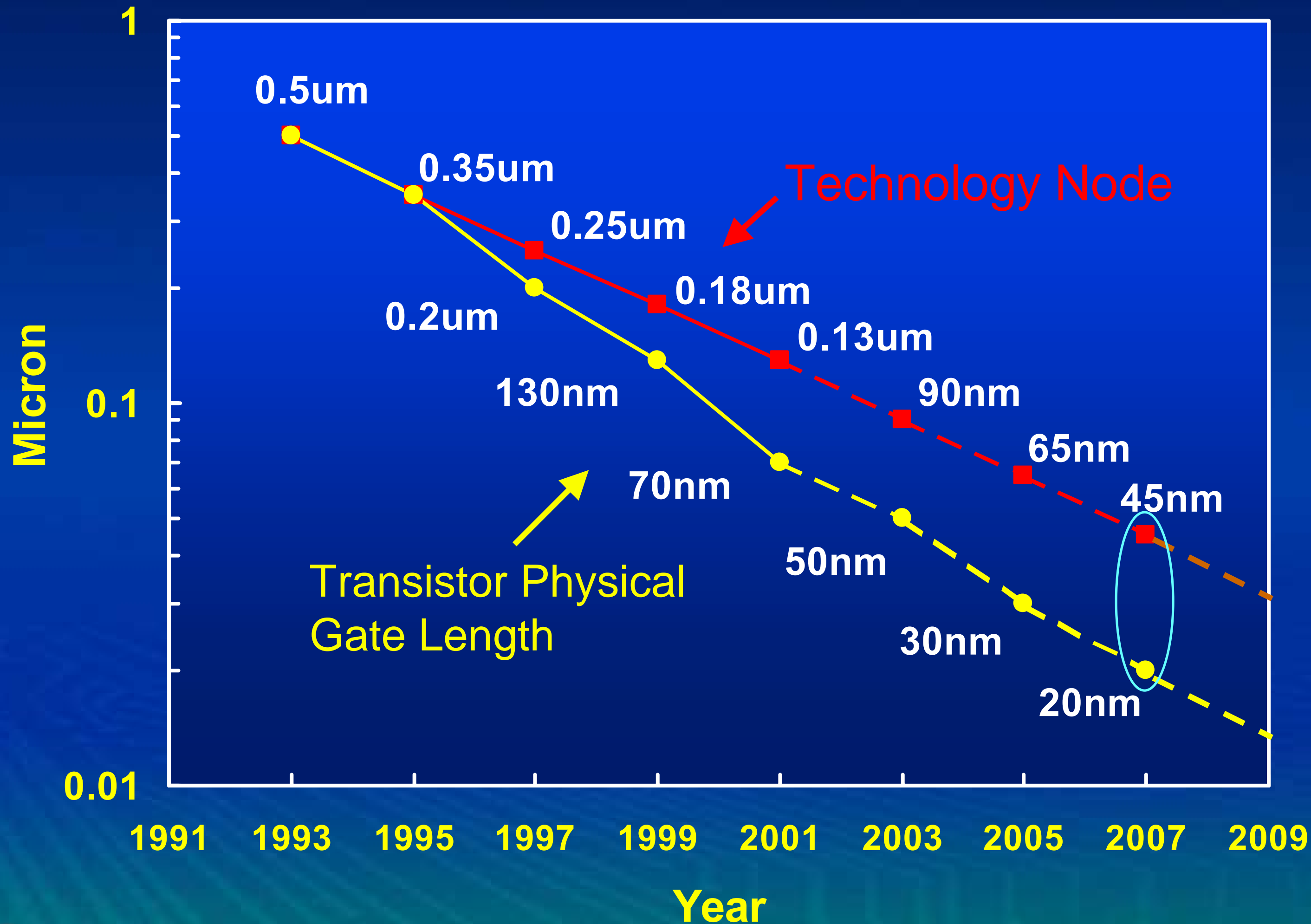
Transistor Physical Gate Length



Source: R. Chau, 6/2001

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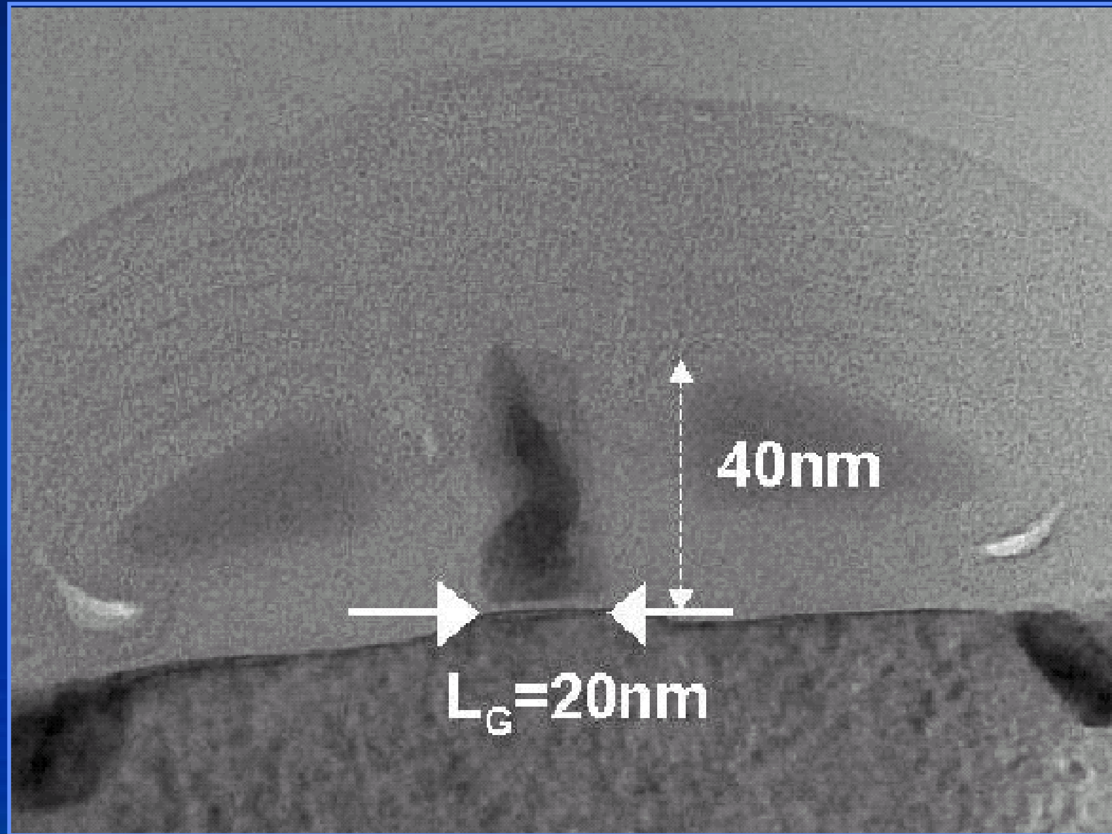
Research Transistor with 20nm Physical Gate Length



For the 45nm technology node – research phase

Source: R. Chau, et.al., SNW 2001

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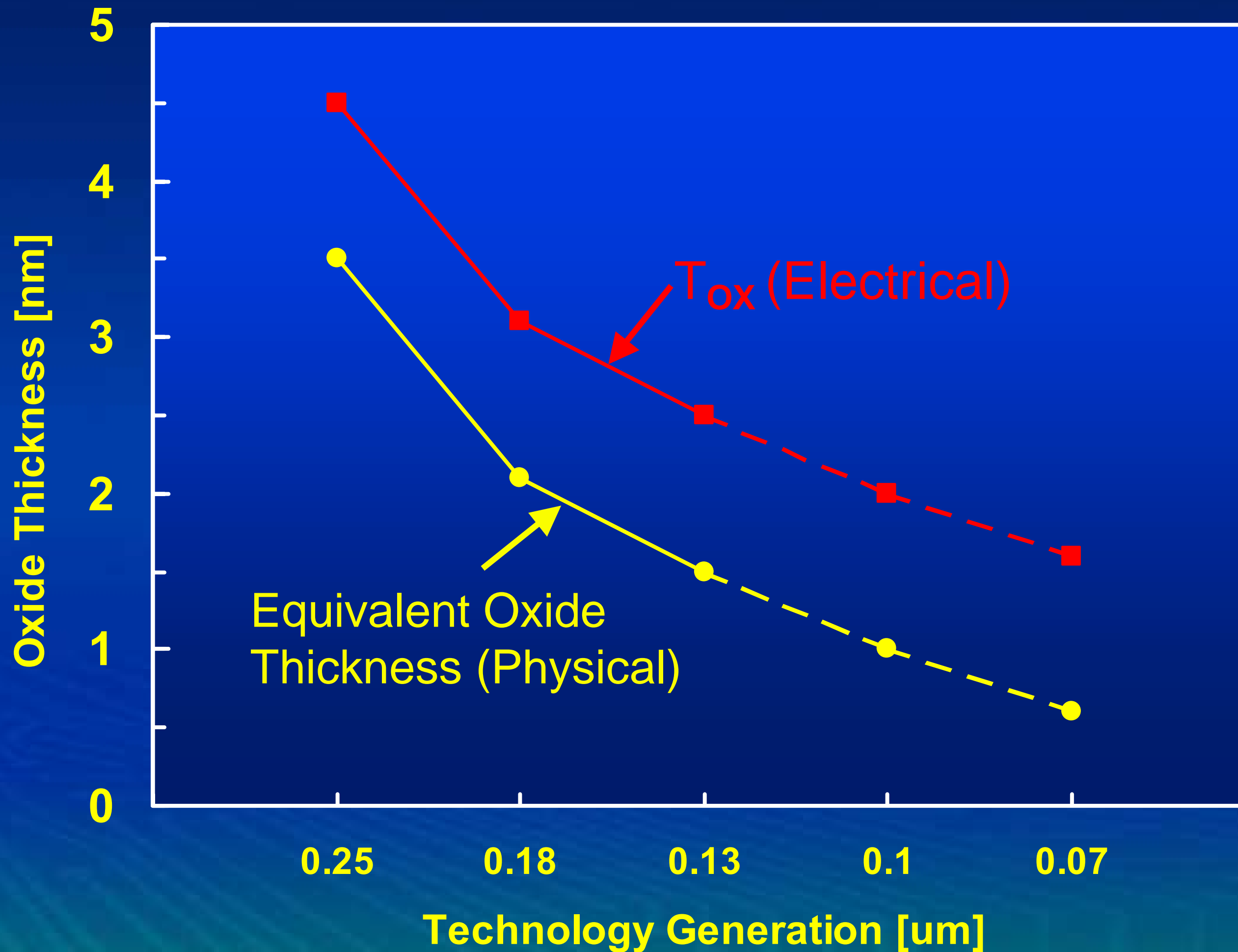
Oxide Thickness Scaling



Source: T. Ghani, VLSI Symposium, 2000

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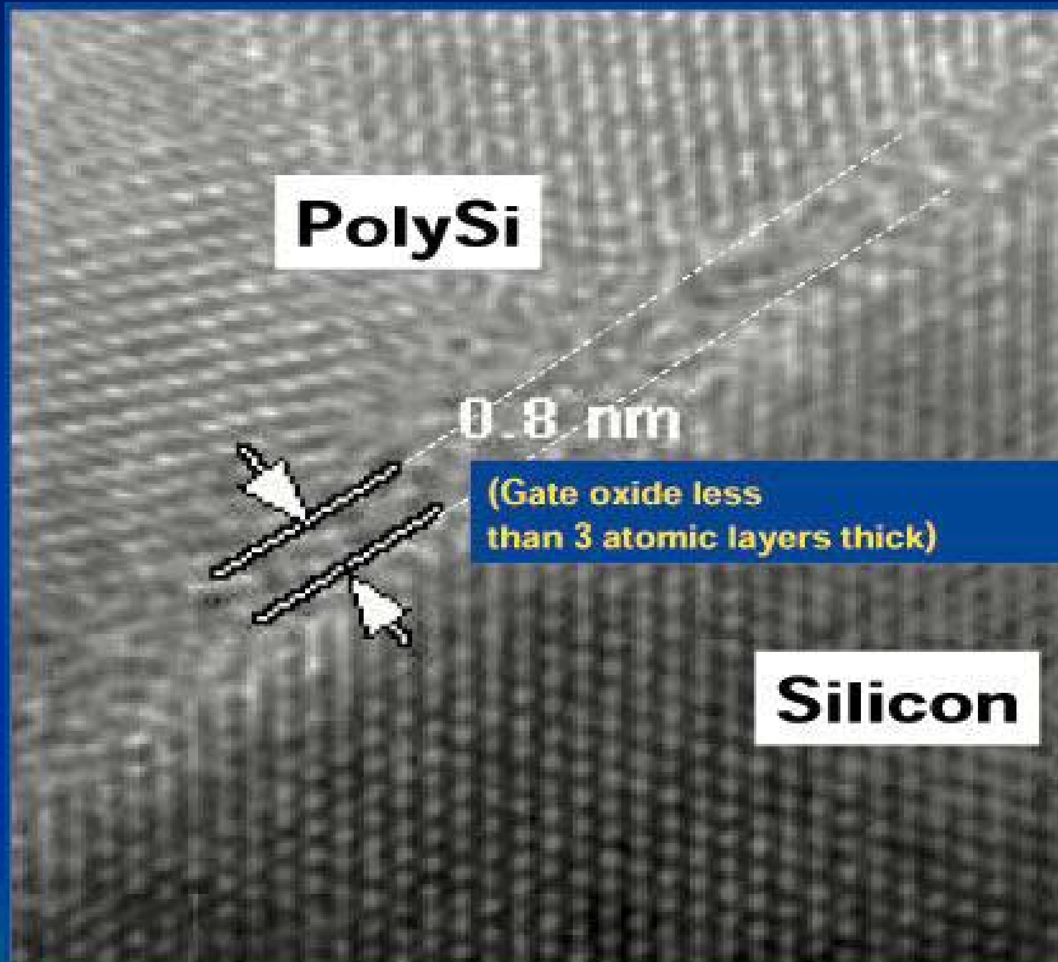
Atoms-Thin Gate Oxide



Source: R. Chau, et.al., IEDM 2000

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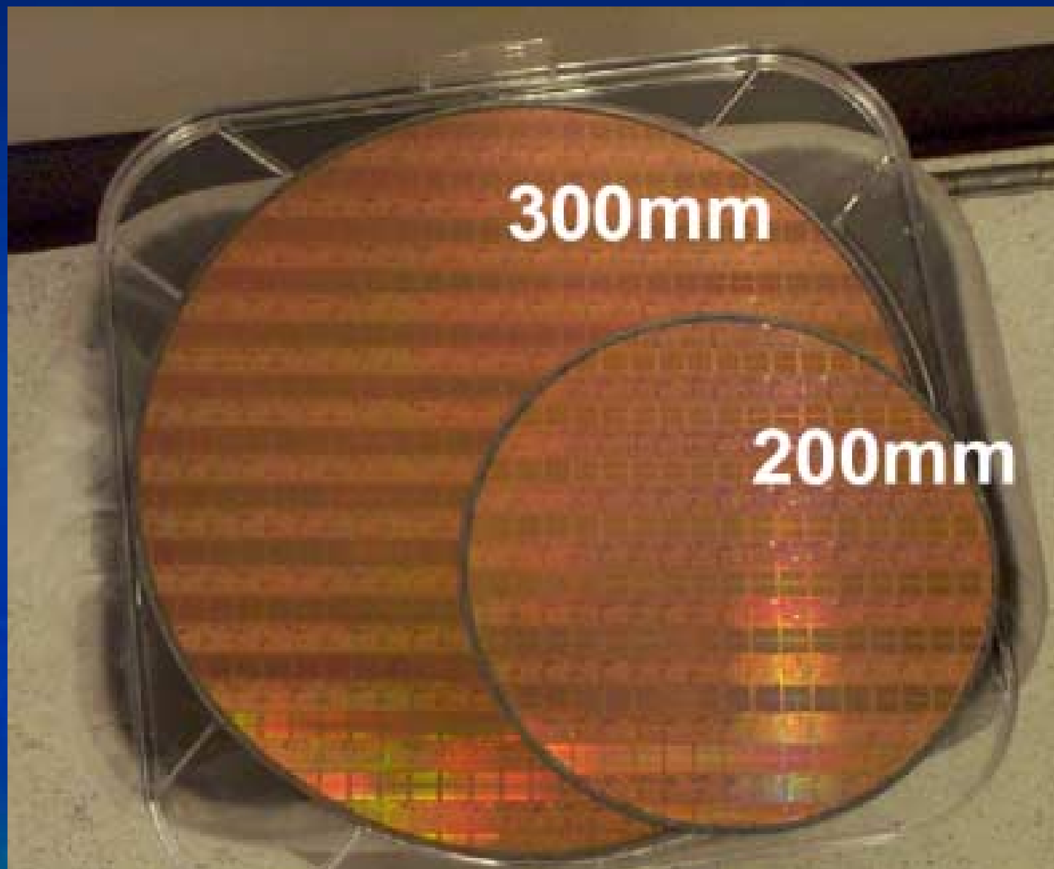
Moore's Law + 300mm Wafers = 4x advantage



- Moore's Law:
  - From 0.18µm to 0.13µm = 2x output
- 300mm Wafers:
  - From 200mm to 300mm = 2x output
- Combined output advantage:
  - 4x output

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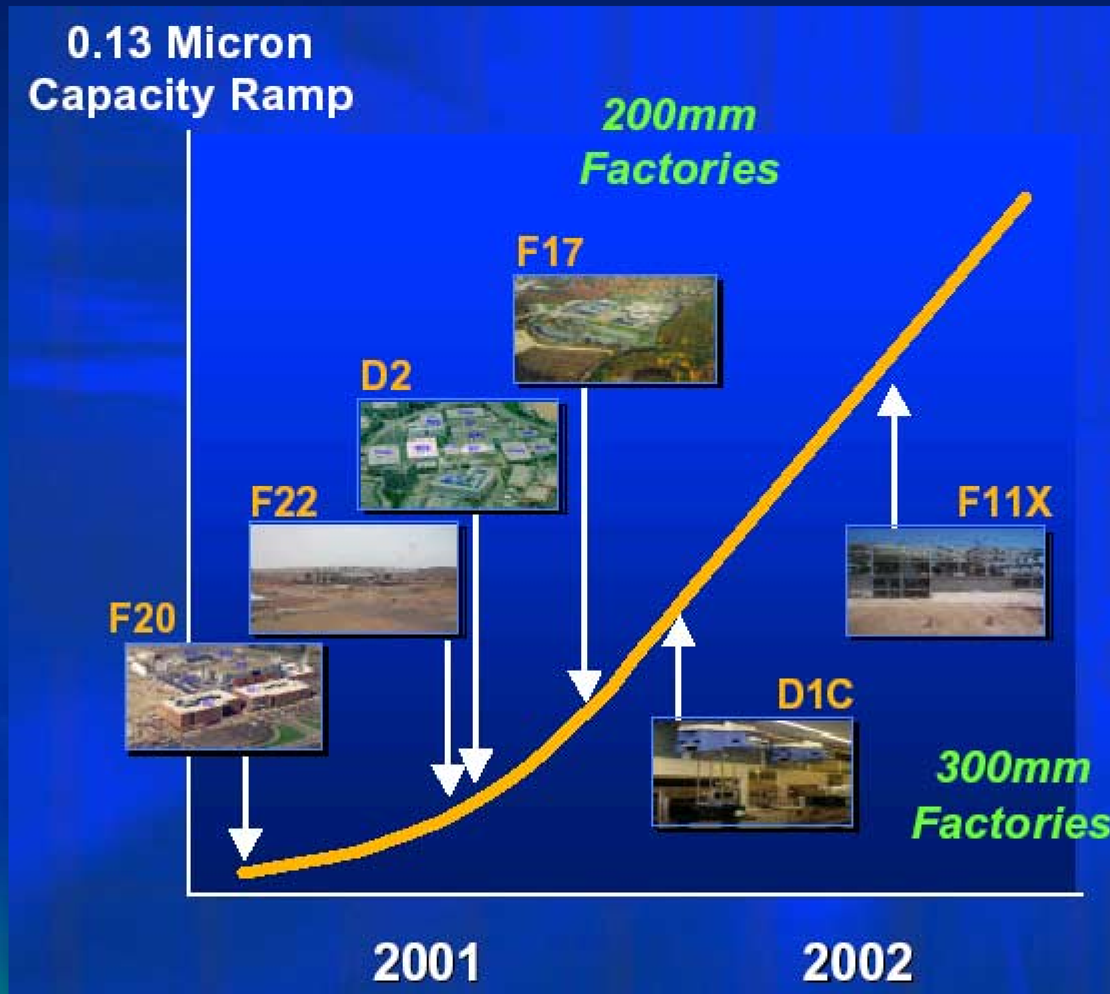
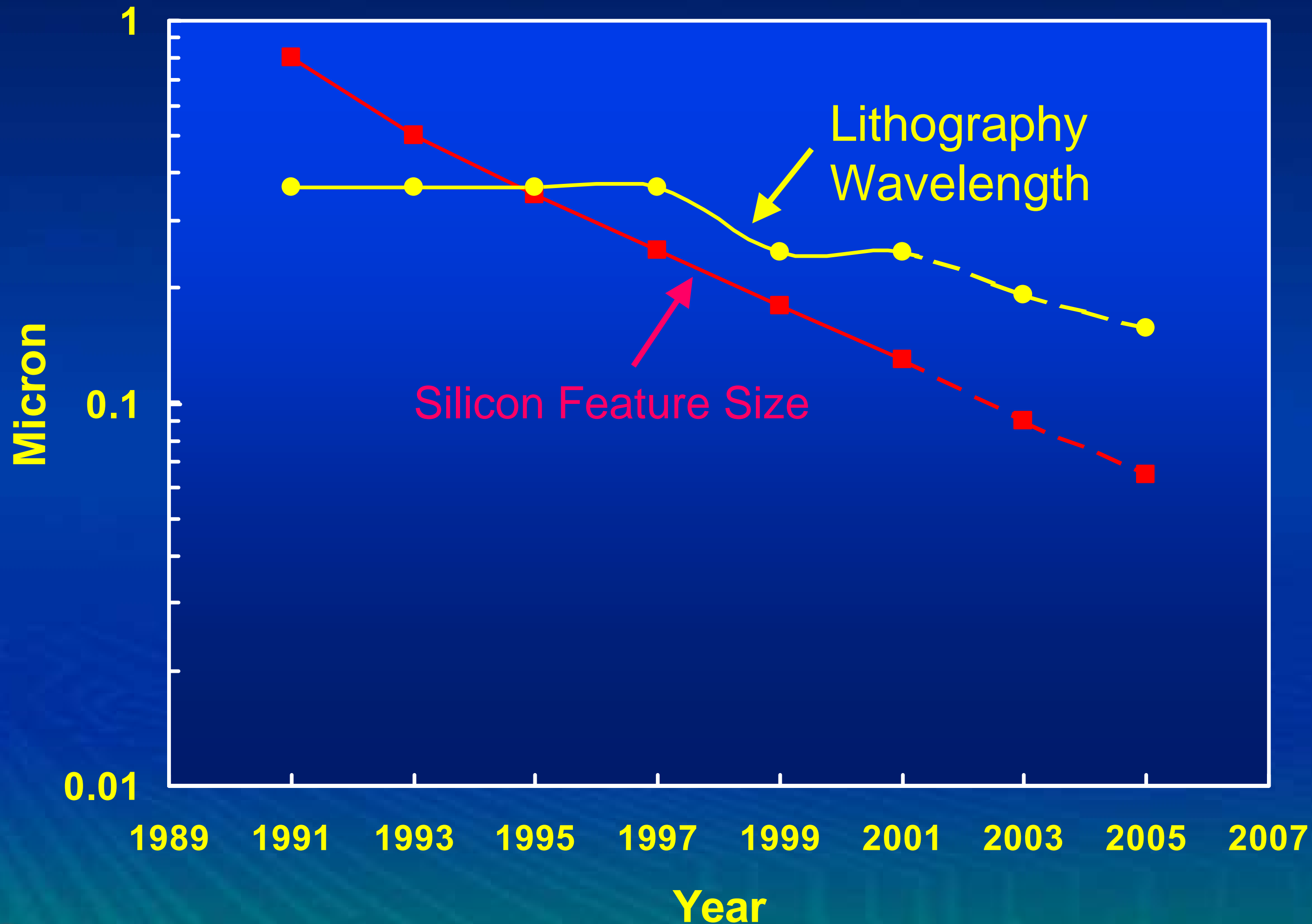
0.13μm Production Ramp



- **Six factories readying 0.13μm production**
  - Plan to spend $7.5B on capital in 2001
- **Yields and volume exceeding expectations**
  - 0.13μm products have been shipping since May

Lithography Challenges



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Extreme Ultraviolet Lithography

- EUV lithography uses extremely short wavelength light (20x shorter than today's lithography processes)
  - *Visible light – 400 to 700 nm*
  - *DUV lithography – 193 and 248 nm*
  - *EUV lithography – 13 nm*
- Will be used first in 2005 for critical lithography steps to produce 70 nm patterns

World's First 6-inch EUV ETS Mask

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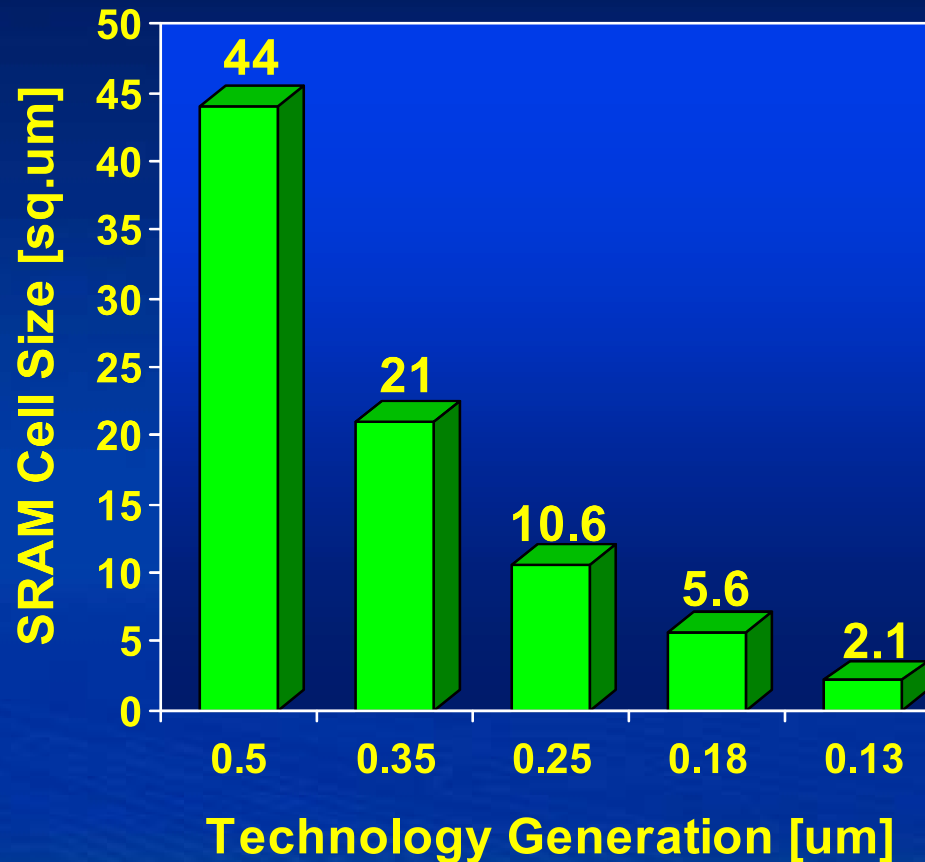
SRAM Cell Size Scaling



- SRAM cell size will continue to scale ~0.5x per generation

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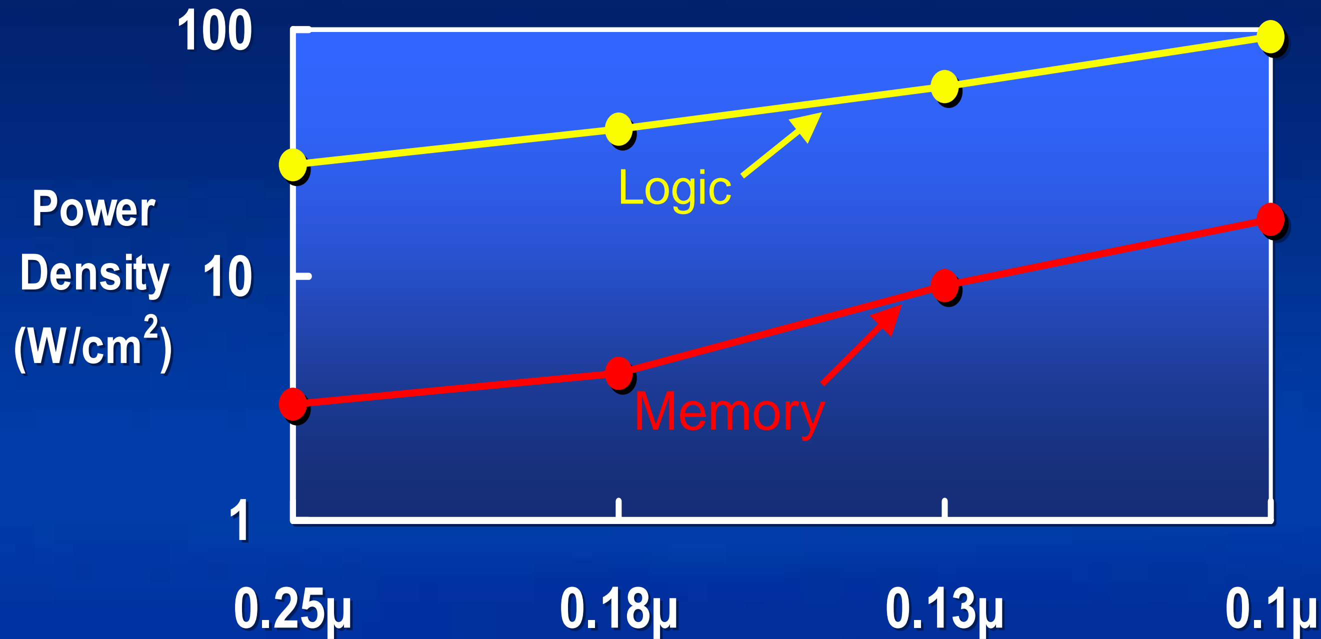
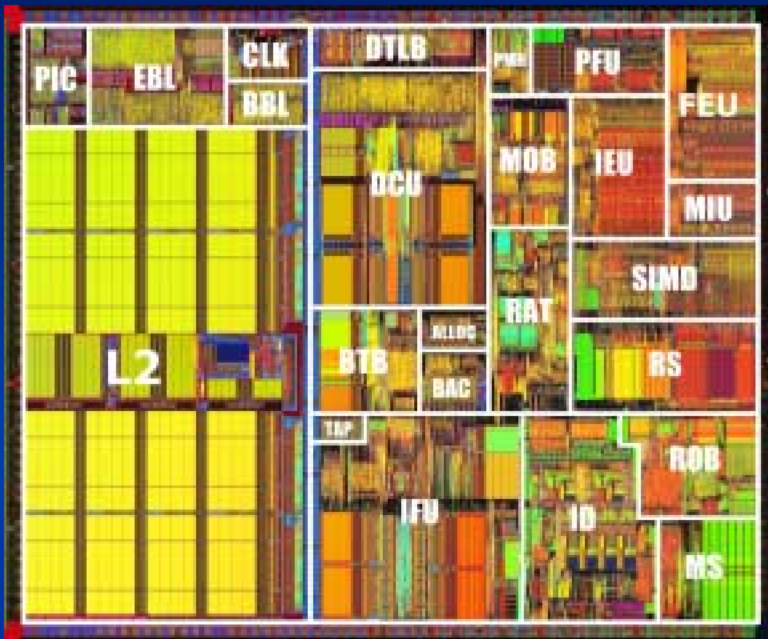
Exploit Memory Power Efficiency

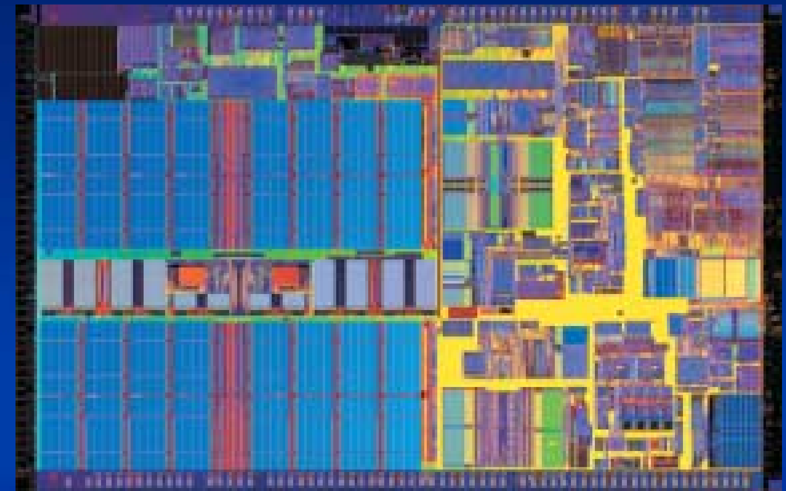


- Static memory has 10X lower active power density
- Lower leakage than logic
- Integrated L2 provides higher bandwidth and lower latency

Example: Pentium® III Processor Evolution



- 0.18µm technology
- 256KB L2
- 28 million transistors
- 106 mm² die size



- 0.13µm technology
- 512KB L2
- 44 million transistors
- 80 mm² die size

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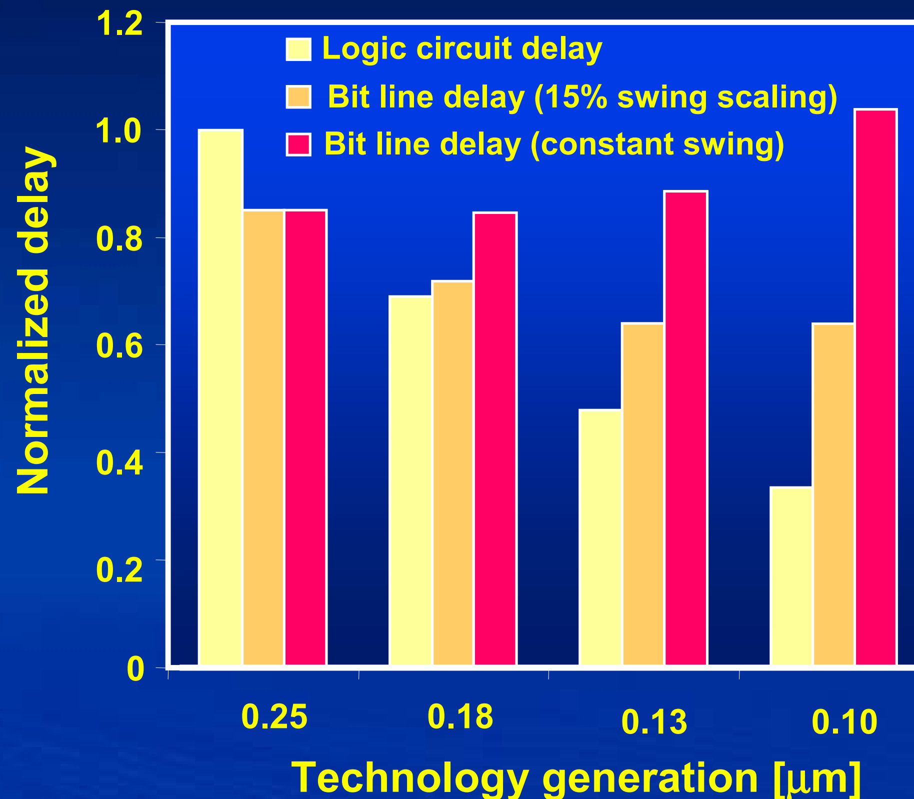
Bit Line Delay Scaling



- Bit line swing limited by parameter mismatch & differential noise
- Cell stability degrades with Vt lowering
- Reducing number of rows per bitline approaching limit

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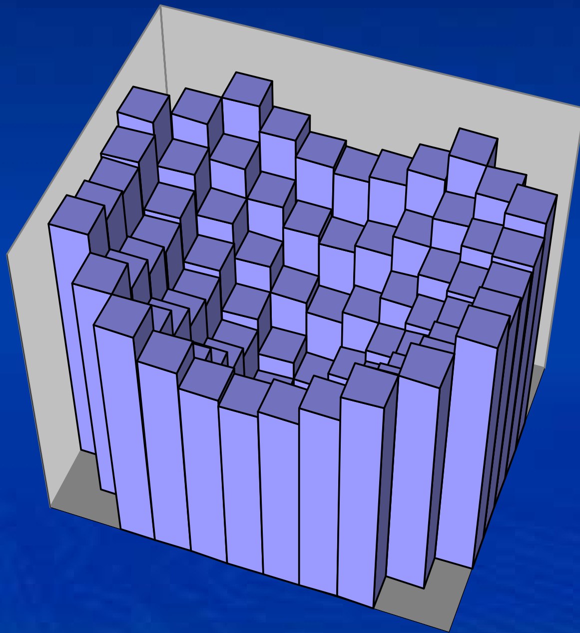
Process Fluctuations

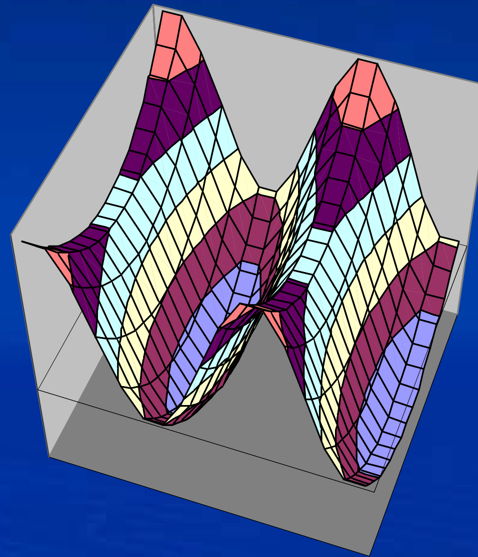
Die-to-Die Fluctuations



Resist Thickness

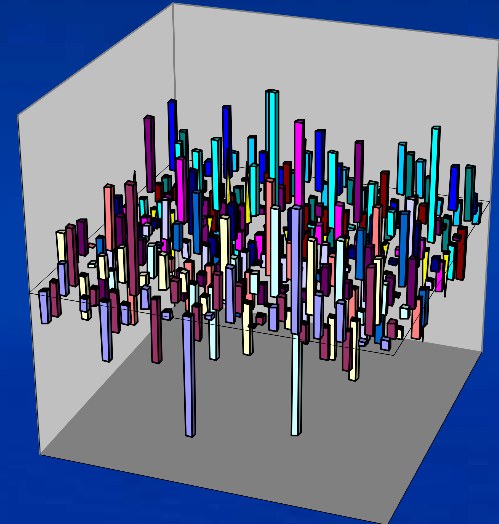
Within-Die Fluctuations

Systematic



Lens Aberrations

Random



Random Placement of Dopant Atoms

Source: K. Bowman, et.al., ISSCC'2001

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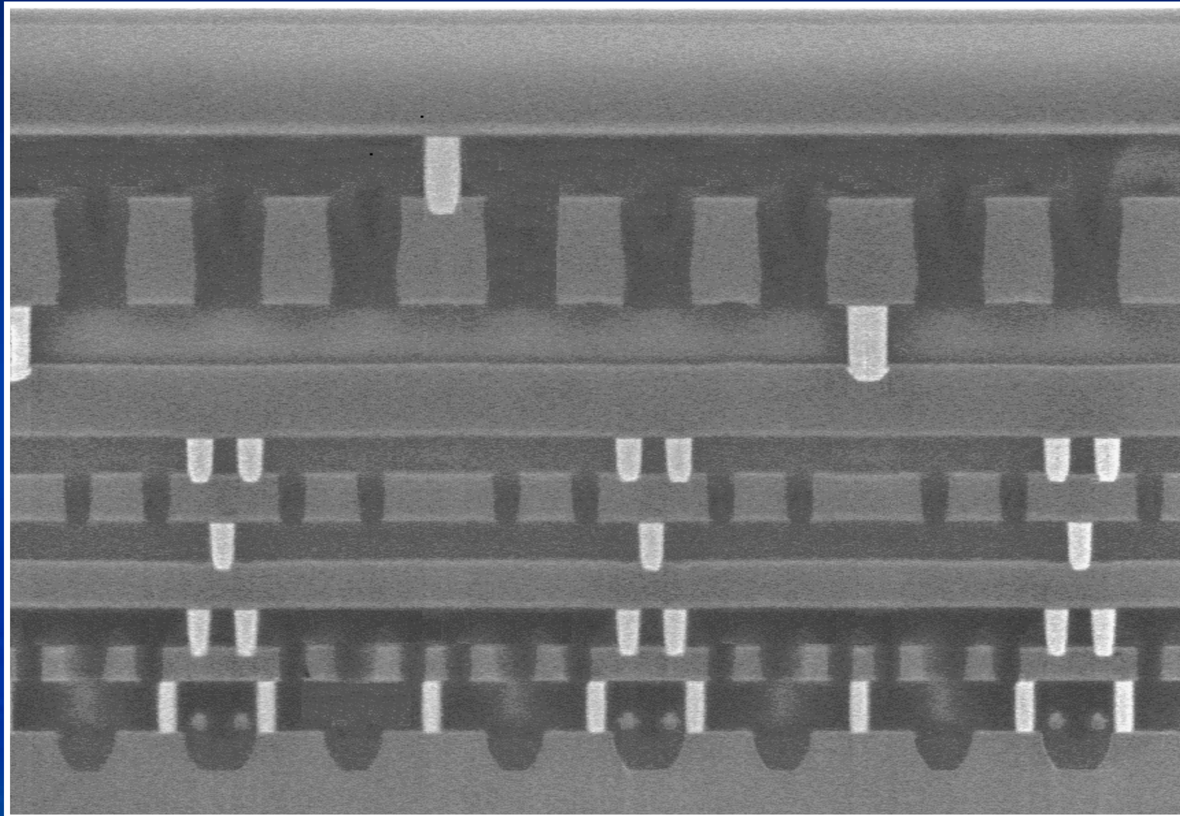
0.18µm Al Interconnect



Metal 6

Metal 5

Metal 4

Metal 3

Metal 2

Metal 1

Transistors

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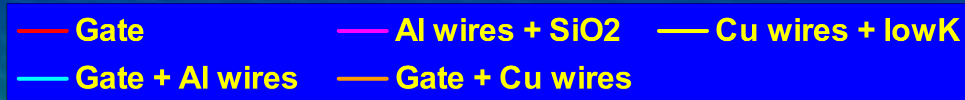
Wires Are Not Scaling Well

Delay [ps]

45
40
35
30
25
20
15
10
5
0

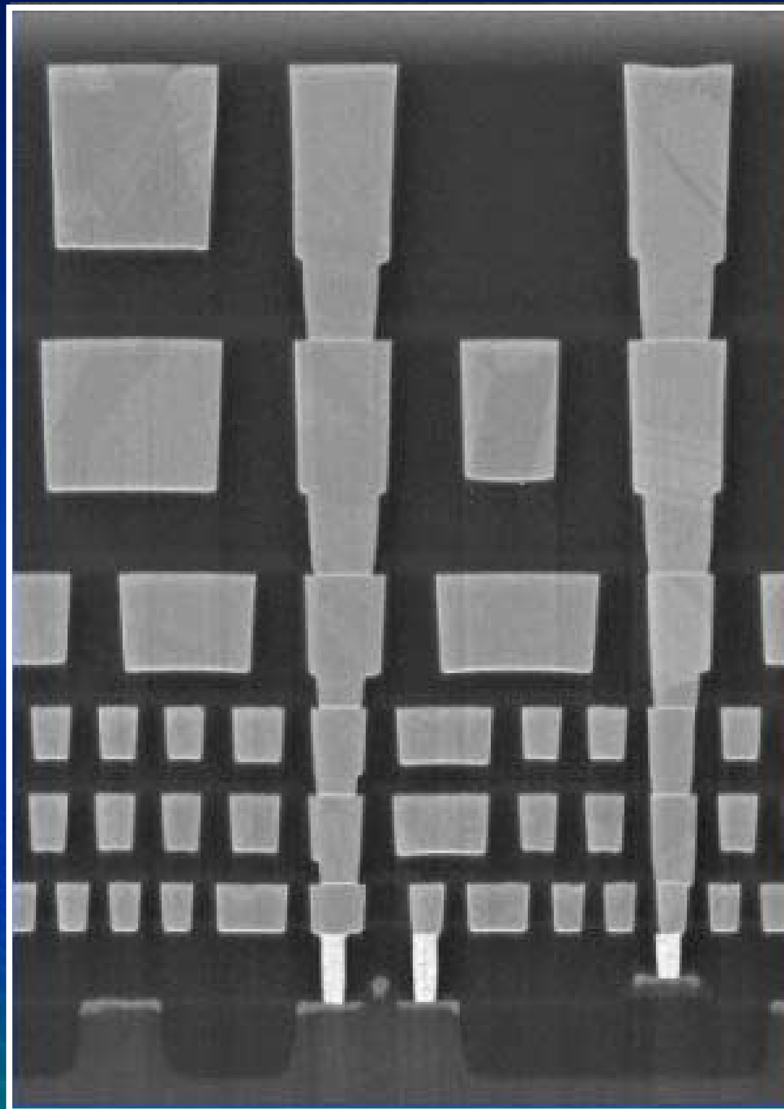
0.65 0.5 0.35 0.25 0.18 0.13 0.1

Process Generation [um]



Source: SIA NTRS projection

0.13µm Cu Interconnect



Metal 6

Metal 5

Metal 4

Metal 3

Metal 2

Metal 1

Transistors

Source: S. Tyagi, et.al., IEDM 2000

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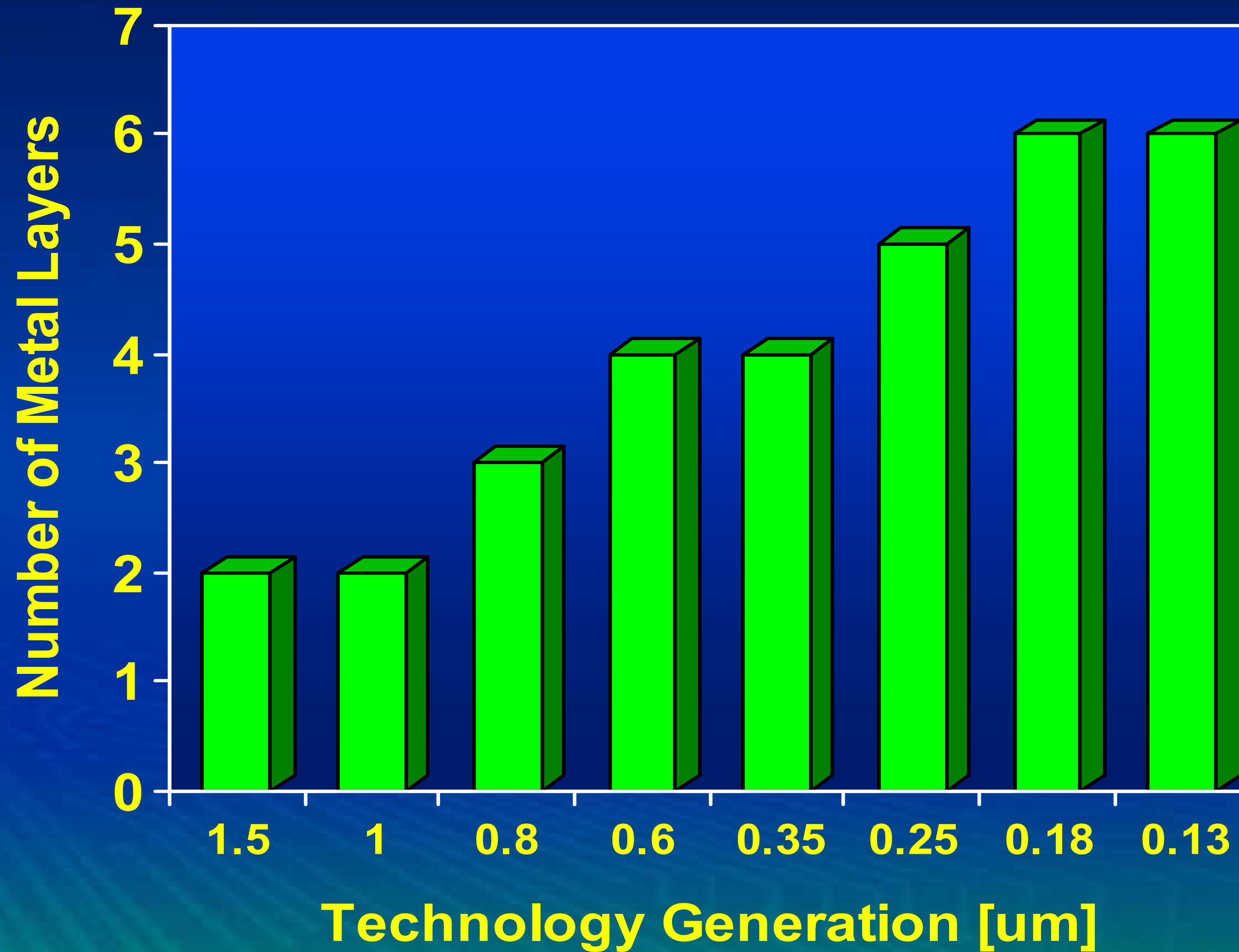
Metal Layers



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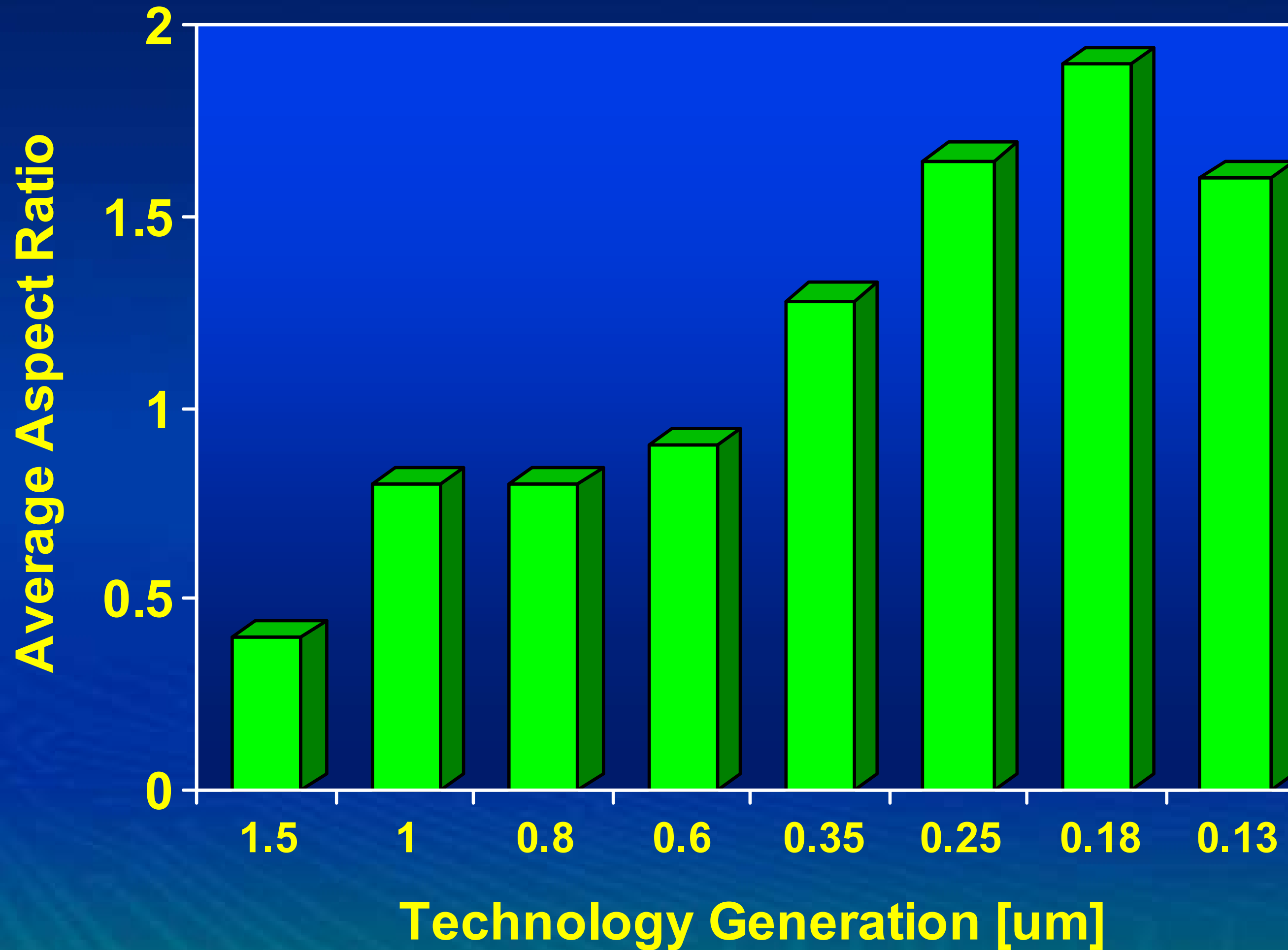
Metal Aspect Ratios



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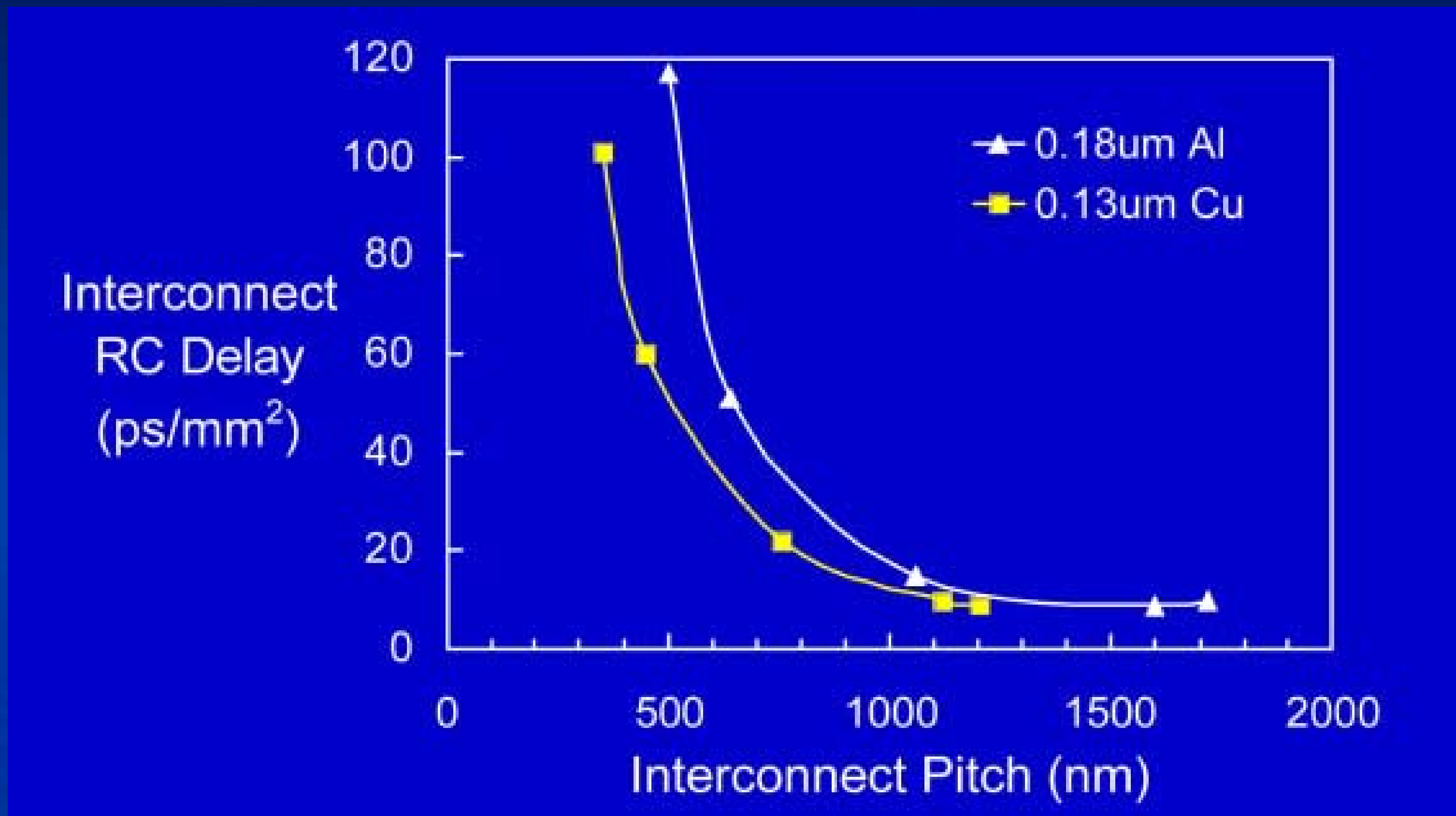
Interconnect RC Delay vs. Pitch



- **40% lower RC delay by using Cu + FSG ILD**

Source: S. Tyagi, et.al., IEDM 2000

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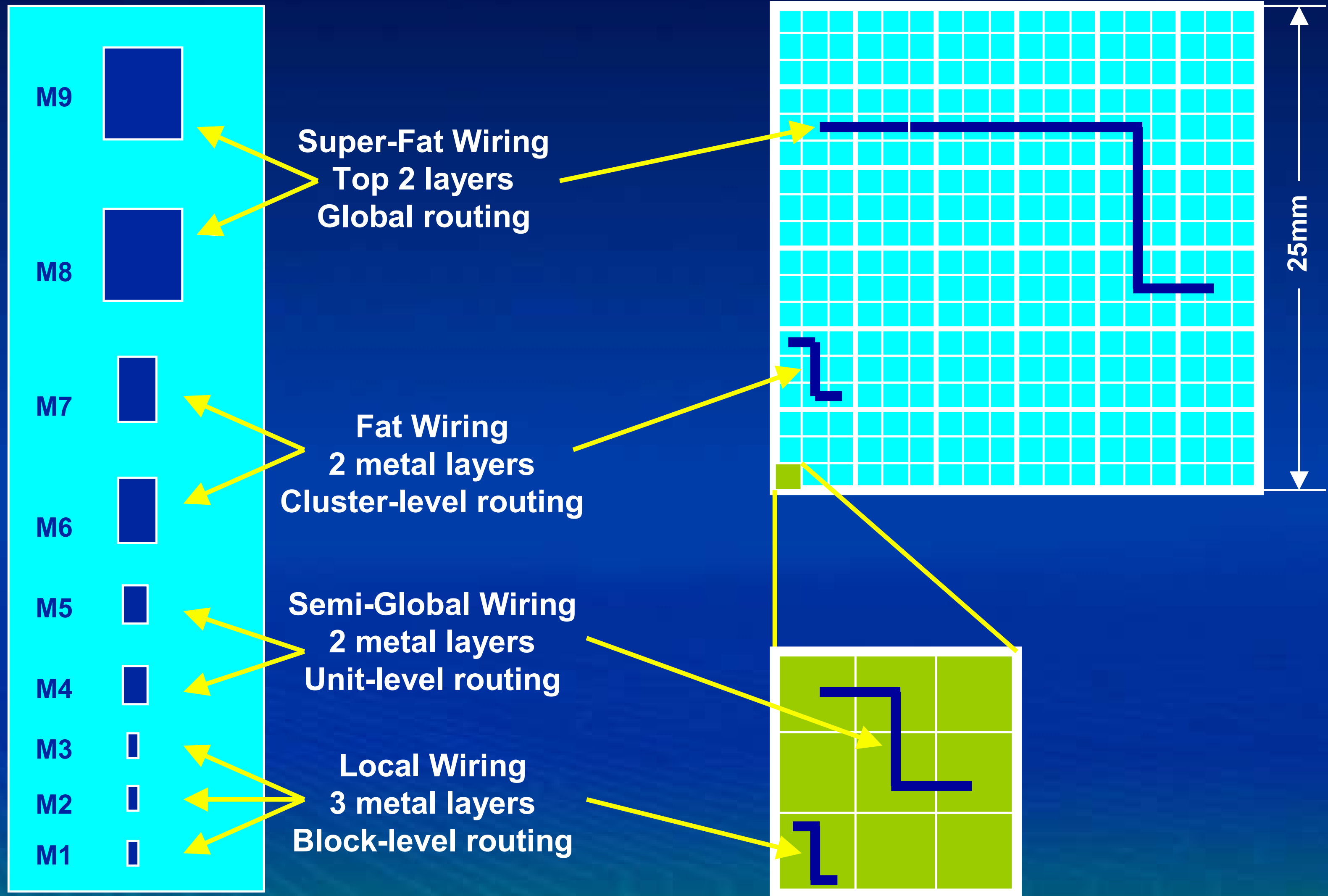
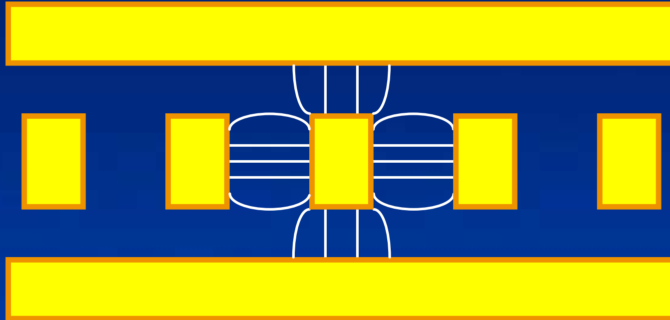
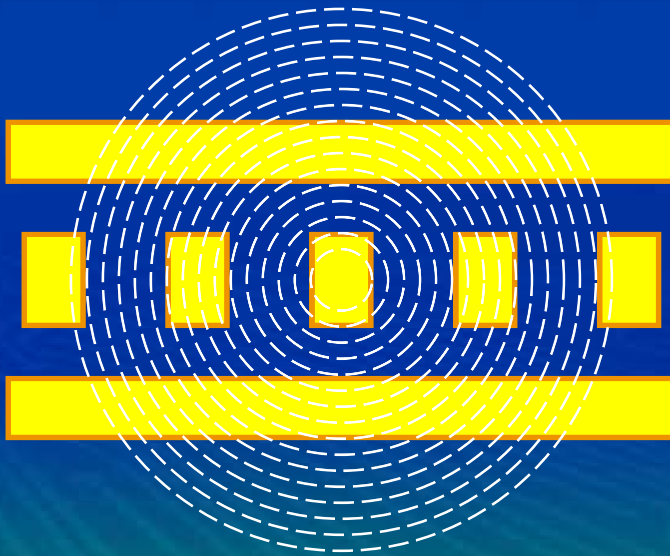
Routing a 70nm Processor



Noise Sources





- Capacitive Coupling
  - Due to electric field
  - “Near” field effect
  - Measures resistance to a voltage change
- Inductive Coupling
  - Due to magnetic field
  - “Far” field effect
  - Measures resistance to a current change
  - Frequency dependent

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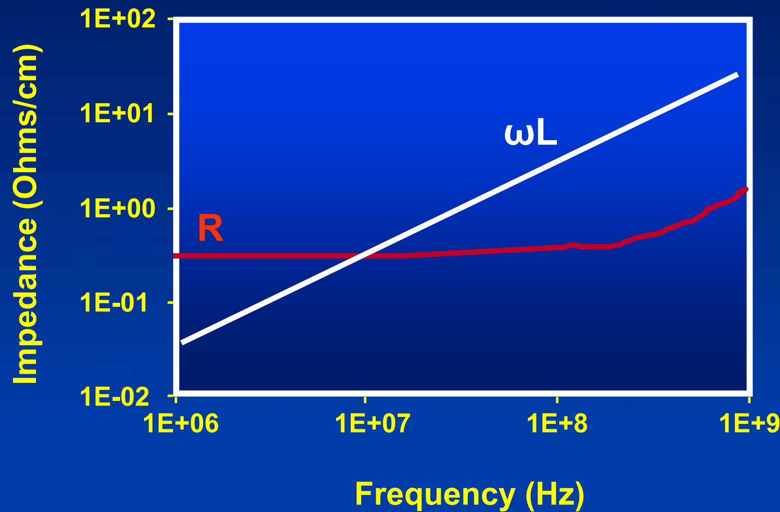
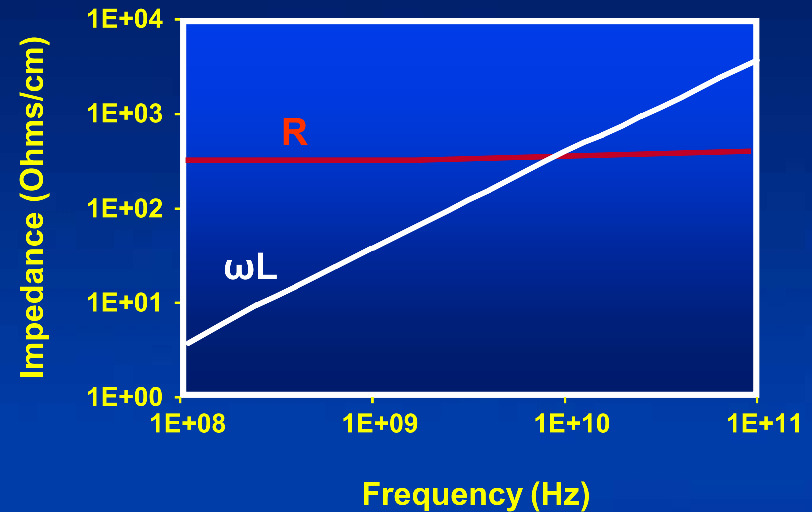
Inductive Noise



PCB (FR4) Signal Trace

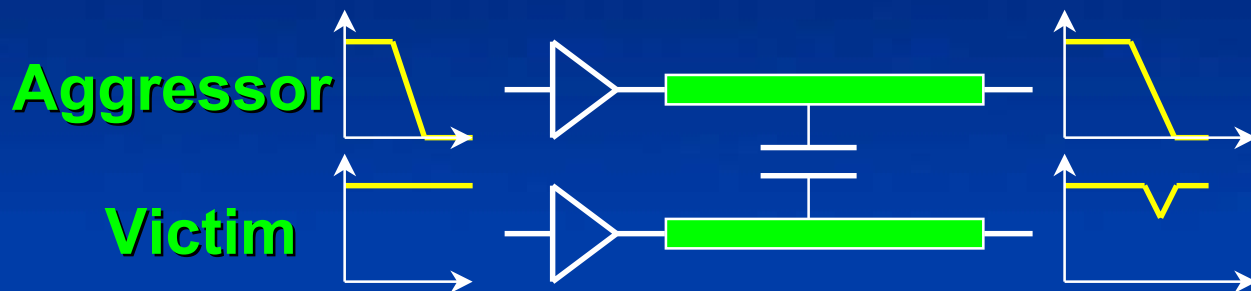


VLSI Metal Line

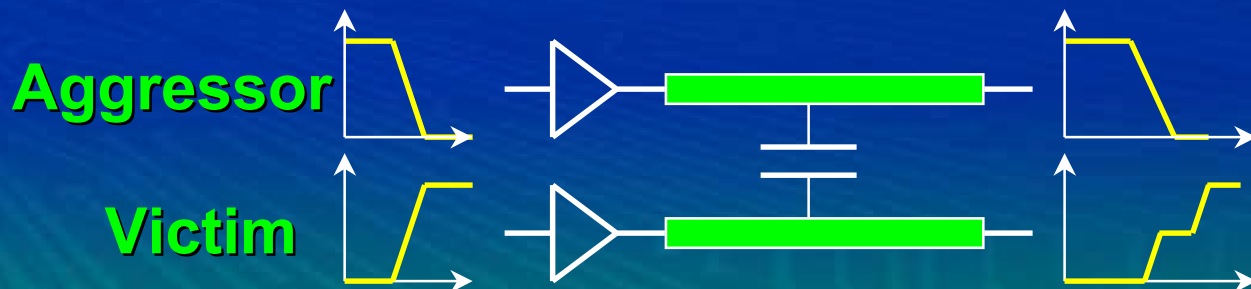
- Inductance of VLSI metal lines is becoming important at operating frequencies above 1GHz

Effects of Capacitive Coupling

- Capacitive coupling can translate into a noise problem



- or a delay problem



Worst Case Input Patterns

- Near attackers couple mostly by capacitance
- Far attackers couple mostly by inductance
- Lenz's law - a change in current will generate an opposing current which resists the change
- Worst-case switching pattern when near and far attackers switch anti-phase

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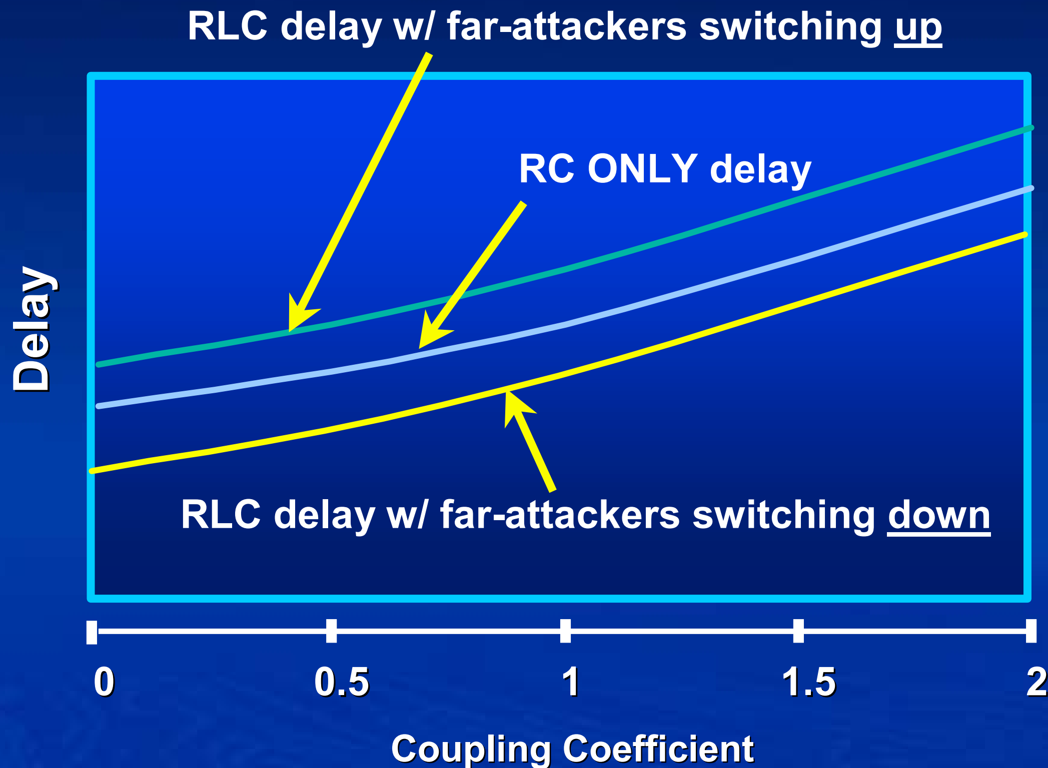
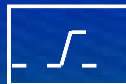
Inductive Noise Impact on Delay





- Capacitive noise effect on delay is modeled by coupling coefficient
- Inductive noise affects delay too
- Inductive noise can also decrease delay

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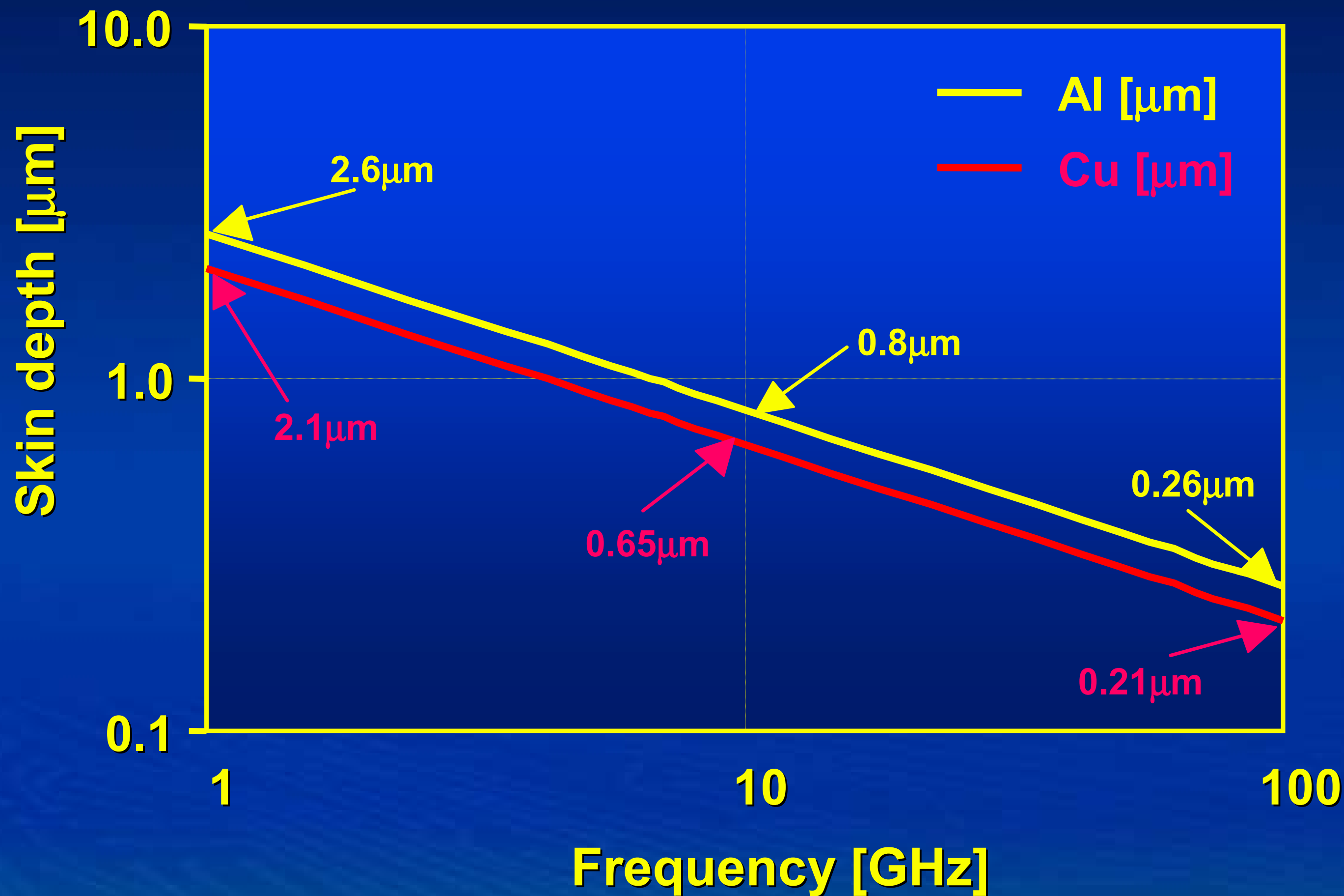
Skin Effect in VLSI Circuits



- Edge frequency is 5-9x the clock frequency

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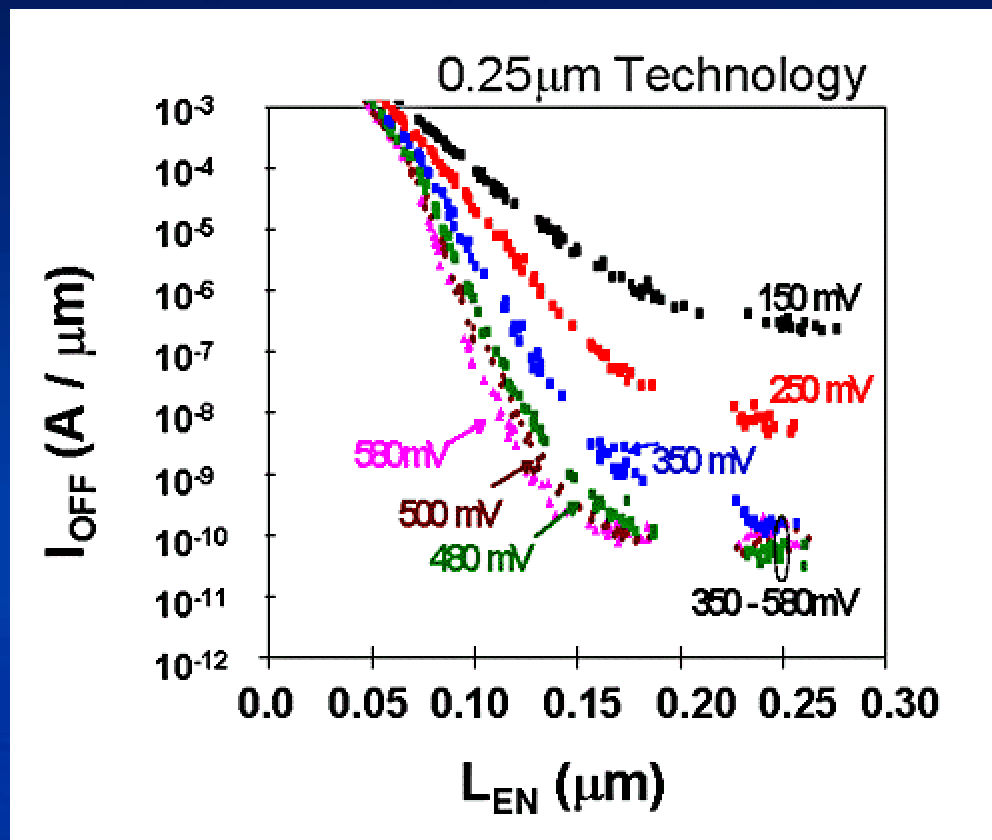
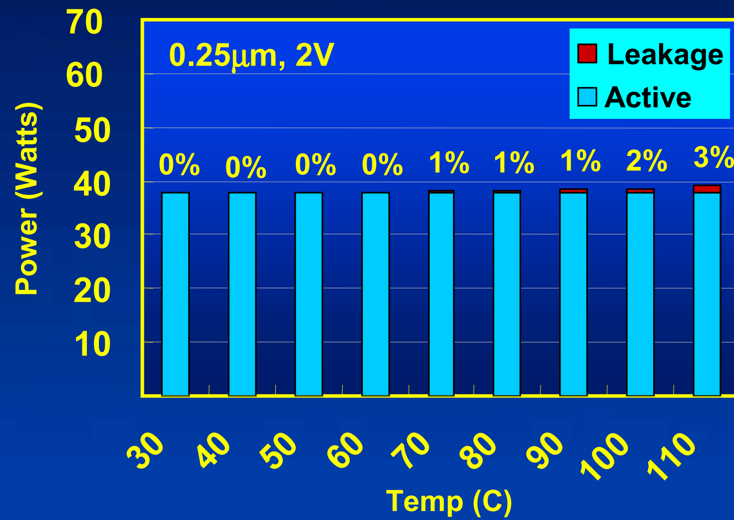
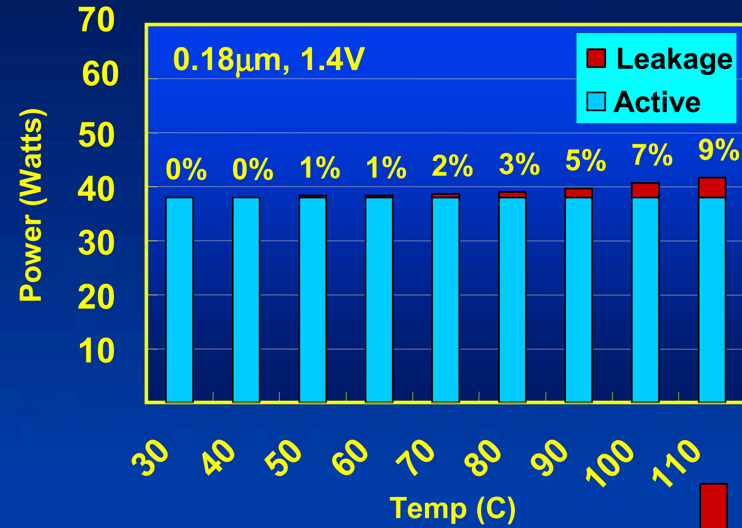
Sub-Threshold Leakage

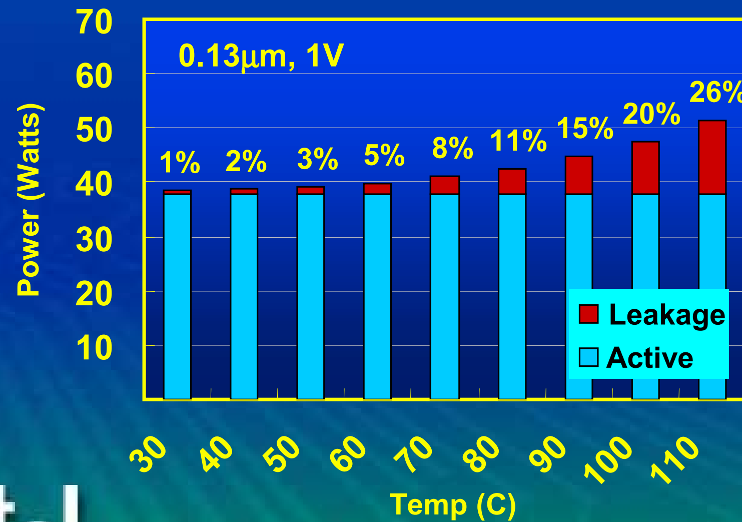


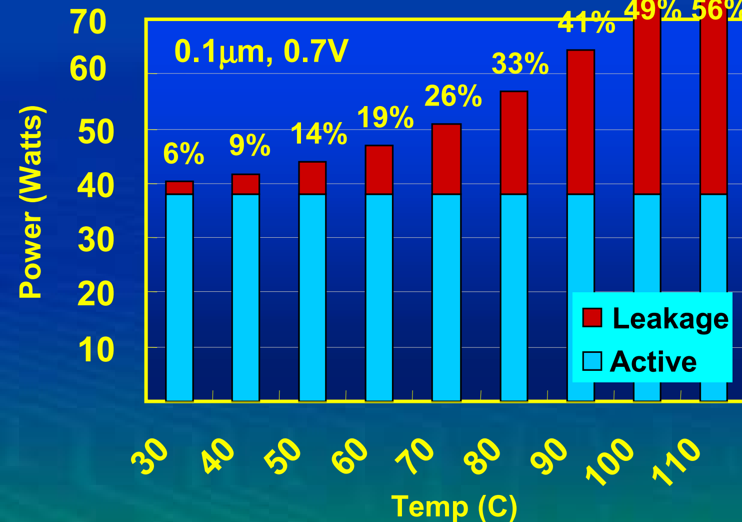
- **Sub-threshold leakage increases for lower channel lengths and lower V_T's**

Estimated Power of a 15mm Processor









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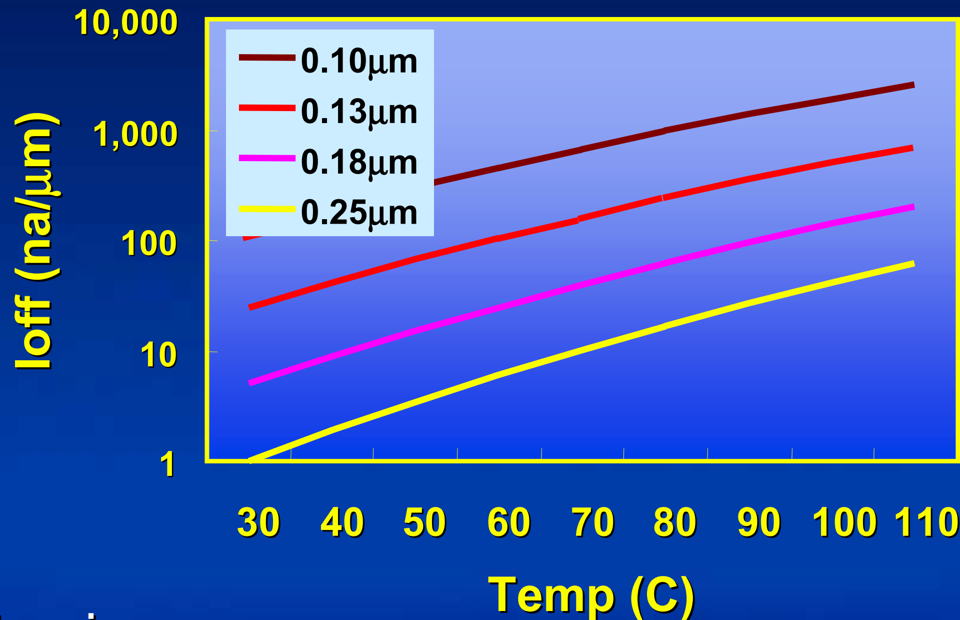
Leakage Impact



- Design issues:
  - Dynamic circuits may fail
  - Design workarounds needed to guarantee burn-in functionality
- Test issues:
  - IDDQ testing may become ineffective
  - Thermal-runaway problems, especially at burn-in

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Conclusion

- We still have not found a fundamental barrier to extending Moore's law
- The challenges are Power and Efficiency
  - Focus on dissipation, delivery, density
- VLSI technology scaling is expected to continue for the next decade

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