THE LOG PERIODIC

www.scvemc.org Santa Clara Valley Chapter of IEEE Electromagnetic Compatibility Society

IEEE SCV EMC Society Meeting: Tuesday, September 13, 2011

Time: Social 5:30 p.m. Presentation 6:30 p.m.

Place: Applied Materials Bowers Cafeteria
3090 Bowers Ave., Santa Clara, CA 95051-0804

Subject: Designing PCB Stackups to Balance Signal Integrity vs. Manufacturability

Speaker: Lee W. Ritchey, President of Speeding Edge

Abstract:

With the ever increasing speeds of logic and RF systems, the demands placed on PCBs have made it necessary to consider more than impedance when designing the stackup used to for PCB manufacturing.

Traditionally, the electronics industry has placed the burden for designing the PCB stackup on the front end engineering personnel at PCB fabricators. While this is convenient for design engineers it places responsibility for several key electrical performance decisions on the fabricator's engineers which they are not equipped to handle. Among those performance decisions are crosstalk rules, impedance targets, interplane capacitance needs and types of weaves that will minimize differential skew between members of a the very high speed differential pairs used in protocols such as PCI Express, XAUI, Double XAUI and other data links that operate at multiple gigabit per second rates.

This session is intended to cover all of the aspects of PCB stackup design from materials choices to arrangement of signal layers and power planes to take the most advantage of the fabrication process. It is taught by an engineer who has been designing PCB stackups for the workstation and super computer marketplace since these products began to be designed and is currently designing stackups for a wide range of products including terabit routers and other products employing signaling protocols to as high as 20 Gb/S. The author has worked with PCB fabricators from the inception of multilayer PCB manufacture and currently works with both fabricators and laminate suppliers to achieve the highest performance from the overall process at the least cost.

Speaker Bio:

Founder and president of Speeding Edge, Lee Ritchey is considered to be one of the industry's premier authorities on high-speed PCB and system design. He conducts on-site private training courses for high technology companies and also has taught courses for UC Berkeley's extension program as well as industry trade-show technical conferences. In addition, he provides consulting services to top manufacturers of Internet and server products. He is the author of two leading books on high speed design disciplines, "Right The First Time, A Practical Handbook on High Speed PCB and System Design, Volumes 1 & 2". He also the author and publisher of a quarterly newsletter, Current Source, that is dedicated to discussing ongoing topics of concern in the high speed design industry.
He is the author of two leading books on high speed design disciplines, "Right The First Time, A Practical Handbook on High Speed PCB and System Design, Volumes 1 & 2". Ritchey holds a B.S.E.E. degree from California State University, Sacramento where he graduated as outstanding senior. In 1998, he was profiled by EE Times, as "the high-speed design ratchet man". In 2004, Ritchey began contributing a regular column, "PCB Perspectives" which appears once a month in EE Times.

Refreshments: Light Dinner and beverages will be served for a fee. Coffee, tea, and snacks are served free of charge.

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$$\nabla \times \vec{H} = \frac{\partial \vec{D}}{\partial t} + \vec{J}$$

$$\nabla \bullet \vec{D} = \rho$$

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