Google

Automated Design Rule Check for EMC Design

High Level Overview of DRC tools

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Outline

- What are Design Checking Rules (DRC) tools ?
  - Are they useful?
- Evaluation of DRC tools
  - Evaluation Criteria
- DRC Workflow Example and Possible Automation
- Design Guidelines / EMC Rules Parameter Optimization
  - Some Examples
- Conclusions and Recommendations

DRC Tools Overview

DRC review

- Time consuming model set-up
- False violations
- Identifying critical nets
- Specifying naming conventions for the tool to recognize the type of signal “gnd”, “***_N and ***_P”
- Automation of the DRC

Manual board review

- Process is time consuming and prone to errors. This is particularly true in PCB with many layers and hundreds of nets
- No need to formally identify critical nets
- Naming conventions are in general self explanatory: gnd, clk, P5V, etc..
- Has to be repeated at each board review

DRC tools is useful to check PCB revisions according to predefined design guidelines and parameters.

Evaluation of DRC tools

Tool Evaluation Criteria

- Number and type of rules supported
- Setup time
  - Selecting rules & nets
- Tool effectiveness
- Possible automation
  - Not using GUI
- Learning curve
  - User friendliness / GUI
- Support, training
  - Accessibility to training
  - Response time of support
- Loading time
- Format of board file supported (.brd, odb++, ...)
- 2D/3D Viewer
- Price

Tool Effectiveness

- False or missing violations
- Feasibility to add new rules
  - Time required and Complexity
  - Rule Customization
- Violation visualization and explanations
- Integration with PCB Layout tools
- Saving rule checking settings for the revised board
- Run time

The Typical Rule Checking Workflow

Select and tag nets (can be time consuming)

- Signal specification, net class, differential net, clock net

Select and tag components

- IC, clock driver, oscillator, capacitor type, passive type, connector

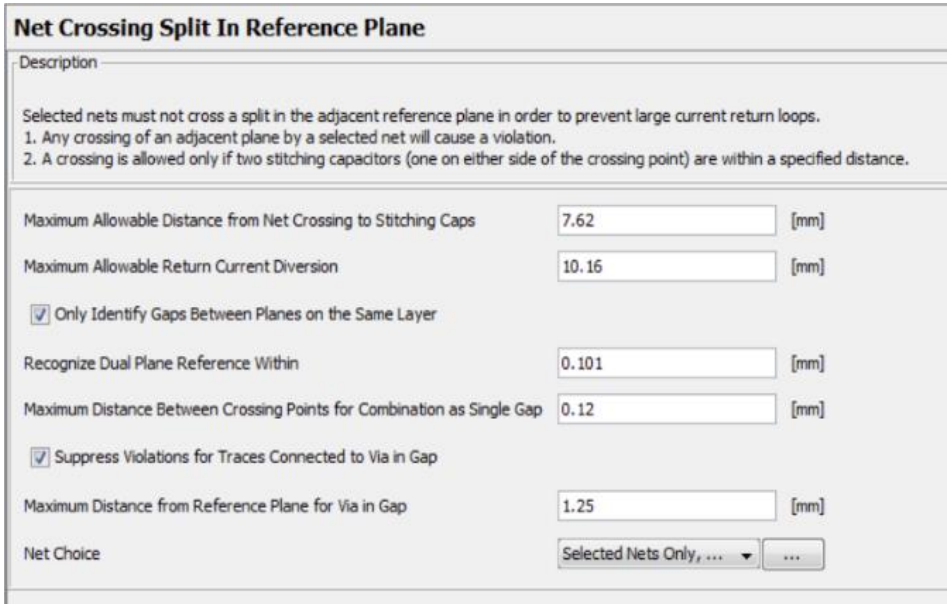
Manage rule set and parameters (may require simulations, EMC experience)

- Signal Reference, Wiring/Crosstalk, Decoupling, Placement, Net & Via Integrity

Start and view violations, discard false violations

- Press the Start button and wait for the EMC & SI/PI violations to be listed

Example of Managing rules and parameters



Rule Definition Example in a DRC tool

What the Maximum Allowable Distance from Net Crossing to Stitching Caps should be? Why 7.62 mm?

Is a stitching cap going to work at high frequency?

What is the ESL of the stitching cap?

Example of false violations: reset lines, USB lines crossing gaps if USB will not be used in typical operating conditions (diagnostic and recovery mode)

DRC Automation Opportunities

- NET Selection and tagging:
  - Signal specifications, net classes, differential nets, clock nets in most tools depend on naming conventions. A net database with naming conventions is convenient for automated process
- Manage rule set and parameters
  - Checking all rules results in hundreds of violations, lots of false or non-critical violations, difficulties in routing. Rules priorities should be used
  - Rule parameters should be customized based on nets' types
- Smart Rules
  - Automatically check violations to make sure that they apply considering other design factors:
    - E.g. critical nets routed too close to PCB edge but the PCB has via stitching. This should not be a violation.
    - E.g. critical nets routed close to a series of antipads that effectively create a slot. This should be a violation

Design Guidelines Using Simulations

- DRC tools requires engineer to define constraint values for rules
- Theoretical design rule recommendations might not be optimal for the specific type of board designs
- Rule of thumb suggestions are not sufficient in practical designs
- Simulations may have to be used to study the effects of the design rules in a specific design
    - Example of impact of design guideline parameters on EMC performance

Example of Design Guidelines Parameters using simulations

- Stitching vias around the board
  - Benefit of the stitching vias
  - Optimal distance between the stitching vias

- High speed signals near the apertures
  - Impact on emissions
  - Design recommendations to reduce the aperture effects

Stitching Vias Around the Board

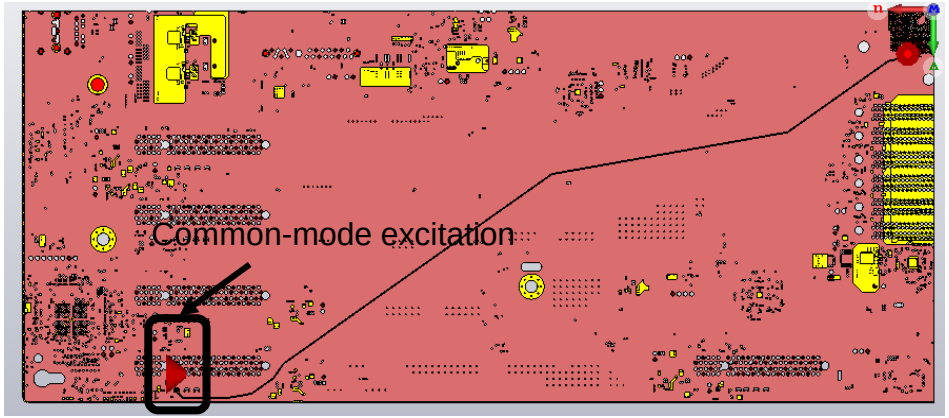
Board edges should be stitched to reduce fields leakage from the edges.

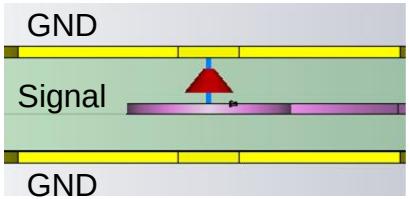
Ideally board should be plated, but

- Might not be beneficial
- EMI from other sources could dominate
- Specially when mechanical holes are not shielded

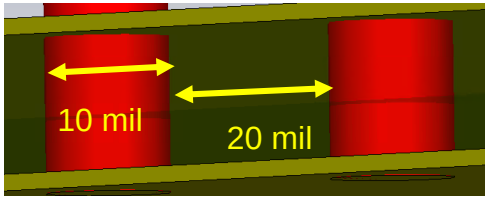
Objectives:

- Evaluate the potential EMC benefits while using stitching vias
- Propose optimal stitching via separation



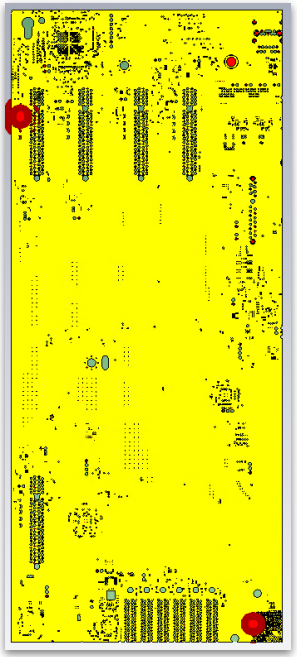


Stack-up

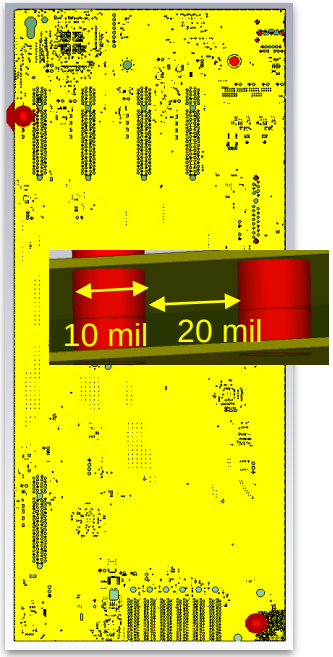


Edge stitching vias

Effect of the Stitching Vias

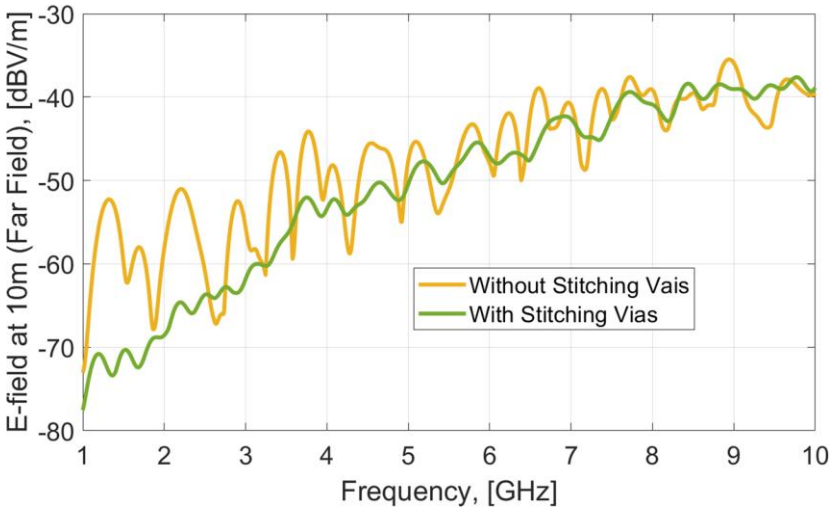


Original design
without stitching vias

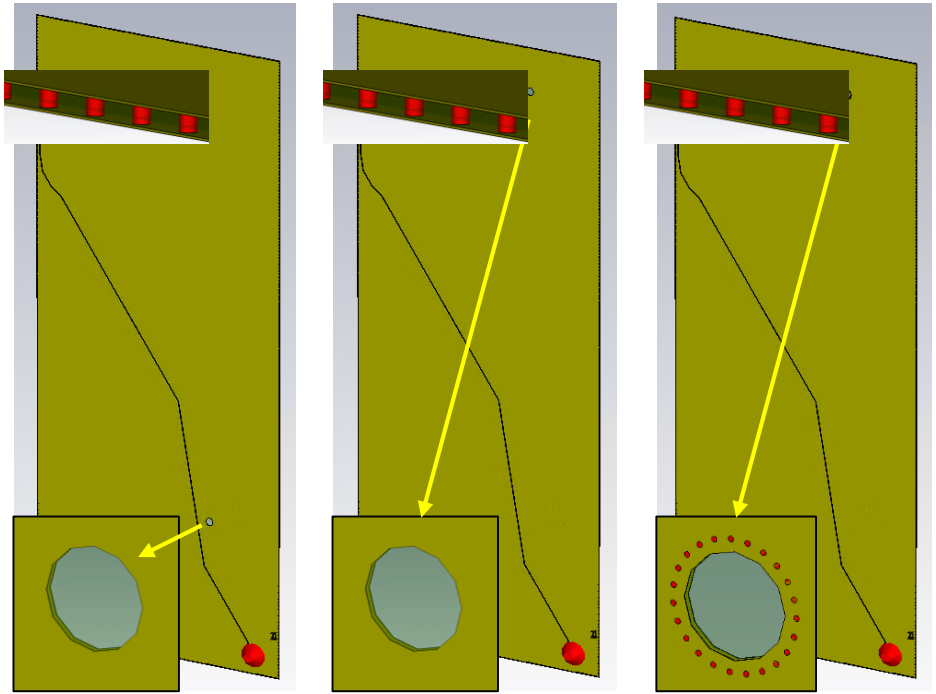


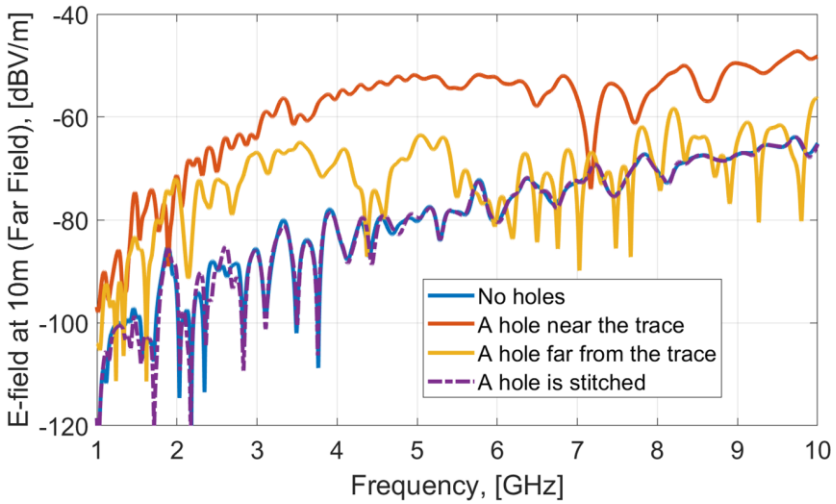
Original design
with stitching vias

- Stitching vias does not affect emissions above 5 GHz
- Emissions are dominated by the holes and/or exposed sources (traces, components,...)



Design Recommendations for Effective Stitching Vias



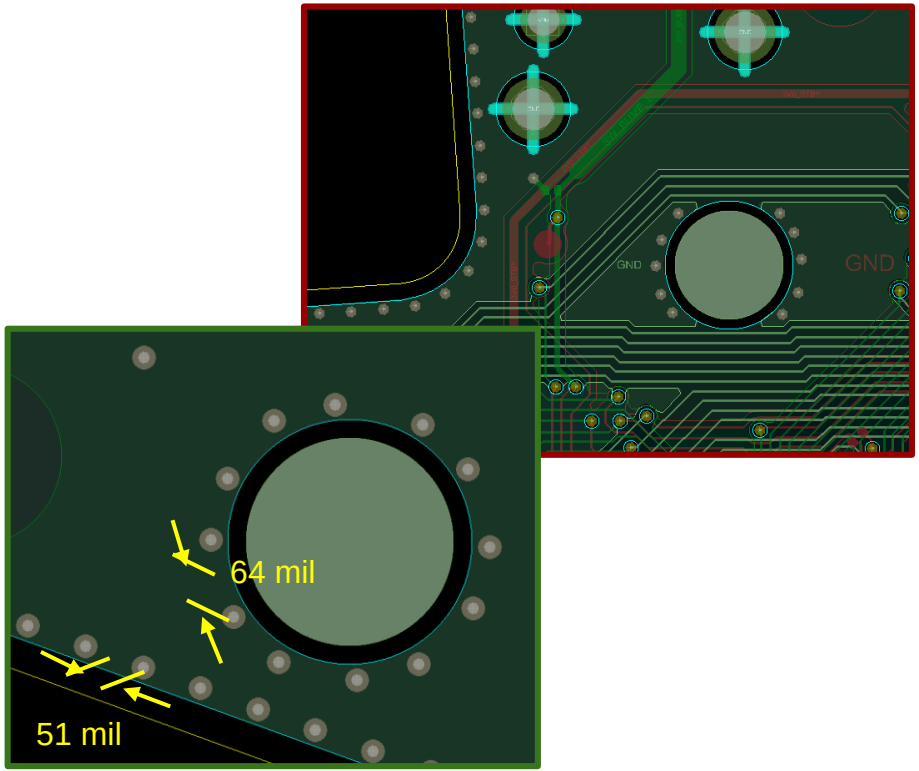


- Emissions are dominated by holes radiations
- Apertures in proximity of traces will radiate more
- Stitching Vias need to be placed around edges and apertures

Recommendations: Vias Stitching

- Emission level depends on
  - Placement proximity of the hole with the signal trace
  - Grounding via density and placement

- The edge stitching is effective when, via stitching around edges and holes are the same



High Speed Signal Near the Aperture

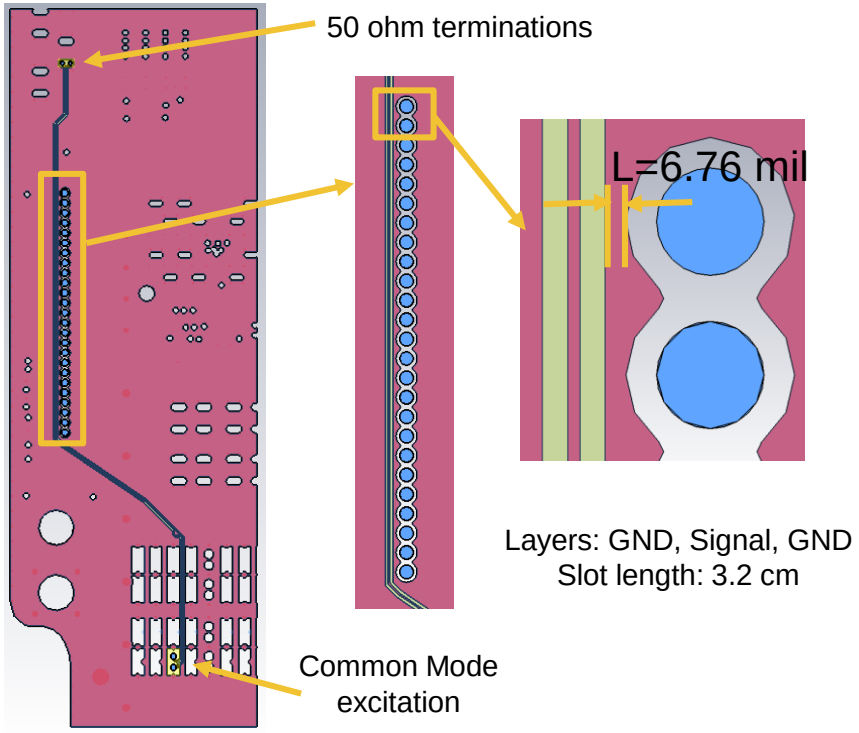
Differential pair near the aperture

Radiation mechanism:

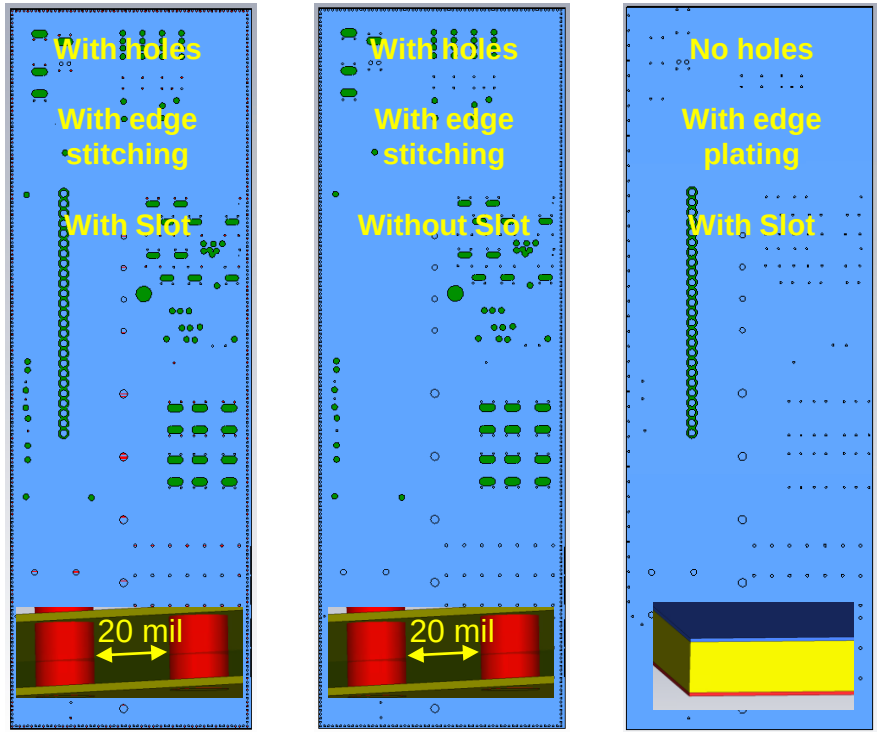
- High speed signal couples to nearby apertures
- Apertures resonate like slot antennas
- Currents escape through apertures and radiate from the edges of a board

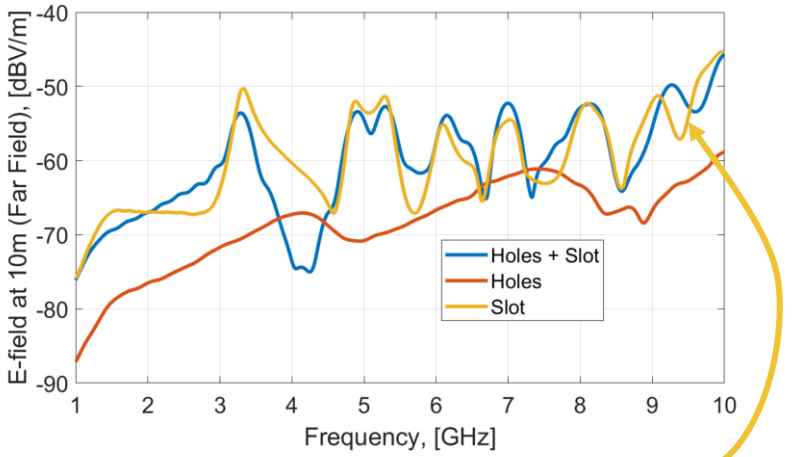
Objectives:

- Investigate impact of the aperture on emissions
- Propose design recommendations to reduce aperture effects



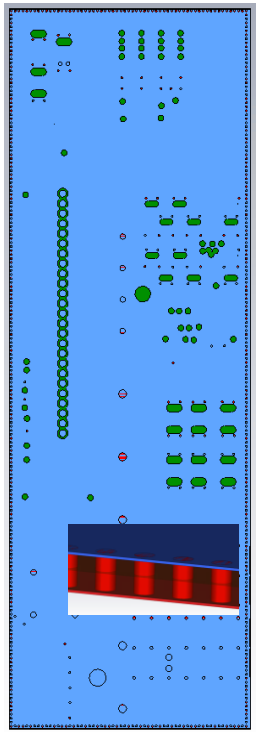
Effect of the Apertures and Holes

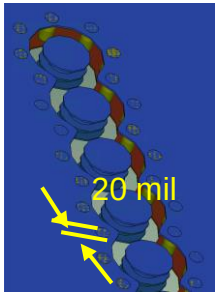




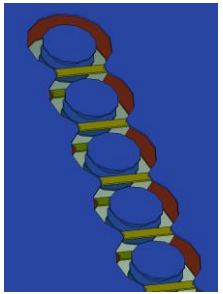
- Emissions due to slot dominate
- Half-wavelength slot resonance at 3.3 GHz
- 4.8 GHz, 5.2 GHz, 6.1 GHz… are due to board dimensions

Design Solutions

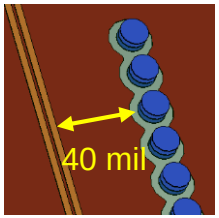




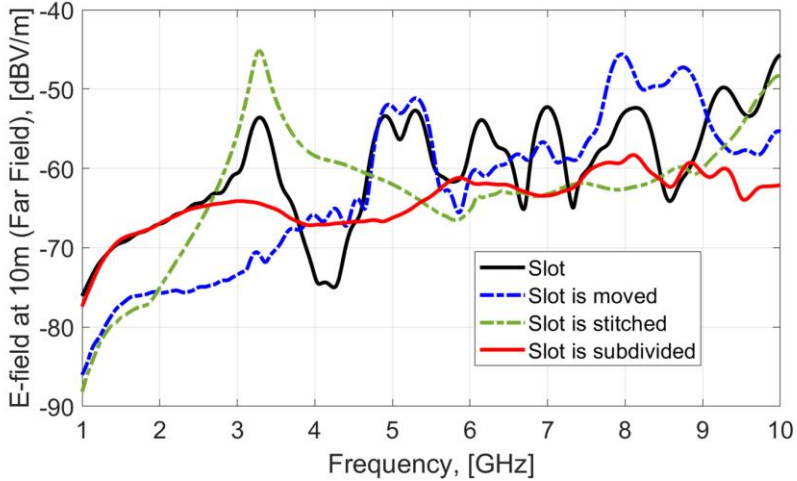
Place stitching vias around the slot



Subdivide the slot with GND traces



Move the slot away from the Trace



Slot is subdivided:

- Current goes around the vias and does not spread to the board edges
- There is no slot, so $\lambda/2$ resonance at 3.3 GHz is gone

Recommendations: A Trace Near an Aperture

Highly recommended

- Subdivide the slot

Recommended

- Place stitching vias around an aperture

Optional, but preferable

- Move an aperture away from the high speed trace

Conclusions and Recommendations

- DRC tools can be very effective and save significant time in PCB review
  - Rule priorities and design parameters for the rules have been defined
  - Many PCB revisions need to be reviewed
  - Hundreds of nets, many layers
  - Database of nets and naming conventions need to be defined only one time

- Automation
  - The process can be automated to same extent
    - Rule customization (“Smart” rules, avoiding false violations, avoiding missing violations)
    - Integration with PCB layout tools (for violations checking and visualization)
    - Integration with simulation tools to define design parameters