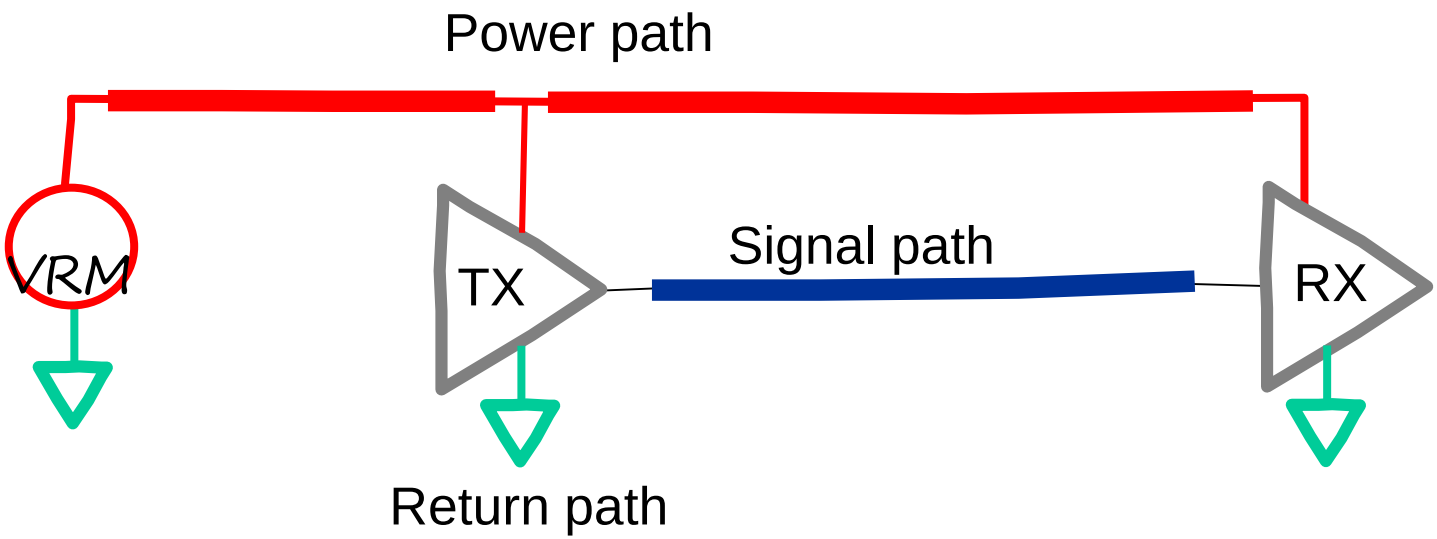
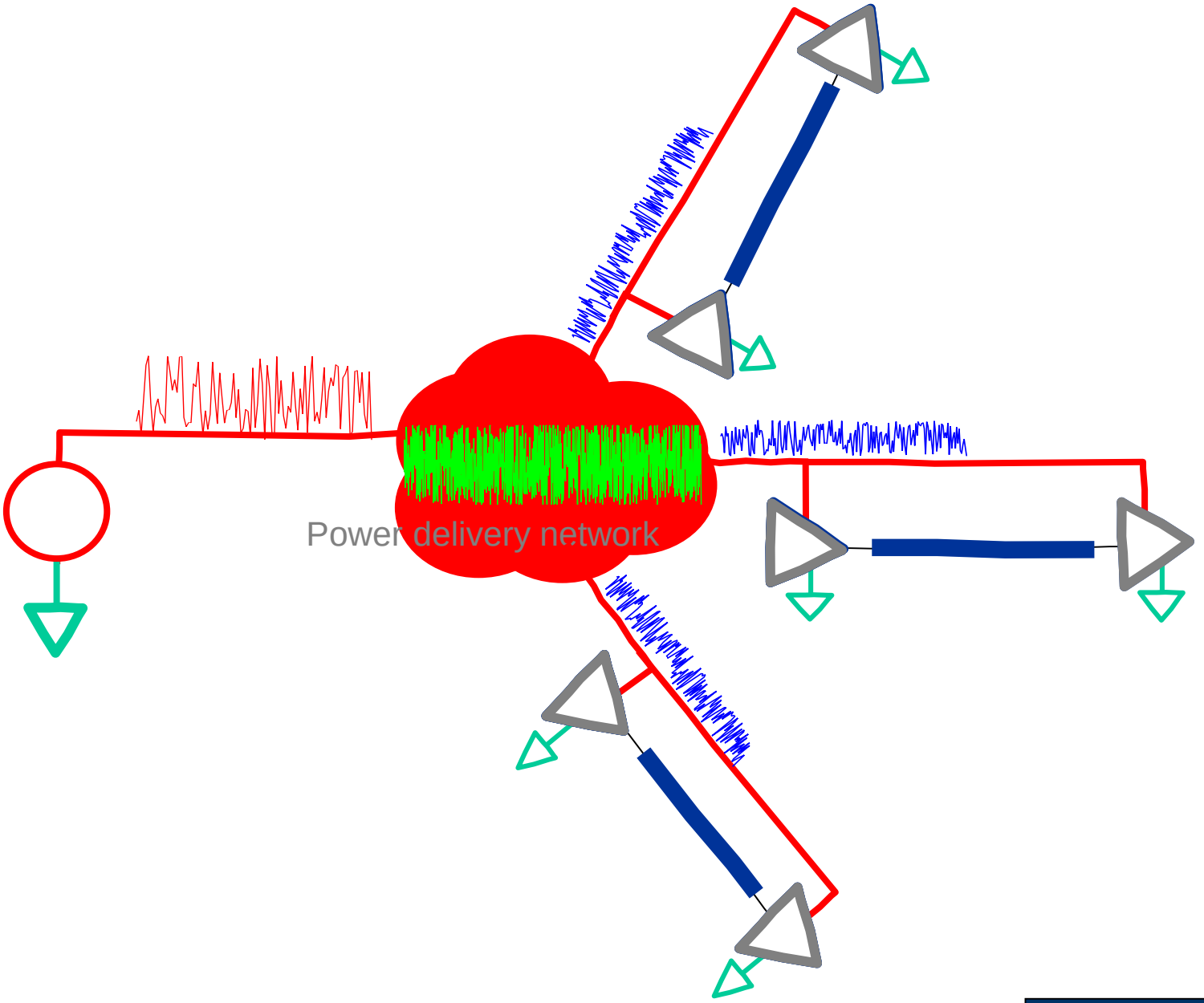
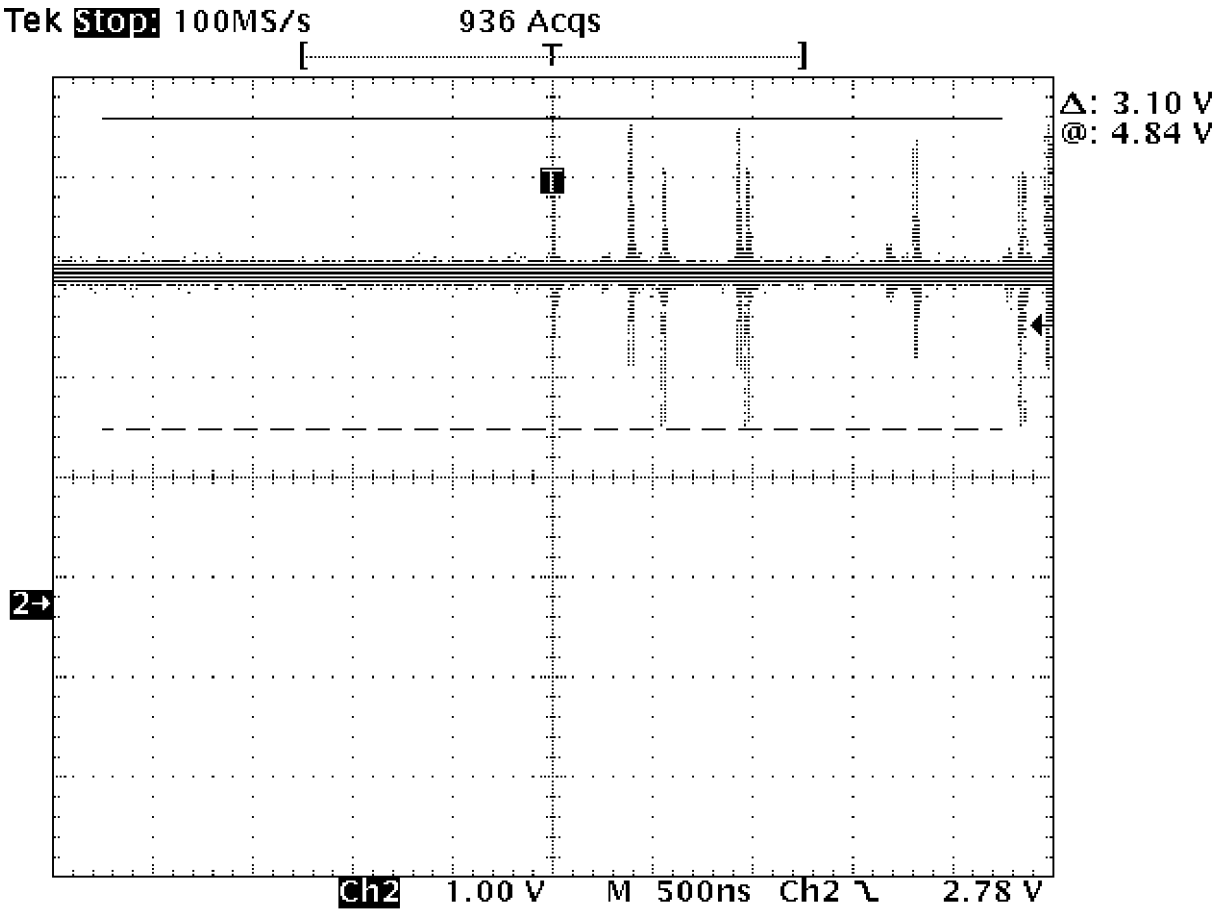
Fundamentals of Power Integrity with Current Design & Analysis Practices

Ihsan Erdin

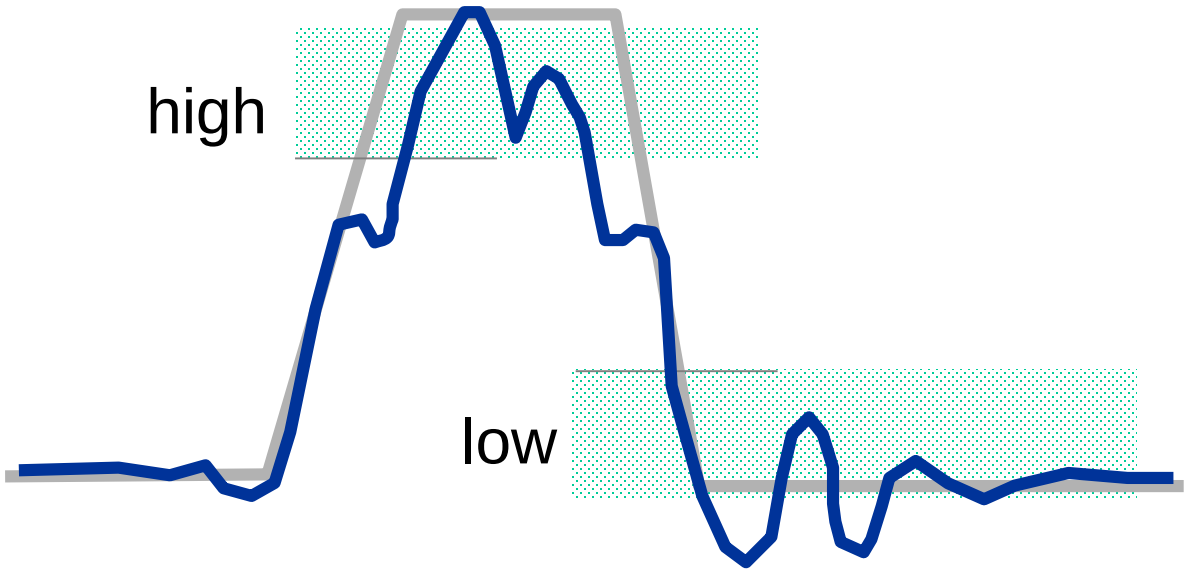

Power path
VRM
TX
Signal path
RX
Return path


Power delivery network

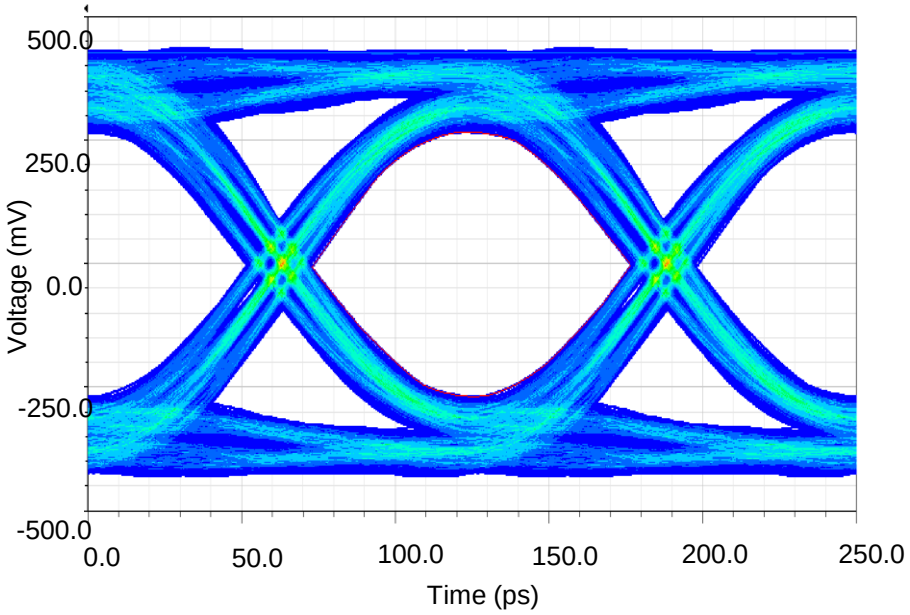
Power Noise on 3.3V Supply

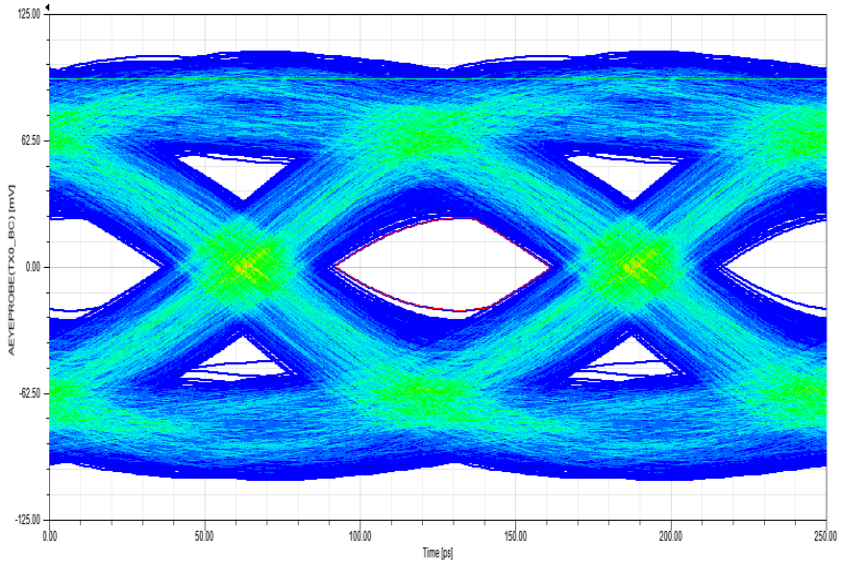


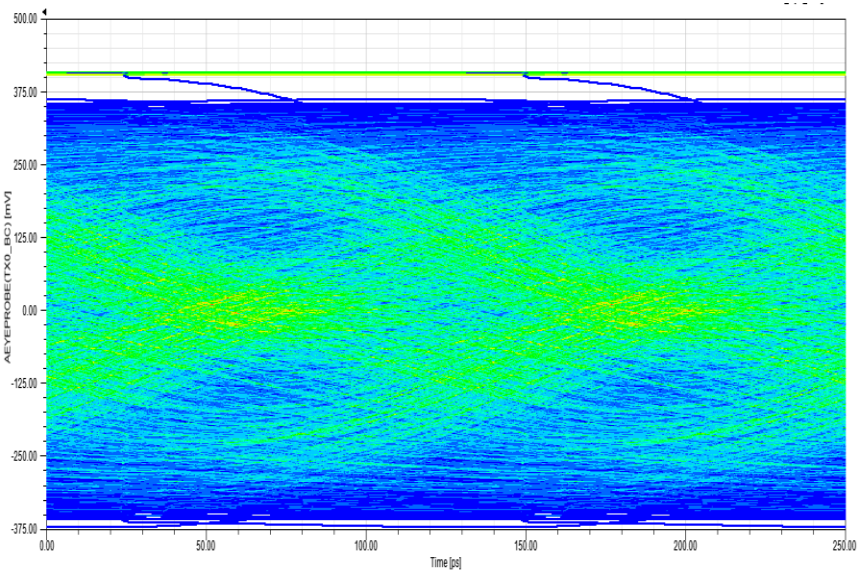
Logic Noise Margins



Receiver Eye Diagram



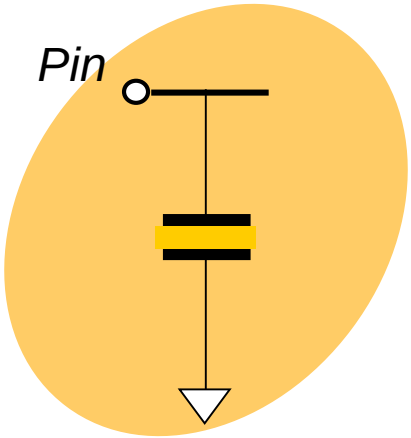


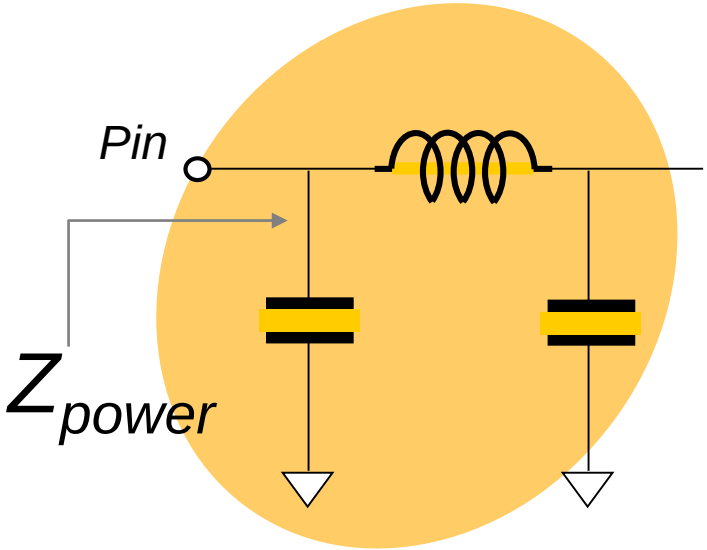


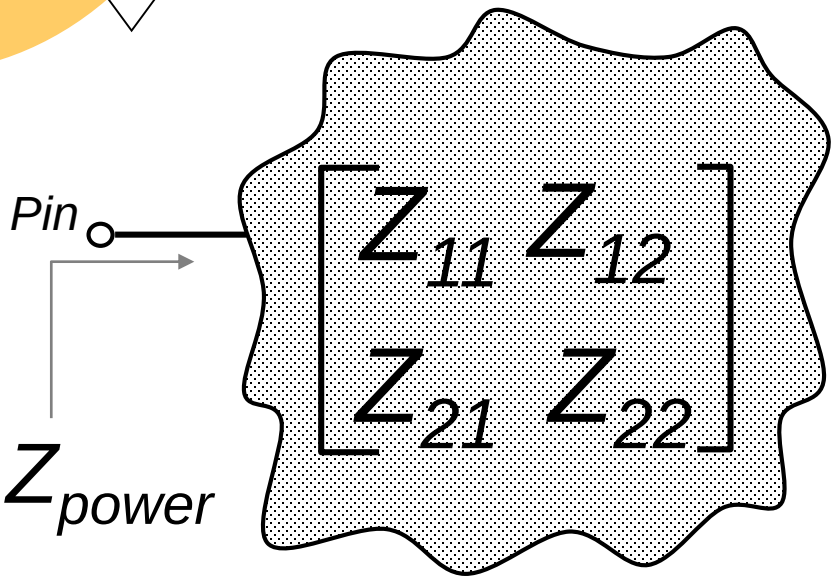
Analysis Parameters

$$V_{noise}(s) = Z_{power}(s) I_{load}(s)$$

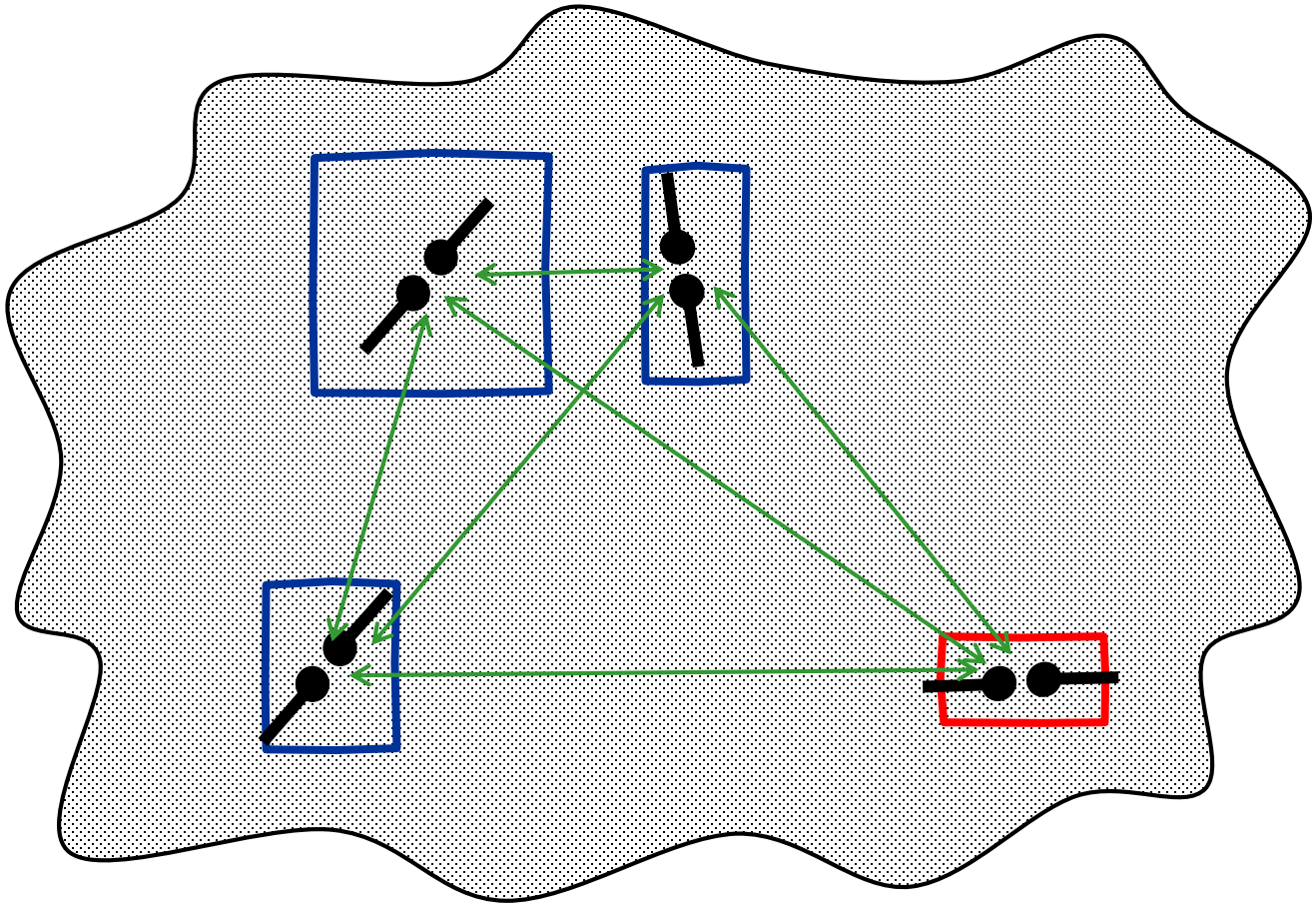
PDN Characterization



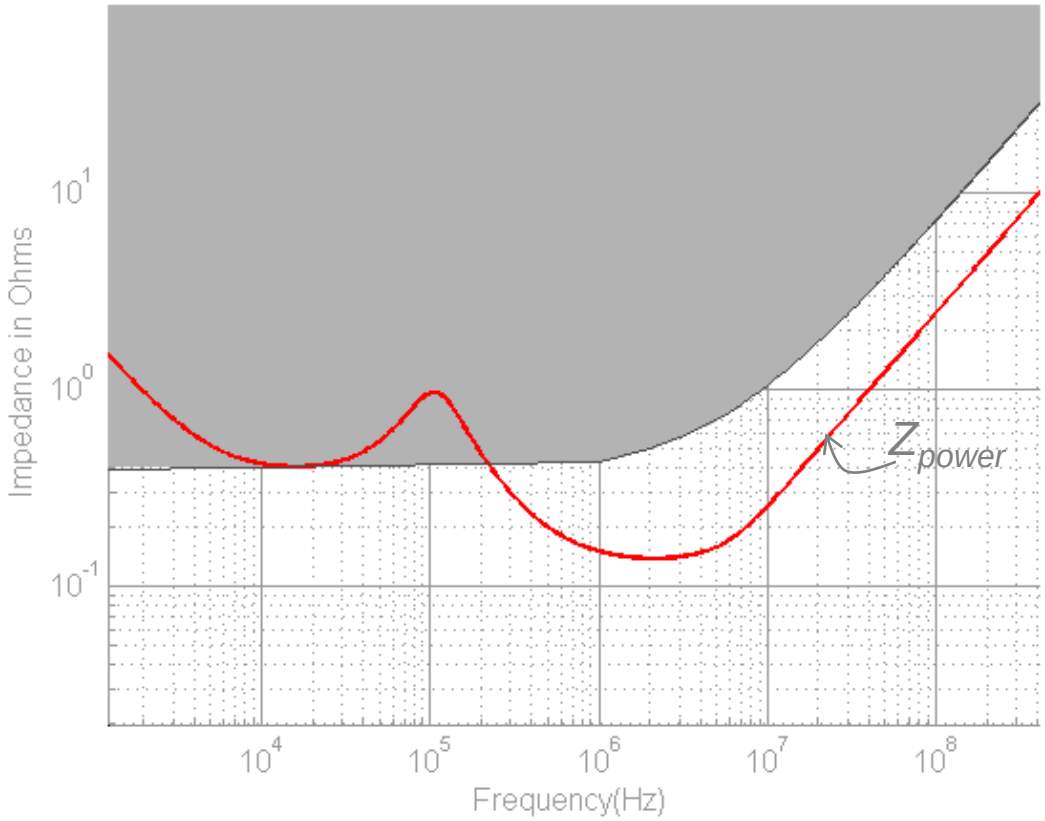




Planar Circuit Analysis

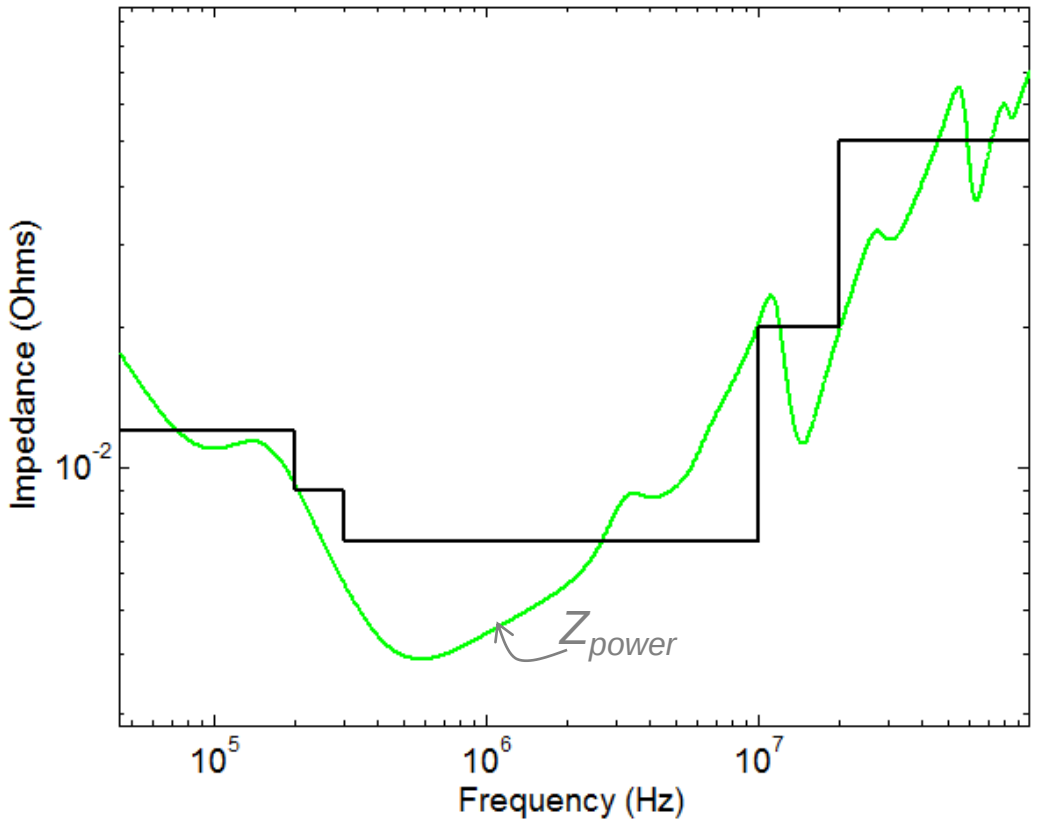


Target Impedance Mask

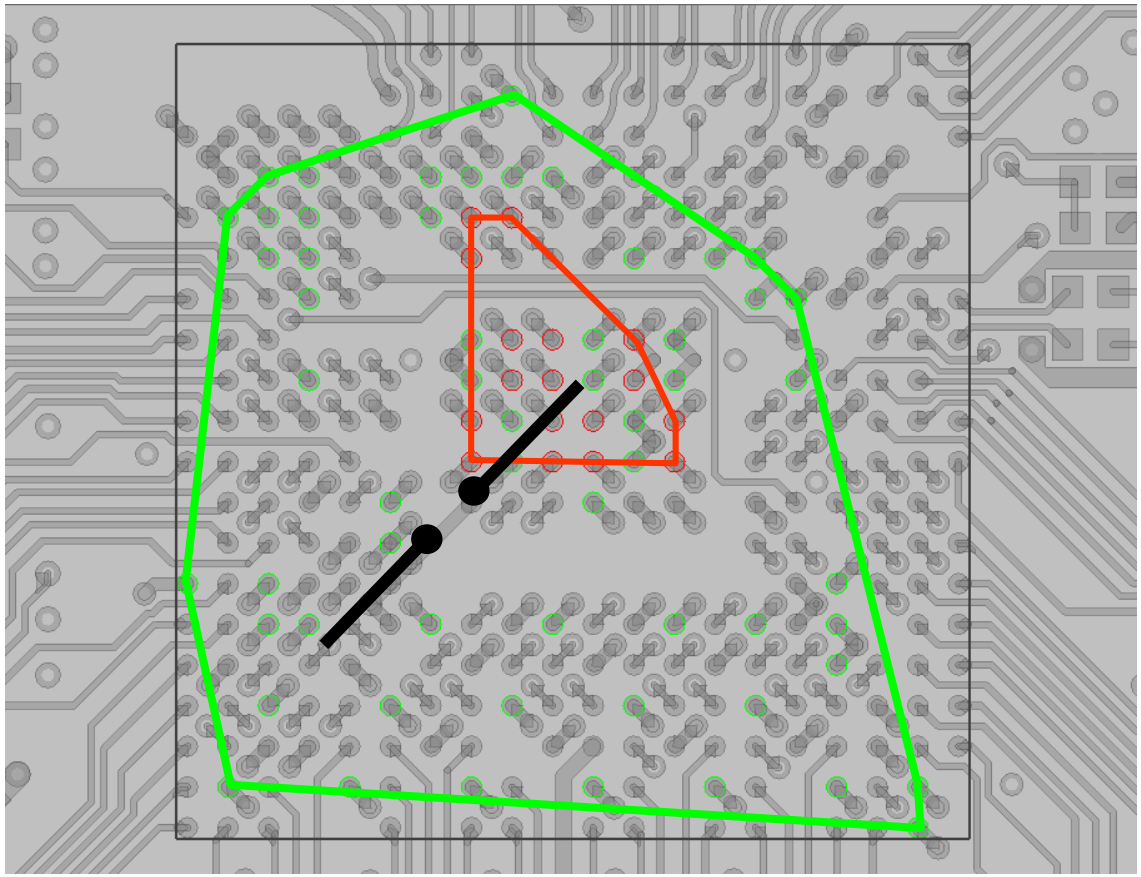


$$Z_{target} \leq \frac{V_{noise}(s)}{I_{load}(s)}$$

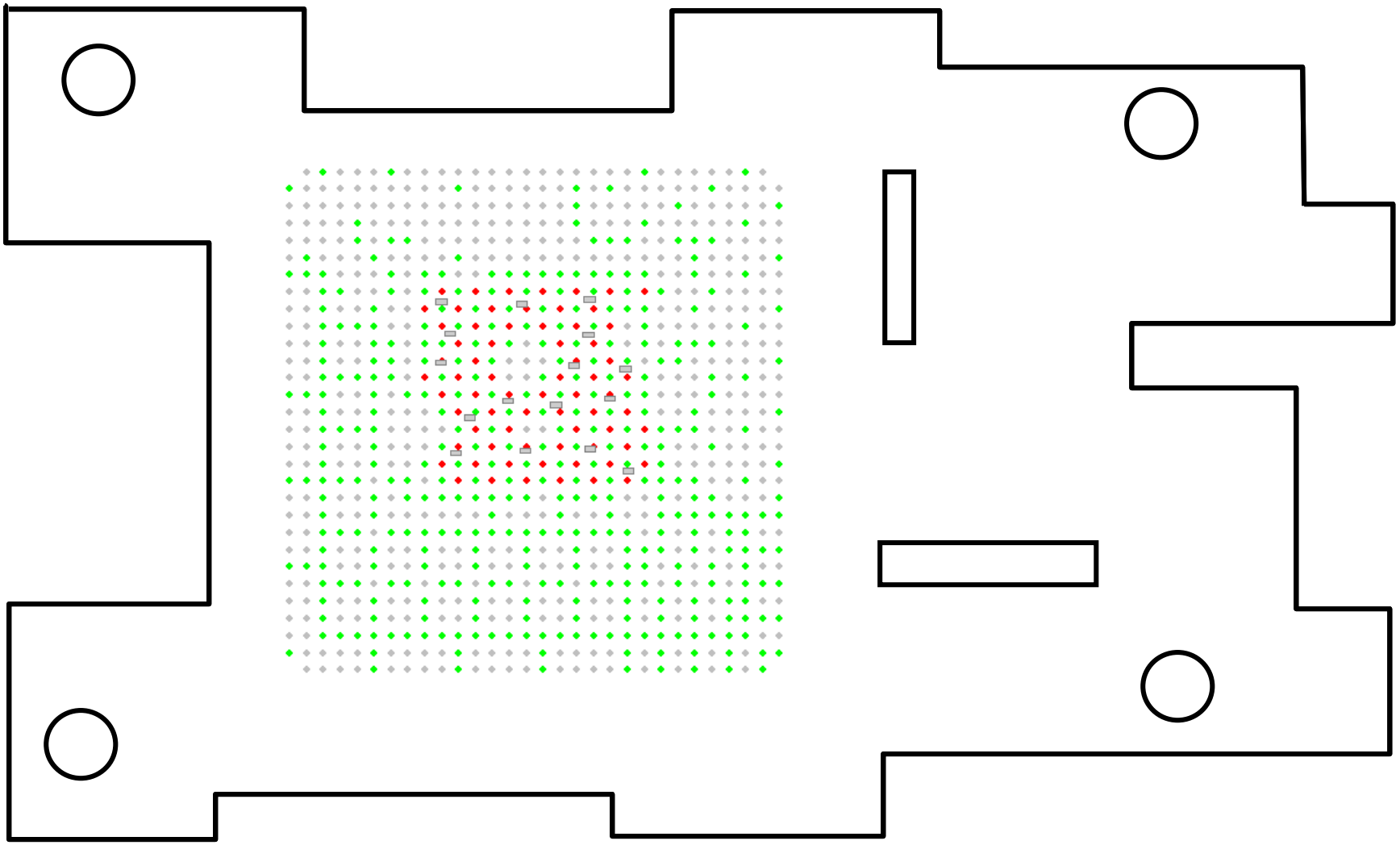
Vendor Provided Impedance Mask

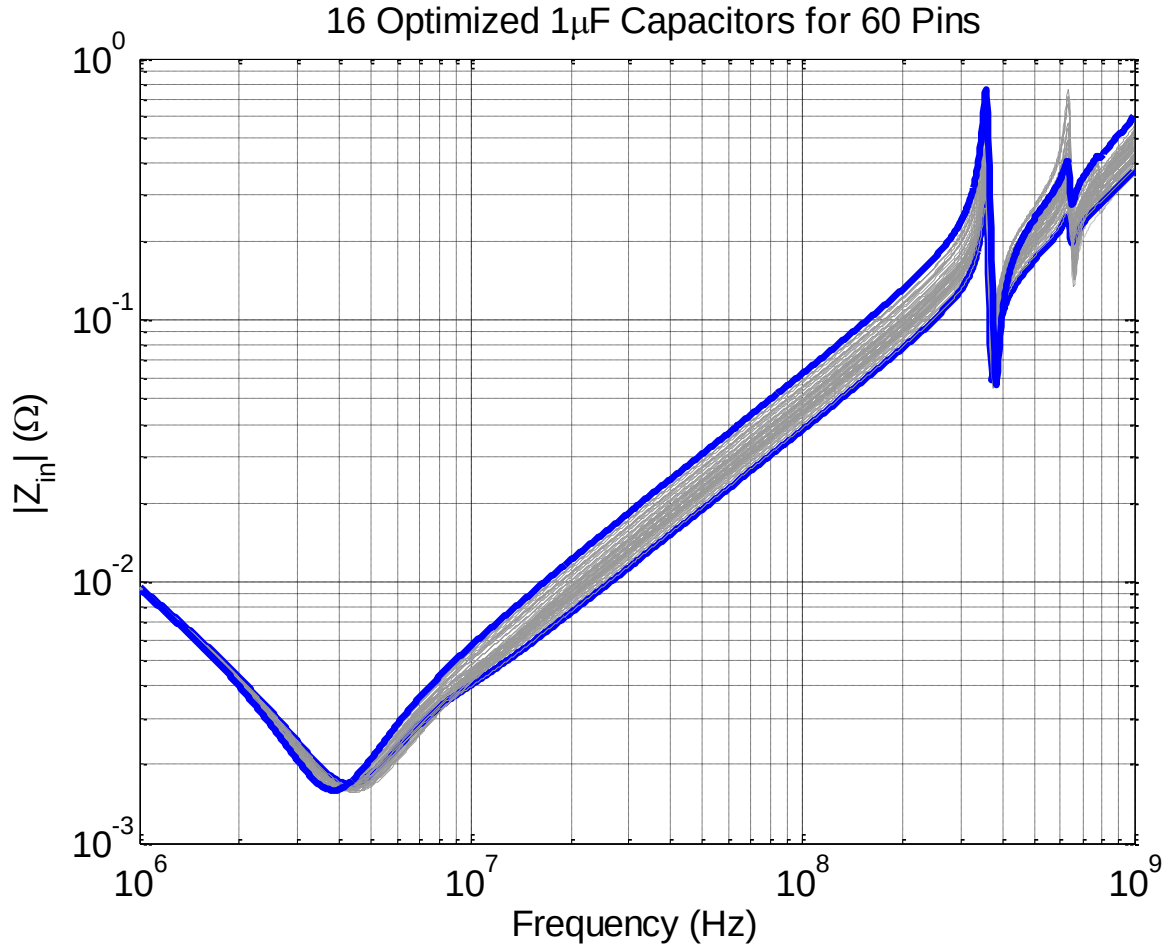


Pin Groups and Representative Port



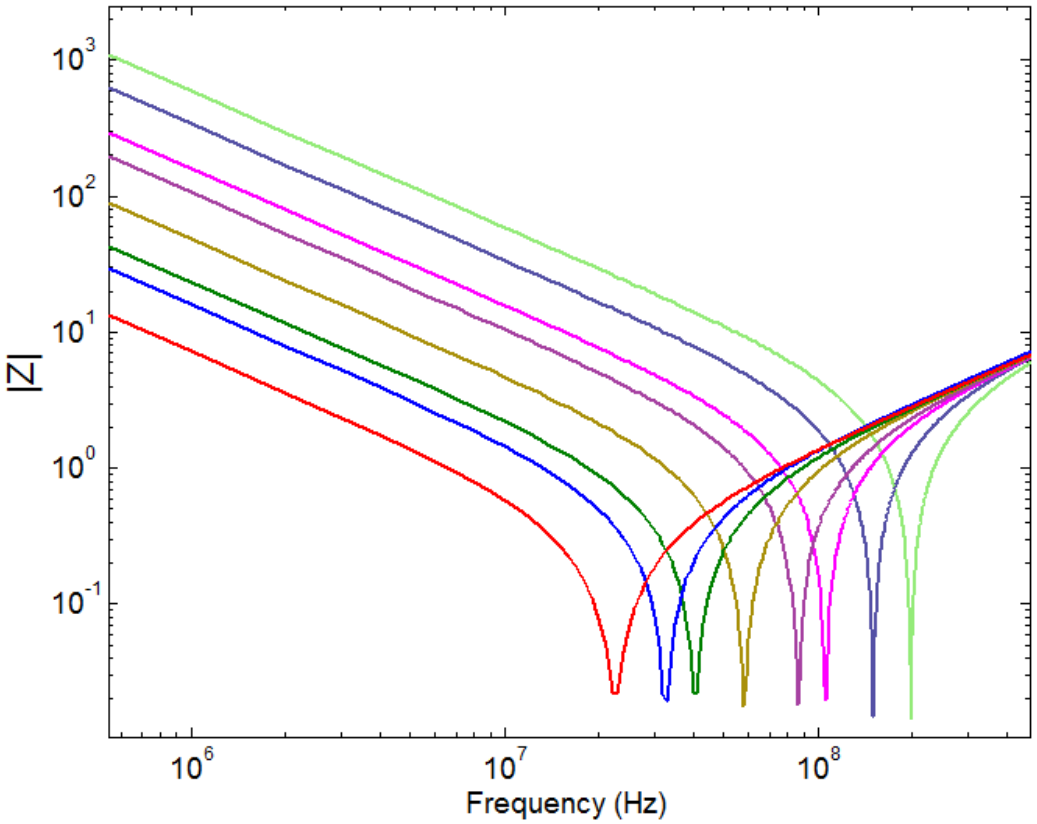
Practical Example



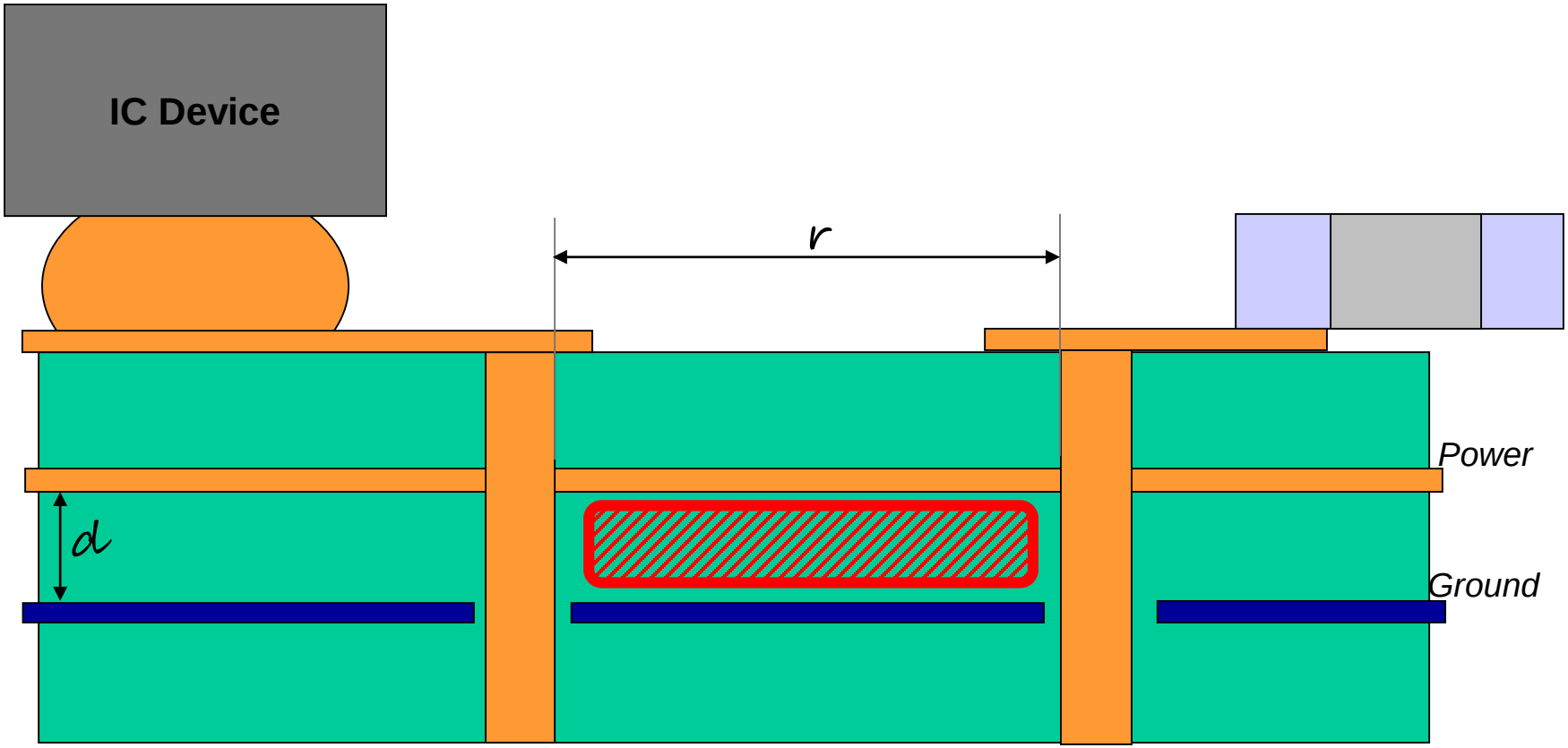


Ihsan Erdin, Ram Achar, "Multipin Optimization of Decoupling Capacitors on Practical Printed Circuit Boards," *2018 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS),* Dec. 2018, Chandigarh, India

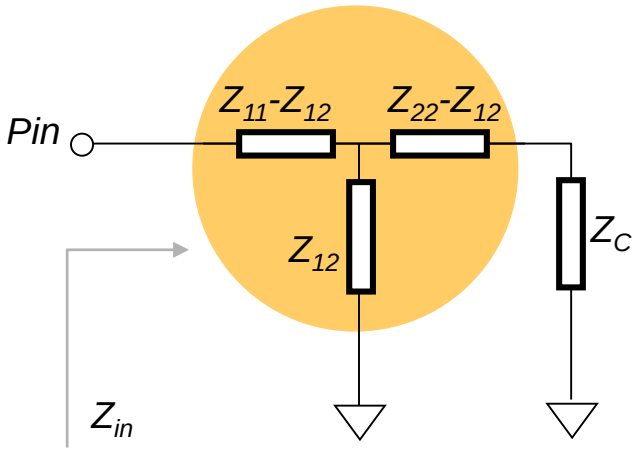
Self-resonance of decoupling



$$Z_c = R + sL + \frac{1}{sC}$$



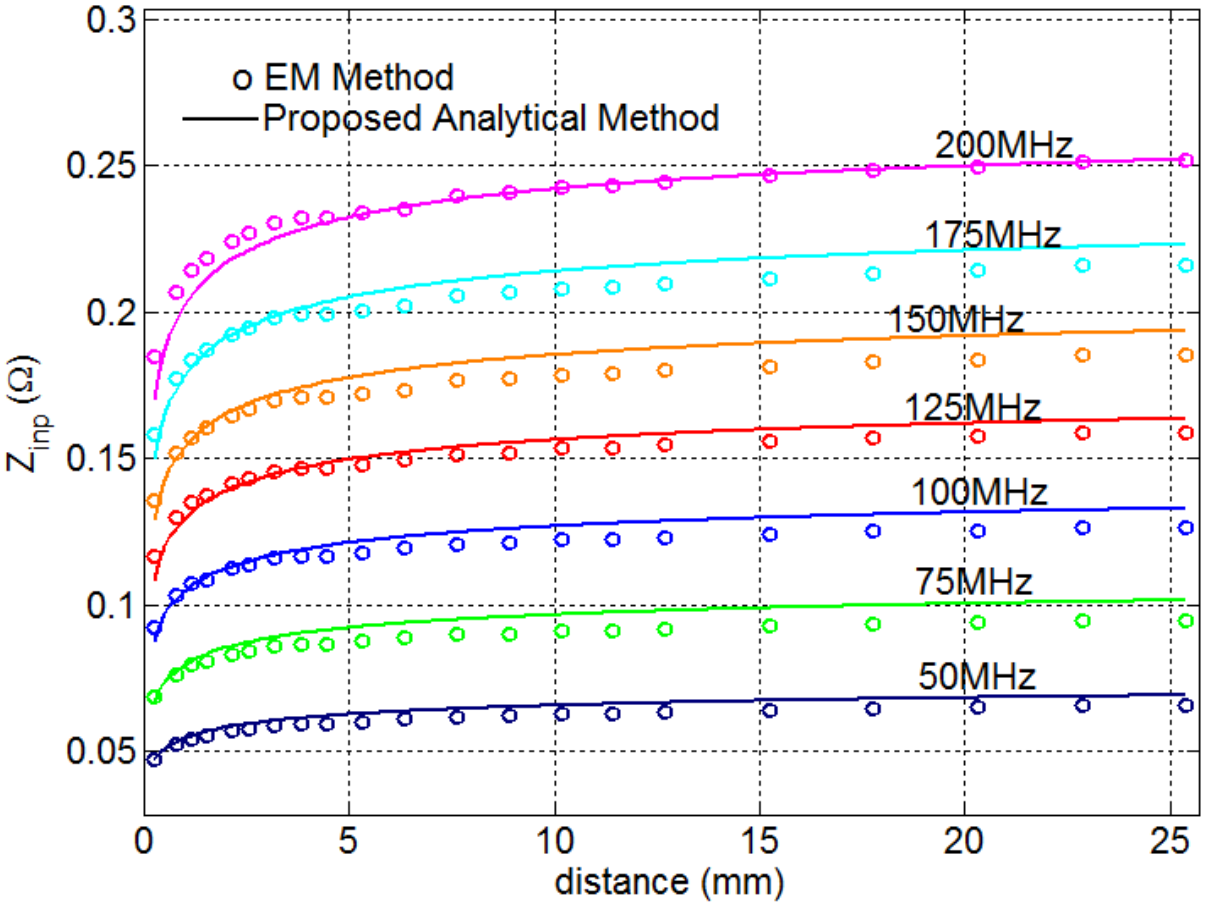
Spread Inductance



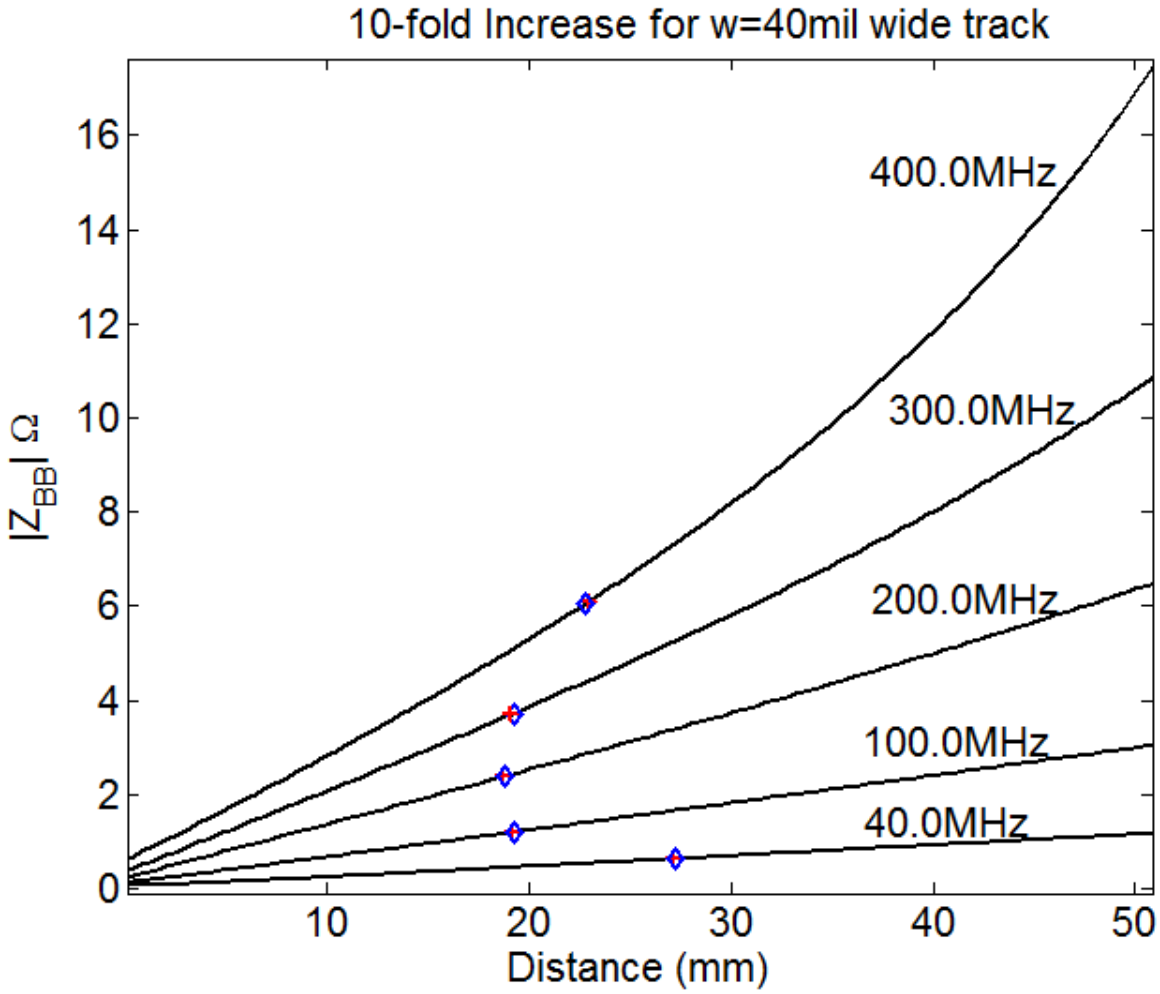
$$Z_{in}(s) = Z_{11}(s) - \frac{Z_{12}^2(s)}{Z_{22}(s) + Z_C(s)}$$

Ihsan Erdin, Ram Achar, "Pin-Capacitor Spacing As A Design Guide To Power Delivery Networks," *2017 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization for RF, Microwave, and Terahertz Applications (NEMO),* pp. 70-72, *May* 2017.

Impedance Increases with Spacing



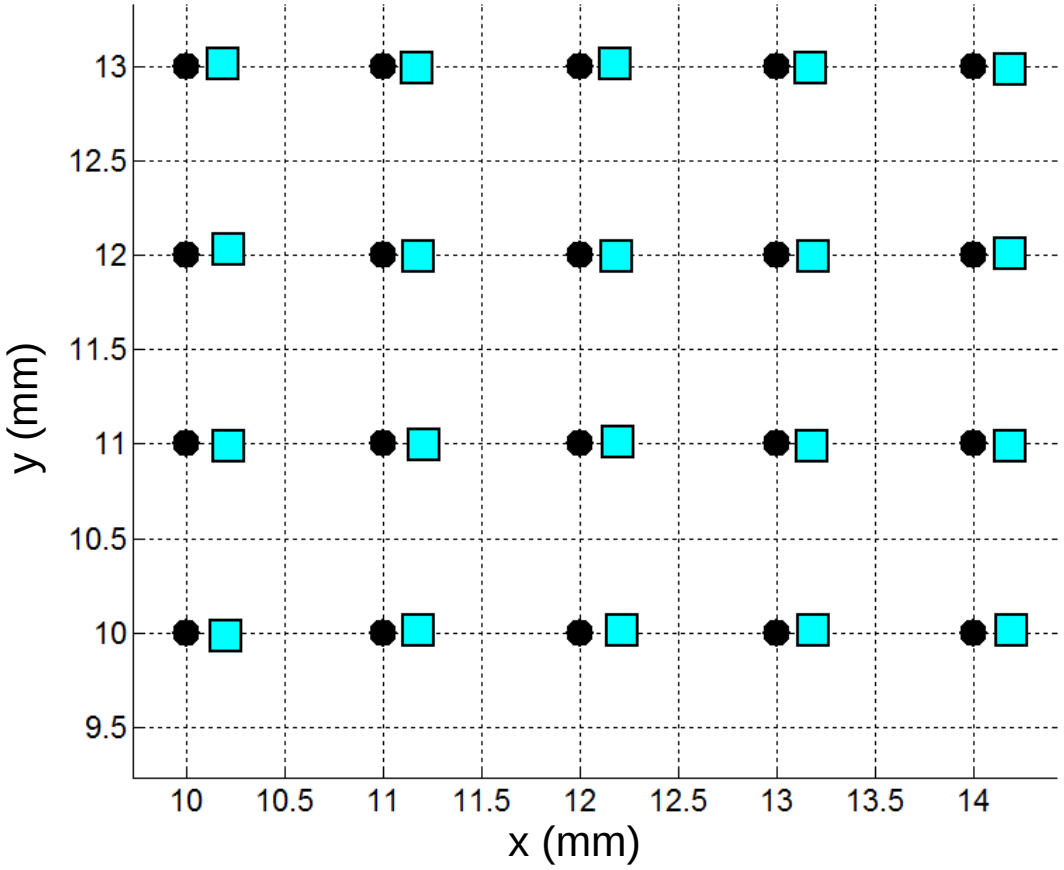
Ihsan Erdin and Ram Achar, "Efficient Decoupling Capacitor Placement Based on Driving Point Impedance," *IEEE Trans. Microwave Theory and Tech.,* vol. 66, pp. 669-677, Feb. 2018.



Ihsan Erdin and Ram Achar, “Analysis of Decoupling Capacitors on Power Transmission Lines," 2018 *IEEE APEMC*, May 2018.

Calculate Required Total Capacitance

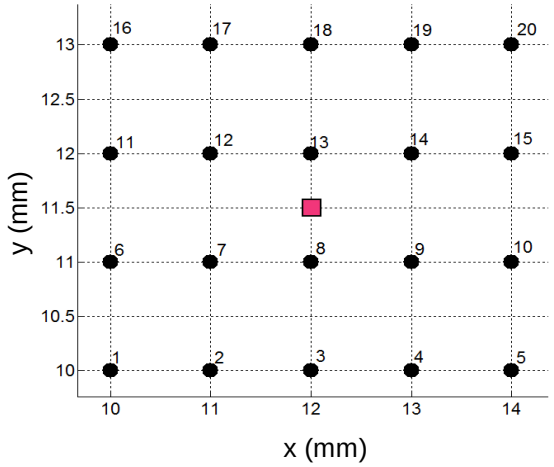
$$C_{total} = \frac{I_{load}(s)}{sV_{noise}(s)}$$

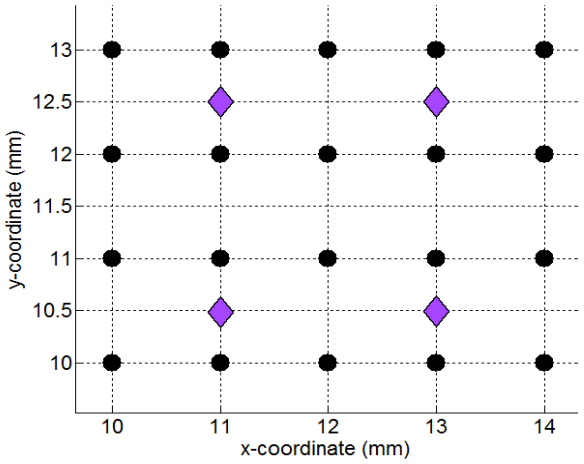


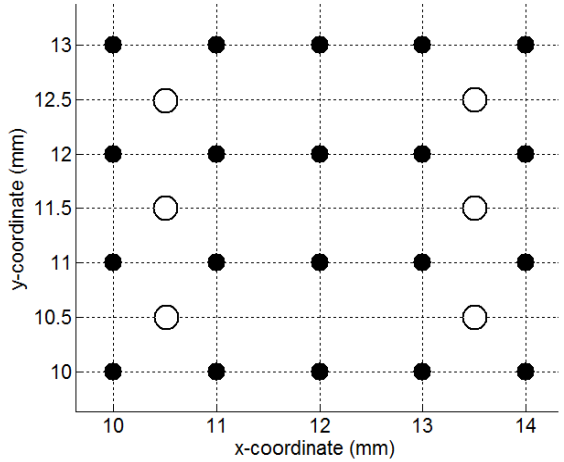
20-pin BGA footprint

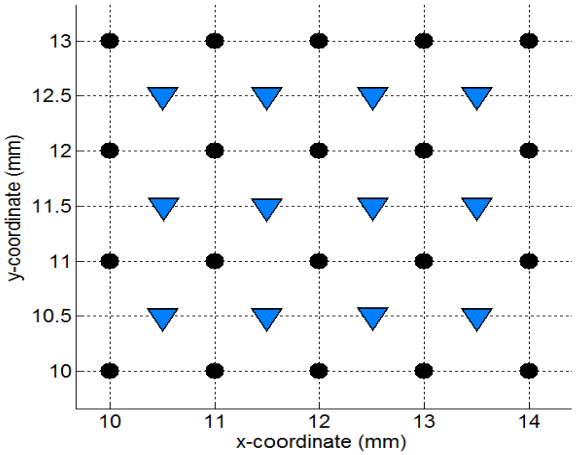
A New Figure of Merit for Capacitor Placement

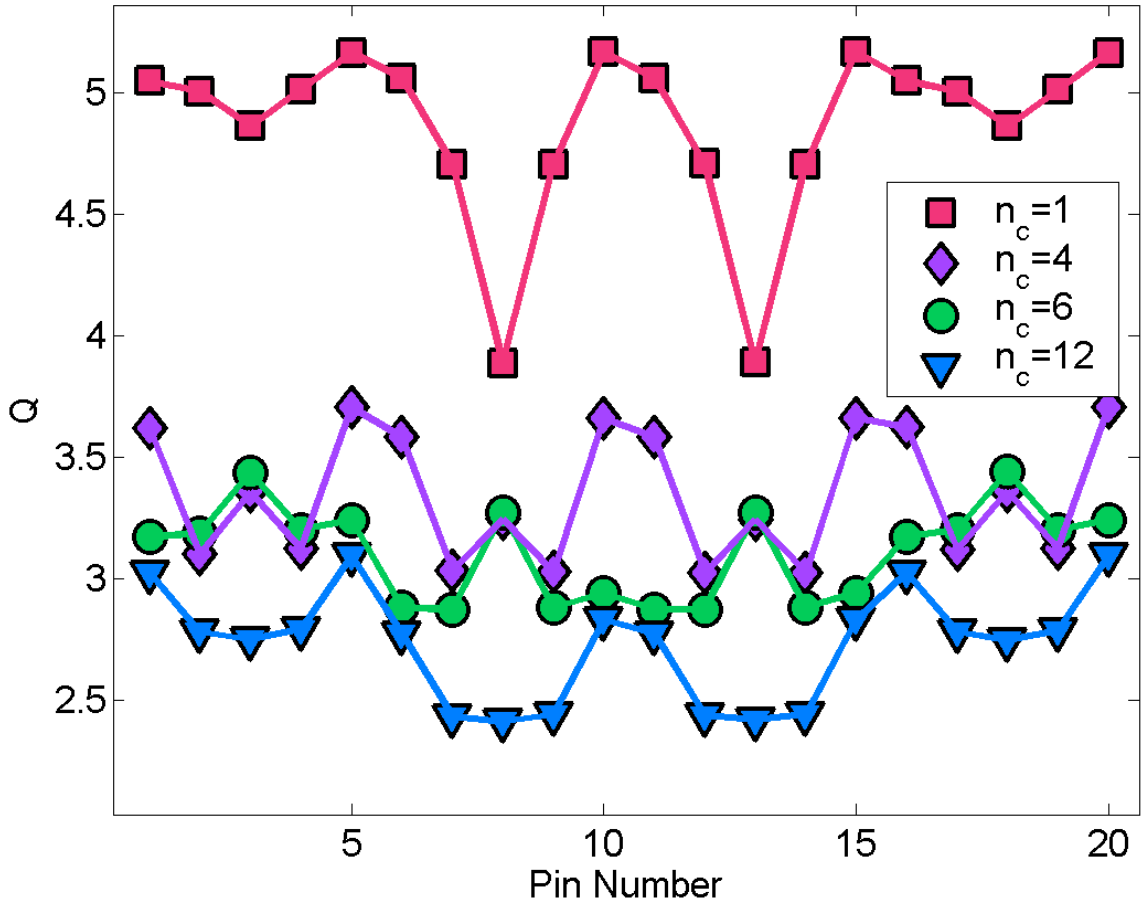
$$Q_i(s) = \left| \frac{Z_{ii}(s,r)}{Z_{ii}(s,r_0)} \right|$$


16
17
18
19
20
11
12
13
14
15
6
7
8
9
10
1
2
3
4
5
13
12.5
12
11.5
11
10.5
10
10
11
12
13
14
y (mm)
x (mm)

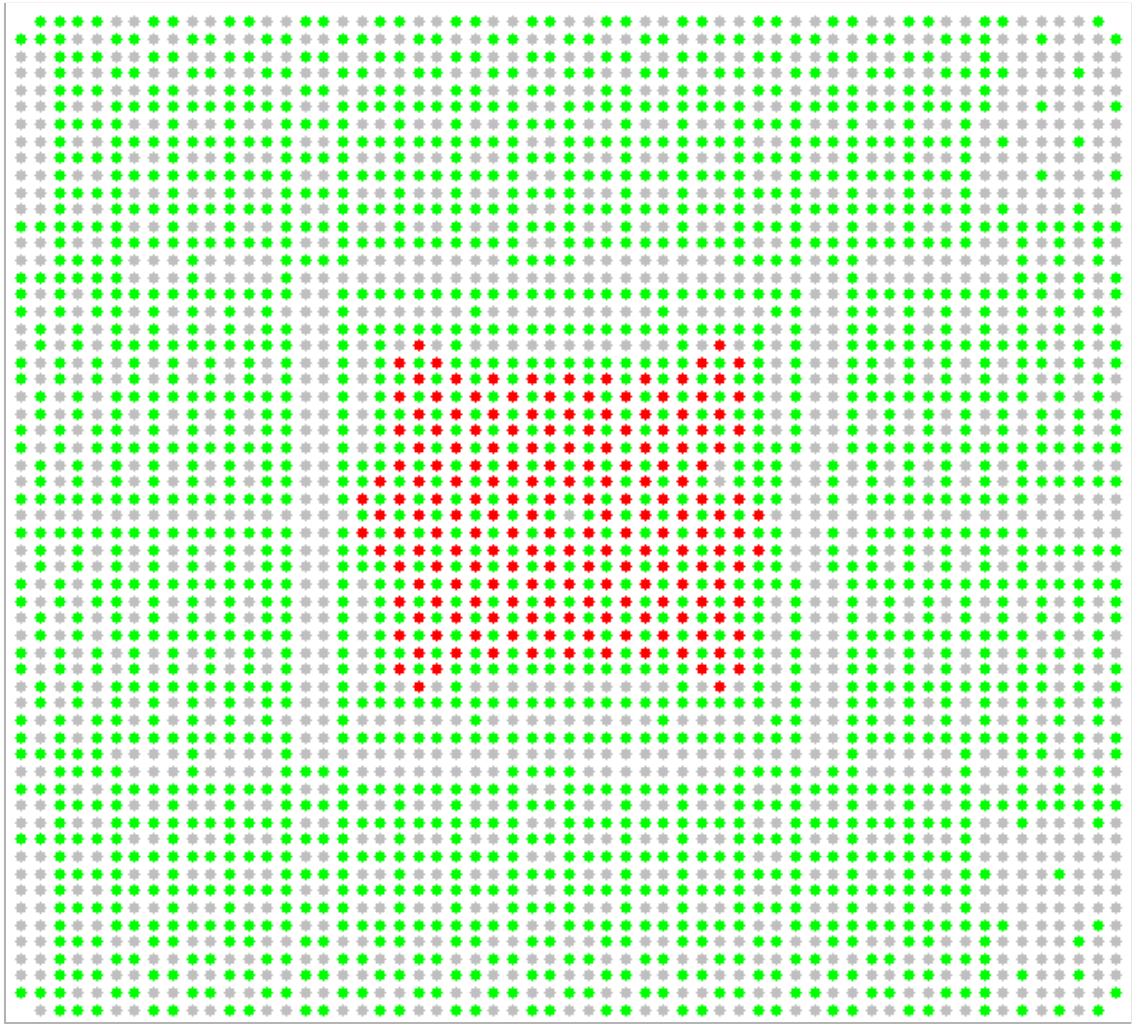

13
12.5
12
11.5
11
10.5
10
10
11
12
13
14
y-coordinate (mm)
x-coordinate (mm)

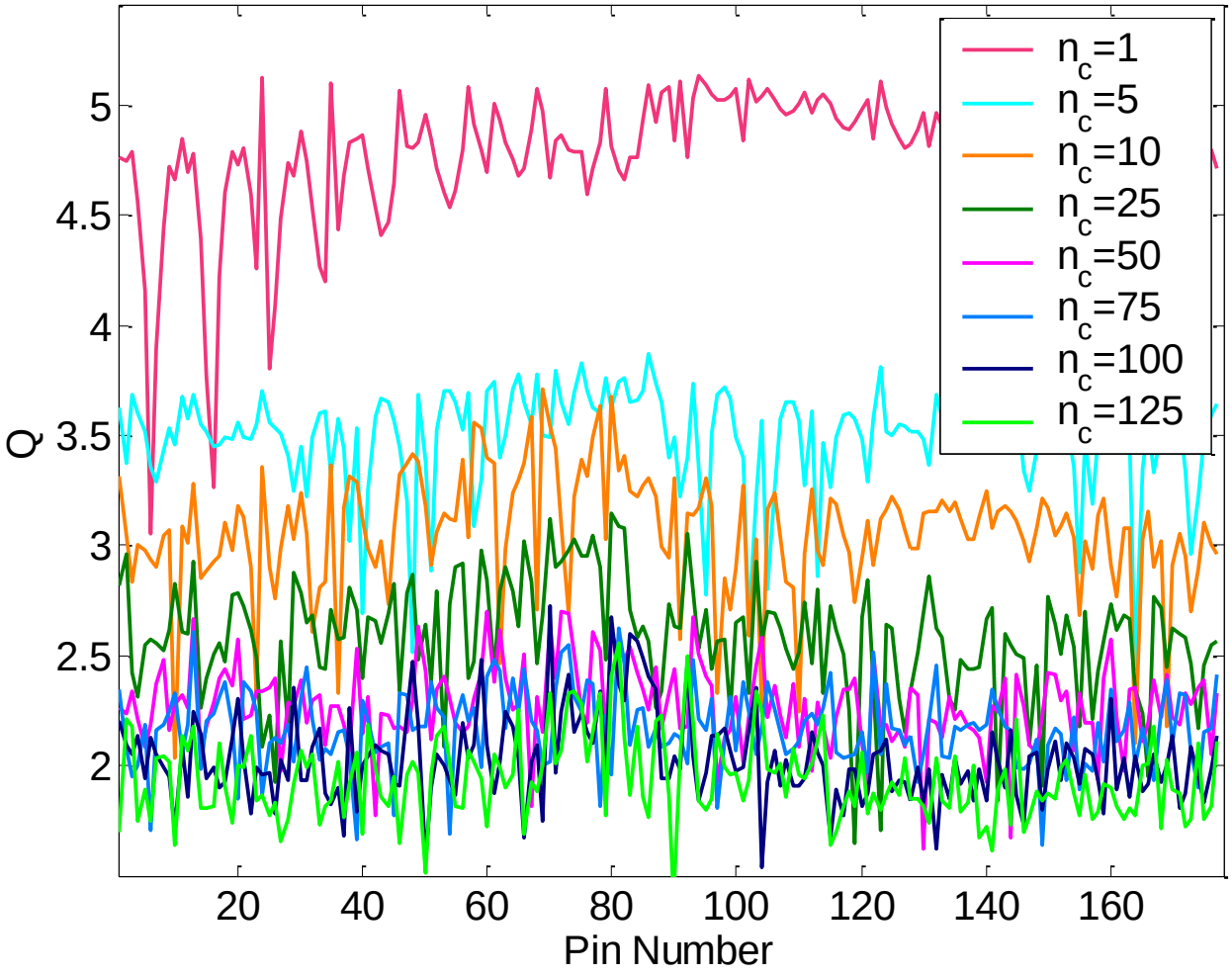

13
12.5
12
11.5
11
10.5
10
10
11
12
13
14
y-coordinate (mm)
x-coordinate (mm)

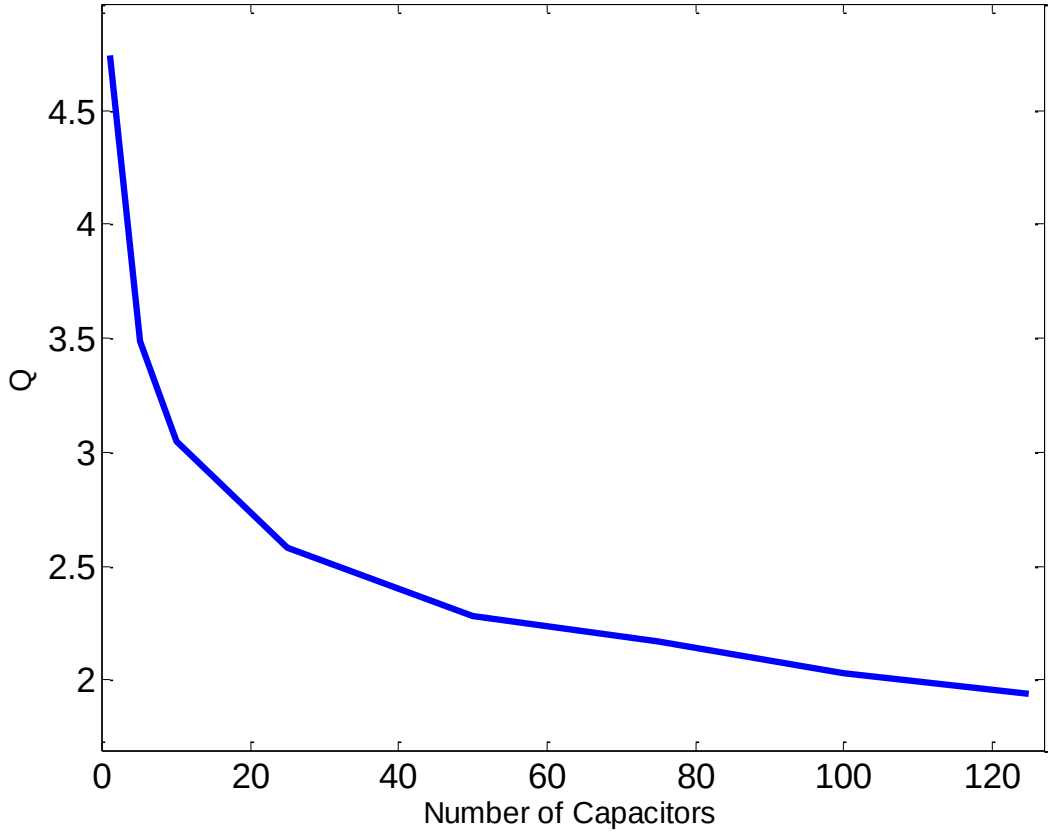

13
12.5
12
11.5
11
10.5
10
10
11
12
13
14
y-coordinate (mm)
x-coordinate (mm)



177 power pins



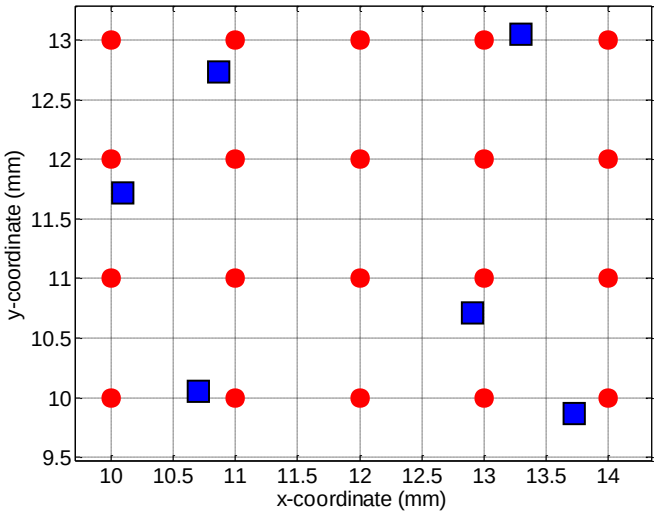



4.5
4
3.5
3
2.5
2
Q
0
20
40
60
80
100
120
Number of Capacitors

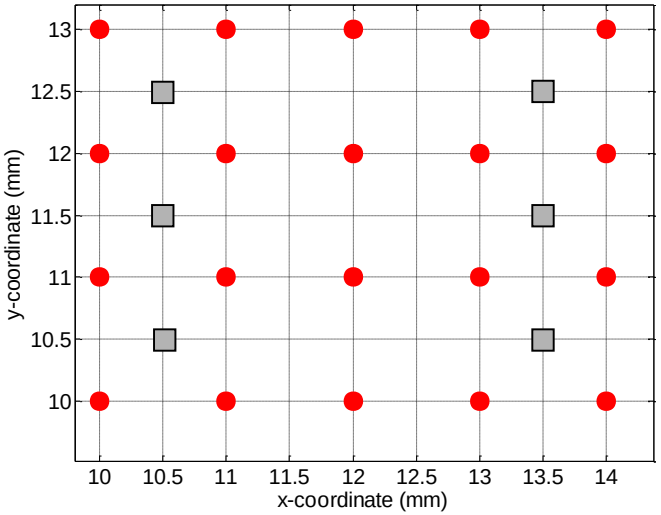
Objective Function for Optimization

$$\overline{Q} = \frac{1}{n_p} \sum_{i=1}^{n_p} \hat{Q}_i$$

Optimized placement

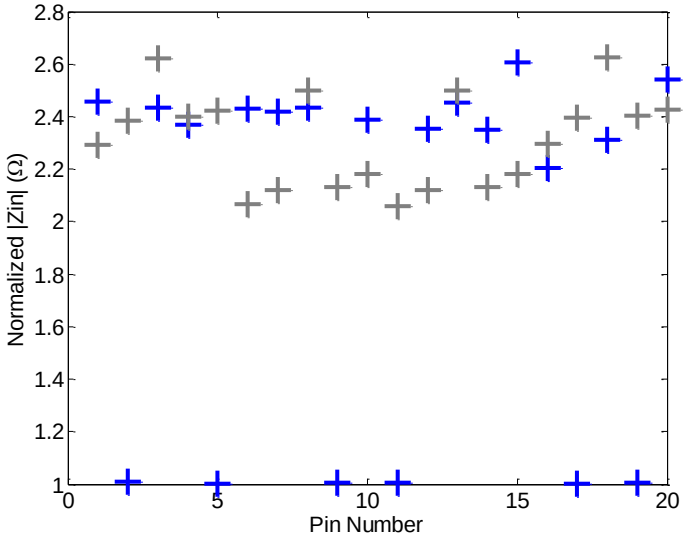


Even placement

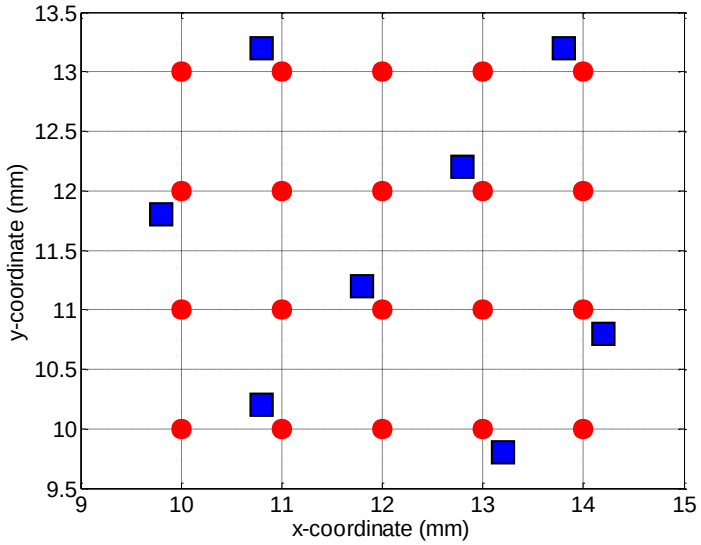


6 capacitors

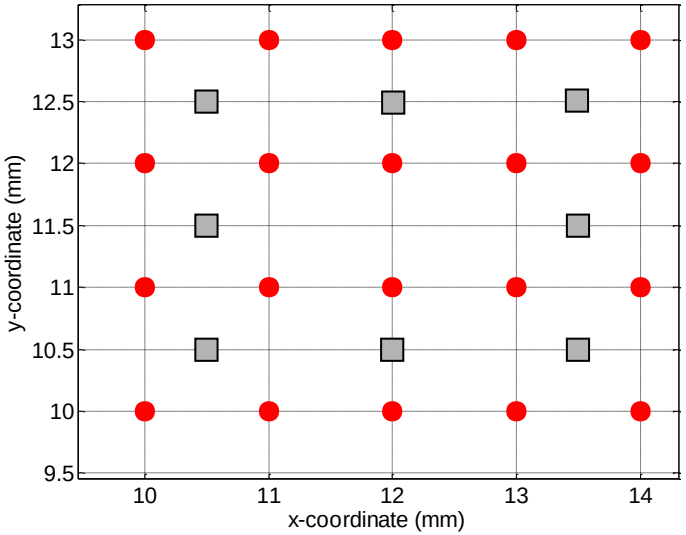
	Optimized	Even
Q_{ave}	1.99	2.31
Q_{max}	2.61	2.62



Optimized placement

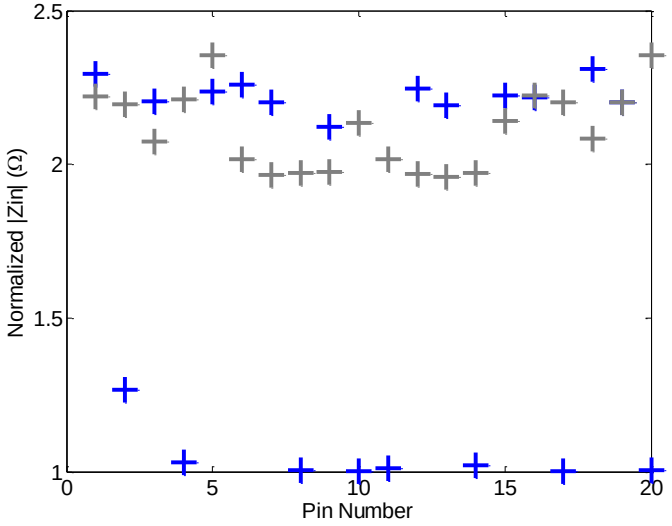


Even placement

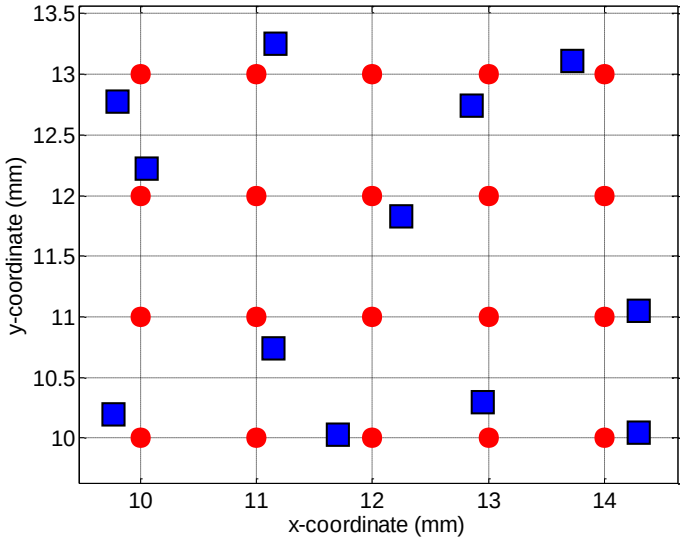


8 capacitors

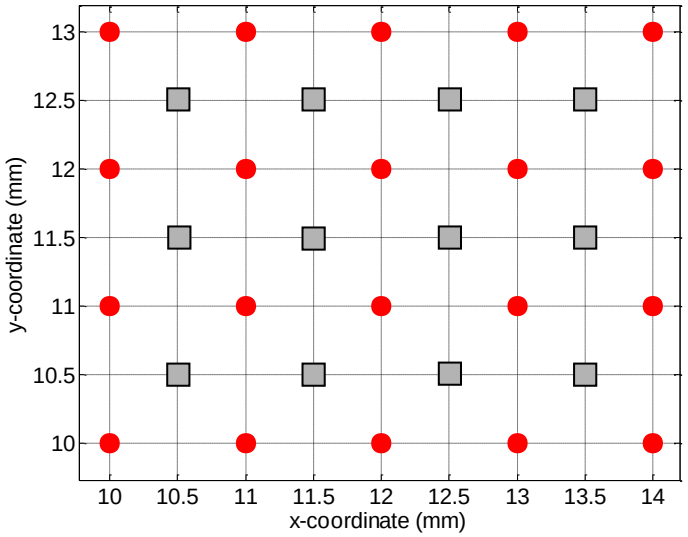
	Optimized	Even
Q_{ave}	1.75	2.11
Q_{max}	2.31	2.35



Optimized placement

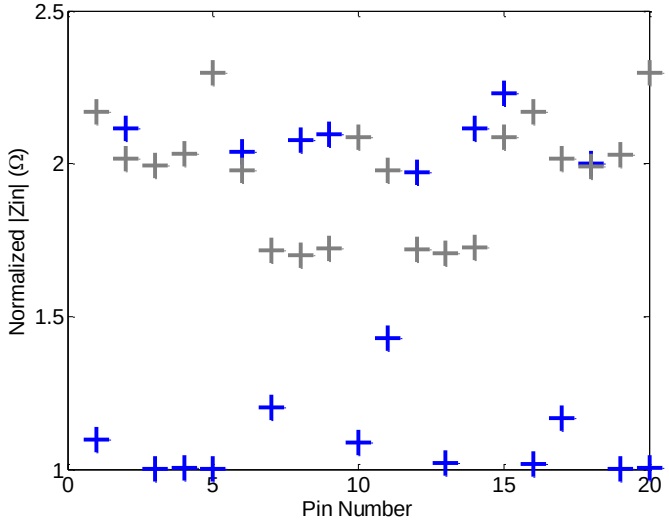


Even placement

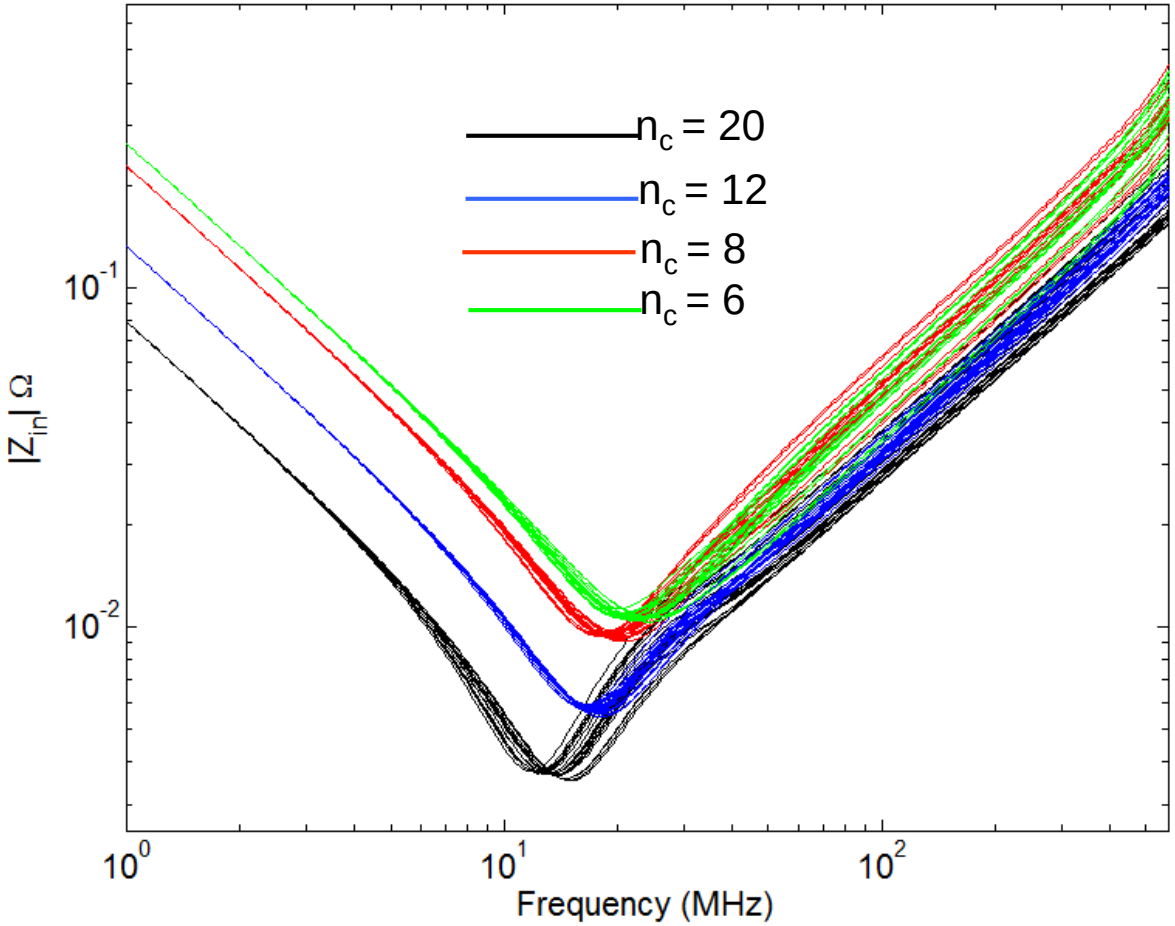


12 capacitors

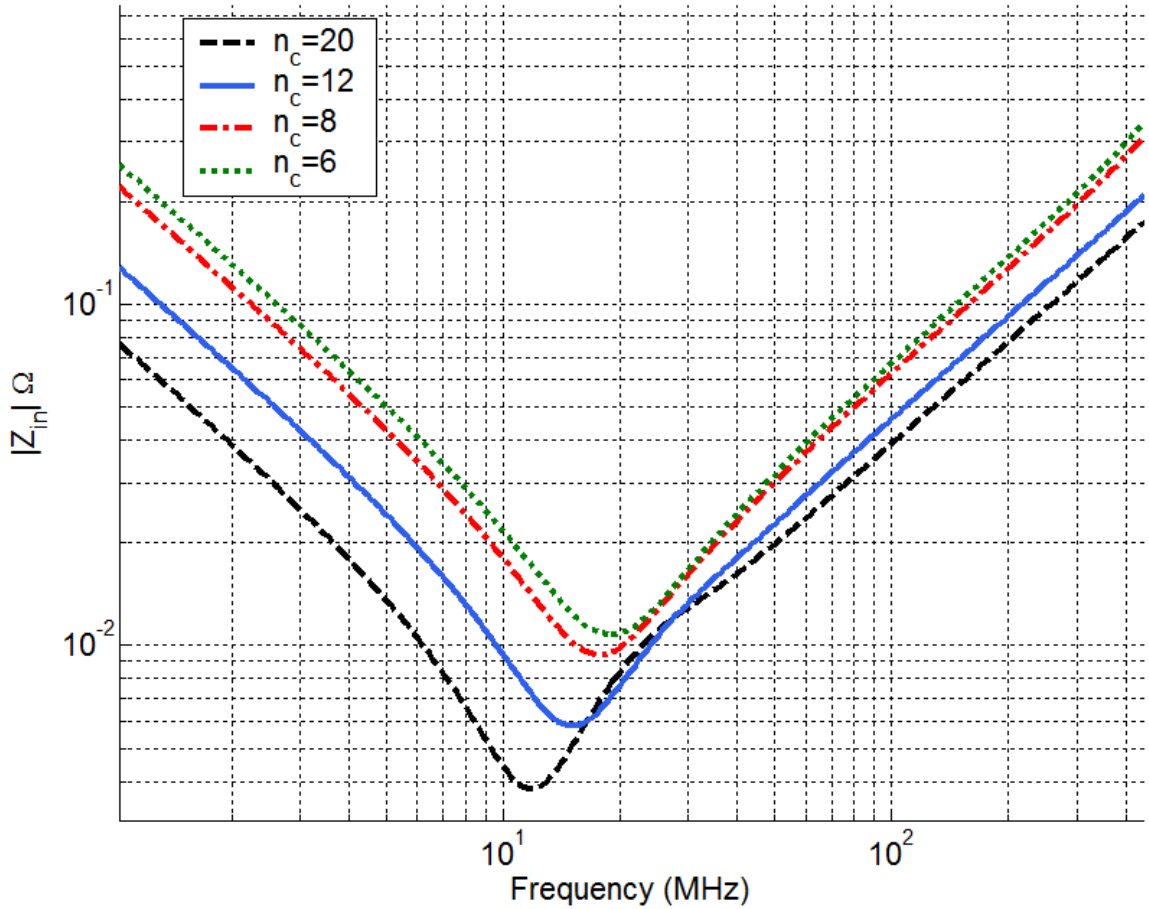
	Optimized	Even
Q_{ave}	1.48	1.97
Q_{max}	2.23	2.30



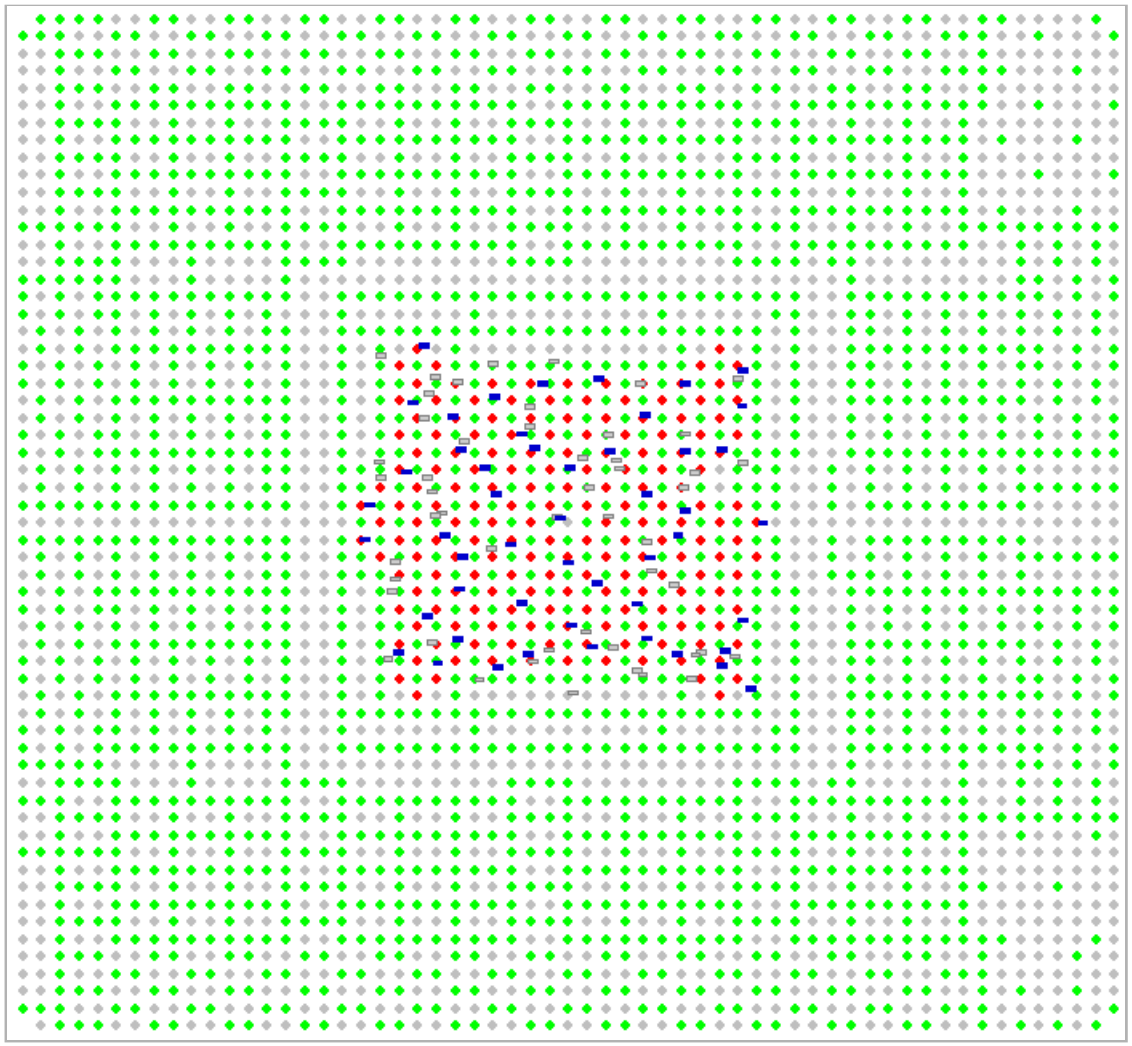
Input Impedance of all pins

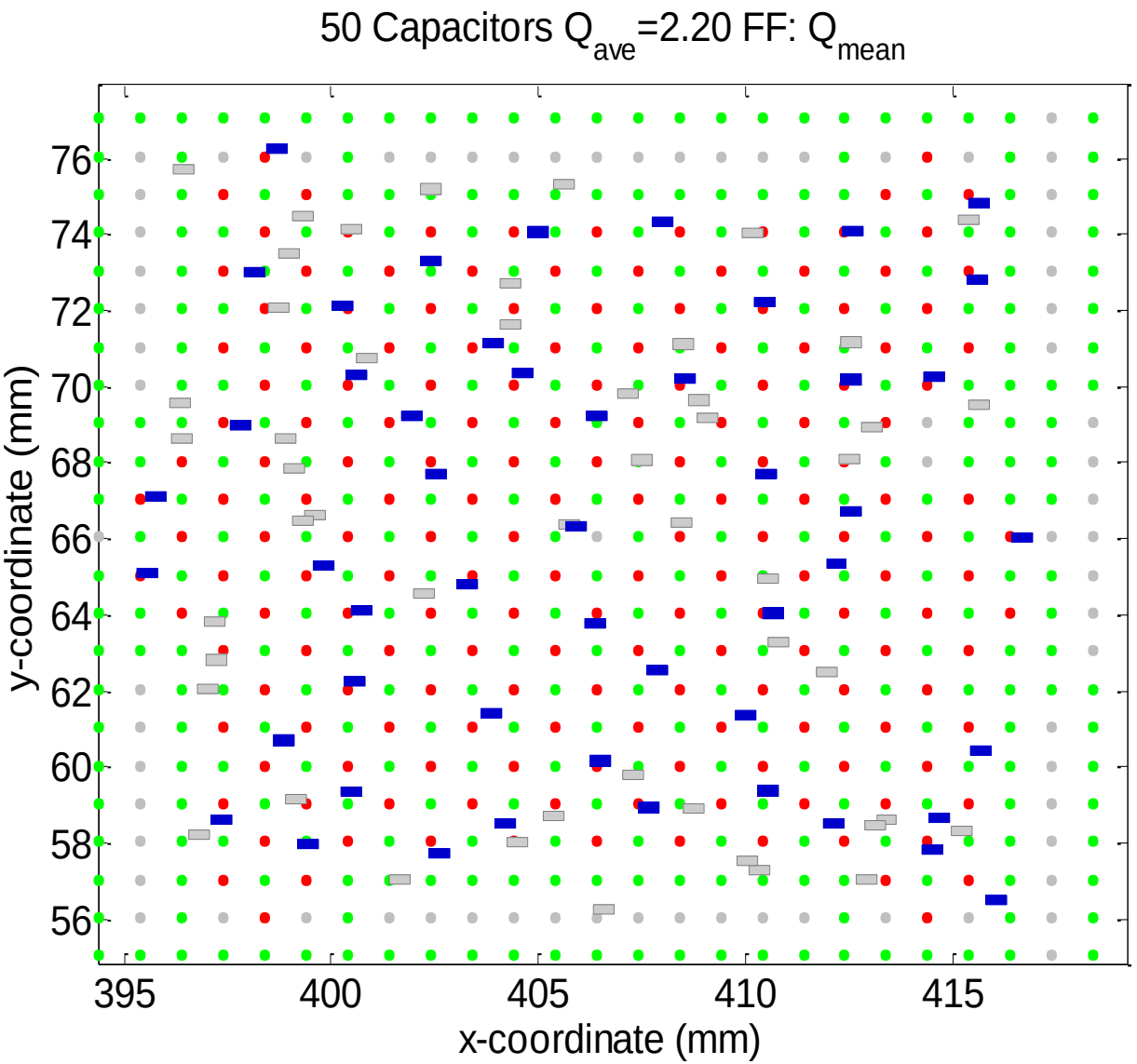


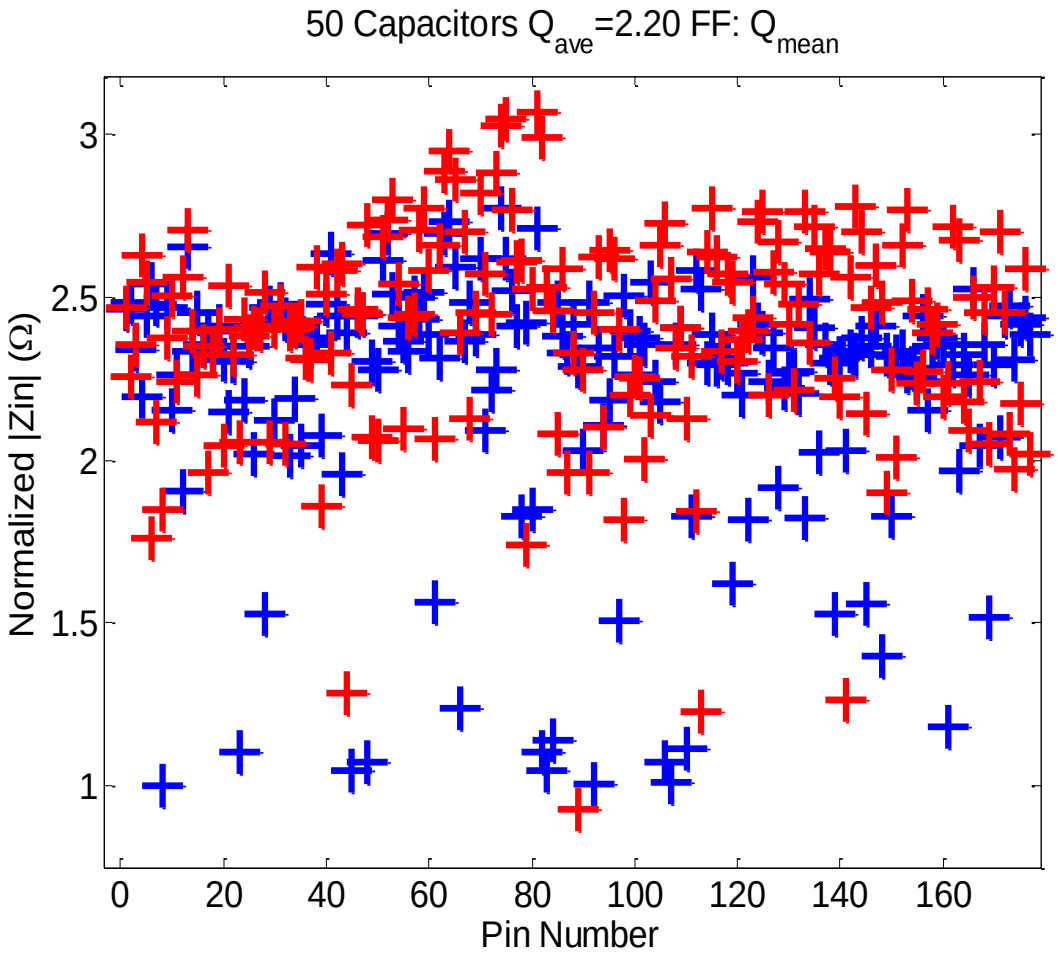
Pins with Lowest Input Impedance



177 power pins







Conclusions

- PI is an extension of SI in shared medium.
- Noise implications increase with data rates.
- Current design practices need to be revised for high data rate applications.
- A new definition is proposed for effectiveness of decoupling capacitors.
- Proposed algorithm considers power pins individually, aims to minimize spread inductance.
- A new objective function is proposed for optimized placement.
- Tested on industrial applications.

Appendix

Model of planar structure

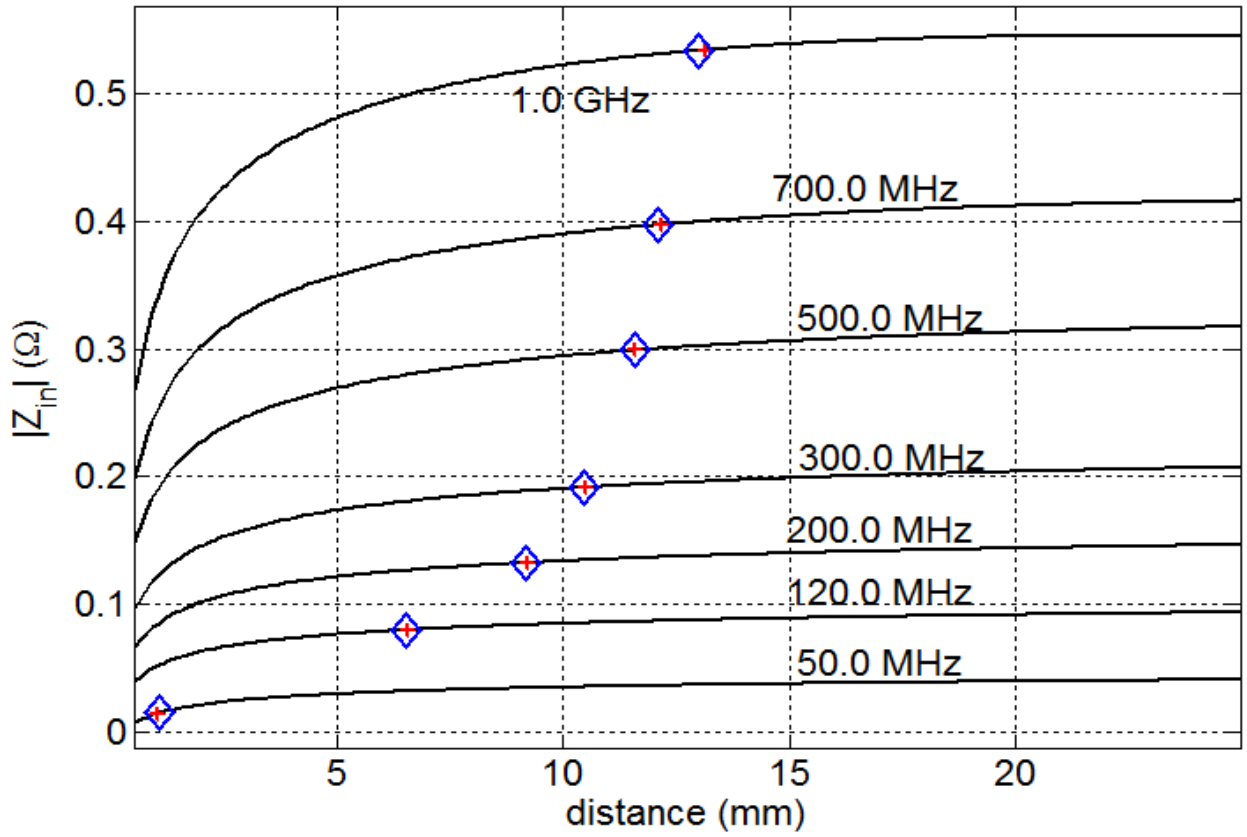
$$Z_{ij} = \frac{s\mu d}{\beta 2\pi r_i} \frac{H_0^{(2)}(\beta \mid r_i - r_j \mid) J_0(\beta r_j)}{H_1^{(2)}(\beta r_i)}$$

Distance at which the capacitor's effectiveness reduces by one qth of its maximum.

$$\left| \frac{Z_{in}(s,r)}{Z_{in}(s,r_0)} \right| \equiv q$$

$$f(s,r) = Z_{in}(s,r) - \frac{q^2 \left| Z_{in}(s,r_m) \right|^2}{Z_{in}^*(s,r)}$$

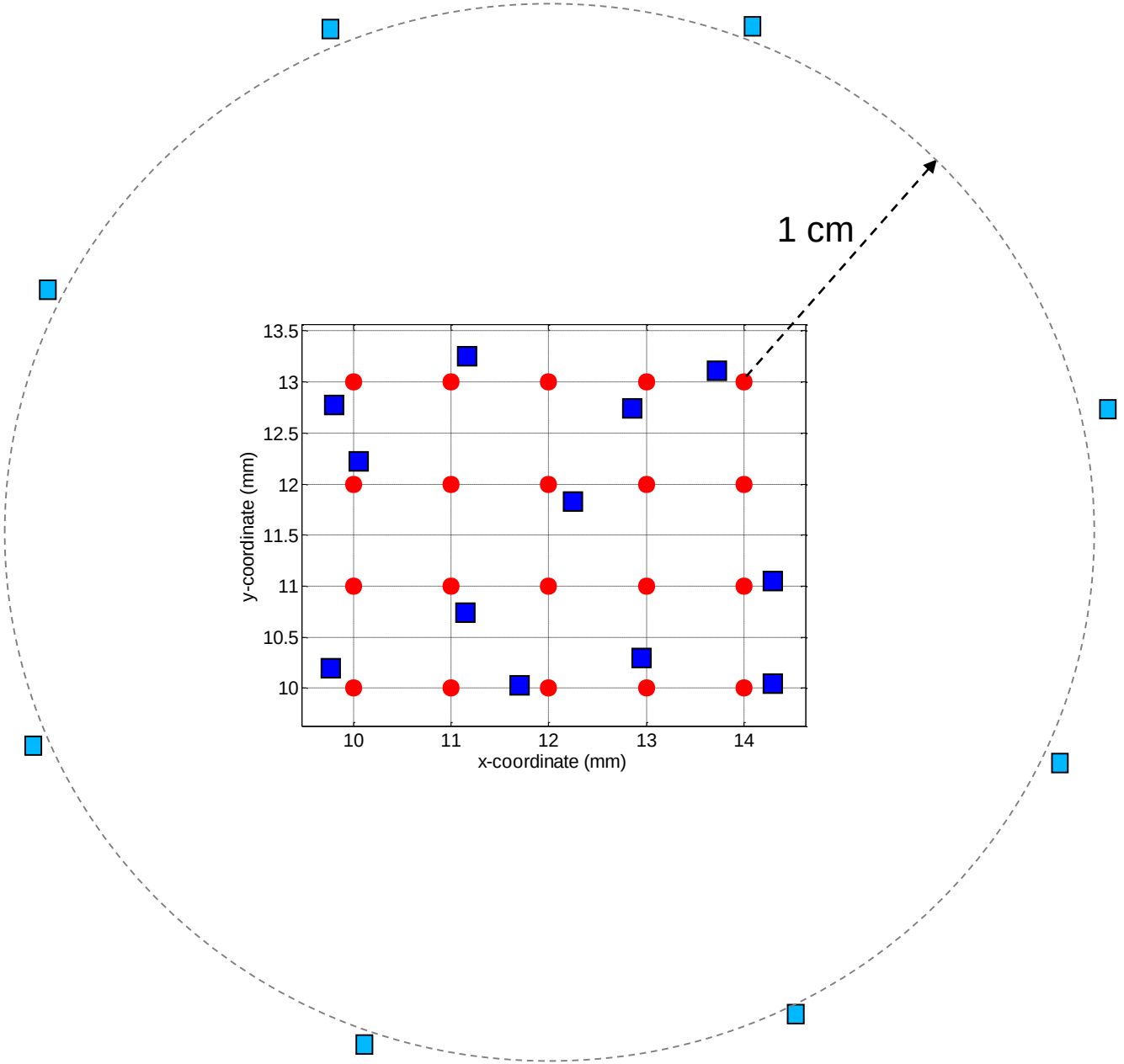
$$r_{n+1} = r_n - \frac{f_n(s,r)}{f_n'(s,r)}$$


1.0 GHz
700.0 MHz
500.0 MHz
300.0 MHz
200.0 MHz
120.0 MHz
50.0 MHz
0.5
0.4
0.3
0.2
0.1
0
5
10
15
20
distance (mm)
|Z_in| (Ω)

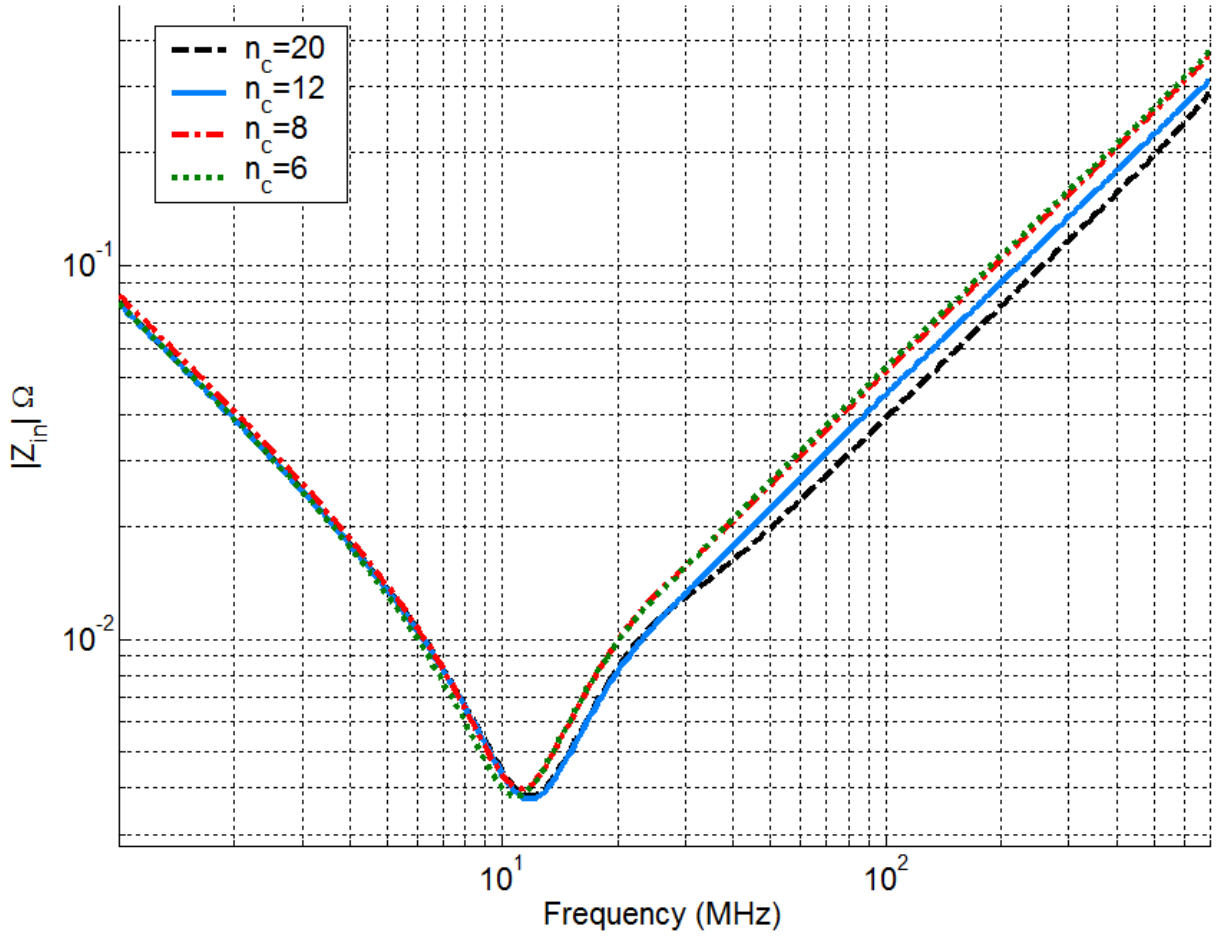
Relations for Multi-pin and capacitor configuration

$$Z = \begin{bmatrix} Z_{n_p x n_p} & Z_{n_p x n_c} \\ Z_{n_c x n_p} & Z_{n_c x n_c} \end{bmatrix}$$

$$Z_{in} = z_{pp} - Z_{pm}[Z_m + Z_c]^{-1} Z_{mp}$$



Worst-case Input Impedance with Additional Capacitors Outside BGA Pinfield



Ihsan Erdin and Ram Achar, “Multi-Pin Optimization Method for Placement of Decoupling Capacitors Using Genetic Algorithm," to appear in *IEEE Trans. Electromagnetic Compatibility,* in Dec. 2018.