High Speed Serial Channel Design

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IEEE

EMC SOCIETY

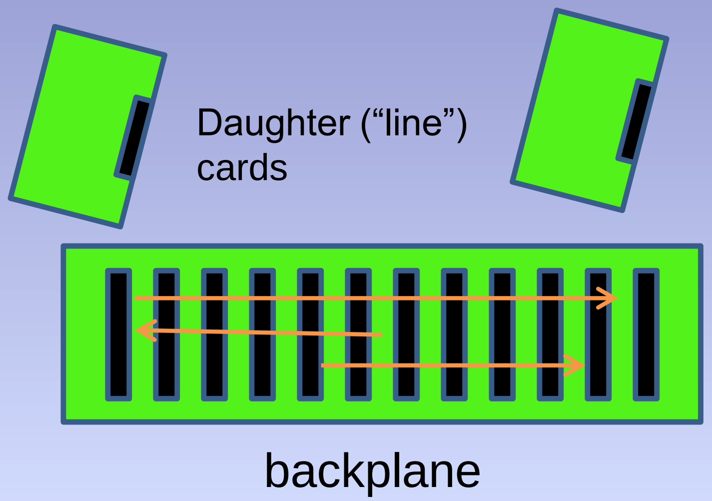
Outline

- Basic channel topologies
- Electrical characteristics of high speed channels
  - key parameters - determined by materials, dimensions, etc.
  - measurement techniques and tools
- "Real world" component examples
- Differential signaling and skew
- Channel examples
- Tools
- Resources and References

Channel Topologies

1980s-1990s
Parallel bus architecture

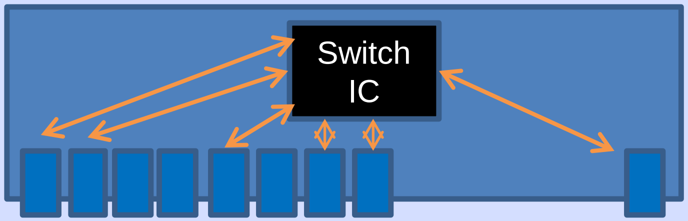
- ISA, PCI, MicroChannel, CPCI
- 16 32 bit slots, 100 MHz
- Line cards with Telco
  (T-1, T-3, OC-192, etc.)
  or Data interfaces; e. g.,
  100 Mb Enet



Technology enablers: High density, low cost Si ICs and FPGAs
Digital Signal Processing

2000s – switched serial architecture

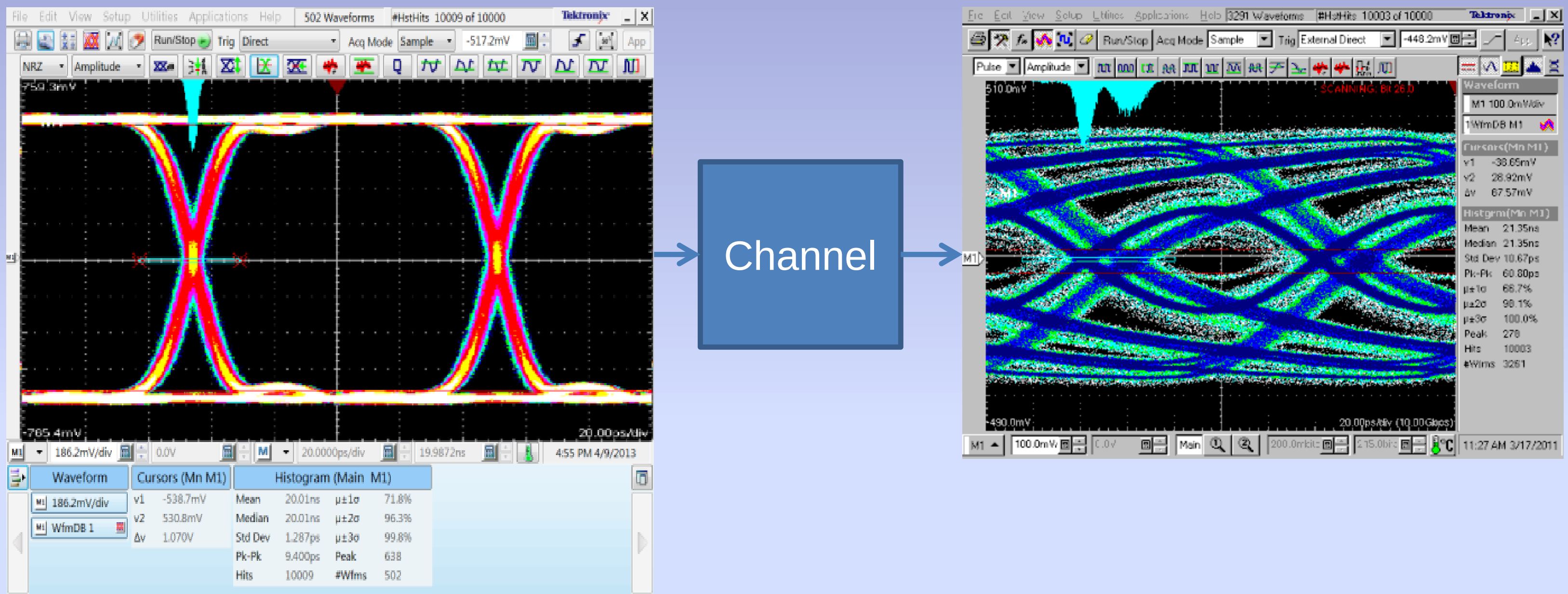
- IEEE 802.3, InfiniBand, Fibre Channel, Serial-ATA, Serial-Attached SCSI, PCI-express
- 2.5/5/10/25 Gb/s/lane
- SFP+ (1 lane)
- QSFP (4 lanes)
- CXP, CFP (12 lanes)



8-32 ports, 1/4/12 lanes each

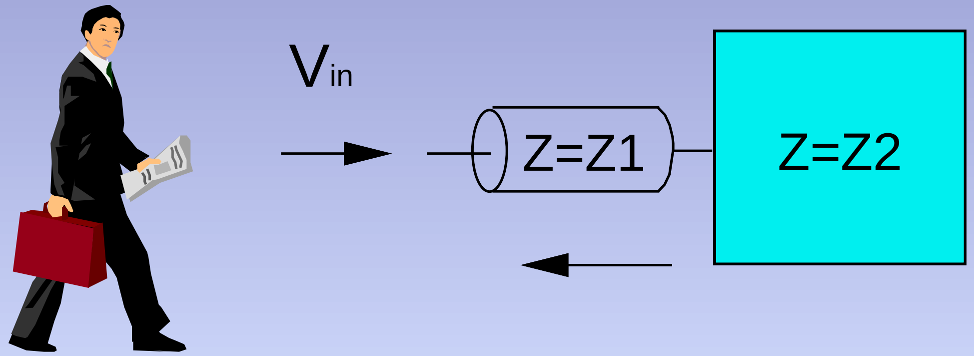
Signal Distortion

What goes in | What comes out



- Why?
  - Impedance discontinuities
  - Frequency-dependent losses in channel
  - Crosstalk
- What can be done about it?

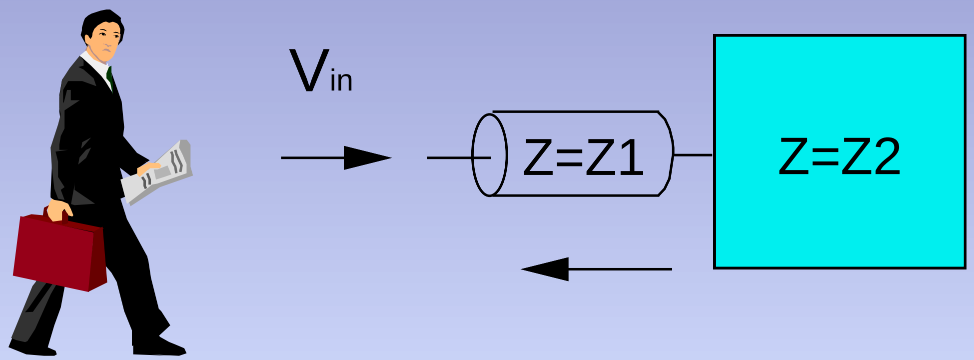
Impedance



Reflection coefficient, $\rho = \dfrac{V_{refl}}{V_{in}} = \dfrac{Z2-Z1}{Z2+Z1}$ (can be + or -, and may be called Γ)

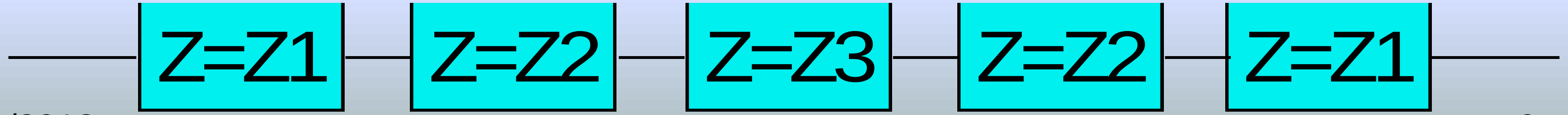
Another useful relationship: $VSWR = \dfrac{1+\rho}{1-\rho}$

Impedance



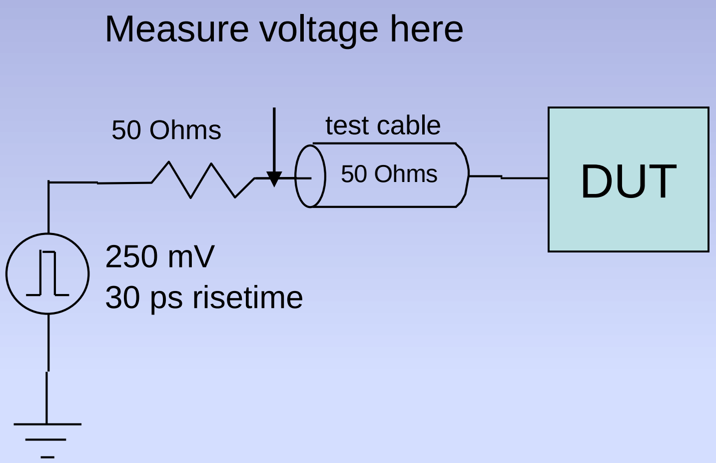
Reflection coefficient, $\rho = \dfrac{V_{refl}}{V_{in}} = \dfrac{Z2-Z1}{Z2+Z1}$ (can be + or -, and may be called Γ)

Imagine what would happen if you had this:



Impedance measurement

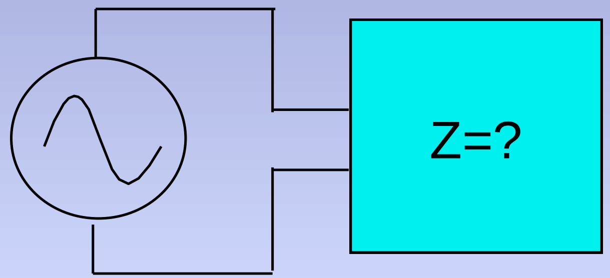
- Time Domain Reflectometer (TDR)



- time domain measurement - measures Z vs. time (distance)
- can be single-ended (shown) or differential (if equipment capable)
- accuracy, resolution degrade with
  - loss in test cables and DUT
  - probe effects (large ground loops, etc.)
- risetime is everything!

Impedance measurement

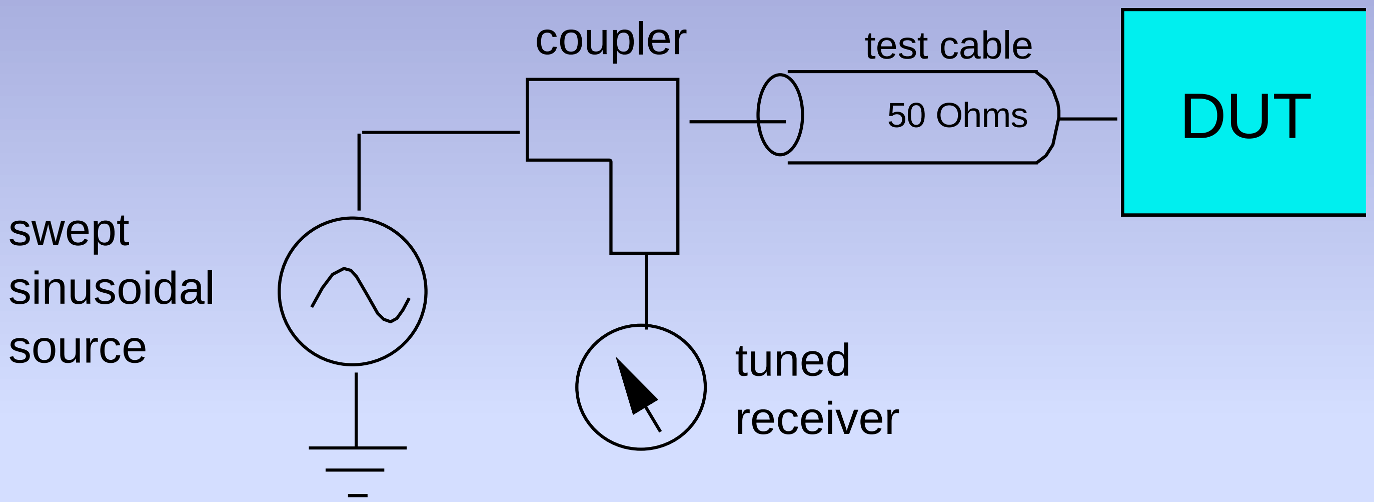
Impedance Bridge



- AC source (oscillator) - must specify frequency (ies)
- Measures R, L, C, Z looking into DUT
- Subject to inaccuracy due to
- resonance of DUT at measurement freq.
- discontinuities in DUT - no position-dependent info

Impedance measurement

Vector Network Analyzer (VNA)

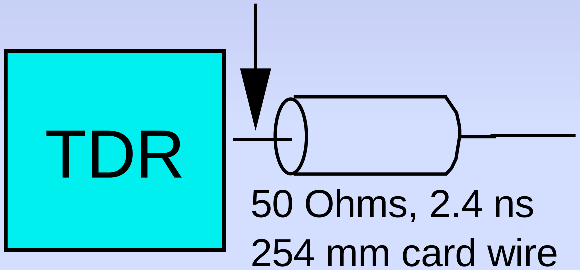


- freq. domain measurement - measures vs. frequency, typically. s parms.
- no spatial (distance) information
- can be single-ended (shown) or differential (if equipment capable)
- accuracy, resolution degrade with
    - loss in test cables and DUT
    - fixture effects, including discontinuities

Impedance example 1

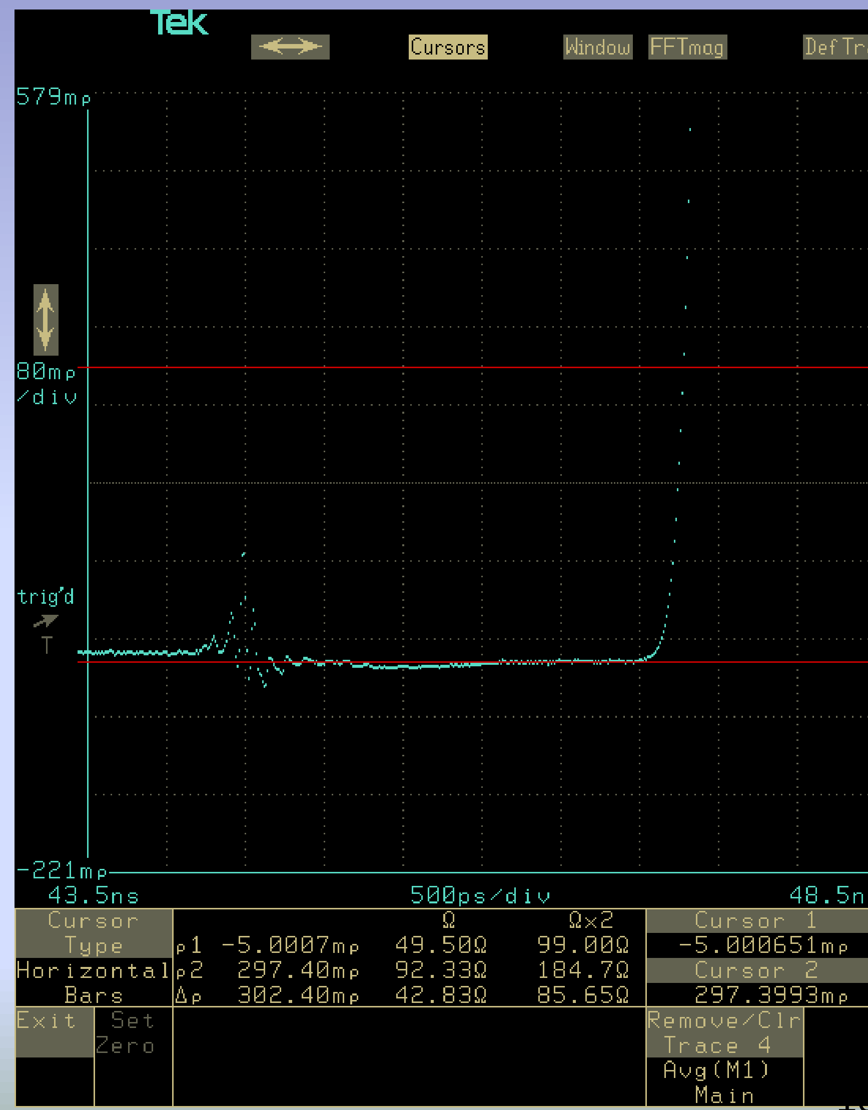
- Matched line, open circuited end

measure voltage here



50 Ohms, 2.4 ns
254 mm card wire

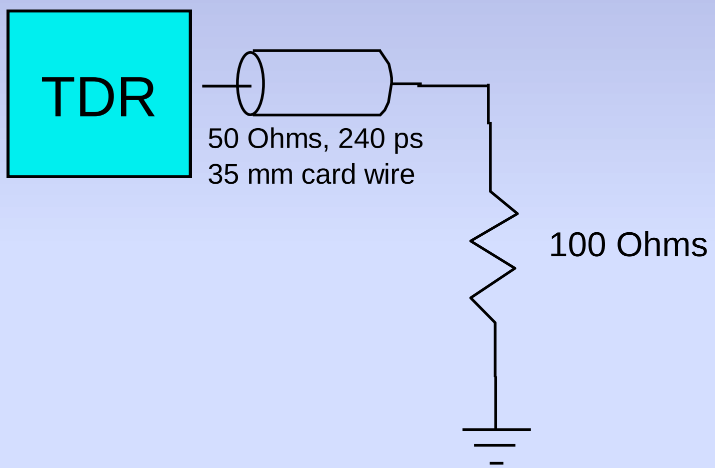
cursors: 1=51.1 Ω
2=N/A

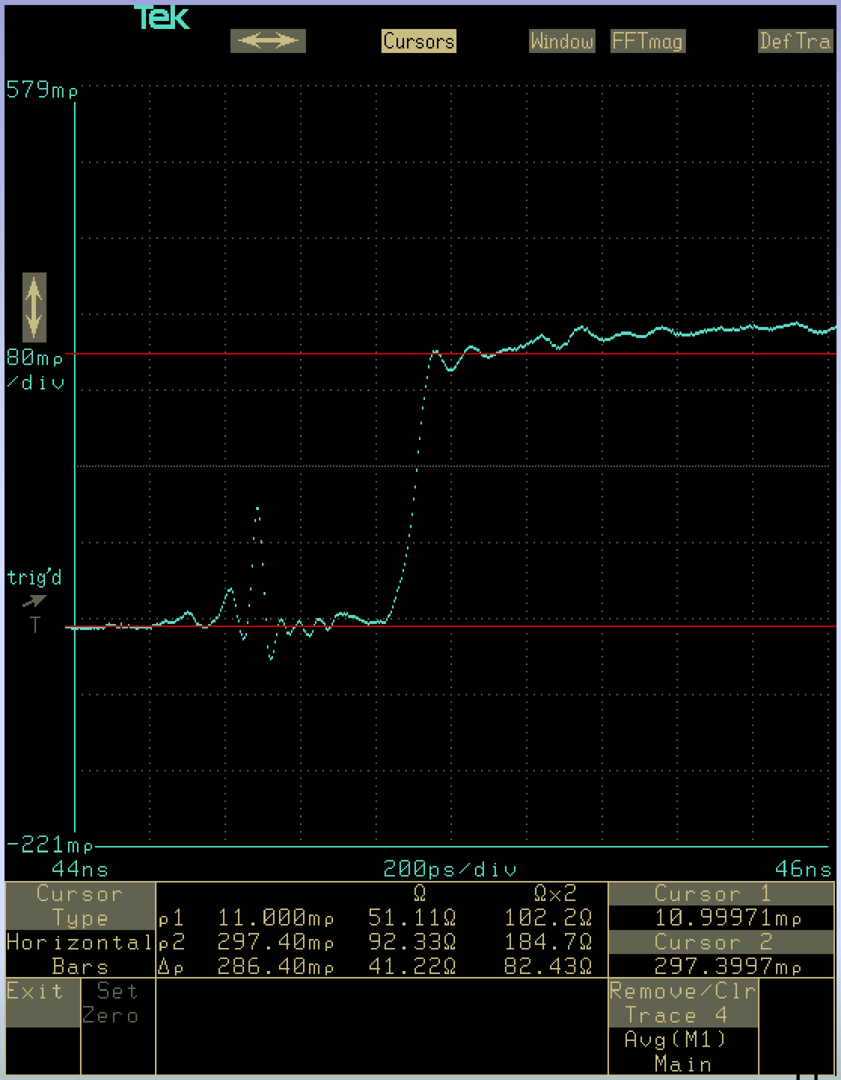


A TDR is a debugger's friend!

Impedance example 2

- Matched line, mismatched resistive load

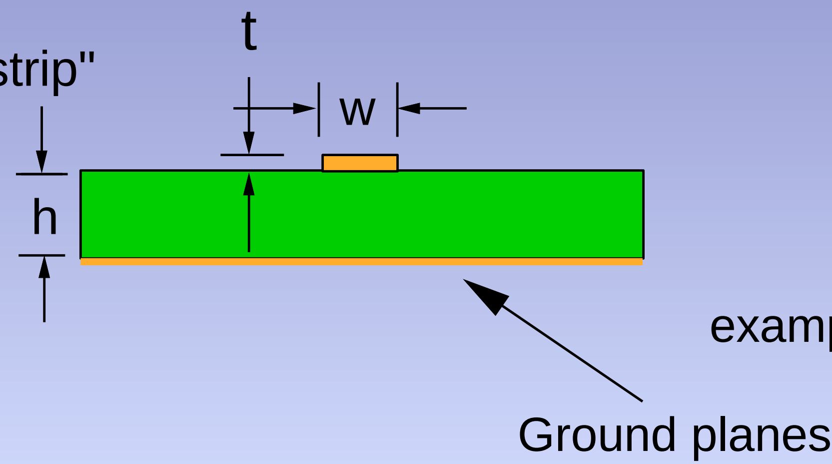




cursors: 1=51.1 Ω
2=92.33 Ω

Card wiring impedance

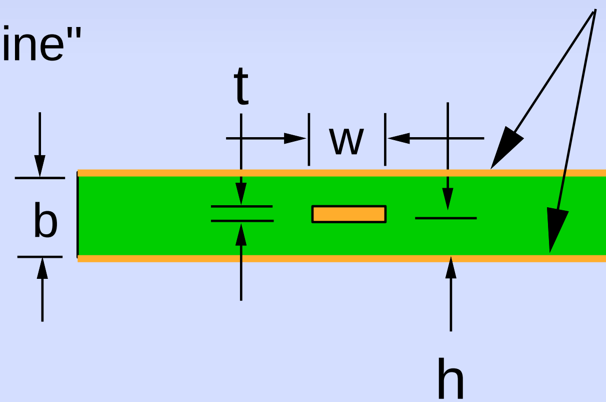
"Microstrip"



$$Z0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln\left(\frac{5.98 * h}{0.8w + t}\right)$$

example: w=6, t=1.4, h=12 -> Z0=60 Ω

"Stripline"



$$Z0 = \frac{60}{\sqrt{\epsilon_r}} \ln\left(\frac{4b}{0.67\pi w\left(0.8 + \frac{t}{w}\right)}\right)$$

example: w=6, t=1.4, b=12, h=6 -> Z0=37 Ω

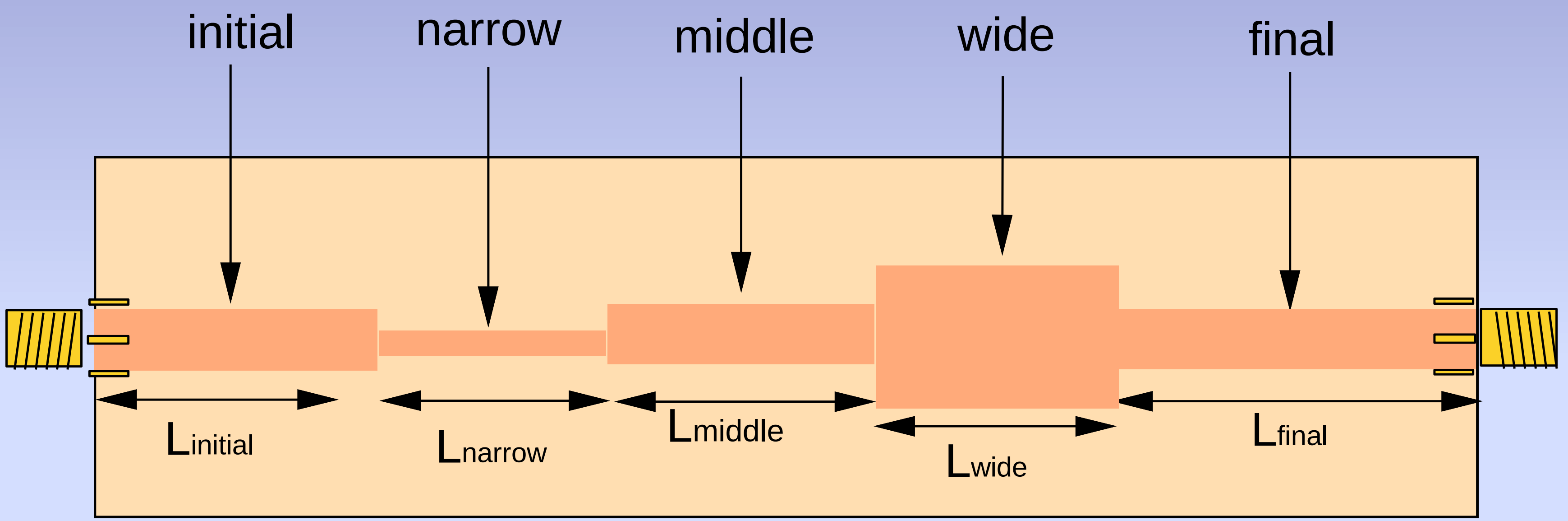
Notes: 1. The stripline may not be vertically symmetric (can be unequal spacing to planes)
2. Other variations exist; e. g., covered microstrip (stripline w/o upper Ground plane)
Reference: Blood: MECL Handbook

Impedance Discontinuities

- Change in geometry of conductors
  - width, thickness of signal conductor
  - proximity to reference plane
- Change in surrounding materials (ε_r)
  - plastic insulators, connector body in connectors
  - conductor dielectric, hot melt, overmold in cables
- Examples
  - Connectors
  - vias

Impedance example 3

"ugly" network

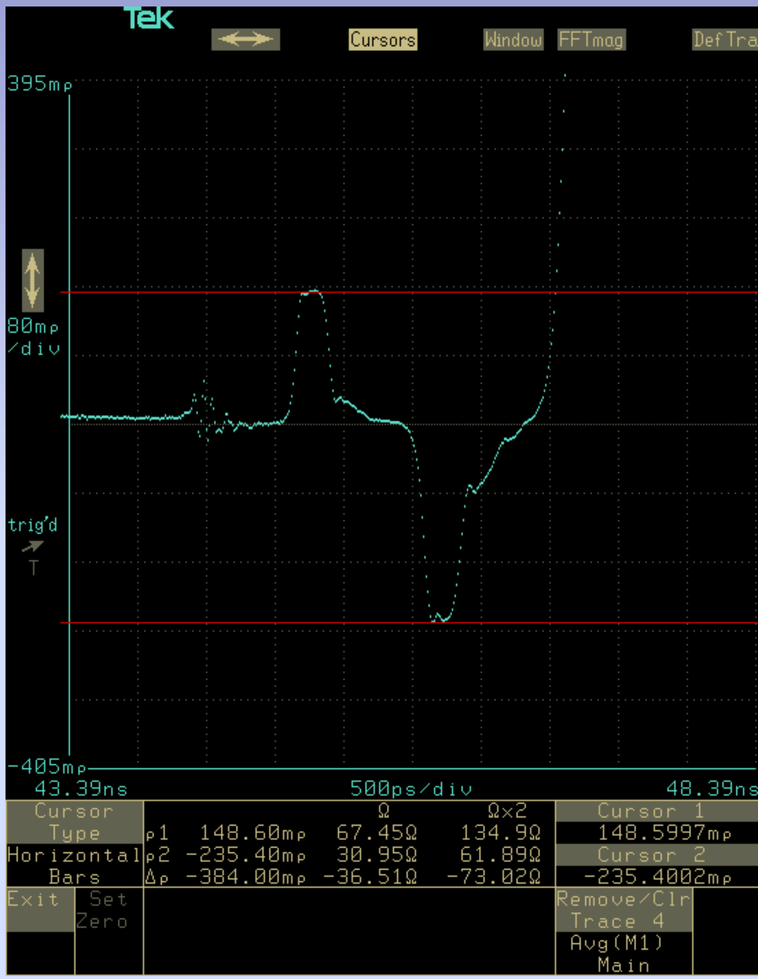


Winitial = 2.77 mm
Wnarrow = 1.24 mm
Wmiddle = Winitial
Wwide = 7.58 mm
Wfinal = Winitial

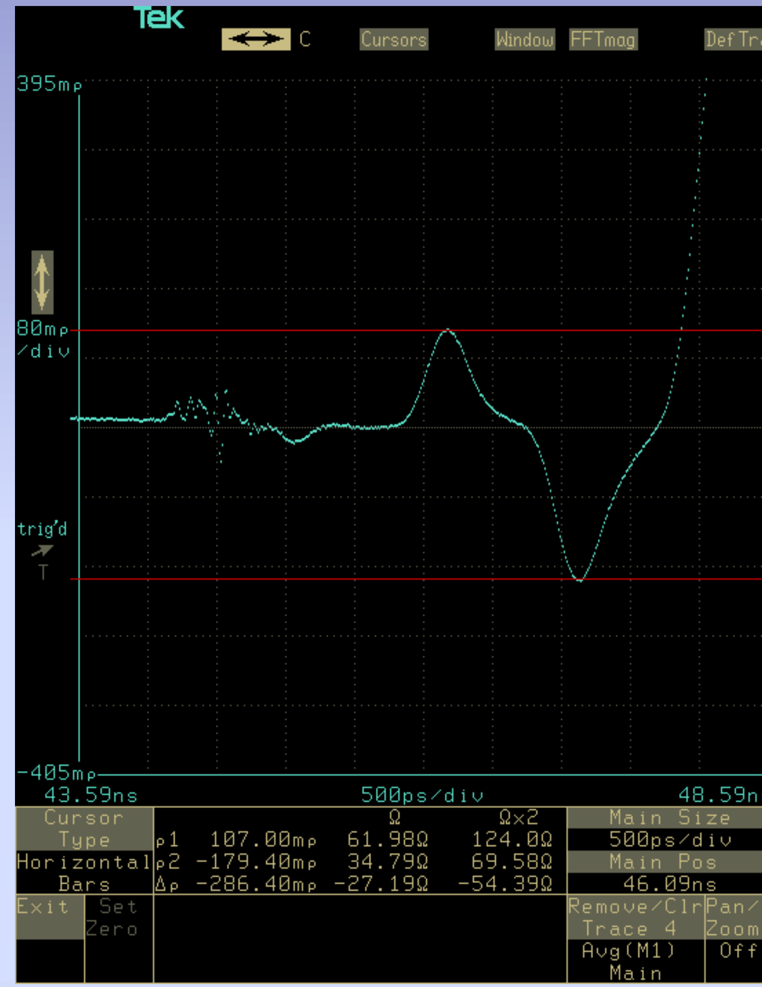
Linitial = 53 mm
Lnarrow = 20 mm
Lmiddle = 56 mm
Lwide = 20 mm
Lfinal = 53 mm

Zinitial = 50 Ω
Znarrow = 67 Ω
Zmiddle = Zinitial
Zwide = 31 Ω
Zfinal = Zinitial

"Ugly" network TDR plots

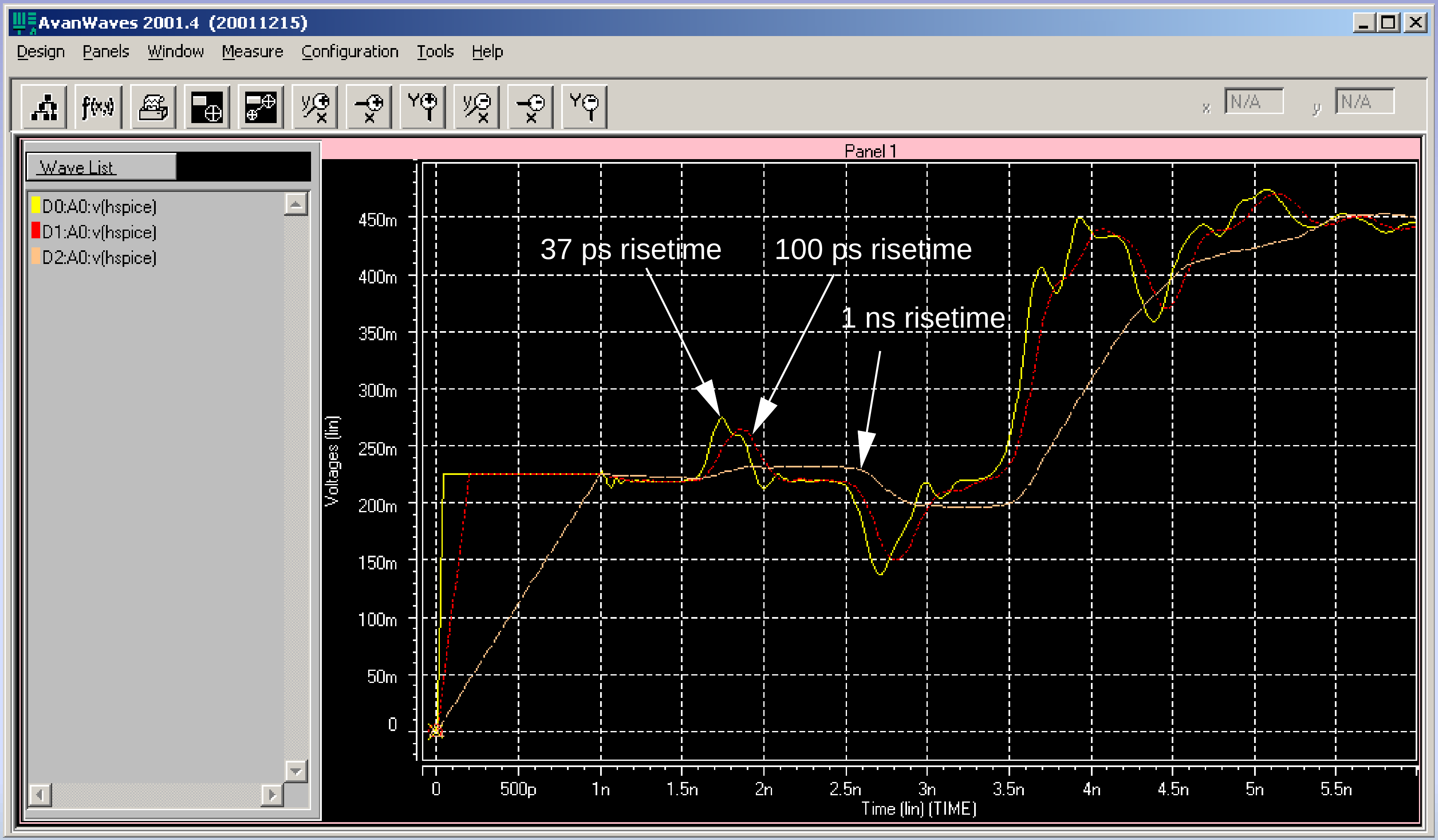


unfiltered: Zmin=30.95, Zmax=67.4



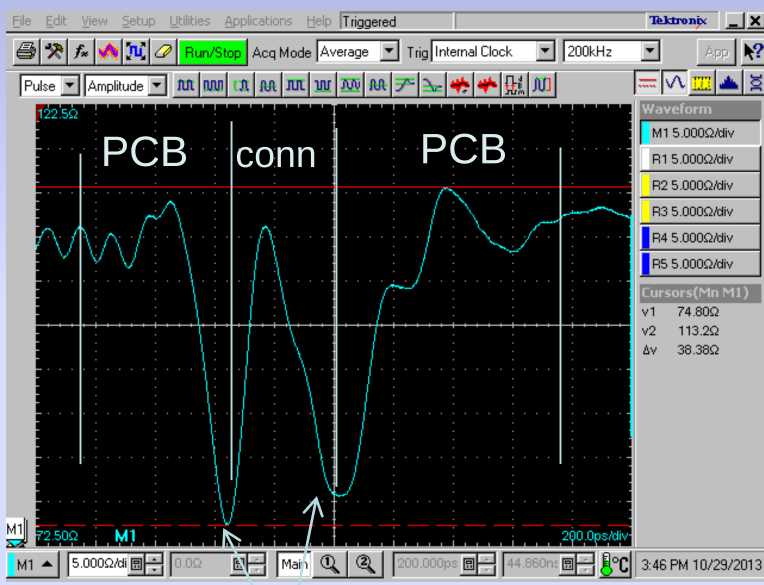
200 ps filter: Zmin=34.79, Zmax=61.98

"Ugly" network simulation



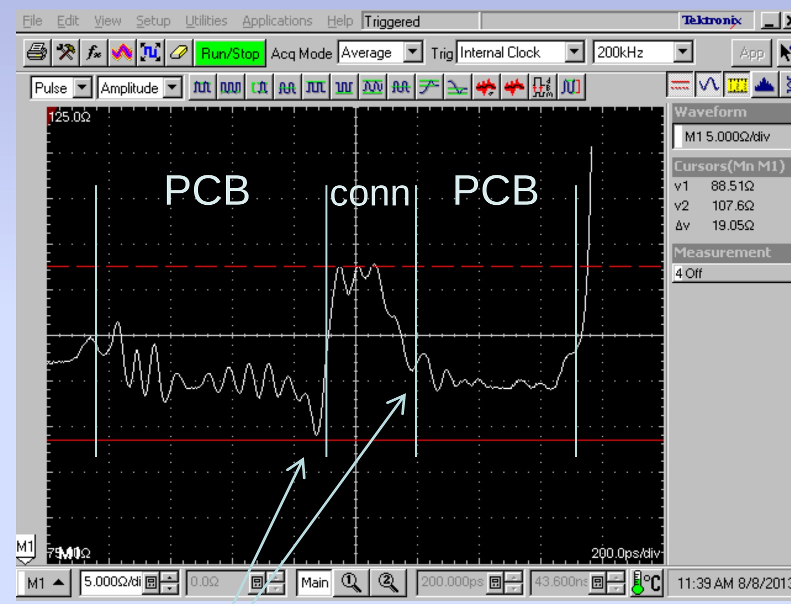
Connectors
Impedance

- FCI Metral™ 3000 Impedance, D3XY



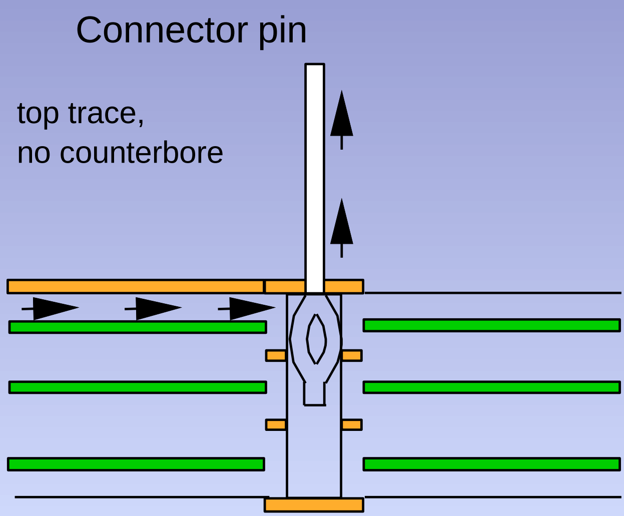
vias

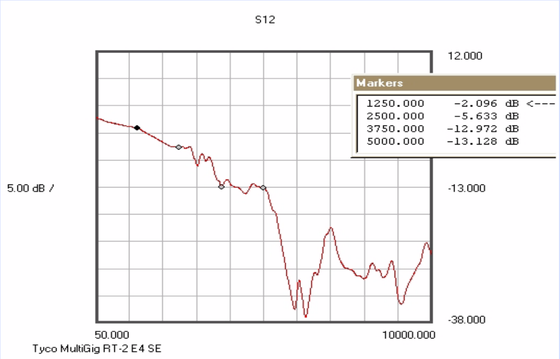
- FCI AirMax™ Impedance, N6O6



vias

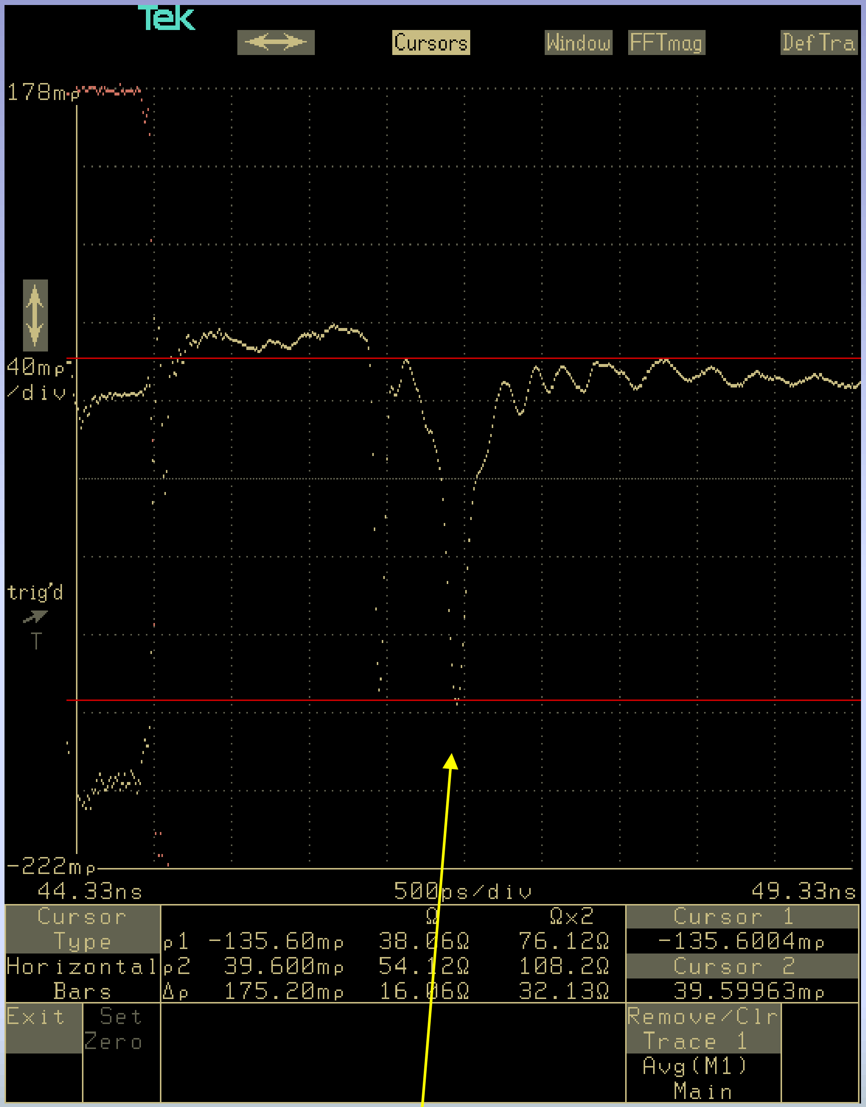
Vias





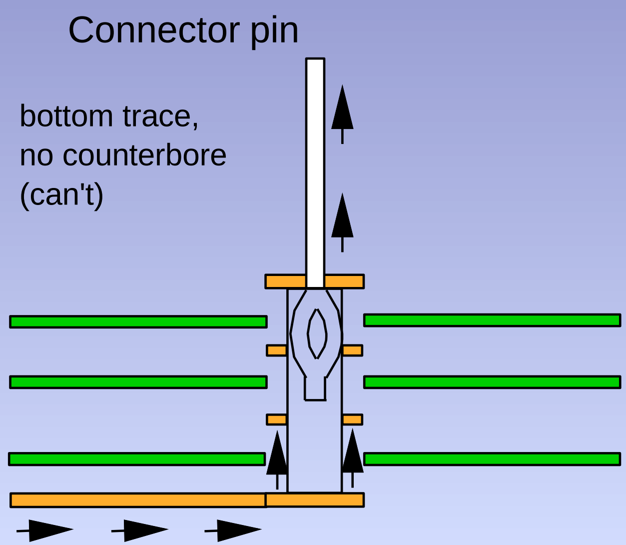
Insertion loss

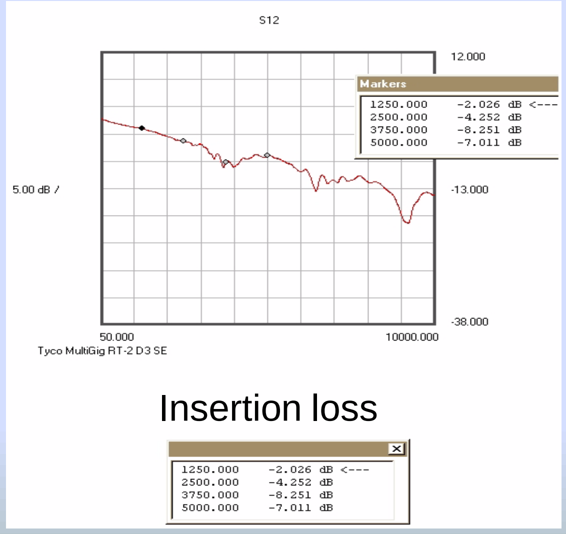
1250.000	-2.096 dB	<---
2500.000	-5.633 dB	
3750.000	-12.972 dB	
5000.000	-13.128 dB	

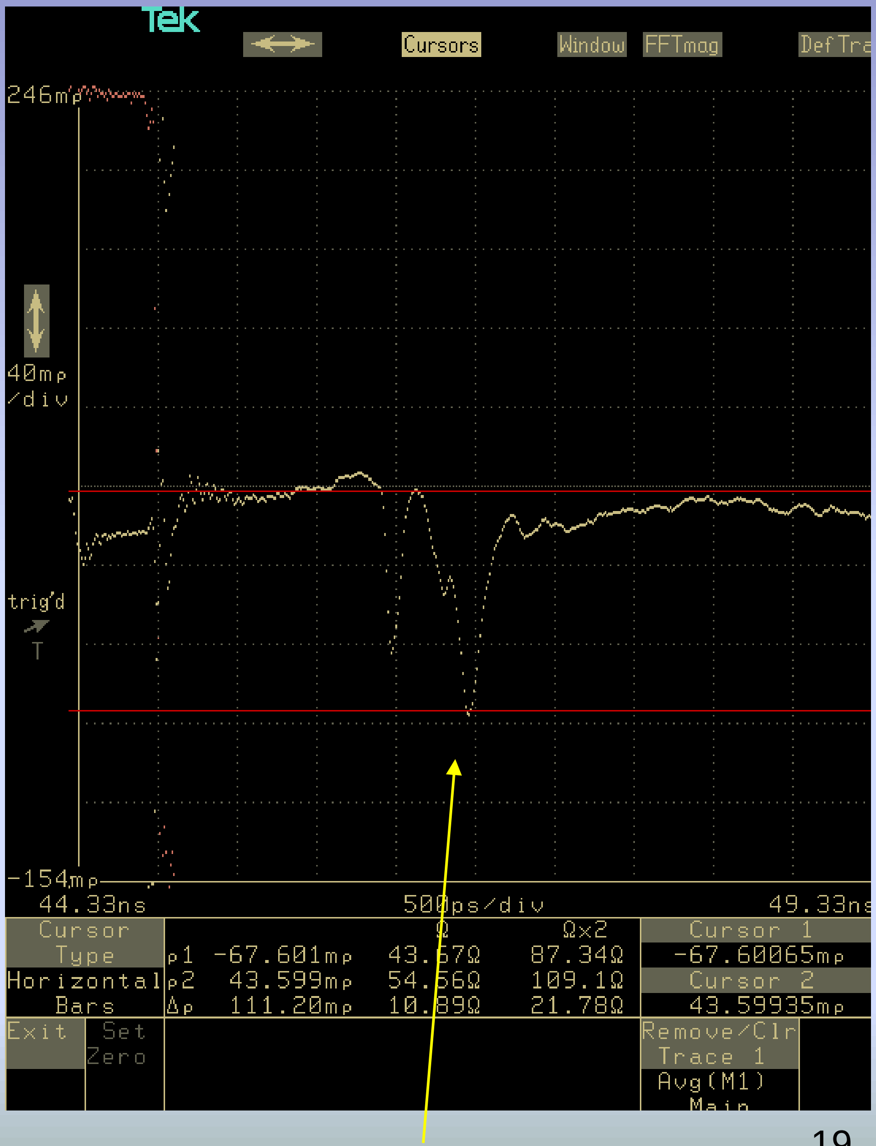


min. Z=38 Ohms

Vias







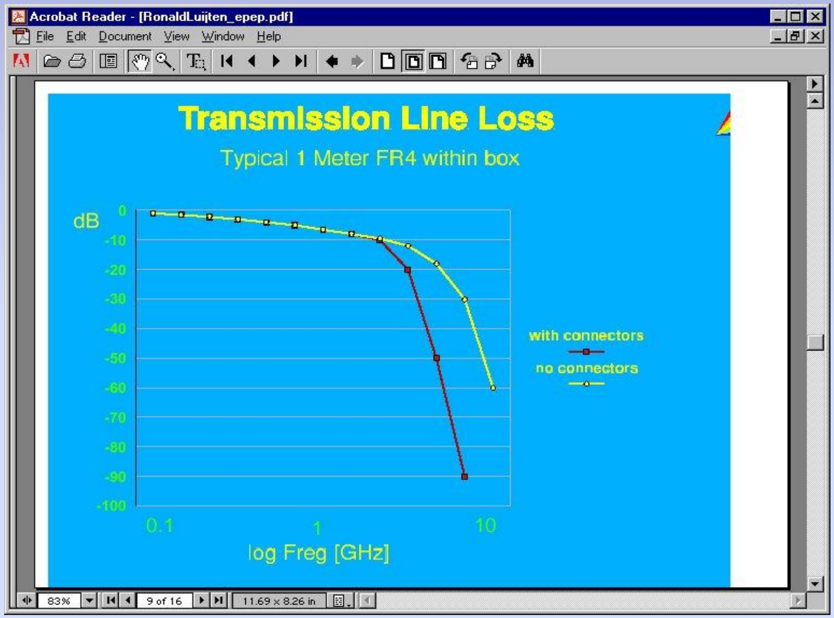
min. Z=44 Ohms

Modeling tools

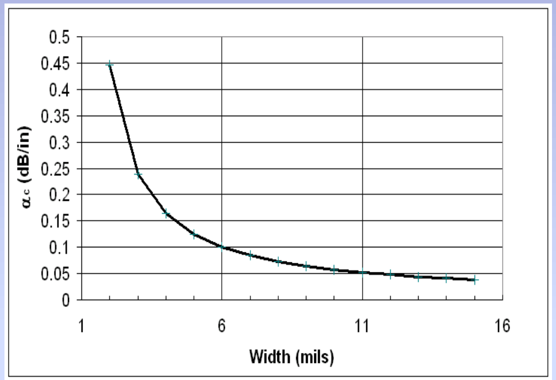
- Cadence Allegro SpectraQuest and Sigrity
- IBM Yorktown EIP tools (CZ2D, EmitPkg)
- Missouri Univ. of Science & Tech. FEMAS
- Polar Instruments (http://www.polarinstruments.com)
- HSPICE built-in field solver
- Field Solvers
  - Agilent EMPro
  - Ansys HFSS, Q3D
  - AWR Microwave Office™
  - CST Microwave Studio™
  - Symberian Simbeor™
- Tektronix IConnect™
- various free tools

Maximizing Channel Signal Integrity

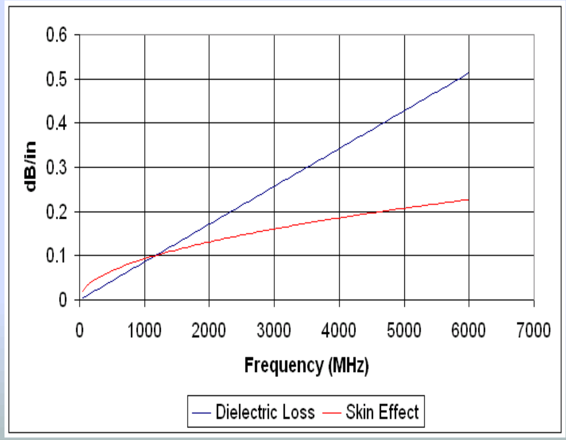
- Understand the channel
- Biggest culprit is frequency-dependent insertion loss (and reflections)
- Next problem is crosstalk



source: R. Luijten, IBM Zurich, 2000 EPEP Conf.



source: J. Cain, Cisco Systems, 2000 EPEP Conf.



- Minimize channel losses, reflections, crosstalk
- Equalize if necessary

Managing Channel Electrical Properties

- Channel Topology
  - PCB or cable?
- Component Selection
  - PCB
  - Connectors
  - Cables
- “Sneaky PCB tricks”
  - Exotic dielectric materials
  - Trace layer selection
  - Back drilling
- Transceiver Characteristics
  - Single-ended or differential?
  - Driver voltage swing
  - Receiver sensitivity
  - Equalization

Dielectric Loss

- Telegrapher's equation: $\gamma = \sqrt{(R + jwL)(G + jwC)} = \alpha + j\beta$

where attenuation = 20 $\log_{10} e^{\mathrm{Re}\,\gamma}$ = 20 $\log_{10} \exp \sqrt{(RG-\omega^2 LC)}$

- Dielectric constant of the medium, $\varepsilon = \varepsilon(1 - j \tan \delta_l)$,

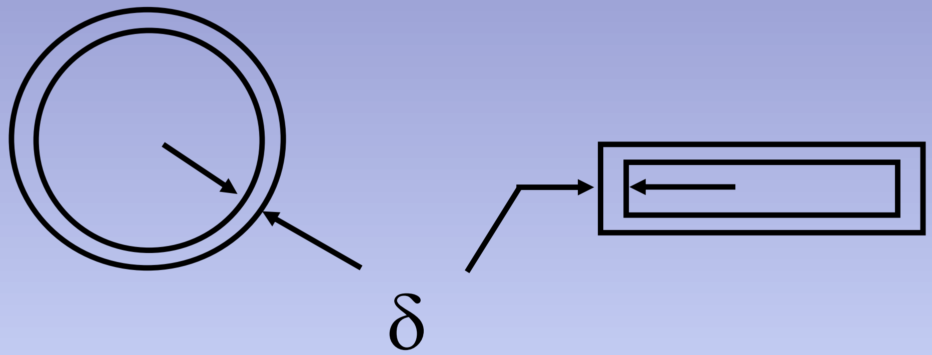
so $G = \sigma C/\varepsilon = \sigma C/D_k = \omega C \tan \delta = \omega C \tan D_f$

Increasing frequency -> shunt losses

- Typical values:

Material	ε	tan δ
FR-4 (normal glass-epoxy card material)	4.5	0.02
NELCO 4000-13	3.7	0.008
Megtron-6	3.5	0.005
PTFE (Teflon)	2.1	0.0003

Conductor (skin) Loss



$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

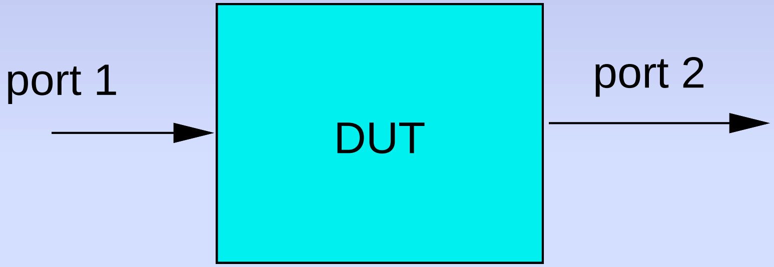
- Charge repulsion forces current to outside of conductors
- Increases effective resistance as frequency increases
- For Copper,

$$\delta = \frac{0.0661}{\sqrt{f}} = 6.61\text{x}10^{-4}\text{ mm} = 0.026\text{ mils at 10 GHz}$$

- Conductors for high performance cables are often Ag-plated - all the current is carried in the plating

s parameters

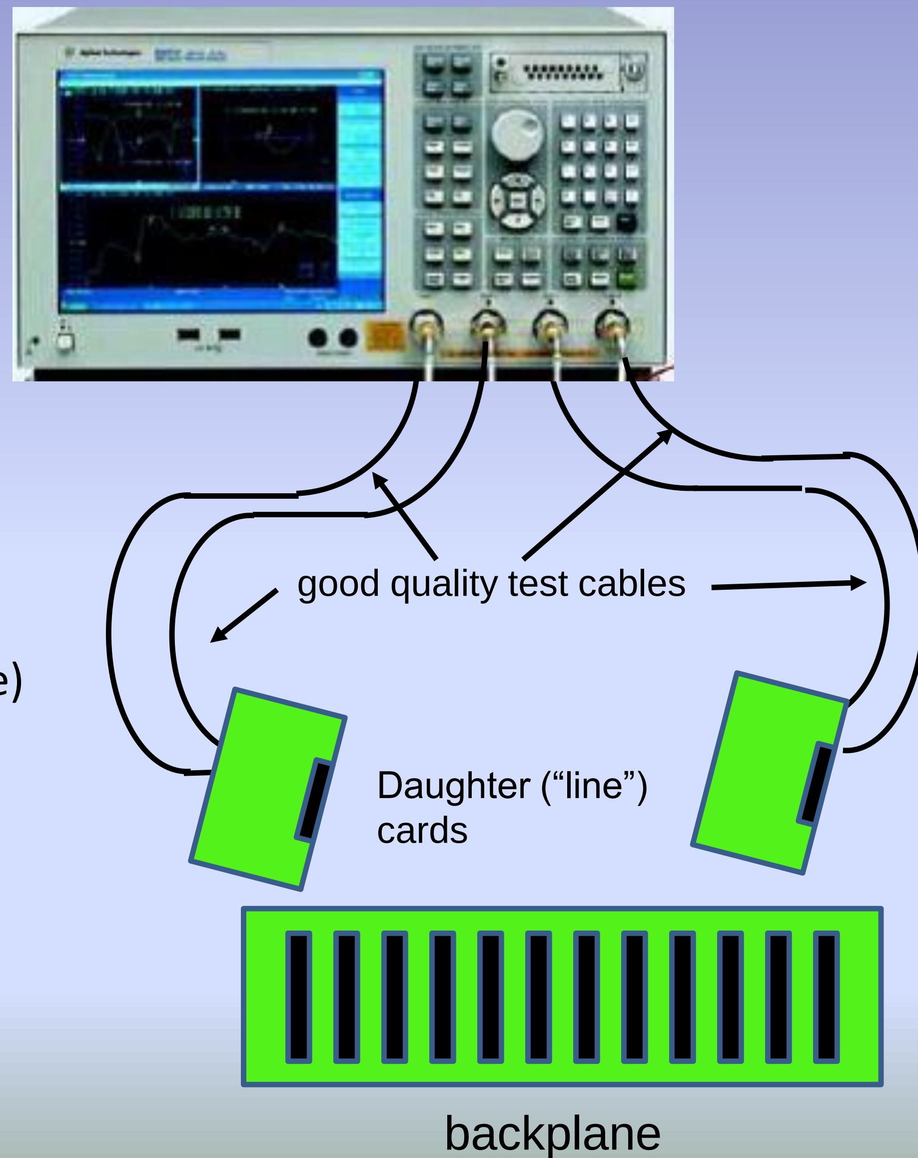
- Describe power transfer relationship between two ports of a DUT
- Normalized to 50 Ohms
- Can be related to other quantities; e. g., Z1 = Z0 (1+s11)/(1-s11)



sxy = power observed at port x due to power applied at port y
s11 = return loss (reflection) at port 1
s21 = insertion loss, port 1 to port 2
s22 = return loss (reflection) at port 2

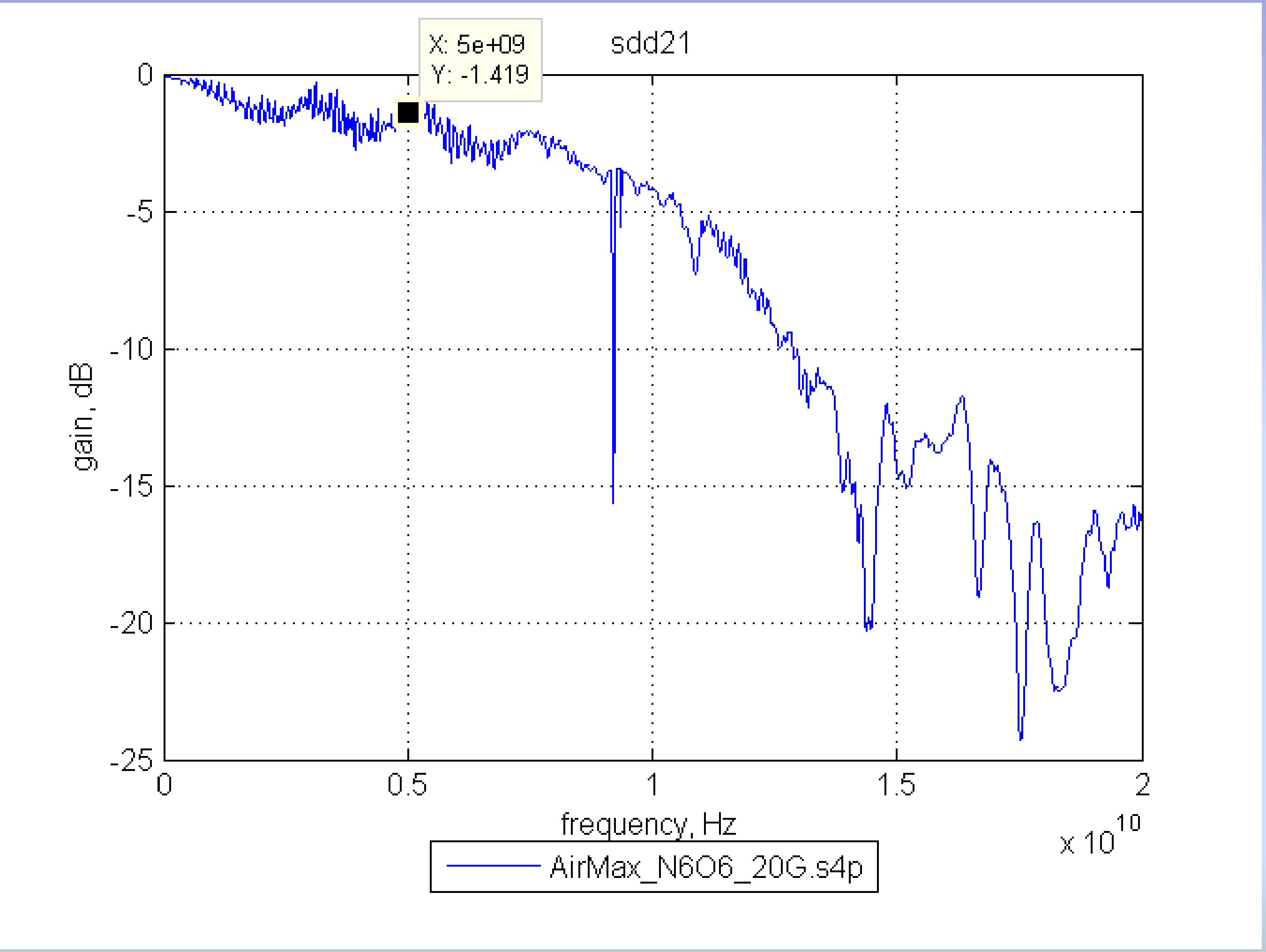
Vector Network Analyzer

- Frequency-swept stimulus and response
- Two or more ports
- No location information
- Displays results in various formats
  - Log magnitude/phase
  - Smith Chart
  - Time domain (w/ software)



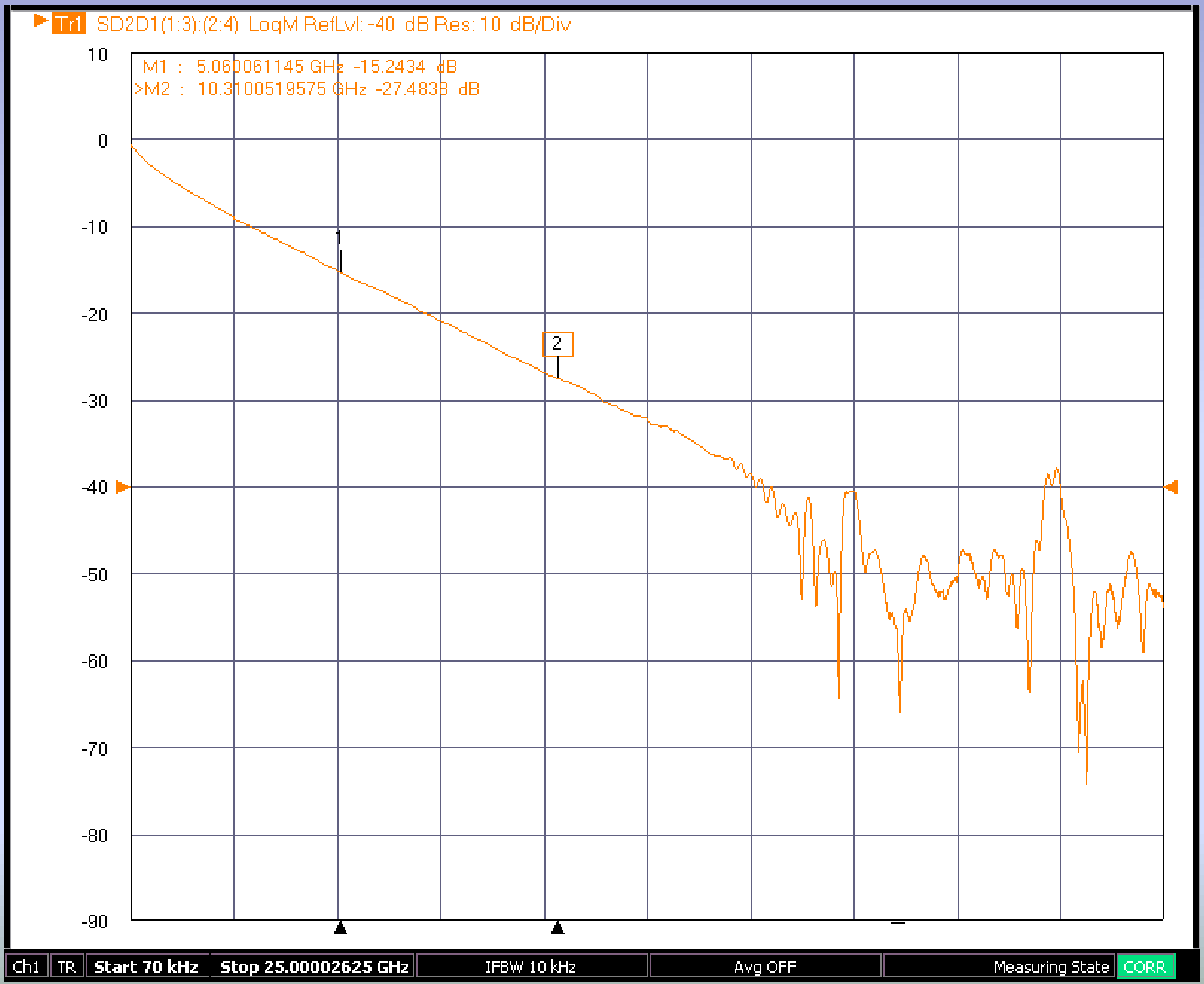
Connector example

Insertion loss

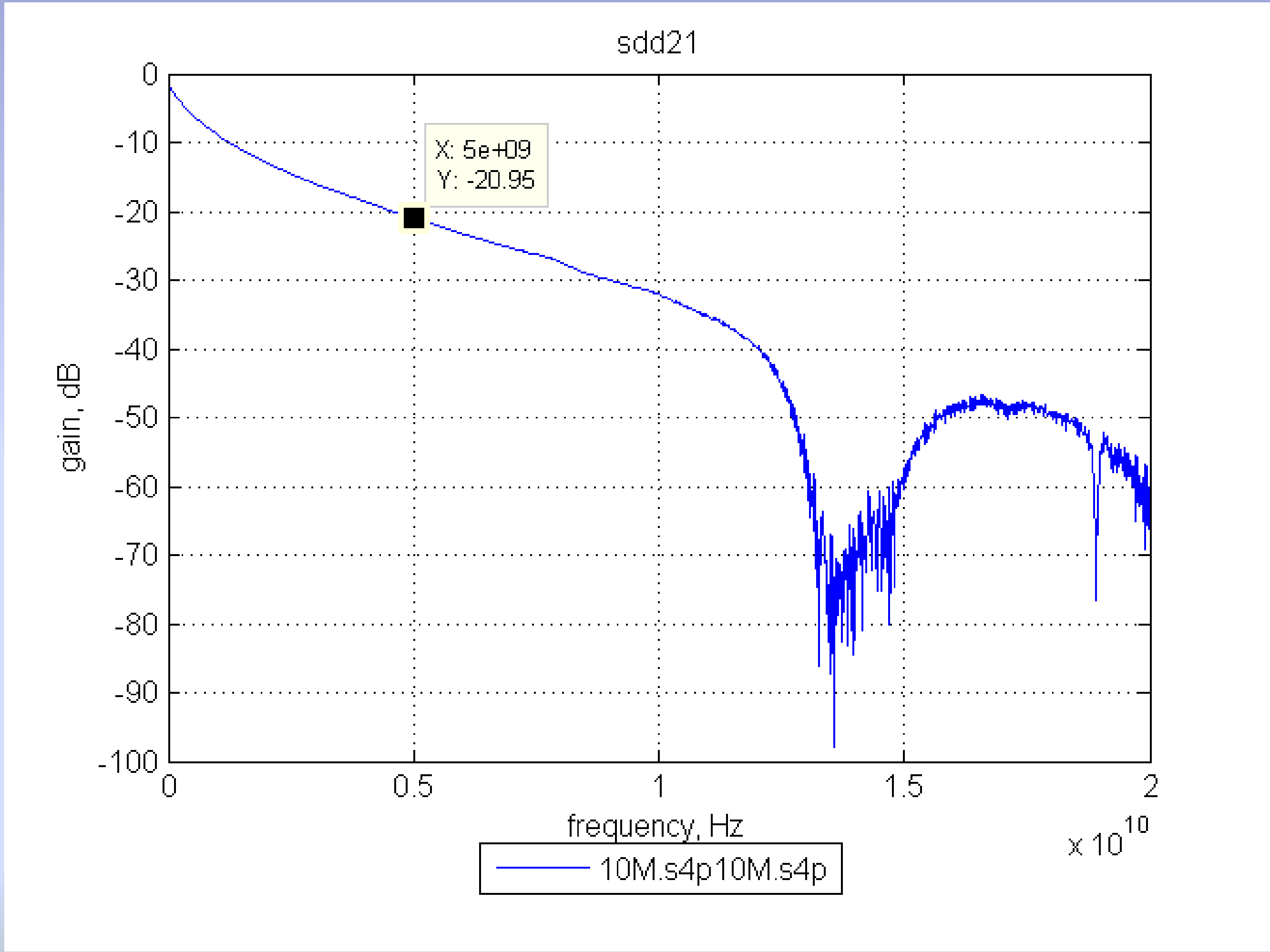


Card wiring example

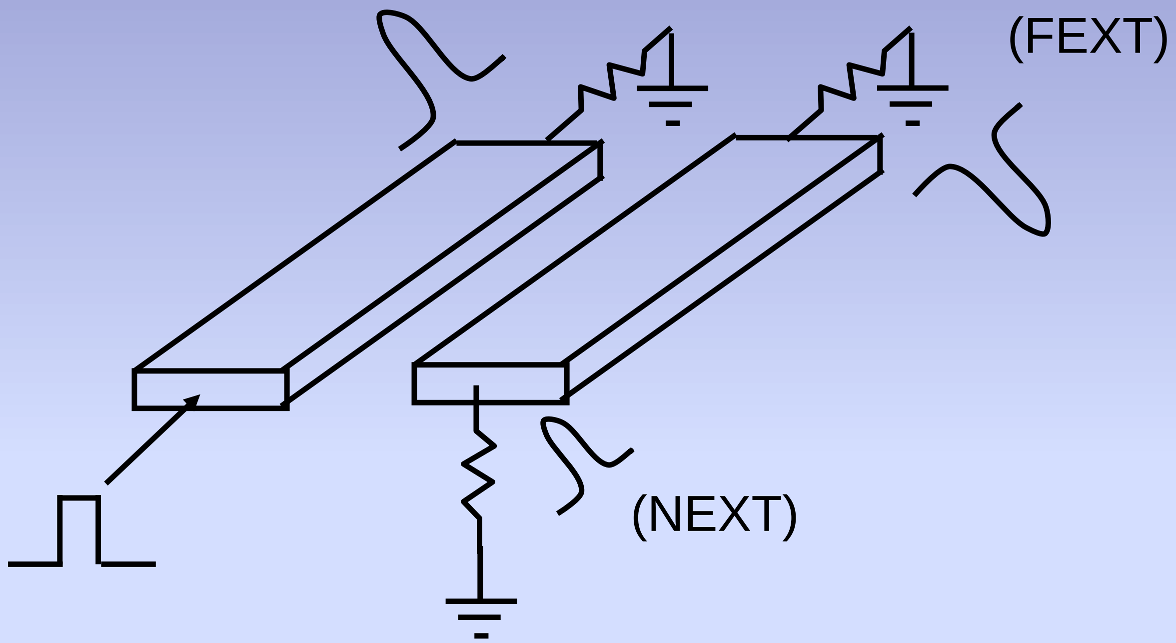
Insertion loss



Cable example
10 meter AWG 26 insertion loss



Crosstalk



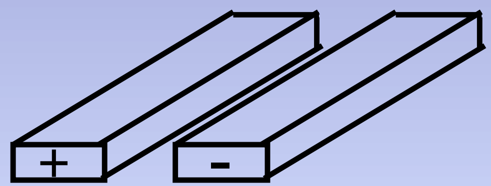
Coupling between conductors:

$$i = C_m \frac{dV}{dt}, \quad v = L_m \frac{di}{dt}$$

it's all about slope, not transition (rise, fall) time!

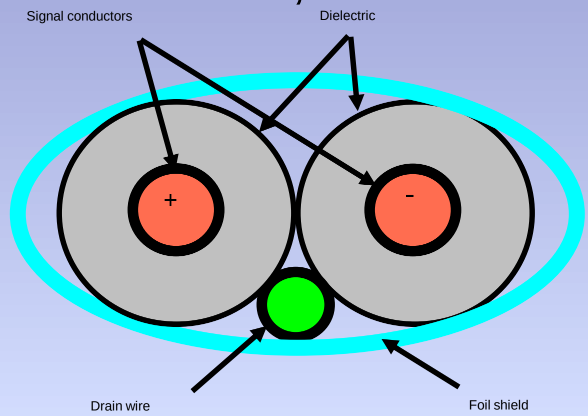
Differential Links

- Each signal transmitted by a pair of conductors, driven 180 degrees out of phase



card wire

cable

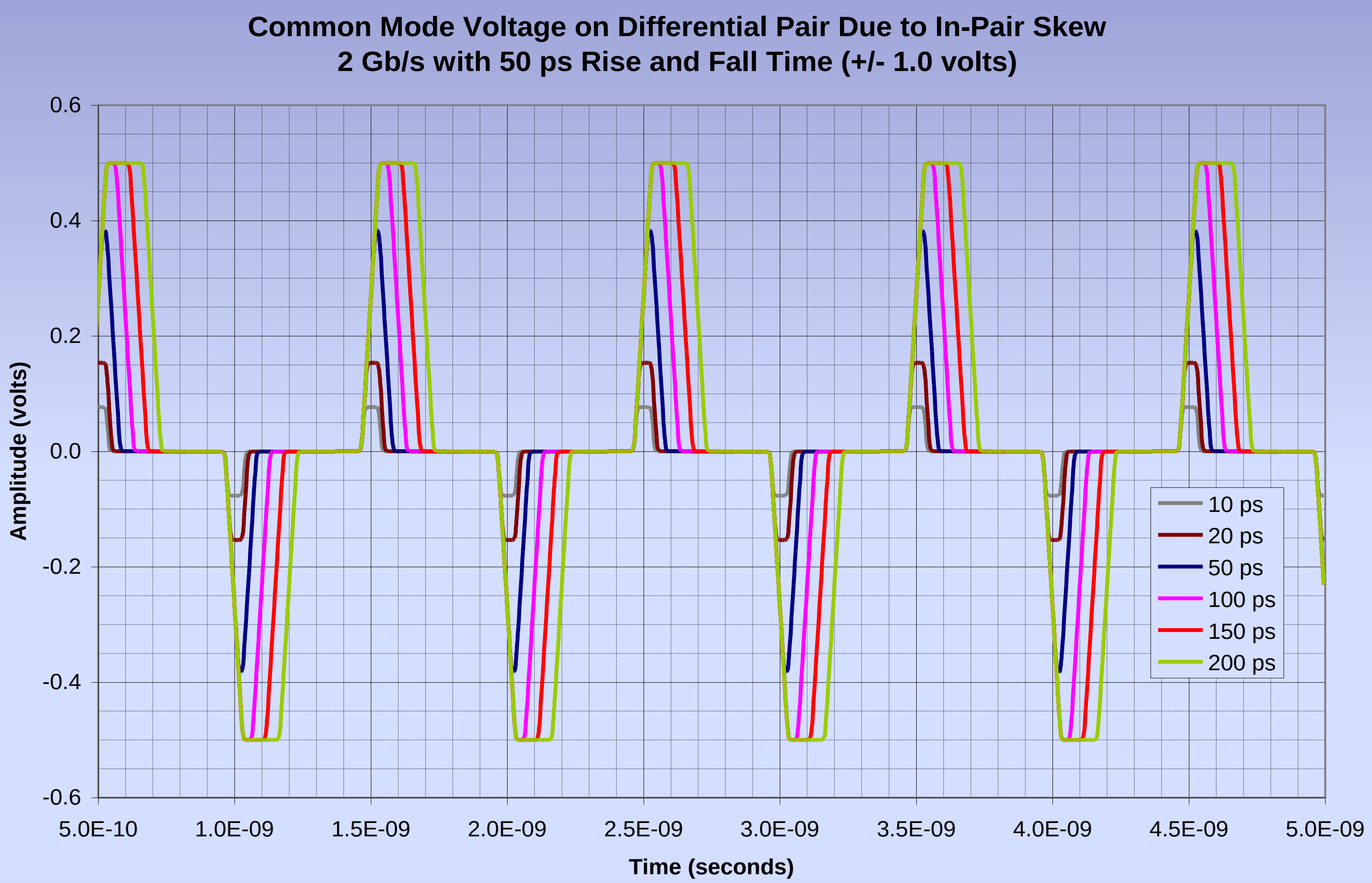


- Considerations:
  - greater common mode noise immunity than single-ended
  - less EMI radiation than single-ended
  - must consider and measure differential quantities
    - analysis, simulation methods
    - test equipment, fixtures
  - additional propagation modes are possible

Differential Pair Skew

- Two types:
  - in-pair (between legs of pair)
    - Due to difference in propagation delay between legs of pair
    - Manifested as "excess attenuation"
    - Spec. limits pretty tight - causes differential imbalance, and can cause EMI problems due to common mode energy
    - Not uniform with length in cables
    - Small amounts of skew create significant common mode noise
    - As little as 1% of bit width for skew can have significant EMI effects
    - As little as 10% of bit width skew creates CM signal of equivalent amplitude to initial signals
  - pair to pair (between pairs)
    - difference in propagation delay between pairs
    - modern interfaces relatively insensitive to it (500 ps limit) - it's corrected in the design

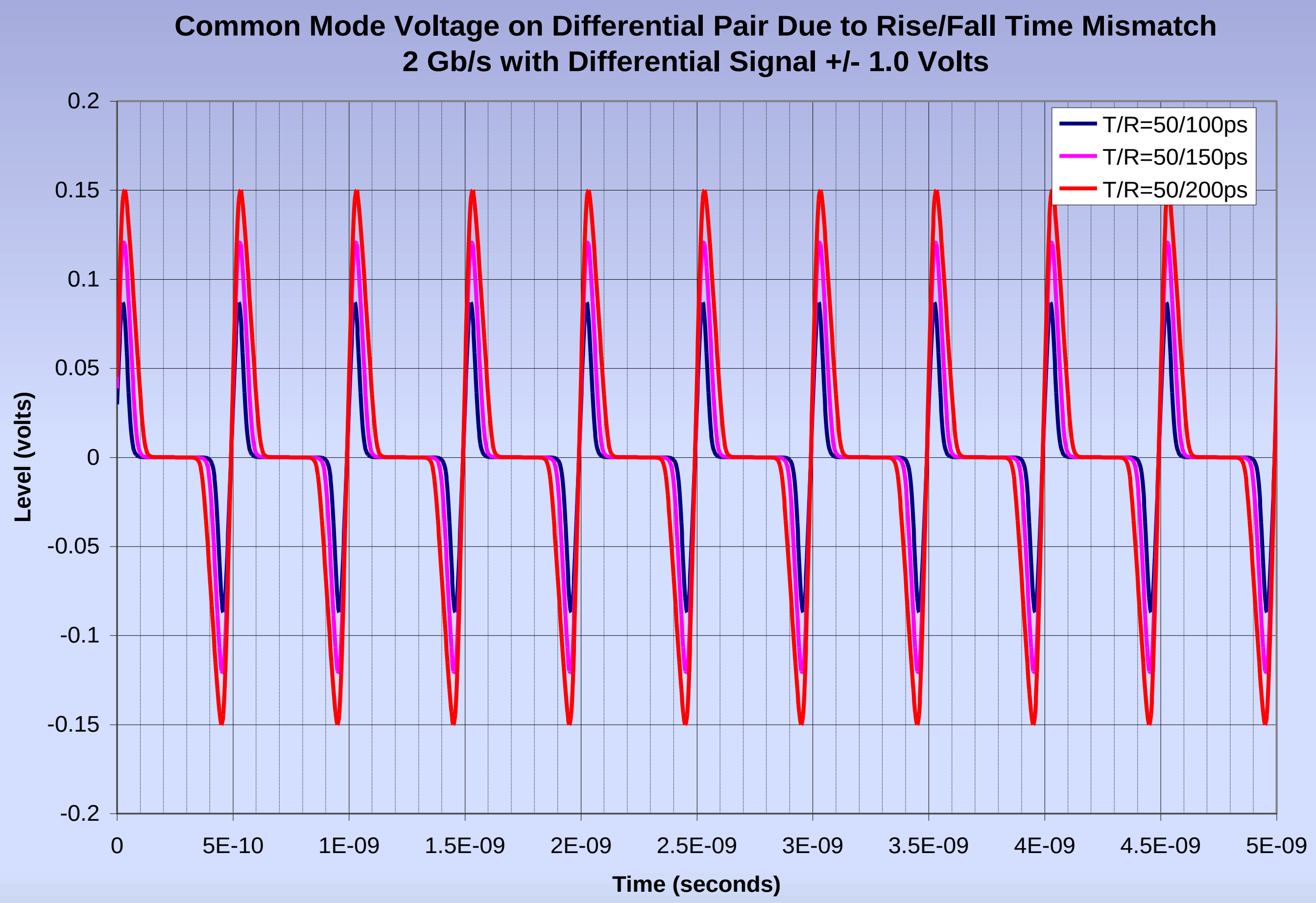
Skew


Common Mode Voltage on Differential Pair Due to In-Pair Skew
2 Gb/s with 50 ps Rise and Fall Time (+/- 1.0 volts)
0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Amplitude (volts)
5.0E-10
1.0E-09
1.5E-09
2.0E-09
2.5E-09
3.0E-09
3.5E-09
4.0E-09
4.5E-09
5.0E-09
Time (seconds)
10 ps
20 ps
50 ps
100 ps
150 ps
200 ps

Rise/fall time mismatch

- Small amounts of mismatch create significant CM noise
- Not as significant as skew, but harder to control!
- Telltale is significant 2nd harmonic content

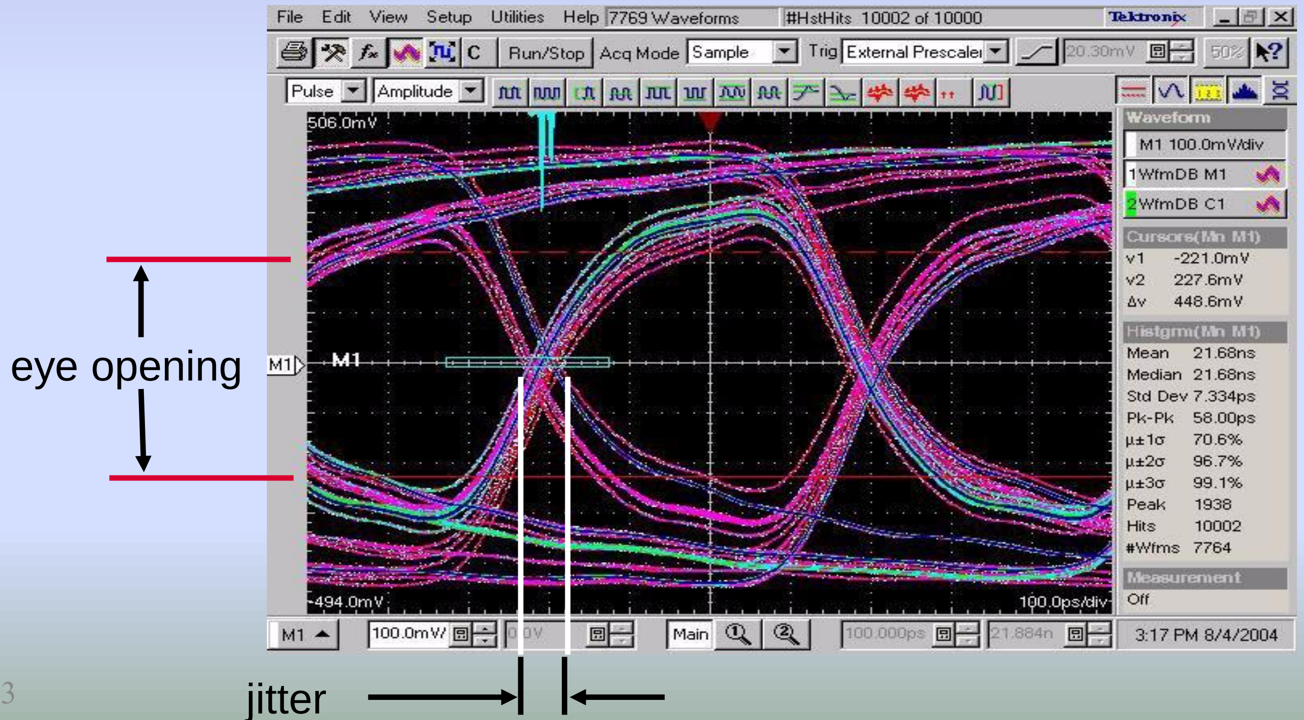
Rise/fall time mismatch



Channel Performance Evaluation

Eye opening and Jitter

- Measures time domain performance of link
- Measured using PRBS or application-specific data pattern (e. g., CJTPAT)
- Eye opening -
  - –vertical "black space" in middle of many overlaid bits
  - –minimum opening needed for receiver to distinguish between "1" and "0"
- Jitter - horizontal width of zero crossing of overlaid waveforms



Eye opening and Jitter - test setup

Pattern or BERT Gen.

Sampling or real-time oscilloscope

Clock

PRBS7, 9, ..31 pattern
Vout ~= 1 Vpp
Trise ~= 30 ps
xx Gb/s

Color-graded display
Infinite persistence
x Histogram hits

Asynch. Crosstalk Source

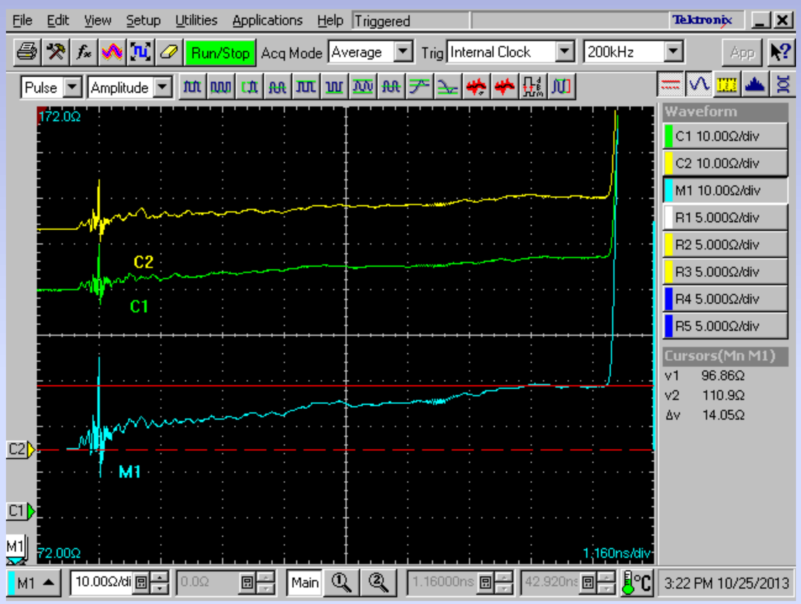
DUT (backplane, cable, etc.)

(terminate unused ports with 50 Ohms to Ground)

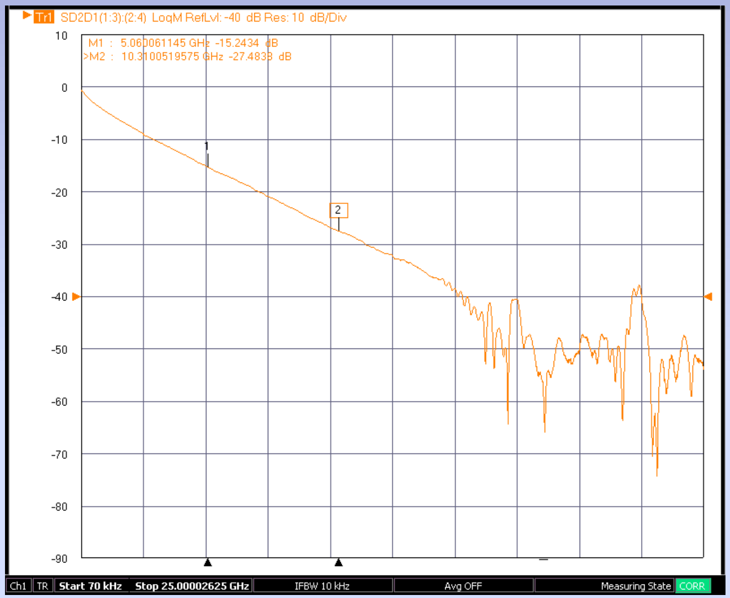
Channel example 1

30 inch PCB trace pair

Impedance



Insertion loss



15 dB@5 GHz

Equalization

- Compensates for frequency-dependent channel loss
- Implemented in
  - Tx or Rx or both
  - Cable, active or passive (e. g., RC)

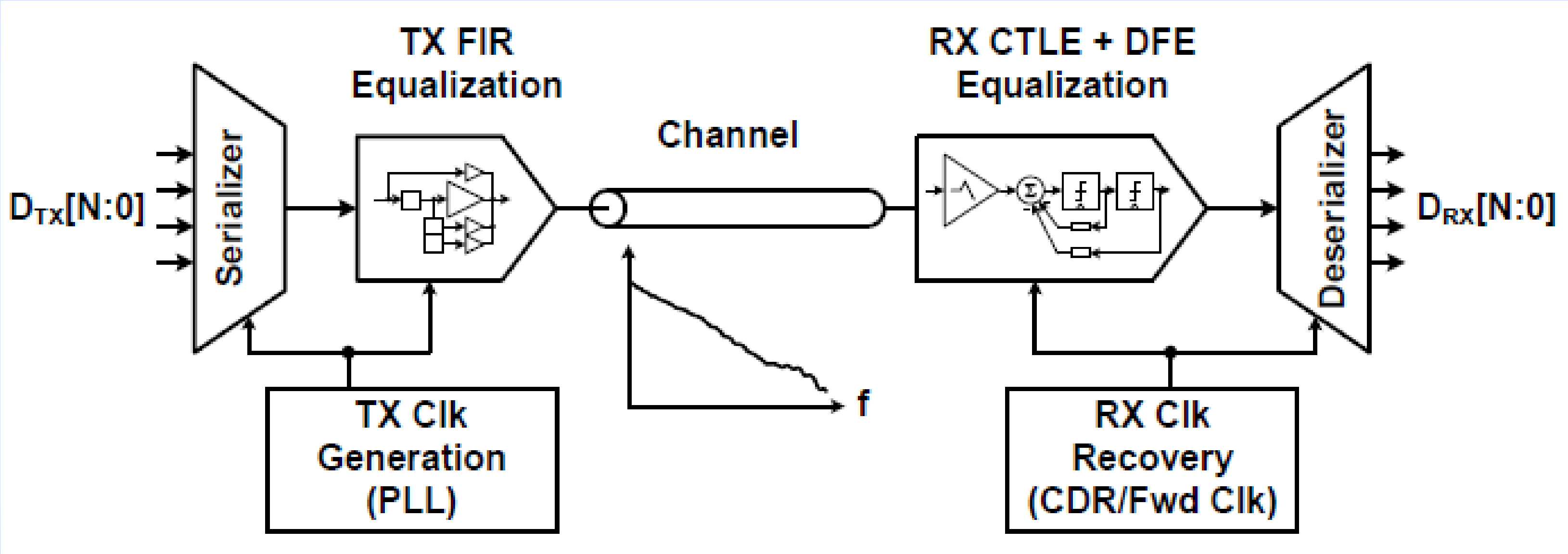
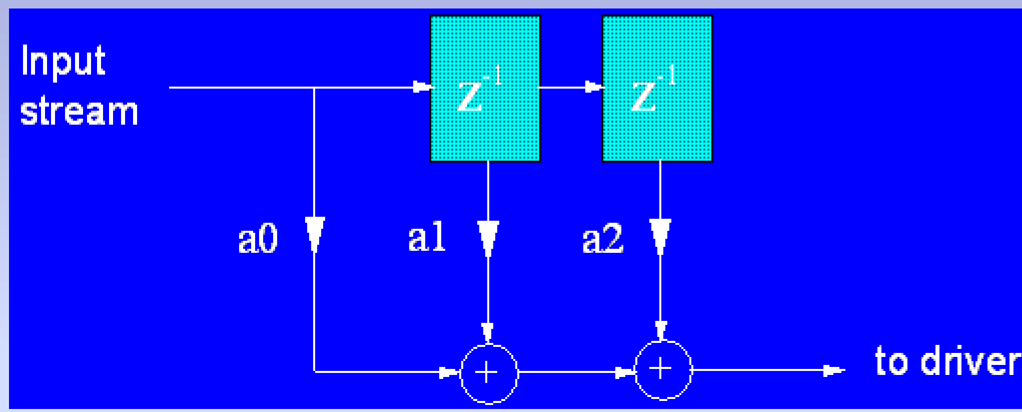


Figure courtesy of Texas A&M Univ.

Transmit Equalization

- One technique: Digital FIR (Finite Impulse Response) filter function applied to input stream ("Feed Forward Equalization")

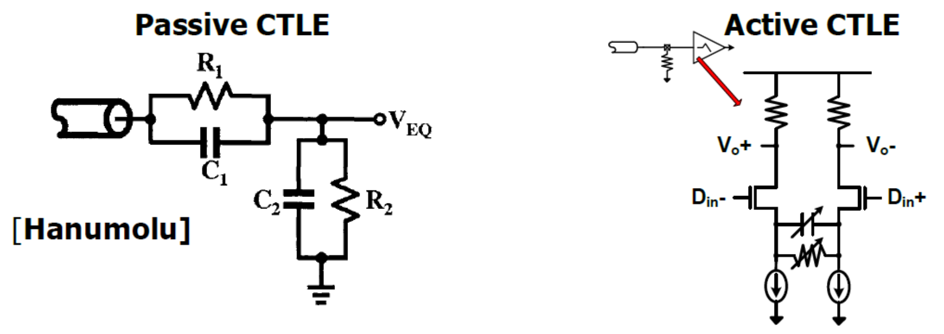


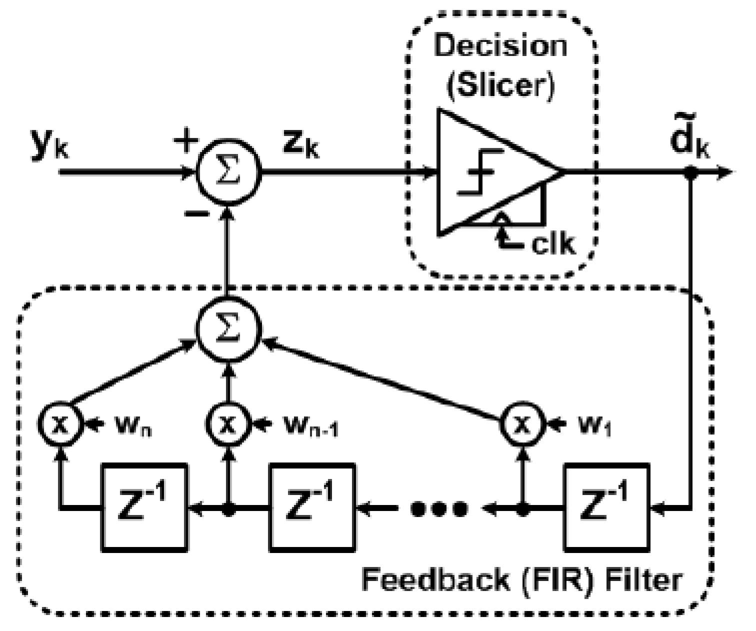
- Transfer function: $Y(z) = \sum_{j=0}^{M} a_j z^{-j}$

- Objective: Create inverse transfer function of channel
  Communications theory -> "matched filter" (RRC)

Receiver Equalization

- Usually a combination of
  - Continuous Time Linear Equalization (CTLE)
  - Decision Feedback Equalization (DFE)



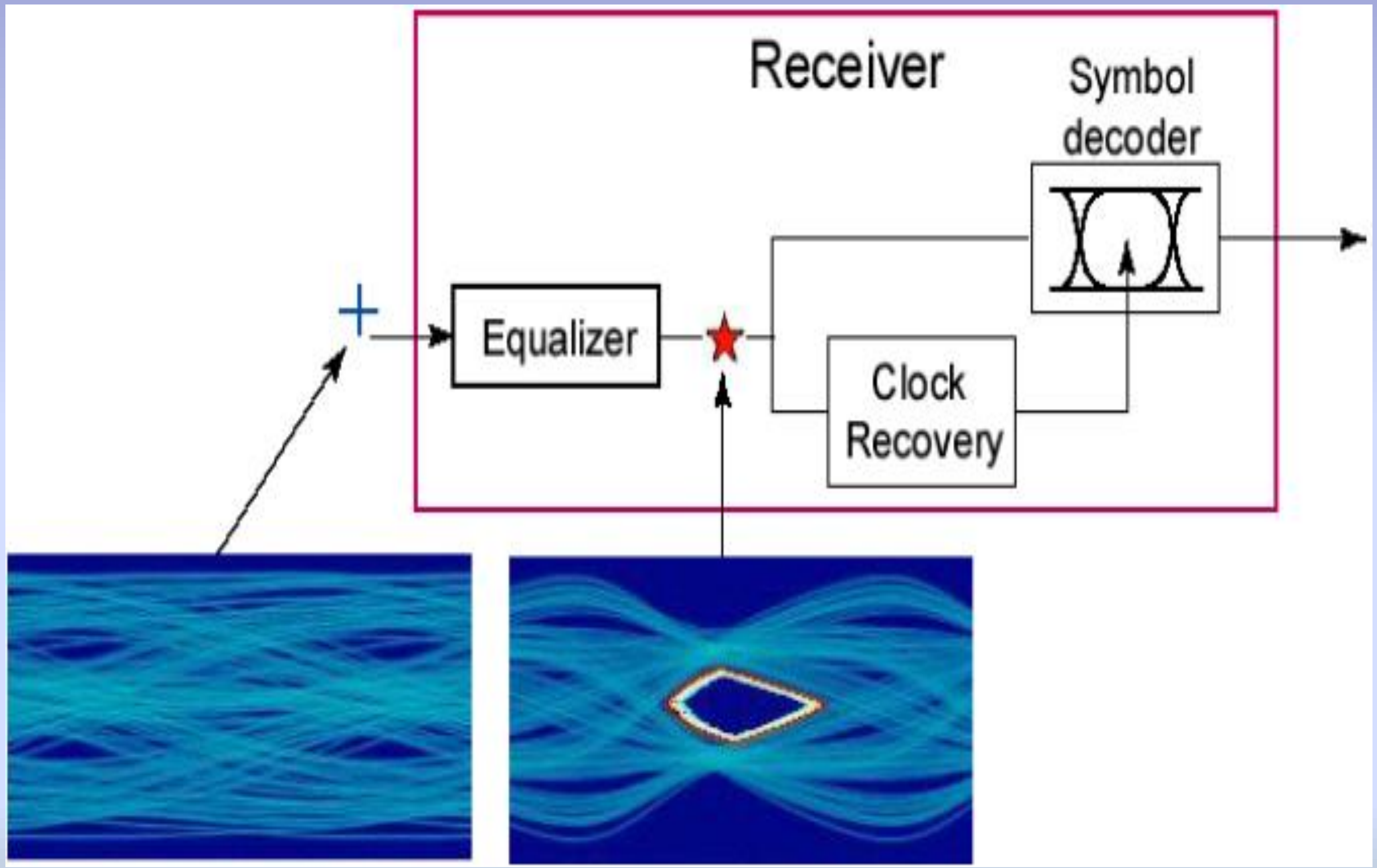


- Different structures equalize different channel distortions

Figures courtesy of Texas A&M Univ.

Receiver Equalization

- Receiver equalization can result in dramatic improvement in eye opening



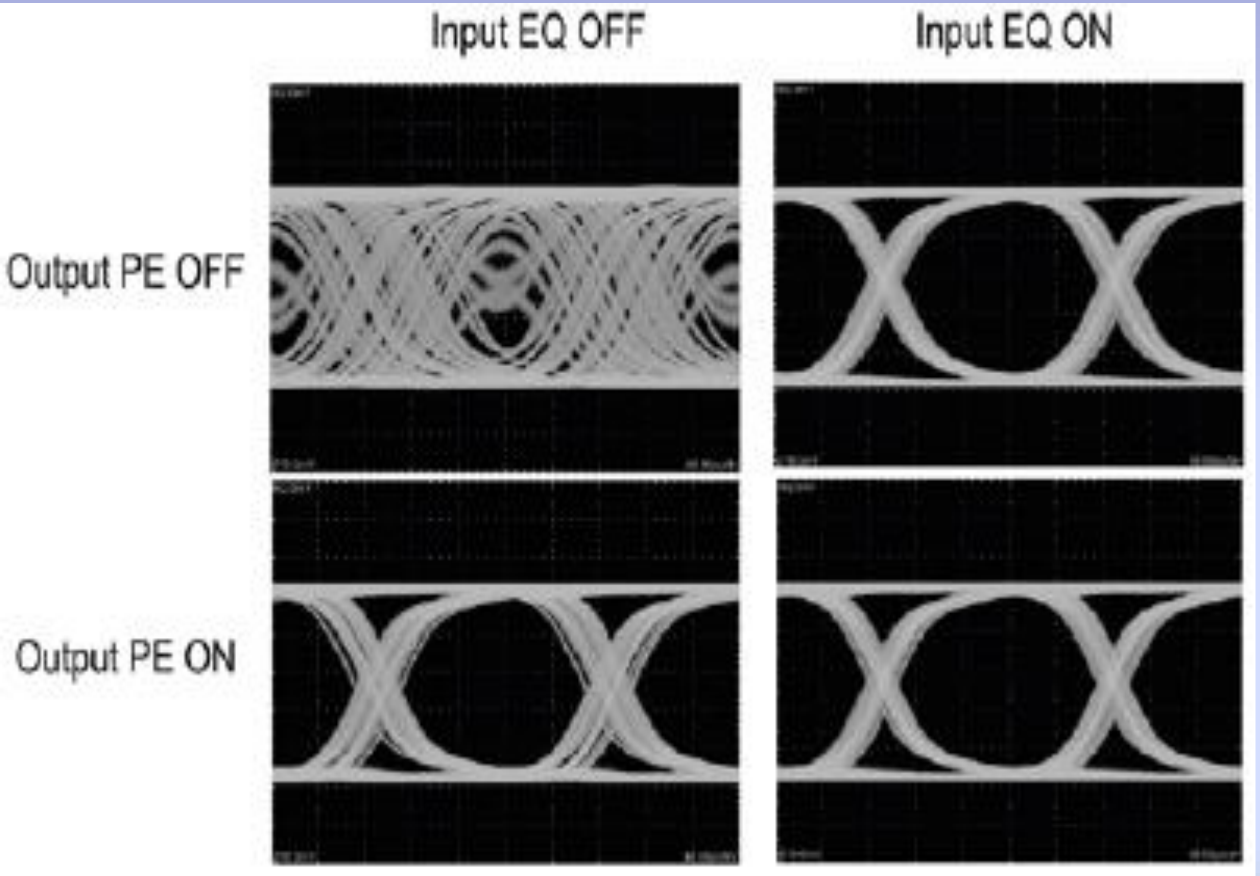
From Moreira, et. al., IEEE 2006 Int'l Design & Test Workshop

Equalization

20” backplane, 4.25 Gb/s

No equalization

Rx equalization only

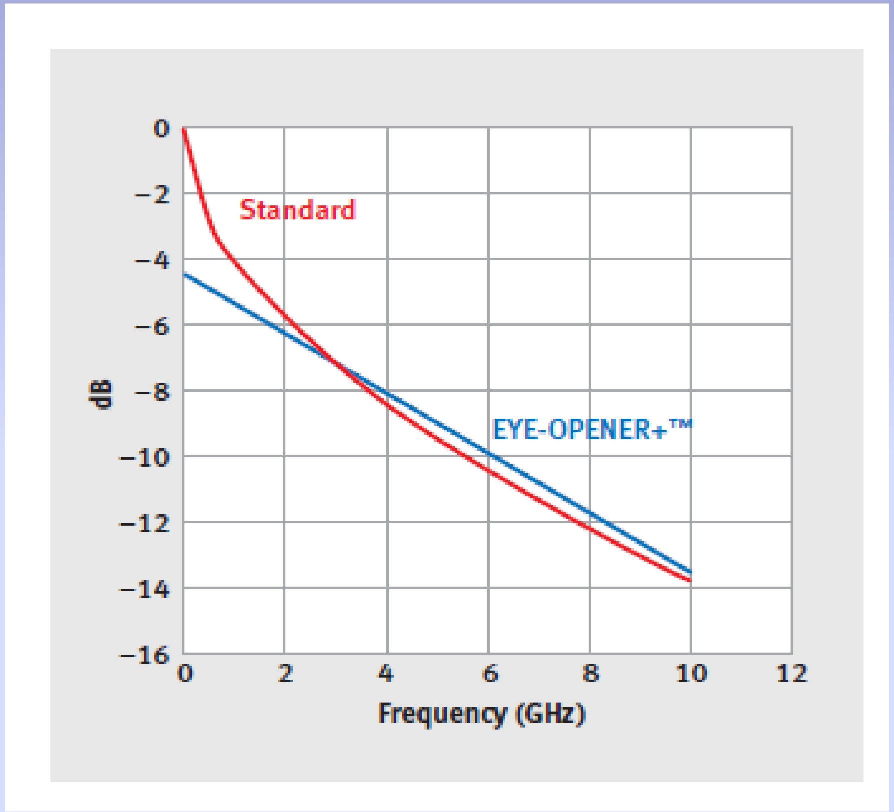


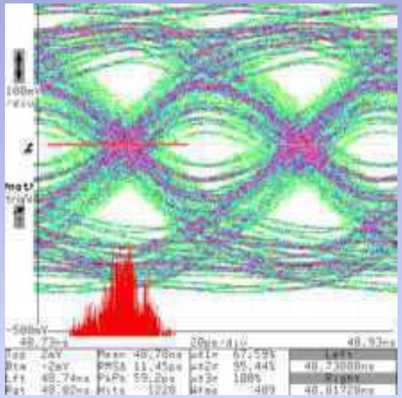
Tx equalization only

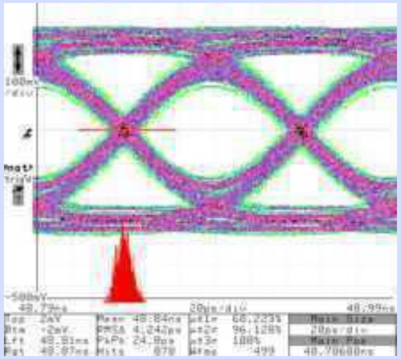
Tx and Rx equalization

Self-equalized cable example

5 meter parallel pair cables







Plots courtesy of W. L. Gore & Assoc.

Simulation

- Tools
  - Agilent ADS
  - Ansys Designer
  - Cadence Allegro Sigrity
  - Matlab
  - Mentor HyperLynx
  - MUS&T FEMAS

- Models
  - SPICE
  - Touchstone files
  - IBIS, IBIS-AMI

References

Standards

- ANSI T10 (SCSI), T11 (Fibre Channel) documents
- EIA-364-xxx test methods documents, available at http://www-ec-central.org
  - 364-90 Crosstalk, -101 Attenuation, -102 Risetime degradation
  - 364-103 Propagation delay, -107 Eye patterns/jitter,
  - 364-108 Impedance, Reflection coeff., VSWR
- IEEE standards
- InfiniBand specification, volume 2, available at http://www.infinibandta.org
- SFF-8410 and other high speed serial channel testing documents

Other

- Agilent Technologies: Understanding the Fundamental Principles of Vector Network Analysis," AN 1287-1, available at http://www.agilent.com
- Bogatin, E: "Differential Impedance Finally Made Simple"
- Carey, Scott, and Weeks: "Characterization of Multiple Parallel Transmission Lines," IEEE Trans. Instr. and Meas., Sept. 1969
- "Copper Cable Electrical Testing," presentation from InfiniBand PlugFest
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- IEEE, DesignCon conference papers

References

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- Blood, W. R., Jr.: MECL Systems Design Handbook (http://www.onsemi.com/home, look for HB205)
- Bogatin, E.: Signal Integrity – Simplified, Prentice-Hall
- Bogatin, Corey, and Resso, M.: "Practical Characterization and Analysis of Lossy Transmission Lines," DesignCon 2001
- Bowick, C.: RF Circuit Design, Howard Sams, 1982
- Deutsch, A.: "Electrical Characteristics of Interconnections for High-Performance Systems," Proc. IEEE, Feb. 1998
- EIA-364 Test Methods, Electronic Components Association, available at http://www.eca.com
- Hall, S. H., Hall, G. W., and McCall, J. A.: High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices, Wiley
- Hewlett Packard Application Note 62, "TDR Fundamentals"
- Hewlett Packard Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design"
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- IBM Journal of Research & Development
- Johnson, H. and Graham, M.: High Speed Digital Design, Prentice-Hall
- Matick, R.: Transmission Lines for Digital and Communications Networks, IEEE Press
- Pozar, D.: Microwave Engineering Wiley, 2005
- Ramo, S., Whinnery, J., and Van Duzer, T.: Fields and Waves in Communication Electronics, Wiley
- Young, Brian: Digital Signal Integrity Modeling and Simulation with Interconnects and Packages, Prentice-Hall
- http://www.murata.com - capacitor calculator
- http://www.te.com, www.molex.com - connector specs., papers on card wiring losses, via characteristics, etc.

Conferences

- DesignCon – end January, in Santa Clara, CA (1/28-31/2014
- IEEE Electrical Performance of Electronic Packaging (EPEP), October
- IEEE EMC Symposium (EMCS)
  - in Raleigh, NC in August, 2014
  - Embedded SI conference
  - http://www.emcs.org
- IEEE ECTC (June), ED, ISSCC
- IEEE SPI workshop (Europe)