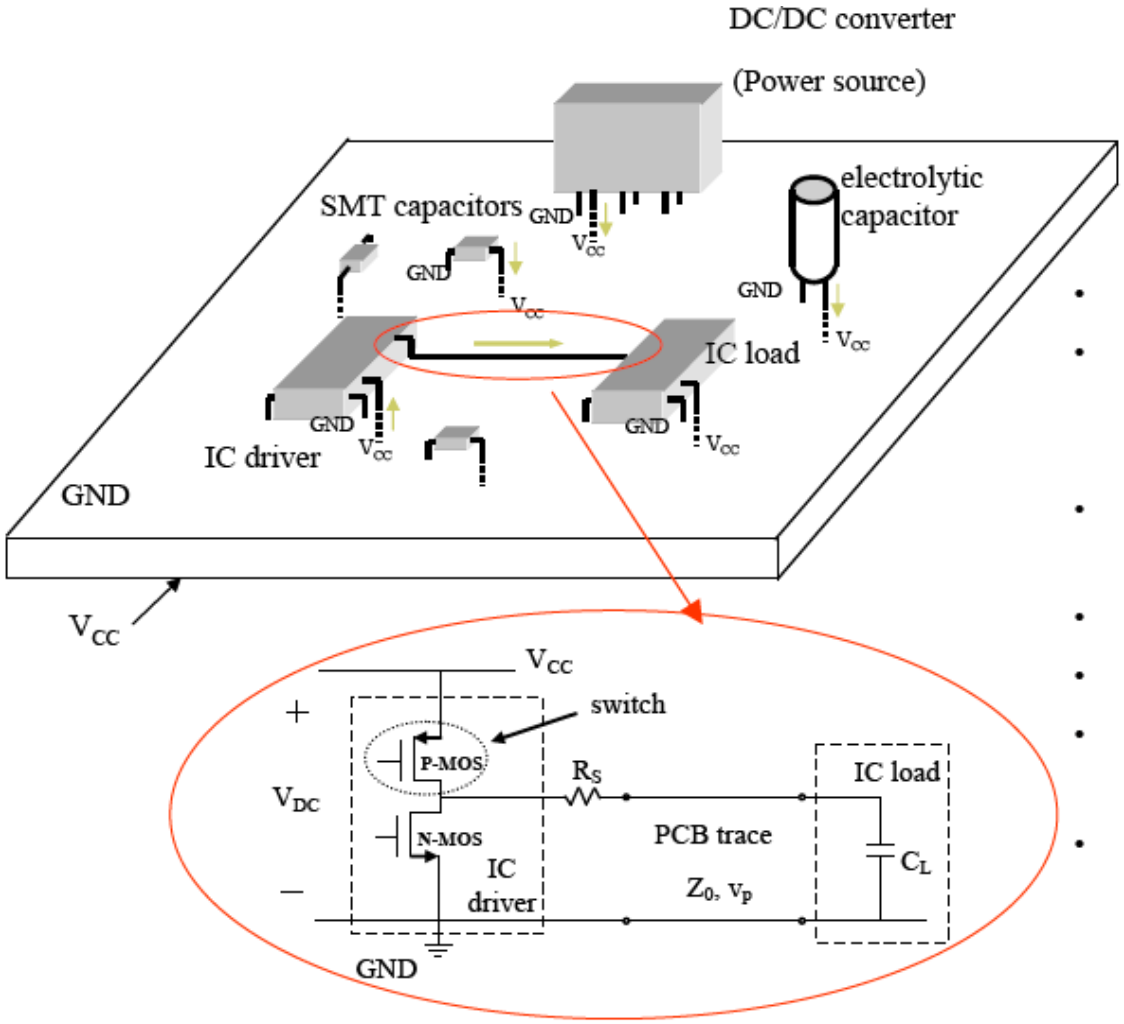
“Ultra-Thin Embedded Capacitance Laminates and how they improve the PDN and can Impact EMC”

Agenda

1. Typical/ Traditional PDN
2. The PDN using embedded capacitance
3. Some Causes of Resonance and EMC in PCB's
4. Ultra-Thin Laminates for Embedded Capacitance and the reducing impact on EMC
5. Some practical results/ case studies
6. What's Next

TYPICAL/ TRADITIONAL POWER DISTRIBUTION NETWORK

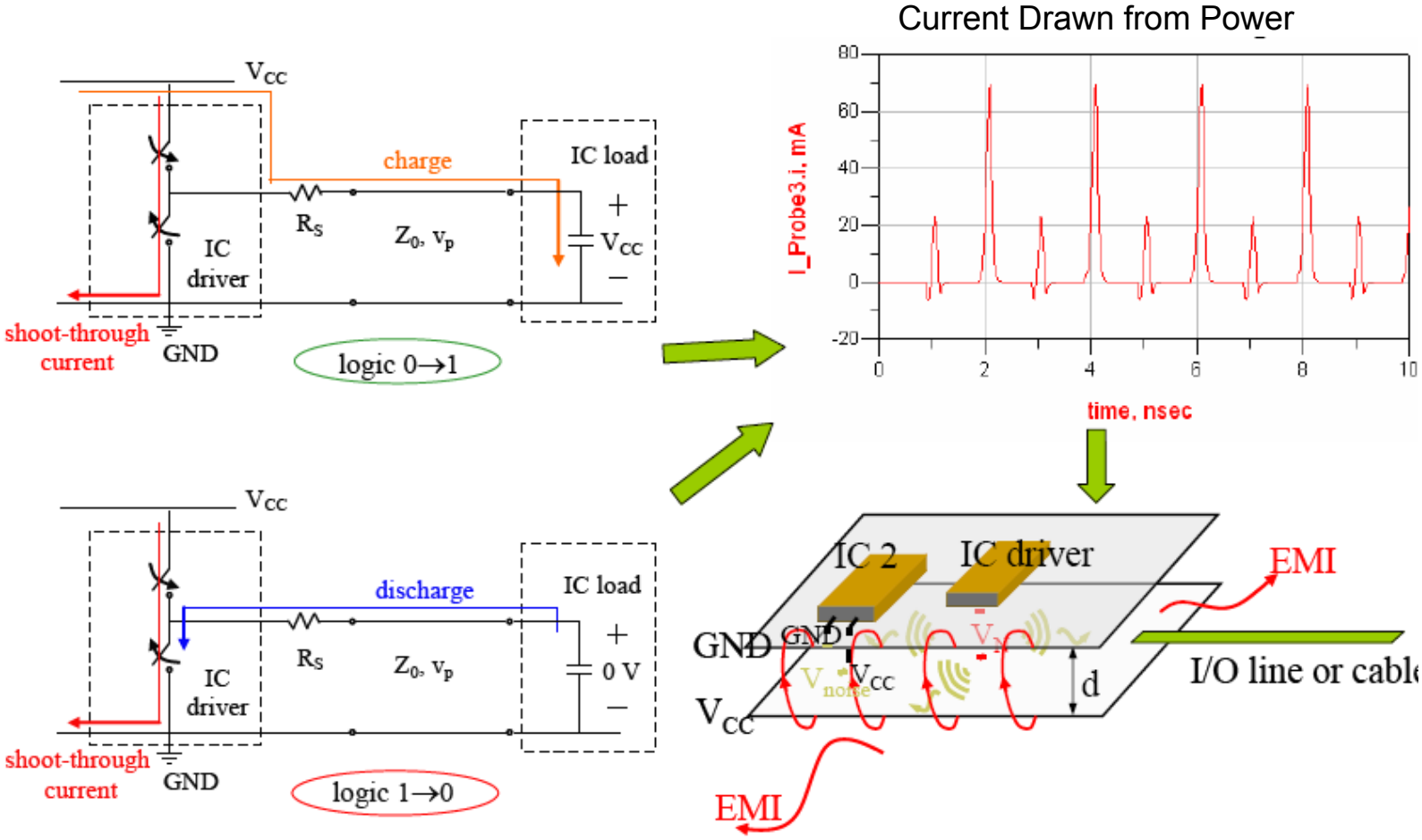
TYPICAL/ TRADITIONAL POWER DISTRIBUTION NETWORK



- Capacitor interconnects;
- Individual capacitor values and packaging forms;
- Number of capacitors needed;
- Capacitor placement;
- PCB stack-up;
- Power/ground plane pair geometry;
- Segmentation and isolation

Courtesy of Dr. Jun Fan

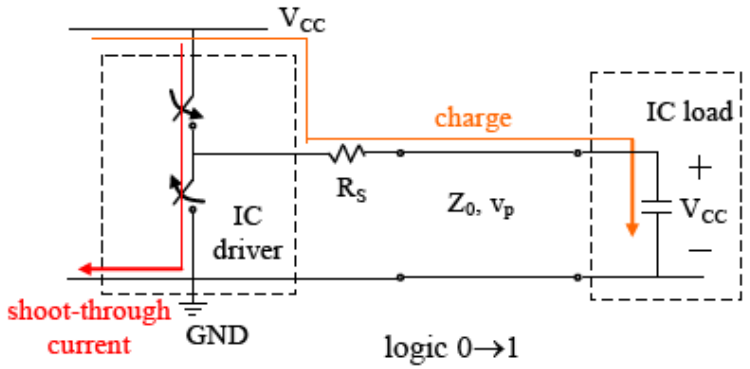
Device Switching And Noise Current

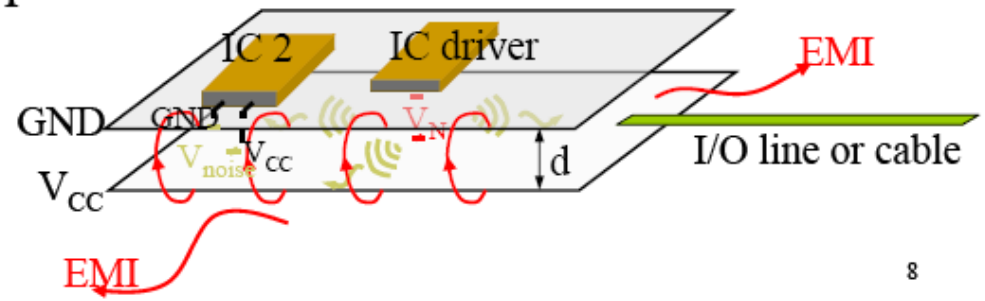


J. L Knighten, B. Archambeault, J. Fan, et. al., "PDN Design Strategies: IV. Sources of PDN Noise," *IEEE EMC Society Newsletter*, Winter 2007, Issue No. 212, pp. 66-76.

PDN Design Objectives

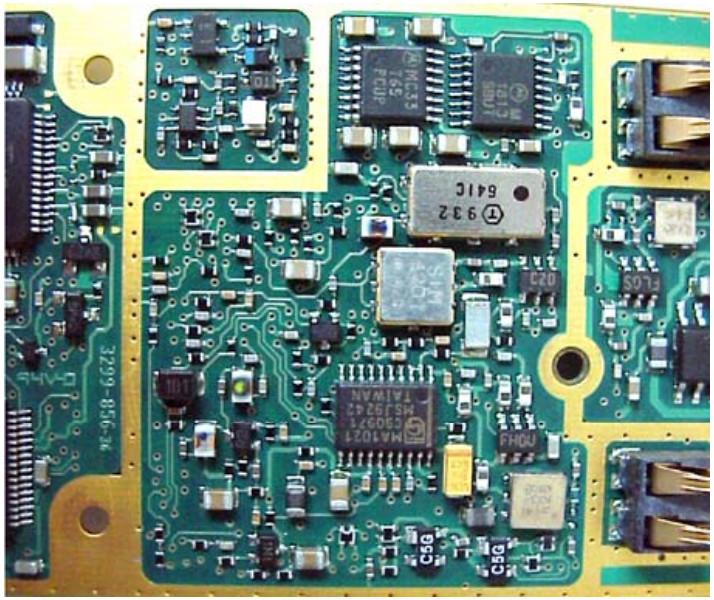
1. Ensure charge supply for logic transitions
   - Enough capacitance to store charge
   - Enough charge readily available for short transitions
2. Minimize noise voltage distribution on the V_{CC}/GND plane pair
   - Low power bus impedance over frequency
   - Noise decoupling
   - Noise isolation

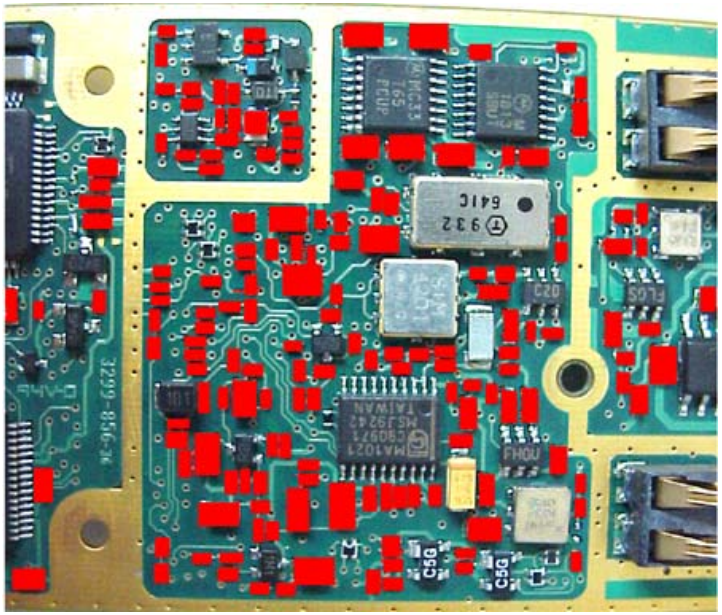




Courtesy of Dr. Jun Fan

Component density is reaching its limit





Passive components

Source: Richard Ulrich University of Arkansas

High capacitance and capacitance uniformity is the key to embed

Background / Motivation

Trends in PCB Development

Ultra-thin Laminate Approach to Embedded Capacitance Technology-

BENEFITS

- Reduction and/or elimination of surface **CAPACITORS** and resistors increases reliability of the device
- **ELECTROMAGNETIC INTERFERENCE (EMI)** from the PCB is reduced or eliminated using some ultra thin film based laminates
- **IMPEDA NCE** is greatly reduced!!!
- RoHS compliant
- Provides more efficient/ excellent **POWER DELIVERY** (charge comes directly underneath the device, 1 mil up)
- **SIMPLIFY CIRCUIT ROUTING** and eliminates 2 vias, traces, and pads for every capacitor eliminated.
- Allows for a smaller **PWB DESIGN- FORM FACTOR** if needed.

Background / Motivation

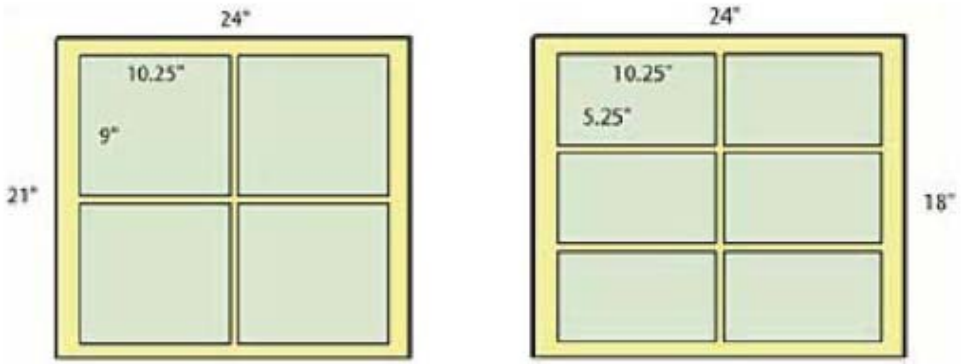
Trends in PCB Development

Cost saving

- Remove thousands of SMT capacitors
- Reduce assembly cost and time
- Improve quality associate with assembly defects
- Reduce board size

Cost Increase

- Additional cost of BC material



(a) Original board design

(b) Board design with BC

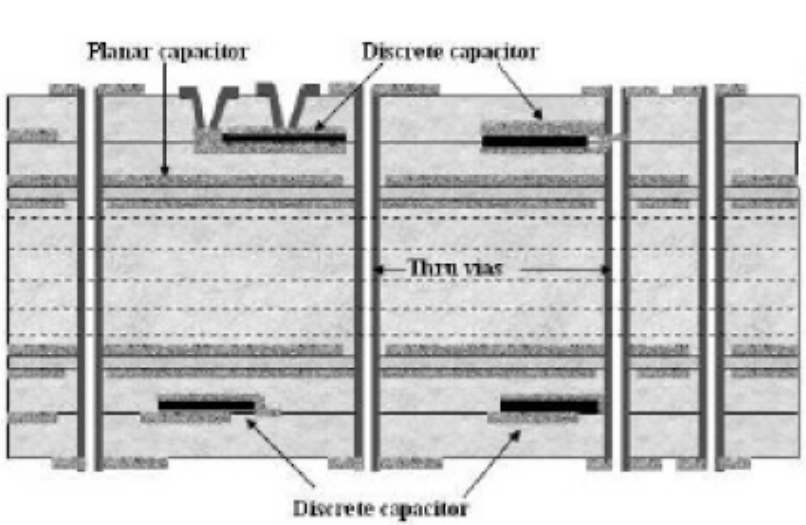
Background / Motivation

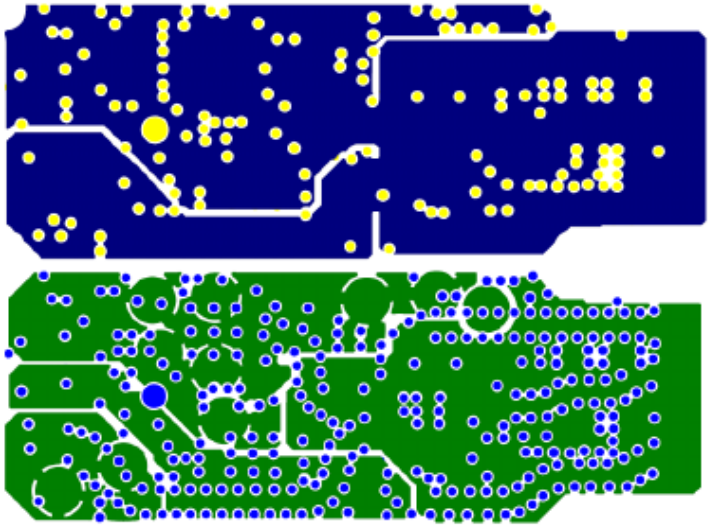
Trends in PCB Development

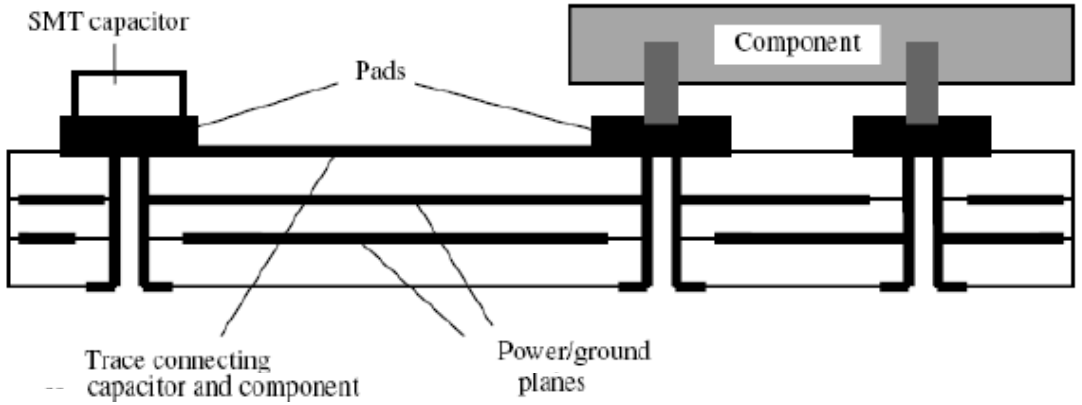
Ultra thin Laminate Approach to Embedded Capacitance Technology- BENEFITS (continued)

- **BETTER ELECTRICAL PERFORMANCE** and HIGHER RELIABILITY demonstrate the benefit of this ultra thin film based embedded capacitance approach
- **ASSEMBLY COST** is reduced by minimizing passives used
- Eliminates or minimizes issues with **POOR SURFACE MOUNT CONNECTIONS** or poor joints since the shared capacitor layer is embedded
- This technology is **NOT NEW** and has been used for many years although there is now more need for it due to densities of the newest designs
- PCB and assembly will be **LIGHTER**

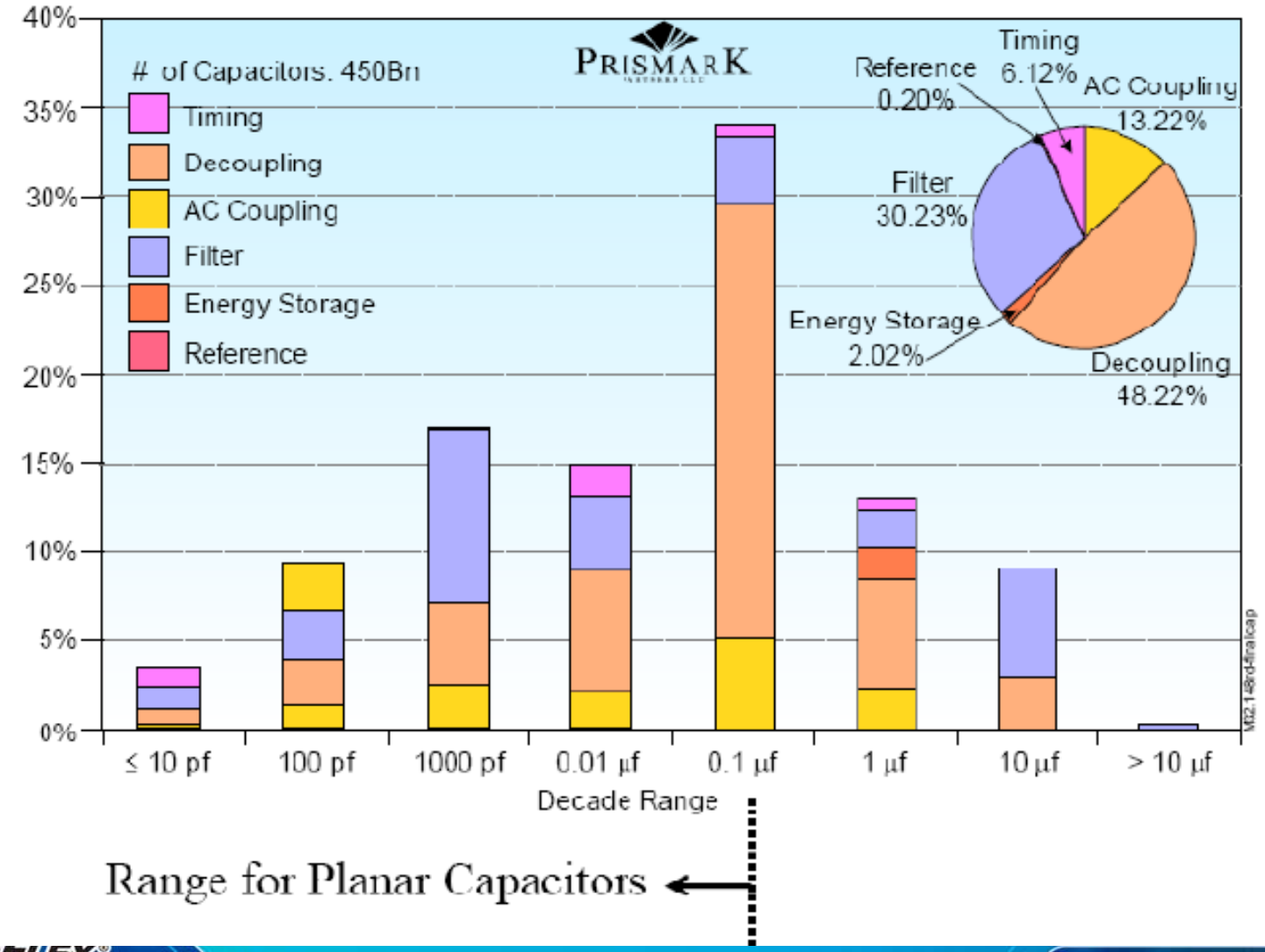
Planar Capacitor and Discrete Capacitor



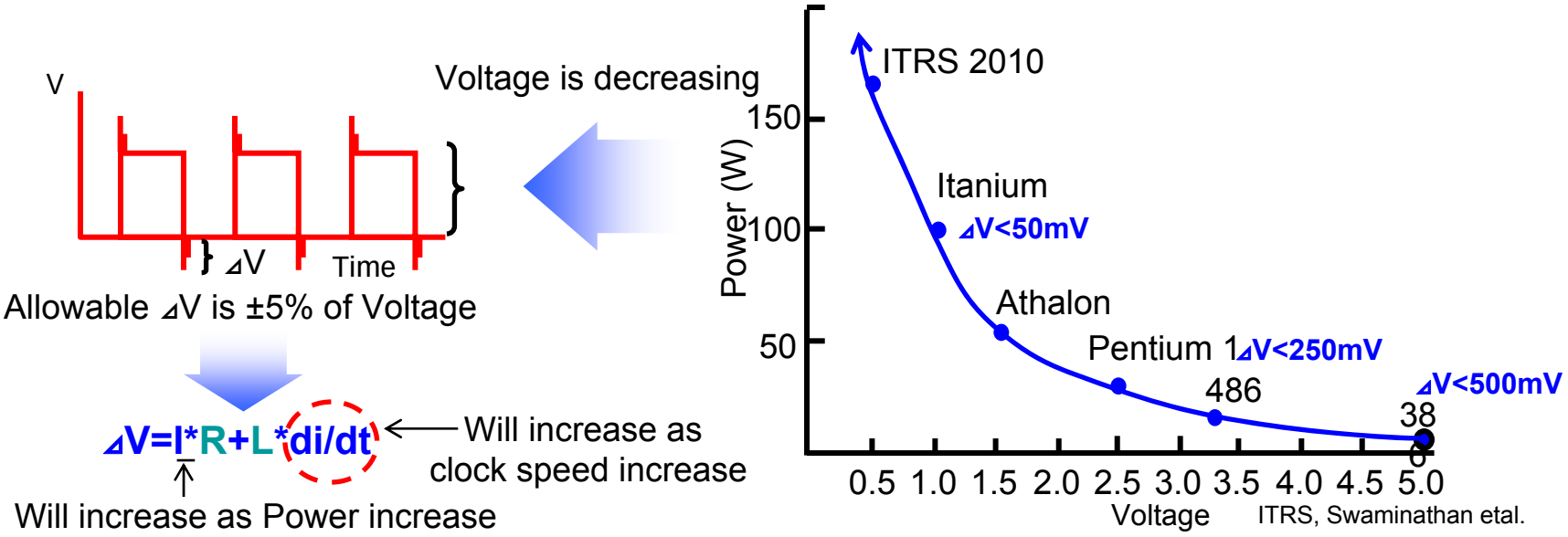


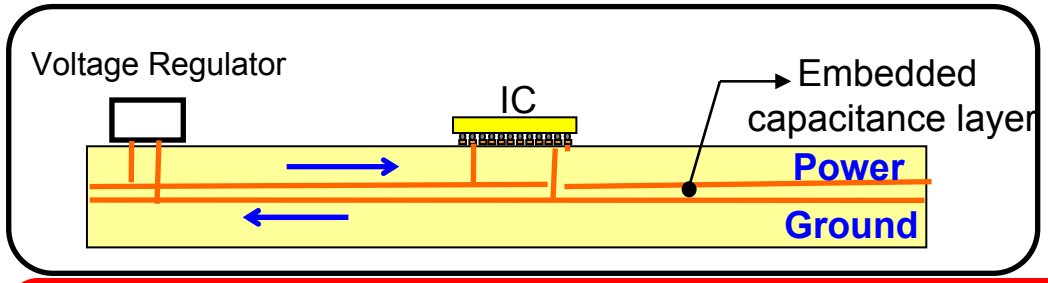


Embedded Capacitance Technology



Background of demand for PCB with Embedded Capacitor





L∝Loop area ∝Power ground thickness

"Thin" power ground plane is the key parameter to improve electrical performance at high frequency!

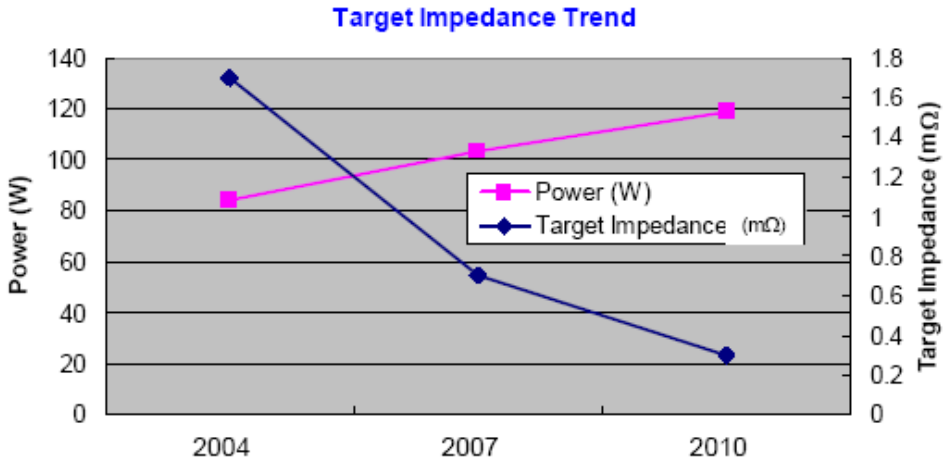
Target Impedance Concept

Target Impedance Trend through Year

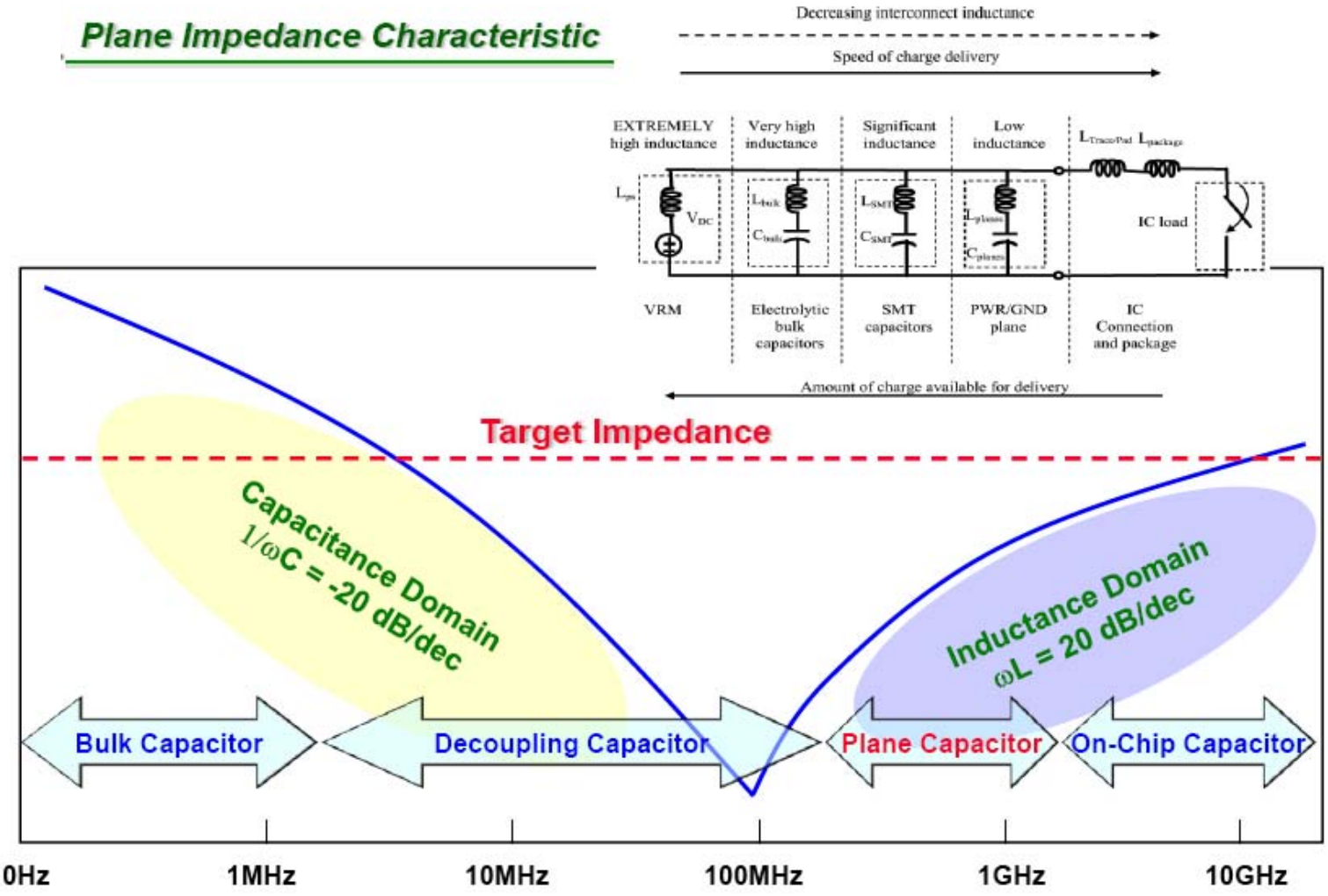
Year	Design Rule (nm)	Power (W)	Vdd (V)	Current (A)	Target Impedance (mΩ)
2004	90	84	1.2	70	1.7
2007	65	103.6	0.9	115.11	0.7
2010	45	119	0.6	198.33	0.3

ITRS, Swaminathan etal.

$$Z_{target} = (V_{dd} \times 0.05) / (I \times 50\%)$$



Plane Impedance Characteristic



Solution

High speed computing boards
Servers, Routers, Super computers

↓

CPU processor speed ↑
Operation voltage ↓
Power consumption ↑

↓

Power distribution improvement

↓

Planar embedded capacitor

Module boards
Cell phones, PDA, Note book

↓

Multiple band ↑
More functions ↑
Cost ↓

↓

Miniaturization / HDI

↓

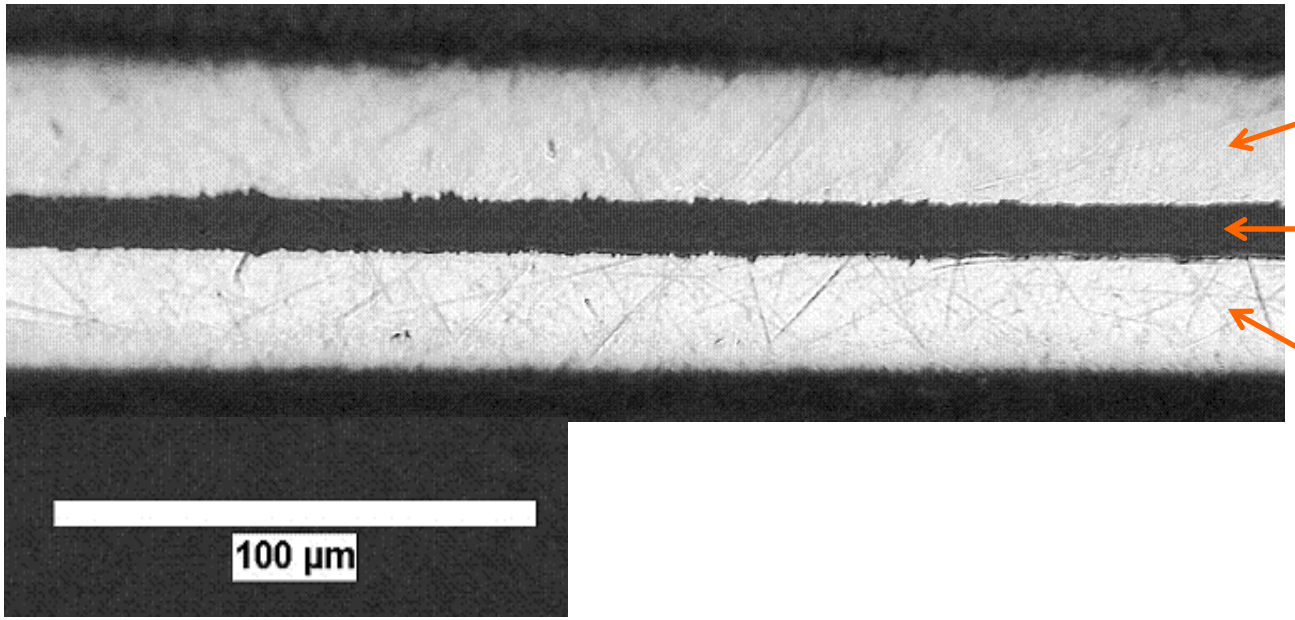
Discrete embedded capacitor

Power/Ground Plane Pair

- thin is always better

Ultra-Thin substrate for use as power distribution layer

Construction of ultra-thin substrate



Copper Foil

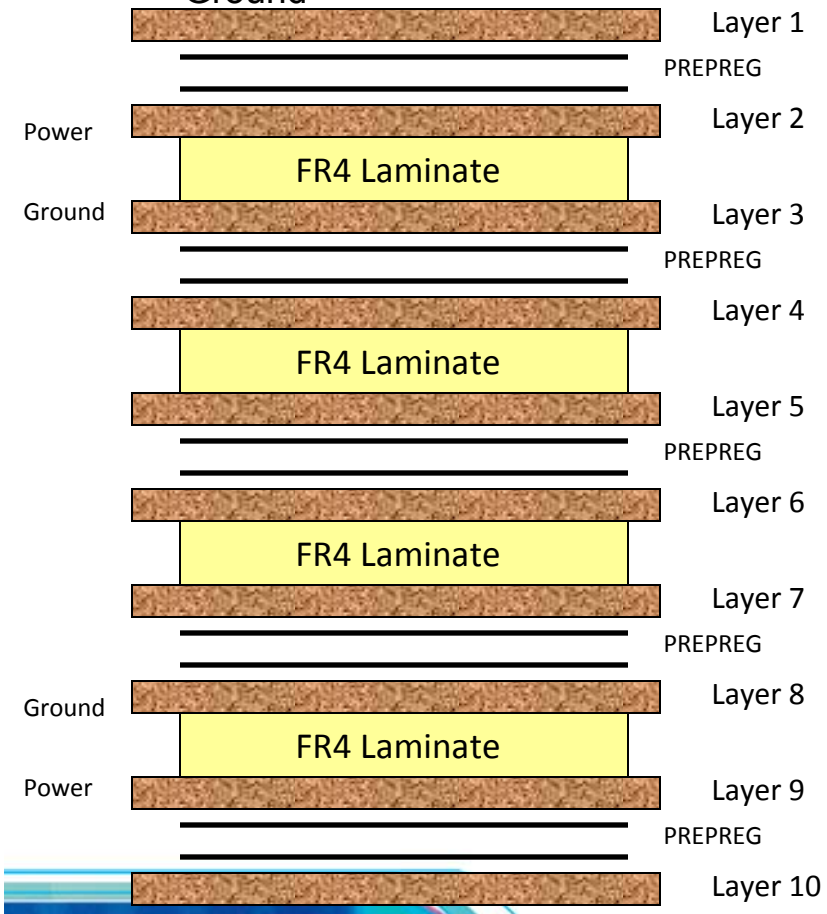
Dielectric layer
8 to 24 um

Copper Foil

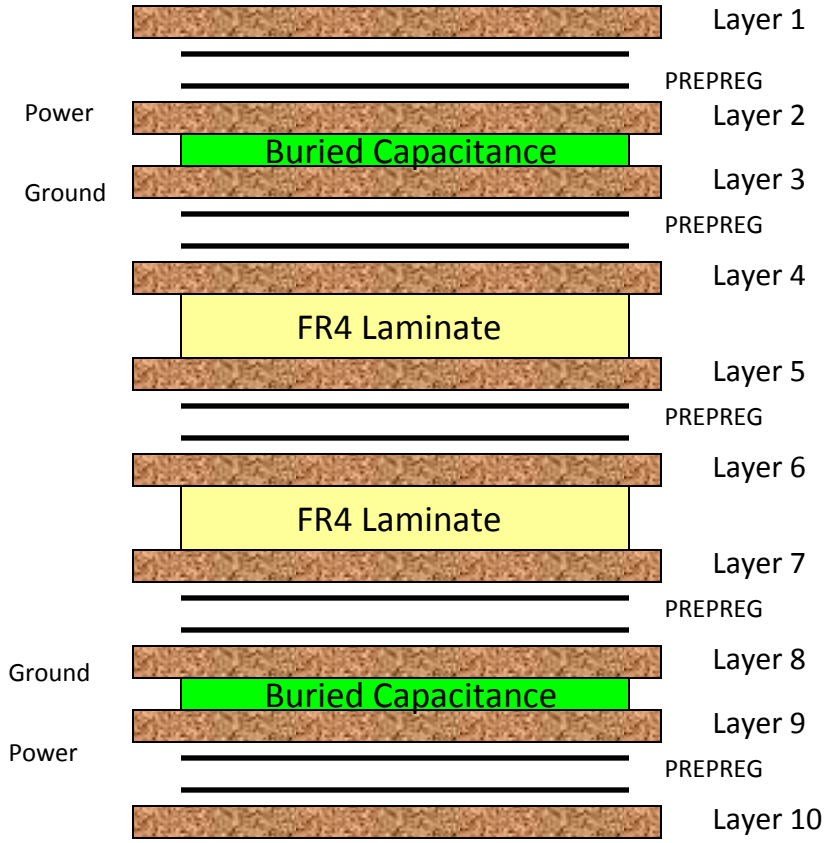
TYPICAL PCB DESIGN AND STACK UP

10 LAYER PCB STACK-UP
With **2** Power-Ground layers at **L2/L3** and **L8/L9**
(using 24 micron laminate in the Power-Ground allows for buried capacitance)

With 50 micron FR4 Power-Ground

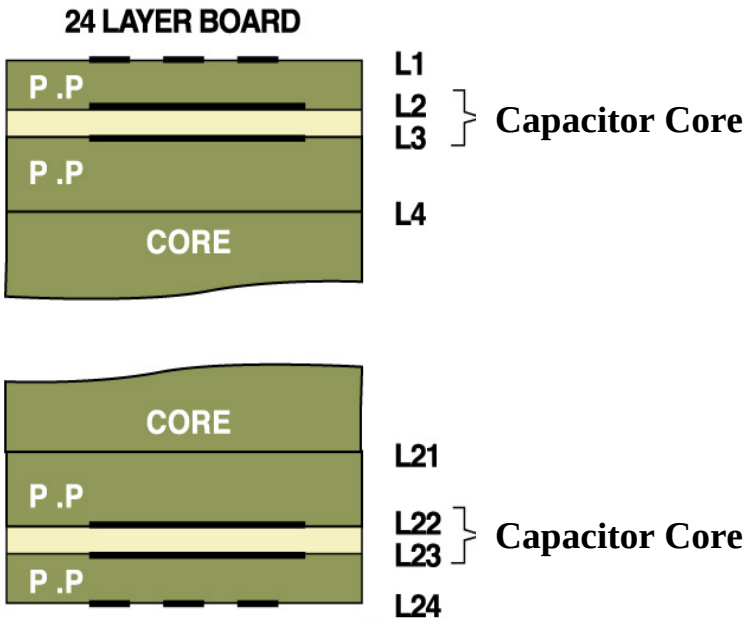


With 24 micron Power-Ground



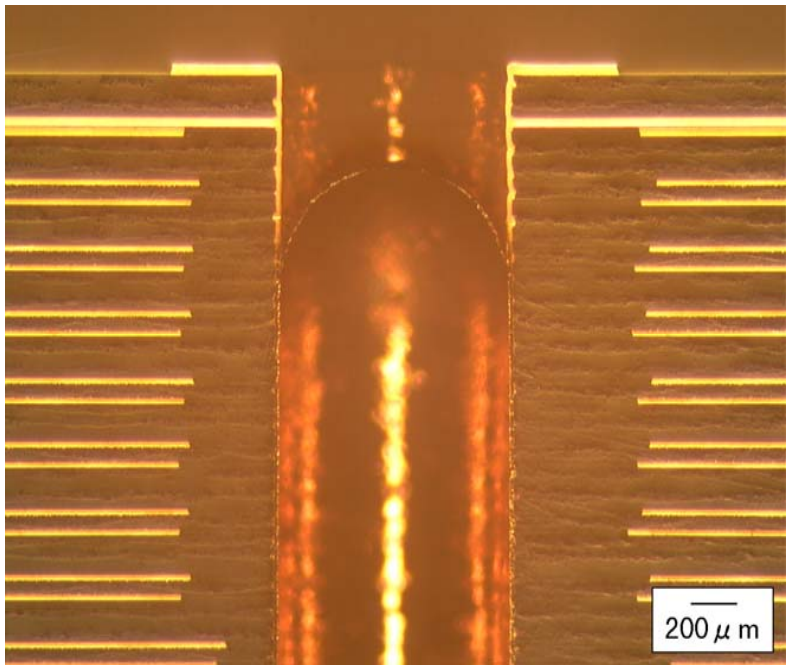
PCB Example

24 Layer Board



Sun Microsystems PCB

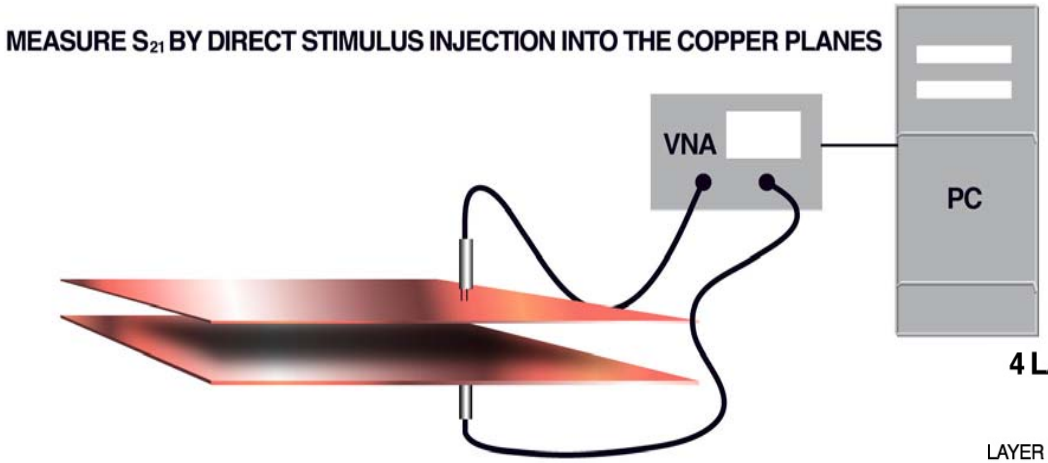
High Volume Server

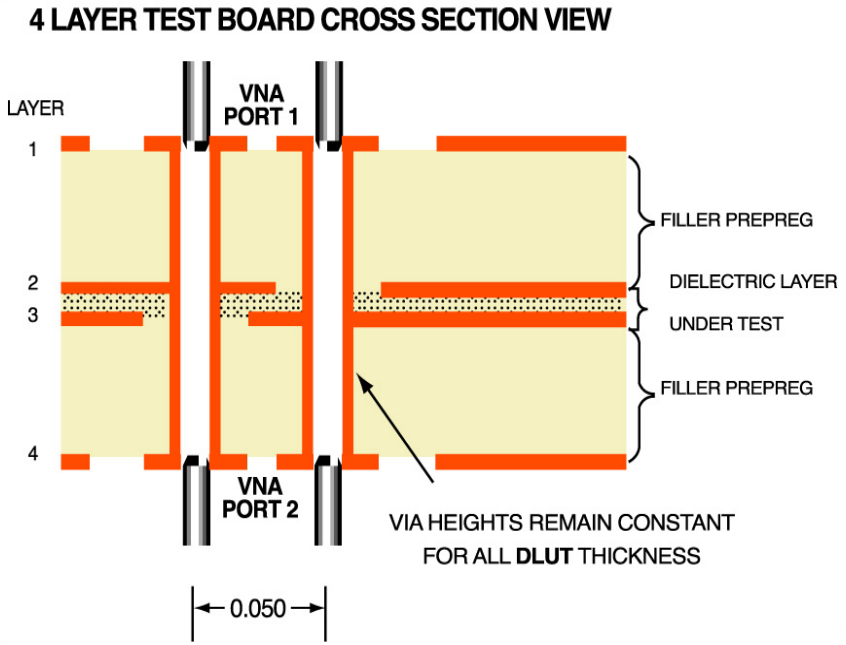


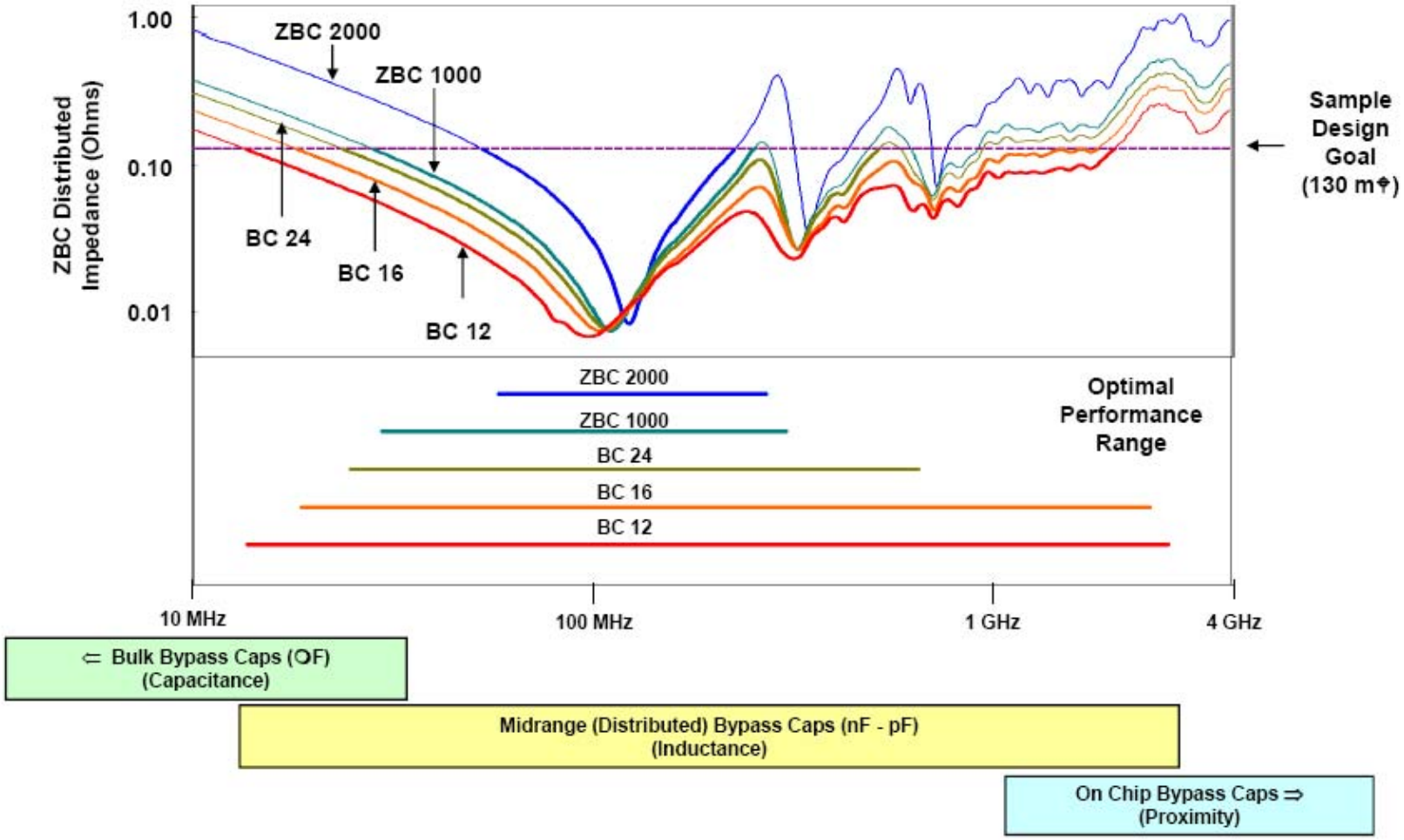
12 µm

IMPROVED IMPEDENCE/ INDUCTANCE

PCB Electrical Performance

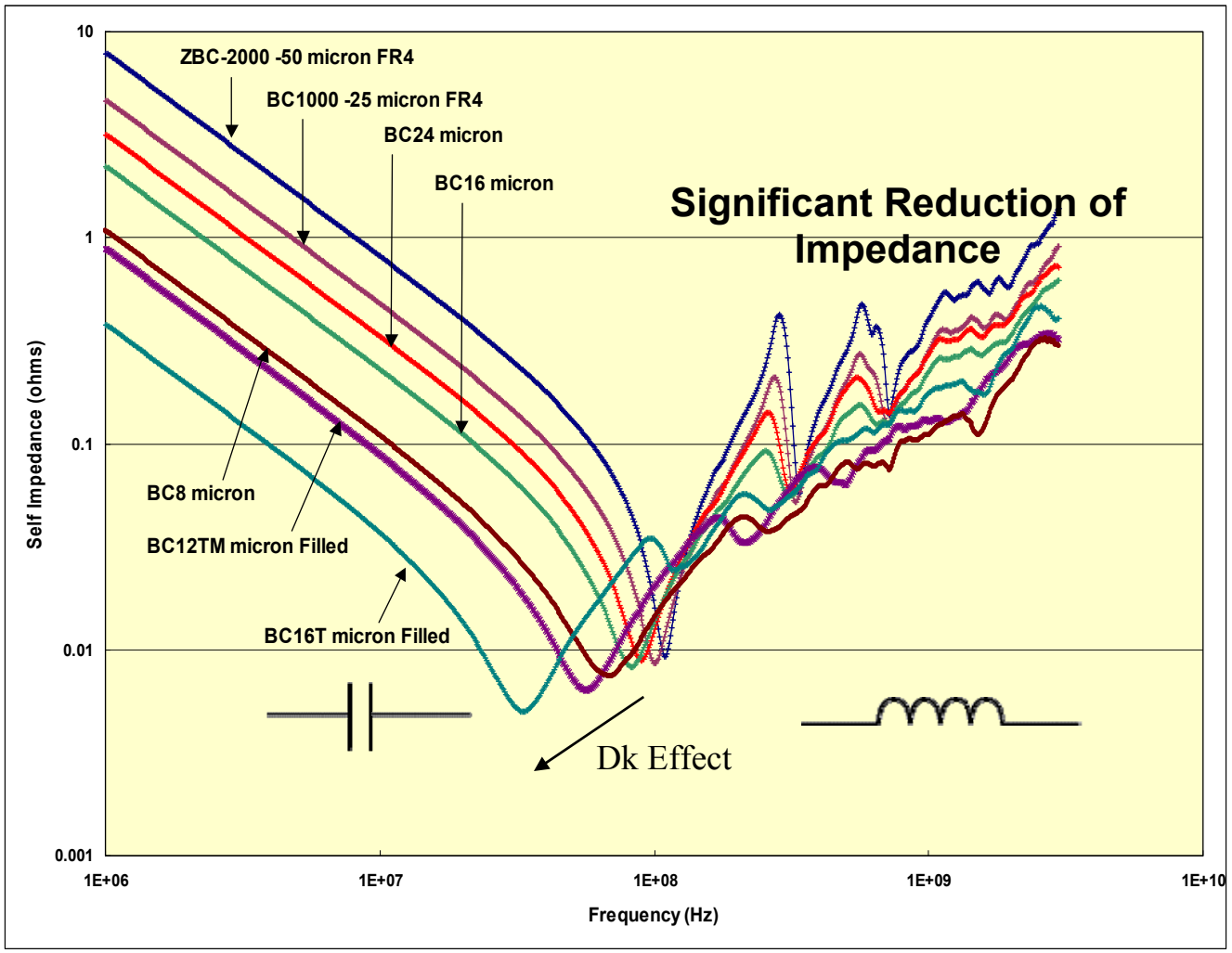






SANMINA-SCI

PCB Electrical Performance

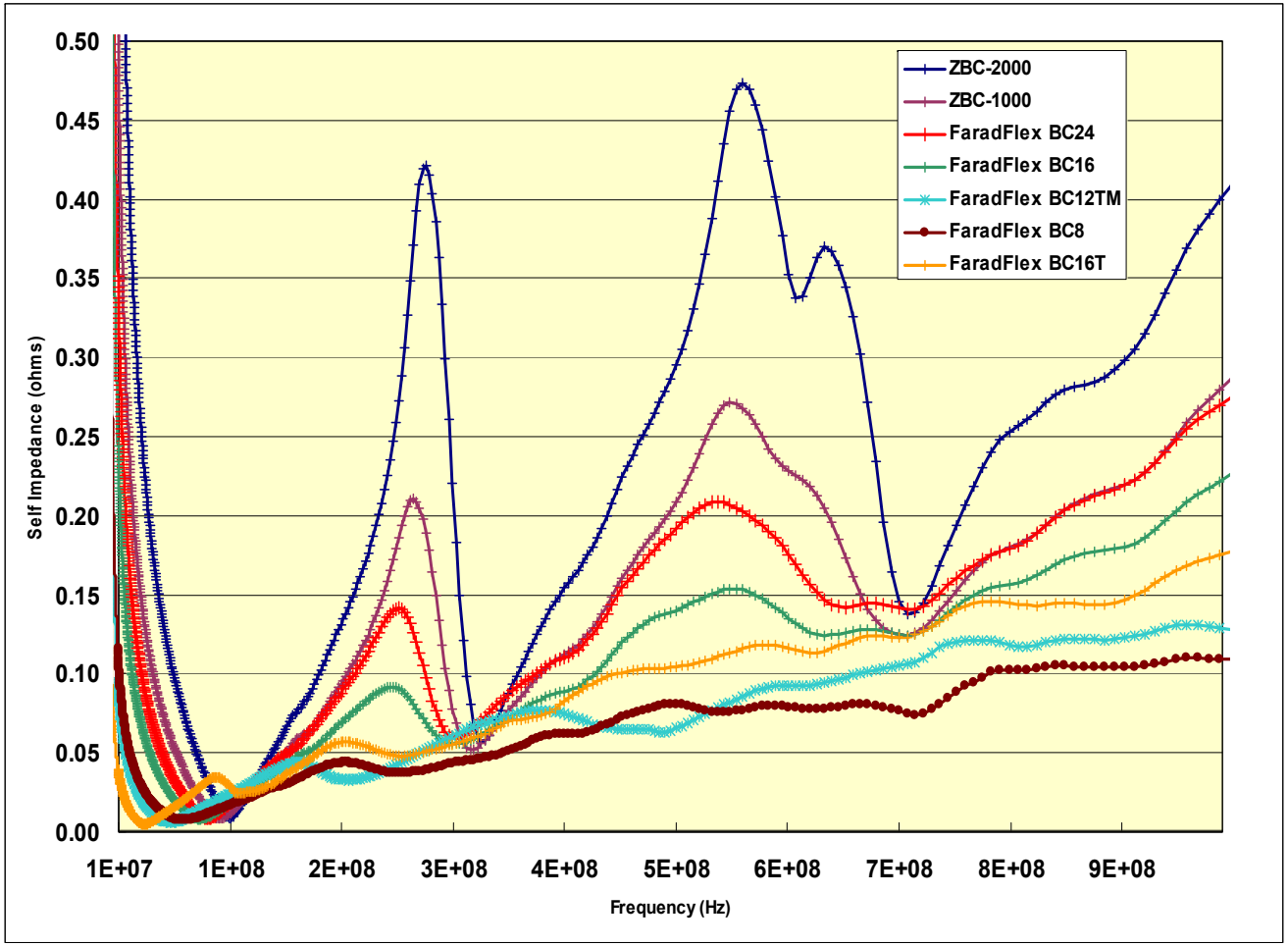


Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

Discrete capacitors of 0.1µF have a resonance frequency of about 15 MHz
Discrete capacitors of 0.01µF have a resonance frequency of about 40 MHz.

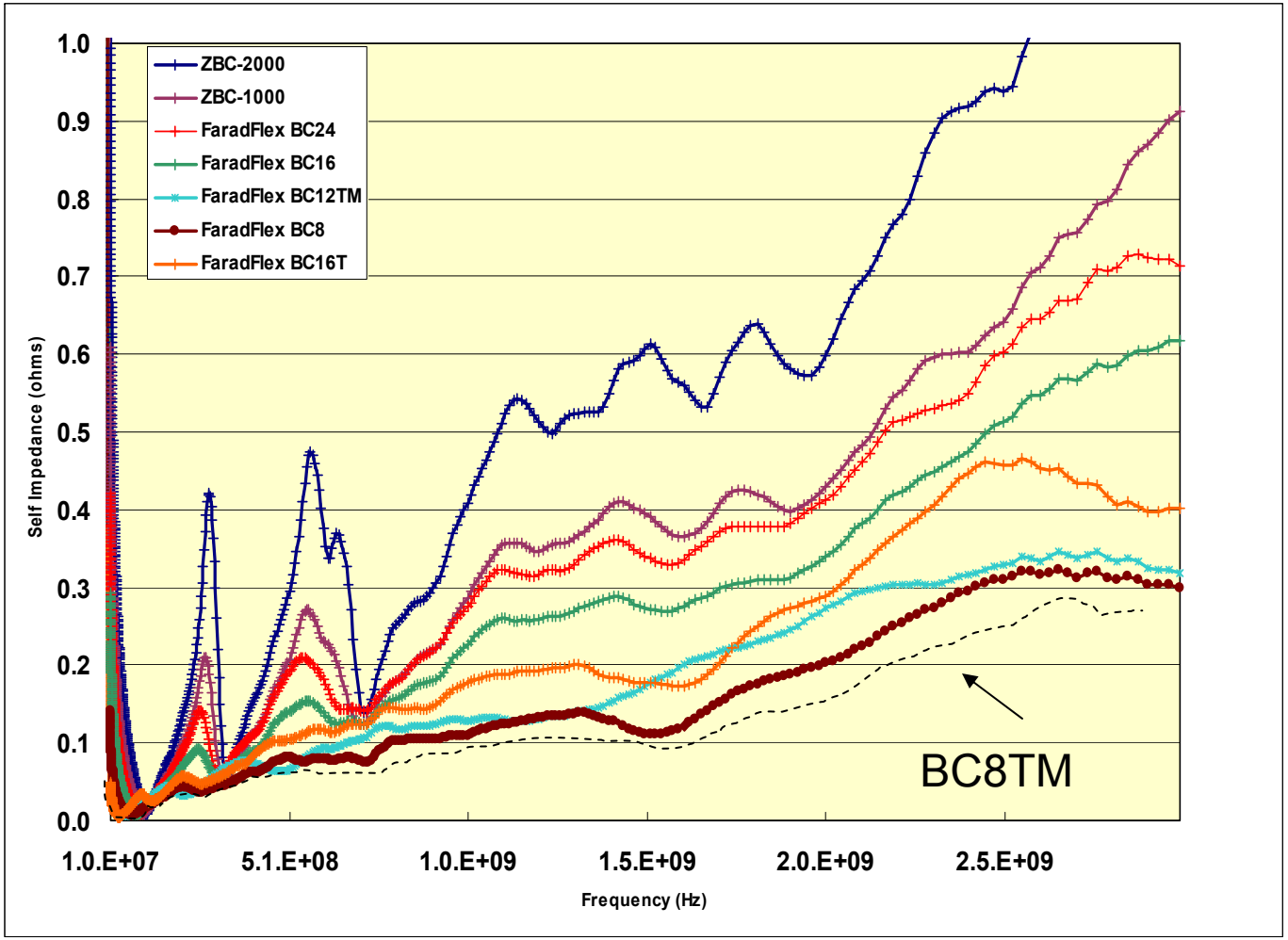
PCB Electrical Performance (Up to 1 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

PCB Electrical Performance (Up to 3 GHz)



Panel Size= 50 in^2
80% Retained Cu

Product	nF
ZBC2000	16
ZBC1000	32
BC24	40
BC16	64
BC12	76
BC8	124
BC12TM	180
BC16T	440

RELIABILITY

Reliability Tests

Description	
6x Through Hole Solder Shock	**PASS**
6x Blind Via Solder Shock	**PASS**
Dielectric Thickness per Cross Section within +/-10%	**PASS**
T-288(>20min)	**PASS**
IST Testing (500 cycles)	**PASS**
Core Level Hi-Pot Testing 100Cores(100V/sec; 500Vmax)	**PASS**
Finished Circuit Level Hi-Pot 50 circuits (100V/sec; 500Vmax)	**PASS**

Courtesy of Sanmina-SCI

PCB FABRICATION/ PROCESSING

Processing guideline

Pre-clean
- Standard process

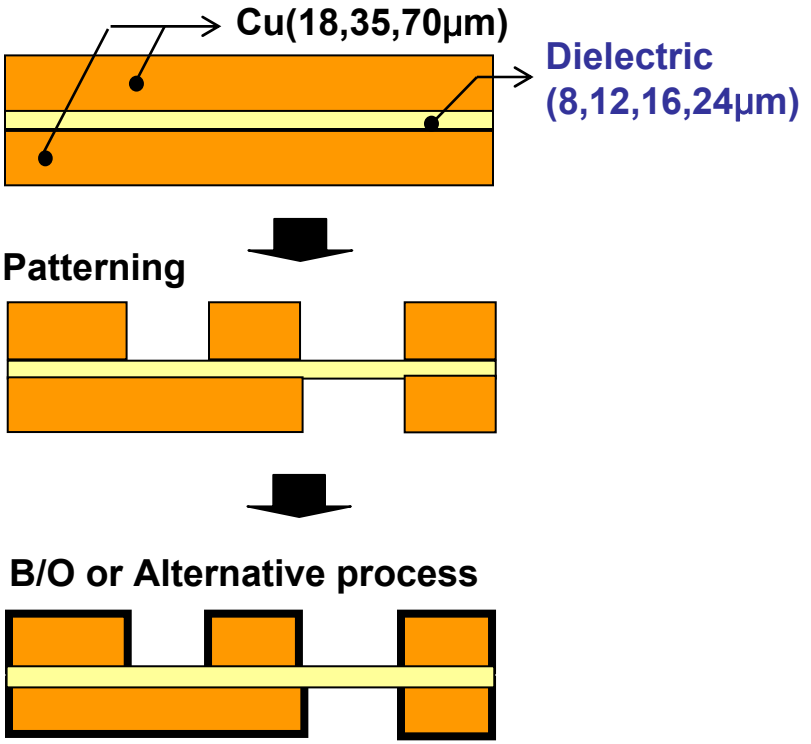
Dry Film lamination
- Standard process

Expose Image
- Standard process

Important

Pattern etching
- Thin core compatible line recommended
  Ex) Thin core Schmid etching line
- Use leader board if not confident
- Careful Handling required

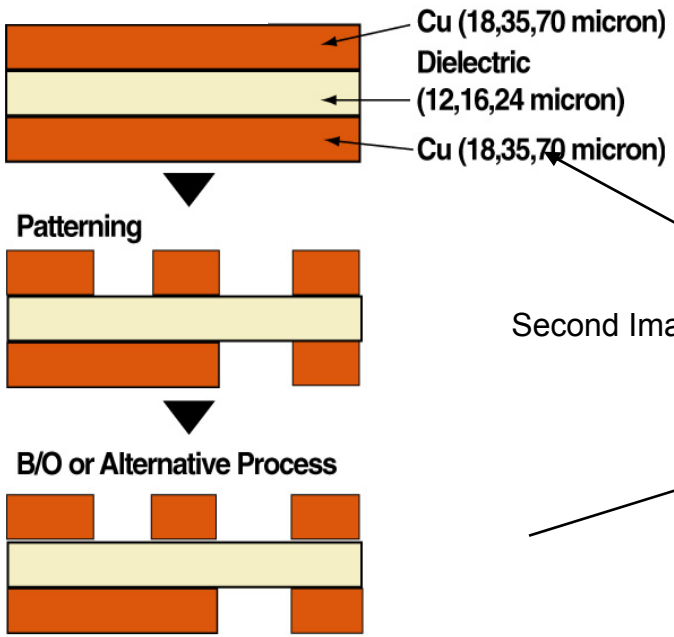
Black oxidizing or alternative oxides
- Thin core compatible line recommended
- Use leader board if not confident
- Horizontal line preferred
- Careful Handling required



Comparison of Inner layer Processes

8 µm to 24 µm Film based laminate and partially filled

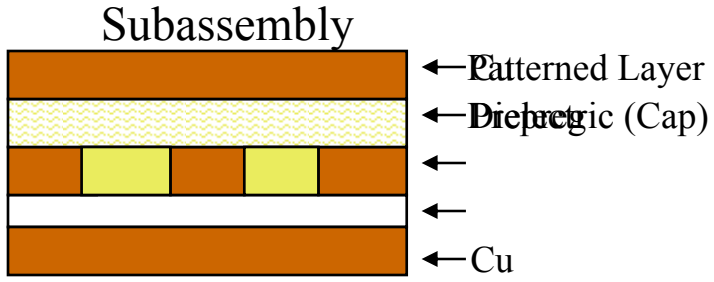
1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative



16µm (Highly Filled with High Dk Particles)

1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative

Second Imaging Step



Second Lamination/ Laminate Subassembly

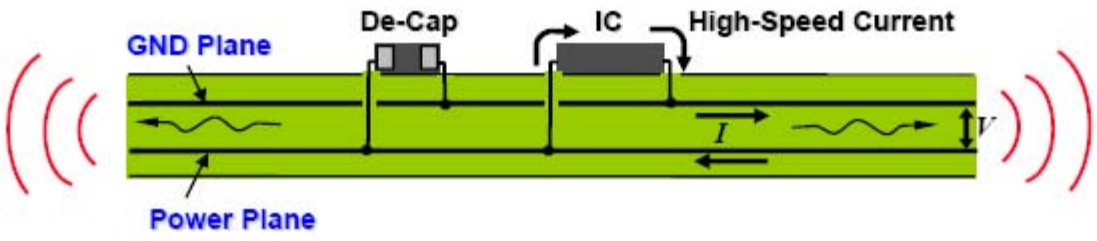
POWER DISTRIBUTIONS NETWORK SIMULATIONS

RESONANCE/ NOISE/ EMI

Why Buried Capacitance Designs Using Buried Capacitance <u>Can</u> Reduce EMI

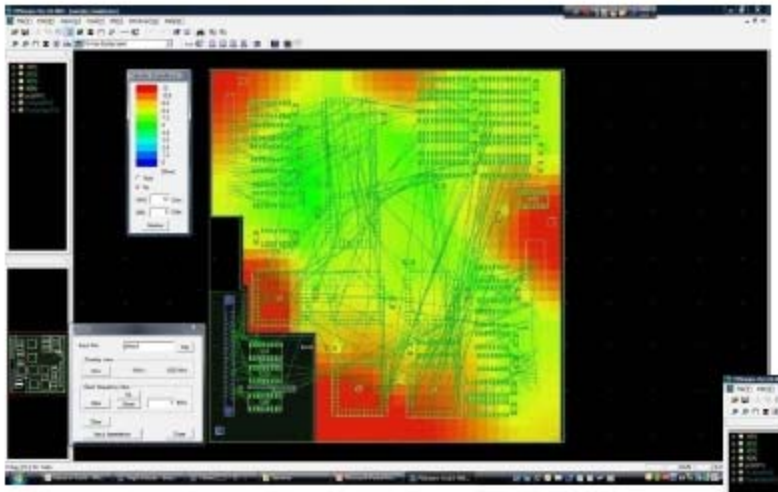
1. *Can minimize loop area* $(E_r = 1.316 \times 10^{-14} \times I \times f^2 \times S / r)$
2. *Can minimize power bus noise*
3. *Can minimize resonance*
4. *Can minimize propagation to the edge (Related to Transfer Impedance (S21))*

E : Electric Field Strength
I : Normal Mode Current
f : Frequency
S : Loop Area
r : Distance



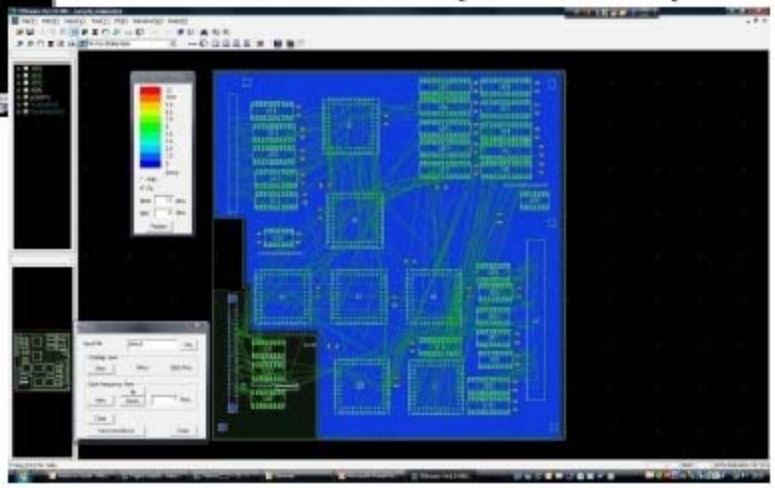
Transfer Impedance Simulation (Z_{21}) with PIStream

Transfer Impedance Analysis 2 mil FR4 VERSUS 1 mil Laminate



FR-4 (0.6 mm Core)

24 micron polymer film type laminate

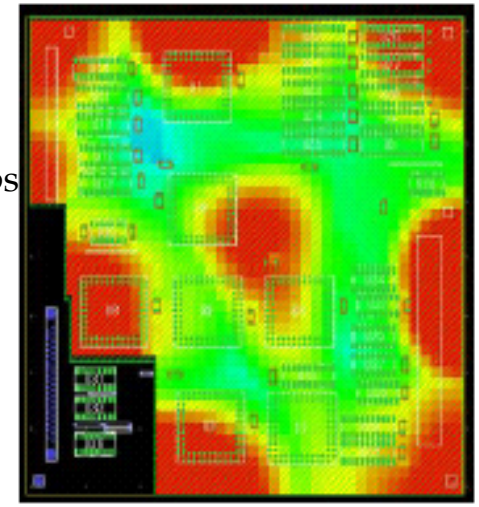


If the transfer impedance is too high…

1. *Increase power bus noise*
2. *Digital circuit noise would affect RF or Analog circuit.*
3. *Increase EMI (related to S21)*

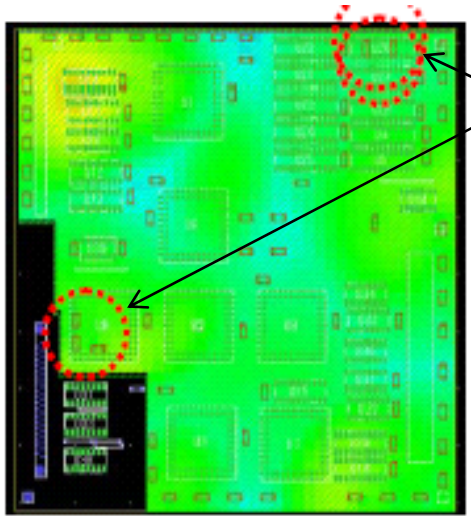
Resonance Distribution

35- 0.1µF caps
for power
supply



0dB

26dB

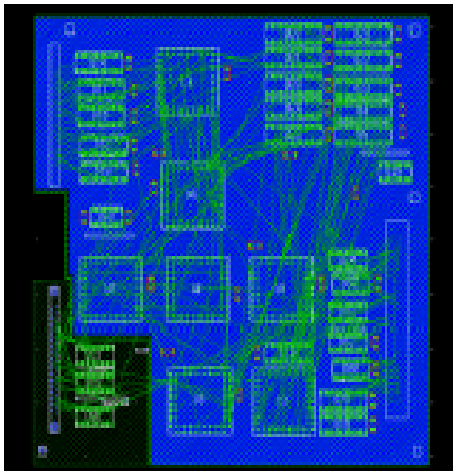


Can not place caps!

35- 0.1µF caps
for power supply
+44-0.1 µF caps
for resonances

0.4mm (16 mil P/G)

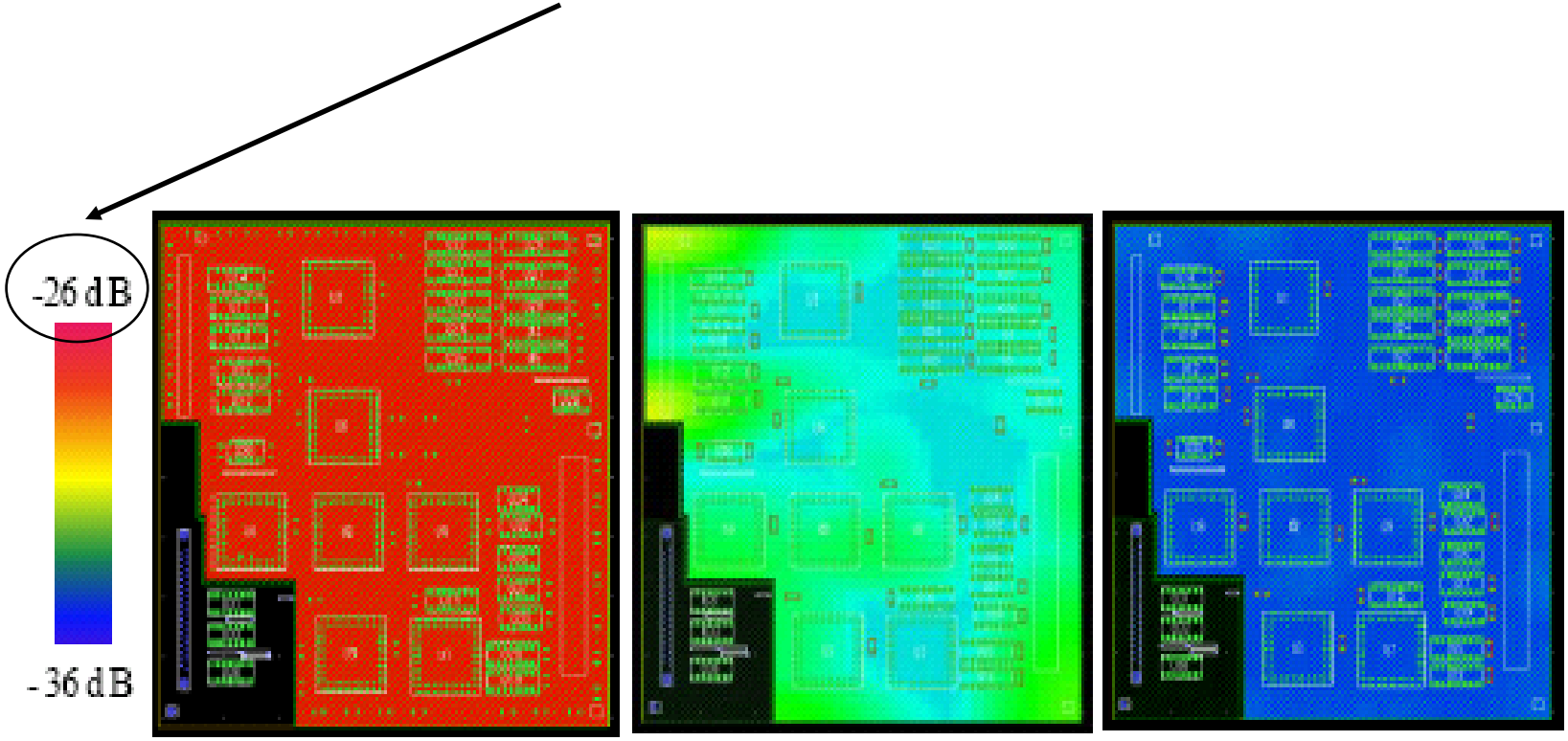
24 µm P/G
Dk 4.4
No additional
caps



0dB

26dB

Resonance Distribution- Lower Noise Threshold



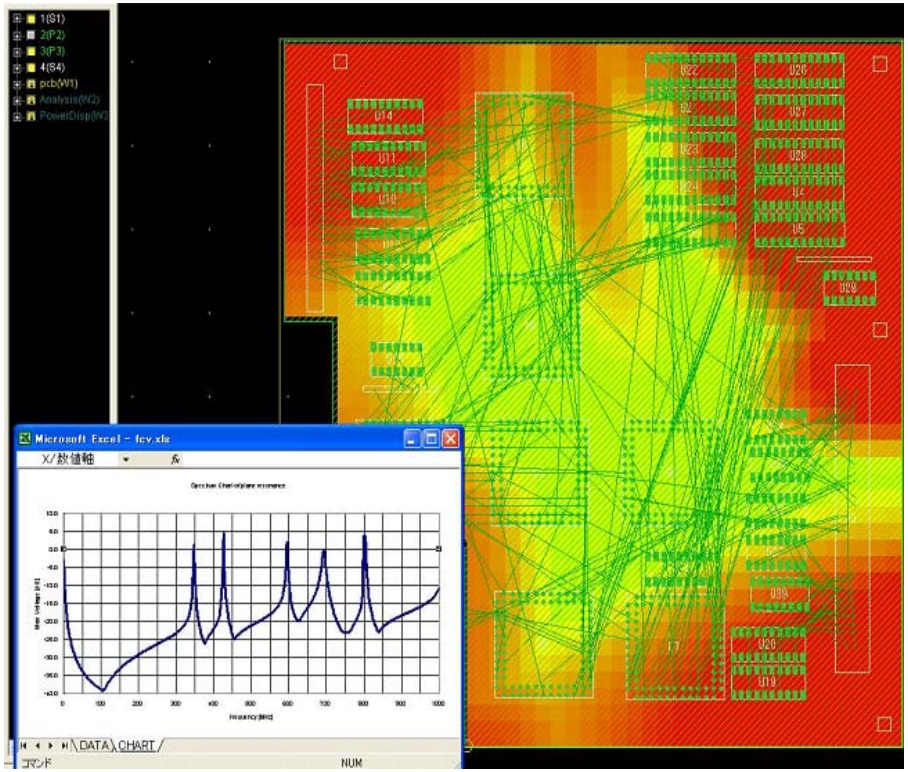
400 µm (16 mil P/G)
79 caps

24 µm P/G
Dk 4.4
35 caps

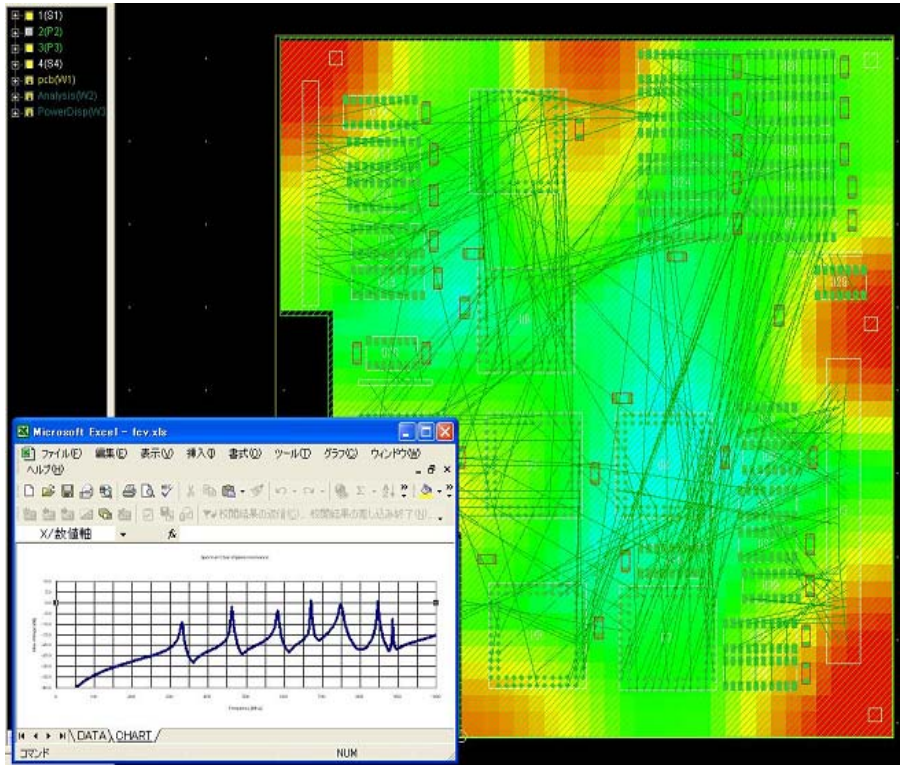
12 µm P/G
Dk 10
35 caps

Test Board –Simulation #2

Standard core(400umFR-4) with no caps

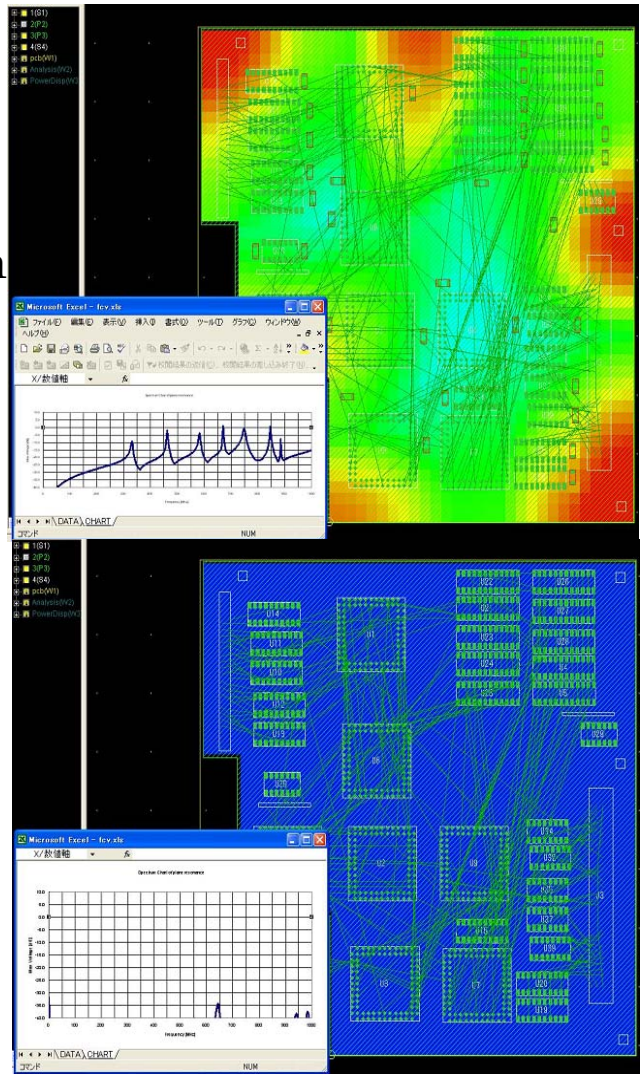


Standard core(400umFR-4) with caps

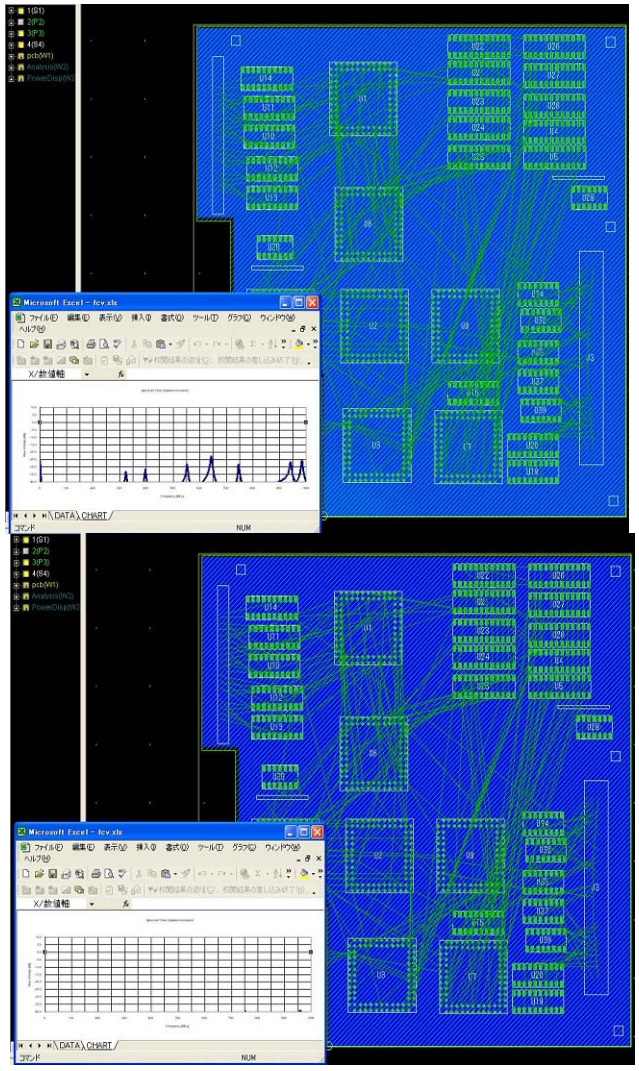


Test Board- Simulation #2

P/G Plane
FR-4 400um
With Caps



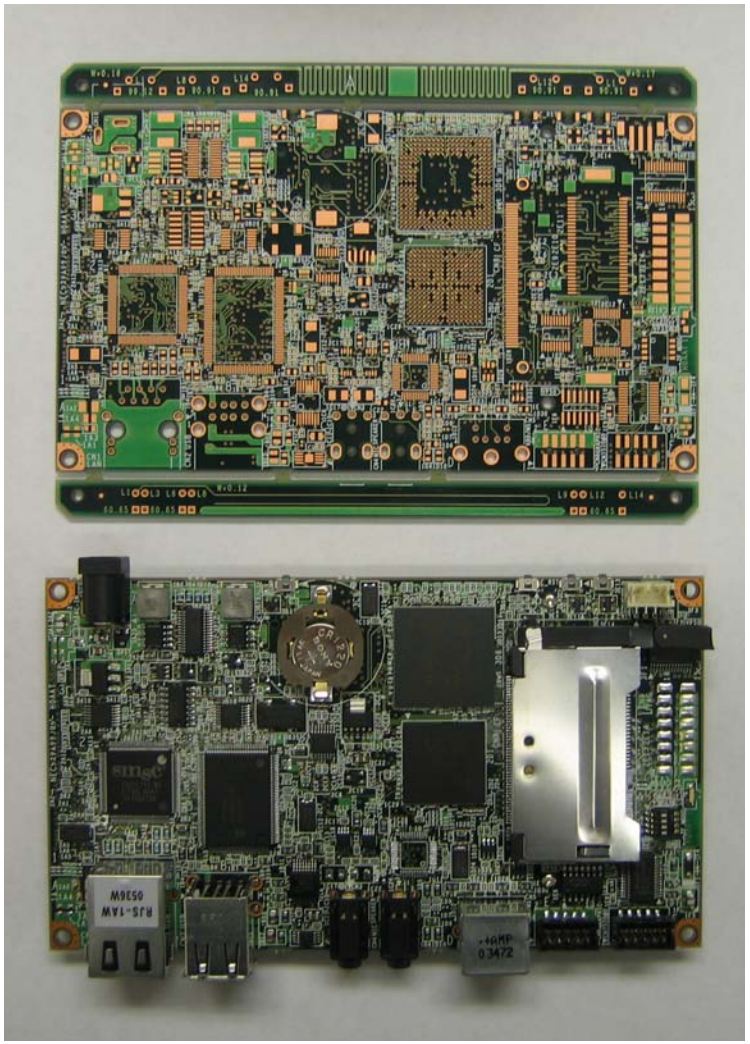
P/G Plane
1 mil



P/G Plane
½ mil

P/G Plane
16 micron
Dk 30

CASE STUDY 1



(by courtesy of NEC System Technology, Inc. & NEC Information Technology, Inc.)

PCB

Construction of Reference Board

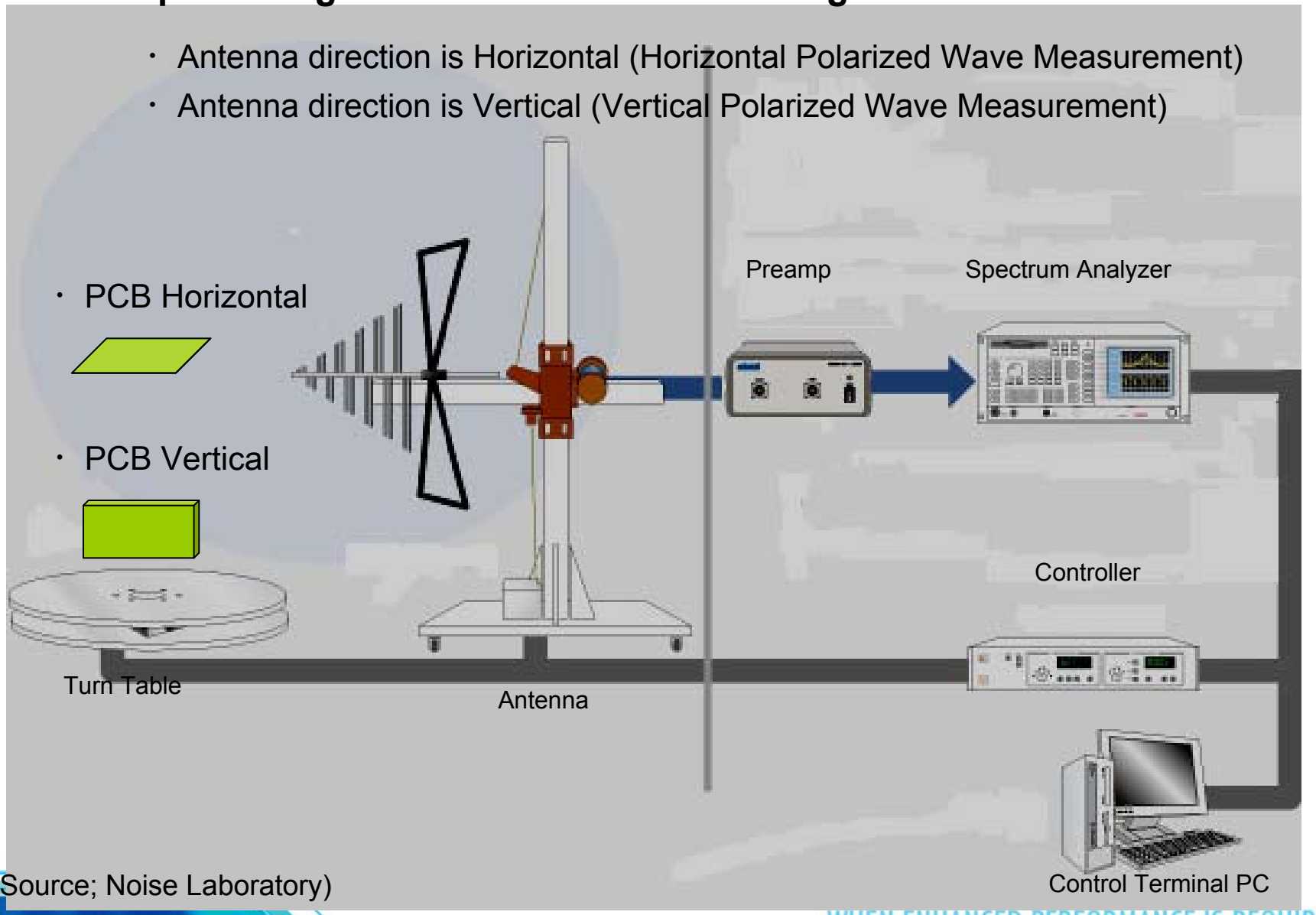
No.	Layer		Thickness[mm]	
		resist		
1	Signal		0.057	Include Plating
		prepreg	0.11	
2	Gnd(Plane)		0.032	
		core	0.15	
3	Signal		0.032	
		prepreg	0.17	
4	Gnd(Plane)		0.032	
		prepreg	0.14	
5	Vdd(Plane)		0.032	
		core	0.15	
6	Signal		0.032	
		prepreg	0.14	
7	Gnd(Plane)		0.032	
		core	0.15	
8	Signal		0.032	
		prepreg	0.14	
9	Signal		0.032	
		core	0.15	
10	Vdd(Plane)		0.032	
		prepreg	0.14	
11	Gnd(Plane)		0.032	
		prepreg	0.17	
12	Signal		0.032	
		core	0.15	
13	Gnd(Plane)		0.032	
		prepreg	0.11	
14	Signal		0.057	Include Plating
		resist		
Total	8		2.36	±0.2mm

Ultrathin Core ½ mil high Dk and 1 mil

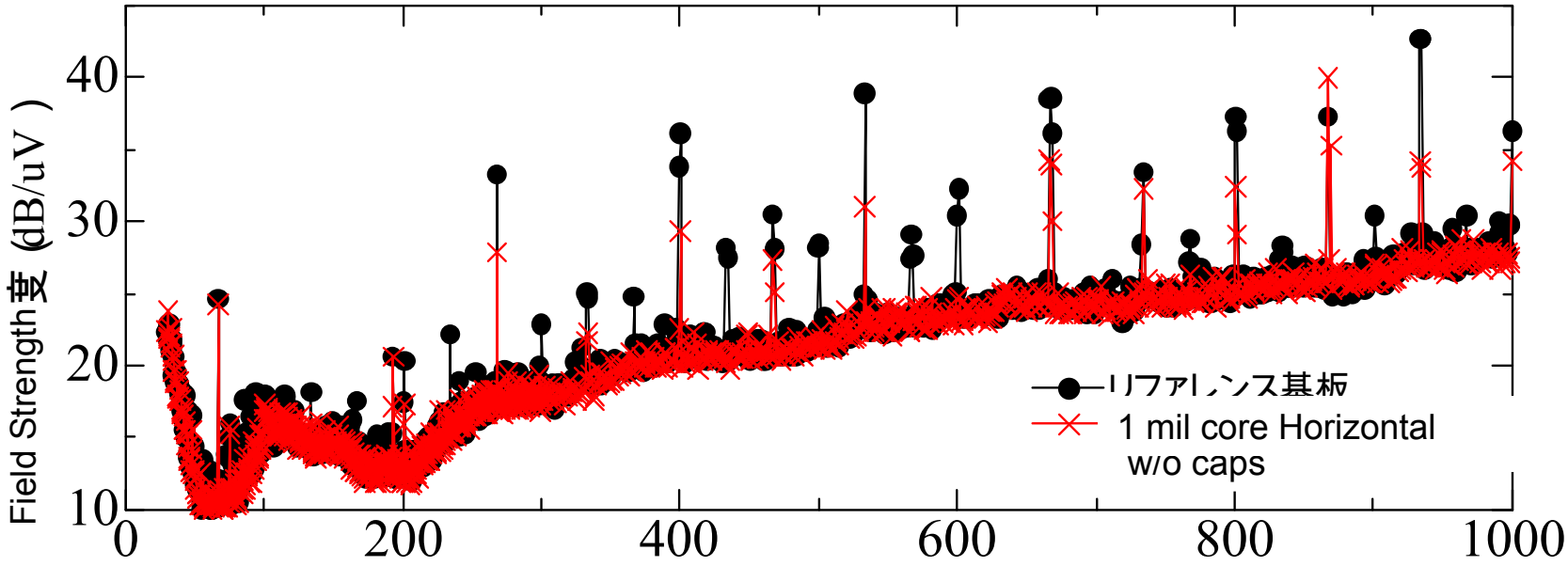
Ultrathin Core ½ mil high Dk and 1 mil

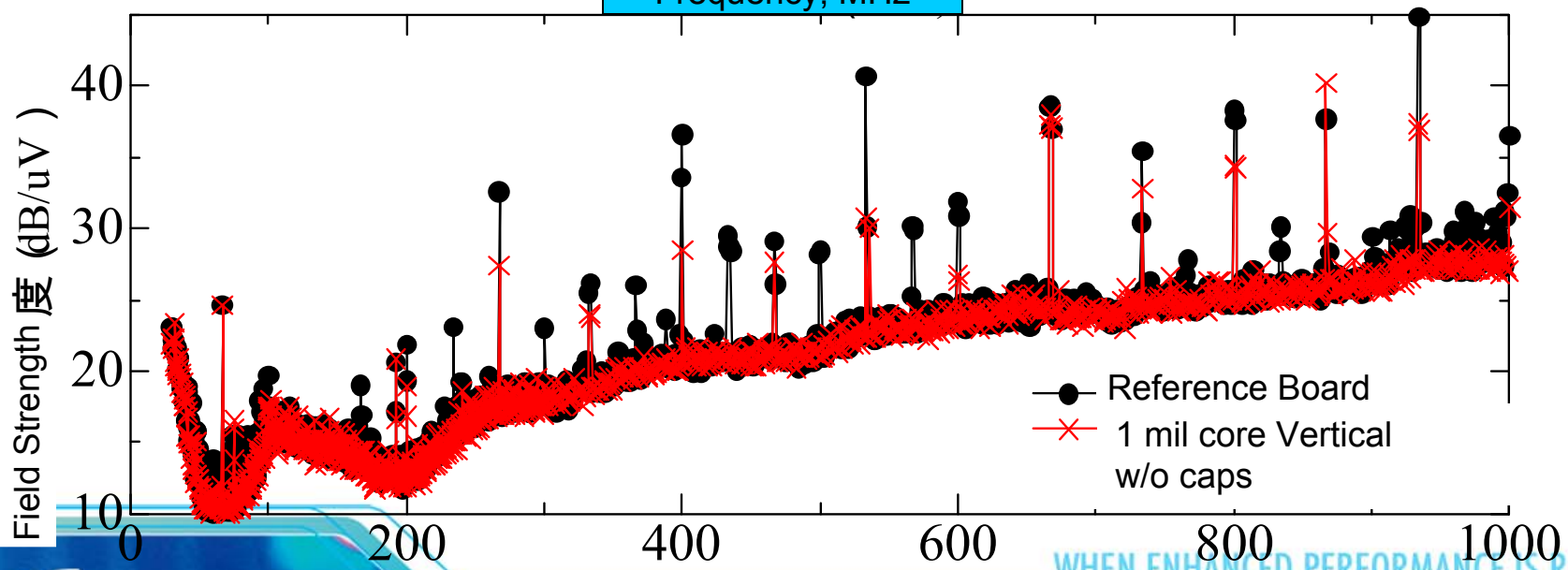
A Conception Diagram of The Distant Place Magnetic Field Measurement

- Antenna direction is Horizontal (Horizontal Polarized Wave Measurement)
- Antenna direction is Vertical (Vertical Polarized Wave Measurement)

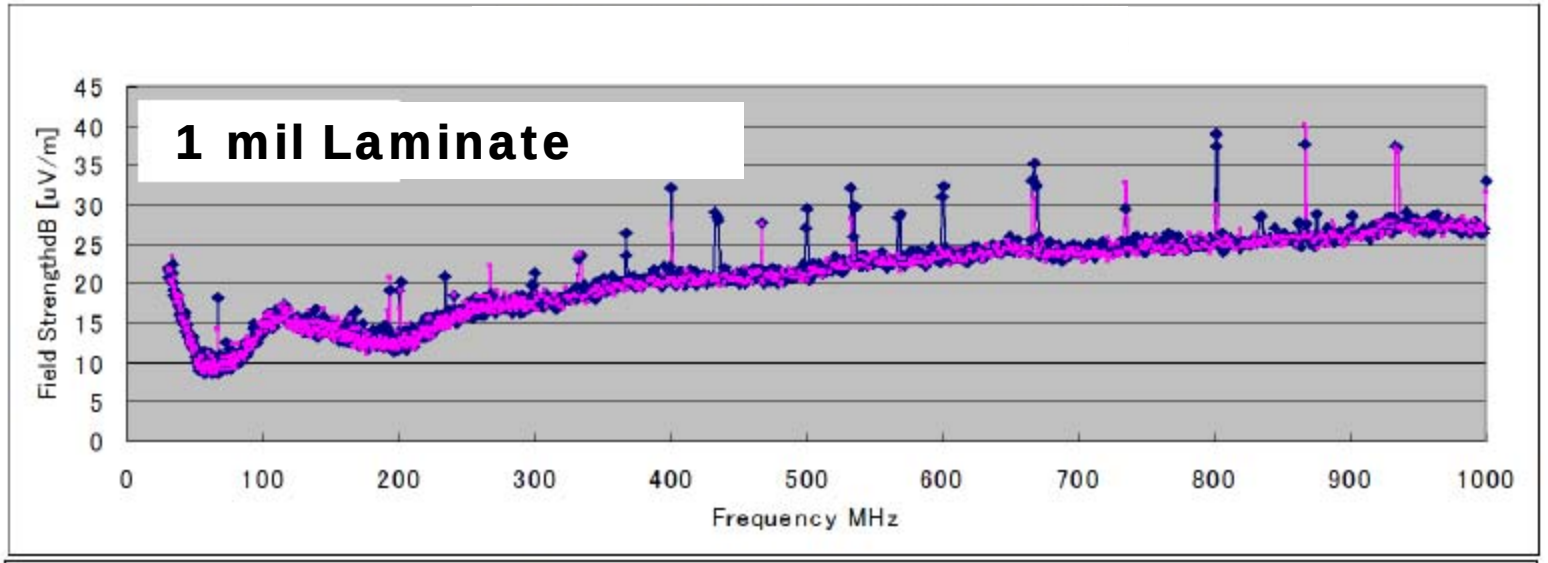


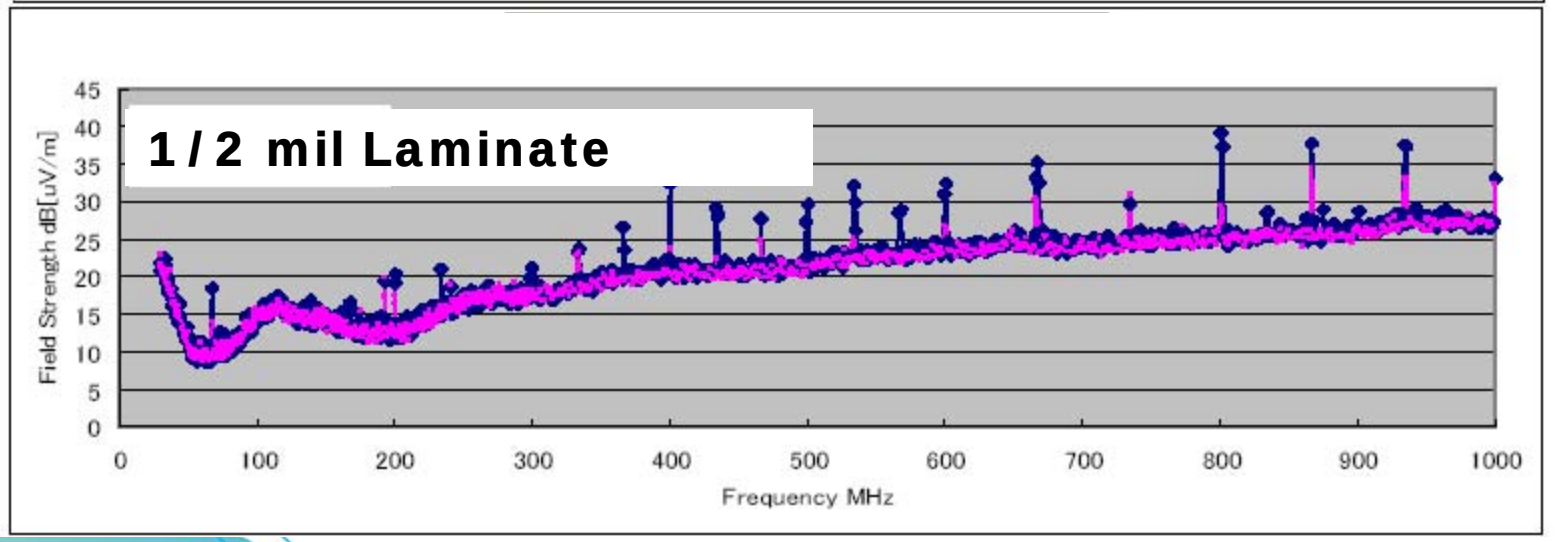
(Source; Noise Laboratory)


Field Strength度 (dB/uV)
40
30
20
10
0
200
400
600
800
1000
リファレンス基板
1 mil core Horizontal
w/o caps
Frequency, MHz

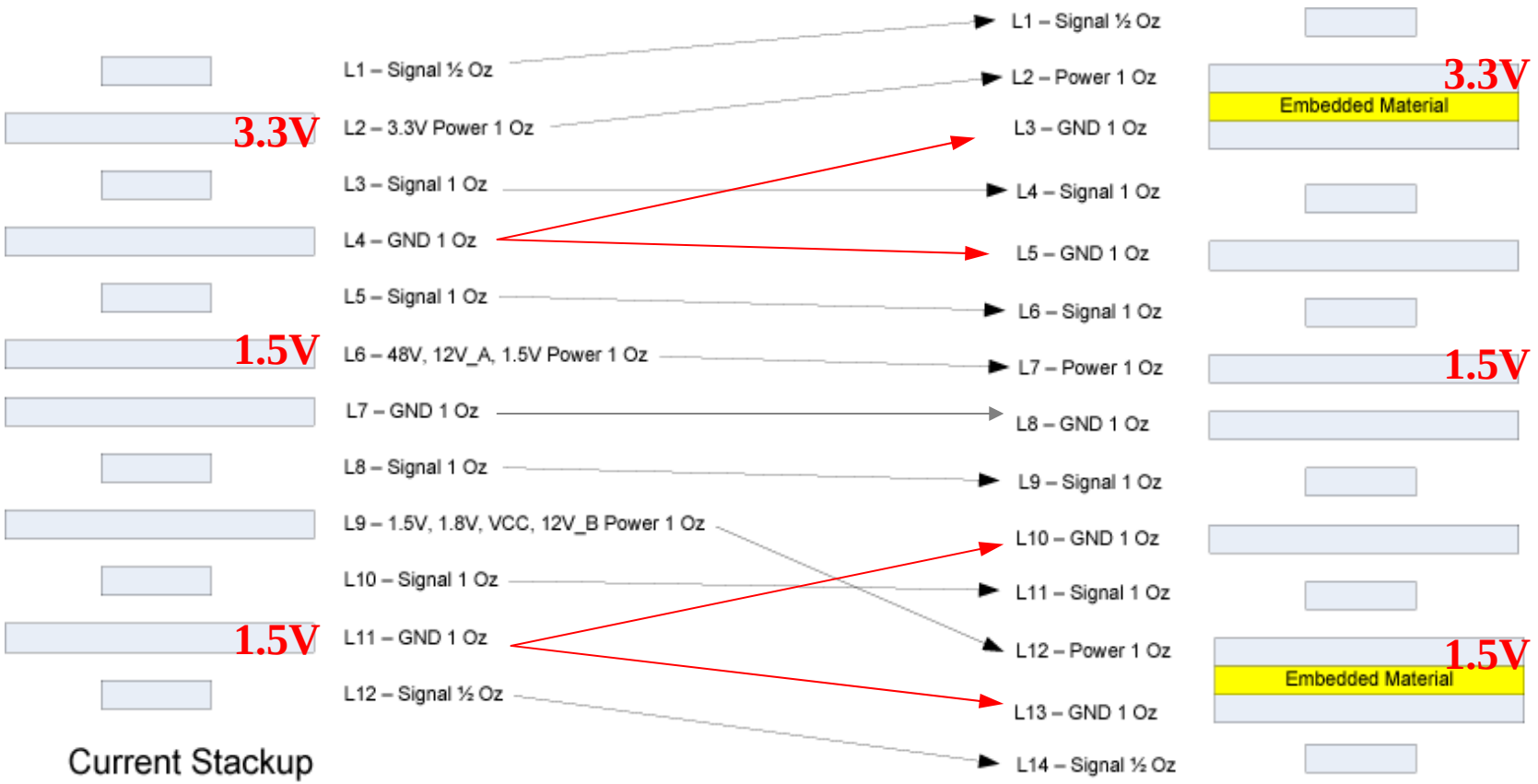

Field Strength 度 (dB/uV)
40
30
20
10
0
200
400
600
800
1000
Reference Board
1 mil core Vertical
w/o caps
Frequency, MHz

Comparison between reference board with Caps and BC without Caps





CASE STUDY 2



Current Stackup

Total Copper:
Power – 3oz
GND – 3 oz

781 0.1µF decoupling capacitors

Emb Capacitance Stackup

Total Copper:
Power – 3oz
GND – 5 oz

Capacitance Measurements

(courtesy of Univ. of Missouri at Rolla)

Plane Pair	FR-4 (nF)	24 µm (nF)	12 µm (nF)	12 µm DK10 (nF)
1.5V/GND	76.1 (75.8)	179.5 (179.0)	286.7 (266)	487 (478)
3.3V/GND	21.2 (21.2)	323.8 (321.3)	551 (541)	1148 (1082)

From LCR Meter

Extracted from VNA

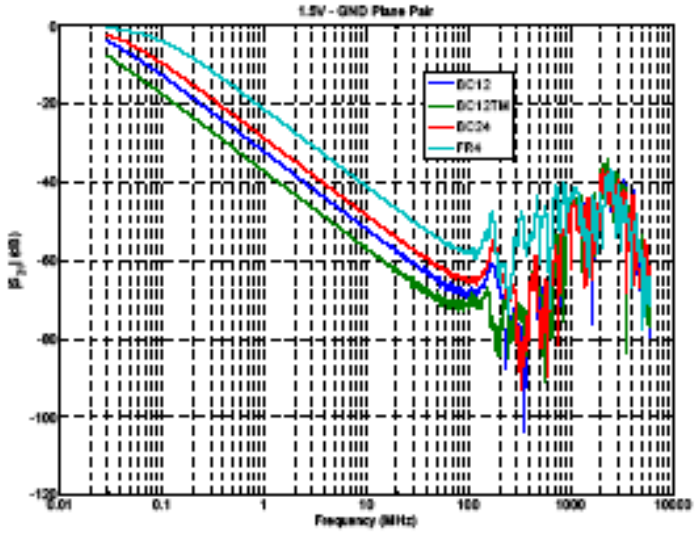
Note: 1.5V plane is split resulting in smaller capacitor area

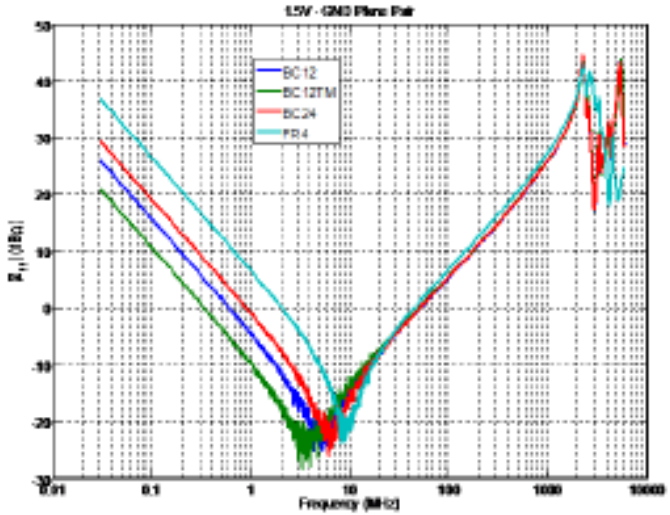
Replaces **78.1 µF** of capacitance on standard board
(781 capacitors of 0.1 µF)

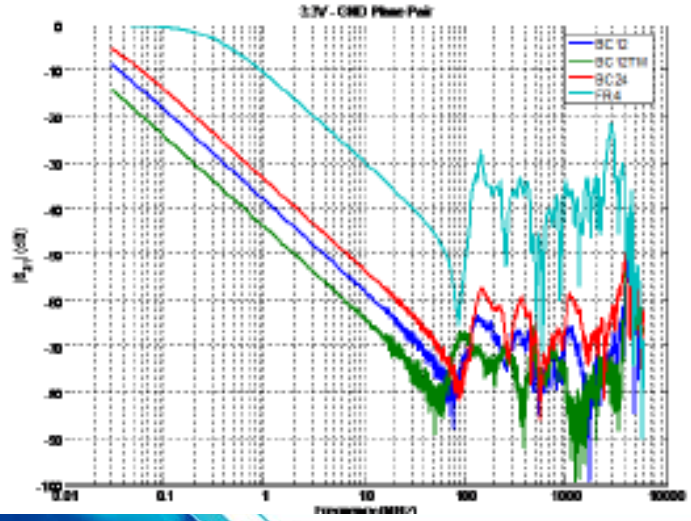
Board Impedance Measurements (S21, Z11)

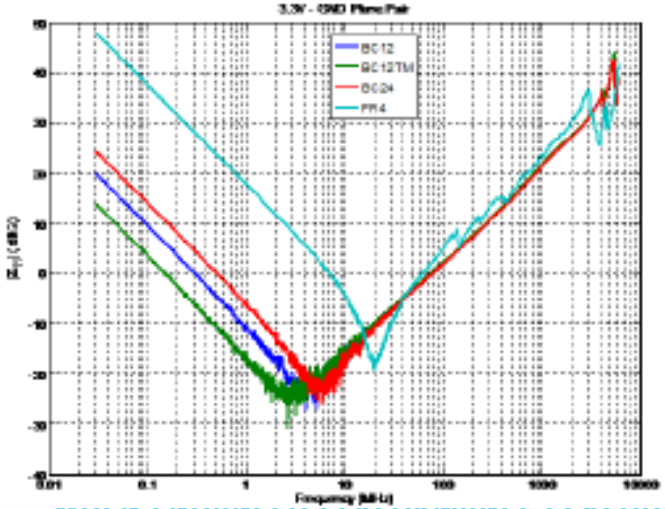
Measurement Equipment : Agilent 8753D (Vector Network Analyzer)

Probe Point : Decoupling Capacitor Pad







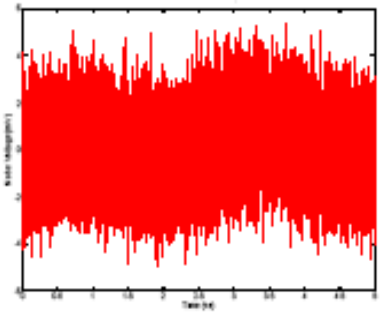


Time Domain Power Bus Noise Measurement

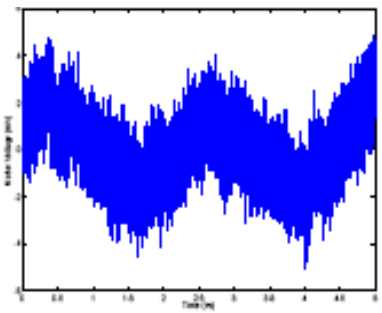
Measurement Equipment : Agilent Infiniium 54855A (Digital Sampling Oscilloscope)

Probe Point : Decoupling Capacitor Pad

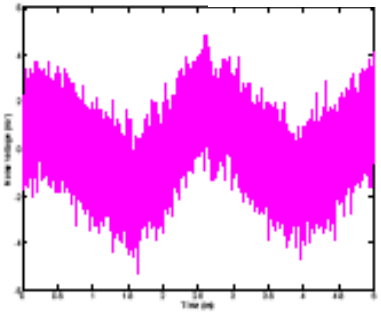
1.5V/GND (FR-4) 50 µm



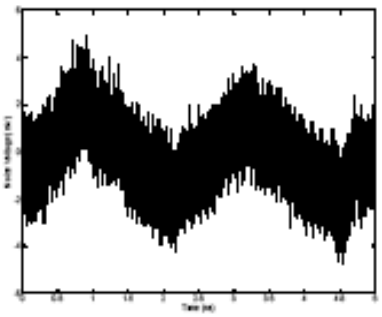
1.5V/GND 24 µm



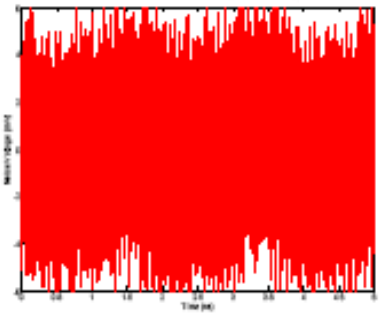
1.5V/GND 12 µm



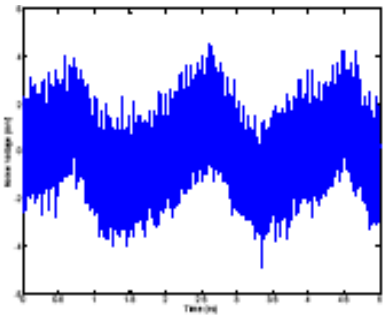
1.5V/GND (12 µm Dk 10



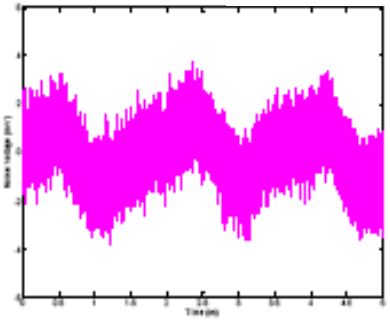
3.3V/GND (FR-4) 50 µm



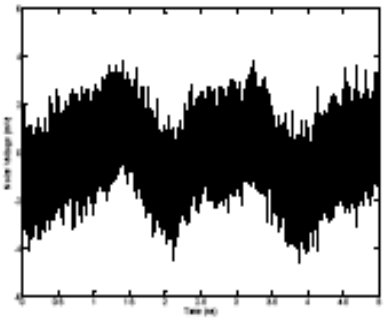
3.3V/GND 24 µm



3.3V/GND 12 µm



3.3V/GND 12 µm Dk 10



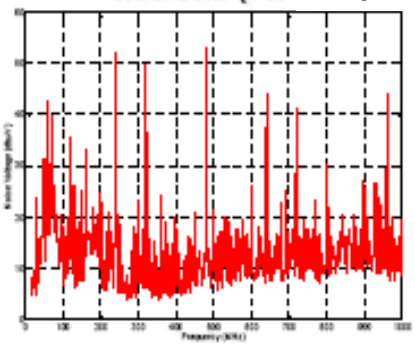
Frequency Domain Power Bus Noise Measurement

Measurement Equipment : Agilent E7404A (Spectrum Analyzer)

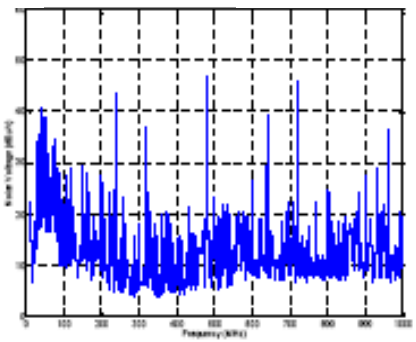
Probe Point : Decoupling Capacitor Pad

Tested to 1 GHz

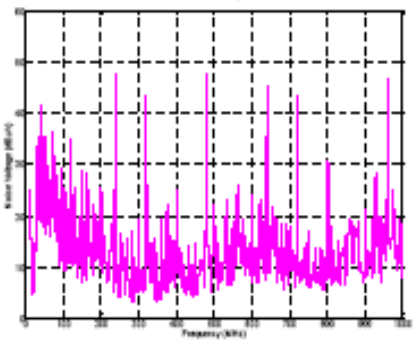
1.5V/GND (FR-4 50 µm



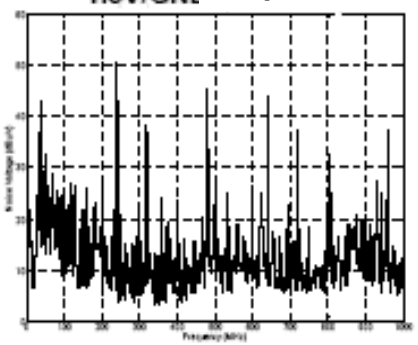
1.5V/GND 24 µm



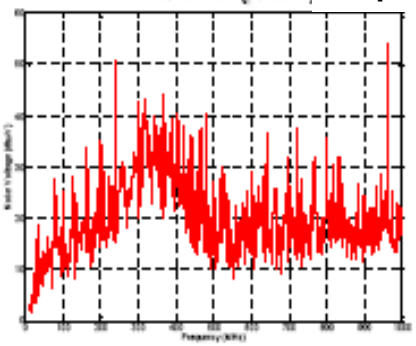
1.5V/GND (12 µm



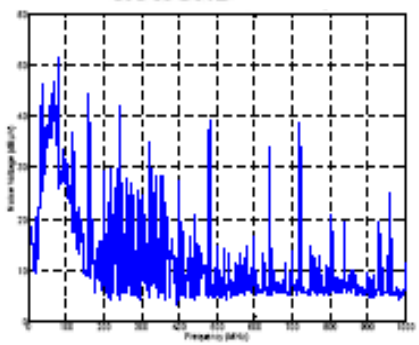
1.5V/GNI 12 µm Dk 10



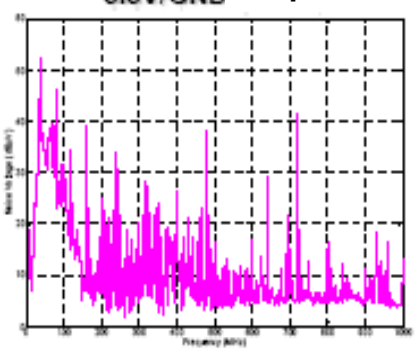
3.3V/GND (FR-4 50 µm



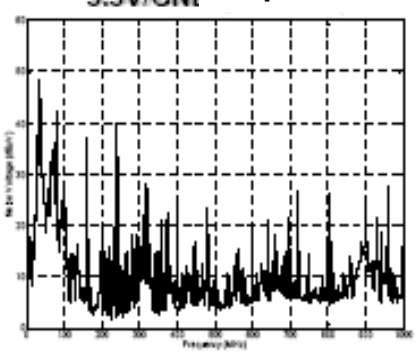
3.3V/GND 24 µm



3.3V/GND 12 µm



3.3V/GNI 12 µm Dk 10

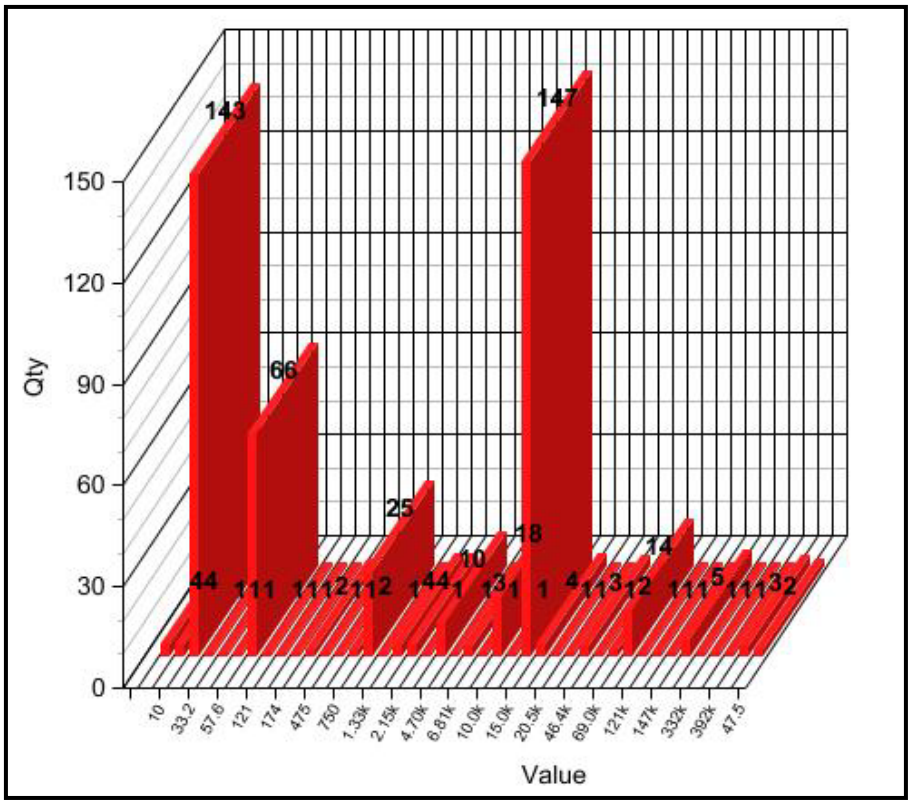


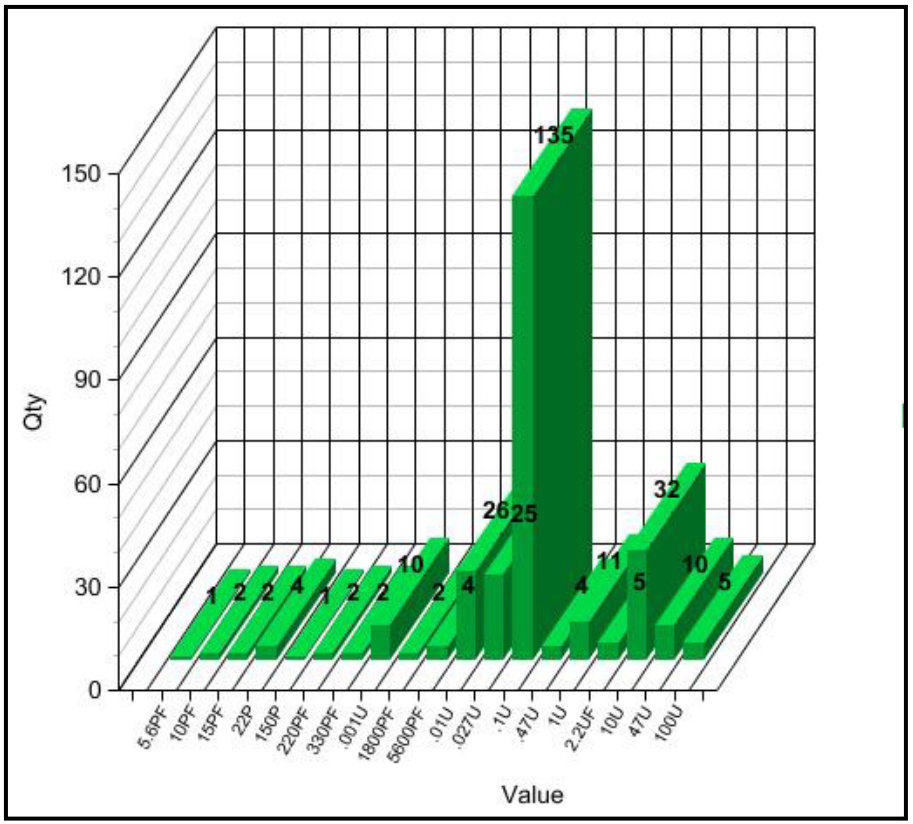
CASE STUDY 3

The Embedded Passives Journey

IPC/APEX – April 2, 2008

Authors:
Bill Devenish – Harris Corp., Mechanical Advanced Development (MAD)
Andrew Palczewski – Harris Corp., PCB Technologist



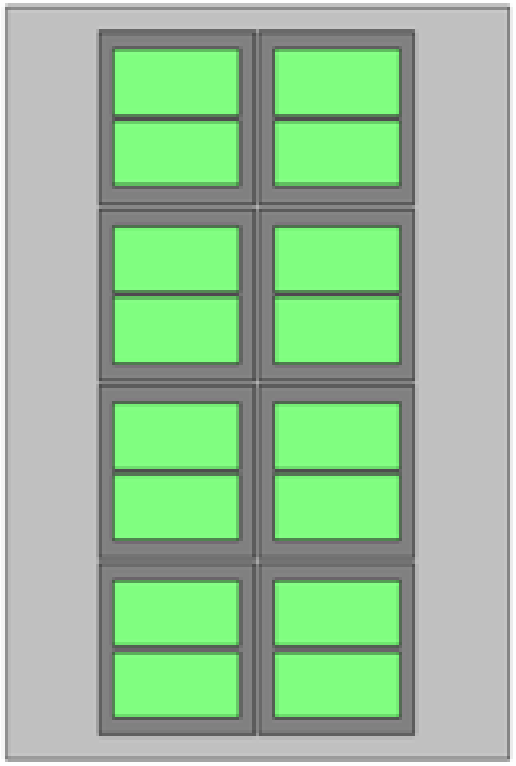


Used with the permission of Harris Corporation

COST SAVINGS		$37.88
- Part Cost		
	CAPACITORS	$1.19
	RESISTORS	$9.77
- Cost of Quality		
	Component	Body
	CAPACITORS	$4.04
		0603
		0402
	RESISTORS	$11.06
		0201
		0402
- Assembly Cost		$11.82
	Total Parts	591

Used with the permission of Harris Corporation

Original Panelization - 16 Up



Size:
Panel: 18.0 x 24.0
Array: 5.6 x 5.524
Part: 4.54 x 2.15

Panel Yield:
8 Arrays of 2 Parts
16 Parts Total
57.3% Material Utilization

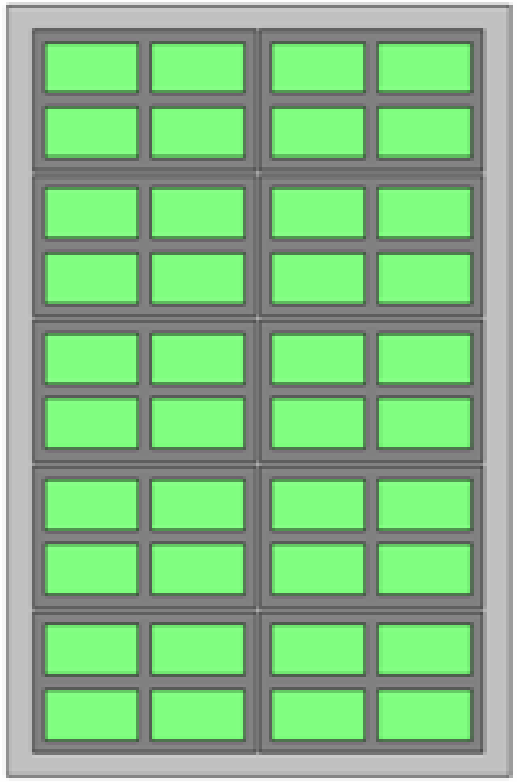
Matrix:
On Panel: 2 x 4, Origin: X3.35 Y0.802
On Array: 1 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.1 x 0.1

Panel Borders:
Left: 3.35 Right: 3.35
Top: 0.802 Bottom: 0.802

Array Borders:
Left: 0.53 Right: 0.53
Top: 0.562 Bottom: 0.562

Revised Panelization - 40 Up



0N6897-49-E redux 25%

Size:
Panel: 18.0 x 24.0
Array: 8.0 x 4.42
Part: 3.4 x 1.61

Panel Yield:
10 Arrays of 4 Parts
40 Parts Total
81.9% Material Utilization

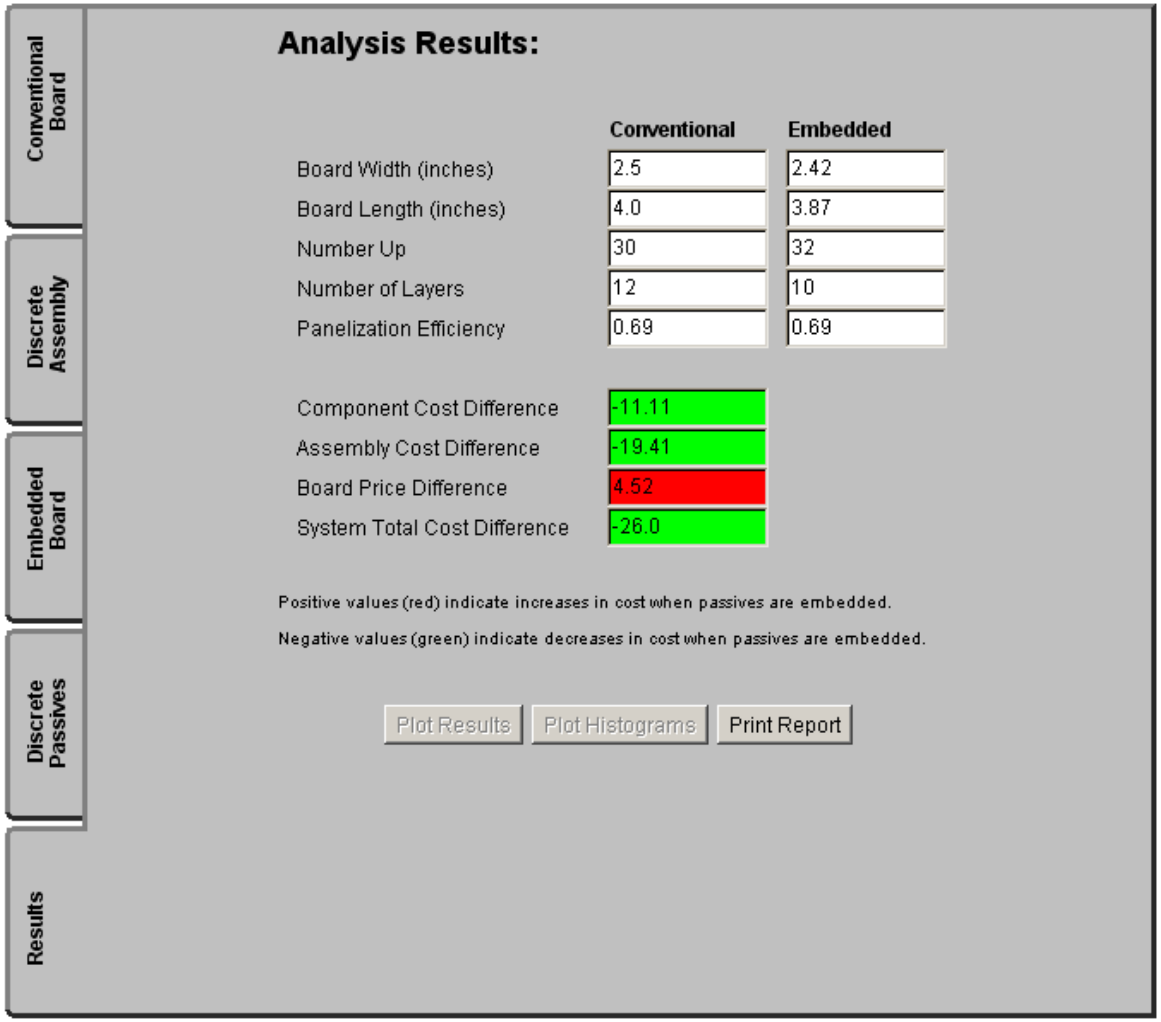
Matrix:
On Panel: 2 x 5, Origin: X0.95 Y0.75
On Array: 2 x 2

Spacing:
On Panel: 0.1 x 0.1
On Array: 0.4 x 0.4

Panel Borders:
Left: 0.95 Right: 0.95
Top: 0.75 Bottom: 0.75

Array Borders:
Left: 0.4 Right: 0.4
Top: 0.4 Bottom: 0.4

Used with the permission of Harris Corporation



Courtesy of Harris Corp. and CALCE

Other Benefits

Capacitor Material vs. FR4

Properties	NiP/Capacitor Core	NiP Core FR-4 (control)	Remarks and Conditions
Sheet Resistivities (ohm/square)	25	25	Nominal
Material Tolerance	+/-5%	+/-5 %	
Load Life Cycling Test Resistor Size: 0.500" X 0.050" Loaded: (Δ R%) @ 150mW Unloaded: (Δ R%)	 <0.9 after 3200 hrs.) <0.74 after 3200 hrs.)	 <5	MIL-STD-202-108I Ambient Temp: 70C On Cycle: 1.5 hrs Off Cycle: 1.5 hrs Length Of Test: 10000 hrs
Current Noise Index in dB	<-23	<-15	MIL-STD-202-308 Voltage Applied: 5.6 Volts
Humidity Test (Δ R%)	0.5	0.5	MIL-STD-202-103A Temp: 40 °C Relative Humidity: 95% Time: 240 hrs
Characteristic (RTC) PPM/°C	-6.0	50	MIL-STD-202-304 Hot Cycle: 25°, 50°,75° 125°C Cold Cycle: 25°, 0°,-25°, -55°C
Thermal Shock (Δ R%)	0.2	-0.5	MIL-STD-202-107B No of Cycles: 25 Hot Cycle Temp: 125 °C Cold Cycle Temp: -65 °C
Solder Float (Δ R%) After 1 Cycle After 5 cycles	 -0.4 -0.6	0.5	MIL-STD-202-210D Temp: 260°C Immersion: 20 Second
Power Density (mW/mil ^{2}) derated at 50%	0.45	0.15	Step-up Power Test Resistor size 0.020" x 0.030"

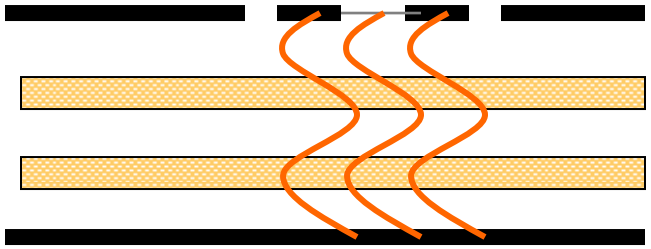
Synergistic Effect !

3X better power density through resistor due to better heat conductivity of the buried capacitor laminate

Buried Capacitance™ Core

Some ultra thin laminates have **3** to **5** times better heat transfer

Standard Core



Thinner dielectric provides better heat transfer

Conclusion

- **Embedded Capacitor and can Improve System Price/Performance by**
  - **Reducing Discrete Caps**
  - **Reducing PWB size**
  - **Increasing Functionality**
  - **Improving power distribution**
  - **Improving Signal integrity**
- **Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency**
- **New Substrates have demonstrated *excellent* electrical performance and physical properties.**
- **They are *compatible* with PCB processing; a truly "drop in" material.**
- **Materials are commercially available from many Fabricators**
- **Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PCBs**
- **GREEN and Lead Free Solution**

Thank You