



**ED/CPMT Chapters of IEEE Orlando Section
AVS and IEEE Student Chapters of UCF
Present guest lecture by**

Dr. Raj Jammy

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IBM Assignee at SEMATECH, Austin, TX**

**20th October, 2006; 12:00 to 1:30
BA 116**

CMOS Scaling and Manufacturing Challenges in the Nano-era

Abstract: As CMOS devices head into the nano-era, a host of new challenges confront the industry - both for scaling as well as for manufacturing. Many device parameters that were hitherto scaled aggressively appear to be hitting roadblocks, at the sametime economic imperatives drive the industry towards further scaling and increased functionality.

CMOS scaling trends, key elements that are under consideration for continued scaling of CMOS devices like gate stack, mobility enhancement in channels, junctions and feasibility of alternate device structures will be reviewed along with some recent results.

Bio: Dr. Raj Jammy graduated with a doctoral degree in Electrical Engineering from Northwestern University in November 1996. He then joined IBM's Semiconductor Research and Development Center in East Fishkill, NY, where he worked on development of ultra-thin dielectrics, advanced doping techniques and other front end of line technologies for deep trench DRAMs. In January 2001 he was appointed as Manager of the Thermal Processes, and Surface Preparation group with additional responsibilities in CMP, Thin Films and Metallization in the DRAM development organization. He moved to IBM T. J. Watson Research Center in Yorktown Heights, NY in June 2002 to manage IBM's efforts on high k gate dielectrics and metal gates. Since June 2005 he has been on assignment from IBM as the director of the Front End Processes Division at SEMATECH in Austin, TX. He holds more than 45 patents and is an author/co-author of over 65 publications/presentations.

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