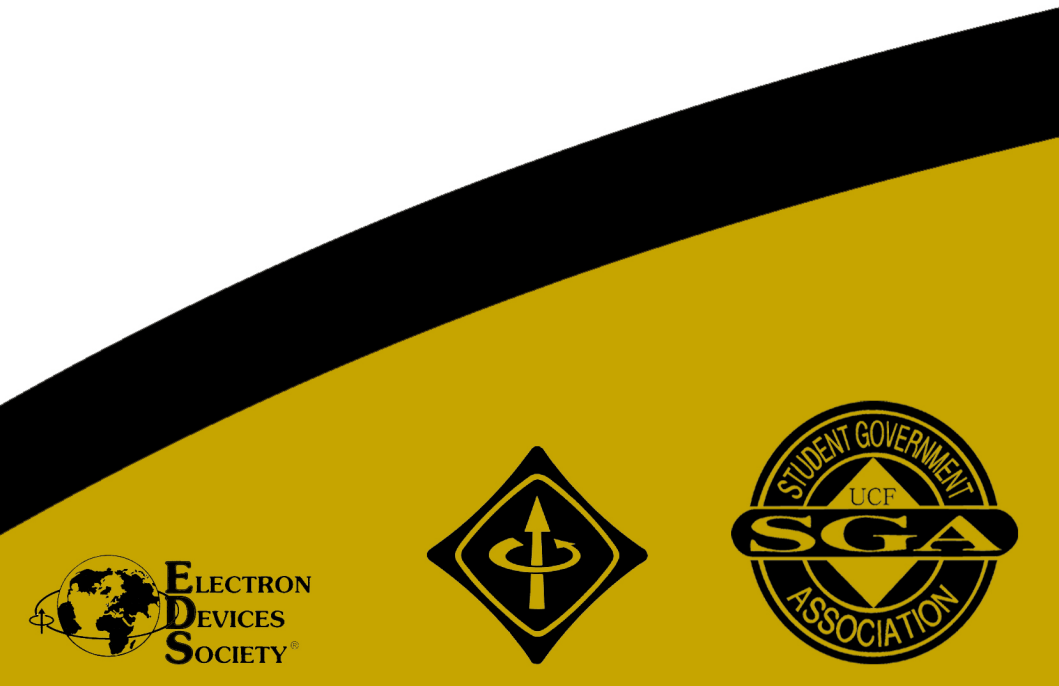
University of Central Florida

IEEE
International Electron Device and Materials Colloquium
Feb 24 - 25 2006



ELECTRON DEVICES SOCIETY®

STUDENT GOVERNMENT ASSOCIATION UCF SGA

Welcome

On behalf of the ED chapter of the Orlando section, I would like to welcome you to the IEEE International Electron Devices and Materials Colloquium. This colloquium is packed with a wealth of knowledge and information, with sixteen internationally recognized distinguished lecturers presenting on different fields of interest in the Electron Device Society. This colloquium will provide an excellent opportunity to UCF's graduate and undergraduate students to interact and exchange their ideas and research activities with these experts. This colloquium is also aimed at providing a networking opportunity for the IEEE members in the central Florida region.

I would like to thank all the sponsors of this event that includes the Student Government Association of UCF, the IEEE Electron Devices society, the IEEE Orlando Section, School of Electrical Engineering and Computer Science, AVS and IEEE student chapters of UCF and John Wiley and Sons. I would also like to thank Drs K. B. Sundaram and J. J. Liou for their guidance in planning this entire colloquium. At this time I would also like to thank Mathew Erickson the current President of IEEE student branch at UCF for his excellent help in the planning and execution of this colloquium. I would also like to thank Vu Lam and Arun Vijayakumar for logistic support. Last but not least, I thank all the Distinguished Lecturers for taking time out of their busy schedules to come to Orlando to participate in this event.

It is again my great honor and pleasure to extend a warm welcome to everyone attending this International Electron Devices and Materials Colloquium.

Ravi Todi
Chair

Program

Friday, Feb. 24th, 2006 (Cape Florida 316 AB Student Union)

8:00 – 8:30	Continental Breakfast
8:30 – 8:40	Welcome Note – Mr. Ravi Todi (Chair: IEEE Electron Device Society, Orlando Section)
8:40 – 8:50	Dean's Address– Dr. Neal Gallagher (Dean College of Engineering and Computer Science)
8:50 – 9:00	Director's Message – Dr. Issa Batarseh (Director School of Electrical Engineering and Computer Science)
9:00 – 9:40	Dr. Ilesanmi Adesida – Processing and Device Issues in GaN and Related Materials
9:40 – 10:20	Dr. Michael Shur– Terahertz Photonics and Electronics
10:20 – 10:40	Coffee Break
10:40 – 11:20	Dr. Rona Belford – No Strain No Gain
11:20 – 12:00	Dr. Stephen Parke – Impact of Flexible-Threshold, Independent-Double-Gate Nanoscale CMOS Devices on Ultra-Low Power Circuits Designs
12:00 – 1:00	Lunch
1:00 – 1:40	Dr. Cor Claeys – Low Frequency Noise Characterization of Advanced Semiconductor Materials and Devices
1:40 – 2:20	Dr. Durga Misra – High-k Gate Dielectrics for Sub-65 nm CMOS Devices
2:20 – 3:00	Dr. Jack Lee – High-k and "Higher-k" Dielectrics
3:00 – 3:20	Coffee Break
3:20 – 4:00	Dr. Supratik Guha – High-k Gate Stacks for Silicon Technology: Materials Interactions at the Nano-scale
4:00 – 4:40	Dr. Kevin Coffey – The Electrical Resistivity of Interconnects: The Classical Size Effect
4:40 – 5:20	Dr. Paul Agnello – Integration Challenges for 45 nm Node and Beyond
7:00 – 10:00	Dinner Reception (by invitation only)

Program

Saturday, Feb. 25th, 2006 (Key West 218 AB Student Union)

9:00 – 9:30	Continental Breakfast
9:30 – 10:10	Dr. Jamal Deen- Highly Sensitive Integrated Biosensor
10:10 – 10:50	Dr. V ik Kapoor - Bio-Electronics Nanotechnology for the Brain
10:50 - 11:10	Coffee Break
11:10 – 11:50	Dr. Francisco Garcia Sanchez – Application of Lambert's W function to electron Device Modeling
11:50 – 12:30	Dr. Paul Yu - High Power Photodiode for Antenna Applications
12:30 – 1:30	Lunch
1:30 – 2:10	Dr. Samar Saha - Design Consideration for Sub-90 nm Split-Gate Flash Memory-Cells
2:10 – 2:50	Dr. Jun J. Liou - Robust Electronic Discharge(ESD) Protection in CMOS Technology
2:50 – 3:00	Vote of Thanks – Matthew Erickson /Ravi Todi
3:00 – 4:00	UCF campus Tour

Ilesanmi Adesida

Ilesanmi Adesida received his Ph.D. degree in electrical engineering from the University of California, Berkeley in 1979. From 1979 to 1984, he worked at the Cornell Nanofabrication Facility and the School of Electrical Engineering, Cornell University. He was the Head of the Electrical Engineering Department at Tafawa Balewa University, Bauchi, Nigeria, from 1985 to 1987. He then joined the University of Illinois at Urbana-Champaign, where he is currently the Donald Biggar Willett Professor of Engineering, the Director of the Center for Nanoscale Science and Technology, and the Interim Dean of the College of Engineering. His research interests include nanofabrication, high-speed optoelectronic devices and circuits. He is a Fellow of IEEE, OSA, AAAS, and AVS. He is currently the President of the IEEE Electron Devices Society.

"Processing and Device Issues in GaN and Related Materials"

Significant and rapid advances in the epitaxial growth of gallium nitride (GaN) and related wide bandgap materials have yielded exciting developments. Both optical and electronic devices have been demonstrated. Light emitting diodes (LEDs) and laser diodes (LDs) operating at various short wavelengths have been shown to be very reliable and are commercially available. AlGaN/GaN heterostructure field effect transistors (HFETs) demonstrating high bandwidths and record microwave powers have also been demonstrated. In spite of these advancements, there are still many issues to be resolved in terms of materials quality, processing methodologies (etching, high temperature stability of ohmic and Schottky contacts, etc), and device design and fabrication. In this talk, we will describe our work on photoelectrochemical (PEC) etching of GaN as a tool for material characterization and device fabrication. Revelations of defect structures especially edge and screw dislocations in n-GaN will be discussed. We will also describe our work on developing thermally stable ohmic and Schottky contacts, inductively coupled plasma reactive ion etching (ICP-RIE) for device fabrication. The DC, RF, CW power and microwave noise performances of AlGaN/GaN HFETs will be presented and discussed.

Michael Shur

Michael Shur received his M. S. E. E. (engineer) degree (with honors) from St. Petersburg Electrotechnical Institute, Ph. D. in Physics and Mathematics from A. F. Ioffe Institute of Physics and Technology and Doctor of Science in Physics and Mathematics degree from A. F. Ioffe Institute in 1992. He is now Patricia W. and C. Sheldon Roberts'48 Professor of Solid State Electronics, Professor of ECSE, Professor of Physics, Applied Physics and Astronomy, Director of Center for Broadband Data Transport Science and Technology, and Director of the RPI Research Site of the NSF I/UCR Center "Connection One." Dr. Shur is a Fellow of Institute of Electrical and Electronic Engineers (IEEE), Fellow and life member of the American Physical Society (APS), Fellow of Electrochemical Society (ECS), Fellow of World Innovation Foundation, Fellow of AAAS, member of Eta Kappa Nu, and Tau Beta Pi, Electromagnetic Academy, Materials Research Society, ASEE, an elected member and former Chair of US Commission D, International Union of Radio Science (URSI), elected Member of NRC of URSI (2003-2004), life member of IEEE MTT, Sigma Xi, and of Humboldt Society of America. He is one of co-developers of AIM-Spice (with over 60,000 users world wide) and co-founder of Sensor Electronics Technology, Inc. He has published many technical papers, authored, co-authored or edited 33 books and 28 book chapters, and has been awarded over 30 patents on semiconductor devices and circuits. Several of his technical publications received the best paper awards. Among his other awards are the Gold Medal of the Russian Ministry of Education, several A. F. Ioffe Best Paper Awards, van der Ziel Award, Senior Humboldt Research Award, Pioneer Award from Compound Semi, RPI School of Engineering Research Award, and Commendation for Excellence in Technical Communications. Dr. Shur is listed by the Institute of Scientific Information (ISI) as one of the Highly Cited Researchers.

"Terahertz Photonics and Electronics"

Terahertz sensing technology has a promise of many breakthrough and enabling applications including detection of biological and chemical hazardous agents, cancer detection, detection of mines and explosives, enhancement of people, building, and airport security, covert communications (in THz and sub-THz windows), and applications in radioastronomy and space research. This tutorial will review the famous THz gap and the-state-of-the-art of existing THz sources, detectors, and sensing systems.

Most existing terahertz sources have low power and rely on optical means of the terahertz radiation. THz quantum cascade lasers using over thousand alternating layers of gallium arsenide and aluminum gallium arsenide have achieved the highest THz powers generated by optical means. Since the energy of a terahertz photon (4.2 meV for 1 THz) is much smaller than the thermal energy at room temperature, room temperature operation of THz lasers might be limited to the high frequency boundary of the terahertz range of frequencies (e.g. close to 30 THz). Improved designs and using quantum dot medium for THz laser cavities are expected to result in improved THz laser performance. Huge THz powers are generated using free electron lasers.

Two-terminal semiconductor devices are capable of operating at the low bound of the THz range, with the highest frequency achieved using Schottky diode frequency multipliers (exceeding 1 THz). High speed three terminal electronic devices (FETs and HBTs) are approaching the THz range (with cutoff frequencies and maximum frequencies of operation around 600 GHz and 340 GHz for InGaAs and SiGe technologies, respectively). A new approach called plasma wave electronics recently demonstrated terahertz emission and detection in GaAs-based and GaN-based HEMTs and in Si MOS and SOI, including the resonant THz detection at room temperature.

Rona Belford

Dr. Belford graduated in 1978 with a First Class Honors degree in Chemistry. During her post graduate studies she changed discipline to Electrical and Electronic Engineering and in 1985 graduated with a Ph.D. in the field of physical electronics at The University of Edinburgh. In 1986 she received the International Prize for Innovative Devices from the Society for Hybrid Microelectronics.

During her tenured post in Edinburgh, lecturing in physical electronics, Dr. Belford ran an active research group concentrating on both electronic and optical materials as sensors. In 1993 she was awarded the RSE research scholarship for research into the behavior of ions in amorphous materials and in 1994 she took up permanent residence in the US. During 1997-99 she initiated and ran a research effort studying strained-Si technology with Edinburgh University. In 1999 she founded Belford Research Inc., for the purpose of researching and exploiting mechanical ways to strain silicon.

Dr. Belford is an Honorary Fellow of the College of Science and Engineering at The University of Edinburgh. She is a Chartered Engineer and a member of the Institution of Electrical Engineers (1990), member of the Institute of Electrical and Electronic Engineers (2000) and the Electron Devices Society (2001). She is also a Chartered Scientist, a Chartered Chemist and a member of Royal Soc. of Chemistry (1978).

“No Strain No Gain”

The quest for ever faster CMOS capability has resulted in deep submicron manufacturing ability. In a normal single scaling step, the channel is reduced by 1/3. As the channel length decreases, capacitance decreases and in reality the delay is reduced by ½ aided to some extent by velocity overshoot. A smaller device equates to faster processing and economy of scale. The latter is no longer true. Reaching the 130 nm node was the first time that the economy of scale was not long-lived enough to offset the costs of research require to attain this node. Still unhappy with yield and longevity, Intel was moved by peer pressure to dip down to 90 nm. New architecture, new dielectrics and conducting materials still couldn’t make up the short fall. These deep submicron devices were just not fast enough. The introduction of strain really saved the day; speed was boosted by up to 30% and power density reduced.

Straining the MOSFET channel has alleviated much of the pressure to attain device speed, and has slowed the need to fabricate smaller nodes. There are a variety of techniques used to create strain. For example biaxial strain can be attained by UHVCVD of Si on to substrates of larger lattice spacing. Local uniaxial strain can be induced by standard processing techniques; for example compression in the p-channel is induced by ion implanting Ge into the source and drain. Strain can be brought about at either wafer-scale or induced locally. Strain can be biaxial or uniaxial; tensile or compressive. The methods of inducing strain are various and have varying degrees of success.

Presented here are results of five years of research and innovation. A number of techniques are described and results given for some of our most outstanding experiments. The methods illustrated here all involve a mix of a number of disciplines including physical electronics and mechanics.

Stephen Parke

Dr. Stephen Parke received the BS and MS degrees in electrical engineering from Purdue University in 1984. In 1984, he joined IBM Microelectronics Division in Essex Junction, VT, where he worked in advanced DRAM process and silicon device design. In 1989, he was awarded an IBM Ph.D. Fellowship, and joined the UC Berkeley Device Research group. He designed, fabricated and studied the behavior of deep-sub-micron MOSFET and lateral bipolar transistors on thin-film SOI, achieving a world-record switching speed in a fully complementary SOI BiCMOS process. He was a co-inventor of the Dynamic Threshold MOSFET (DTMOS) for sub-volt, low-power portable CMOS applications. In 1993, he received the Ph.D. degree and joined the IBM Semiconductor R&D Center in Fishkill, NY where he worked in the 256Mb DRAM process development alliance between IBM, Toshiba, and Infineon. In August 1996, he joined the Electrical Engineering faculty of Boise State University at the inception of its new College of Engineering. He developed several new microelectronics courses and laboratories at BSU. He initiated the construction and equipping of the Idaho Microfabrication Lab cleanroom, which opened in 1998. Dr. Parke currently leads Boise State's RF-SOI research group which is involved in extensive advanced CMOS technology development, funded by NSF, DoD, and local start-up companies. His group is working on radiation-hardened ultra-low-power integrated circuit technology for aerospace and communication applications. He is an Associate Professor of Electrical Engineering at BSU, and Chief Scientist at American Semiconductor, Inc. in Boise. Dr. Parke holds nine patents and has authored or co-authored over 30 research papers. He is a Senior Member of IEEE, a 2000 IEEE Millenium medallist, and an international leader in the IEEE Electron Device Society. He is also a member of Tau Beta Pi and Eta Kappa Nu honorary societies.

"Impact of Flexible-Threshold, Independent-Double-Gate Nanoscale CMOS Devices on Ultra-Low-Power Circuit Designs"

The ITRS roadmap predicts that double-gate devices will be required at the 45nm CMOS node, in order to preserve adequate electrostatic gate control of scaled channel lengths. A variety of double-gate transistors are under development, such as FinFET, Tri-Gate, etc. However, it has become clear over the past couple of years, that an even more promising advantage of double-gate devices is their ability to independently control both gates, using one gate to shift the threshold voltage (and therefore the power vs. speed/gain tradeoff) and the other gate as the signal input. It is also possible to use both gates as signal inputs to halve the number of transistors required for static, dynamic, and passgate digital logic families, or to build ideal one-transistor mixers and varactors for analog/mixed-signal/RF circuits. Flexible-threshold IDG-CMOS devices such as FlexFET and MigFET are now under development, providing early demonstration of some of these circuit advantages. Static leakage can be reduced below the femptoamp level at the same time that drive current is enhanced by 70% to 1.5mA/um. These circuit design advantages of IDG-CMOS are so compelling that implementation at the 130nm, 90nm, and 65nm nodes is desirable. This paper uses the 130nm FlexFET IDG-CMOS technology that has been developed by American Semiconductor, Inc. and Boise State University as the basis for implementing various exciting ULP circuit design concepts

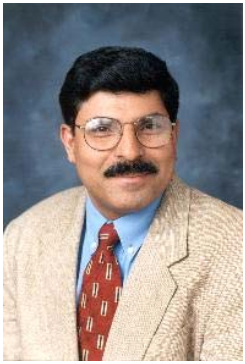
Jack Lee

Jack C. Lee received the B.S. and M.S. degrees in electrical engineering from University of California, Los Angeles, in 1980 and 1981, respectively; and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1988. He is a Professor of the Electrical and Computer Engineering Department and holds the Cullen Trust For Higher Education Endowed Professorship in Engineering at The University of Texas at Austin. From 1981 to 1984, he was a Member of Technical Staff at the TRW Microelectronics Center, CA, in the High-Speed Bipolar Device Program. He worked on bipolar circuit design, fabrication and testing. In 1988, he joined the faculty of The University of Texas at Austin. His current research interests include thin dielectric breakdown and reliability, high-K gate dielectrics and gate electrode, high-K thin films for semiconductor memory applications, and semiconductor device fabrication processes, characterization and modeling. He has published over 250 journal publications and conference proceedings. Dr. Lee has been awarded two Best Paper Awards, numerous Teaching/Research Awards and several patents. Dr. Lee is a Fellow of IEEE.

“High-K and "Higher-K" Dielectrics”

Scaling gate oxide thickness of MOSFET is known to improve short channel effects, subthreshold characteristics, drive current and transconductance. However, oxide thinning also results in an increased gate leakage current and standby power, degraded dielectric reliability and more severe impurity penetration effects. High dielectric constant (high-K) thin films might provide solution since physical thickness can be made thicker while maintaining high capacitance. Hafnium-based high-K dielectrics such as HfO2, HfON and HfSiON have attracted a great deal of attention because of their potential for successful integration into CMOS technology. However, channel mobility degradation, charge trapping and reliability are major concerns. In this talk, we will discuss various techniques (e.g. optimization of interfacial layer, incorporation of N, Si, Al and La, high-temperature forming gas anneal and optimized profiles) for improving channel mobility, EOT (equivalent oxide thickness) scaling and reliability of high-K devices. Process trade-off will be discussed in detail. For example, nitrogen incorporation is known to reduce interfacial oxidation and thus allows EOT scaling. However, it does result in higher interface charge density and degraded mobility. Alternative methods to achieve thinner EOT without N incorporation will also be discussed. More recently, "higher-K" (i.e. K > 25) dielectrics have been proposed in order to scale down EOT below 1.0nm. We will review potential candidates and the challenges. We will also present our recent experimental results of Hf-Ti-O dielectrics. Finally, we will present the transient charge effects of high-K dielectrics on CMOS inverter and ring oscillator operation.

Durga Misra



Dr. Durgamadhab (Durga) Misra has received his M.S. and Ph.D. degrees both in Electrical Engineering from University of Waterloo, Waterloo, Canada. He has been with the Department of Electrical and Computer Engineering of New Jersey Institute of Technology (NJIT) as a faculty member since the fall of 1988. His current research focus is deep-submicron CMOS gate stacks. He received several research awards from the National Science Foundation and Industry. In 1997 he worked at the VLSI Research Department at Bell Laboratories of Lucent Technologies. He received IEEE Regional Activities Board's International Leadership Award and is currently a Distinguished Lecturer of Electron Device Society of IEEE. He has organized many International Symposiums on Solid-State Science and Technology field during the Technical Meetings of the Electrochemical Society and IEEE. He served as the Chairman of North Jersey Section of IEEE during 2003 and 2004.

“High-K Gate Dielectrics for sub-65nm CMOS Devices”

To achieve the International Technology Roadmap for Semiconductors (ITRS) objective both low-k and high-k dielectric materials will be integrated into standard CMOS technologies. For high speed interconnects low-k is a requirement. Stringent power requirements in the chips, on the other hand, dictate replacement of silicon dioxide as it has already reached the direct tunneling regime. In this talk some of the on-going research work on charge trapping in high-k dielectrics such as HfO_2 and $HfSi_xO_y$ will be discussed in detail. Detection mechanism of electrically active intrinsic traps will be outlined. Energy levels of both positively and negatively charged bulk defects have been found to be lying within the Si band-gap. Based on the activation energies of these deep traps and existing theoretical models of intrinsic and extrinsic defects, H-related defects as well as O-related defects are found to be responsible for positive and negative charge trapping respectively. Noise measurements of $HfSi_xO_y$ will be discussed with respect to poly and metal gates. High-k on alternate substrates like Ge substrate will also be discussed.

Cor Claeys

Cor Claeys was born in Antwerp, Belgium. He received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium. From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. Since 1990 he is Head of the research group on Radiation Effects, Cryogenic Electronics and Noise Studies. He is also responsible for Technology Business Development. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He coedited a book "Low Temperature Electronics" and wrote a book "Radiation Effects in Advanced Semiconductor Materials and Devices". He also authored and co-authored six book chapters and more than 600 technical papers and conference contributions related to the above fields. He is an associated Editor for the Journal of the Electrochemical Society.Dr. Claeys is a member of the European Material Research Society, a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter and is presently elected AdCom member of the Electron Devices Society and Vice-President for Chapters and Regions. He also received the IEEE Third Millennium Medal. In 1999 he was elected as Academician and Professor of the International Information Academy. In 2004 he received the Electronics Division Award of the Electrochemical Society.

“Low Frequency Noise Characterization of Advanced Semiconductor Materials and Devices”

This lecture first outlines the different types of low frequency noise occurring in deep submicron silicon MOSFETs and their use as an analytical tool. The noise sources comprise white noise, Generation-Recombination (GR) noise, Random Telegraph Signal (RTS) fluctuations and 1/f or flicker noise. The fundamental basis of each noise type will be briefly described and illustrated by some practical examples. In a second part, the impact of the properties of the silicon substrate (orientation, crystallization technique, SOI, SiGe) on the noise performance is discussed. Finally, the impact on the low-frequency (LF) noise behavior of different advanced process modules, such as gate stack (thermal SiO2, nitrided oxides, high-k materials, metal gates), device isolation (LOCOS and STI based), silicidation, and gate engineering is illustrated. Some state of the art processing such as e.g. FUSI and strained SiGe layers will also be discussed.

Supratik Guha

Supratik Guha is presently Senior Manager, Semiconductor Materials and Devices at the IBM T. J. Watson Research Center in Yorktown Heights, NY, and has been with IBM since 1995. His responsibilities there include driving IBM's research activities in new materials for future CMOS front end applications, technologies for thermal management of microprocessors, and silicon based microphotonics. His own research interests are in the area of nanoscale semiconductor devices and the exploration of new materials technologies on silicon platforms—over the past several years he has been responsible for new materials development at IBM for high dielectric constant advanced gate stacks. In the past he has worked in the area of III-N based light emitting devices on silicon and was responsible for demonstrating the first GaN based LEDs grown on Si. From 1992 to 1995, he was at the 3M Corporate Research Labs where he investigated degradation mechanisms in ZnSe based injection lasers and was a member of the team that developed the first room temperature blue injection lasers. Supratik received his Ph.D. in materials science from the University of Southern California in 1991. He has authored over 60 refereed publications and book chapters and presented numerous invited talks. He holds 20 patents.

“High-k dielectric gate stacks for silicon technology: materials interactions at that nanoscale”

Commercial device structures have so far been simple from an “inter-layer” compatibility perspective-- they have employed either similar materials (such as III-V on III-V) or structures where one element is common (Si/SiO2). This will change, however, if high dielectric constant insulator and metal gates replace the time tested Si-SiO2-polysilicon gate stack of a MOSFET. When nanometer thick layers of such dissimilar materials are stacked on top of one another, with thicknesses that may be spanned by a dozen or so atomic jumps, the “as-grown” layer profiles can end up being significantly altered over time. I will describe some of the key materials phenomena that we have had to understand over the past several years, particularly the role of oxygen and the formation of unwanted interfacial oxide layers, in order to be able to controllably study such structures. These issues, examined in the context of silicon CMOS technology, will be relevant to any devices involving semiconductor-oxide interlayers.

Kevin Coffey

Kevin Coffey received his B.A. in physics from New College in Sarasota, FL in 1975. After an early industrial career in electrophotography and magnetic recording he continued his academic career earning a Ph.D. in Materials Science from the Massachusetts Institute of Technology in 1989. After receiving his doctorate he initially returned to industry, working primarily in the field of thin film magnetic recording materials with IBM, and joined the University of Central Florida in 2002. He is currently an Associate Professor and a member of the Advanced Materials, Processing and Analysis Center (AMPAC) with a home in the Department of Mechanical, Materials, and Aerospace Engineering and an affiliation with the Departments of Physics and Electrical and Computer Engineering. His research interests in the materials science and electronic properties of thin films continue, with special focus on nanoscale conductors, magnetic materials and solid state reactions in thin films.

"The Electrical Resistivity of Interconnects: The Classical Size Effect"

High performance nanoscale conductors are required for interconnecting arrays of future nanoelectronic devices, whether conventional silicon-based MOS transistors or an alternative technology. However, it has long been known that surface and grain boundary scattering lead to strong resistivity increases in conductors with dimensions below about 100 nm. This resistivity increase is known as the "classical size effect" and scales with the electron-phonon scattering length in the metal, which is ~40 nm for Cu. To enable optimum scaling of high performance nano-interconnects at and below the 45nm design node, it is important to understand the physical origin of the conductivity degradation, to guide silicon nanotechnology to new materials and processes that have the greatest potential for high performance nano-interconnects.

The scattering of electrons from grain boundaries and external surfaces both play a role in the classical size effect, but the relative importance of these mechanisms is not yet clear. Previous studies have provided conflicting reports attributing the dominant mechanism to either surface scattering, or to grain boundary scattering, or even to an increase in film contamination as Cu linewidth is reduced. This controversy is primarily because the decrease in film thickness or linewidth of polycrystalline samples is accompanied by a decrease in grain size, and grain boundary and surface scattering give a similar functional form to the resistivity increase as the film thickness/ linewidth (and thus also grain size) is reduced. In this talk we will describe an alternative experimental approach and present the results of our current status to separate the surface and grain boundary scattering in Cu nanoscale conductors.

Paul Agnello

Dr. Agnello received his B.S., M.S., and Ph.D. degrees, all from the Electrical, Computer and Systems Engineering Department of Rensselaer Polytechnic Institute. He joined IBM Thomas J. Watson Research Center in 1988 and the IBM Technology Group in 1992. Over his career at IBM he has worked on low temperature CVD processing of Si and SiGe epi and selective epi, Co and Ti alloy silicide development, 0.25um node device integration and 180nm node Cu BEOL integration. He managed the device integration group responsible for bringing IBM's 130nm and 90nm SOI CMOS technologies to market and currently he manages the High Performance CMOS Integration and Device project responsible for 45nm high performance CMOS technologies. Dr. Agnello is the author or co-author of more than 60 publications and holds more than 15 U.S. patents.

“Integration Challenges for 45nm Node and Beyond”

The author will discuss the High Performance CMOS roadmap and technology scaling. Scaling of technology beyond the 90nm node has been challenging due to the fact that conventional gate dielectrics are at their scaling limit, and supply voltage scaling is proving difficult due to fixed threshold voltages. The industry has turned to strain to enhance channel mobility and improve performance. Local strain provides significant mobility enhancements but its benefits are diminished as ground rules are reduced to 45nm and beyond. This presentation will describe a number of the options that have been investigated for implementing local strain in Si CMOS processes and discuss the option that IBM has chosen for 90nm and 65nm nodes. Integration challenges for some of the options for performance enhancement beyond the 45nm node, such as Hybrid Orientation Technology (HOT) and High K metal gate, will also be discussed.

Jamal Deen

Dr. Jamal Deen was born in Georgetown, Guyana. He completed a Ph.D. degree (1985) in Electrical Engineering and Applied Physics at Case Western Reserve University (CWRU), Cleveland, Ohio, U.S.A. His Ph.D. dissertation was on the design and modeling of a new CARS spectrometer for dynamic temperature measurements and combustion optimization in rocket and jet engines and was sponsored by NASA, Cleveland. He is currently Professor of Electrical and Computer Engineering, McMaster University, Hamilton, Ontario and holder of the Senior Canada Research Chair in Information Technology. Dr. Deen was a Fulbright-Laspau Scholar from 1980 to 1982, an American Vacuum Society Scholar from 1983 to 1984, and an NSERC Senior Industrial Fellow in 1993. He is a Distinguished Lecturer of the IEEE Electron Device Society EDS and has been very active in the Compact Modeling, Education and Optoelectronics EDS committees. Dr. Deen was awarded the 2002 Thomas D. Callinan Award from the Electrochemical Society - Dielectric Science and Technology Division; the Distinguished Researcher Award, Province of Ontario in July 2001; and has won four best paper awards. Dr. Deen is currently an Editor of IEEE Transactions on Electron Devices; Executive Editor of Fluctuations and Noise Letters; and Member of the Editorial Board of Interface, an Electrochemical Society journal and The Journal of Nanoscience and Nanotechnology. His research record includes about 330 peer-reviewed articles (about 70 are invited), 14 invited book chapters and 6 awarded patents. He is a Fellow of IEEE (Institute of Electrical and Electronic Engineers), Fellow of EIC (Engineering Institute of Canada) and a Fellow of ECS (the Electrochemical Society).

“Integrated Biosensor”

Recently there has been an increasing interest in the development of electronic sensors for the detection and identification of biological species. For example, label-free DNA detection has been made possible by the use of field effect sensors. In these systems, the intrinsic charge of the DNA molecules is detected through the use of a modified metal-oxide-semiconductor field-effect transistors (FETs) where the gate area has been functionalized to make them sensitive to the species of interest. The feasibility of this approach has been demonstrated experimentally, but the sensitivity of these systems has to be significantly improved if they are to be used as a means to detect and identify biological species such as pathogen agents quickly and at low cost. The sensitivity of biosensors is ultimately determined by their noise properties: while in principle it is possible to amplify an arbitrarily small electric signal, if this signal is embedded in noise very little information can be recovered. In this presentation, we will discuss a Bio-FET sensor we have been developing for animal pathogen detection. We will discuss the detailed modeling of all important parts of the electrolyte-sensor system and will show that by detailed analyses of both signal and noise characteristics of the integrated sensor system, that it is possible to optimize the Bio-FET’s performance. Finally, we will show how to create highly integrated and parallel detection systems by integrating the sensor and the processing electronics on the same chip and what are the resulting system’s performance characteristics.

Vik Kapoor

Dr. Vik J. Kapoor is A nationally recognized specialist in microelectronics, Prof. Kapoor holds M.S. (1972) and Ph.D. (1976) degrees from Lehigh University, Pennsylvania, where he was awarded the Eastman Kodak prize for excellence in teaching. He went to work in California's Silicon Valley at Fairchild Corp. as a senior design engineer designing computer chips during the cutting edge of the computer revolution. Dr. Kapoor joined Case Western Reserve University in 1978 as an Assistant Professor. He joined the University of Cincinnati in 1983 as Professor and Director of Graduate Studies, and in 1986 became the head of the Electrical and Computer Engineering. He joined the University of Toledo in 1994 as Dean of the College of Engineering and then became the University President in January 1999. He is Professor of Bioengineering and Electrical Engineering and Director of Biomedical Nanotechnology Research Laboratory since June 2000. He is also a courtesy professor of Electrical & Computer Engineering at the University of Central Florida, Orlando since 2004.

He was awarded the "IEEE Third Millennium Medal" in 1999 for his contribution to the Electrical Engineering profession. For his outstanding scientific and technical contributions in semiconductor microelectronics, he was elected a Fellow of the Electrochemical Society in 1993 and was awarded "Thomas D. Callinan Award" in 1991. Dr. Kapoor has published over 170 scientific papers and has been a major advisor for 43 M.S. and Ph.D. students and 34 undergraduate students' projects/theses.

“Bio-Electronics Nanotechnology for the Brain”

Silicon and Silicon Germanium Bio-Electronics nanotechnology is being developed for the investigation of living neural networks of the brain. The action potential generated by the brain neuron placed onto contact with the gate of a field effect transistor modulates the drain-source current of the transistor. This device known as a neuron transistor can be used to obtain noninvasive recordings of neuronal activity. In addition, an array of neuron transistors can be fabricated to obtain information about the activity of neuronal networks. This novel bio-electronics nanotechnology is used in studying the development of living neural networks. This “Hybrid” neural network will allow the study of how neurons maintain and change their interconnections with time. These chips (with memory and sensors) can mimic the function of neurons in the brain and replace damaged parts of the brain for the Alzheimer’s disease. Can the computer think as a brain? What is the on horizon for the next 50 years? Is it molecular-scale electronics or self-assembly molecular electronics for nanotechnology?

Francisco García Sánchez

Francisco. J. García Sánchez was born in 1947 in Madrid, Spain. He received the B.E.E., M.E.E. and Ph.D. degrees in Electrical Engineering from the Catholic University of America, Washington, DC, USA, in 1970, 1972 and 1976, respectively.

In 1977, Prof. García Sánchez joined the faculty of the Electronics Department at Universidad Simón Bolívar (USB), Caracas, Venezuela, where he became a full professor in 1987. He is a member of the External Evaluation Commission of Mexico's National Institute of Astrophysics, Optics, and Electronics. He presently holds a Research Professorship chair at USB, is a Level IV Researcher (highest rank) in Venezuela's Scientific Research System, and is an EDS Distinguished Lecturer. Prof. García Sánchez past research experience is in the areas of polycrystalline compound semiconductor thin- and thick-film deposition techniques for photovoltaic solar cells and sensors, and the electrical characterization and modeling of biological tissues, ceramics and other composite materials. His group's present research interests lay mainly in the area of semiconductor device modeling, especially MOSFETs. He has published over 120 articles (including 18 invited) in national and international refereed technical journals and conferences. He is the coauthor of a book on MOSFET modeling, and has edited several specialized collective works.

He is a past Chair of IEEE´s CAS/ED/PEL Societies Venezuela Joint Chapter, and presently is a member of IEEE Leon K. Kirchmayer Graduate Teaching Award and Undergraduate Teaching Award Committee, a member of EDS Graduate Student Fellowship Subcommittee, Vice-Chair of EDS Subcommittee for Regions & Chapters for Latin America (SRC-LA), and elected member of EDS Administrative Committee (AdCom).

“Applications of Lambert's W function to electron device modeling”

Abstract - Many problems in physics and engineering are described by implicit lineal-exponential equations. Closed-form explicit analytic solutions of these transcendental equations may be obtained by the use of the Lambert W function, thus providing simple expressions that make the described phenomenon more physically understandable and numerically manageable. Explicit solutions based on this function may be readily evaluated and manipulated since it is possible to explicitly differentiate and integrate this function. The amount of Lambert W function applications have significantly increased in recent years. In this talk we explain the usefulness of this function in solving such transcendental equations, which frequently arise in electronics. We present a review of some of its mathematical properties and its numerical evaluation, and examine some of its applications. Its usefulness is illustrated in electron device modeling applications, such as non-ideal junctions with parasitic series resistance and shunt conductance, solar cell characteristics, and channel surface potential in bulk and double-gate undoped MOSFETs.

Paul Yu

Dr. Yu is a professor and Chair of the Department of Electrical and Computer Engineering at the University of California at San Diego (UCSD). At UCSD he is conducting research on semiconductor materials and devices for photonics and microwave applications. His recent work is in the area of analog fiber-optic link for antenna remoting. He is a founding member of the IEEE AP/ED/MTT Chapter of San Diego, the Vice-President of Education Activities of IEEE Electron Device Society (EDS), and a Distinguished Lecturer of EDS. He is a Senior member of IEEE.

“High Power Photodiode for Antenna Applications”

This presentation gives an overview of the requirements of optoelectronic links for their insertion in applications such as CATV, broadband wireless LAN and other sensing applications. In particular, recent developments of high power photodiodes for direct conversion of modulated optical signals to RF signals for antenna transmission will be described.

Samar Saha

Dr. Samar K. Saha, currently, is the Manager of Technology Simulation group at Silicon Storage Technology, Inc., Sunnyvale, CA, an Adjunct Professor in Electrical Engineering department at Santa Clara University, Santa Clara, CA, and an Associate Graduate Faculty in Electrical and Computer Engineering department at the University of Nevada, Las Vegas, NV. Prior to industry, Dr. Saha worked as an Assistant Professor in Electrical Engineering Department at Southern Illinois University, Carbondale, IL, and Auburn University, Auburn, AL. Since 1984 he worked in various positions at National Semiconductor Corporation, LSI Logic Corporation, Texas Instruments, and Philips Semiconductors. He has authored more than 60 papers, holds four US patents, and offered tutorials/short-courses on Technology CAD and Compact modeling. His research interests are in the areas of MOS device and flash memory cell architecture and scaling, Quantum and hot carrier effects, process device and compact modeling, and TCAD and R&D management. He received the Ph.D. degree in physics from Gwahati University and M.S. degree in engineering management from Stanford University. Dr. Saha is a senior member of IEEE and is a Distinguished Lecturer of Electron Devices Society (EDS). He is the chair of IEEE-EDS Compact Modeling Technical Committee, a member of EDS-meetings committee and publications committee, an EDS-representative to the Council of Electronic Design Automation (CEDA), and the treasurer of Santa Clara Valley chapter of IEEE-EDS. He is one of the guest editors of the special issue of IEEE Transactions on Electron Devices on "Advanced Compact Models and 45-nm Modeling Challenges."

“Design Considerations for Sub-90 nm Split-gate Flash Memory-Cells “

In this presentation a systematic procedure for scaling split-gate flash memory cells to sub-90 nm gate length and below is described. A split-gate cell consists of a select gate (SG) with gate oxide thickness of about 15-nm and a floating gate (FG) with tunneling oxide thickness of about 10-nm. The programming operation is achieved by source-side injection (SSI) of hot carriers to FG while erase operation is performed by Fowler-Nordheim (FN) tunneling of carriers from FG to SG. As the SG and FG devices are two MOS transistors in series, referred to as the "2T-cell", the split-gate cell scaling is limited to ~ 120-nm regime and above.

The main limitation of the scaling of the split-gate NVM cell is the programming-coupling ratio (CRP), which is achieved from the drain overlap under FG. As the FG transistor length decreases, the overlap decreases and the programming efficiency decreases due to a decrease in CRP. However, to utilize the full potential of over-erase and over-program immunity and simple program erase mechanisms of the split-gate NVM cells for embedded applications, it is crucial to scale split-gate flash memory cell to sub-90 nm regime. In the recent years, enormous theoretical and experimental studies have been reported to scale the split-gate flash memory cells below 90-nm. In this lecture, different novel 2d- and 3d-cell architectures to scale split-gate flash memory cells to sub-90 nm regime are discussed. First of all, the scaling procedure of the conventional 2T-cells, cell architecture, technology options, and the performance are described. It is shown that the conventional split-gate cell with SG and FG can be scaled down to sub-100 nm regime using the innovative technology design such as SD extensions, highly localized double halo architecture, and so on. Then an option to modify the conventional 2T-cells with an additional coupling gate (CG) to achieve CRP from the top to scale down FG and therefore, the cells to 65-nm regime is presented. Finally, the non-planar 3d-split-gate cell structures with ballistic injection of carriers for fast hot-electron programming are described. The cell performance, reliability issues, 2T and 3T cell compact modeling for circuit simulations for all the cells studied are, also, discussed.

Jun J. Liou

Juin J. Liou received the B.S. (honors), M.S., and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1982, 1983, and 1987, respectively. In 1987, he joined the Department of Electrical and Computer Engineering at the University of Central Florida, Orlando, where he is now a Professor. Dr. Liou has published six textbooks (another in preparation), more than 190 journal papers (including 14 invited articles), and more than 140 papers (including 48 keynote or invited papers) in international and national conference proceedings. He has been awarded more than $5.5 million of research grants from federal agencies, and has held consulting positions with research laboratories and companies in the United States, Japan, Taiwan, and Singapore. In addition, Dr. Liou serves as a technical reviewer for various journals and publishers, a chair or member of the technical program committee for several international conferences, and a regional editor for the Microelectronics Reliability, an international journal published by Elsevier Science Publisher.

Dr. Liou received ten different awards on excellence in teaching and research from the University of Central Florida and six different awards from the IEEE Electron Device Society. Among them, he was awarded the UCF Distinguished Researcher Award three times (1992, 1998, 2002) and the IEEE Joseph M. Biedenbach Outstanding Engineering Educator Award in 2004 for his exemplary teaching, research, and international collaboration. Dr. Liou is an IEEE EDS Distinguished Lecturer, IEEE EDS Treasurer, Chair of the IEEE EDS Finance Committee, Vice-Chair of the IEEE EDS Regions/Chapters Committee, member of the IEEE EDS Administrative Committee, member of the IEEE EDS Educational Activities Committee, member of the IEEE EDS Ex-Officio Administrative Committee, and Senior Member of the IEEE. Dr. Liou is a Fellow of the IEE and holds the Cao Guang-Biao Endowed Professorship from Zhejiang University, China.

“Robust Electrostatic Discharge (ESD) Protection in CMOS Technology”

Electrostatic discharge (ESD) is a process in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and more than 35% of chip damages can be attributed to such an event. An overview on the ESD sources, models, and protection solutions will first be given in this talk. This is followed by the development of a compact yet accurate MOS model suitable for SPICE circuit simulation under the ESD event. Finally, a robust ESD protection solution for data communication transceivers will be presented.

Notes

Colloquium Committee

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Ravi Todi - EECS, University of Central Florida
Orlando FL 32816
rtodi@mail.ucf.edu
Tel. (407)-823-4476 Fax. (407)-823-5835