Integrated Circuits for Extreme Environments using Gallium Nitride Transistors

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Impetus for ICs in Extreme Environments

Irrespective of sensor type, any signal of interest in an extreme environment has to be converted to electronic form at some point along the signal path toward the user interface (e.g., GUI)

- in a highly localized extreme environment, e.g. inside an aircraft jet engine, there is the option to place the electronics out of the “hot zone”

- if the sensor output is a weak electrical signal, best practice is to place the pre-amp as close to the sensor as possible

Impetus for ICs in Extreme Environments

In a non-localized extreme environment, e.g. Venus' surface at 470°C, there is no option to place electronics outside the "hot zone"…it's hot everywhere!

→ cooling systems and heat shields must designed into the overall system solution…

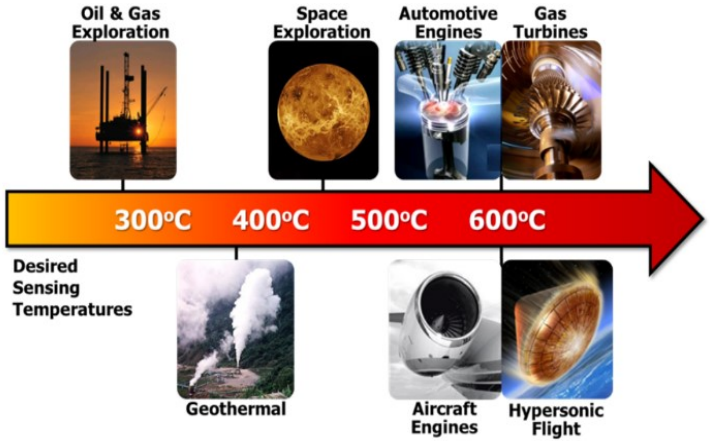
What if reliable cooler-less electronics were available?

Examples of Extreme Environments

- High-Temperature
- Low-Temperature
- Wide Temperature Range
- Erosive Flow and Corrosive Media
- High Pressures
- Intense Vibrations
- Intense Radiation
- Multi-extreme

Applications in Extreme Environments

- Space
- Automotive
- Military
- Geothermal Production Wells and Oil and Gas Well Drilling



ref: XLab, Stanford Univ.

Temperature Limits of Transistor Technologies

"Standard bandgap" semiconductors (~ 1 eV)

- Si technology < 150°C, SOI technology < 300°C
  - control and/or sensing electronics solutions for environments in excess of T limits above must incorporate a cooling system, e.g. Stirling cycle refrigerator
  - **adds cost, weight, complexity and increased risk of failure**

Wide-bandgap semiconductors such as GaN (> 3 eV)

- superior stability at high temperature and in high radiation environments
  - higher bandgap → lower n_i at higher T → remains a semiconductor at higher T
  - **possibility of electronics solutions with no cooling system in 500°C environments**

Advantages of GaN FETs compared to Si and GaAs FETs

GaN is first synthesized in 1932 by Johnson *et al*

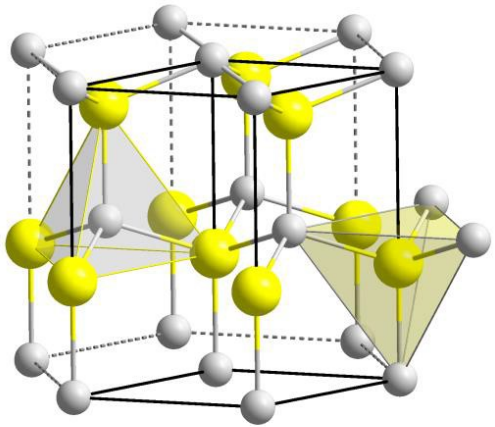


Figure 1 Wurtzite structure of GaN.

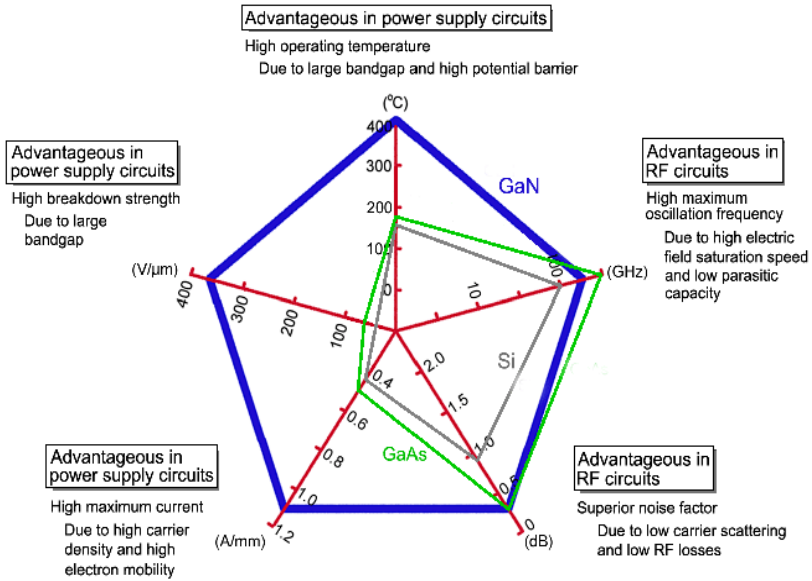


Figure 2 Comparison of breakdown field, maximum oscillation frequency, noise factor, maximum current density, and operating temperature of GaN-, GaAs-, and Si-based FETs.

ref: GaNSystems.com, 2019

Properties of the GaN interface with $Al_xGa_{1-x}N$

- Band-bending and strong polarization at the heterointerface
- Both contribute to formation of a 2-D electron gas (2DEG)
  - no intentional doping required → no ionized impurity scattering to reduce electron mobility
  - high mobility (2000 cm^2/V-s) → "HEMT" (high electron mobility transistor)
  - high 2DEG density (1E13 e^-/cm^2) → high output current (> 1 A/mm)

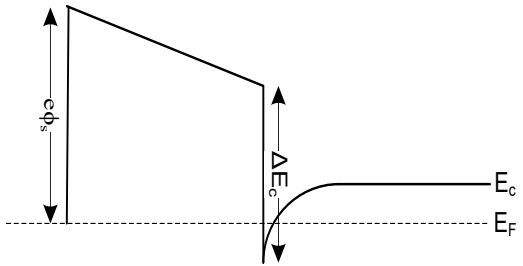


Figure 3 Conduction band diagram of AlGaN/GaN HFET.

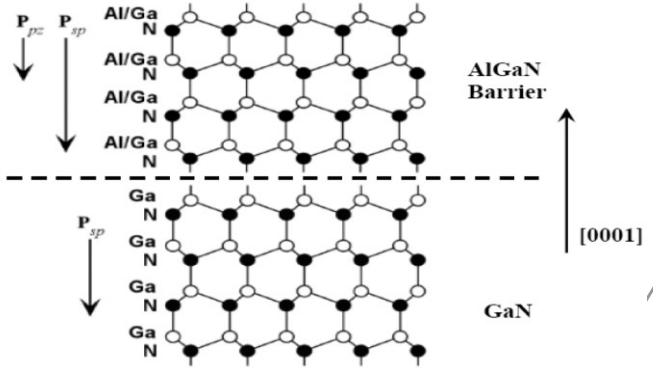


Figure 4 Spontaneous and piezoelectric polarization vectors in a metal-face Wurtzite AlGaN/GaN heterostructure.

Physical Layout of GaN HEMT

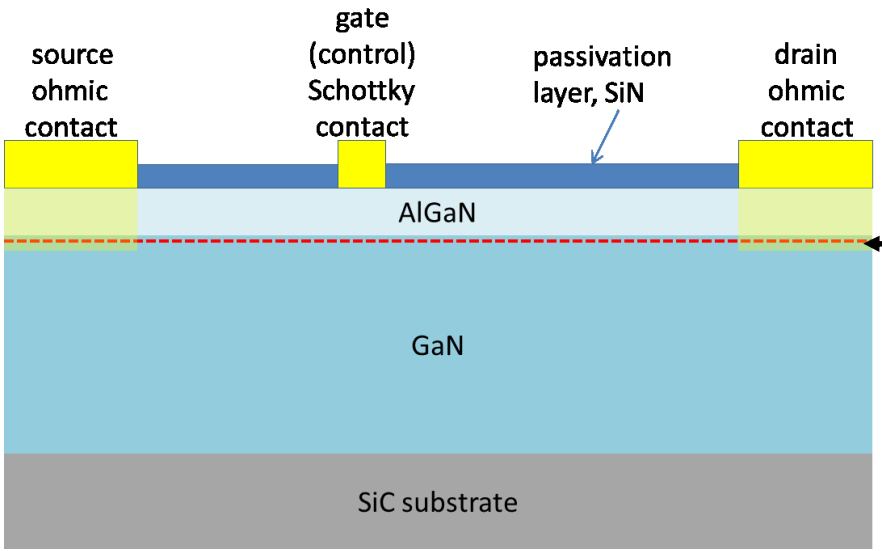


Figure 5. Cross-sectional schematic of a single-finger AlGaN/GaN HEMT.

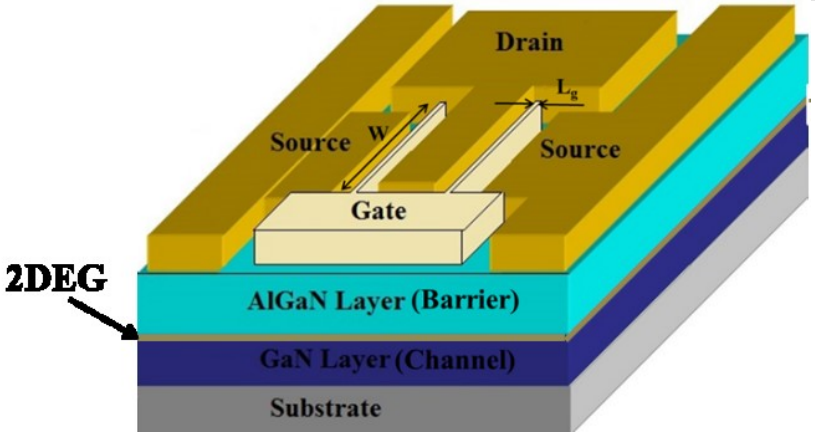


Figure 6. Typical device structure of a two-finger AlGaN/GaN HFET. Lg is the gate length and W is the gate width of the HEMT.

GaN HEMT Limitations to Reliable High T Operation

- Gate contact
  - gate process modification was given highest priority in this work
  - NRC uses a Ni-based gate, which is the industry-standard developed for RF applications such as 5G networks and cell phone transmitter chips
  - Ni works fine for applications < 300°C but…does it diffuse into the semiconductor at higher temp?
- Drain/source Ohmic contacts
  - lower priority: processed at 825°C to achieve Ohmic source and drain contacts…not expected to be an issue for use at 500°C
- Dielectric layers (passivation and capacitors)
  - lower priority: anneal cycles show good mechanical stability up to 600°C

NRC GaN Foundry Technologies: development timeline and features

NRC owns and operates the only GaN foundry in Canada (~ 10 worldwide)

GaN1000, GaN800, GaN500, GaN150 *(depletion mode, normally ON),* **e-GaN500** *(enhancement mode, normally OFF)*

- developed over ~ 15 years, primarily for RF power applications
- MMIC platform (monolithic microwave integrated circuit) on SiC substrates
- all passive elements R, C, L included in Physical Design Kit (PDK)

GaN150 (0.15μm gate length)

- PDK/Design Manual released in 2015
- gate feature size beyond stepper lithography resolution capability; must be patterned with e-beam writer, adding complexity and cost
- achieved target of 10dB gain (38GHz), P_{out} = 5W/mm gate width

GaN500 (0.5μm gate length)

- PDK/Design Manual released 2010, version 3.1 in 2016
- two levels of interconnect metal, including air bridge for 3μm thick 2ME
- GaN500 is the selected platform for current experiments for new applications in extreme environments
- parallel process development of reliable complementary e-mode/d-mode HEMTs

→ **toward GaN-based microprocessors**

Project Phases

1. Materials and discrete HEMTs; anneal cycles and testing at RT

2. On-wafer testing at intended operating temperature (500°C); generate new PDK specific to 500°C Top using neural networks model

3. Full IC design/fab cycles → toward microprocessor applications; start engineering reliability testing of bare die

4. Packaging solution (via partnership), if necessary

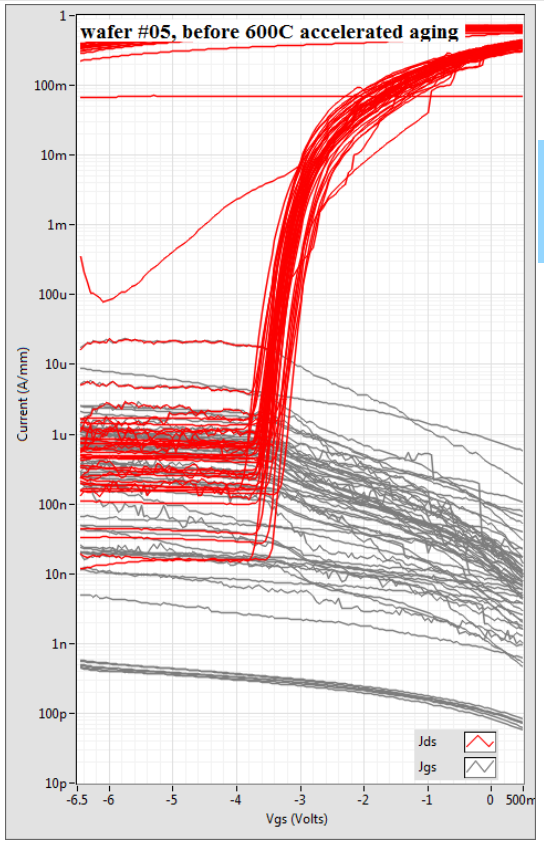
5. Full (integrated die + package) reliability testing and qualification

6. Space qualification (flight), if such an application is sought

Design of Experiment: Phase 1

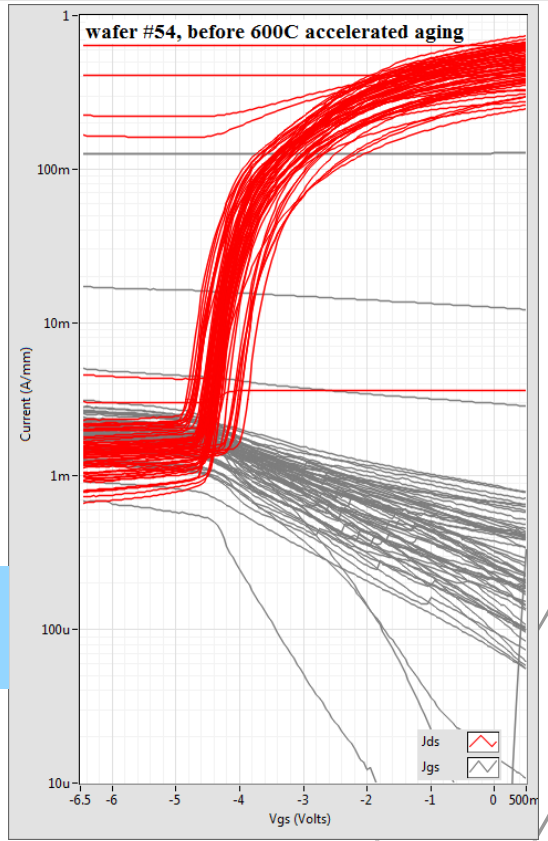
- Fabricate and test nominally identical GaN/AlGaN HEMT wafers, the exception being:
  - NRC modified Ni-based gate processing
  - modified gate process sequence, not just the metal itself
- Devices under test are dual-finger HEMTs with gate lengths 0.5μm, 1.0 μm and 1.5 μm
- Perform Accelerated Aging anneal cycles at **600°C**, then test again
  - plot OFF state drain current (a.k.a. leakage current) vs aging time → stable or failed gate?
- Use a reliability model (Microsemi) with an Arrhenius-based acceleration factor to calculate the predicted MTTF (in days) due to thermal processes only (diffusion) for device operation at **500°C**
  - surviving thermal-only stressing is a necessary condition to passing active testing at the same T

Results: 0.5um Lg devices at t=0, 600°C accelerated aging



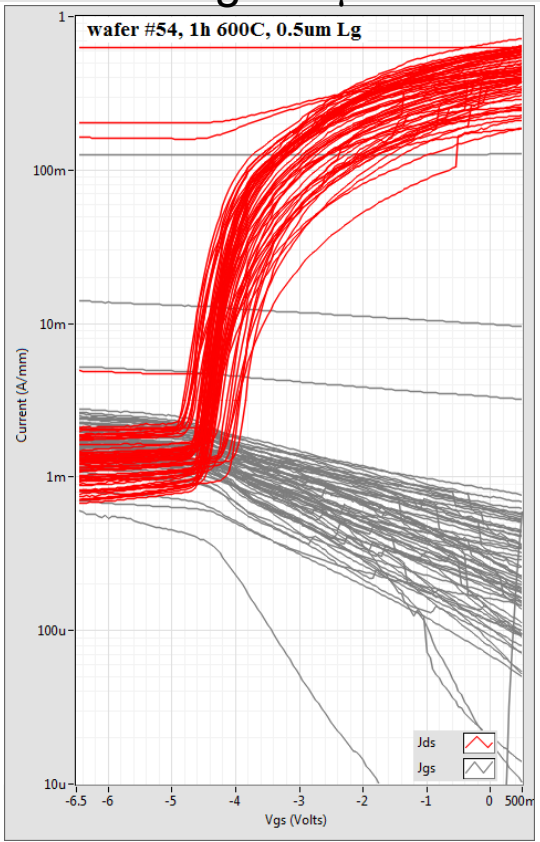
←Ni gate process

modified gate process→

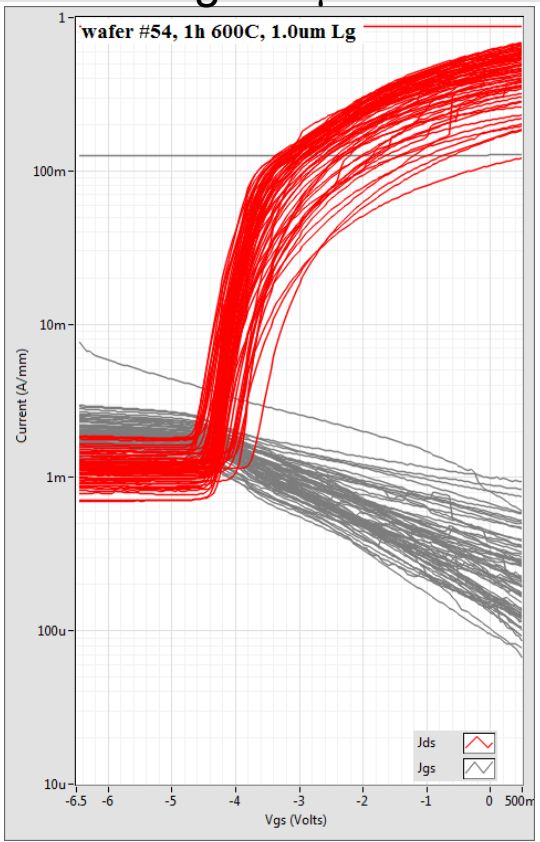


Results: wafer with modified gate process after 1h at 600°C

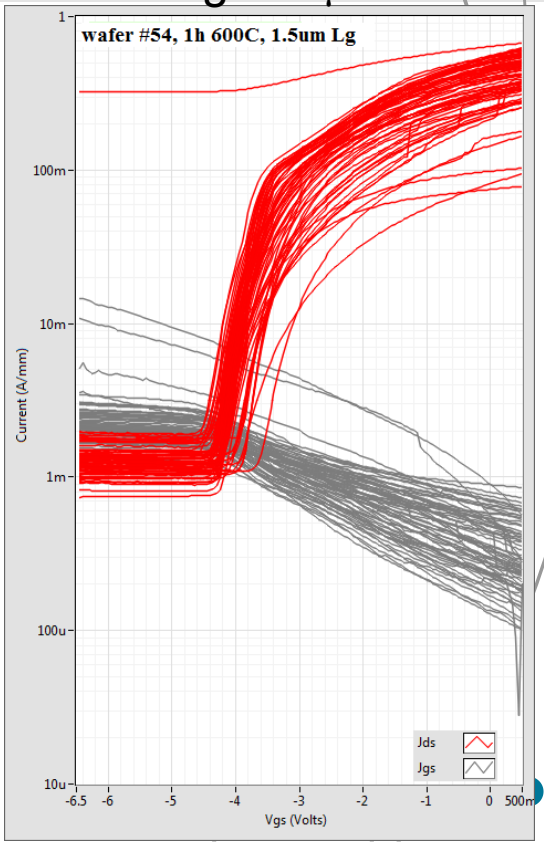
Lg=0.5µm



Lg=1.0µm

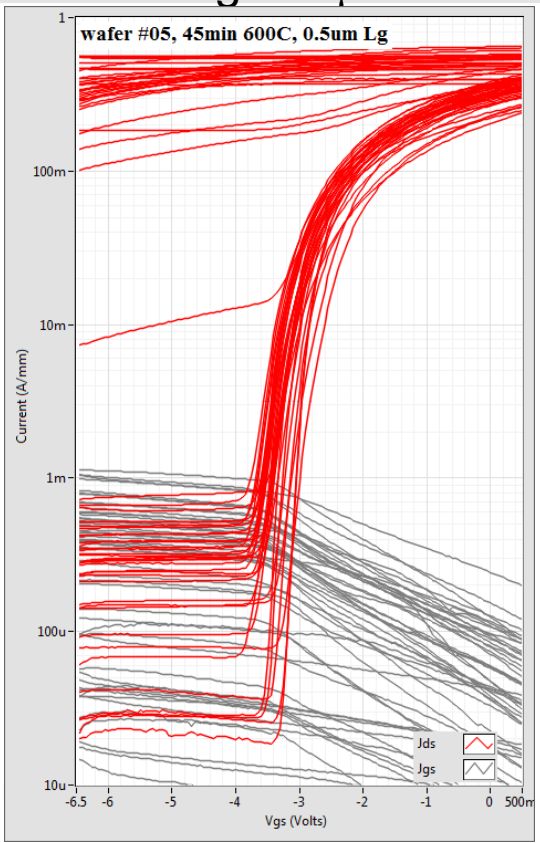


Lg=1.5µm

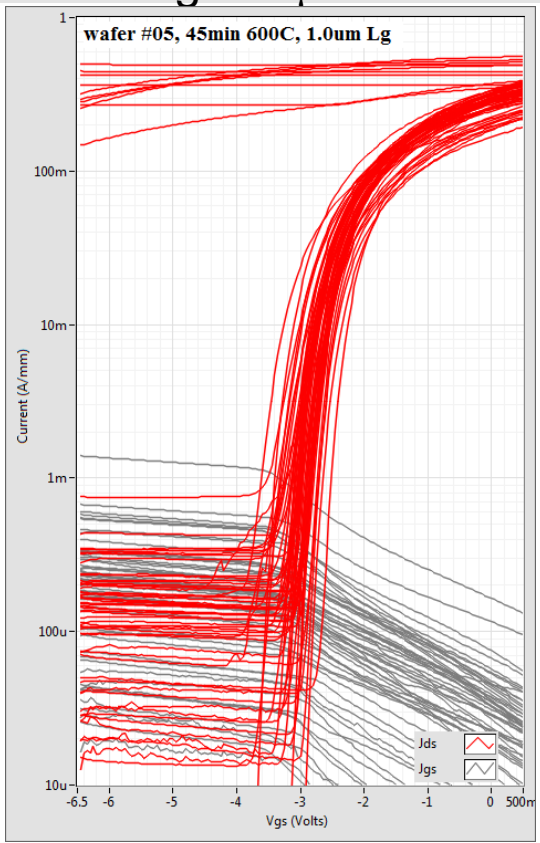


Results: wafer with std Ni gate process after 0.75h at 600°C

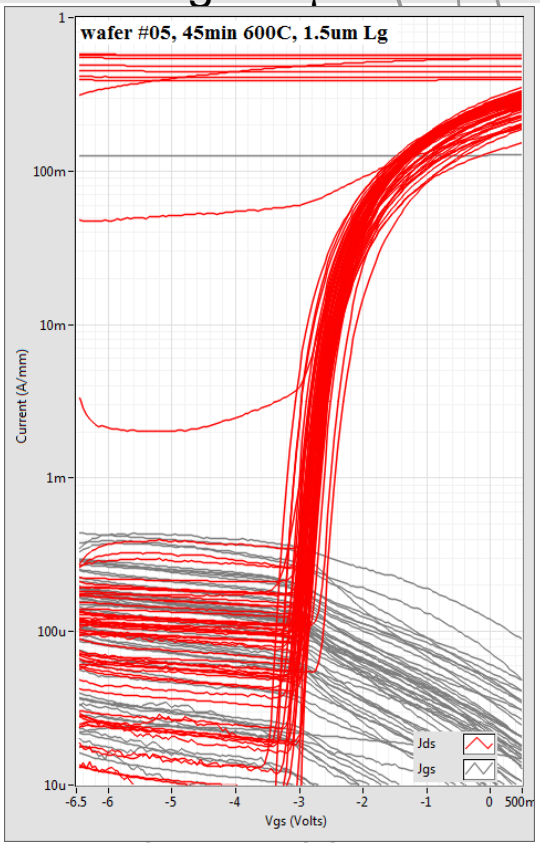
Lg=0.5µm



Lg=1.0µm



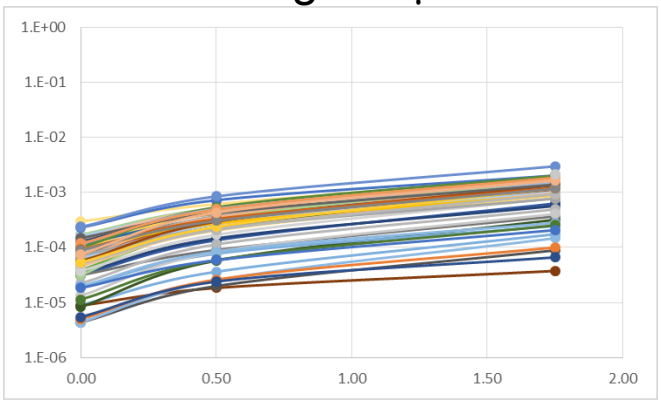
Lg=1.5µm



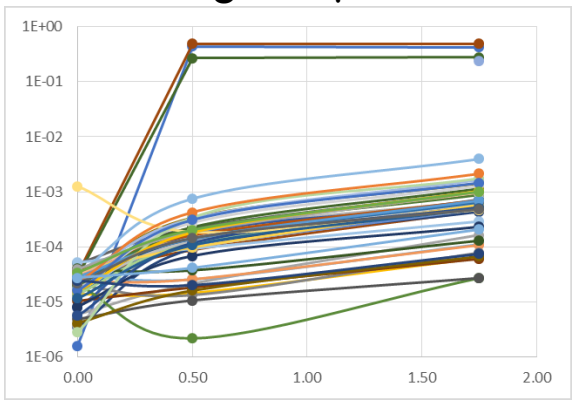
Results: tracking each device, Ni-based gate wafer

Jd OFF (A/mm) vs aging time (h)

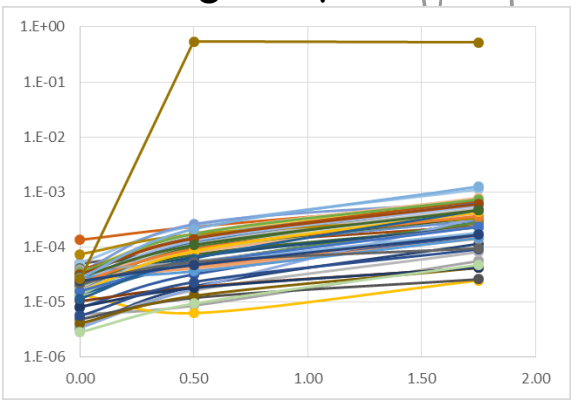
Lg=0.5µm



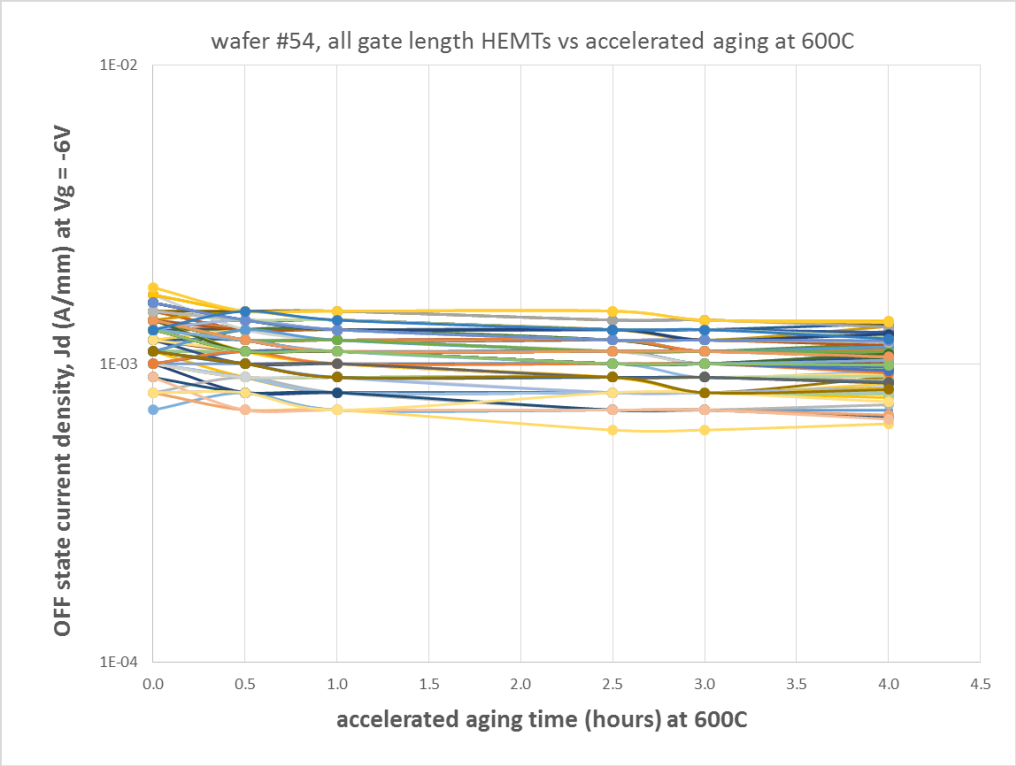
Lg=1.0µm



Lg=1.5µm



Results: tracking each device with aging time, modified gate process



Estimation of MTTF for HEMTs using modified gate process

Reliability Calculator (ref. Microsemi Micronote 1004)

T use (°C)	activation energy Ea (eV)	
500	0.7	*(0.7eV generally accepted value)*

accelerated aging cycle #	T accelerated aging (°C)	time (min)	hours	cumul. hours	number of failures (r)	number of dev tested (D)	acceleration factor Af = (Ea/k)*(1/Tuse-1/Taa)	total # of device hours (DH)	equivalent device hours (EDH)
6	600	60	1.0	4.0	0	125	3.3	125.0	416.6
5	600	30	0.5	3.0	0	125	3.3	62.5	208.3
4	600	30	0.5	2.5	0	125	3.3	62.5	208.3
3	600	60	1.0	2.0	0	125	3.3	125.0	416.6
2	600	30	0.5	1.0	0	125	3.3	62.5	208.3
1	600	30	0.5	0.5	0	125	3.3	62.5	208.3
									1,666 **<--sum of EDH**

CHI SQUARED
at 60% confidence (α)
1.83

Failure Rate (λhour) =	5.50E-04
FIT (failures in 1E9 hours) =	549879
MTTF (hours) =	1,819
MTTF (days) =	**75.8**

SUMMARY / CONCLUSION

- Modified gate process gives **500°C MTTF greater than 76 days**
  - no failures for any gate length device after 4h accelerated aging at 600°C
  - more aging time needed to establish time of 1st failure

- NRC modified Ni-based gate HEMTs
  - 1000x increase in leakage current
  - 4 catastrophic failures occurred (3 for Lg=1.0um, 1 for Lg=1.5um)
    Lg=0.5um **500°C MTTF = 18 days** after 2h accelerated aging at 600°C
    Lg=1.0um **500°C MTTF = 4 days** after 2h accelerated aging at 600°C
    Lg=1.5um **500°C MTTF = 1 day** after 2h accelerated aging at 600°C

NRC modified gate process passes this Phase 1 accelerated aging test toward requirement of 60 day MTTF at 500°C