PV Inverter UL1741/IEEE 1547 Test & Verification

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AC Power Corp.

Preen


Preen
PV Inverter ATE and Verification System
Indicator of working power
Load ON indicator
Indicator of faults
Preen
PV Inverter ATE and Verification System

Agenda

1. Background
2. Overview of present IEEE 1547.1 test Items
3. The importance of Ride Through to avoid cascade failure of the utility grid during server under frequency or voltage events
4. Impacts on test equipment requirements
5. Impacts on product design and development

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About Preen

- Company Name:

  AC Power Corp. (Preen)

- Established: ***1989 in Taiwan***
- Factory Location: ***Taipei, Suzhou, Tianjin***
- Specialized in power electronics, AC Power Corp. (Preen) has been developing products based on its core technology of Power Conversion.

  Product line includes Programmable AC Power Supplies, Programmable DC Power Supplies, Power Supplies for Defense Industries, Renewable Energy Simulators, Line Conditioners and UPS.

  Boasting one of the broadest product lines in the industries, Preen specializes in High Power Source and has developed AC power source up to 2 MVA with high power density.

About Preen Factory Location

Taipei Headquarter & Factory

1989

Suzhou Factory

2001

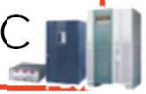
Tianjin Factory

1993

About Preen Product Lines

AC
Power Source
(Frequency Converter)

0.5-2,000kVA

- AFV-P 
- AFV 
- AFC 
- AMF 
- PAS 
- BPS 

DC
Power Supply

2-180kW

- ADG-L 
- ADG-P 
- ADC 

AVR & UPS

1-400kVA

- APS 
- APH 

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AC
Power Source

High Performance Programmable AC Power Supply

AFV-P series

600-5000VA
40-500Hz
15-1000Hz (opt.)

Programmable AC Power Source

AFV series

10-2000kVA

AC Power Source Frequency Converter

AFC series

0.5-2000kVA

Regenerative Grid Simulator

PAS-F series

30-200kVA

Regenerative AC Power Source

PFV series

30-200kVA

Programmable Wide Frequency AC Power Source

PWF series

20-200kVA

45-500Hz

300-800Hz

Solid State Shore Power Supply

BPS series

100-2000kVA

400Hz Power Supply Ground Power

AMF/AMV series

0.5-400kVA

DC
Power Supply

Programmable DC Power Supply

ADG-L series

4-12kW

Programmable High Power DC Power Supply

ADG-P series

30-100kW

Rack Mount DC Power Supply

ADC series

2-64kW

UPS & AVR

Solid State Voltage Regulator

APS series

1-300kVA

Inductive Voltage Regulator

APH series

10-1000kVA

- Background
- Testing Standards and Regulations

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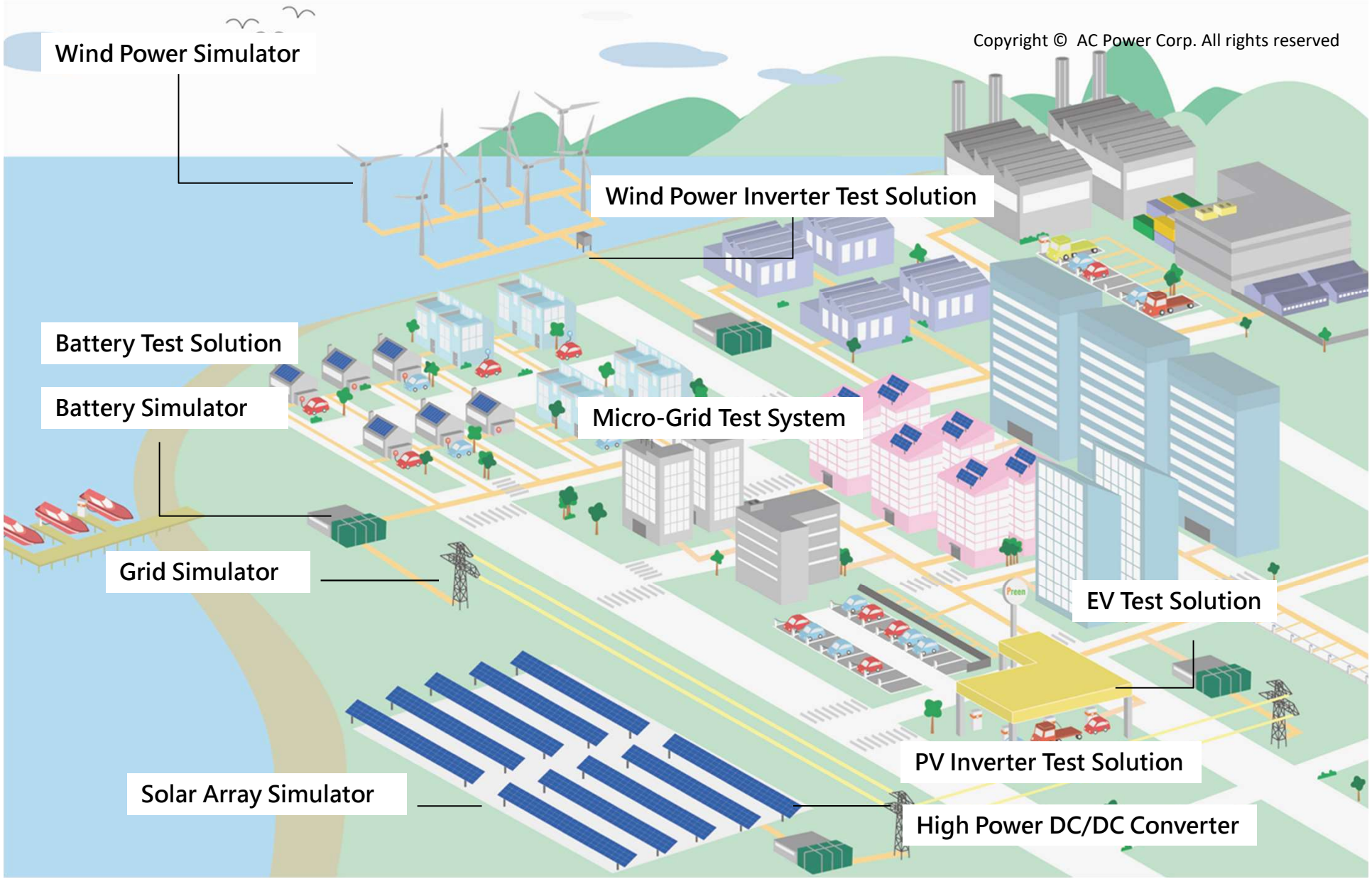
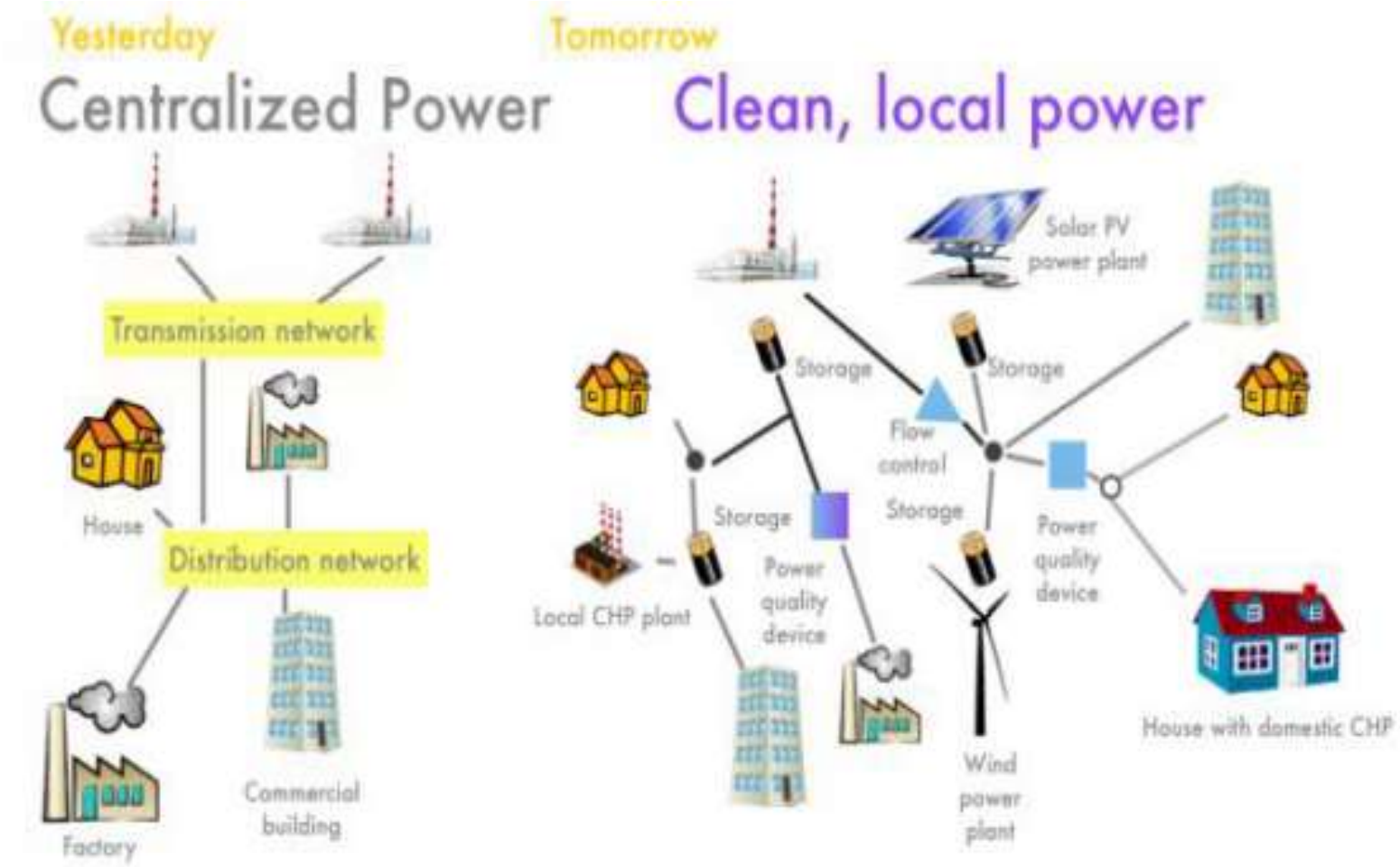
Grid Connect Related Test



Background

- Distributed Resources (DR) Power



International Regulations for Verification(I)

Major related international regulations including the followings:

Product specific	Operation and grid interconnection requirements
UL 1741: Inverter, Converters, Controllers and Interconnection System Equipment for Use with Distributed Energy Resources	**IEEE 1547**: Standard for Interconnecting Distributed Resources with Electric Power Systems
IEC 62116: Test Procedure of Islanding Prevention Measures for Utility- Interconnected Photovoltaic Inverters	**IEC 61727**: Photovoltaic (PV) Systems Characteristics of the Utility Interface
IEC 62109-1/2: Safety of Power Converters for Use in Photovoltaic Power Systems – General requirements	**VDE-AR-N 4105**: Power Generation Systems Connected to the LV Distribution Network
	BDEW : Technical Guideline: Generating Plants Connected to the MV Network
	EN 50438: Requirements for the Connection of Micro-Generators in Parallel with Public Low Voltage Distribution Networks

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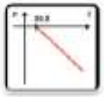
International Regulations for Verification(II)

Major related international standards comparison
IEEE-1547(.1) (US) vs. VDE-AR-N-4105 (Europe)

- **IEEE 1547**:
  - Issued in 2003
  - Kept simple (ignores high PV penetration)
  - For Distributed Sources ≤ 10 MVA and 60 Hz frequency
  - Short tripping times for out-of-bound conditions and long reconnection time limits
  - No grid management features
  - Only IEEE 1547 and 1547.1 are standards, the following parts are so called recommended practices!

- **IEC, EN, VDE, BDEW**
  - More recent (e.g. VDE-AR-N 4105:**2011**)
  - Issued in countries with **very high PV penetrations**
    ⇒ **best practice and expertise**
  - Specific requirements for PV inverter technologies
  - Grid support features (BDEW 2009):
    - Power curtailment 
    - Frequency control P(f) 
    - Reactive power injection (VAR) 
    - Low Voltage Ride Through 
    - Full dynamic grid support

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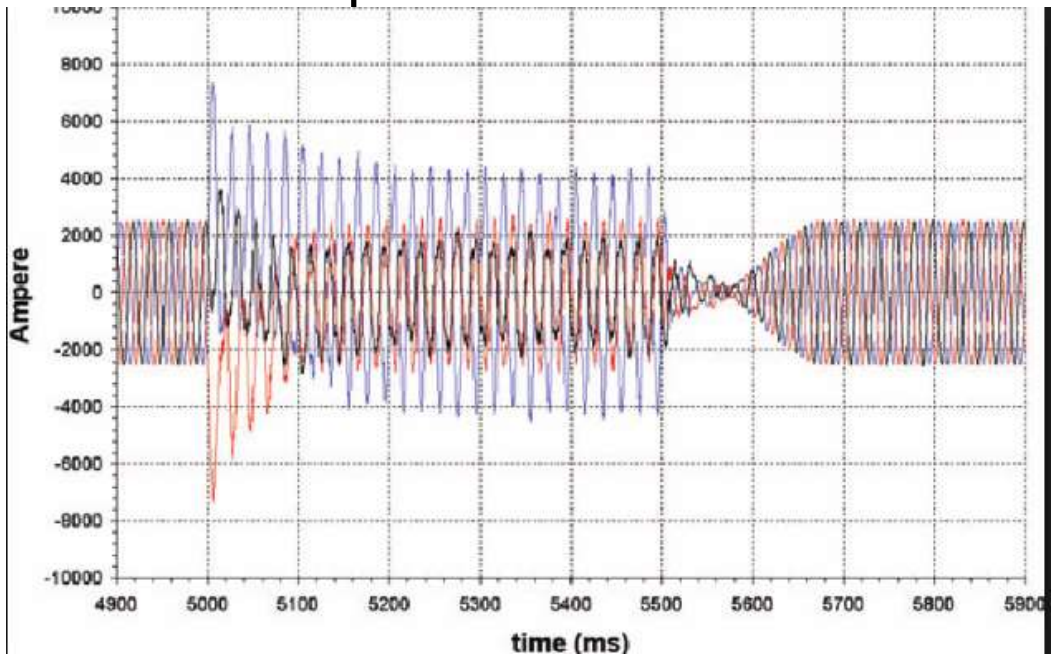
IEEE Standard 1547

- IEEE Standard 1547 is presently being amended to provide more flexibility in the "must trip" requirements, which allow V/FRT to be implemented by utilities or other local entities, but do not mandate these ride-through capabilities. The base IEEE 1547 standard, however, is required by recently-changed IEEE Standards Association rules to undergo full review and potential revision.



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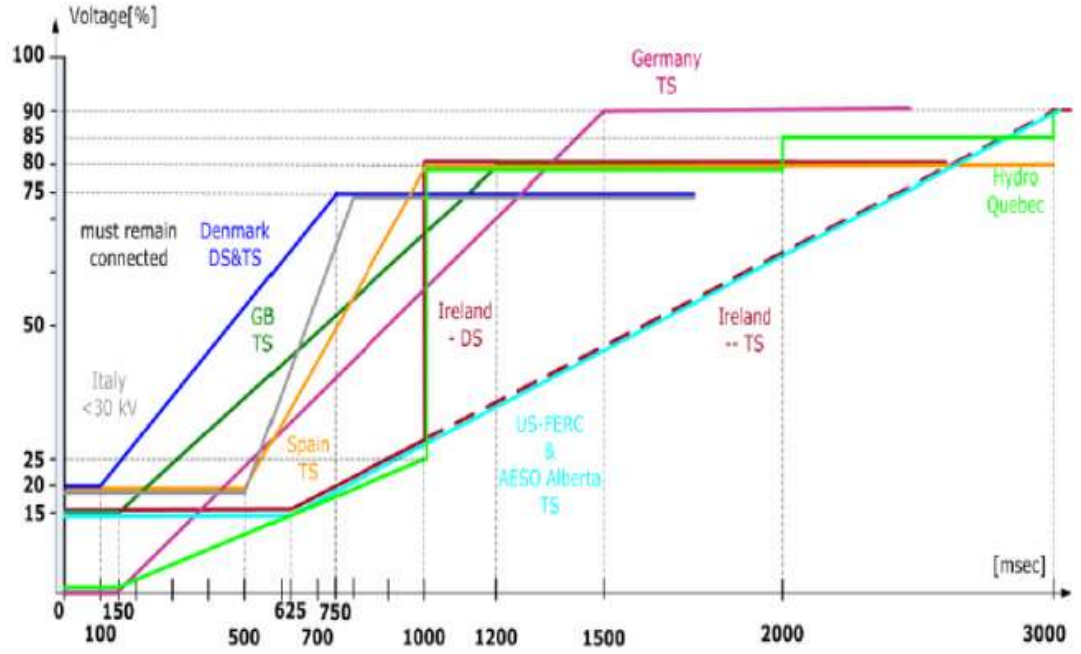
IEEE 1547.1 Test Items

- Response to abnormal voltage conditions (IEEE 1547.1-5.2)
- Response to abnormal frequency conditions(IEEE 1547.1-5.3)
- Synchronization Test (IEEE 1547.1-5.4)
- DC Injection Test (IEEE 1547.1-5.6)
- Anti-Islanding Test (IEEE 1547.1-5.7)
- Open Phase Test (IEEE 1547.1-5.9)
- Reconnect Test (IEEE 1547.1-5.10)
- Harmonics Test (IEEE 1547.1-5.11)

LVRT requirements in international grid codes.

GC Country	During Fault		After Fault	
	V_{min}(%)	T_{max}(s)	V_{min}(%)	T_{max}(s)
Germany	0.0	0.15	90	1.5
Italy	0.0	0.2	85	1.5
Spain	20	0.5	80	1.0
Japan >2016	30	1.0	80	1.5
Japan< 2016	30	1.0	80	1.0
Australia	0.0	0.45	80	0.45
USA	15	0.625	90	3
Denmark	25	0.14	75	0.75



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- Equipment Requirements

Test Instrument Requirements

	Name	Function Requirements
	PV Array Simulation (DC Power Supply)	•Simulate PV Array Characteristic in different lighting condition and temperature. (I-V Curve Simulation) •Satisfy EN50530 Accuracy Requirements (0.05% + 0.05% FS and a current accuracy of 0.1%)
	Grid Simulation (AC Power Source)	•Simulate Grid Voltage and Frequency Variation •Support Low Voltage Rid Through Test or Fault Ride Through Testing (LVRT) •Accuracy Requirements (Voltage 0.1V, Frequency 0.01%)
	RLC Load	•Simulate AC Device Resonance to check the anti-islanding protection function •For examination the working efficiency , maximum output capability •To simulate different working condition for PV Inverter (V, I)
	Measurement System (DAQ, DMM, Power Analyzer)	•Each measurement shall have an uncertainty of no more than 0.5 times the accuracy of the EUT. Measurement equipment shall be capable of confirming the manufacturer's stated performance.

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Test System Overview

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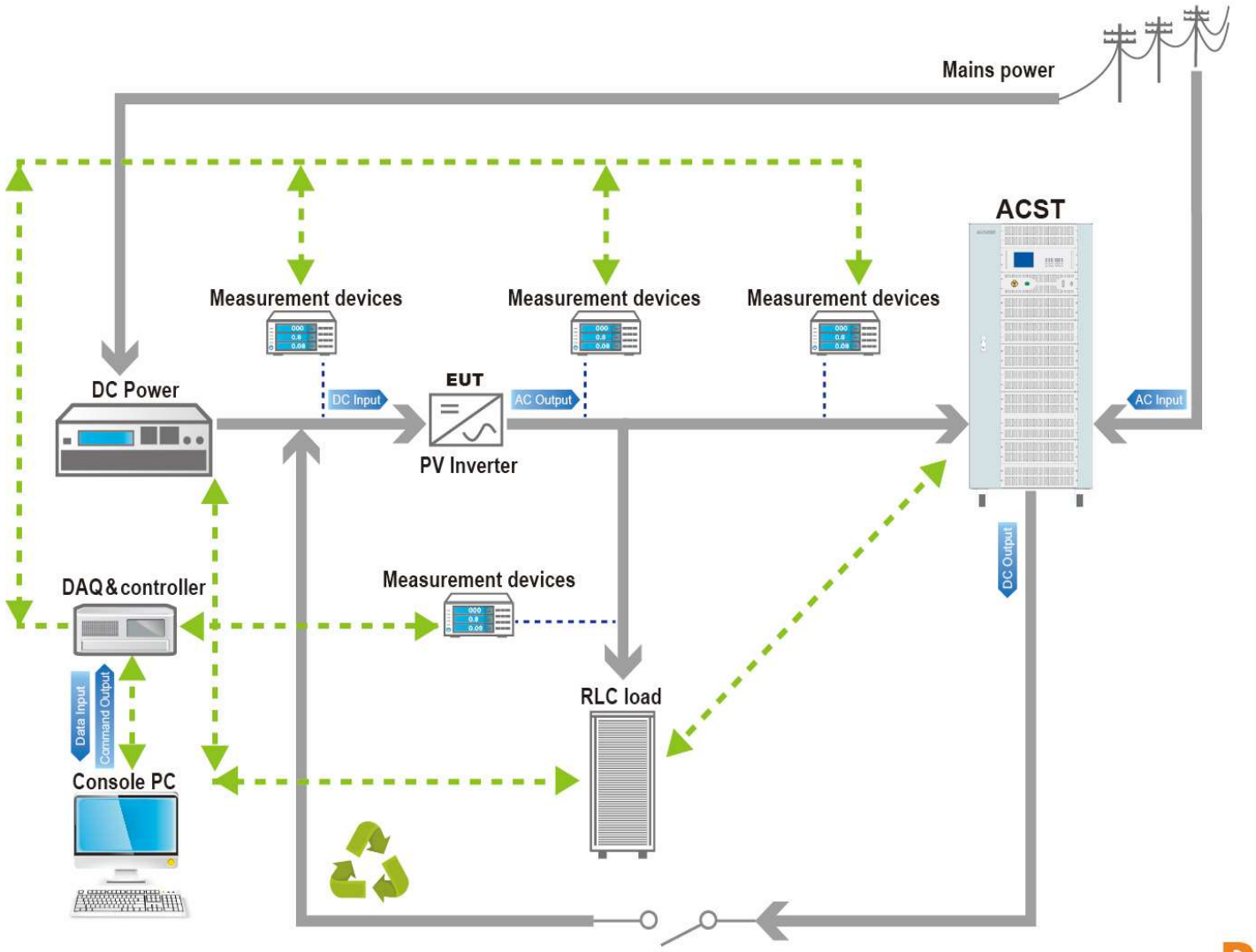
Test System Overview Block Diagram



PS:
All dotted green lines denote the communication channels, they could be RS-485, GPIB, Ethernet, USB or the direct data transfer via coaxial cable.

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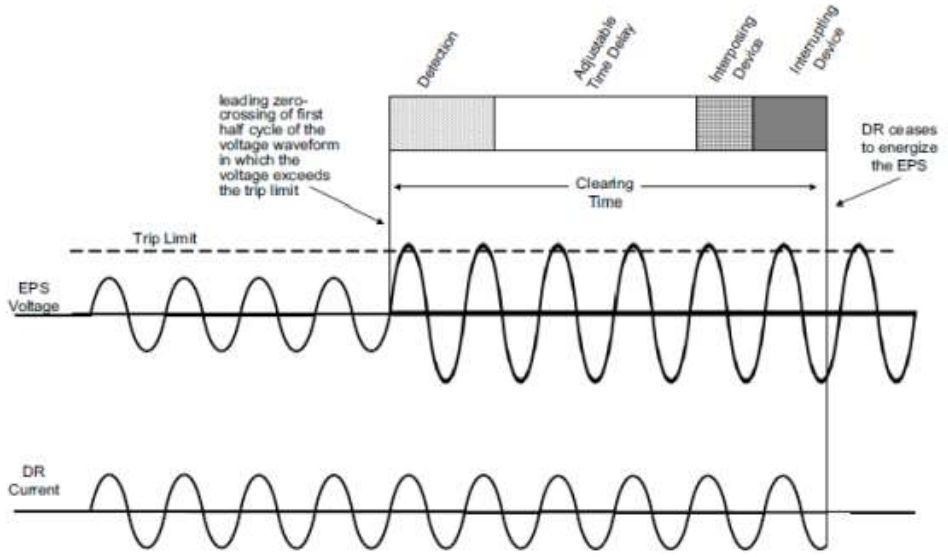
- IEEE 1547. 1 Test Standards

Abnormal Voltage Test(IEEE 1547.1-5.2)

- Testing under load shall be at both
  - Its minimum operating current and
  -At both unity power factor (p.f.) and the minimum DR p.f. (leading and lagging) as specified by the manufacturer at as close as possible to 100% full rated output current.

Voltage range (% of base voltage[a])	Clearing time(s)[b]
V< 50	0.16
50 ≤ V< 88	2.00
110 < V < 120	1.00
V ≥ 120	0.16



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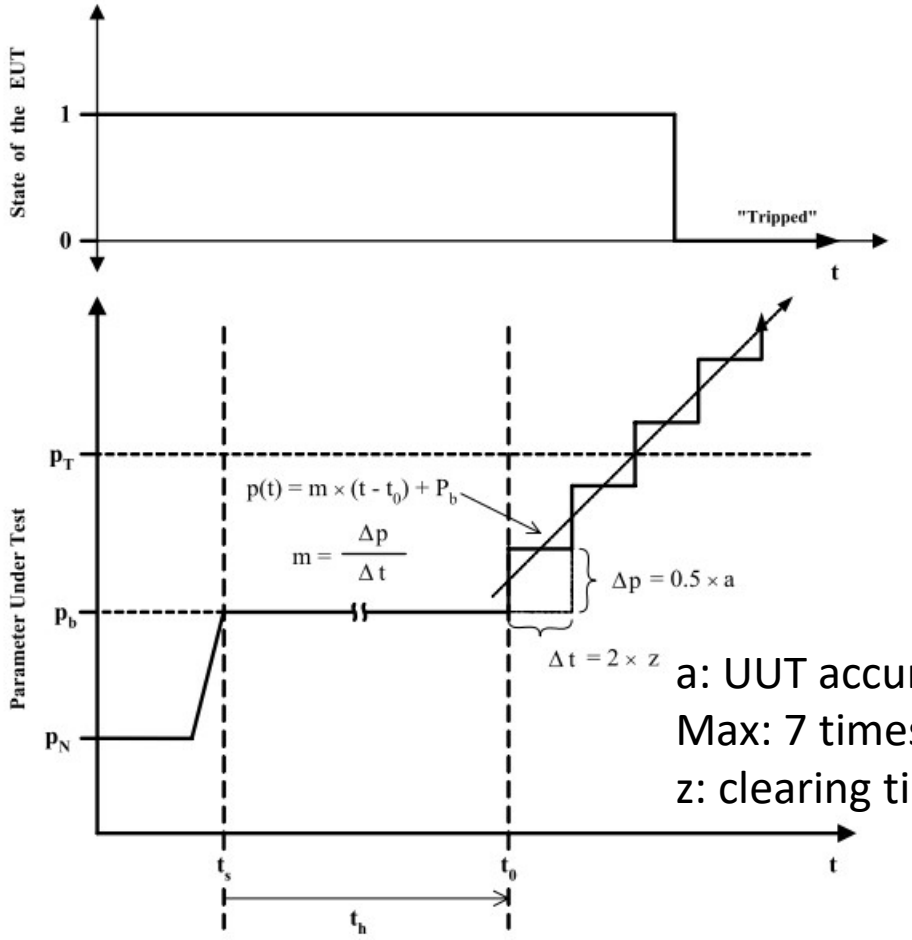
IEEE 1547.1-5.2 (Slow Voltage Test)

- OVER VOLTAGE – SLOW VOLTAGE TESTS
- UNDER VOLTAGE – SLOW VOLTAGE TESTS



a: UUT accuracy
Max: 7 times (will go into protection)
z: clearing time

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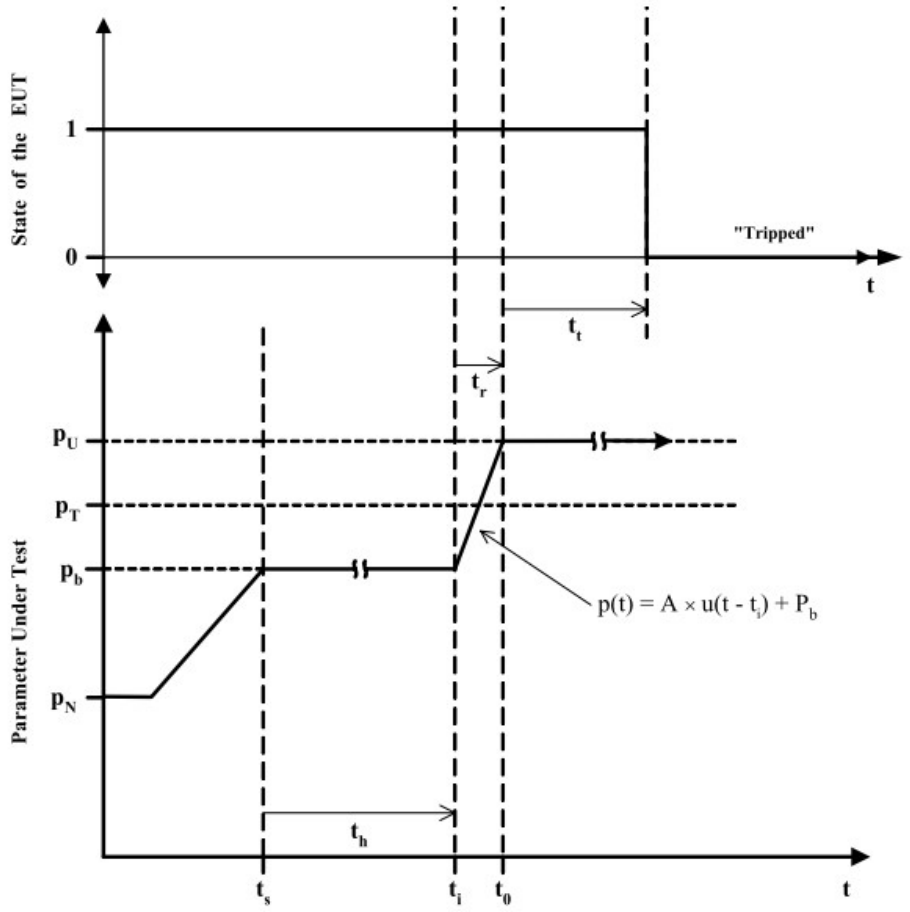
IEEE 1547.1-5.2 (Fast Voltage Tests)

- OVER VOLTAGE – FAST VOLTAGE TESTS
- UNDER VOLTAGE – FAST VOLTAGE TESTS



Rate voltage – 2a to:
120% 0.16sec

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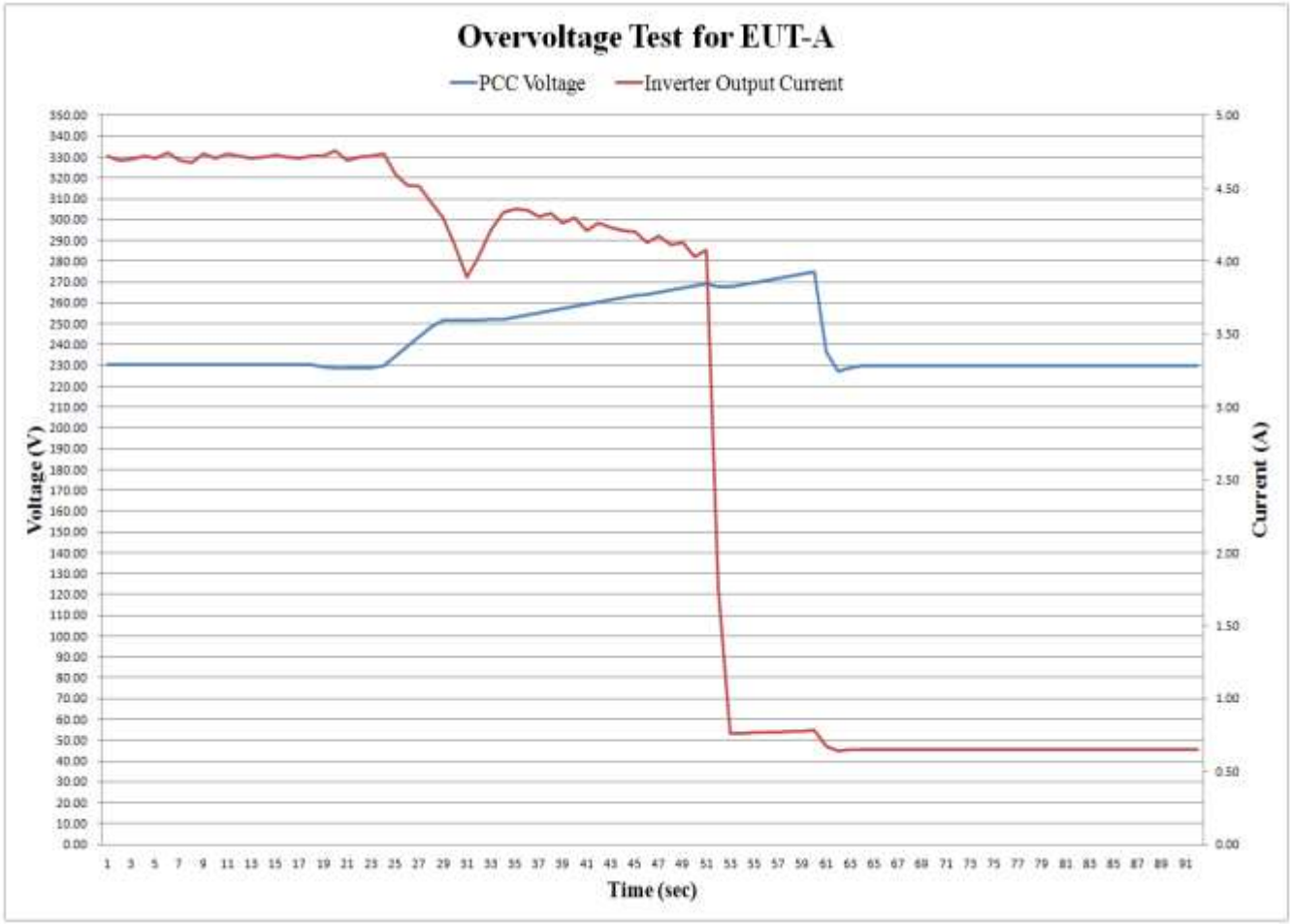
Example Test Result

Over voltage Test Result (Slow)



Nominal Voltage 240

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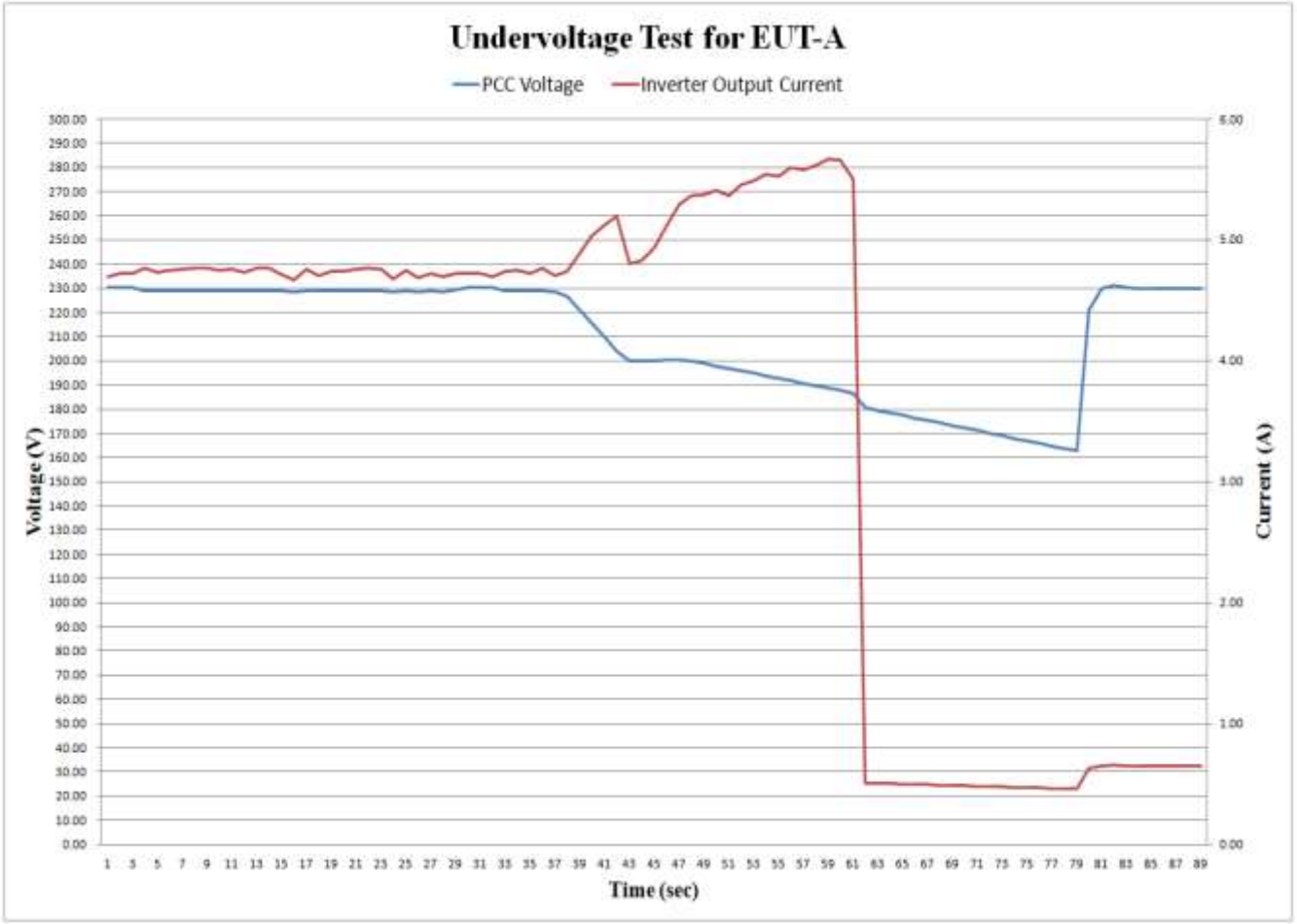
Under voltage Test Result (Slow)



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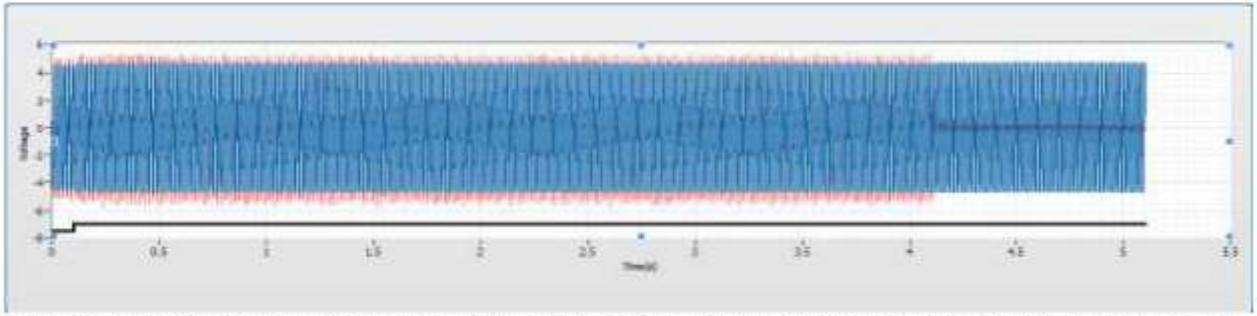
Slow Voltage Test Results Example- Overvoltage

Transients on one phase at a time				
Iteration (by phase)	Measured voltage			% variation of average from set point
	Phase A (V)	Phase B	Phase C	
1	257.9			
2	257.4			
3	257.5			
4	257.2			
5	257.4			
Phase A average	257.5	N/A	N/A	0.19%

Previously measured Voltage Trip Limits (Vrms)		A	B	C
		257.5V		
Iteration	Phase	Time to Disconnect (ms)		
1.	A	4021		
2.	A	3749		
3.	A	3984		
4.	A	2683		
5.	A	3848		

*** Red figures denote "not complied with the regulation requirements".



Notes for above figure: Blue: AC voltage, Red: Inverter output current, Black: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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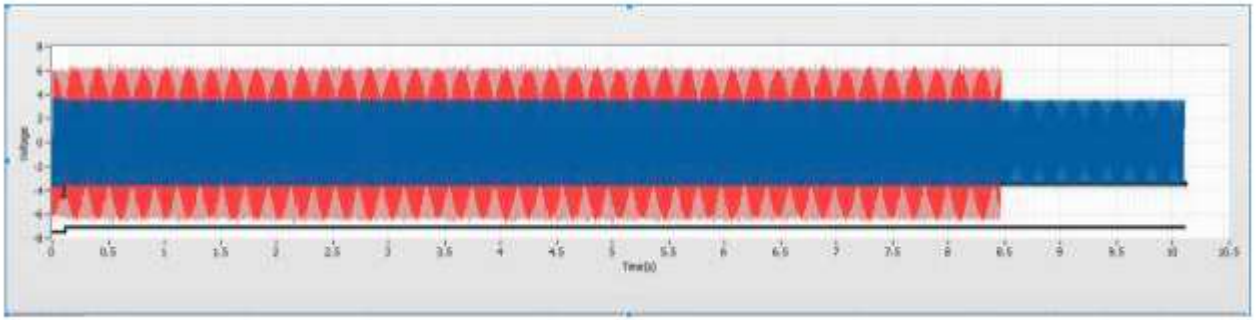
Slow Voltage Test Results Example- Undervoltage

Transients on one phase at a time				
ITERATION (by phase)	Measured voltage			% Variation of Average from set point
	Phase A	Phase B	Phase C	
1	206.7			
2	206.6			
3	206.6			
4	206.7			
5	206.7			
Phase A Average	206.7	N/A	N/A	2.1%

Previously measured voltage trip limits (vrms)		Phase a	Phase b	Phase c
		206.7 v		
Iteration	Phase	Time to disconnect (ms)		
1.	A	8473		
2.	A	4845		
3.	A	6578		
4.	A	6929		
5.	A	7490		

*** Red figures denote "not complied with the regulation requirements".



Notes for above figure: Blue: AC voltage, Red: Inverter output current, Black: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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Overvoltage fast trip limit magnitude verification tests

Table 1 limits Trips on Phase A Calculated Incremental Voltage		Overvoltage / Fast Trip Limit Voltage Magnitude Identification Test Measured Pre-Trip Voltage Phase A (V)	Phase B (V)	Phase C (V)	Measured Clearing Time (ms) (N/A if trip did not occur)
115% X Vnom =		276.9			633.5
116% X Vnom =		279.2			632.9
117% X Vnom =		281.7			629.6
118% X Vnom =		284.9			628.5
119% X Vnom =		286.7			552.7
120% X Vnom =		289.2			497.6
121% X Vnom =		292.0			273.4
122% X Vnom =		294.7			206.9
123% X Vnom =		297.3			352.2
124% X Vnom =		299.6			129.6
125% X Vnom =		301.7			132.8
126% X Vnom =		304.3			48.5
127% X Vnom =		306.7			116.0
128% X Vnom =		309.1			90.8
129% X Vnom =		310.6			82.3
130% X Vnom =		312.9			85.5

Overvoltage fast trip limit magnitude verification tests:
Fixed trip limits per IEEE 1547, table 1

IEEE 1547.1
Sec. 5.2.1.2

Previously Measured Trip limit Phase A:		299.6	V
Overvoltage / Fast Trip Limit Voltage Magnitude Verification/Confirmation Trials			
Iteration	Measured Pre-Trip Voltage (V)	Measured Clearing Time (ms)	
1	299.6	122.2	
2	299.7	117.5	
3	299.6	123.8	
4	299.8	152.6	
5	299.7	138.3	

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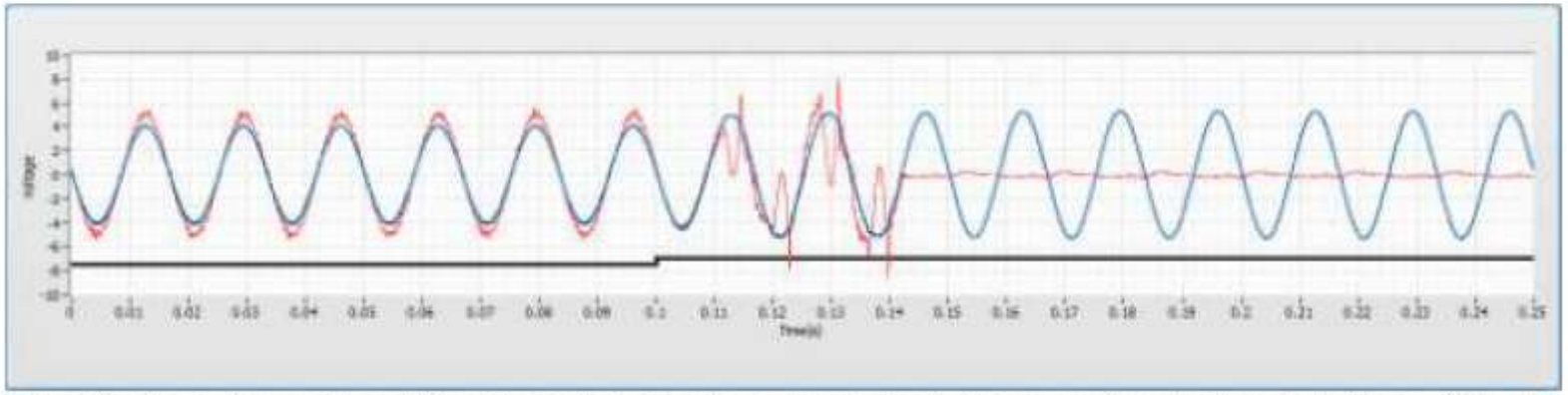
Overvoltage fast trip clearing time verification tests

Previously measured Voltage Trip Limits (Vrms)	A	B	C
	299.6V		

Iteration	Phase Selected For Test [A][B][C][L-L]	Time to Disconnect (ms)
1.	A	41.7
2.	A	47.7
3.	A	41.2
4.	A	40.2
5.	A	48.5



Notes for above figure: Blue: AC voltage, Red: Inverter output current, Black: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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Undervoltage fast trip limit magnitude verification tests

Table 1 limits Trips on Phase A CALCULATED INCREMENTAL VOLTAGE		Undervoltage / Fast Trip Limit Voltage Magnitude Identification Test Measured Pre-Trip Voltage Phase A (V)	Phase B (V)	Phase C (V)	Measured Clearing Time (ms) (N/A if trip did not occur)
60% X Vnom =		142.9			37.3
59% X Vnom =		140.4			37.4
58% X Vnom =		138.8			36.8
57% X Vnom =		136.6			36.6
56% X Vnom =		134.1			36.6
55% X Vnom =		131.7			35.7
54% X Vnom =		129.5			37.3
53% X Vnom =		127.1			37.4
52% X Vnom =		124.6			34.4
51% X Vnom =		122.5			34.8
50% X Vnom =		120.5			36.2
49% X Vnom =		117.2			36.6
48% X Vnom =		115.7			35.7
47% X Vnom =		112.7			37.3
46% X Vnom =		110.6			33.5
45% X Vnom =		108.3			36.5

Undervoltage fast trip limit magnitude verification tests : IEEE 1547.1
Fixed trip limits per IEEE 1547, table 1 Sec. 5.2.2.2

Previously Measured Trip limit Phase A:		142.9 V
Undervoltage / Fast Trip Limit Voltage Magnitude Verification/Confirmation Trials		
Iteration	Measured Pre-Trip Voltage (V)	Measured Clearing Time (ms)
1	142.9	38.1
2	142.8	38.2
3	142.8	38.7
4	142.7	37.9
5	142.8	37.6

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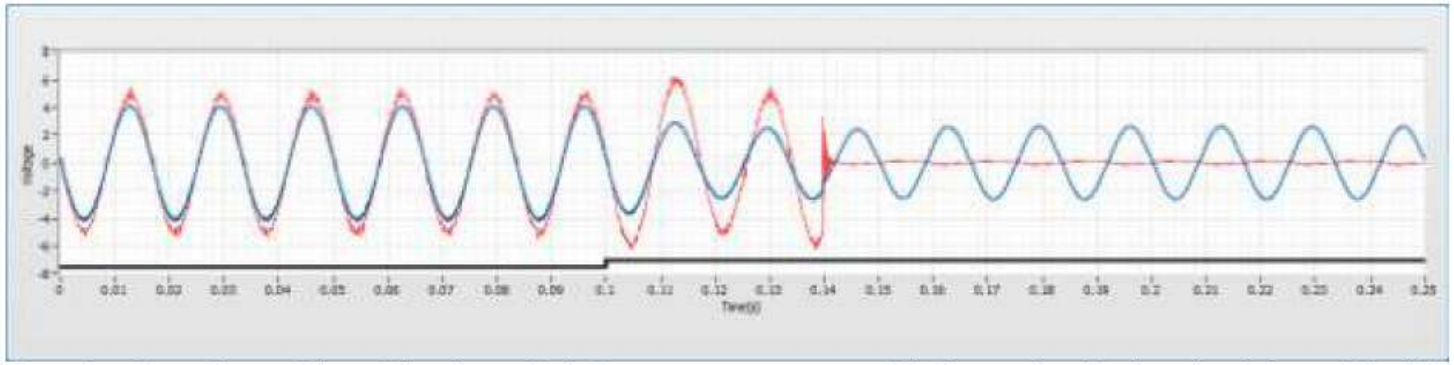
Undervoltage fast trip clearing time verification tests

Previously measured Voltage Trip Limits (Vrms)	A	B	C
	142.9 V		

Iteration	Phase Selected For Test [A][B][C][L-L]	Time to Disconnect (ms)
1.	A	38.1
2.	A	37.7
3.	A	38.5
4.	A	38.8
5.	A	37.9



Notes for above figure: Blue: AC voltage, Red: Inverter output current, Black: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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Response to abnormal frequency conditions(IEEE 1547.1-5.3)

DR size	Frequency range (Hz)	Clearing time(s)[a]
≤ 30 kW	> 60.5	0.16
	< 59.3	0.16
> 30 kW	> 60.5	0.16
	< (59.8 – 57.0) (adjustable set point)	Adjustable 0.16 to 300
	< 57.0	0.16

[a]DR ≤ 30 kW, maximum clearing times; DR > 30 kW, default clearing times.

Ex: 61Hz accuracy: 0.1Hz

1. 60.8Hz (+2a)
2. 61.2 (+4a)

……. Until trip

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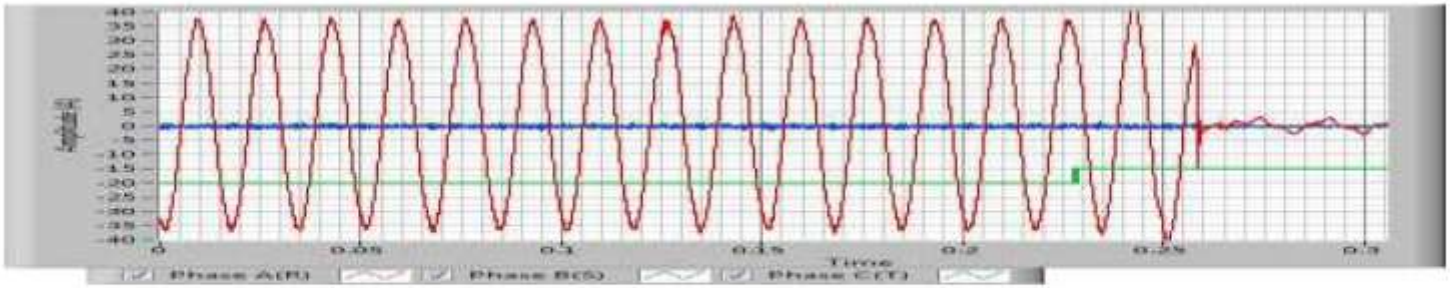
Overfrequency trip clearing time verification tests

Previously measured Frequency Trip Limit (Hz)	60.71
Iteration / Hz	Measured clearing time (ms)
(1) 60.71	26
(2) 60.71	29
(3) 60.71	29
(4) 60.71	27
(5) 60.71	28



Notes for above figure: Red: Inverter output current, Green: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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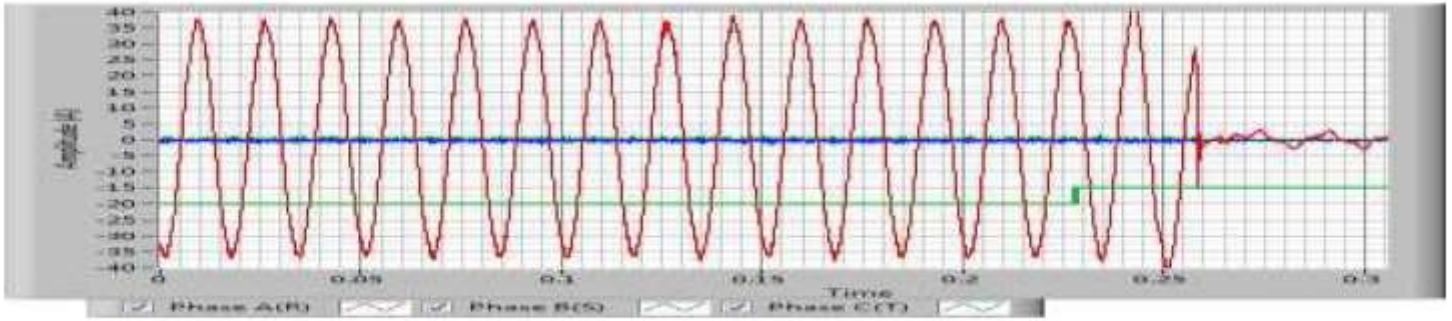
Underfrequency trip clearing time verification tests

Previously measured Frequency Trip Limit (Hz)	59.30
Iteration / Hz	Measured clearing time (ms)
(1) 59.30	29
(2) 59.30	29
(3) 59.30	28
(4) 59.30	30
(5) 59.30	28



Notes for above figure: Red: Inverter output current, Green: synchronization signal from AC grid simulator. (synchronization signal toggles when AC source changes state).

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Synchronization Test (IEEE 1547.1-5.4)

- Synchronization parameter limits for synchronous interconnection to an EPS or an energized local EPS to an energized Area EPS

Aggregate rating of DR units (kVA)	Frequency difference (Δf, Hz)	Voltage difference (ΔV, %)	Phase angle difference (ΔΦ, °)
0 – 500	0.3	10	20
> 500 – 1 500	0.2	5	15
> 1 500 – 10 000	0.1	3	10

Test under Full load,
Measure max. current when PV Inverter connect to grid
(for protect the equipment damaging from inrush current)

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Synchronization Test Result – Voltage Variation

Test iteration	Startup current (maximum RMS value recorded during the Startup period) (Amps)			Input Startup Voltage
----	Phase A	Phase B	Phase C	(Vrms)
1	20.997			239.8
2	20.971			240.0
3	20.980			240.1
4	20.971			240.1
5	20.989			239.9
6	20.980			240.0
7	20.954			239.9
8	20.962			240.1
9	20.954			240.0
10	20.962			240.0

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DC Injection Test (IEEE 1547.1-5.6)

- LIMITATION OF DC INJECTION FOR INVERTERS WITHOUT INTERCONNECTION TRANSFORMERS)

100 % output power

	Limit (%)	Limit (mA) (calculated)	Measured Values		
			Phase A (mA)	Phase B	Phase C
DC injection	0.5% of (EUT) I_{nom}	5.31	3.54		

66 % output power

	Limit (%)	Limit (mA) (calculated)	Measured Values		
			Phase A (mA)	Phase B	Phase C
DC injection	0.5% of (EUT) I_{nom}	5.31	1.46		

33 % output power

	Limit (%)	Limit (mA) (calculated)	Measured Values		
			Phase A (mA)	Phase B	Phase C
DC injection	0.5% of (EUT) I_{nom}	5.31	1.23		

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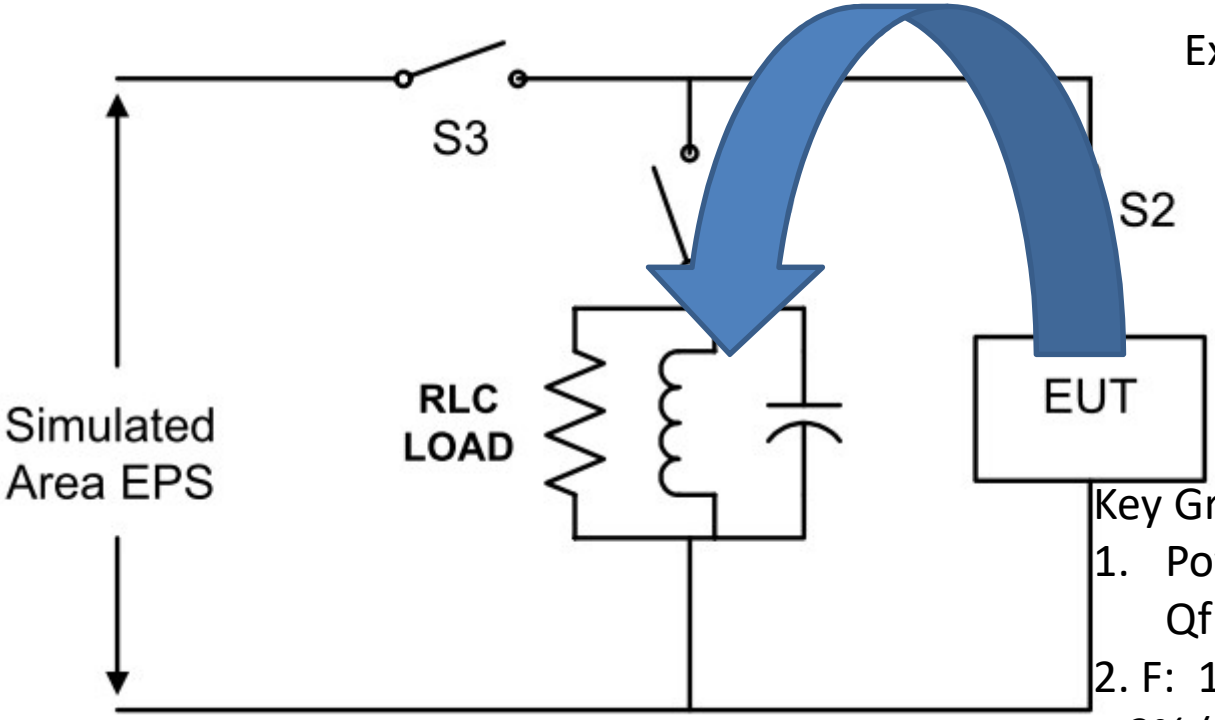
Anti-Islanding Test (IEEE 1547.1-5.7)

- Unintentional islanding test:
- The purpose of this test is to verify that the DR interconnection component or system ceases to energize the area EPS as specified in IEEE Std 1547 when an unintentional island condition is present. This test determines the trip time for the test conditions specified in 5.7.1. **(Response to Anti-Islanding protection within 2 sec)**



Ex: Frequency disturbance method

Key Grid Simulator Indicators:

1. Power: ~ 0W (ex: +/- 10W) (Adjust R)
   Qf of 1.0 ± 0.05
2. F: 1st harmonic current must adjust < 2% (Rated current) (Adjust L,C)

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UNINTENTIONAL ISLANDING TEST OF EUT POWER OF 100% - part1

100% of rated Load	Actual Balanced Load Condition – Measured (for Phase A)
	Phase A
Utility voltage (Vac)	239.8
Total Real Power (Watts)	5024
Total Reactive Power – capacitive (Vars)	5287 (*)
Total Reactive Power – inductive (Vars)	5013
Capacitive Tank Current(A)	22.048
Inductive Tank Current(A)	20.907
Resistive Tank Current(A)	20.645

(*): This value is significantly larger than the real and inductive power due to a bulky isolation transformer connected in between the EUT and the test point.

Test equipment Operating Status during test:		
Input Supply Operating Voltage	389	~~[Vac]~~[Vdc]
Grid Voltage	239.8	Vac
Grid Frequency	60.00	Hz
Inverter Power	5015	W
Q Value Verified: Must be 1.0 +/- 0.05	1.025	----

Preen

UNINTENTIONAL ISLANDING TEST OF EUT POWER OF 100% - part2

Percent of balanced LC load		Measured inverter output current to grid before opening S3 (A)			Clearing Time	Resonant Frequency of RLC load (+)
Percent	Iteration	Phase A	~~Phase B~~	~~Phase C~~	**ms**	**Hz**
90 %	1	20.988			113	61.48
	2	20.968			89	61.47
	3	21.047			92	61.43
91 %	1	21.107			172	61.37
	2	21.008			94	61.39
	3	20.968			156	61.38
92 %	1	21.026			91	61.26
	2	21.086			125	61.26
	3	21.067			107	61.25
93 %	1	21.120			79	61.15
	2	21.106			123	61.12
	3	21.067			99	61.14
94 %	1	20.869			97	60.98
	2	20.968			115	60.99
	3	21.047			83	61.06

⋮

To 110%

Adjust to 100% balance (record R, L, C)

L Value: 100%->90% (trip faster),

100%->110% (trip faster),

Test 3 times to ensure the result

Preen

UNINTENTIONAL ISLANDING TEST OF EUT POWER OF 60% and 33%

Repeat Test for following conditions

- UNINTENTIONAL ISLANDING TEST OF EUT POWER OF 60%
- UNINTENTIONAL ISLANDING TEST OF EUT POWER OF 33%

Preen

Open Phase Test (IEEE 1547.1-5.9)

- The purpose of this test is to verify that the ICS ceases to energize the area EPS upon loss of an individual phase at the PCC or at the point of DR connection.
- Open one phase conductor disconnect while the EUT is operating at the greater of
  — 5% of rated output current or
  — The EUT’ s minimum output current.

Phase tested	Operating current (A)	Clearing Time (ms)	Comments
A	1.525	67	
A	1.520	61	
A	1.530	65	
A	1.510	64	
A	1.490	54	

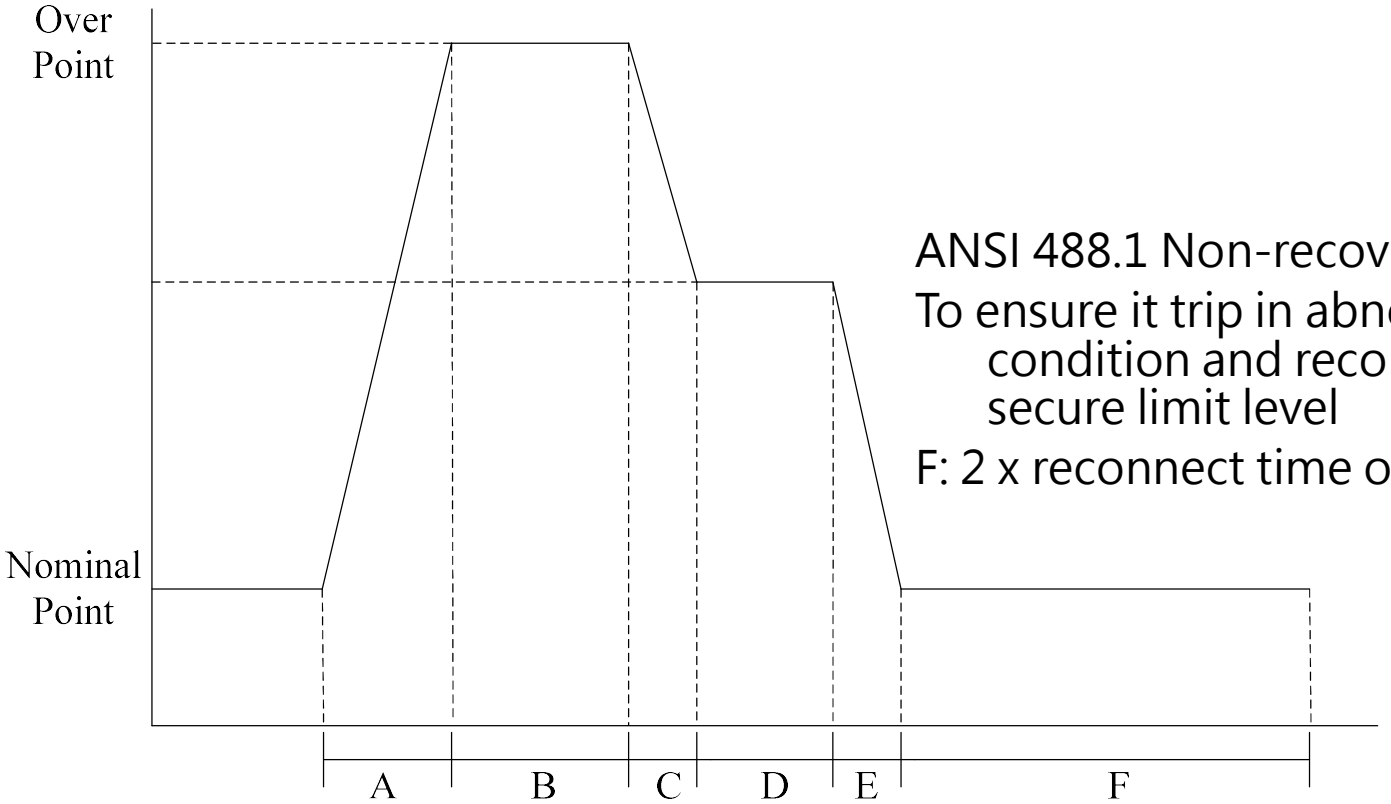
Check if will trip or not

Preen

Reconnect Test (IEEE 1547.1-5.10)

The purpose of this test is to verify the functionality of the DR interconnection component or system reconnect timer, which delays the DR reconnection to the area EPS following a trip event.

- **Method A**



ANSI 488.1 Non-recovery level

To ensure it trip in abnormal condition and reconnect in secure limit level

F: 2 x reconnect time of EUT spec

Preen

Reconnect Test – Method A

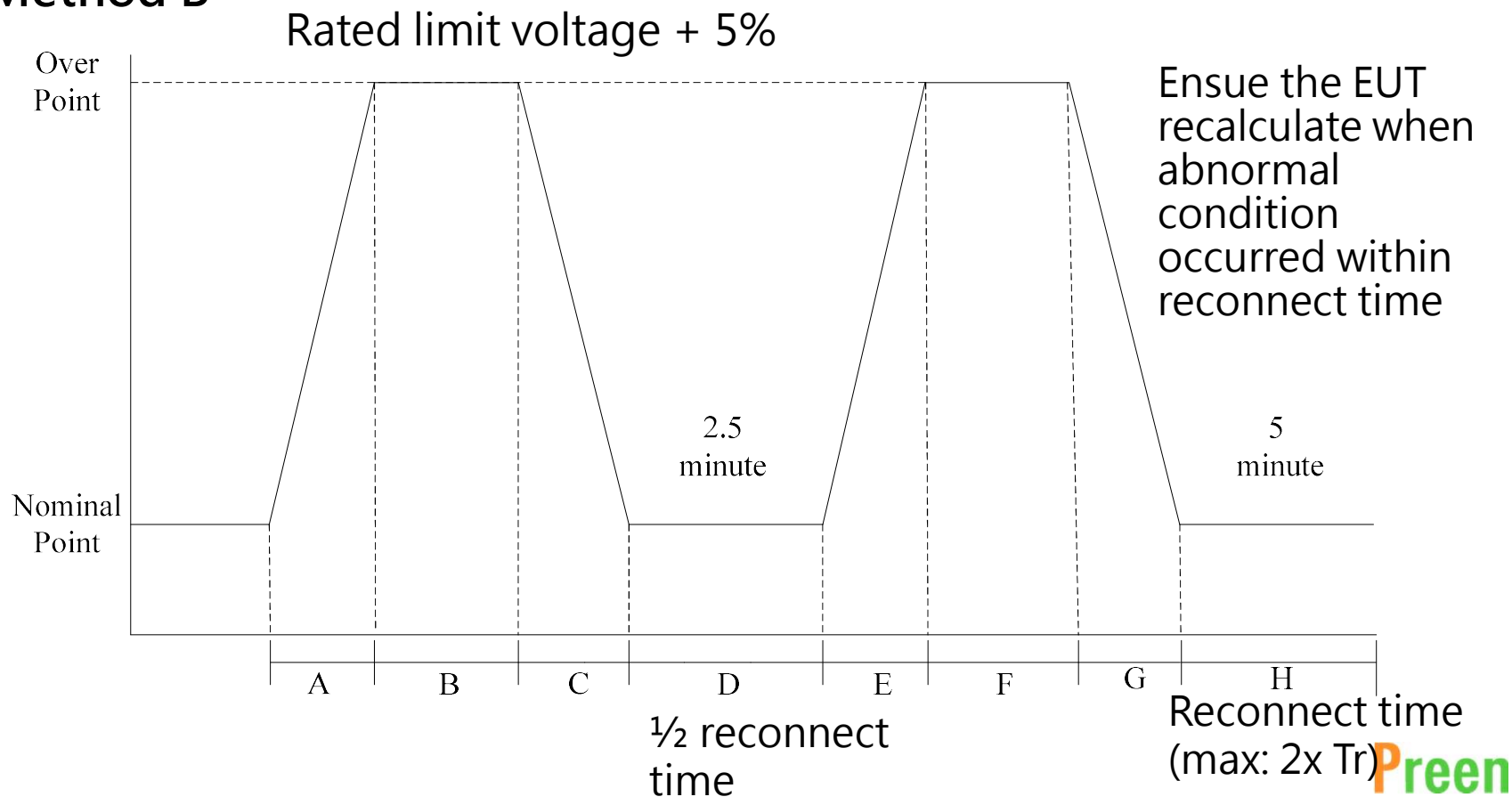
Method A: results - 5 minute timer - **trip level hysteresis.**				
Programmed Re-connect time:				30 s (*)
Output Voltage (V)				240 V
Output Current (A)				21.02A
STEP	TRANSIENT DESCRIPTION	MEASURED TRANSIENT MAGNITUDE (V/Hz)	MEASURED HOLDING TIME (S)	MEASURED RECONNECT TIME (S)
1	Overvoltage (105%)	276.4	2	
2	Overvoltage (Calculated Overvoltage Reconnection Magnitude)	256.2	60	29.6
3	Return to Nominal	240.0	60	= 0
4	Undervoltage (95%)	199.2	4	
5	Undervoltage (Calculated Undervoltage Reconnection Magnitude)	210.0	60	29.8
6	Return to Nominal	240.0	60	= 0
7	Overfrequency (105%)	63.74	0.32	
8	Overfrequency (Calculated Overfrequency Reconnection Magnitude)	60.70	60	> 60
9	Return to Nominal	60.00	60	29.8
10	Underfrequency (95%)	56.33	0.32	
11	Underfrequency (Calculated Underfrequency Reconnection Magnitude)	59.10	60	> 60
12	Return to Nominal	60.00	60	29.7

Preen

Reconnect Test (IEEE 1547.1-5.10)

The purpose of this test is to verify the functionality of the DR interconnection component or system reconnect timer, which delays the DR reconnection to the area EPS following a trip event.

- **Method B**



Preen

Reconnect Test – Method B

Method B: results - **5 minute timer reset function.**				
Programmed Re-connect time:				30 s
Output Voltage (V)				240 V
Output Current (A)				21.02 A
STEP	TRANSIENT DESCRIPTION	MEASURED TRANSIENT MAGNITUDE (V/Hz)	MEASURED HOLDING TIME (S)	MEASURED RECONNECT TIME (S)
1	Overvoltage (105%)	276.4	2	
2	Return to Nominal (for a maximum of 1/2 of the reconnect time setting)	239.9	15	> 15
3	Overvoltage (105%)	276.3	2	
4	Return to Nominal	239.9	60	29.9
5	Undervoltage (95%)	199.2	4	
6	Return to Nominal (for a maximum of 1/2 of the reconnect time setting)	240.0	15	> 15
7	Undervoltage (95%)	199.2	4	
8	Return to Nominal	240.0	60	29.8
9	Overfrequency (105%)	63.74	0.32	
10	Return to Nominal (for a maximum of 1/2 of the reconnect time setting)	60.00	15	> 15
11	Overfrequency (105%)	63.74	0.32	
12	Return to Nominal	60.00	60	29.8
13	Underfrequency (95%)	56.33	0.32	
14	Return to Nominal (for a maximum of 1/2 of the reconnect time setting)	60.00	15	> 15
15	Underfrequency (95%)	56.33	0.32	
16	Return to Nominal	60.00	60	29.9

Preen

Harmonics Test (IEEE 1547.1-5.11)

- The purpose of this test is to measure the individual current harmonics and total rated-current distortion (TRD) of the DR interconnection component or system under normal operating conditions. The results shall comply with the requirements of IEEE Std 1547. Self-excited induction generators shall be tested using the procedure for synchronous generators.

Individual harmonic order h (odd harmonics)[b]	h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h	Total demand distortion (TDD)
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

Maximum harmonic current distortion in percent of current

Preen

Odd Oder Harmonics

Harmonic order	Limit (%)	Limit (+) (A)	Measured Values - **Odd order** Harmonics (A) for different load levels		
			33%	66%	100%
I-THD	NA	NA	4.23%	1.76%	1.31%
I-TDD	5%	NA	1.40%	1.17%	1.31%
1	100%	21.363	7.083	14.215	21.361
3	4%	0.854	0.183	0.081	0.107
5	4%	0.854	0.105	0.082	0.047
7	4%	0.854	0.106	0.100	0.062
9	4%	0.854	0.028	0.033	0.027
11	2%	0.427	0.029	0.017	0.017
13	2%	0.427	0.011	0.015	0.013
15	2%	0.427	0.007	0.012	0.005
17	1.5%	0.320	0.010	0.005	0.009
19	1.5%	0.320	0.005	0.006	0.003
21	1.5%	0.320	0.005	0.005	0.003
23	0.6%	0.128	0.006	0.005	0.003
25	0.6%	0.128	0.005	0.006	0.002
27	0.6%	0.128	0.003	0.006	0.002
29	0.6%	0.128	0.008	0.006	0.003
31	0.6%	0.128	0.010	0.006	0.002
33	0.6%	0.128	0.005	0.008	0.003
35	0.3%	0.064	0.009	0.007	0.005
37	0.3%	0.064	0.011	0.010	0.006
39	0.3%	0.064	0.009	0.016	0.010

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Even Oder Harmonics

Harmonic order	Limit (%)	Limit (A) (+)	Measured Values - **Even order** Harmonics (A) for different load levels		
			33%	66%	100%
2	1%	0.214	0.113	0.099	0.123
4	1%	0.214	0.105	0.127	0.194
6	1%	0.214	0.054	0.060	0.066
8	1%	0.214	0.013	0.024	0.043
10	1%	0.214	0.016	0.014	0.022
12	0.5%	0.107	0.007	0.015	0.009
14	0.5%	0.107	0.008	0.008	0.009
16	0.5%	0.107	0.007	0.005	0.008
18	0.375%	0.080	0.005	0.003	0.005
20	0.375%	0.080	0.006	0.005	0.005
22	0.375%	0.080	0.005	0.005	0.002
24	0.15%	0.032	0.005	0.006	0.002
26	0.15%	0.032	0.005	0.004	0.002
28	0.15%	0.032	0.006	0.007	0.002
30	0.15%	0.032	0.006	0.003	0.002
32	0.15%	0.032	0.005	0.009	0.003
34	0.15%	0.032	0.008	0.006	0.003
36	0.075%	0.016	0.015	0.009	0.003
38	0.075%	0.016	0.009	0.012	0.004
40	0.075%	0.016	0.012	0.013	0.006

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Low Voltage Ride Through Test (>50kW)

- It is becoming increasingly evident that large-scale penetration of distributed resources (DR) that have sensitive voltage and frequency trip points with short delay times, as mandated by the current version of IEEE Standard 1547, pose a risk to bulk power system security. This issue is well described in the NERC Integration of Variable Generation Task Force Task 1-7 report.

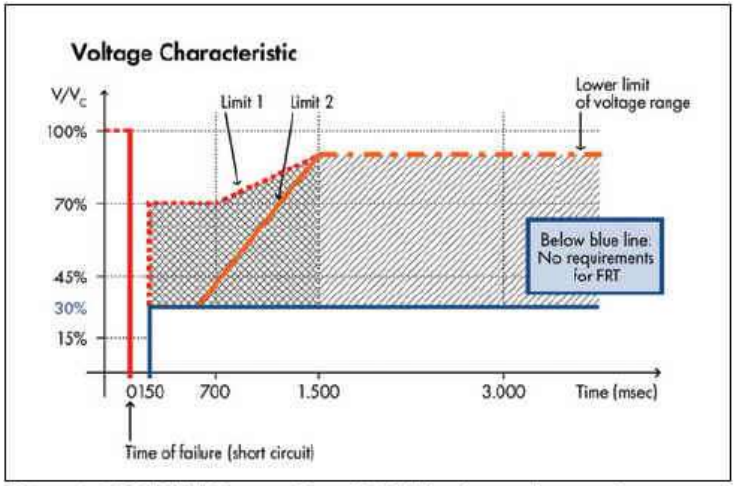

Figure 4. BDEW LVRT curve. From 'BDEW' tech. requirements for generating units on the medium voltage grid-June 2008 (Source: SMA America)

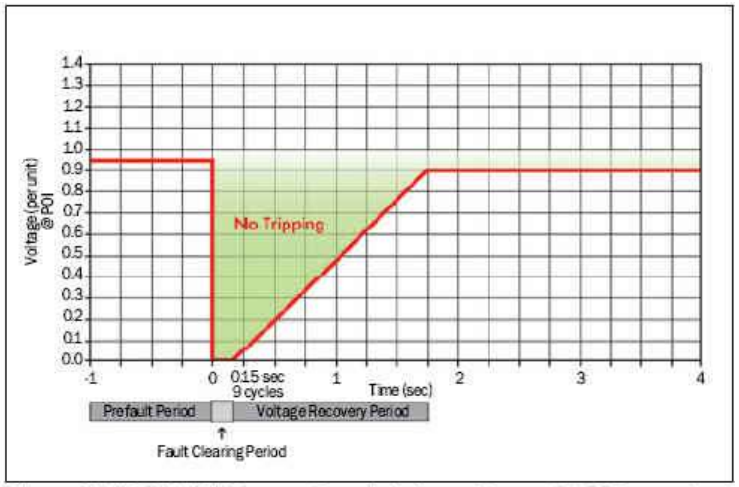

Figure 5. ERCOT LVRT curve for wind plants. From ERCOT operating guide (Source: ERCOT)

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Challenges for equipment manufactures

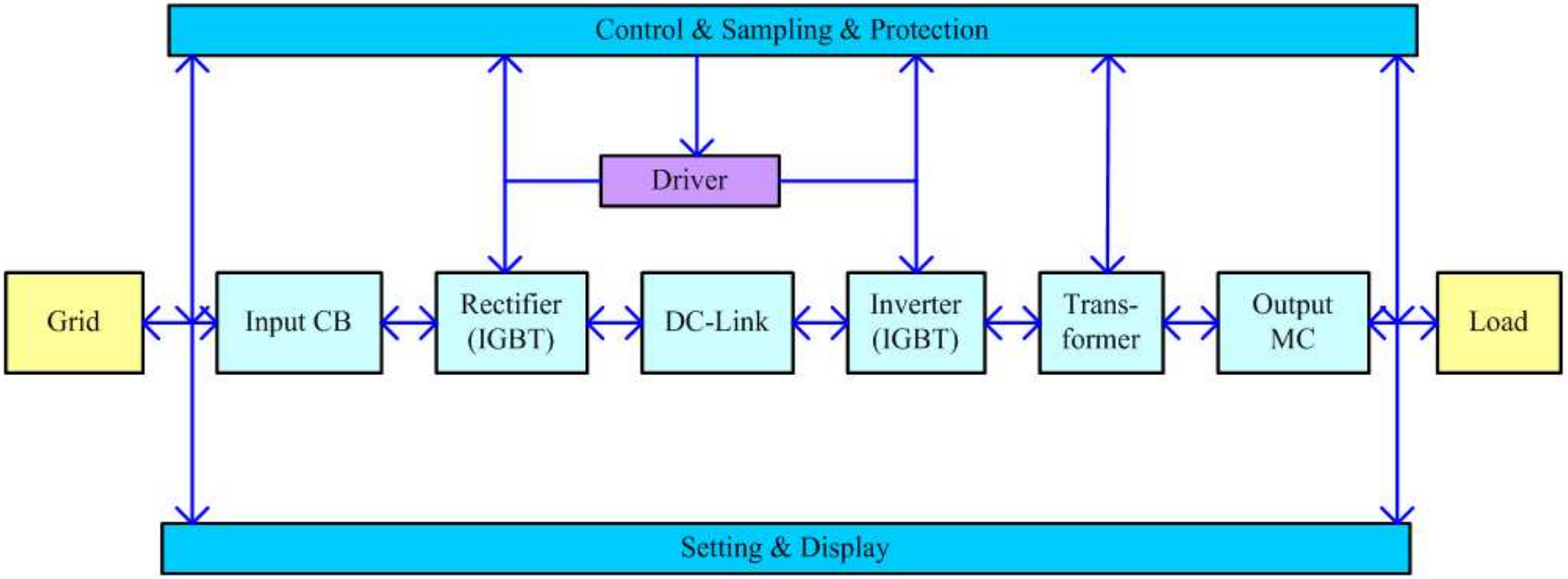
- Challenges:
  - How to make a AC source with high capacity and robust
  - How to make it as a regenerative type to the grid system and sink the current from PV Inverter (reactive power)
  - How to drop the voltage to the desire point ~0V (or <5% of rated voltage)

PAS Series (Regenerative Grid Simulator)

PAS-F Series is a programmable bi-directional AC grid simulator for testing grid-tied PV Inverters up to 2MVA. The power source includes embedded setup for Low Voltage Ride Through Test (LVRT) and supports RS232, RS485, USB, GPIB or LAN communication interfaces.

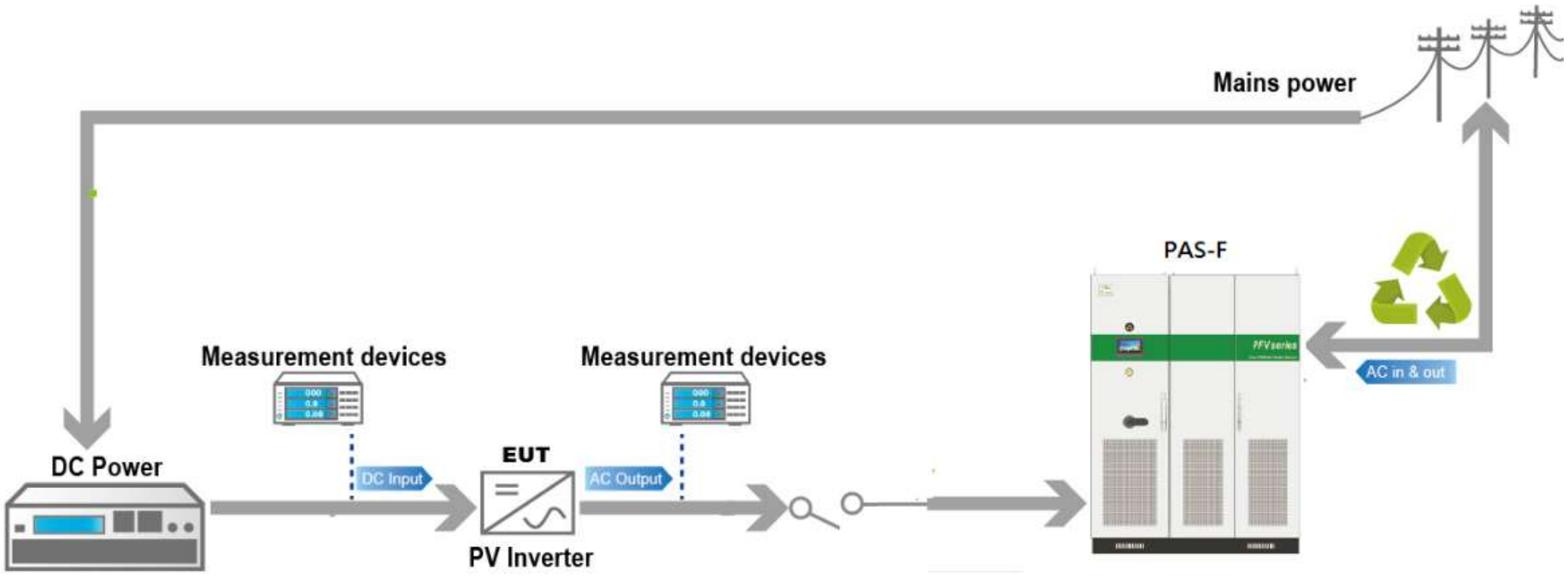
PAS Series Grid Simulator (IGBT Based)	
Capacity	60~2000kVA
Input Phase	3Phase
Input Voltage	277V/480V+/-15%
Output Voltage	0V~300Vac (L-N)
Output Frequency	45~65Hz
Input Power Factor	0.99
Regulation	<0.5%
Efficiency	>92%
Frequency Stability	<0.01%
THD	<1%
Unbalance Load	100% Unbalance Load
Adjustable Voltage Resolution	0.1V
Adjustable Frequency Resolution	0.01Hz

Working Principle of Regenerative Grid Simulator (4 quadrant)



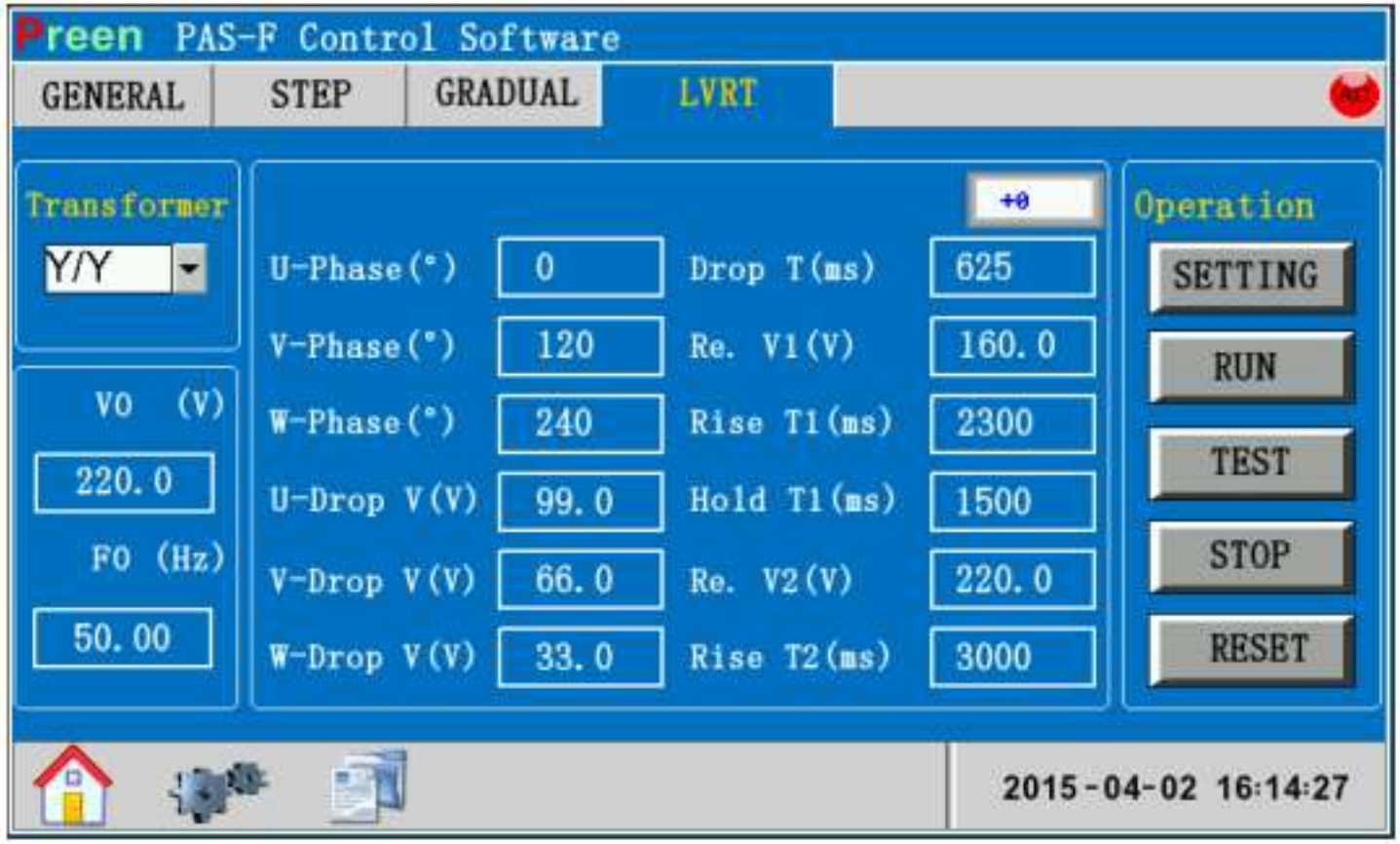
Preen

Method 2: By Regenerative Type Grid Simulator



Preen

Build-in LVRT Test Graph



Product Outlooking

AFV 2000kVA

PAS 1600kVA

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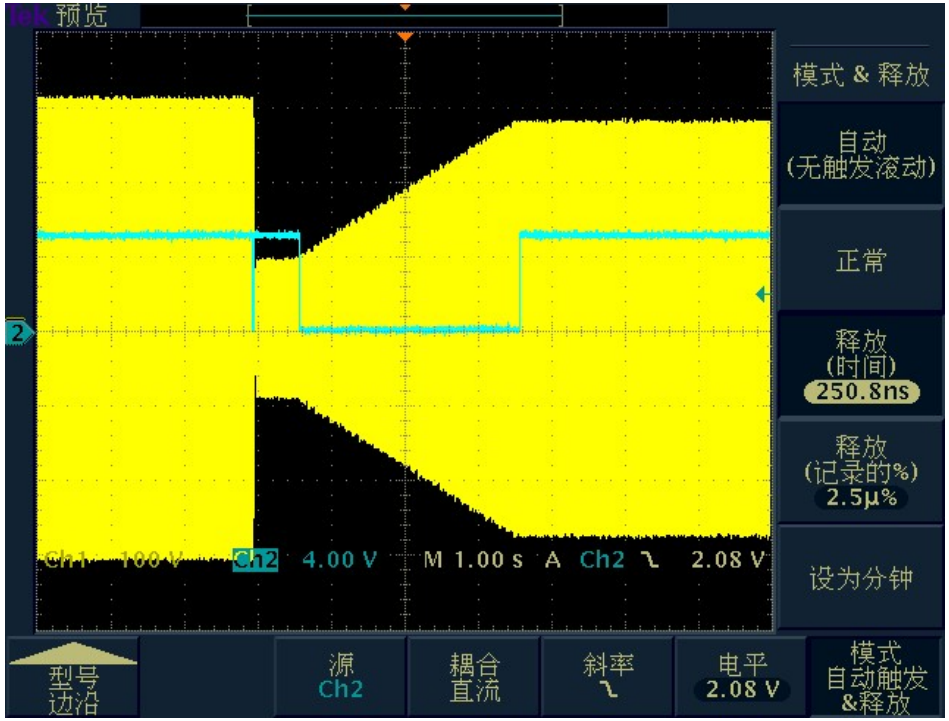
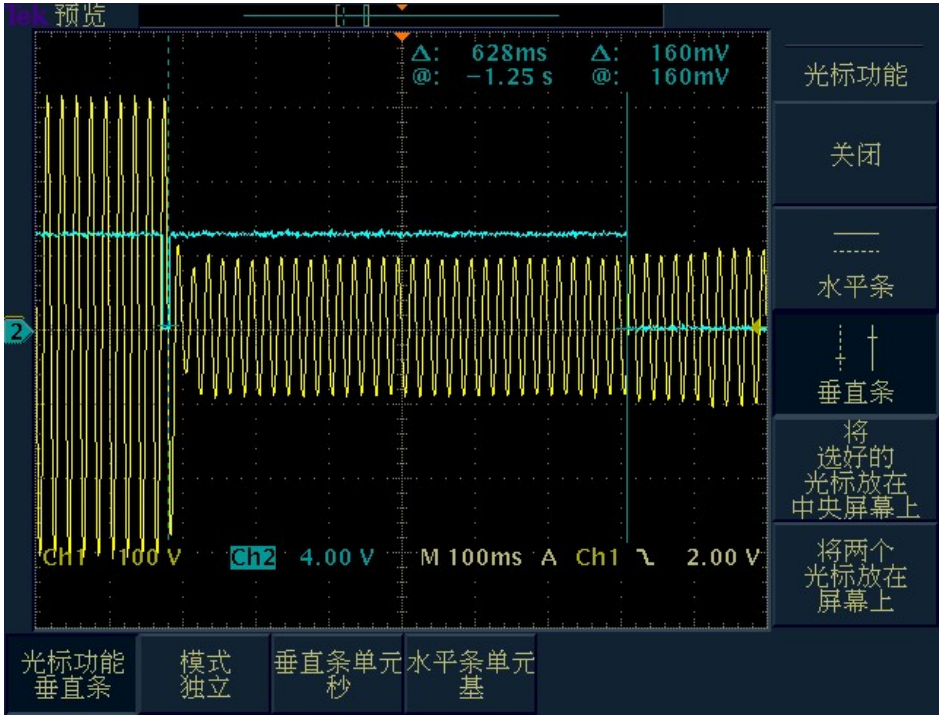
LVRT Tests (1)



LVRT Test



Voltage Drop Point

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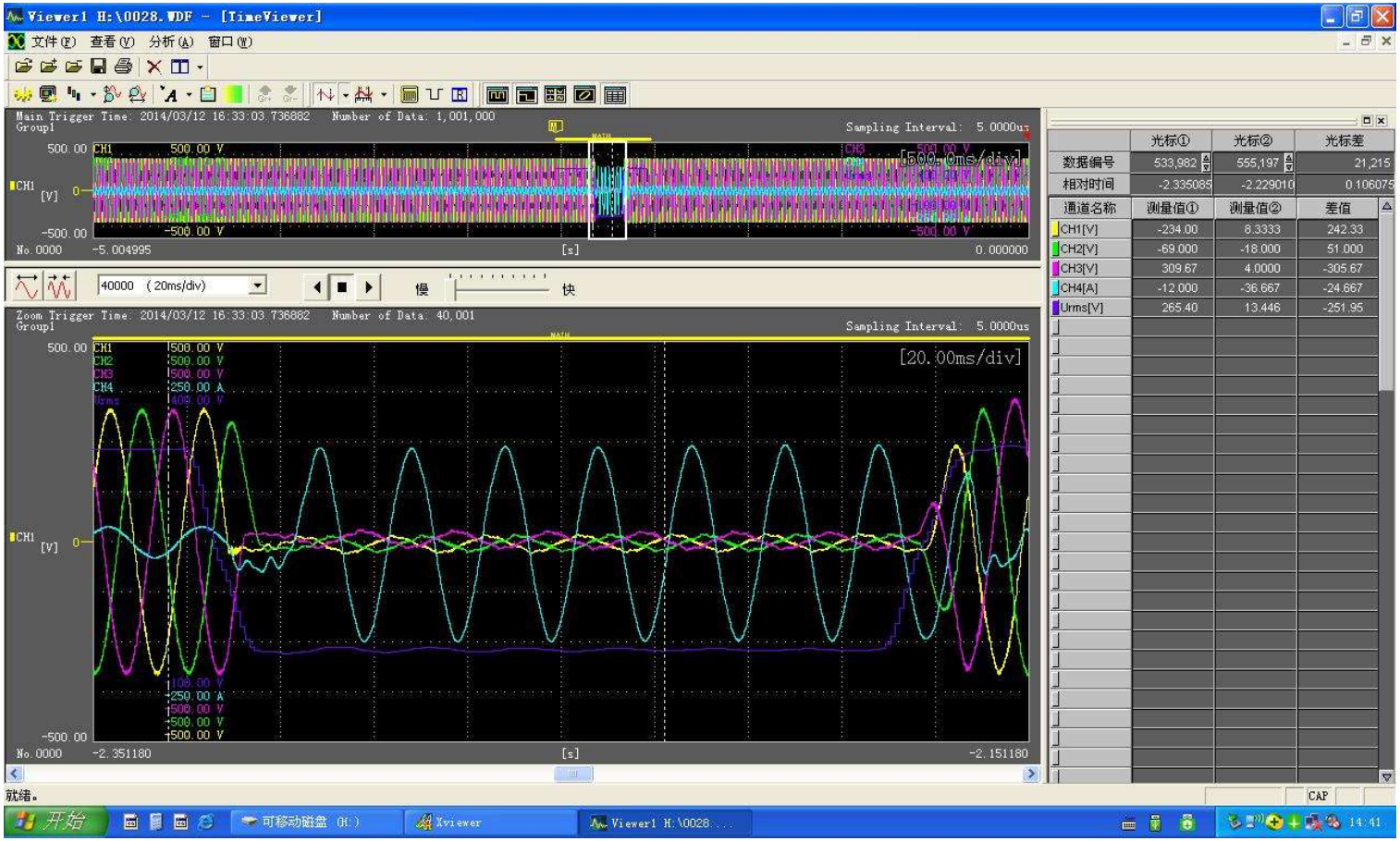
LVRT Tests (2)



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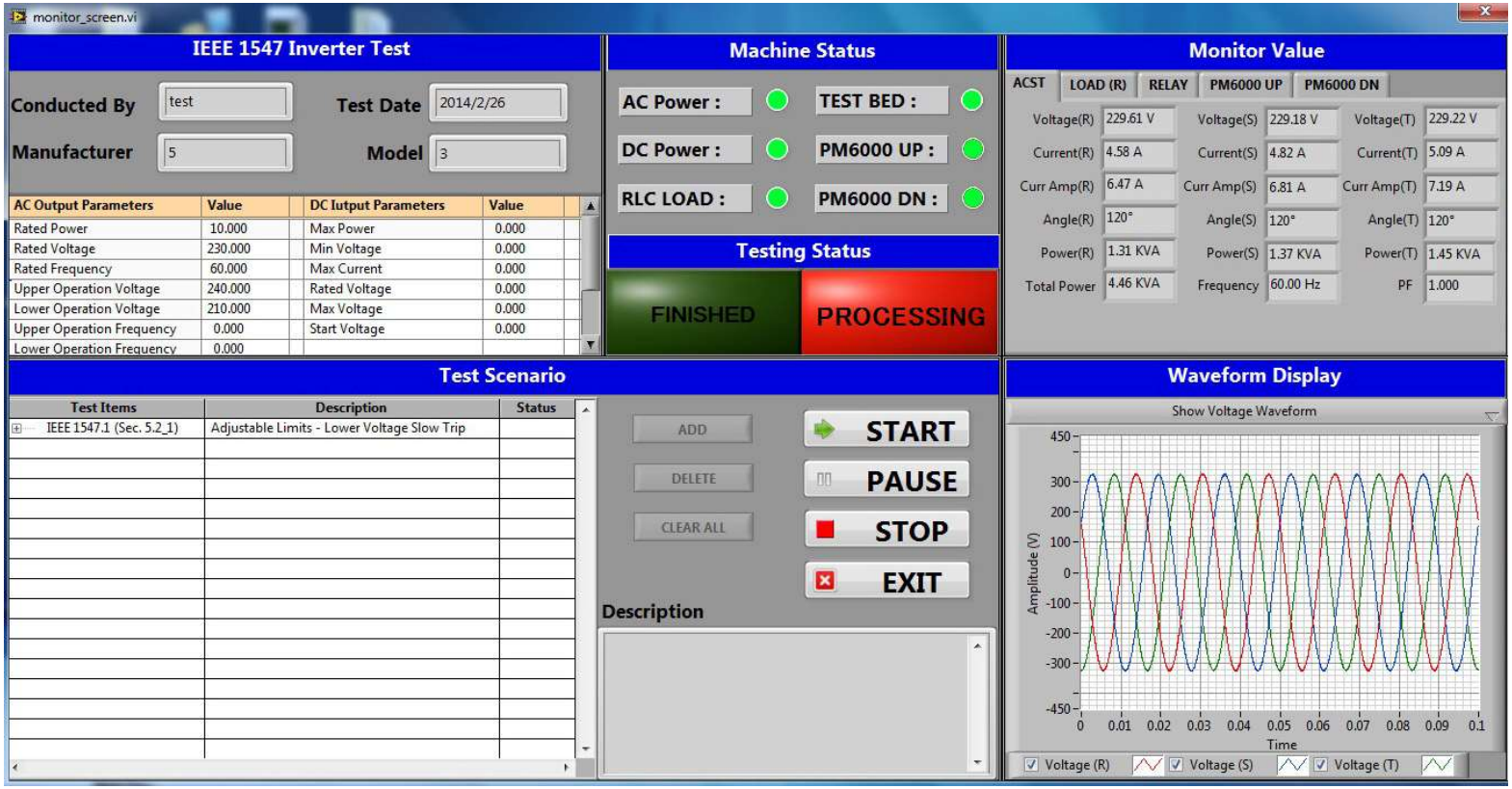
5kW PV Inverter / Micro Inverter Test System

Virginia Tech Future Energy Electronics Center

UL Northbrook

Preen

Test Software (1)



(i). This software is the key function of the whole system, which can provide the users a fully automatic execution of all the procedures specified in IEEE-1547 & IEEE-1547.1

(ii). Above is the main page of the software, also the central control and monitoring page. All the other control and monitoring branch out from here.

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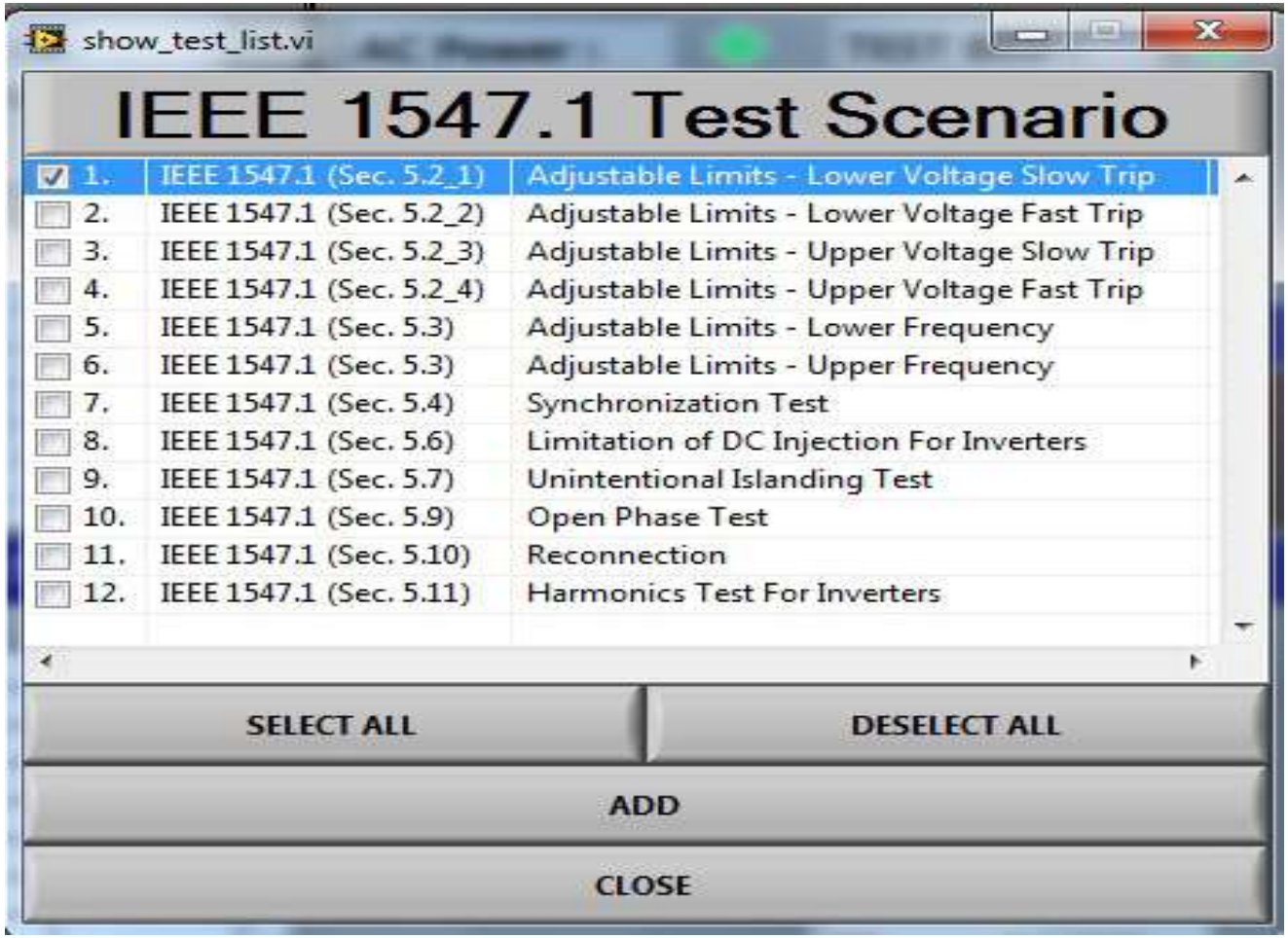
Test Software (2)



(i). This page shows the flexibility and modularization of four software. All the procedures in IEEE-1547.1 can be individually picked and executed in a user defined sequence.

(ii) Automatically Generate Test Report

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TUV 120kW PV Inverter Test System

ITRI (TUV Alliance) 120kW PV Inverter Testing Facility: The lab help PV inverter manufacturers to streamline procedures, as at present different countries have different standards for the equipment.

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100kW PV Inverter Test System

This solution includes :

- Programmable DC Power Supply
- Programmable AC Power Source
- Digital Power Meter
- Power Analyzer
- Programmable AC Electric Load
- System Controller
- Testing Software

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500kW PV Inverter Production Test

DC Power Supply **1200kVA Grid Simulator**

500kW Grid Connected Test System

Preen

Thank you for joining us

AC Power Corp.

US Office (Key Power Inc.)

192 Technology Road, STE S

Irvine, CA 92618

TEL : 949-988-7799