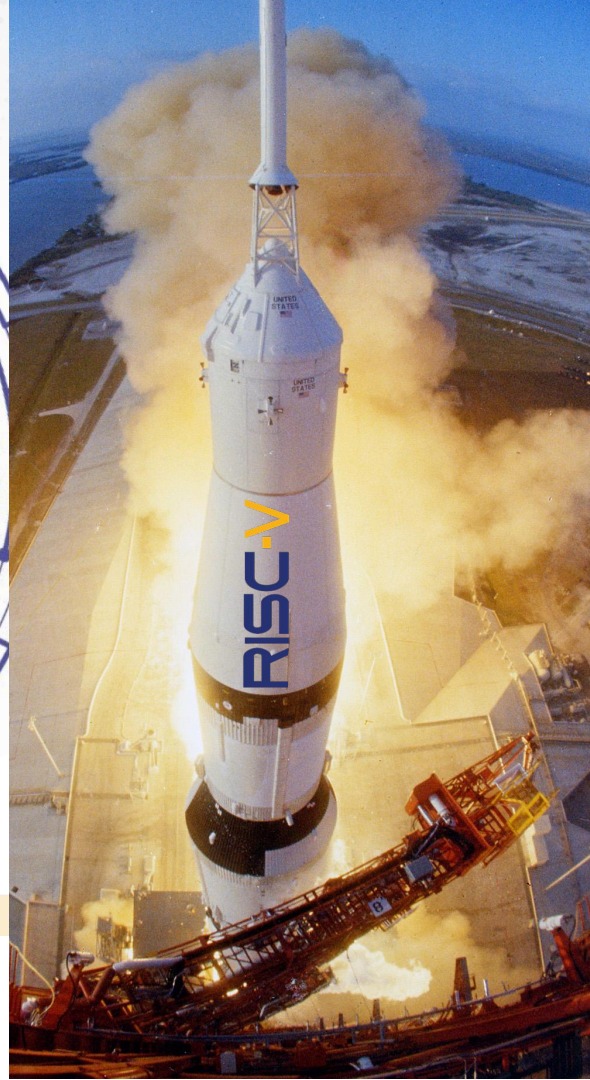
SiFive

RISC-V®

An Unlimited Future



Drew Barbier
Senior Director, Product Management
March 16th, 2023

Special Thanks - Krste Asanovic

The bulk of this presentation is from Krste Asanovic's talk:

The Past, Present, and Future of RISC-V
https://www.youtube.com/watch?v=RrVRMFjYti0

Krste Asanovic
Prof. EECS, UC Berkeley;
Chairman, RISC-V Foundation;
Co-Founder and Chief Architect,
SiFive Inc.

Who Am I?

Drew Barbier

SiFive Inc.

Senior Director, Product Management

Bio

- Early joiner to SiFive (March 2017)
- ASIC Architect, Faraday
- Arm, Various

Companies and their ISAs Come and Go

- Digital Equipment Corporation, RIP! (**PDP-11**, **VAX**, **Alpha**)
- Intel's dead ISAs (**i960**, **i860**, **Itanium**, …)
- **SPARC**

Why entrust your software investment to a proprietary ISA?

  - Opened up MIPS R6 ISA in 2018, then made not open in 2019, now doing RISC-V….
- **IBM POWER**
  - Initially proprietary, opened up in 2019 as OpenPower. Crickets…
- **ARM**
  - Sold to Softbank in 2016
  - Nvidia announced acquiring ARM 2020, deal cancelled 2022, now to IPO, …

Open Interfaces Are Accepted Practice!

Field	***Open Standard***	***Free, Open Implementations***	***Proprietary Implementations***
Networking	Ethernet, TCP/IP	*Many*	*Many*
OS	Posix	Linux, FreeBSD	Windows
Compilers	C	gcc, LLVM	Intel icc, ARMcc, Xcode
Databases	SQL	MySQL, PostgresSQL	Oracle 12C, DB2
Graphics	OpenGL/Vulkan	Mesa3D	DirectX
ISA	??????	----------	x86, ARM, IBM360

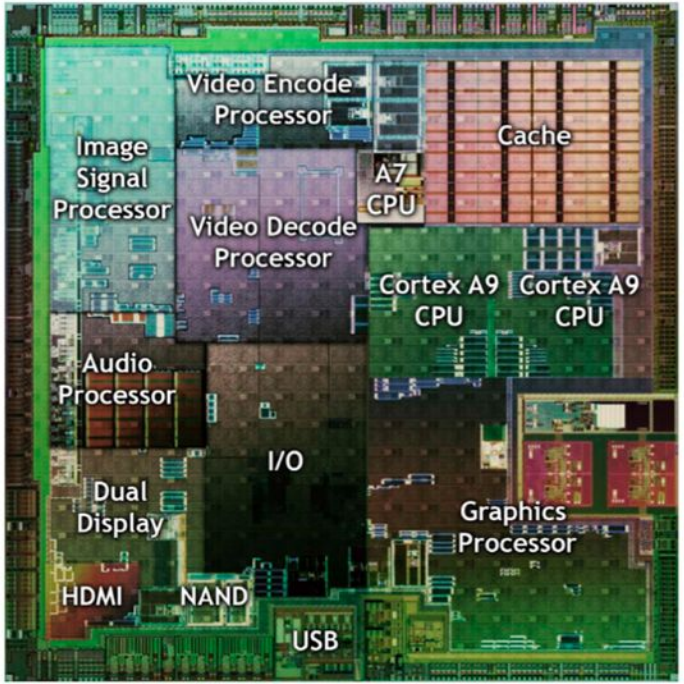
Why not successful open standards and multiple open-source & proprietary implementations, like other fields?

Many ISAs on one SoC

- Applications processor (usually ARM)
- Graphics processors
- Image processors
- Radio DSPs
- Audio DSPs
- Security processors
- Power-management processor
- > dozen ISAs on some SoCs – each with unique software stack

Why?

- Apps processor ISA too big, inflexible for accelerators
- IP bought from different places, each proprietary ISA
- Engineers build home-grown ISA cores



NVIDIA Tegra SoC

Do we need all these different ISAs?

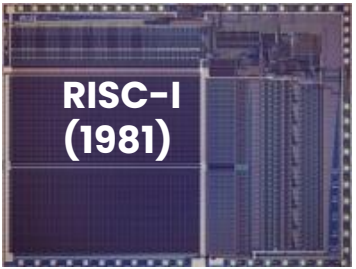
Must they be proprietary?

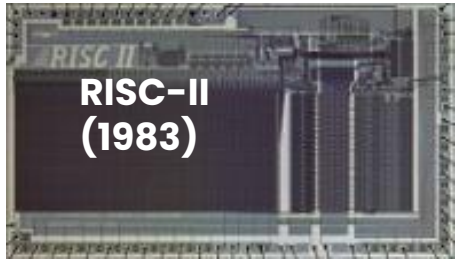
Must they keep disappearing?

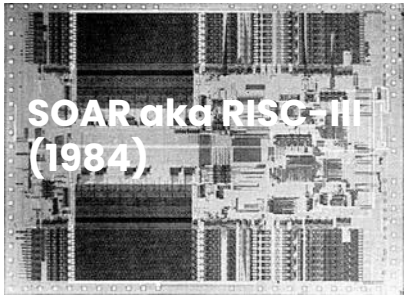
What if there was one stable free and open ISA everyone could use for everything?

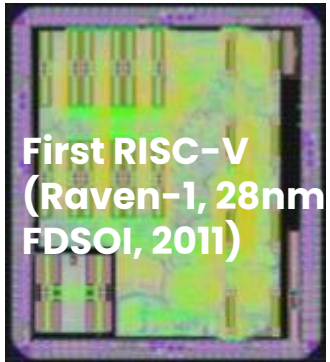
RISC-V Background

- In 2010, after many years and many research projects using MIPS, SPARC, and x86, time for architecture group at UC Berkeley to choose ISA for next set of projects
- Obvious choices: x86 and ARM
  - x86 impossible – too complex, IP issues
  - ARM mostly impossible – complex, no 64-bit in 2010, IP issues
- Began a "3-month project" during summer 2010 to develop clean-slate ISA
  - Principal designers: **Andrew Waterman**, **Yunsup Lee**, **David Patterson**, **Krste Asanovic**
- Four years later, May 2014, released frozen base user spec
  - many tapeouts and several research publications along the way
- Name RISC-V (pronounced "risk-five") represents fifth major Berkeley RISC ISA










Hot Chips 2014
Flint Center, Cupertino

RISC-V International (RVI)

SiFive

- RISC-V is a free and open Instruction Set Architecture (ISA)
- Frozen base user spec released in 2014, contributed, ratified, and openly published by RISC-V International

RISC-V International is a non-profit entity serving members and the industry

Our mission is to accelerate RISC-V adoption with shared benefit to the entire community of stakeholders.

- ✔ Drive progression of **ratified specs, compliance suite, and other technical deliverables**
- ✔ **Grow the overall ecosystem / membership,** promoting diversity while preventing fragmentation
- ✔ Deepen **community engagement and visibility**


Just a subset of 2022...

RISC-V Ecosystem

Software

Open-source software:
Gcc, binutils, glibc, Linux, BSD, LLVM, QEMU, FreeRTOS, ZephyrOS, LiteOS, SylixOS, …

Commercial software:
Lauterbach, Segger, IAR, Greenhills, WindRiver, Micrium, ExpressLogic, Ashling, Imperas, AntMicro, …

RISC-V International

ISA specification | Golden Model | Compatibility

Hardware

Open-source cores:
Rocket, BOOM, RI5CY, Ariane, PicoRV32, Piccolo, SCR1, Swerv, Hummingbird, WARP-V, XiangShan, BlackParrot, …

Commercial core providers:
Alibaba, Andes, Bluespec, Cloudbear, Cobham, Codasip, Cortus, Imagination, InCore, MIPS, Nuclei, Semidynamics, **SiFive**, StarFive, Syntacore …

Inhouse cores:
Nvidia, WDC, Seagate, Alibaba, +others

RISC-V (Modest) Project Goal

SiFive

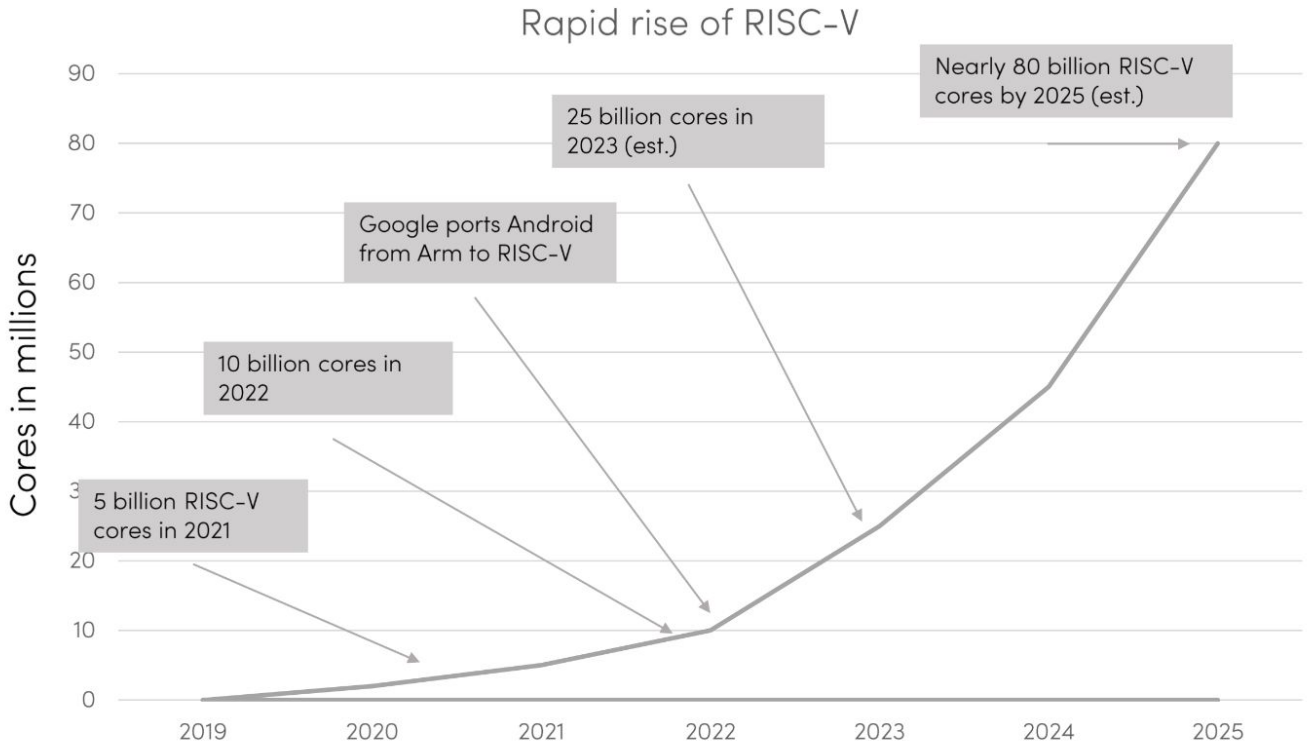
Become the industry-standard ISA for all computing devices

This is happening!

Far faster, more domains, than anyone predicted
Demand at every performance level (low to ludicrous)
Demand for all features of all other ISAs ever built!

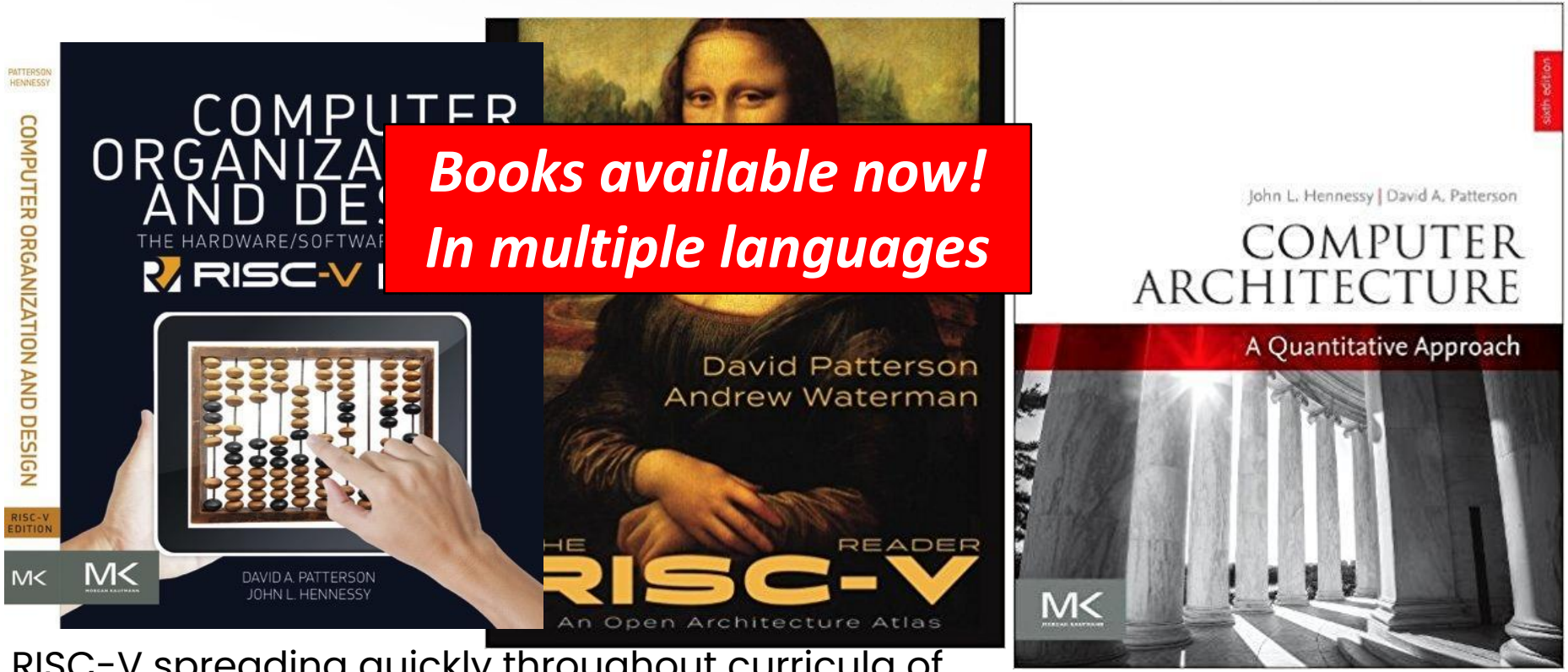
Using a new community ISA spec development model

Chip industry rapidly adopting RISC-V



Source: SEMICO Market Research Corp. 3/21

RISC-V in Education



Books available now!
In multiple languages

RISC-V spreading quickly throughout curricula of top schools (>>10,000s undergrads/year)

Why is RISC-V So Popular?

- Engineers sometimes “don’t see forest for the trees”
- The movement is not happening because some benchmark ran 10% faster, or some implementation was 30% lower power (though that might be true)
- The movement is happening because new business model changes everything
  - Pick ISA first, then pick vendor or build own core
  - Add your own extension without getting permission
  - Commercial, academic, and open-source ecosystems can coalesce around a single open standard

Comparing ISA Business Models

ISA	Chips?	Architecture License?	Commercial Core IP?	Add Own Instructions?	Open-Source Core IP?
x86	Yes, ***three*** vendors	***No***	***No***	***No***	***No***
ARM	Yes, ***many*** vendors	Yes, ***expensive***	Yes, ***one*** vendor	***No*** *(Mostly)*	***No***
RISC-V	Yes, ***many*** vendors	Yes, ***free***	Yes, ***many*** vendors	***Yes***	***Yes, many available***

RISC-V: The ISA that likes to say "Yes"

RISC-V Completeness

- Large number of extensions ratified in 2021
- Vectors
  - Full application vectors (“V”) + subsets for embedded (“Zve*”)
- Hypervisor
  - supports Type-1 and Type-2
- Scalar Crypto
  - NIST and Shang-Mi cipher suites
- Cache Management Operations
  - Block prefetch, zero, clean/flush/discard
- Virtual Memory Enhancements
  - Larger pages (64KiB), PTE-based memory attributes, faster invalidate
- More extensions in flight for 2022 and beyond
  - IOMMU, Advanced scalable interrupts, vector crypto, FP16, BF16, pointer masking, …

Fragmentation Versus Diversity

Fragmentation:
Same thing done different ways

Diversity:
Solving different problems

How is RISC-V Avoiding Fragmentation?

Two powerful forces keep fragmentation at bay:

1. **Users**: No one wants a repeat of vendor lock-in.

2. **Software**: No one, not even nation state, can afford their own software stack. Upstream open-source projects only accept frozen/ratified Foundation standards.

Managing Diversity

Raw extensions

- Base + standard extensions + custom extensions
- Full suite of options available for experimentation and specialized uses
- Massive combinatorial space of options

ISA Profiles

- Packages of ISA extensions for given domain
- Initial set: RVI20 (basic), RVA20/22/23 (application processor)
- Factor out common ISA combinations for use in platform standards

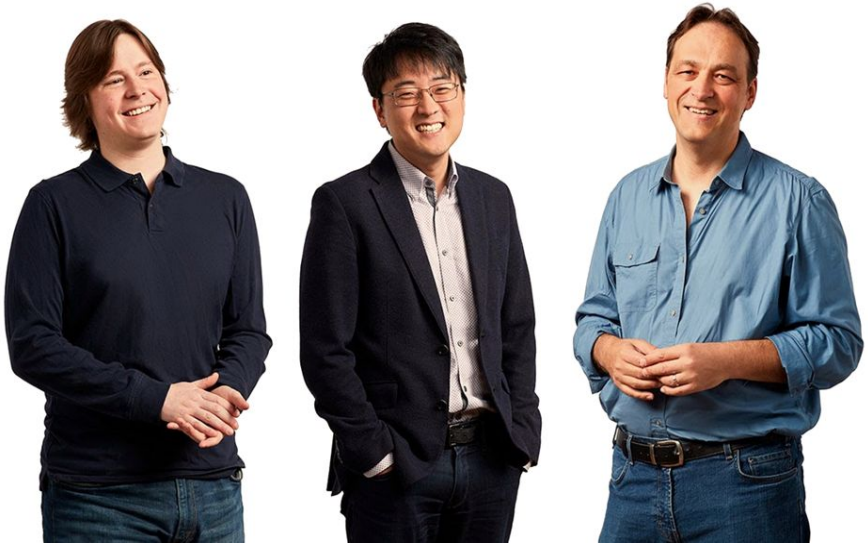
Platform standards

- Hardware/software standards for platforms (much more than just ISA)
- Initial focus OS-A platform for Unix-like OS (includes IOMMU, AIA, etc)


SiFive
Leading RISC-V
Forward

SiFive: The RISC-V Founder and Brand Standard

The Inventors of RISC-V



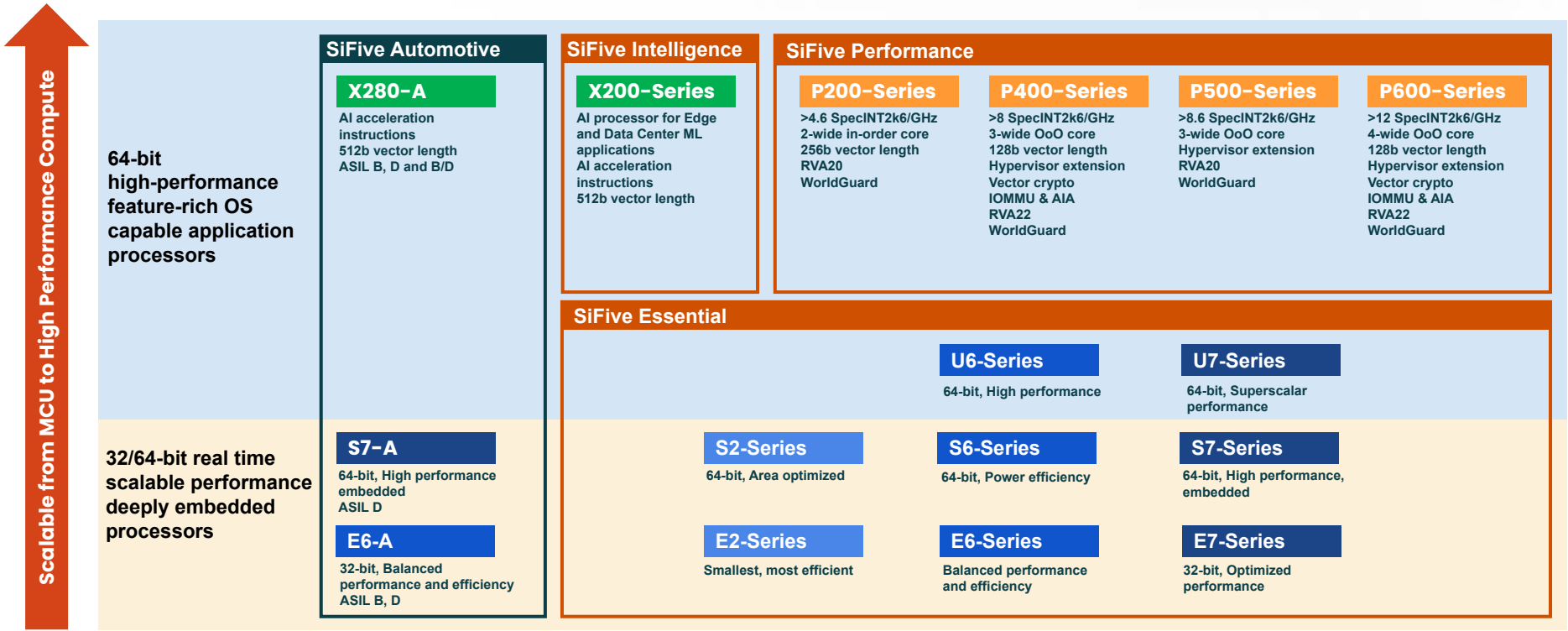
SiFive's founders are the same UC Berkeley professor and PhDs who invented the RISC-V Instruction Set Architecture (ISA) in 2010

The Most Respected Private Semiconductor Company
2022

GSA 2022 AWARDS CELEBRATION
WINNER

300+	100+	8 of 10	500+	$2.5B+
Design Wins	Customers	Top semiconductor companies work with us	Employees	Valuation

SiFive broad IP portfolio



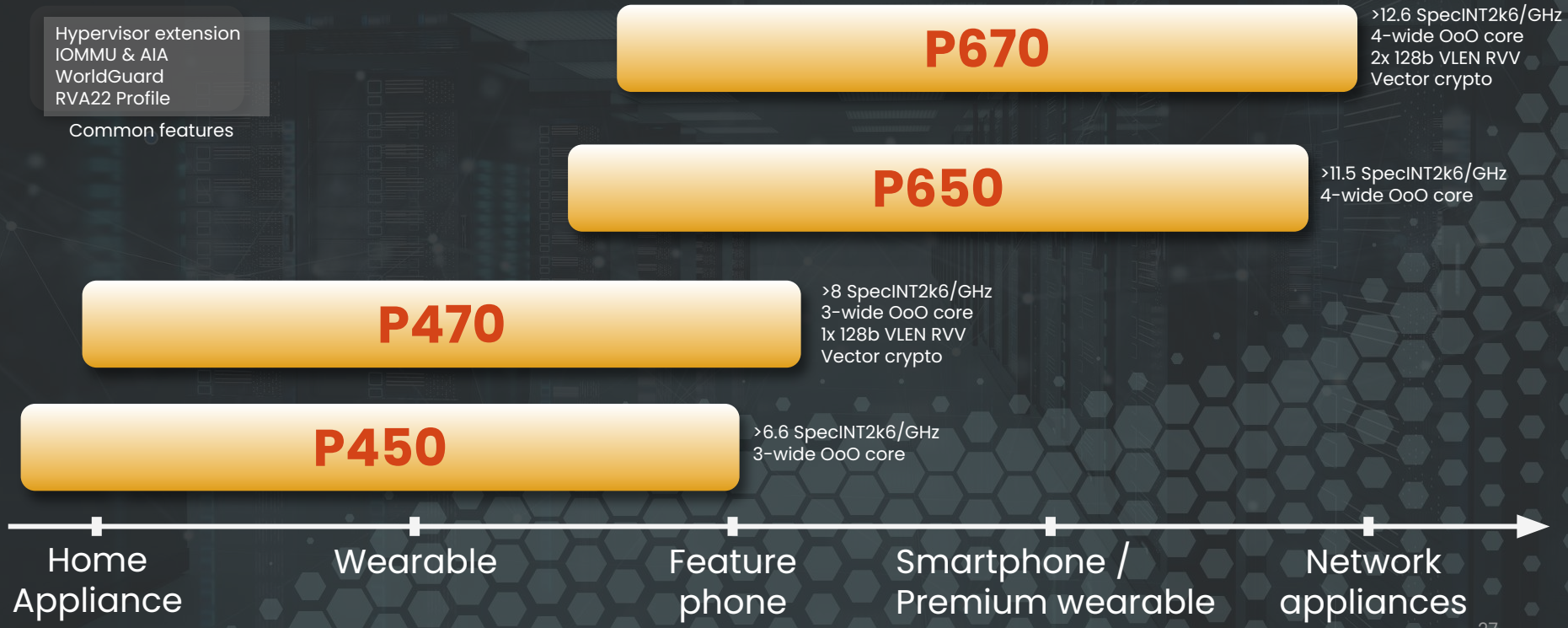
SiFive Performance™ Family

Market **leading RISC-V** Application **Processors**

- Performance density leadership
- First with latest RISC-V features, standards, and technology
- High performance with optimized power efficiency
- SiFive momentum with NASA, Google, and Intel Horse Creek

SiFive Performance Family

2023 Product Lineup

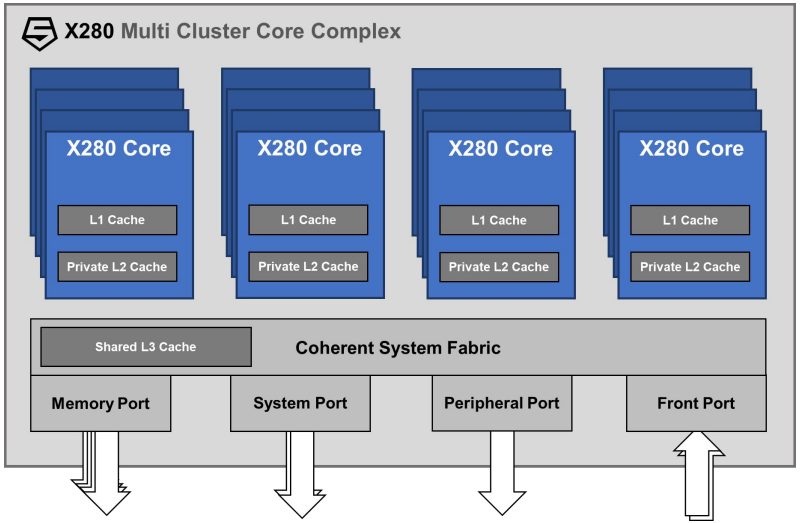


SiFive® Intelligence™ X280 Processor

Optimized for the modern workload

- Highly optimized for AI models and software frameworks
- Enables highly efficient, simple system design
- Ideal companion to custom NN hardware accelerators
- RISC-V Vectors brings market leading performance and power efficiency
- Performance scalability with multi-cluster, multi-core configurability
- Strong momentum in image processing and data center compute applications

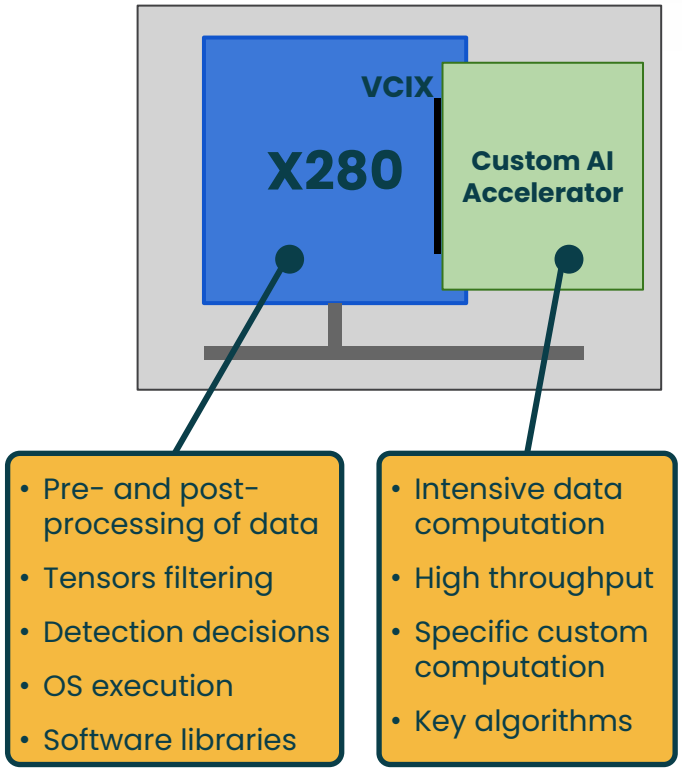
Scaling Performance with Multi-core



Extended Performance, Simple Software

- Flexibility to configure number of clusters and cores to meet performance at minimal area, power
- Full data Coherency across all cores in the multi-core system
- Support of Linux OS to simplify multi-core software usage model, data management
- Multiple SoC connectivity ports offering coherent memory mapped accesses across all cores

AI dataflow optimization

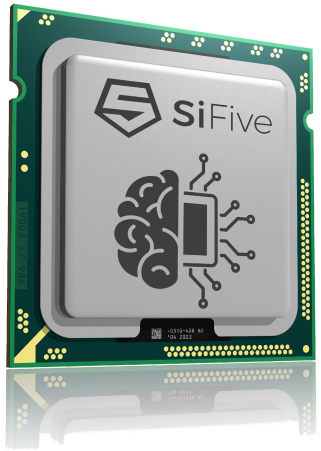


Workload and task management

- Simplify AI accelerator design for required use cases
- Provide comprehensive data management, dataflow and housekeeping reducing latency, power and area
- Vector Coprocessor Interface Extension **(VCIX)** enables tightly coupled connectivity to an AI accelerator for optimized performance
- Linux OS with single toolchain for complete application control

SiFive

Thank you



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