



IEEE CEDA CTS, Nov. 12, 2013



Nanometer IC Design for Manufacturability and Reliability in Extreme Scaling and Beyond

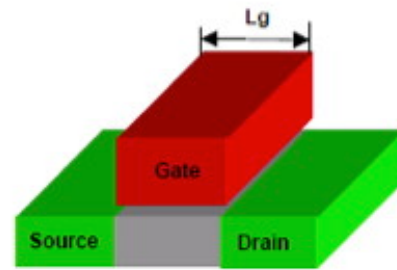
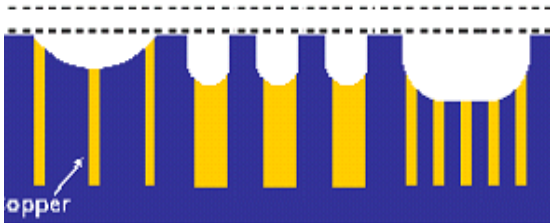
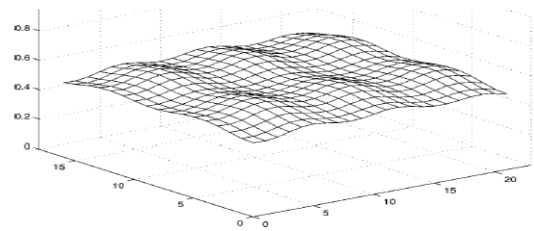
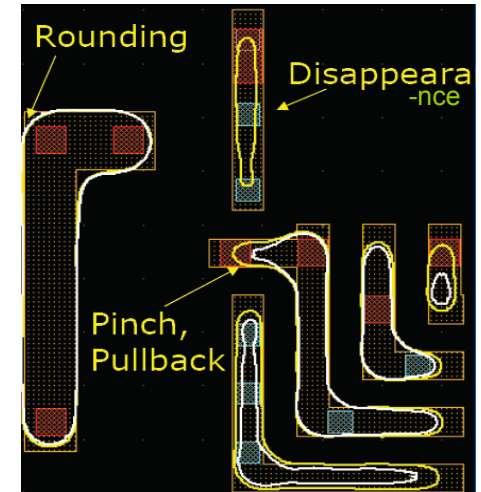
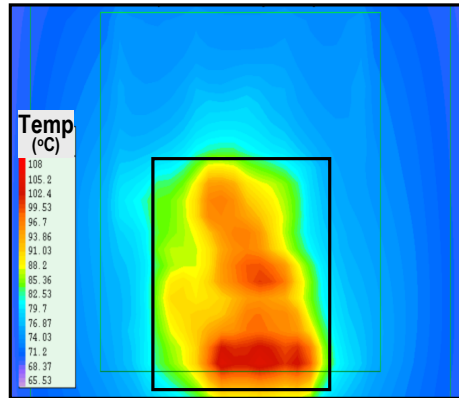
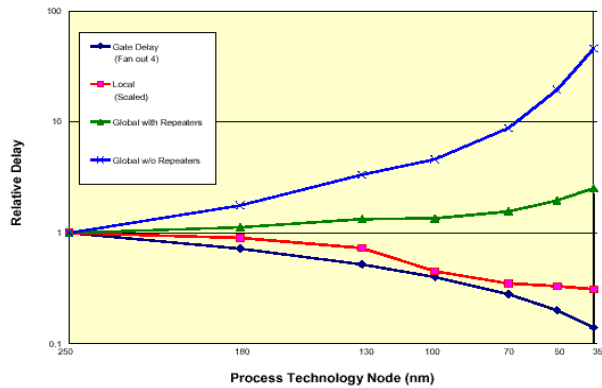
David Z. Pan

Dept. of Electrical and Computer Engineering

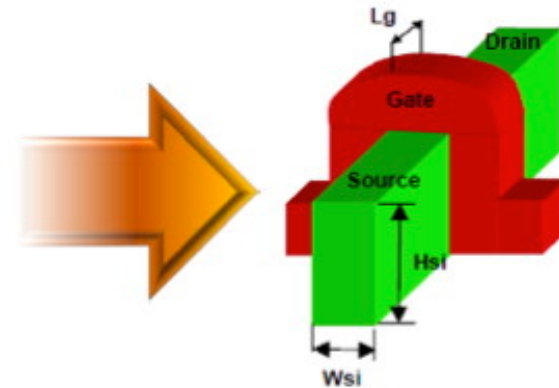
The University of Texas at Austin

<http://www.cerc.utexas.edu/utda>

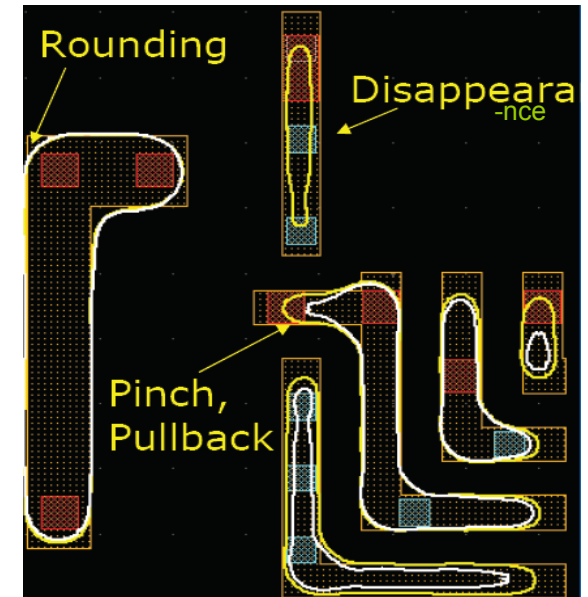
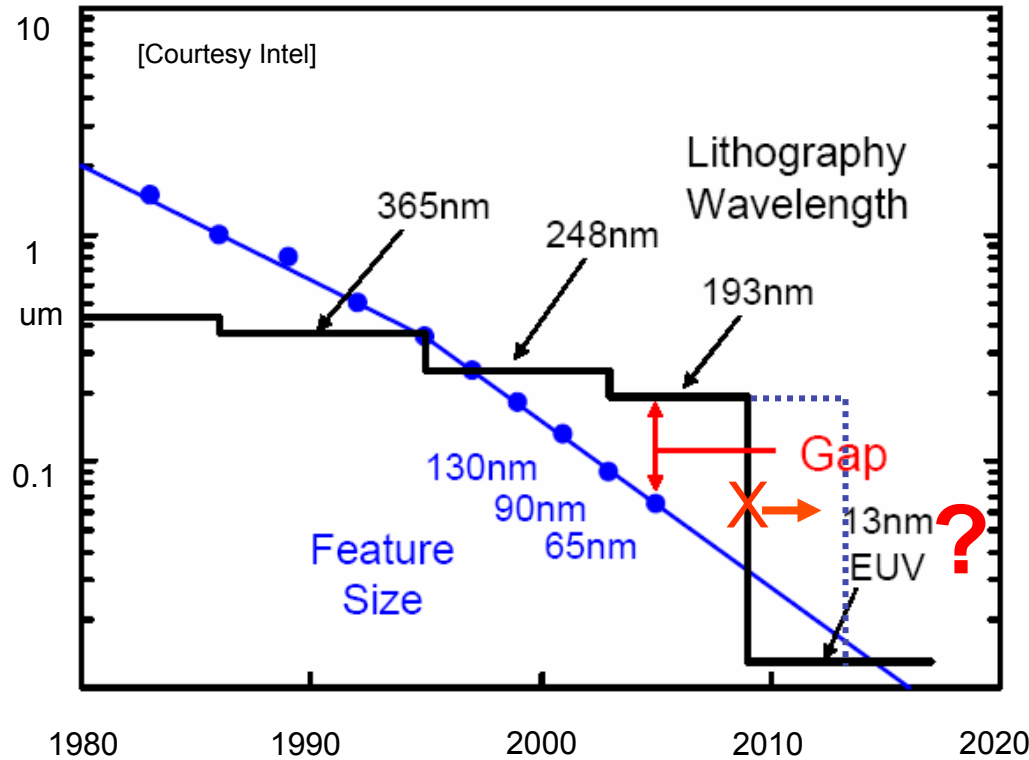
Nanometer Issues



Conventional Planar FET

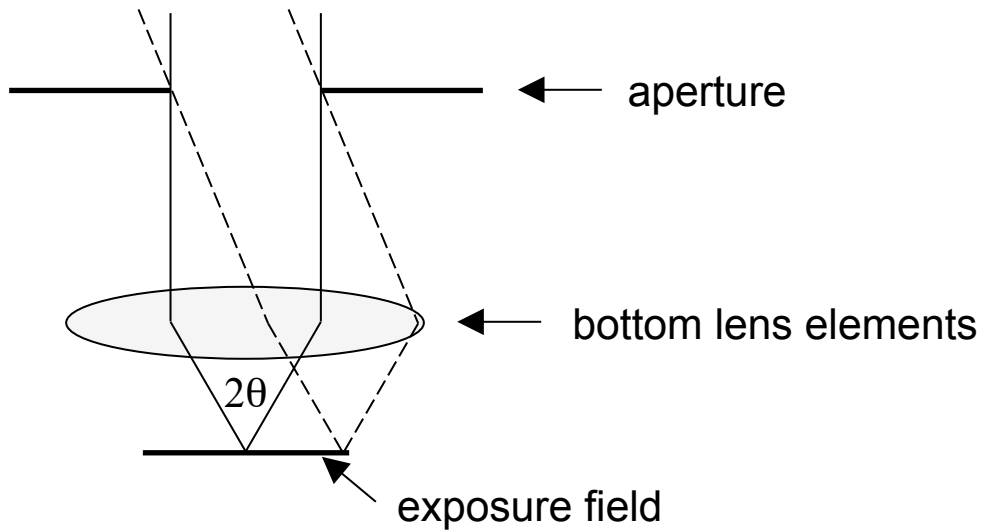


Lithography Status & Challenges



- ◆ The industry forced to extend 193nm lithography
 - › Immersion, extreme RET
 - › Double/Triple Patterning Lithography for 22nm/14nm, ...

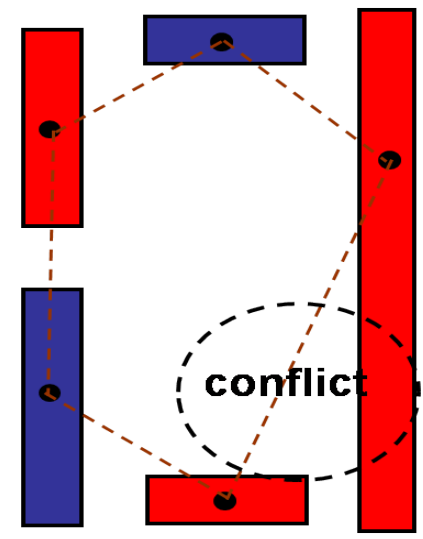
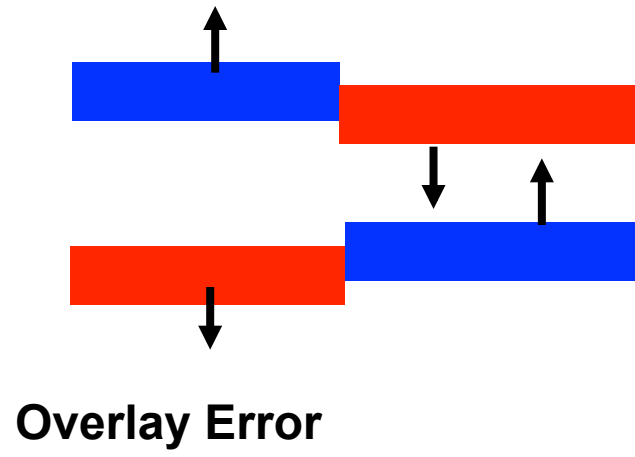
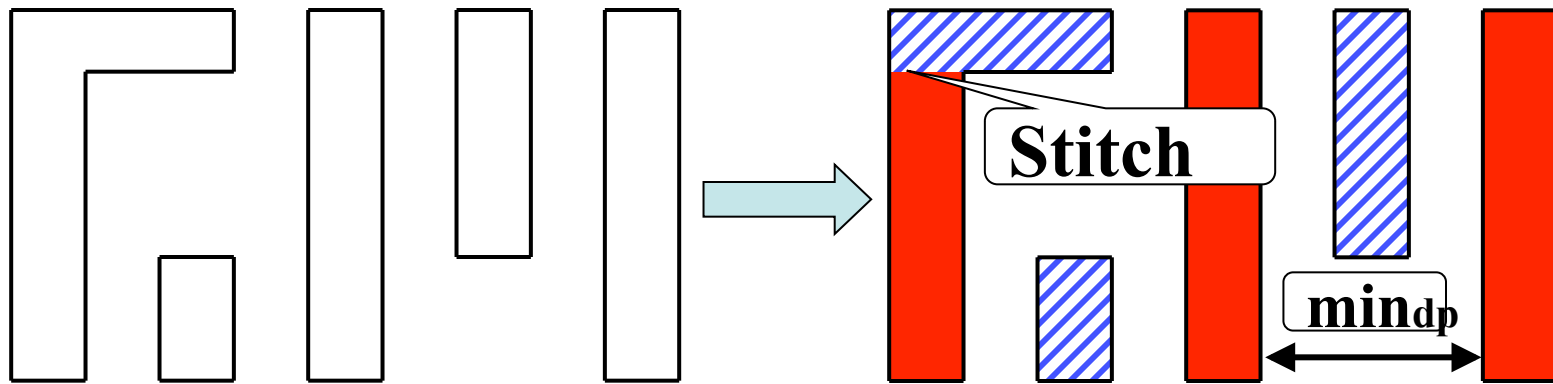
Resolution Limit of Optical Lithography



$$\begin{aligned} \text{pitch} &> \frac{0.5\lambda}{n\sin\theta} \\ &= \frac{0.5 * 193}{1.35} \\ &= 72 \text{ nm} \end{aligned}$$

With single exposure, the practical limit is ~80 nm

What is Double Patterning?



Back in 2003



Jeffrey: "Daddy, don't worry. I can show you some **bright** ideas!"

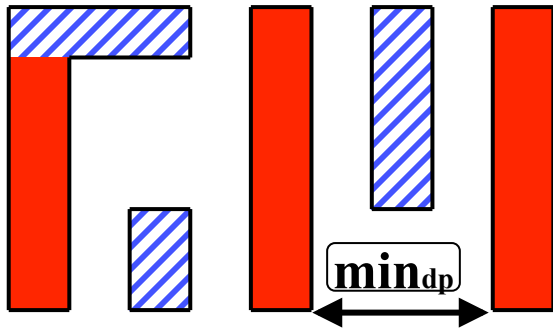


"Double patterning!!!"

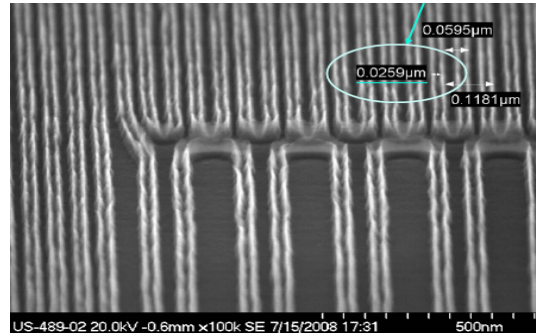
Emerging Lithography



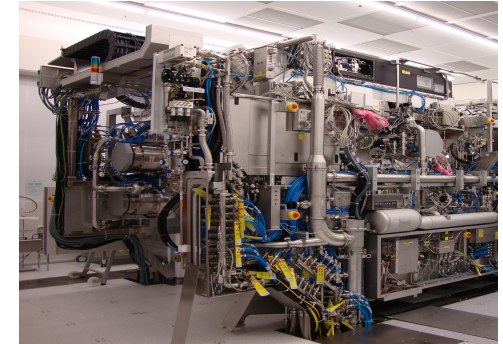
193i w/ DPL



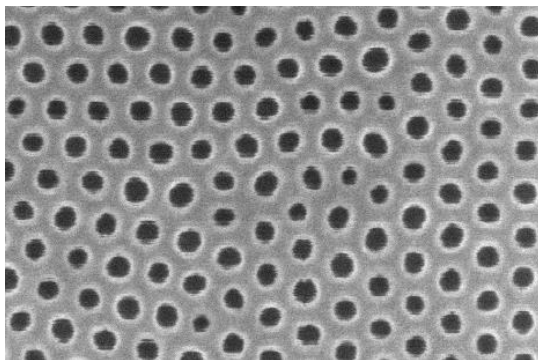
Quadruple patterning



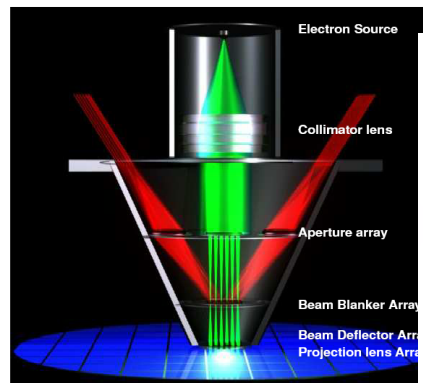
EUV



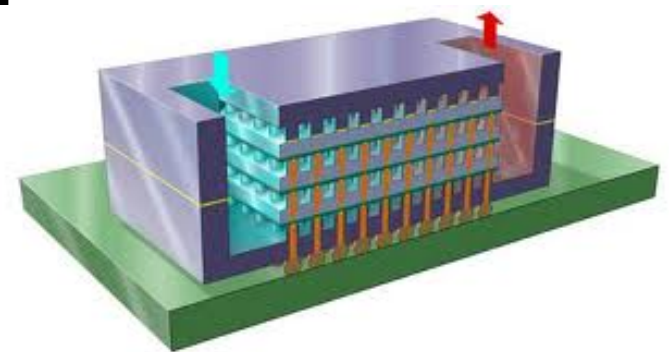
DSA



E-beam



3D-IC



The “**Moore**”, the **Merrier**!

◆ **More Moore**

- Nano-Patterning for Extreme Scaling
- Lithography Aware Physical Design

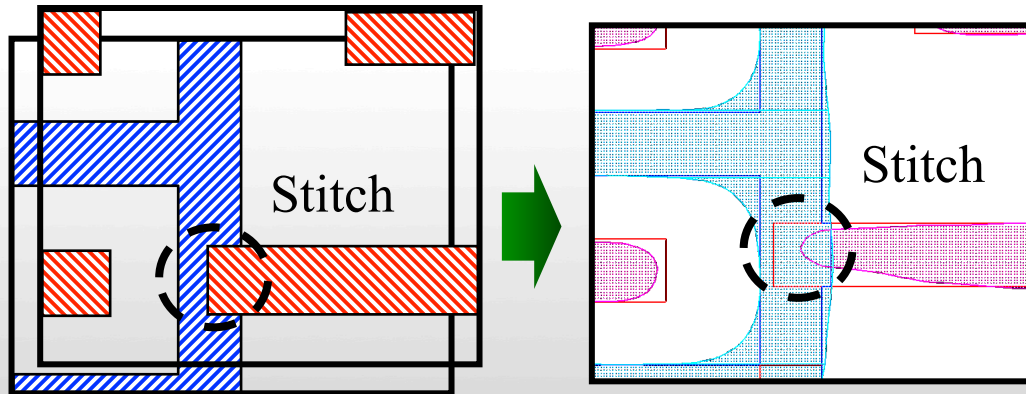
◆ **A different kind of “Moore”**

- 3D Integration
- New devices (e.g., nanophotonics) ...

→ Need synergistic design and technology co-optimization for cross-layer resilience

DPL Layout Decomposition

Minimum Stitch Insertion

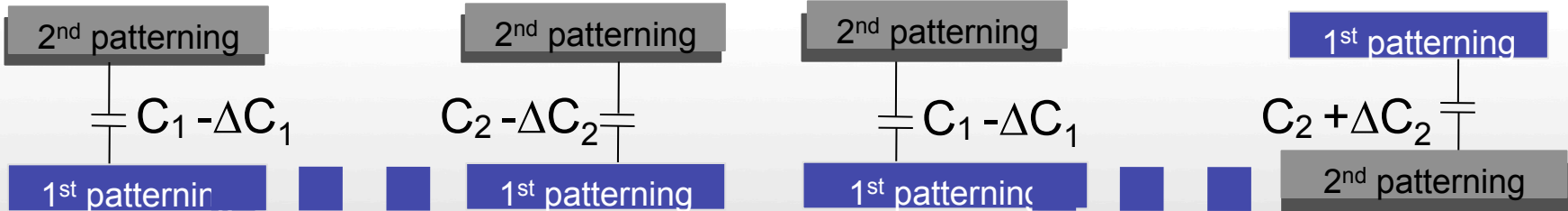


[Lucas SPIE'08]

- 1) Minimize stitch #
- 2) A bit more overlap margin for stitch, but area increases

Overlay Compensation

[Yang+, ASPDAC10]

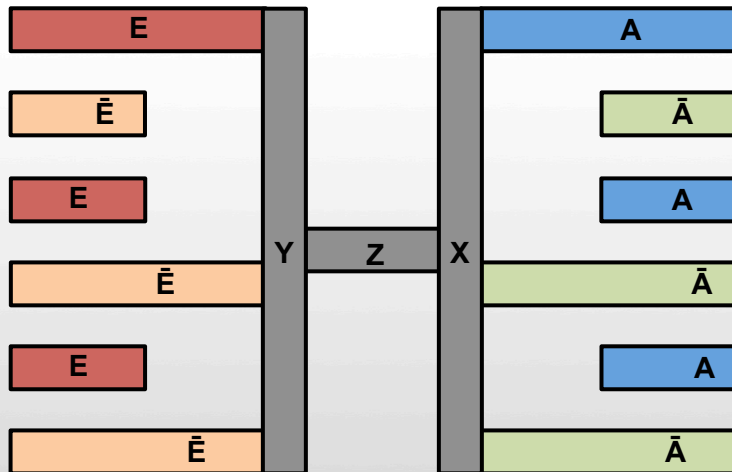


Without Overlay Compensation

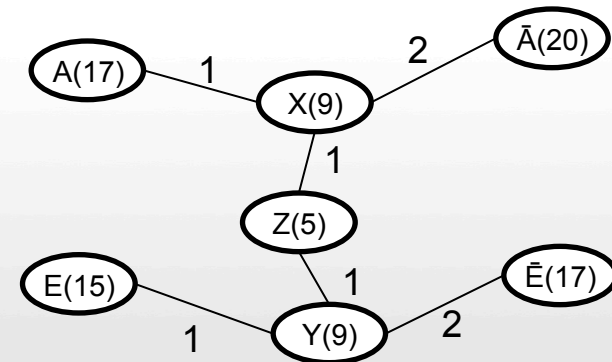
With Overlay Compensation

A Graph-Partitioning Based, Multi-Objective Decomposer

Decomposition Graph Construction



[Yang+, ASPDAC10]



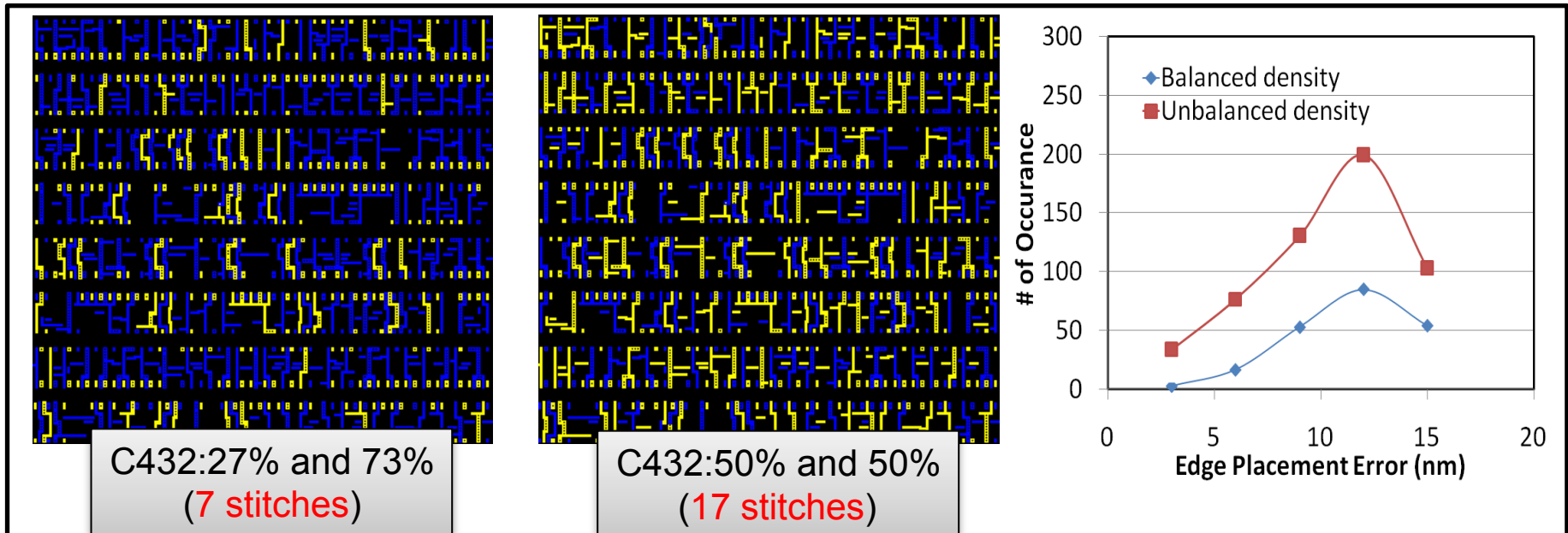
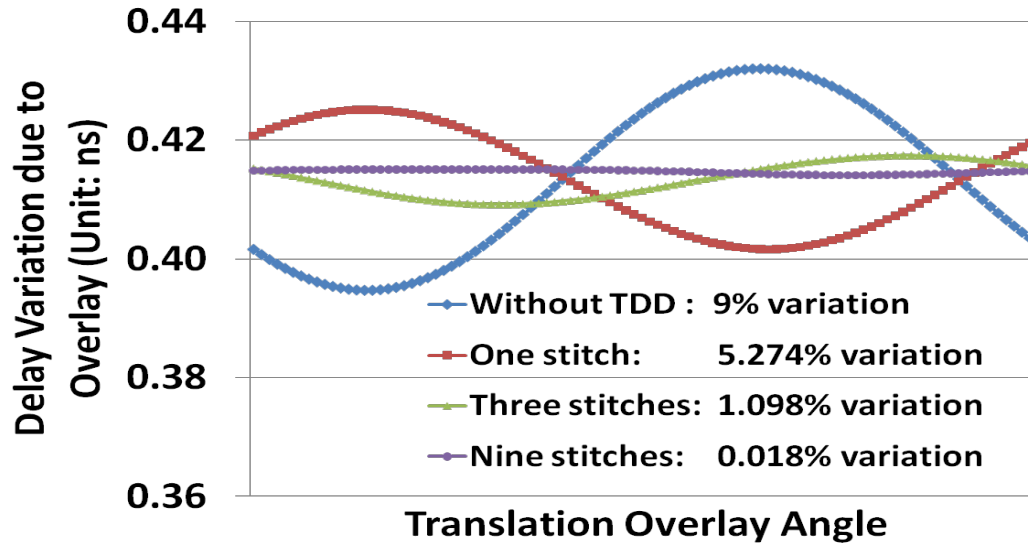
Constraint:
(A, \bar{A}) and (E, \bar{E}) are repulsive pairs.

Theorem : Stitch minimization problem is equivalent to the min-cut partitioning of the decomposition graph

Extensions of the framework: to incorporate other constraints and costs into graph partitioning, e.g., **balanced density, overlay compensation**, and so on

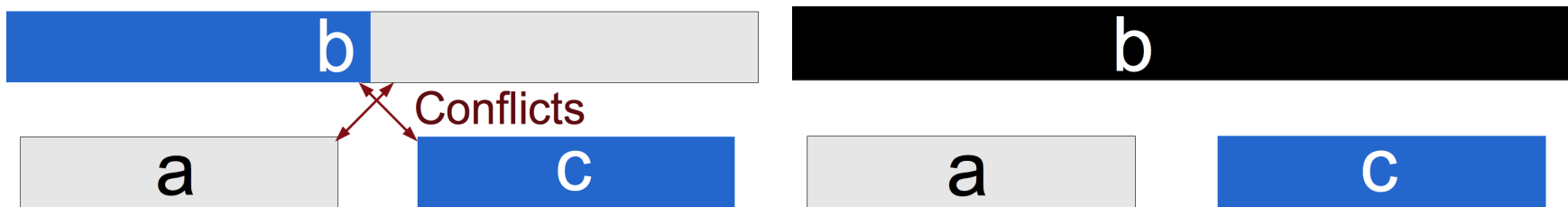
Overlay Compensation & Density Balancing

[Yang+, ASPDAC10]



Triple Patterning

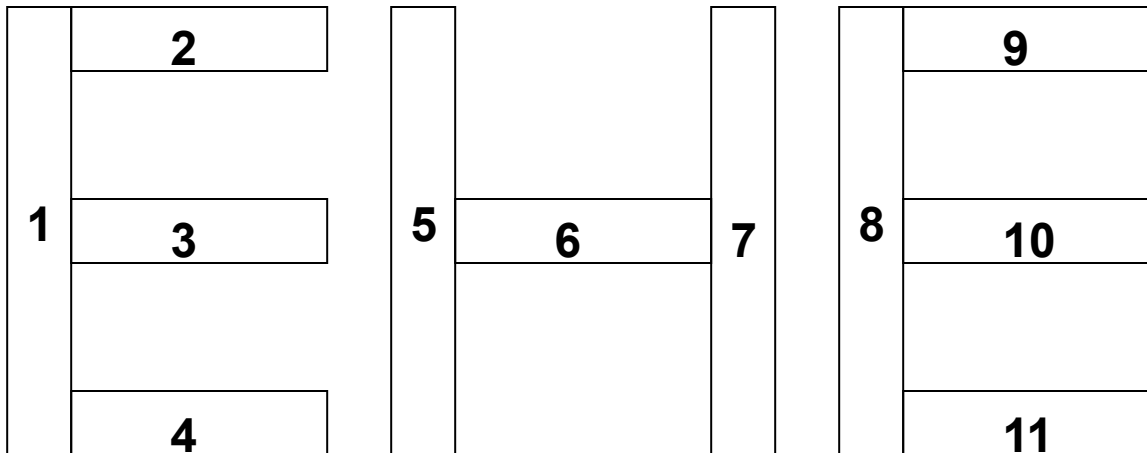
- ◆ Extension of double patterning concept
- ◆ Original layout is divided into three masks
 - › Resolve native conflicts of DPL
 - › Achieve further feature-size scaling (14nm, 11nm)



- ◆ Very active research area!
- ◆ DAC'12 Best Paper; ICCAD'13 Best Paper
- ◆ ICCAD'13 Special Session
 - › Session 3B: Triple Patterning, Triple the Trouble?

Electronic Beam Lithography

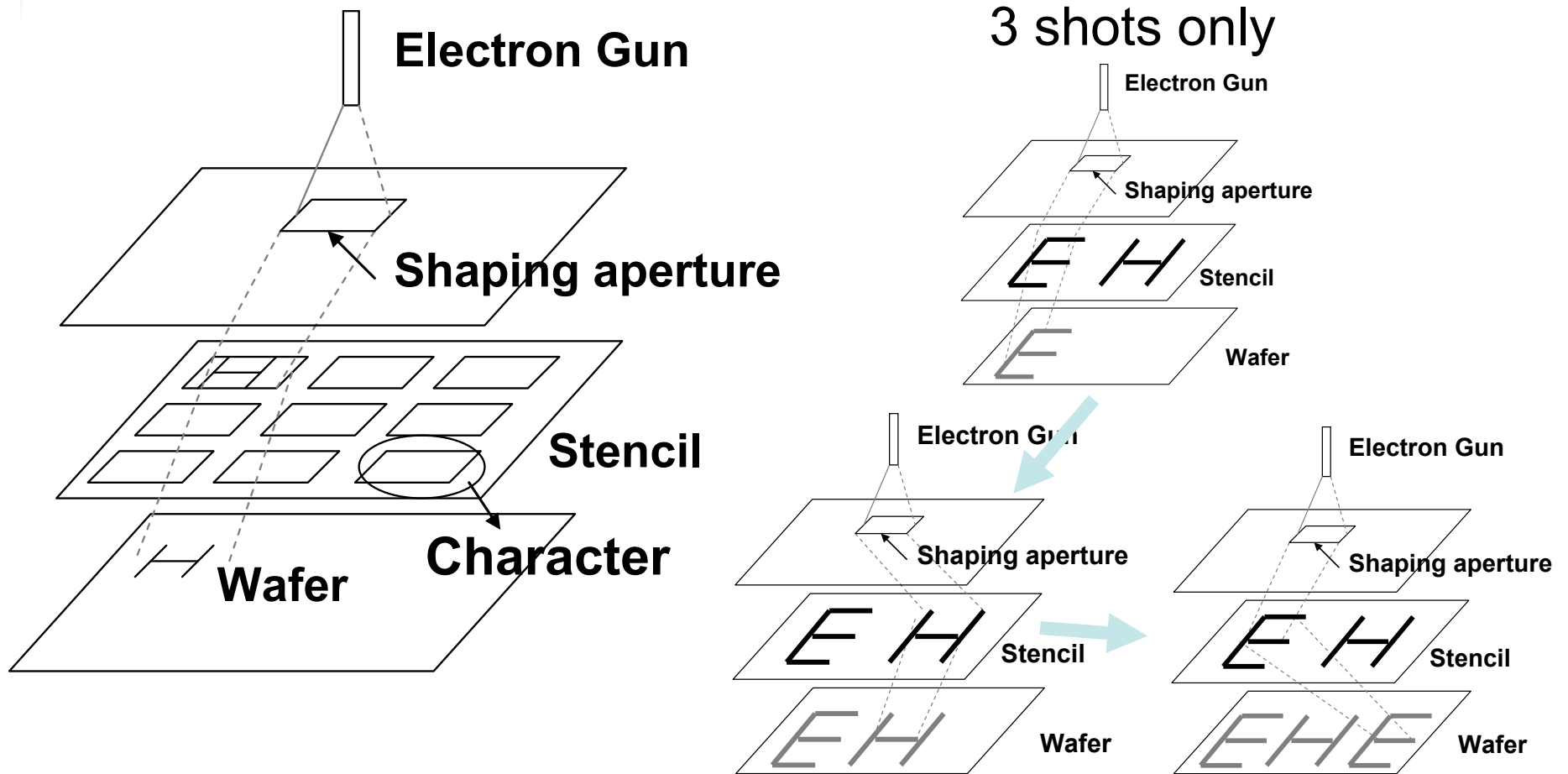
- ◆ Maskless technology, which shoots desired patterns directly into a silicon wafer
- ◆ Low throughput is its major hurdle
 - › E.g., Variable Shaped Beam (**VSB**)



Total number of 11 shots are needed

Character Projection (CP) Technology

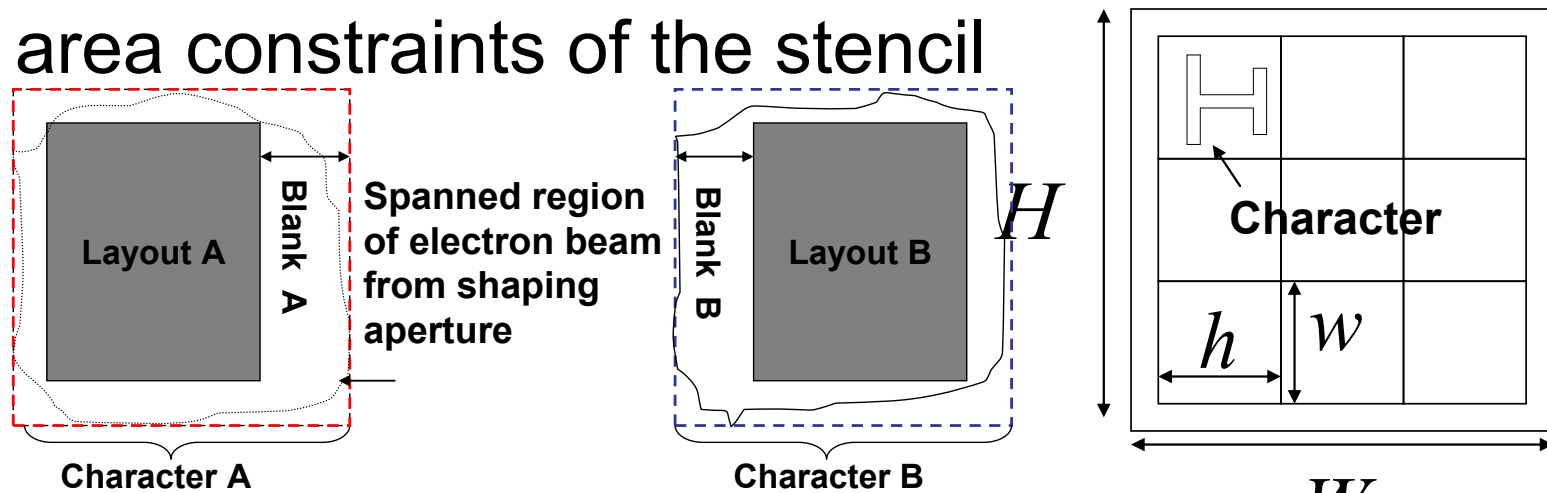
- ◆ Print some complex shapes in one electronic beam shot, rather than writing multiple rectangles.



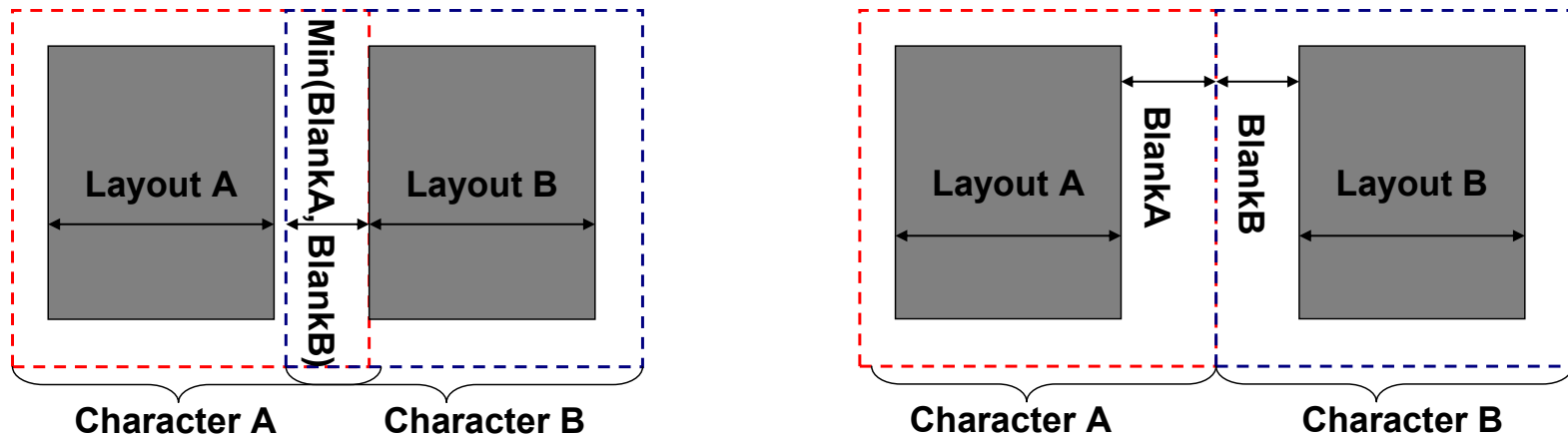
Overlapped Characters Planning

[Yuan and Pan, ISPD'11 Best Paper Award]

- ◆ The number of characters is limited due to the area constraints of the stencil



- ◆ By over-lapping adjacent characters, more characters are allowed to be put on the stencil



The “Moore”, the Merrier!

◆ More Moore

- Nano-Patterning for Extreme Scaling
- **Lithography Aware Physical Design**

◆ A different kind of “Moore”

- 3D Integration
- New devices (e.g., nanophotonics) ...

➔ **Need synergistic design and technology co-optimization for cross-layer resilience**

LAPD

Another LAPD

- ◆ Double/multiple patterning layout compliance/decomposition
- ◆ Post-layout, maybe too late!
- ◆ Lithography Aware Physical Design (LAPD) →
- ◆ Litho Hotspot **Detection**
- ◆ Litho Friendly Design
 - › Hotspot **Avoiding/Correction**
 - › **Correct by Construction/Prescription**

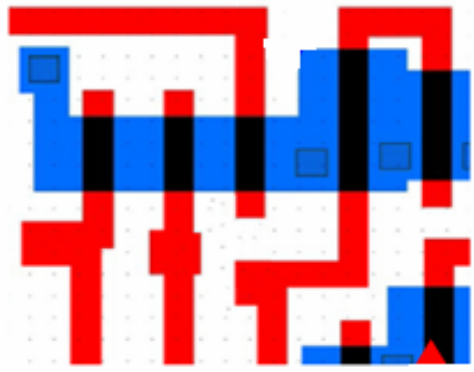


Detection

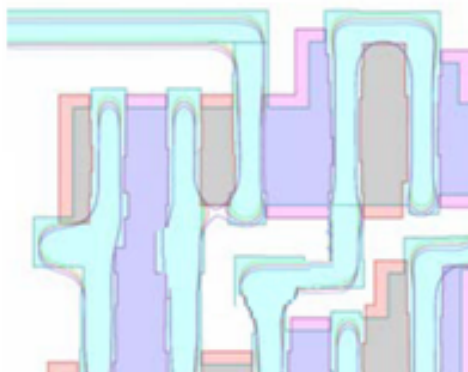


Correction

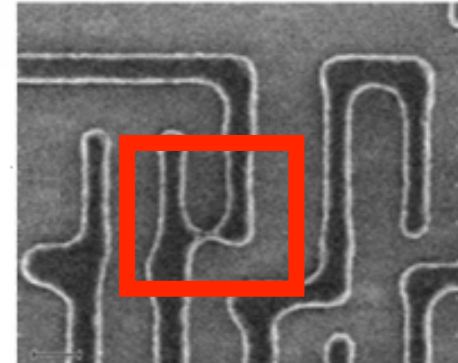
Lithography Hotspot Detection



Layout



Litho simulations



Chip

◆ Lithographic hotspots

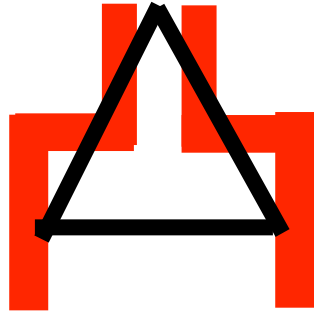
- › What you see (at design) is NOT what you get (at fab)
- › Hotspots mean poor printability
- › Highly dependent on manufacturing conditions
- › Exist after resolution enhancement techniques

◆ Litho-simulations are extremely CPU intensive

- › Full-blown OPC could take a week
- › Impossible to be used in inner design loop

Various Approaches

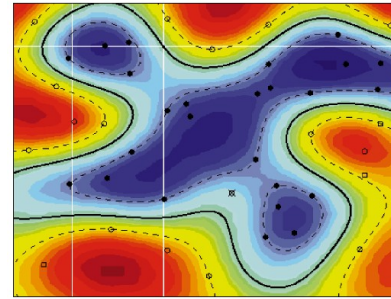
[Xu+ ICCAD07]
[Yao+ ICCAD08,
[Khang SPIE06],
etc.



Pattern/Graph Matching

◆ Pros and cons

- › Accurate and fast for known patterns
- › But too many possible patterns to enumerate
- › Sensitive to changing manufacturing conditions
- › High false-alarms



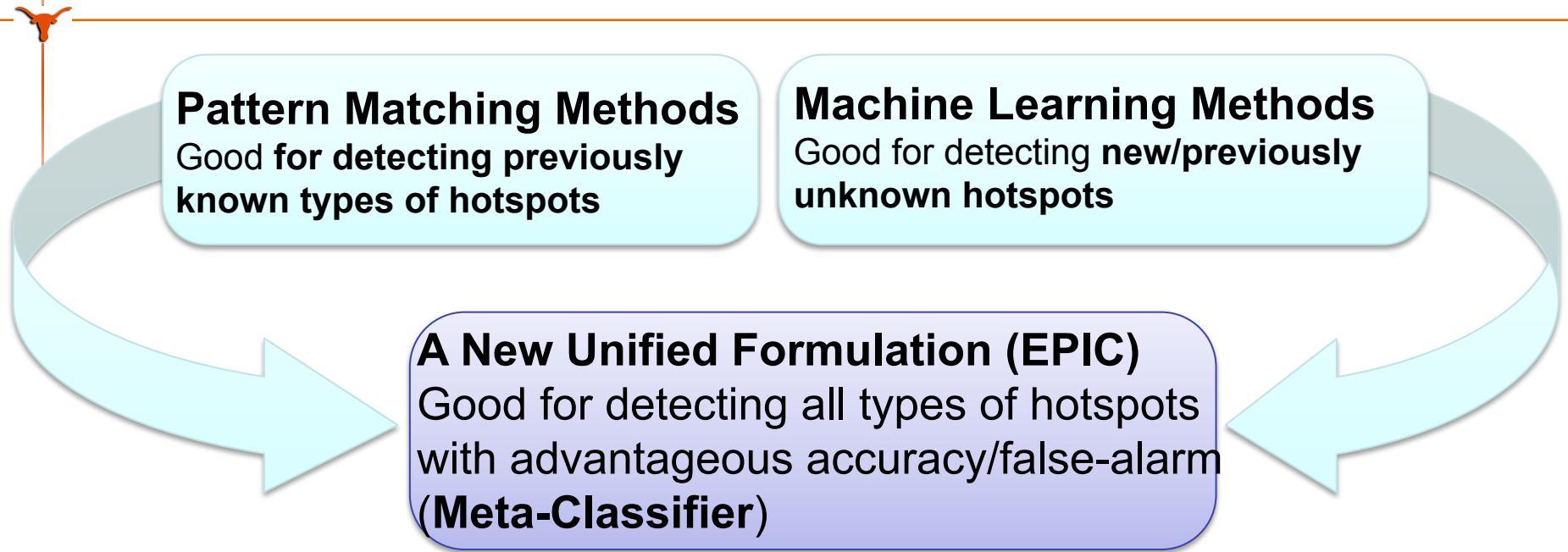
SVM [J. Wu+ SPIE09]
[Drmanac+ DAC09]
Neural Network Model
[Norimasa+ SPIE07][Ding
+ ICICDT09]
Regression Model
[Torres+ SPIE09]

Data Mining/Machine Learning

◆ Pros and cons

- ◆ Good to detect unknown or unseen hotspots
- ◆ Accuracy may not be good for “seen” patterns (cf. PM)
- › Hard to trade-off accuracy and false alarms

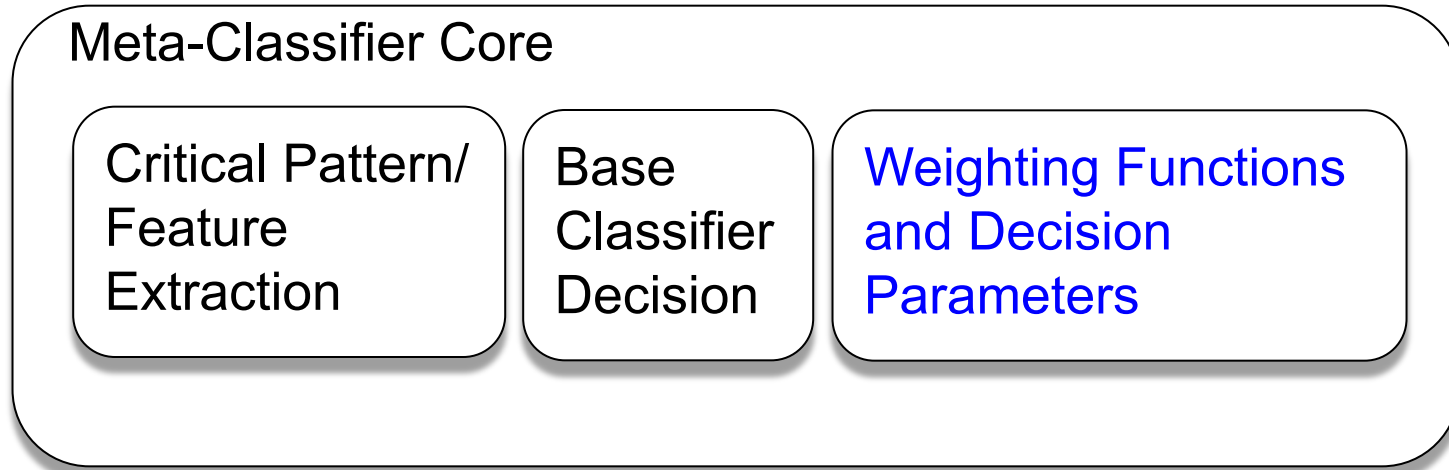
A New Meta-Classification Paradigm



- ◆ Meta-Classification combines the strength of different types of hotspot detection techniques

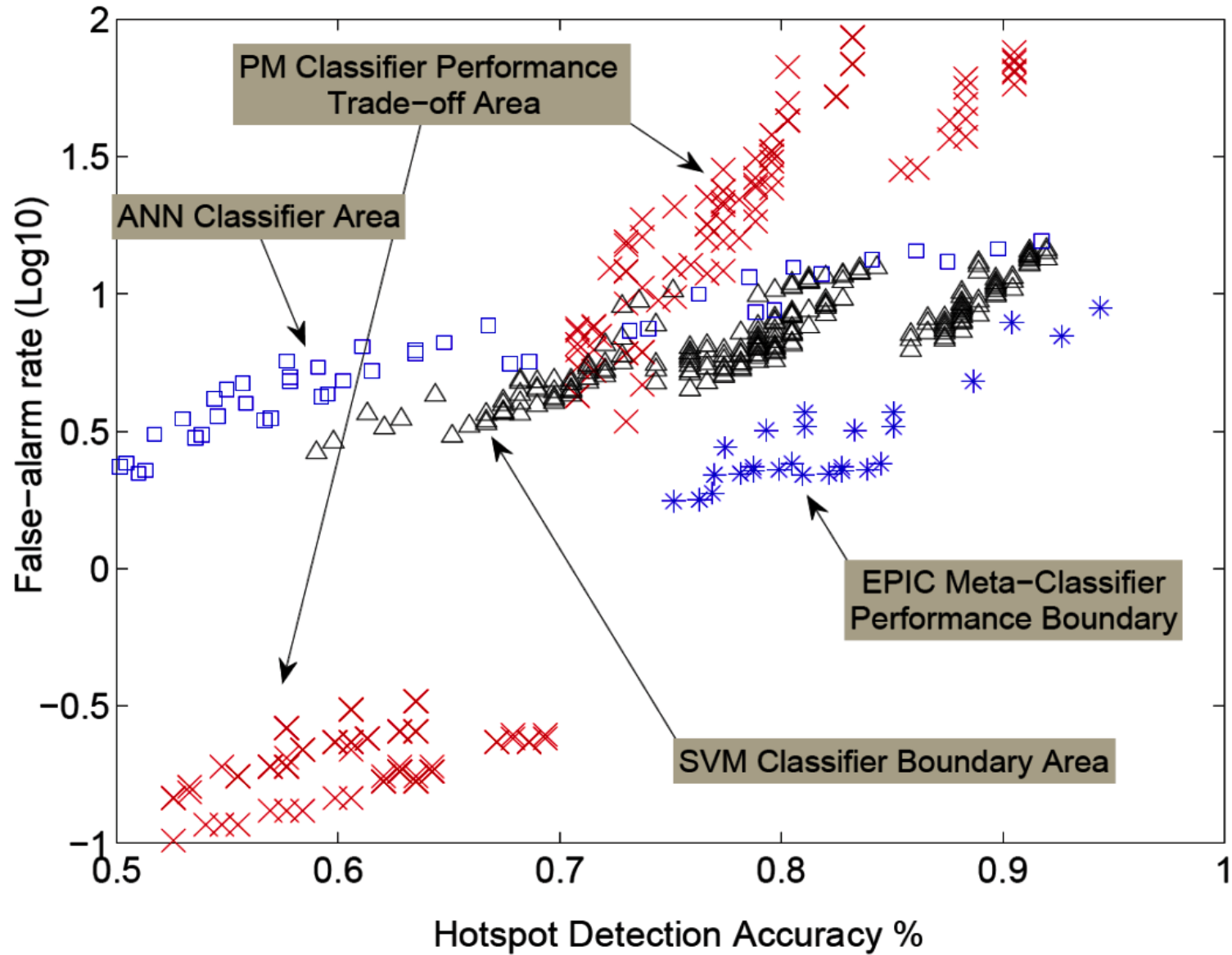
[Ding et al, ASPDAC 2012]

Components of Meta-Classifer Core

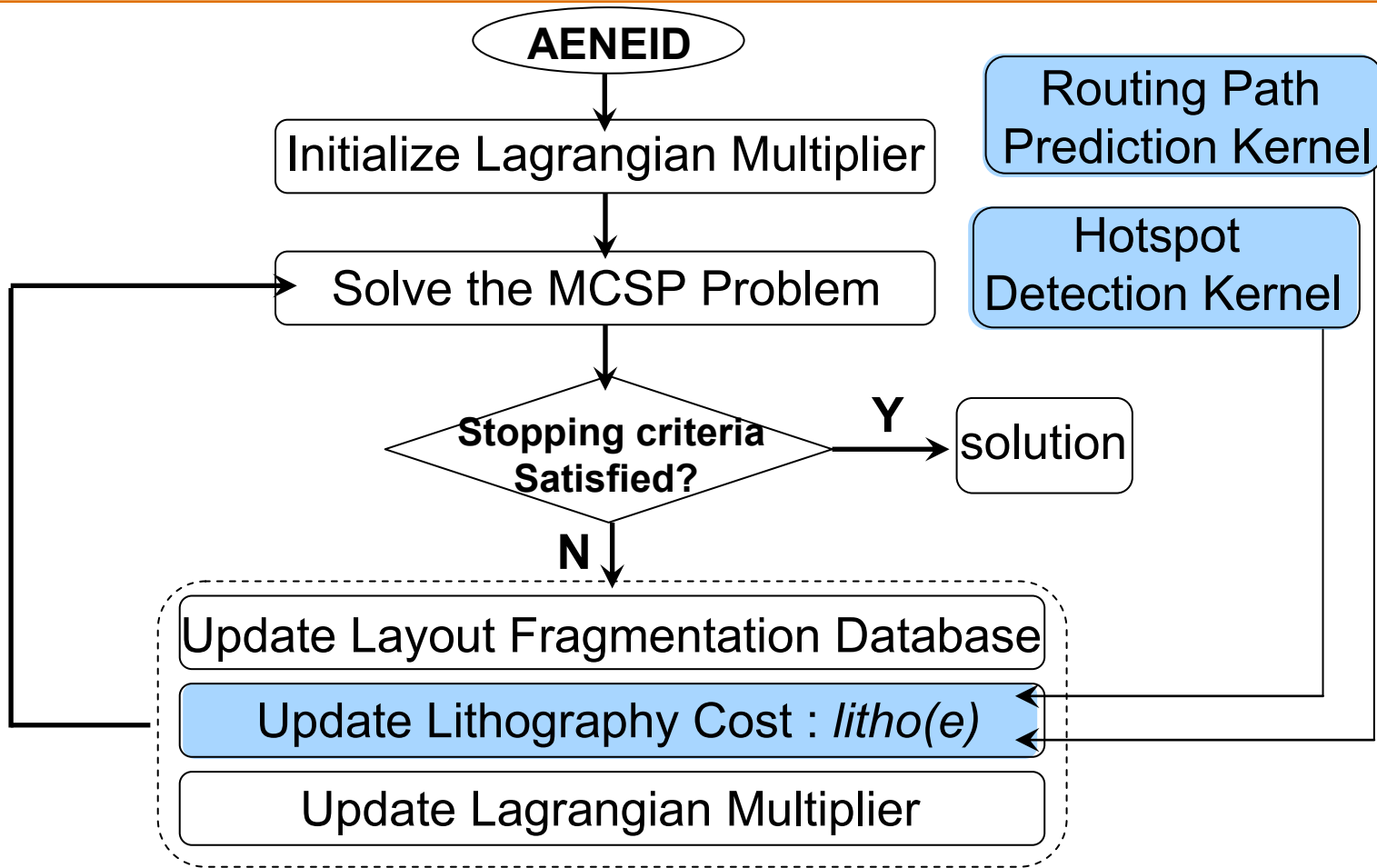


- ◆ Base classifier results are first collected
- ◆ Weighting functions to make the overall meta decision (e.g., quadratic programming)
- ◆ Threshold with accuracy and false-alarm trade-off

False-alarm Rate and Accuracy



AENEID Router [Ding+, DAC'11]



- ◆ Using the machine learning models, we built a new detailed router AENEID to avoid hotspot patterns

Abstraction to Synthesis & Above?



- ◆ Can we further extend the abstraction up to logic synthesis?
 - › Not just lithography hotspot, but other hotspots such as reliability metrics including BTI, oxide breakdown
- ◆ Machine learning to raise the abstraction?
- ◆ NSF/SRC FRS program (started April 1, 2003)
- ◆ NSF/SRC/DFG Cross-Layer Resilience Workshop in Austin, July 11 and 12

The “Moore”, the Merrier!

◆ More Moore

- Nano-Patterning for Extreme Scaling
- Lithography Aware Physical Design

◆ A different kind of “Moore”

- **3D Integration**
- New devices (e.g., nanophotonics) ...

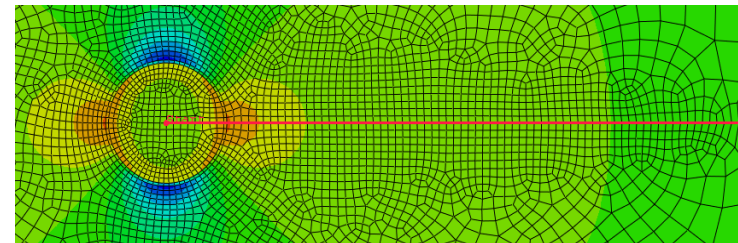
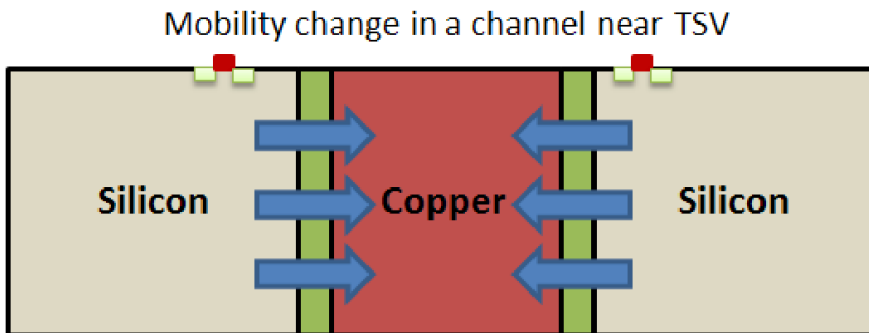
➔ **Need synergistic design and technology co-optimization for cross-layer resilience**

Thermal/Mechanical Stress

Material	CTE in $10^{-6}/K$ at $20^{\circ}C$
Si	3
W	4.5
Cu	17

CTE : Coefficient of thermal expansion

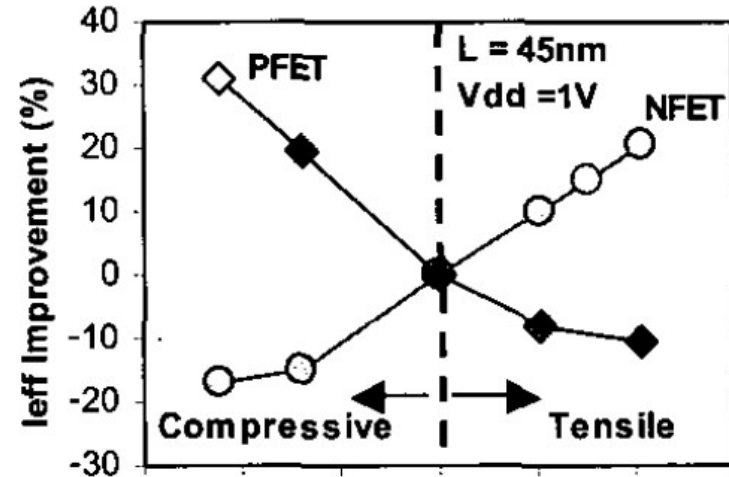
TSV: $250^{\circ}C \sim 400^{\circ}C$ process (Higher than operating temperature)
Since Cu has larger CTE than Si \rightarrow tensile stress in Si near TSV.



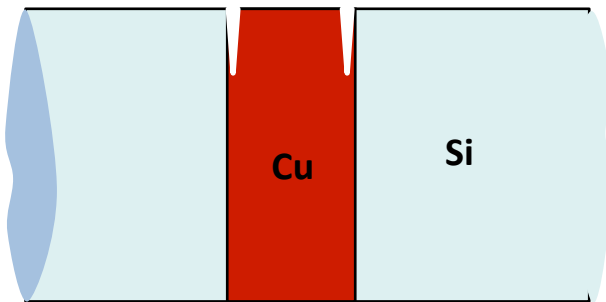
Stress => Variability/Reliability

- ◆ Systematic Variations

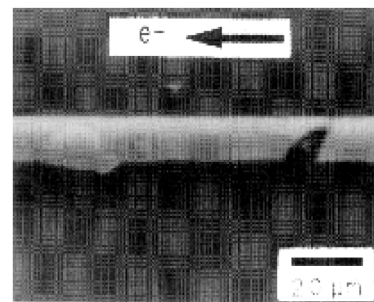
- › Mobility
- › Timing



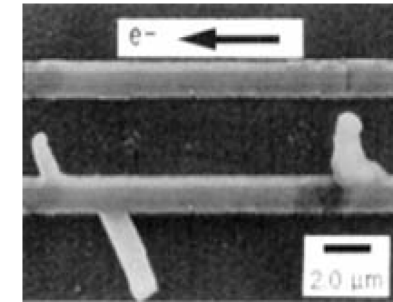
- ◆ Reliability (interfacial crack, EM, etc.)



Interfacial Crack



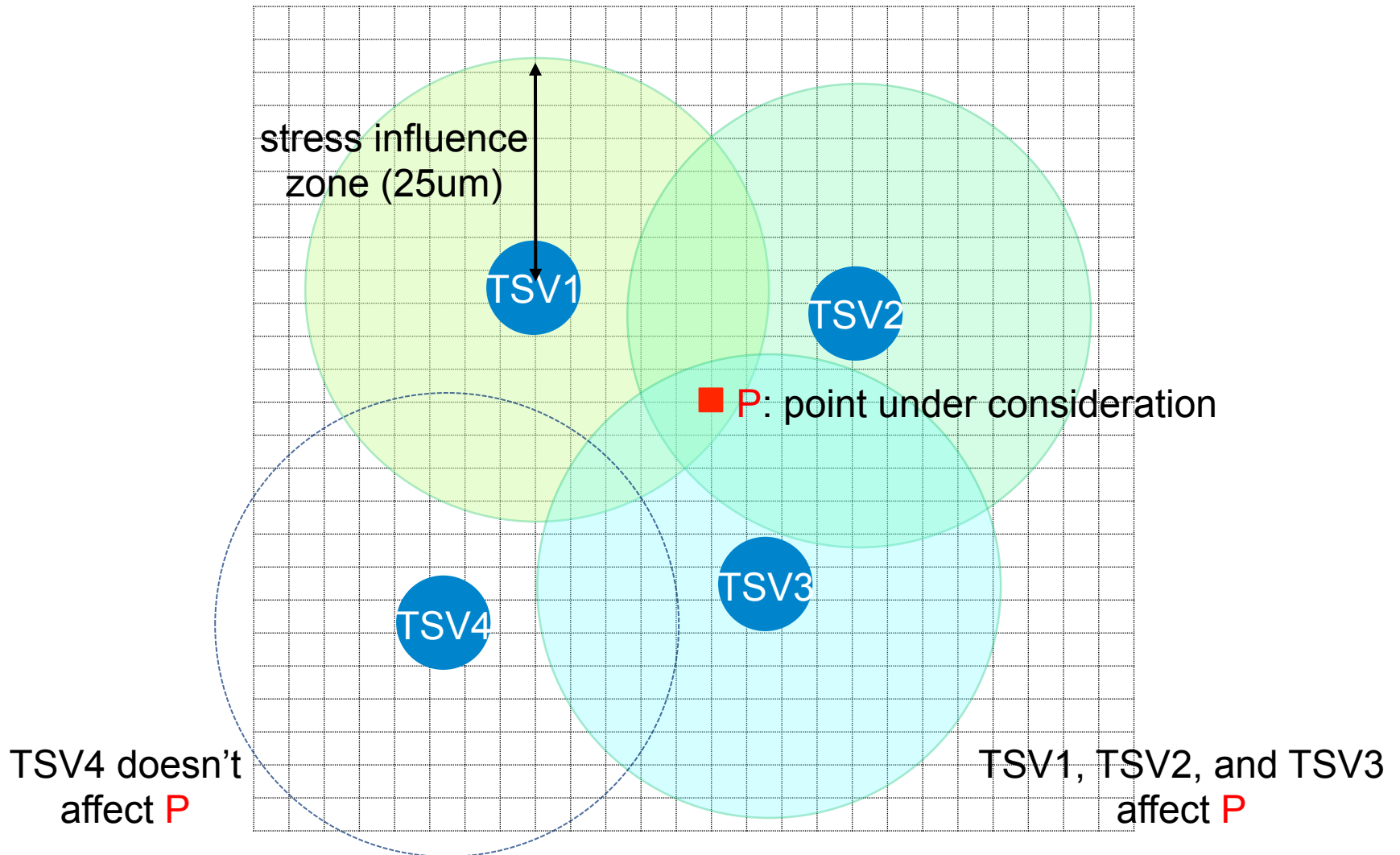
Electromigration Effect – Open



Electromigration Effect – Short

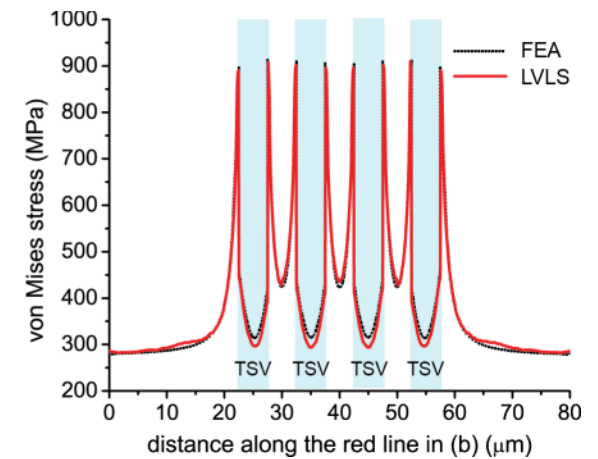
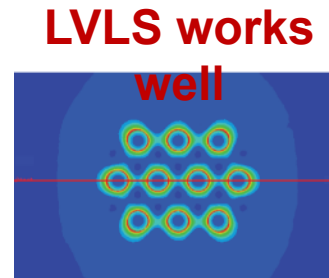
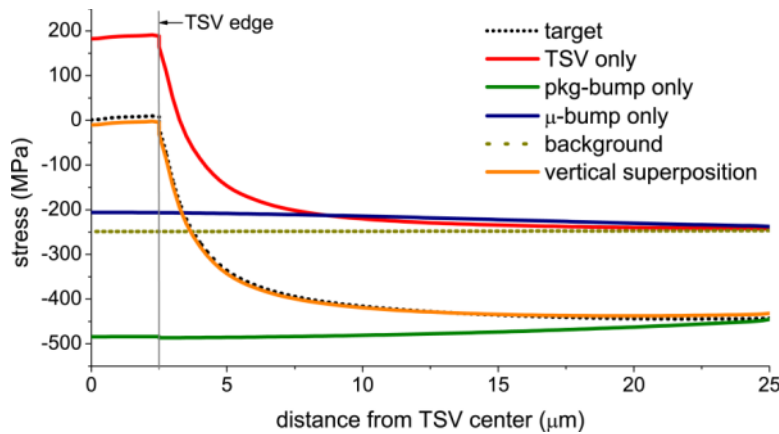
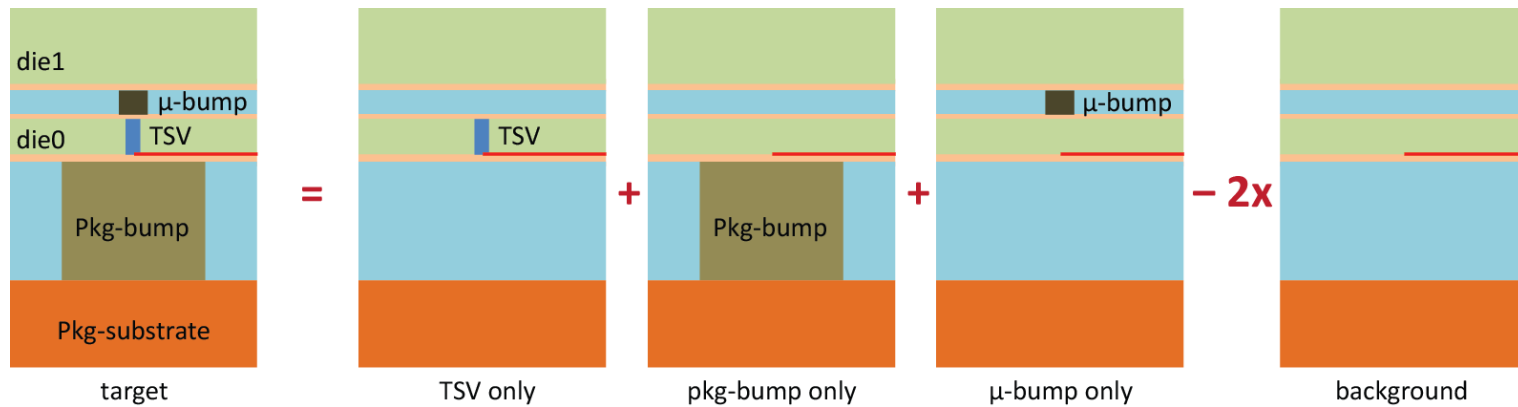
Lateral Linear Superposition [ECTC'11, DAC'11]

- ◆ Full-chip stress analysis considering multiple TSVs



(Lateral &) Vertical Superposition

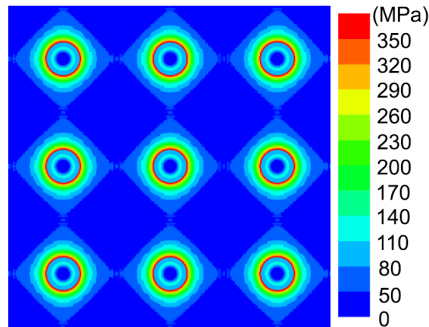
- ◆ Stress components are added up “vertically”



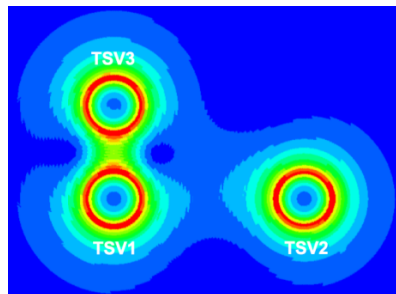
Reliability/Variability Impact of Stress

1. Von Mises Reliability

- Von Mises Yield is function of stress tensor



(a) Von Mises stress with TSV array

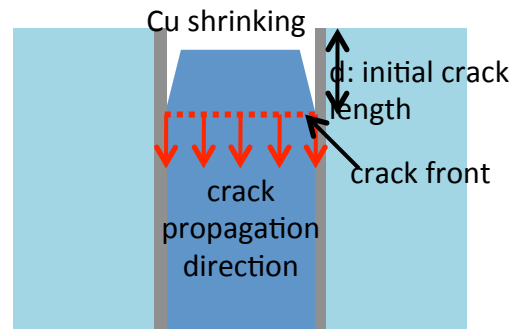


(b) Von Mises stress with three TSVs

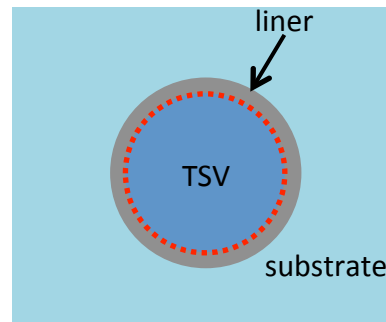
[J. Mitra et al., ECTC'11]

2. Crack: Energy release rate (ERR)

- TSV stress affects ERR of TSV structure
→ aggravate crack



(a) Side view

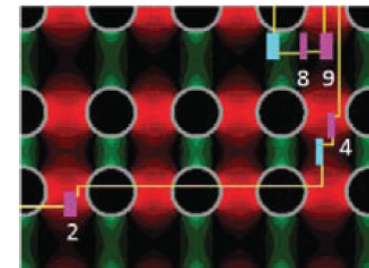


(b) Top view

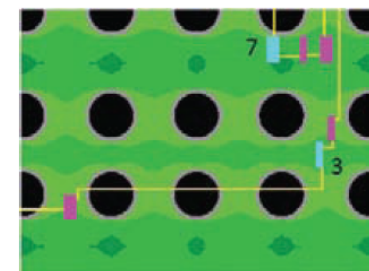
[M. Jung et al., ICCAD'11]

3. Mobility/ V_{th} variation of MOS

- TSV stress changes mobility of hole/electron
→ timing, V_{th} variation



(a) Hole mobility variation



(b) Electron mobility variation

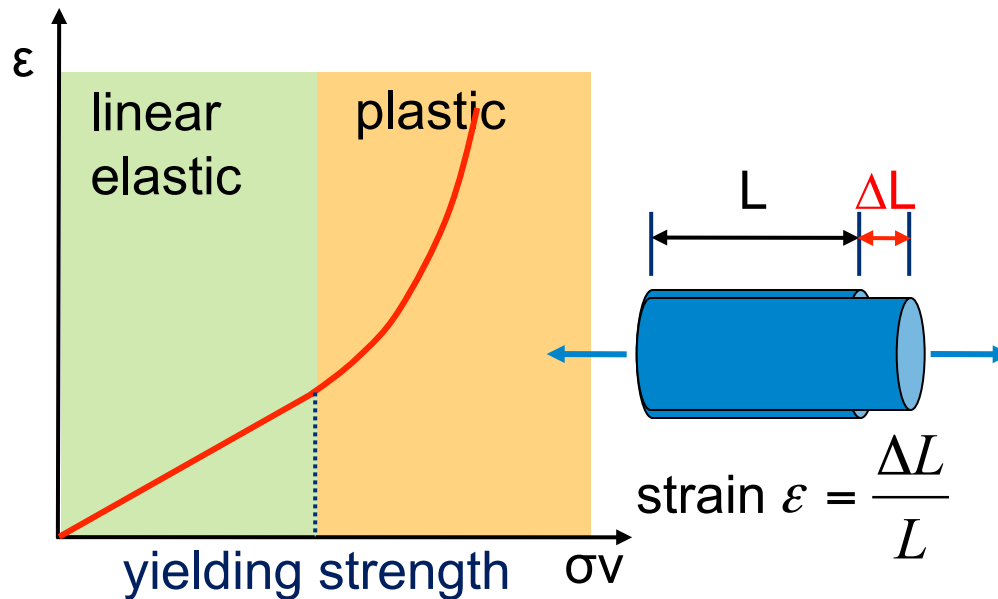
[J. Yang et al., DAC'10]

From Stress to Reliability

◆ Von Mises Reliability Metric

$$\sigma_v = \sqrt{\frac{(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2 + 6(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{zx}^2)}{2}}$$

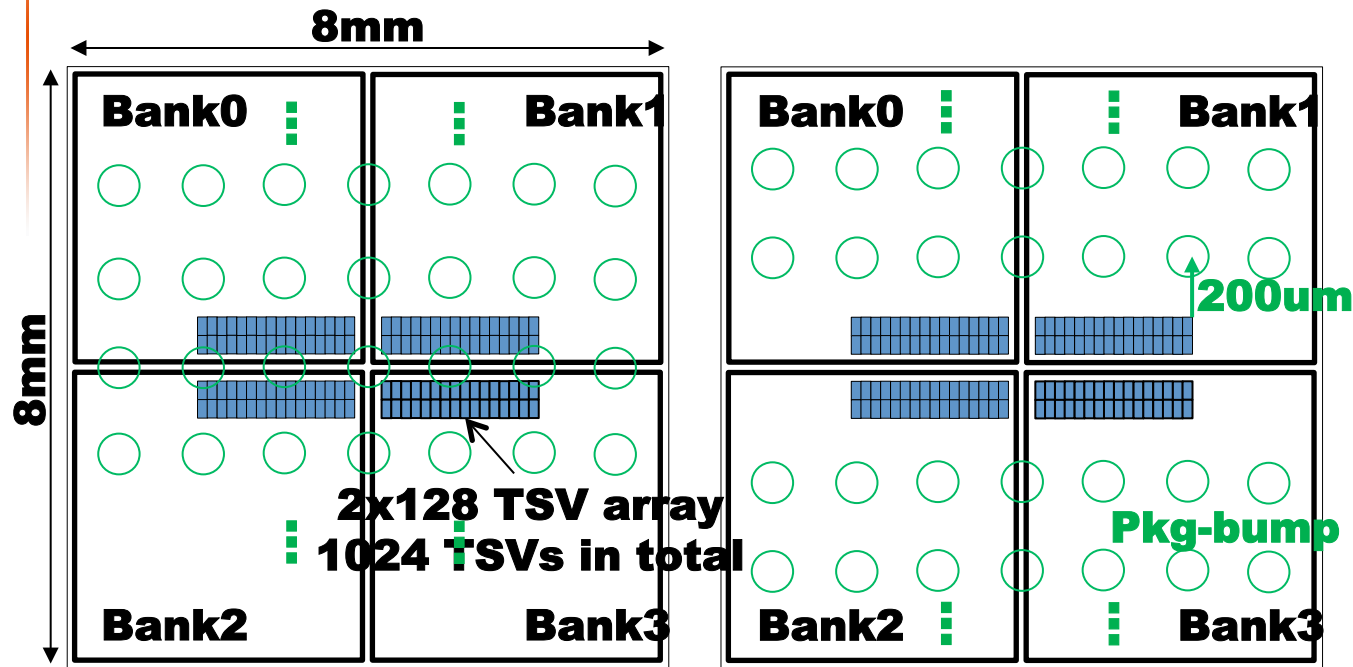
◆ Physical meaning



If $\sigma_v >$ yielding strength, deformation will be permanent and non-reversible

Yielding strength
- Cu: 225 ~ 600 MPa
- Si: 7,000 MPa

Wide I/O 3D DRAM

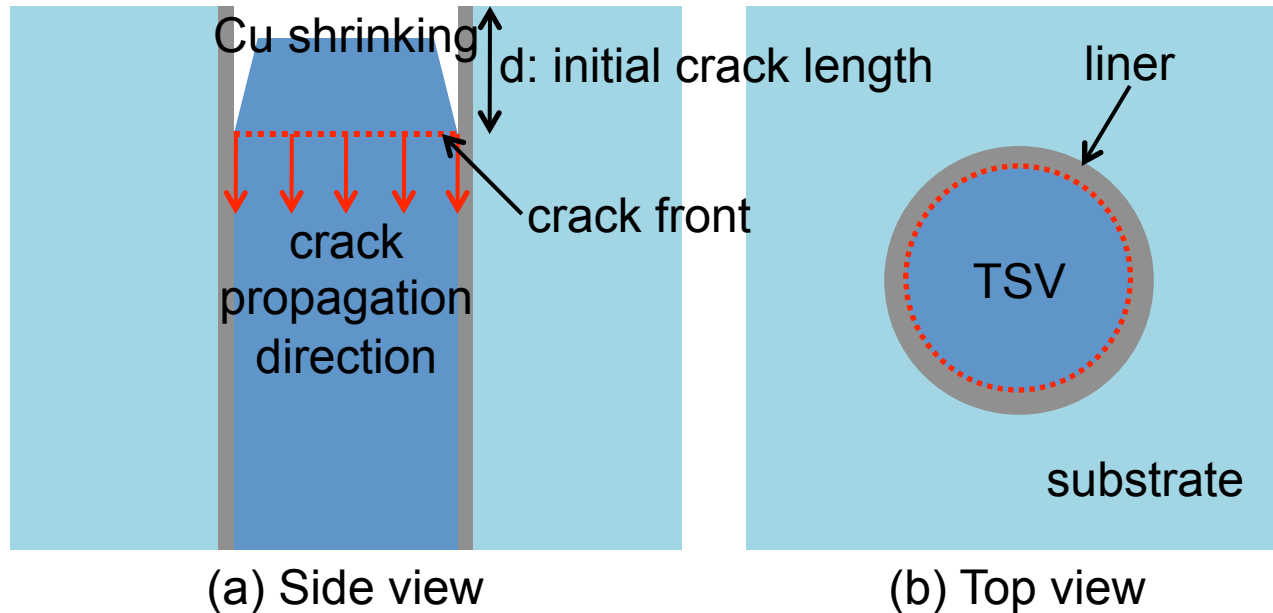


case (b) shows that chip/package co-design can greatly reduce mechanical reliability problem in TSV-based 3D ICs

(a) Pkg-bumps are placed underneath TSV arrays (b) Pkg-bumps are placed 200um apart from TSV arrays

case	von Mises stress distribution (MPa)				
	780-810	810-840	840-870	870-900	900-930
(a)	30	114	52	220	608
(b)	182	842	0	0	0

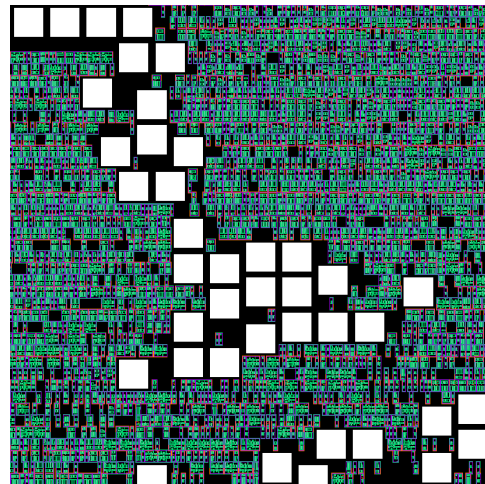
TSV Interfacial Crack



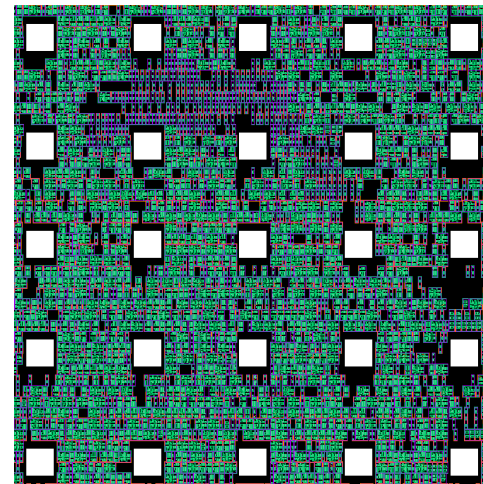
- **Cu shrinks faster than Si under negative thermal load ($\Delta T = -250^{\circ}\text{C}$)**
- **Model through Energy Release Rate (ERR)**
- **Full chip model with design-of-experiments of different layout styles and multiple TSV structures**

Full-Chip Crack Analysis and Study

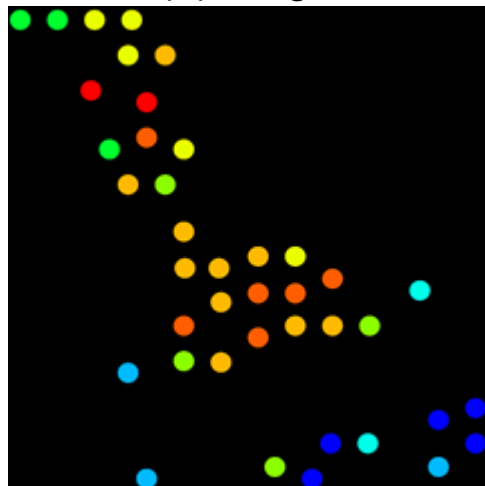
◆ Regular vs. irregular TSV arrays



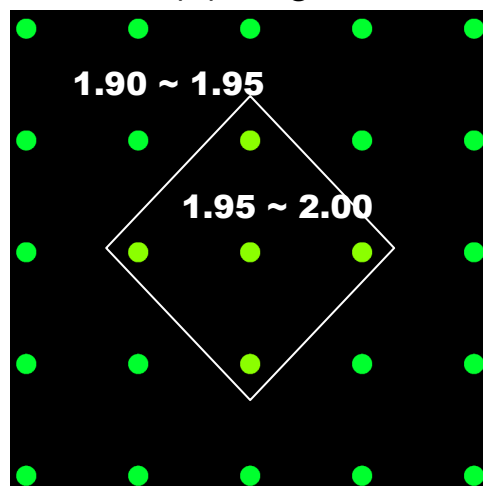
(a) IrregA



(b) RegA



(c) ERR map of IrregA



(d) ERR map of RegA

100μm

ERR
(J/m²)

2.15
2.10
2.05
2.00
1.95
1.90
1.85
1.80

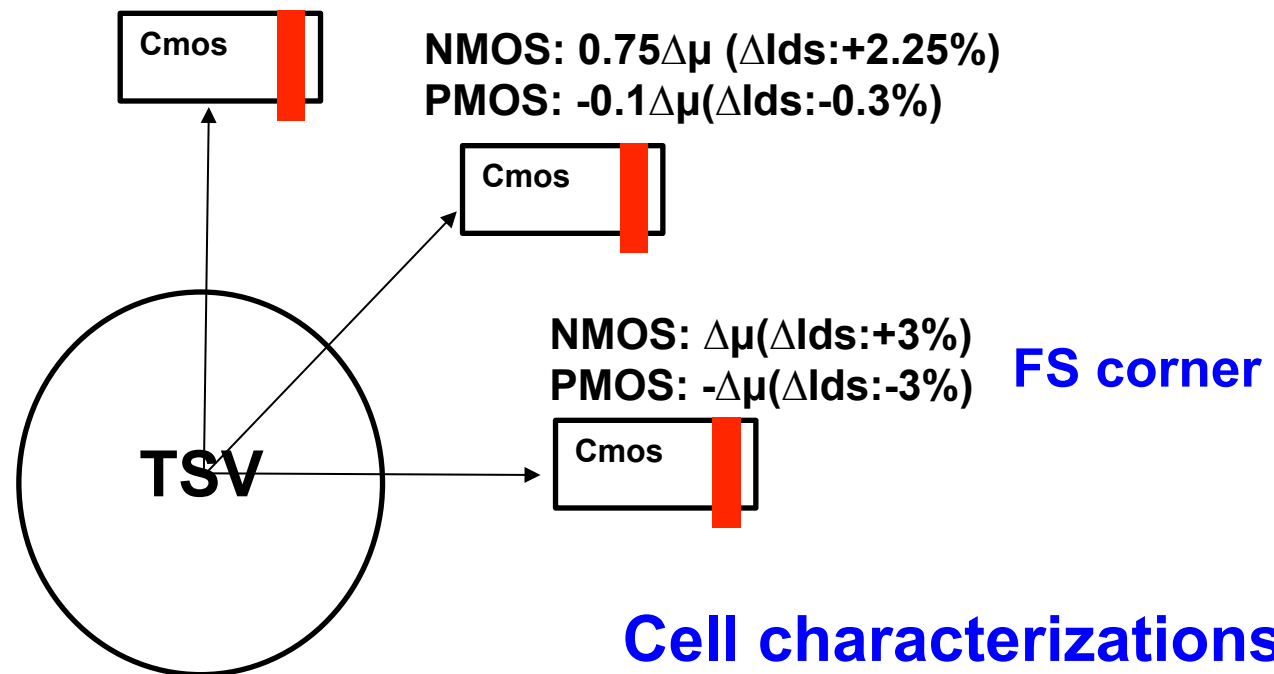
Stress Effect on Mobility & Current

CMOS (Stress: 200MPa, R=r)

[Yang+, DAC' 10]

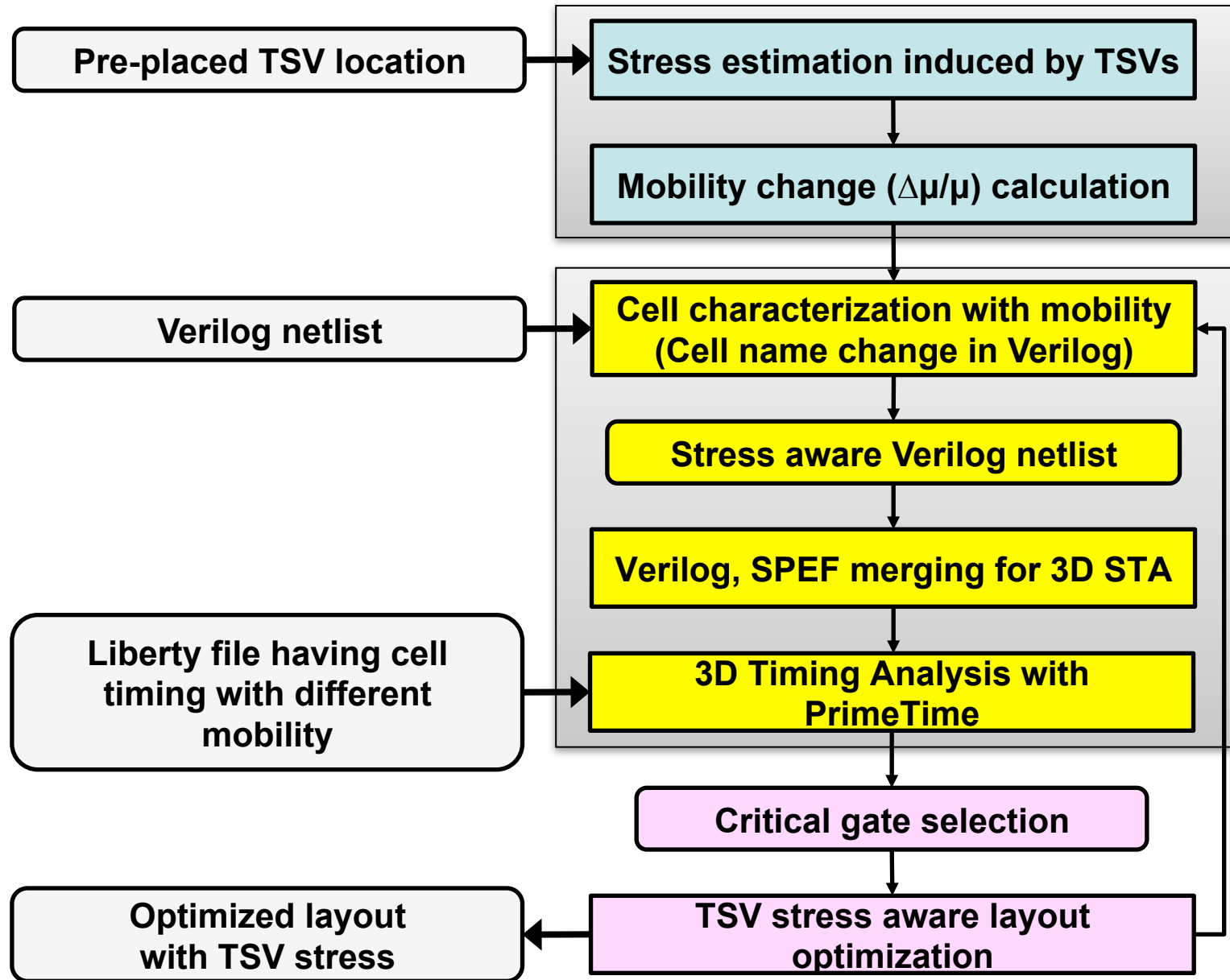
NMOS: $0.5 \Delta\mu$ (ΔI_{ds} :+1.5%)

PMOS: $0.6\Delta\mu$ (ΔI_{ds} :+1.8%)



Cell characterizations based on distance and orientation are needed

Stress Aware Design Flow [Yang+, DAC' 10]



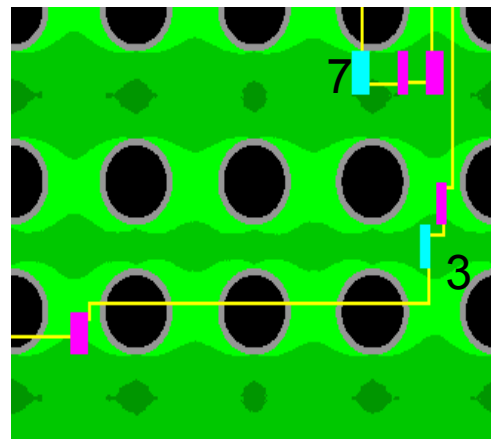
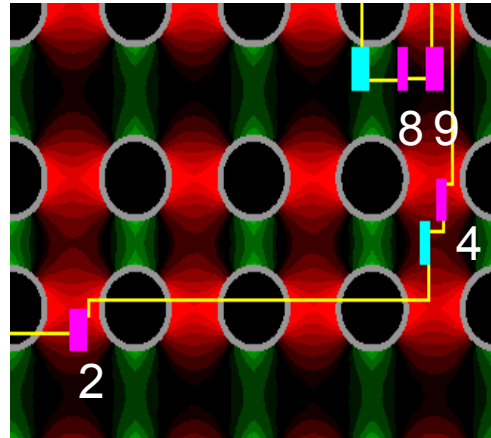
Stress-Aware ECO



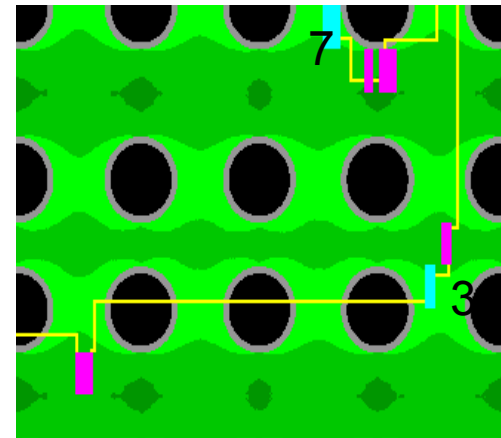
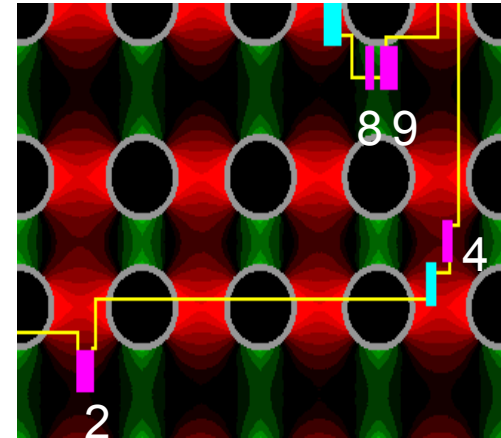
Rising critical optimization with hole contour

Falling critical optimization with electron contour

Original cell placement



After cell perturbation



The “Moore”, the Merrier!

◆ More Moore

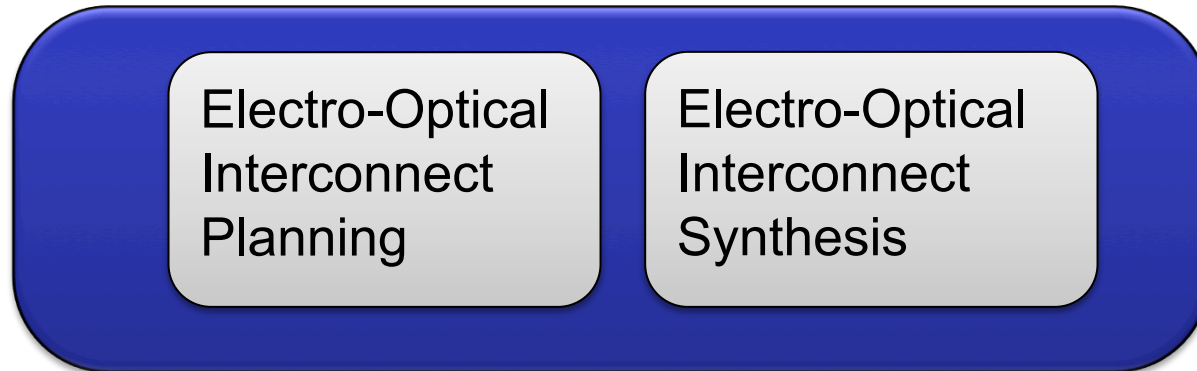
- Nano-Patterning for Extreme Scaling
- Lithography Aware Physical Design

◆ A different kind of “Moore”

- 3D Integration
- **New devices (e.g., nanophotonics) ...**

➔ Need synergistic design and technology co-optimization for cross-layer resilience

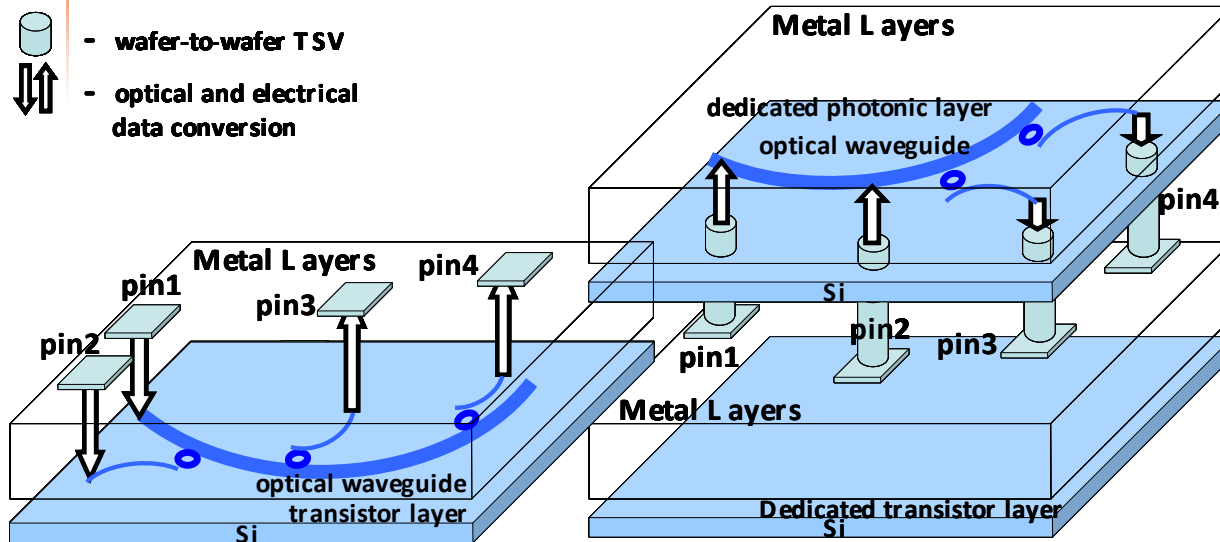
Nanophotonics On-chip Integration



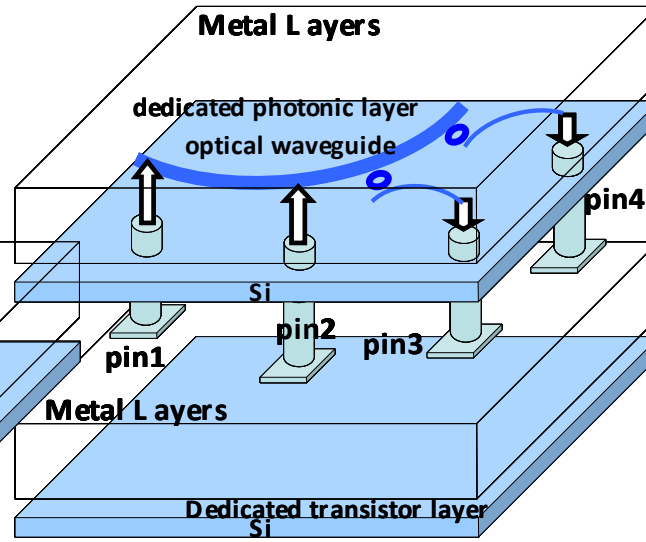
- ◆ Holistic Optical Interconnect Planning and Synthesis
 - › Co-design and optimization with electrical interconnect
 - › Optical interconnect library (OIL)) [Ding+, DAC'09, SLIP'09, and available <http://www.cerc.utexas.edu/~ding/oil.htm>]
 - › WDM, partitioning, routing, ...
- ◆ Nanophotonics is a very active field
- ◆ Many new research problems for CAD community!

Case Study 1: O-Router [Ding et al, DAC'09]

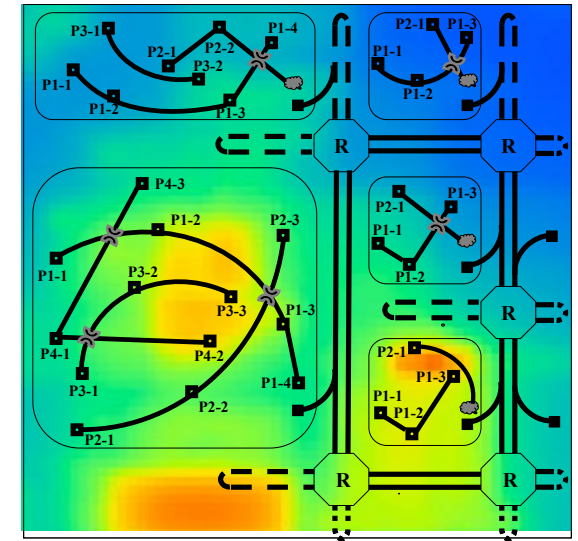
- wafer-to-wafer TSV
- optical and electrical data conversion



(a)



(b)



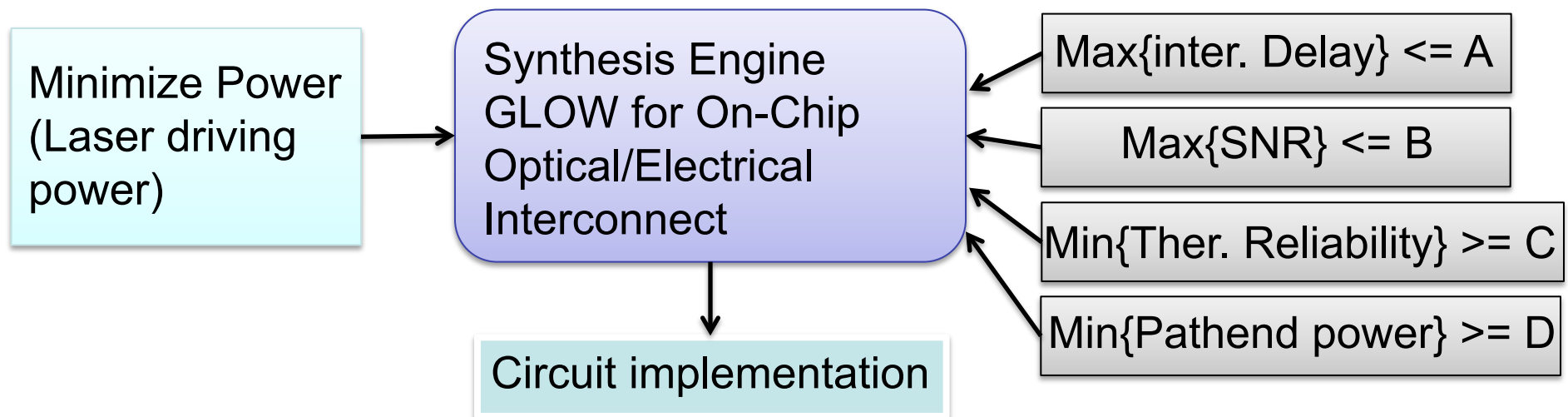
(c)

- ◆ Objectives: performance (throughput, latency, power), cost (\$\$, economics)
- ◆ Constraints (SNR, signal integrity, reliability, system-level reqs.)

Case Study 2: GLOW

[Ding et al, ASPDAC'12]

- ◆ Global router for low-power **thermal-reliable** optical interconnect synthesis using Wavelength Division Multiplexing (WDM)



Conclusion

- ◆ Optical lithography still pushing ahead for 14nm, 11nm, 7nm → extreme scaling
 - › Multiple patterning, EUV, DSA, and hybrid lithography
- ◆ Design enablement with lithography capability co-optimization from mask to physical synthesis (and higher level, e.g., NSF/SRC FRS)
 - › Cross-layer resilience
- ◆ Horizontal scaling → Vertical scaling: 3D-IC
 - › Reliability/Variability issues
- ◆ New material/devices → new CAD paradigms and tools

Acknowledgment

- ◆ Support/collaboration from NSF, SRC, NSFC, Sematch, IBM, Intel, Oracle, Fujitsu, Qualcomm, Synopsys, Mentor Graphics, Toshiba, ...
- ◆ The materials in this talk include results from many former/current PhD students at UTDA
 - › They are the ones who did the real work!
- ◆ Collaborators
 - › DFM: IBM, Intel, Globalfoundries, Mentor, Synopsys, etc.
 - › 3D-IC: Prof. Sung Kyu Lim's group at Georgia Tech
 - › Optical: Prof. Ray Chen's group at UT Austin