Electromigration Study for Multi-scale Power/Ground Vias in TSV-based 3D ICs

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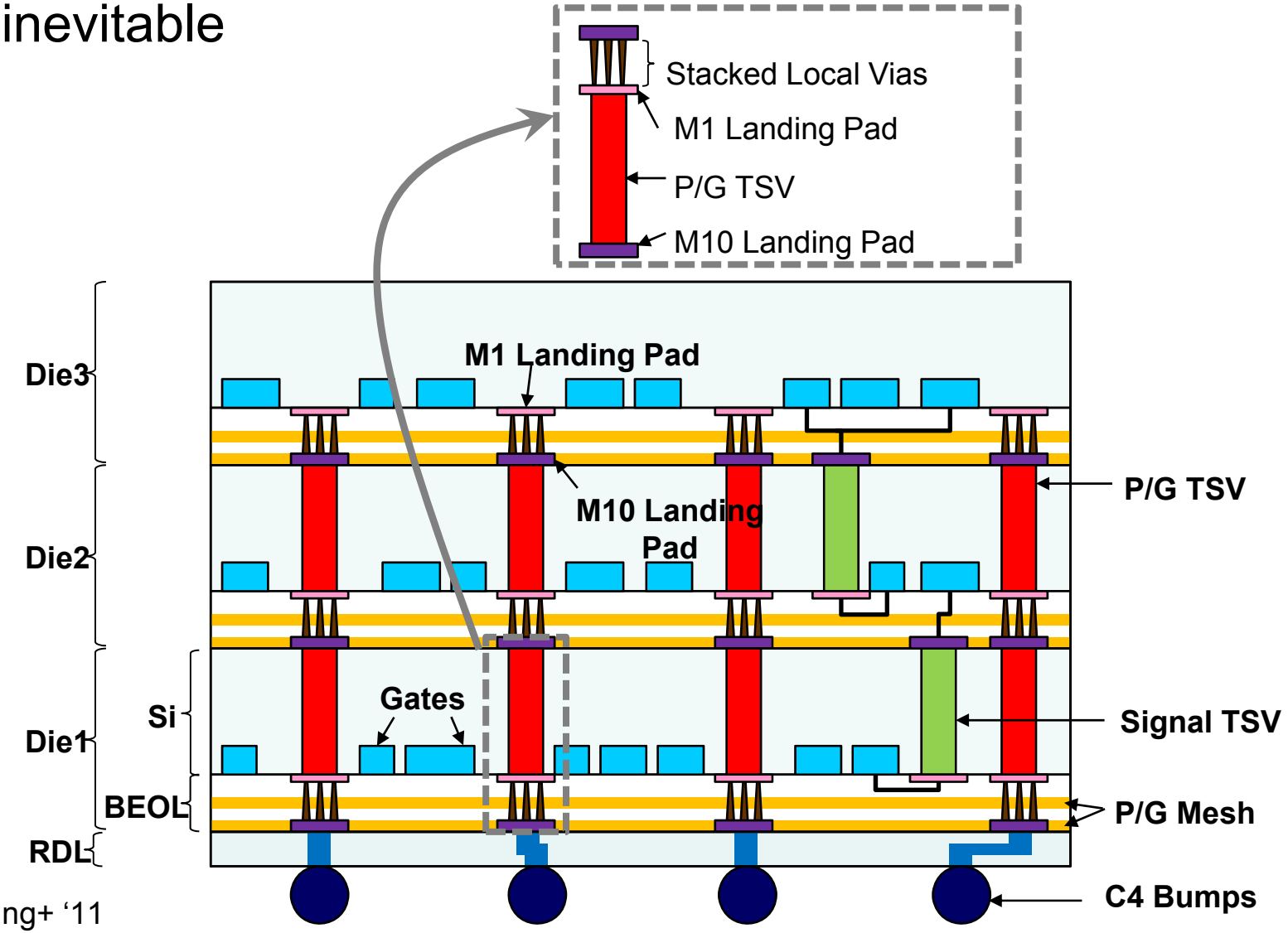
Outline

- Introduction
- EM Modeling for Multi-scale P/G Vias
- Study of EM of Multi-scale P/G Vias
- Electromigration of Full-chip 3D PDNs with Multi-scale Vias
- Summary

Power/Ground Network in 3D ICs

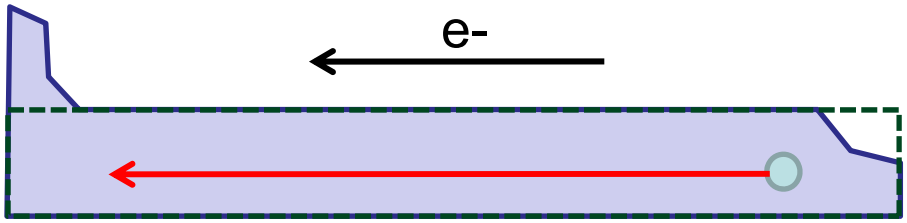
- With via-first/middle TSVs, multi-scale vias (MSV) are inevitable



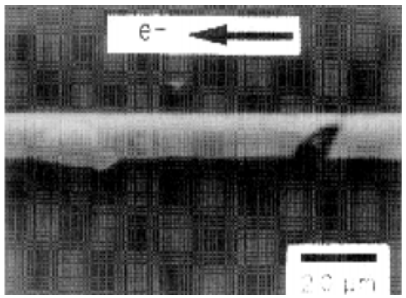
[1] M. Jung+ '11

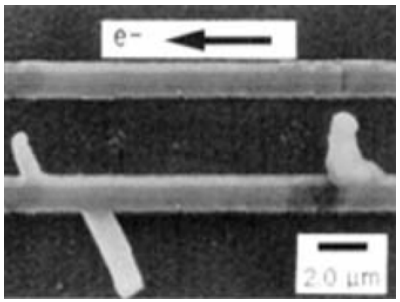
Electromigration

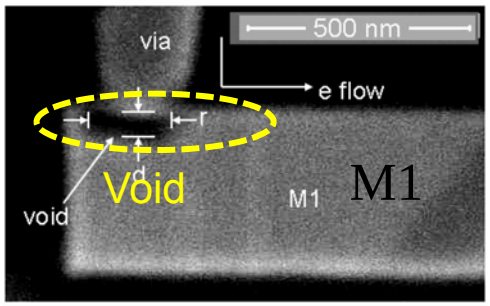
- Electromigration (EM):
  - Atomic diffusion due to high current density
  - Also depends on temperature and stress
  - Can generate voids, hillocks

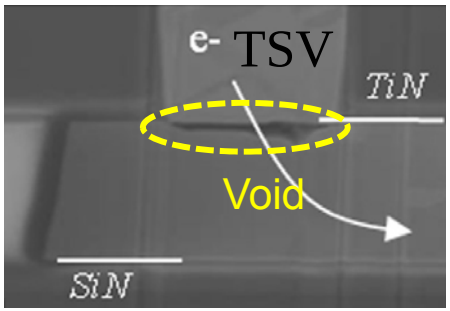


metal atom movement





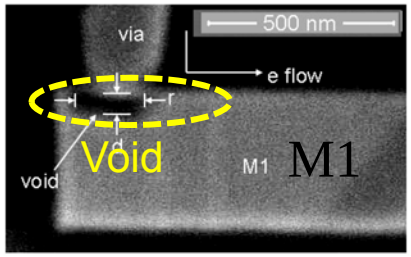


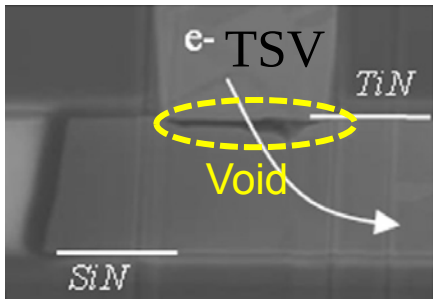


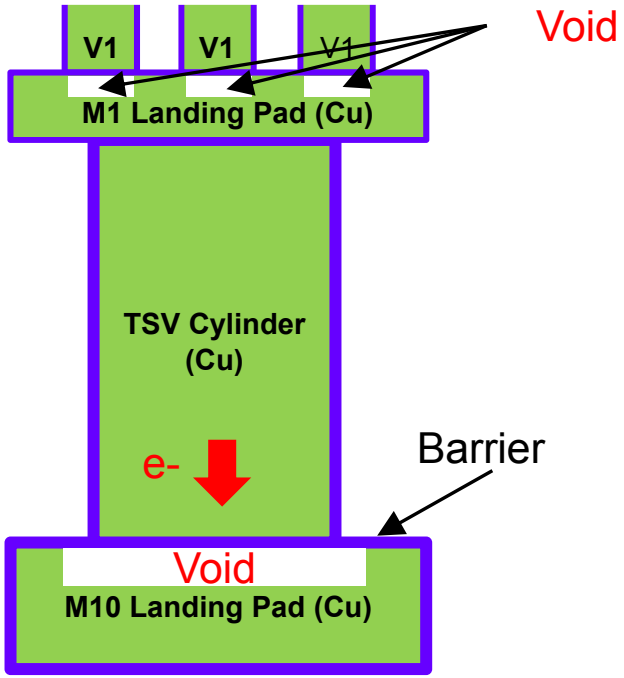
[2] D. Rittman '04 [3,4] A. Roy '11, T. Frank+ '13

EM in Multi-Scale Vias (MSV)

- Electromigration (EM) can generate voids under the local via (V1) and TSV cylinder
- Voids change the resistance of MSV structure
  - Cause current imbalance of P/G network
- EM 'failure' criteria: 10% resistance increase







[3] T.Frank+ '13
[4] A. Roy '11

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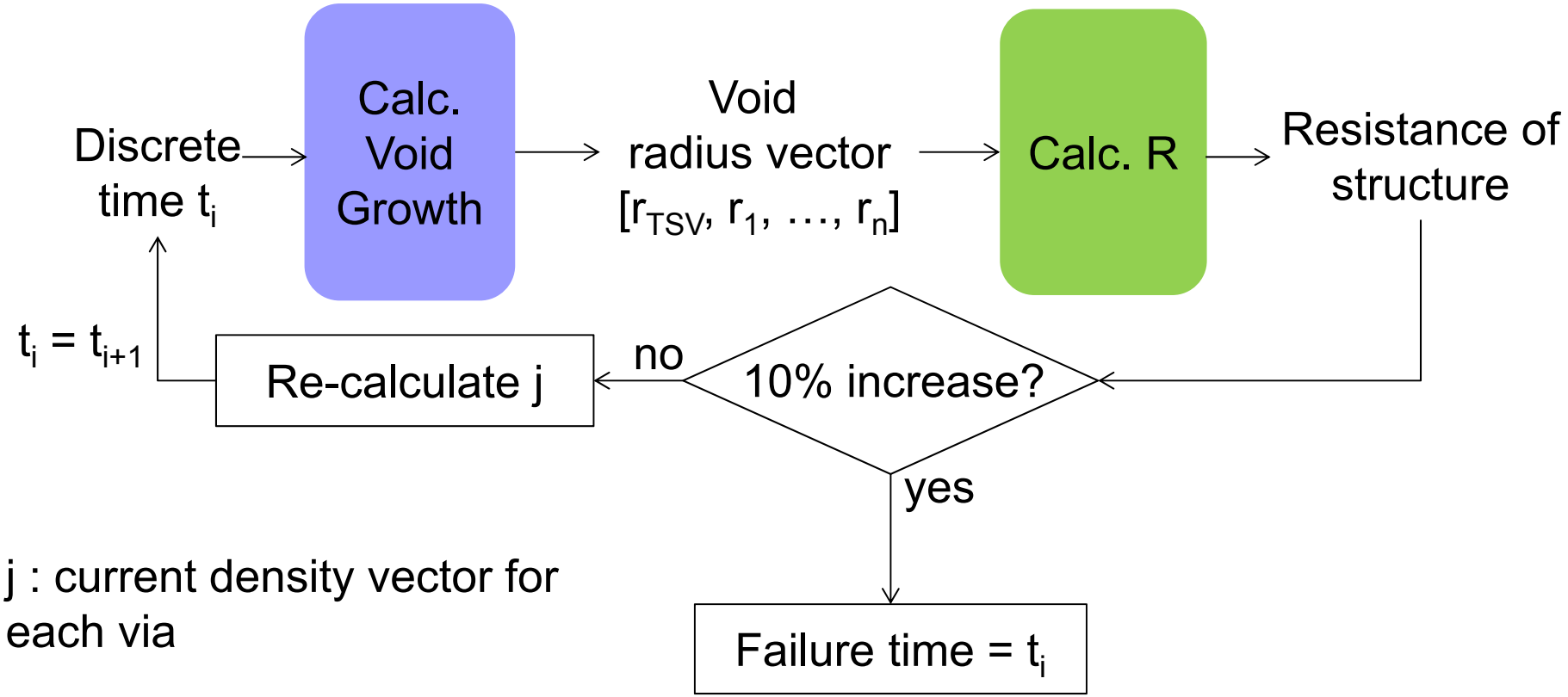
Algorithm for Modeling EM Failure

- Step 1: Calculate void growth for local vias and a TSV
- Step 2: Calculate resistance of local vias, TSV and MSV
- Increase time, iterate until reach the critical resistance
- Implemented with Python programming language



j : current density vector for each via

Step 1: Calculation of Void Growth

- Vacancy flux equations for EM modeling

$$\vec{J_v} = -D_v \left(\nabla C_v - C_v \frac{eZ^*}{kT} \rho \vec{j} + C_v \frac{f\Omega}{kT} \nabla \sigma \right)$$

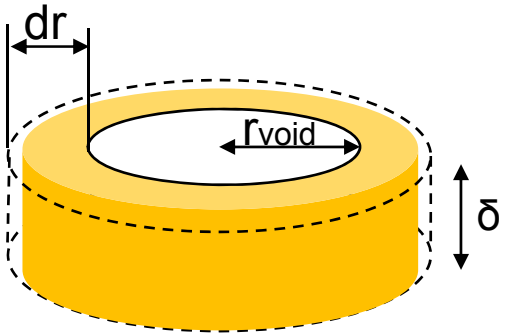
$$D_v = D_o \cdot exp(\frac{-Ea}{kT})$$

- Cylindrical void growth model

$$dV = \alpha f \Omega A J_v dt = 2\pi \delta r_{void} dr$$

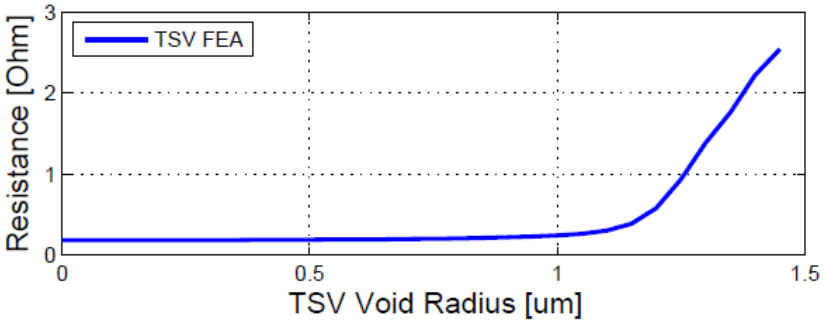
$$dr = \frac{\alpha f \Omega A J_v dt}{2\pi \delta r_{void}}$$

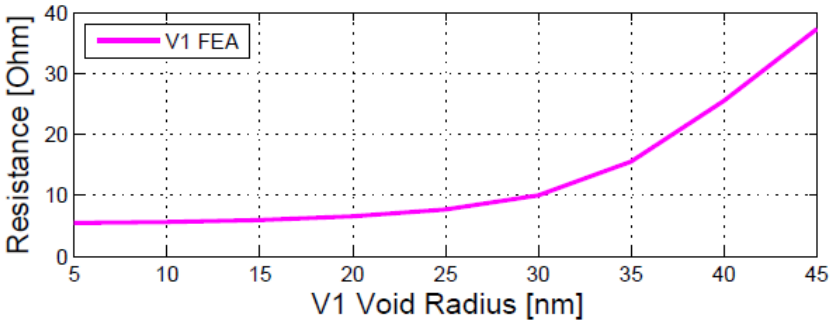
$\overrightarrow{J_v}$: total vacancy flux
c_v : vacancy concentration
$\overrightarrow{j}$: current density vector
σ : hydrostatic stress
T : temperature

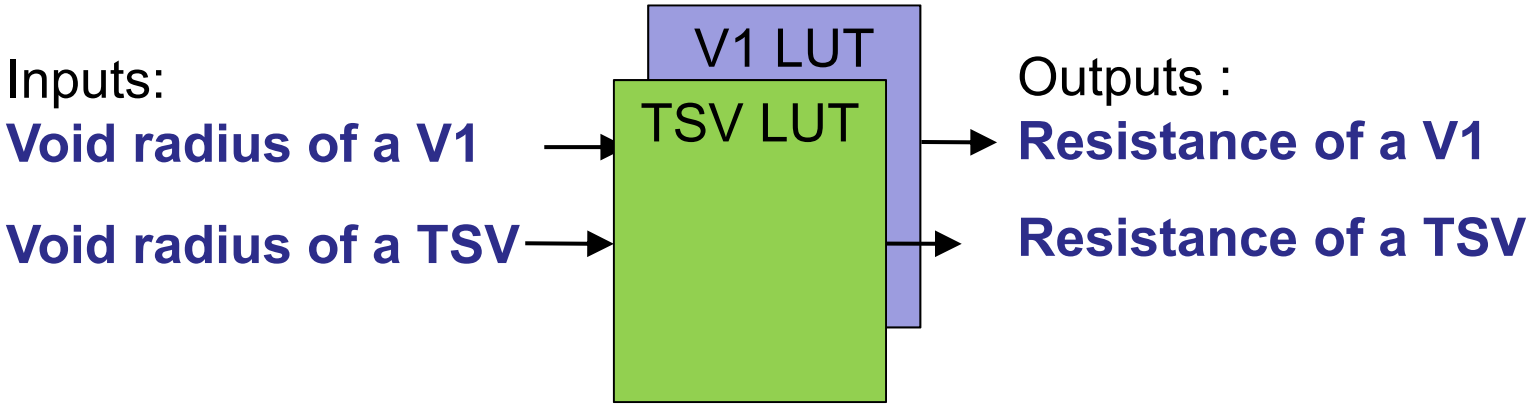


Step 2: Calculation of Resistance

- Generate look-up tables (LUTs) with FEA simulation
  - Input: radius of void, output: resistance of the structure
  - 2 LUTs required: 1 for TSV, 1 for local via

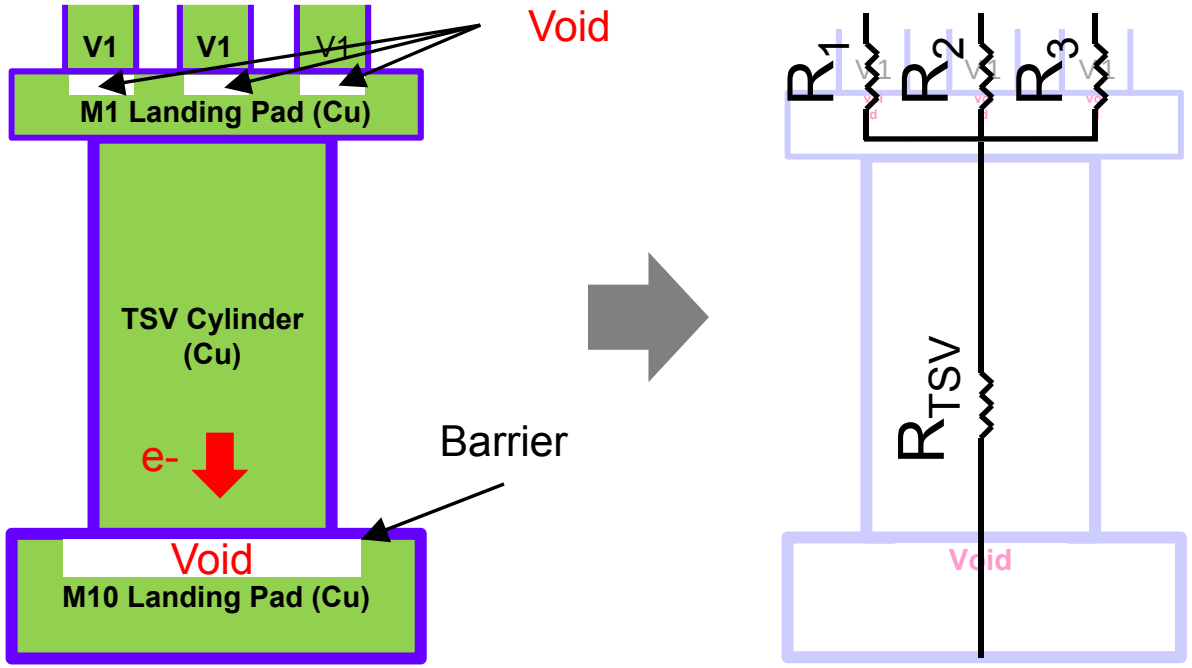






Step 2: Calculation of Resistance

- Resistance of the entire MSV can be calculated with resistance model



$$R_{MSV} = \frac{1}{\sum_{i=1}^{n} \frac{1}{R_i}} + R_{TSV} \ , i \in [1, n]$$

Algorithm for Modeling EM Failure

- Step 1: Calculate void growth for local vias and a TSV
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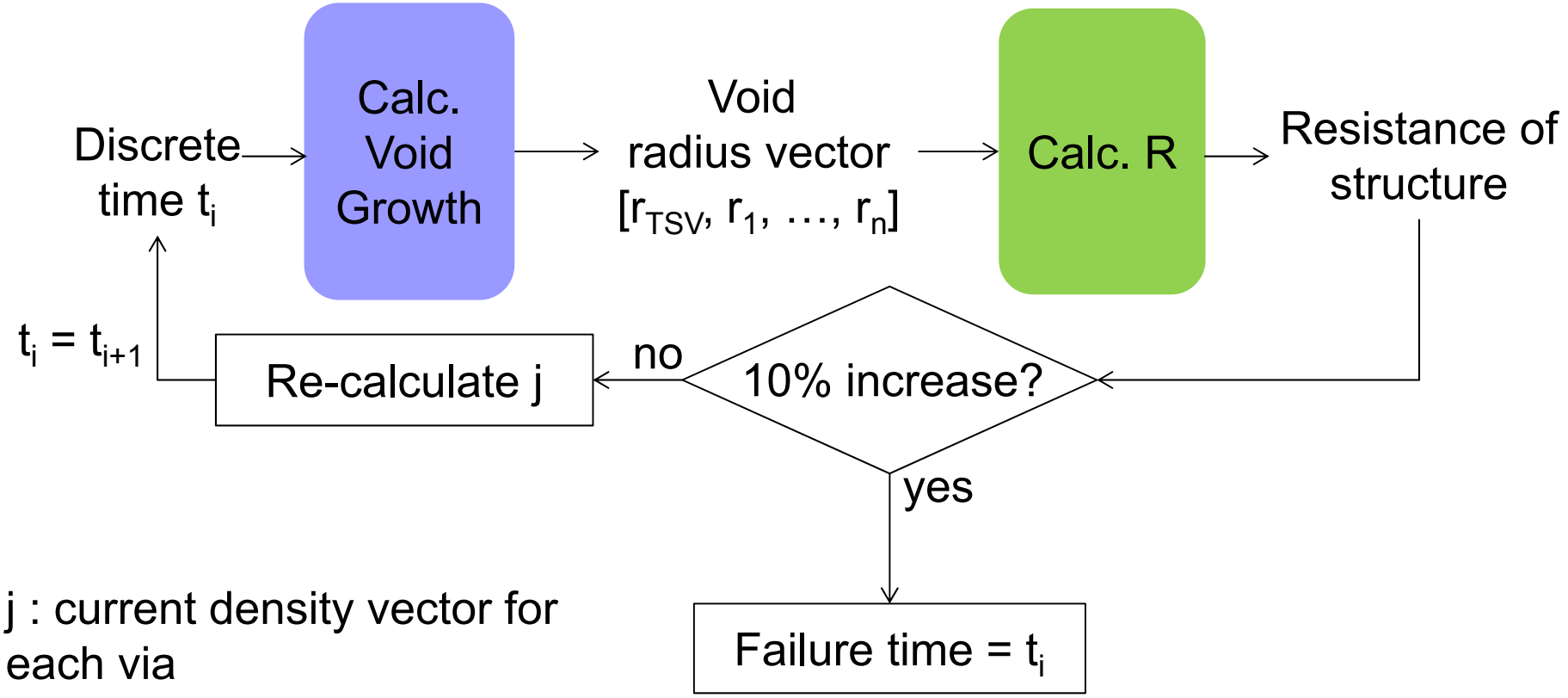
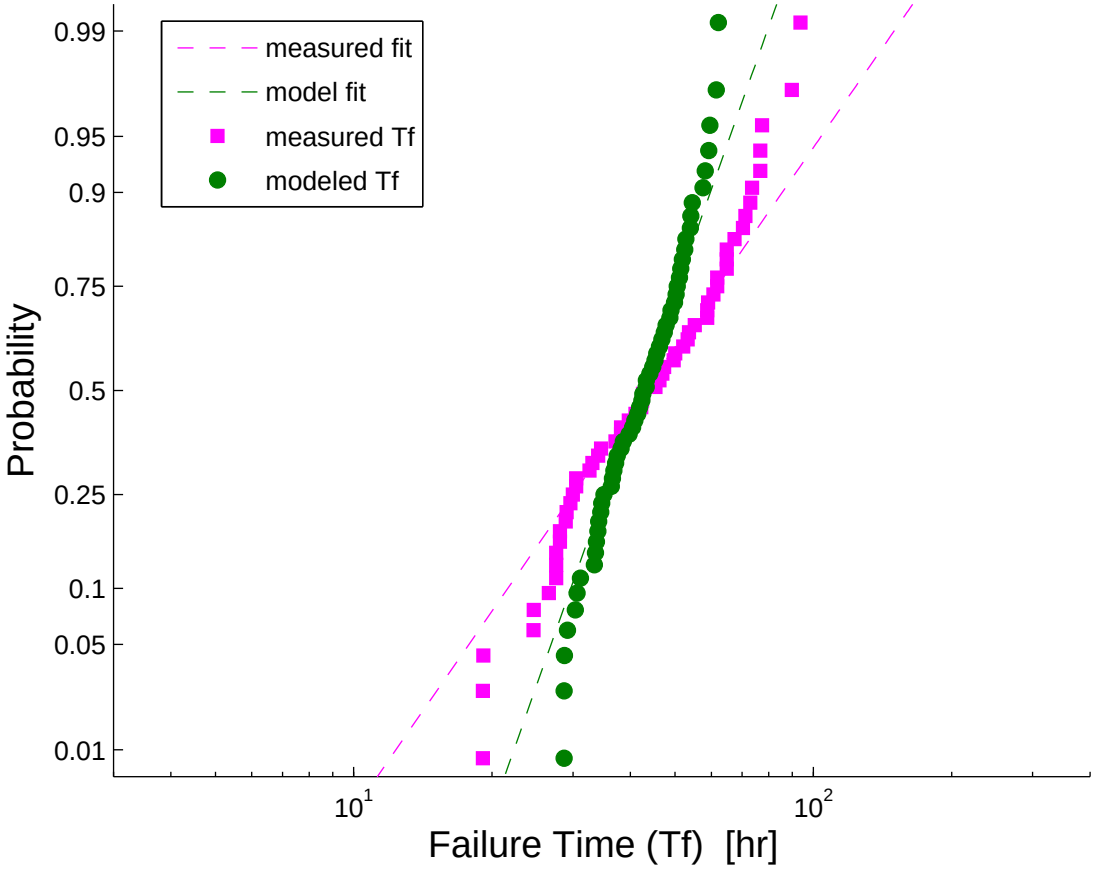
- Increase time, iterate until the critical resistance value



j : current density vector for each via

Evaluation of Our Model

- Comparison of modeled EM-induced failure time against measured data[2] on a log-normal probability plot



[5] T. Frank+ '11

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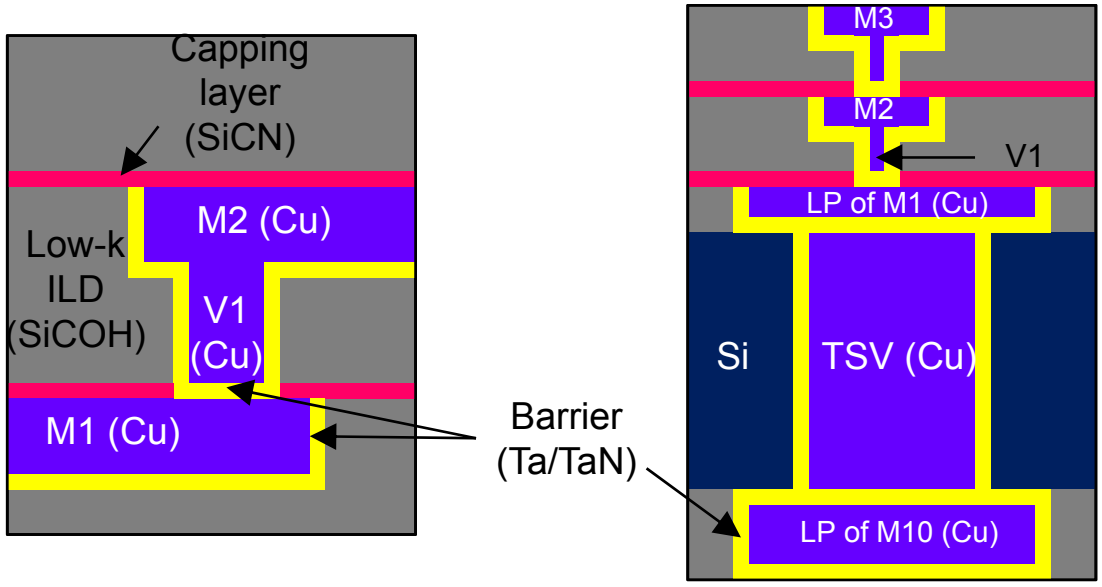
1) Impact of Barrier Resistivity

- Barrier: prevents diffusion of Cu, enhances adhesion
- Once void is developed in Cu, barrier can be the only path that the current can flow
- Barrier resistivity can significantly attribute the change of resistance of MSV structure due to EM



<LocalVia> <MSV>

1) Impact of Barrier Resistivity

- Barrier resistivity (TaN) can vary in the order of magnitude depending on the N_2 partial pressure

N_2 pressure	0 %	5 %	10 %	20 %	30 %
ρ TaN [1e-8Ωm]	95	254	702	2810	14800

[6] H. Nie+ '01

→ Examine the relationship between resistivity and Tf

ρ TaN [1e-8Ωm]	Tf [a.u.]
200	1300
500	1136
2000	992
5000	939
10000	917

→ The higher resistivity, the lower Tf we get

2) Analysis on Void-free Local Vias

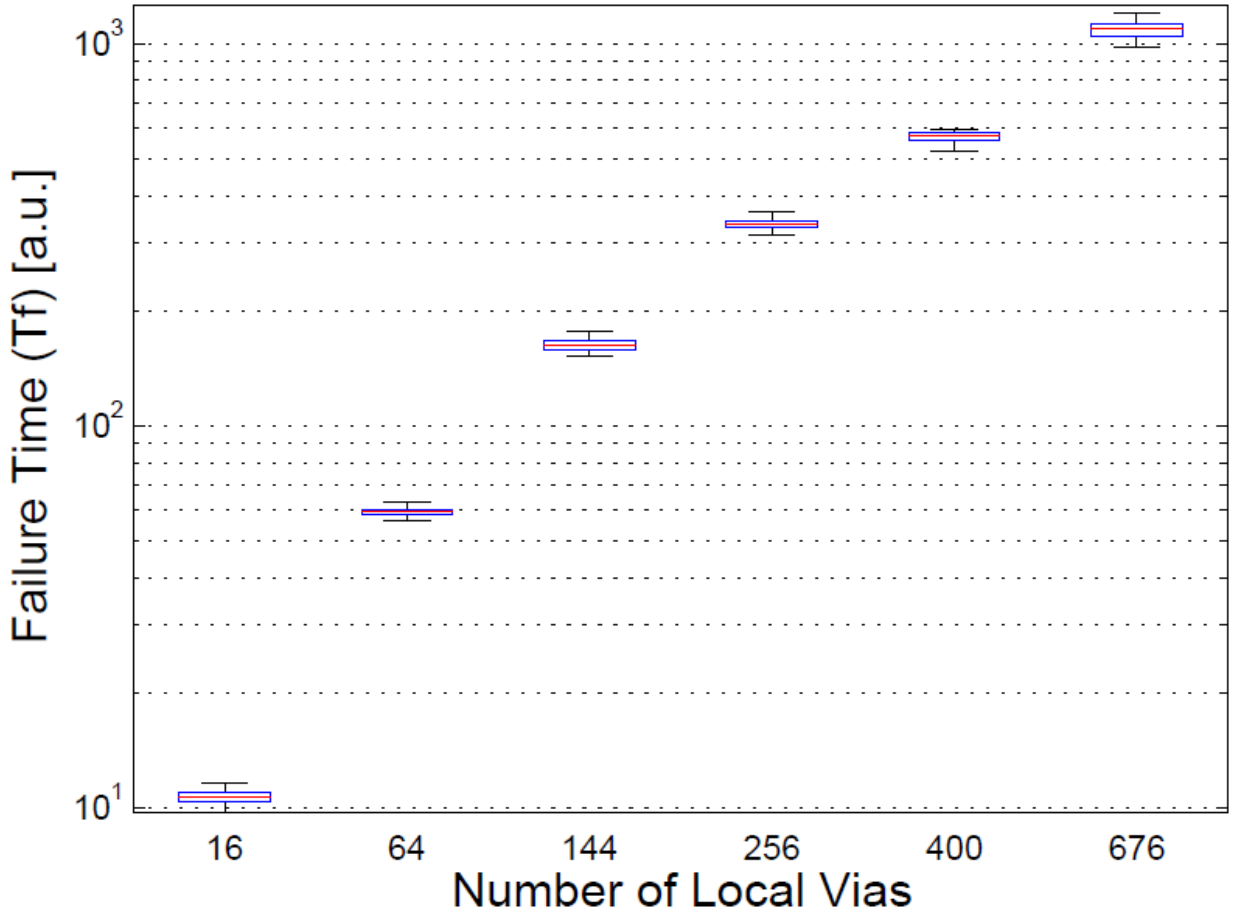
- Percentage refers to void-free ratio among local vias
- If all the local vias have initial voids (column with 0%), Tf of MSV is dominated by local vias
- If more and more local vias become void-free, Tf of MSV can be dominated by TSV

Void-free TSV | The TSV & some local vias have voids | Void-free local vias

ρ TaN [1e-8Ω]	Tf by V1 voids only [a.u.]	Tf byTSV void and V1 voids (%: V1s w/o void)				Tf by TSV void only [a.u]
		0 %	10%	50%	90%	
200	1311	1300	1594	6658	7269	7328
500	1150	1136	1264	4825	5792	5914
2000	1006	992	1058	2533	4286	4444
5000	967	939	1017	2025	3842	4075
10000	942	917	997	1850	3683	3911
Avg. ratio	1	0.98	1.10	3.42	4.68	4.82

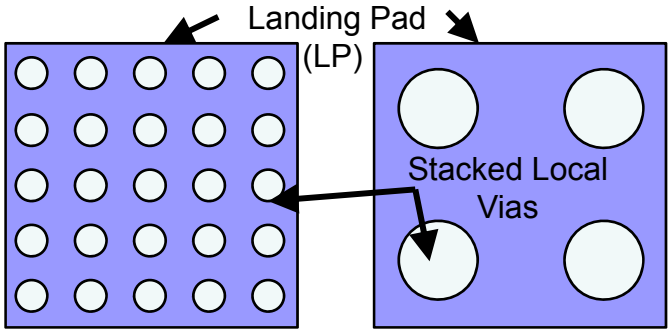
3) Study on Number of Local Vias

- Assume same size of local vias (V1 in 45nm technology)
- More local vias in a MSV → Much longer Tf
- 30 samples for each case with current variation



4) Trade-offs: Via Size & Num of Vias

- Larger local via can be more robust to EM even with smaller number of vias



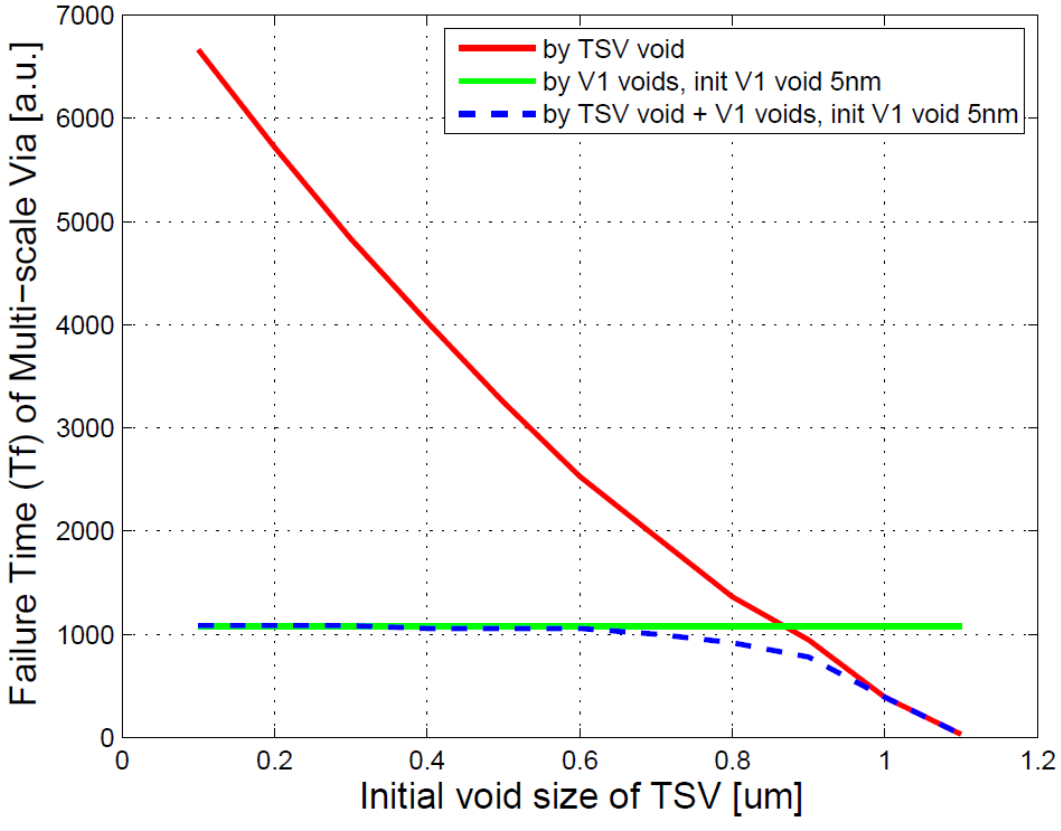
$$j_{o,via} = \frac{I_{o,TSV}}{n \times A_{via}} = \frac{j_{o,TSV} \times A_{TSV}}{n \times A_{via}}$$

$$Area = n \times A_{via}$$

Via Layer	D_via	#Via/LP	Jo [MA/cm^2]	Init r_void	Crit r_void	Tf [a.u.]	Area [um^2]	Tf/Block Area
V1	65nm	676	6.47	5nm	36.8nm	1078	1.61	670
V2	70nm	529	6.95	5nm	38.0nm	1044	1.50	696
V4	140nm	144	5.44	5nm	64.8nm	2411	1.91	1261
V8	400nm	16	5.44	5nm	144nm	5583	1.91	2923

5) Impact of Initial Void

- If the initial void of TSV is small, mostly EM of V1 can dominate the MSV lifetime
- However if TSV crack becomes significant, EM of TSV can determine the MSV lifetime



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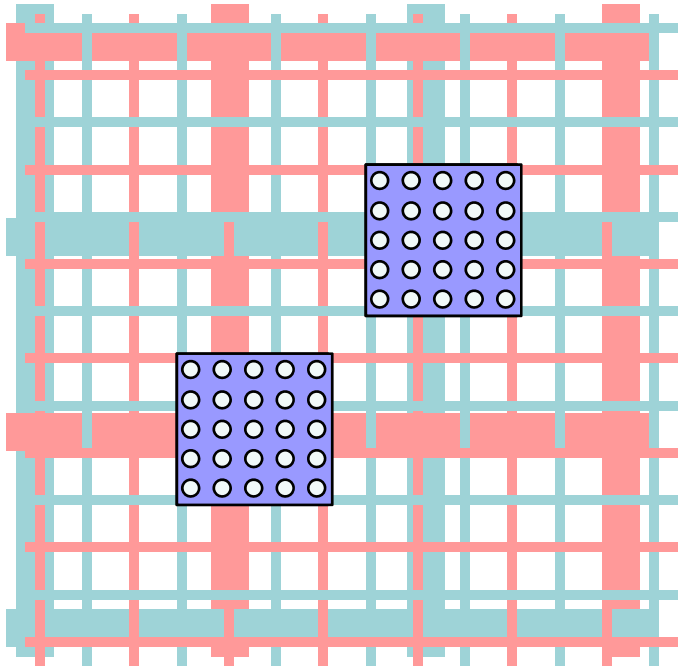
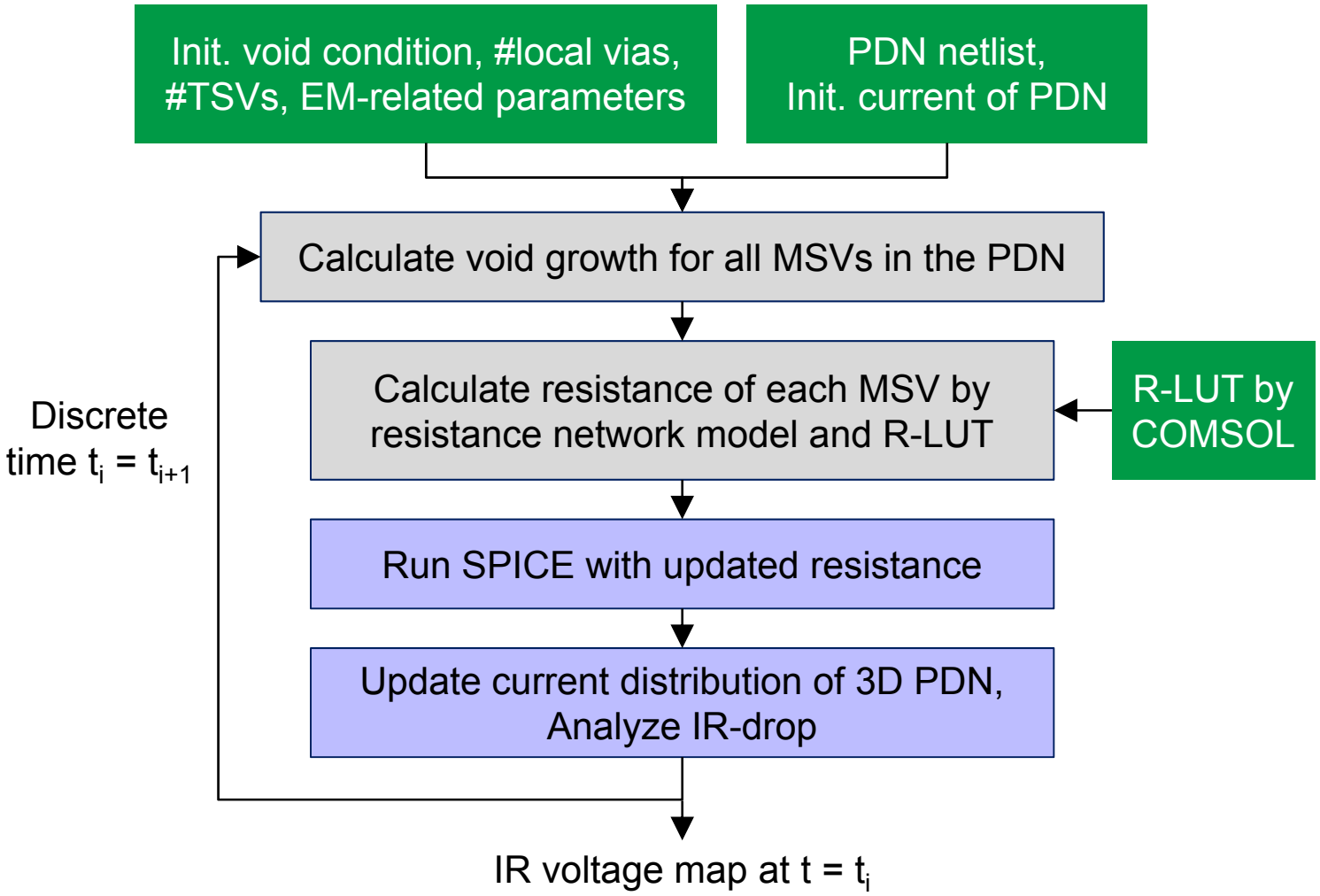
EM of Full-chip 3D Power Network

- Suggest full-chip EM analysis of P/G multi-scale vias
  - Useful to have more EM-robust designs for 3D ICs



EM of Full-chip 3D Power Network

- Flow to analyze EM of 3D power distribution network (PDN)



Benchmark 3D PDNs

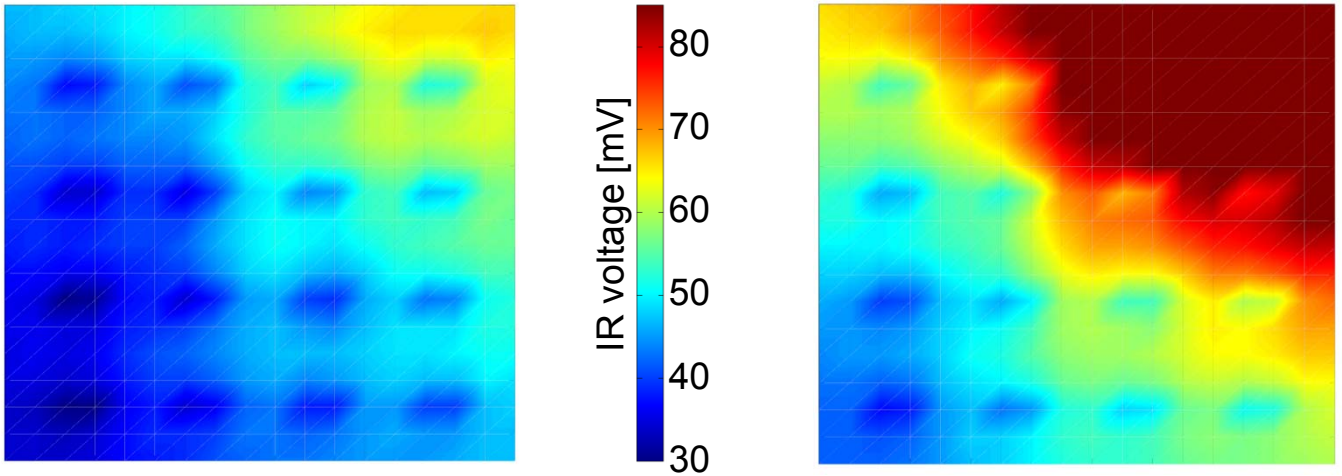
- Use 3D PDNs with stacked 2-dies [6]

	Area [mm^2]	Power density [W/mm^2]		Power grid	# TSVs	# C4 bumps
		Top	Bottom			
PDN1	25	0.57	0.57	50 x 50	144	144
PDN2	64	0.80	0.75	60 x 60	225	225
PDN3	81	0.80	0.80	90 x 90	484	484
PDN4	121	0.71	0.91	110 x 110	729	729
PDN5	225	0.47	0.49	150 x 150	1369	1369

[7] X. Zhao+ '13

IR-drop of MSVs in 3D PDNs

- Average IR voltages of MSVs are increased due to EM

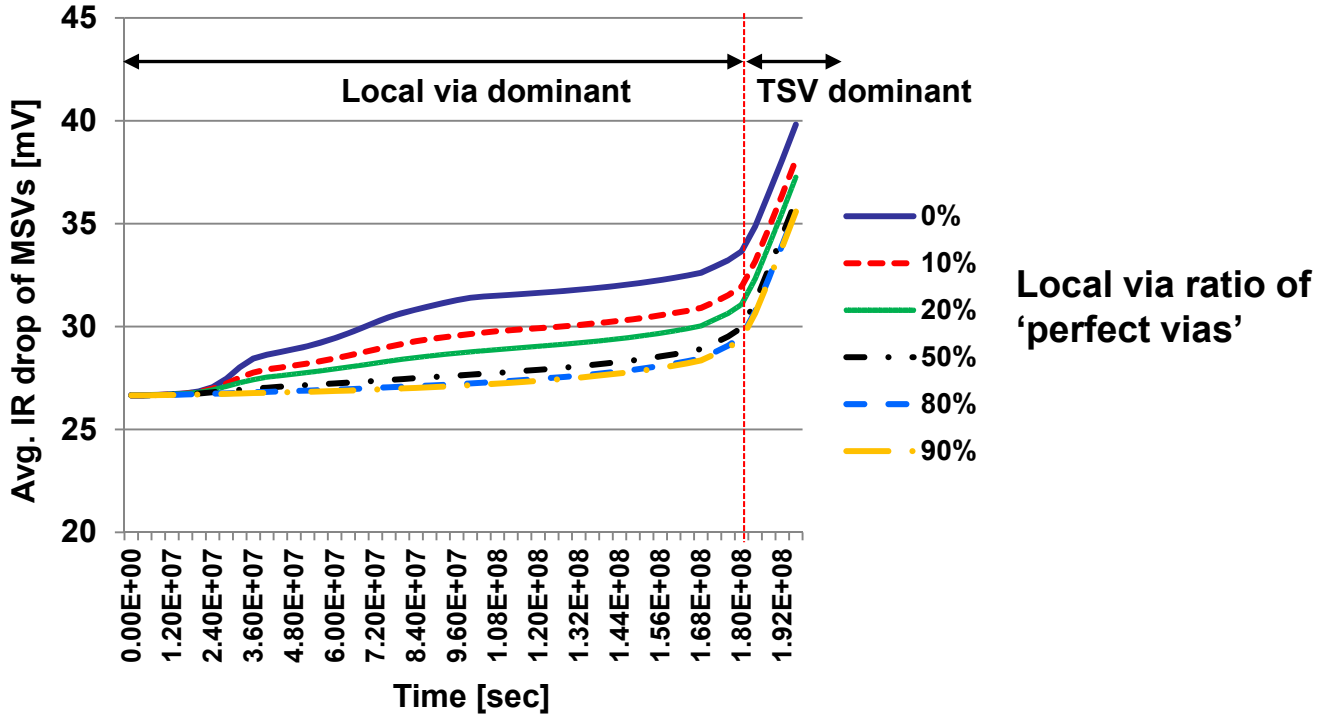


t = 0 t = 1.8e8 seconds

	Avg. IR-drop of MSVs [mV] (%: increase)				Avg. runtime per iter.
	t=0	t=5e7 s (1.6 yrs)	t=1e8 s (3.2 yrs)	t=2e8 s (6.3 yrs)	
PDN1	33.96	38.33	39.93	41.45 (22.1 %)	0.82 s
PDN2	44.82	52.38	53.11	57.50 (28.7 %)	4.89 s
PDN3	45.60	53.30	54.08	59.98 (31.5 %)	7.84 s
PDN4	45.67	53.38	54.17	60.60 (32.7 %)	13.63 s
PDN5	26.66	28.90	31.40	39.81 (49.3 %)	26.29 s

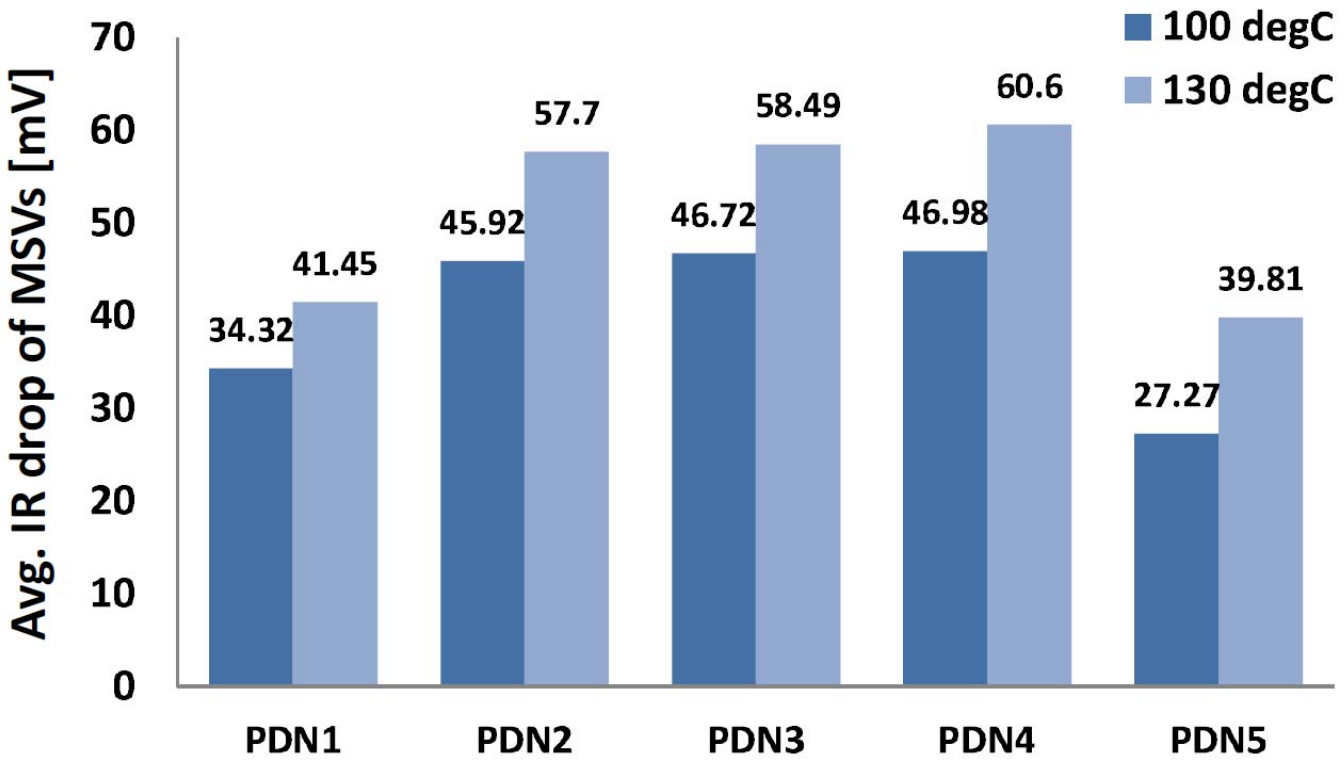
Effect of Initial Void Condition

- If we don't have initial void (= void seed), void growth will not appear at that location
- More 'perfect vias' can reduce EM and IR-drop in PDNs



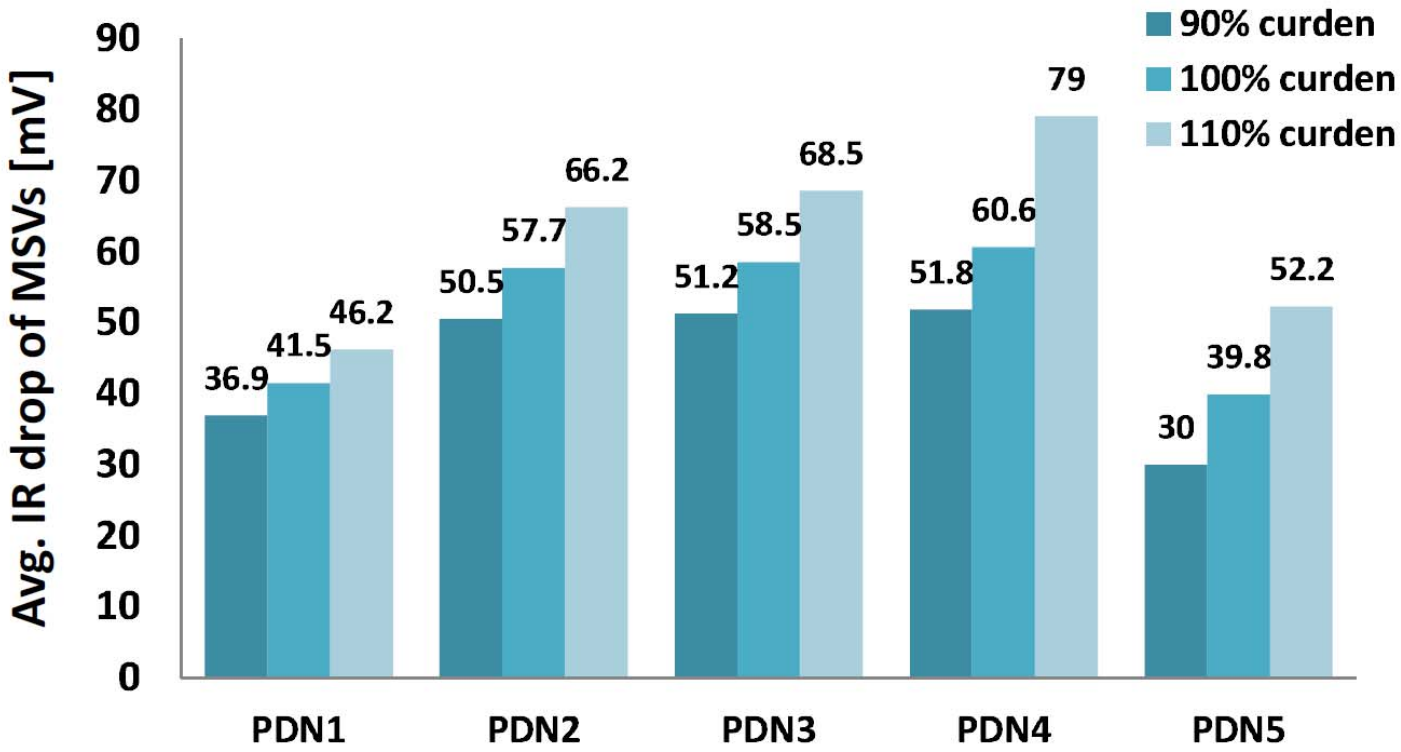
Impact of Temperature

- Higher temperature, more EM we have
  - ➔ Higher IR-voltages on average



Impact of Current Density

- More current density, more EM we have
  - ➔ Higher IR-voltages on average



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Summary: EM Study in MSV

- Proposed an efficient EM modeling flow for multi-scale vias (MSVs) in 3D PDN
- Investigated the impact of number and size of local vias, initial void condition on EM-induced failure time of MSV structure
- Studied the interplay between EM of local vias and EM of TSV, and analyzed its impact on EM of the MSV structure
- Analyzed IR-drop of full-chip level 3D PDNs with a proposed EM modeling flow

Thank you!

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