

Fundamentals on Continuous-Time Sigma-Delta Modulators

DLP Series, sponsored by the CASS

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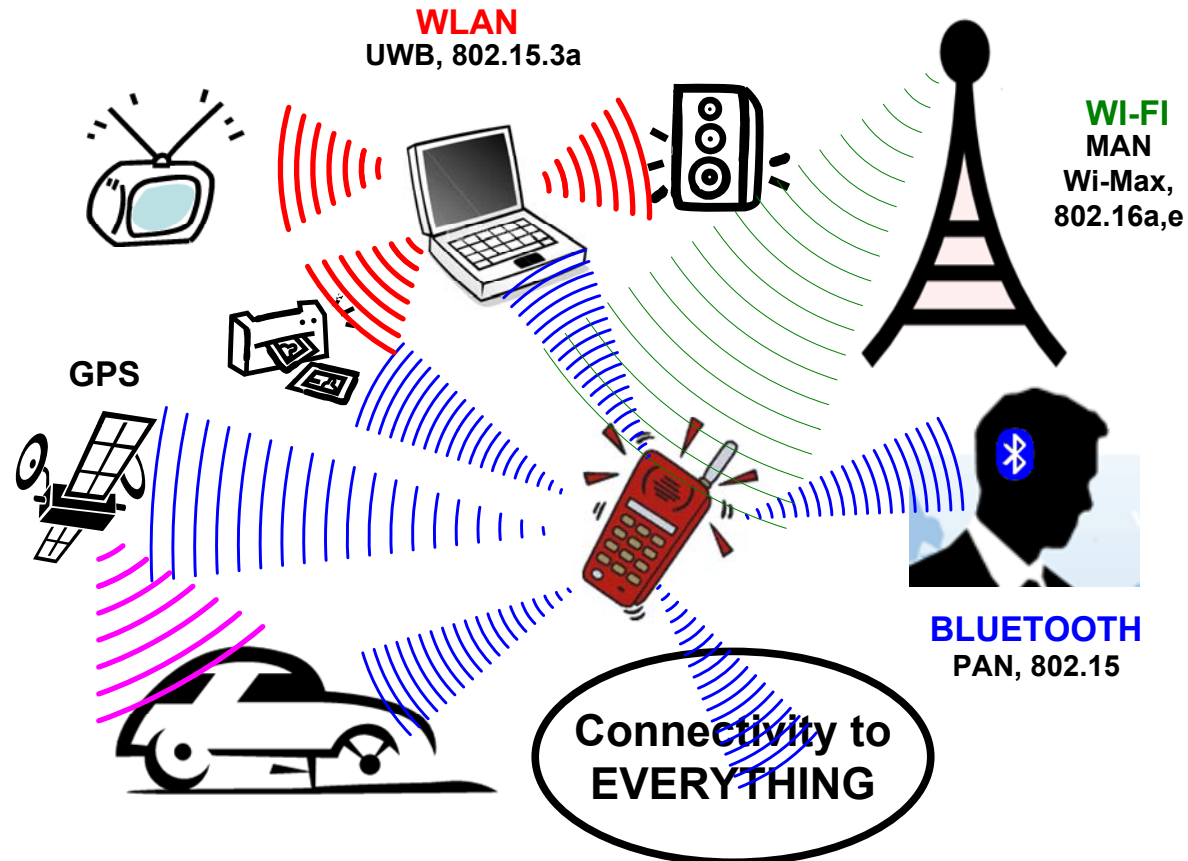
September 19, 2013



Outline

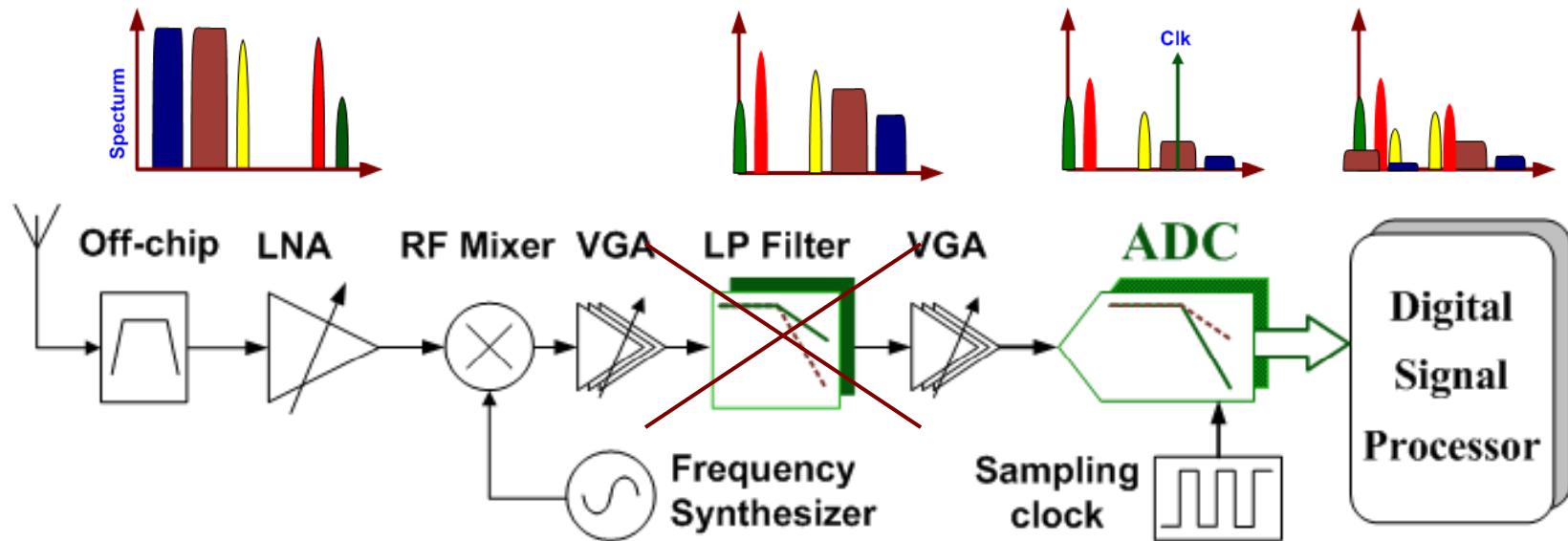
- **Introduction**
- **Fundamentals of Sigma-Delta Modulators**
 - **Stability**
 - **Clock Jitter**
 - **Blockers Tolerance**
- **Quantizer Issues**
 - **Voltage Mode versus Current Mode**
- **Improving blocker tolerance**
 - **Efficient non-invasive filtering**
 - **Saturation detector**
- **Current Research Projects**
- **TAMU: Where we are?**
- **Conclusions**

Introduction: Connectivity



- ❖ Increasing number of wireless standards
- ❖ Support of multiple-standards on the same chip
- ❖ Advances in Integrated RF design towards universal devices
- ❖ Software Radio: easy addition of new standards

Direct Conversion Multi-Standard Receiver



System issues in broadband systems:

High frequency filtering is especially critical in broadband applications

Rejection of Blockers: ADC filtering must be complemented by LP filtering

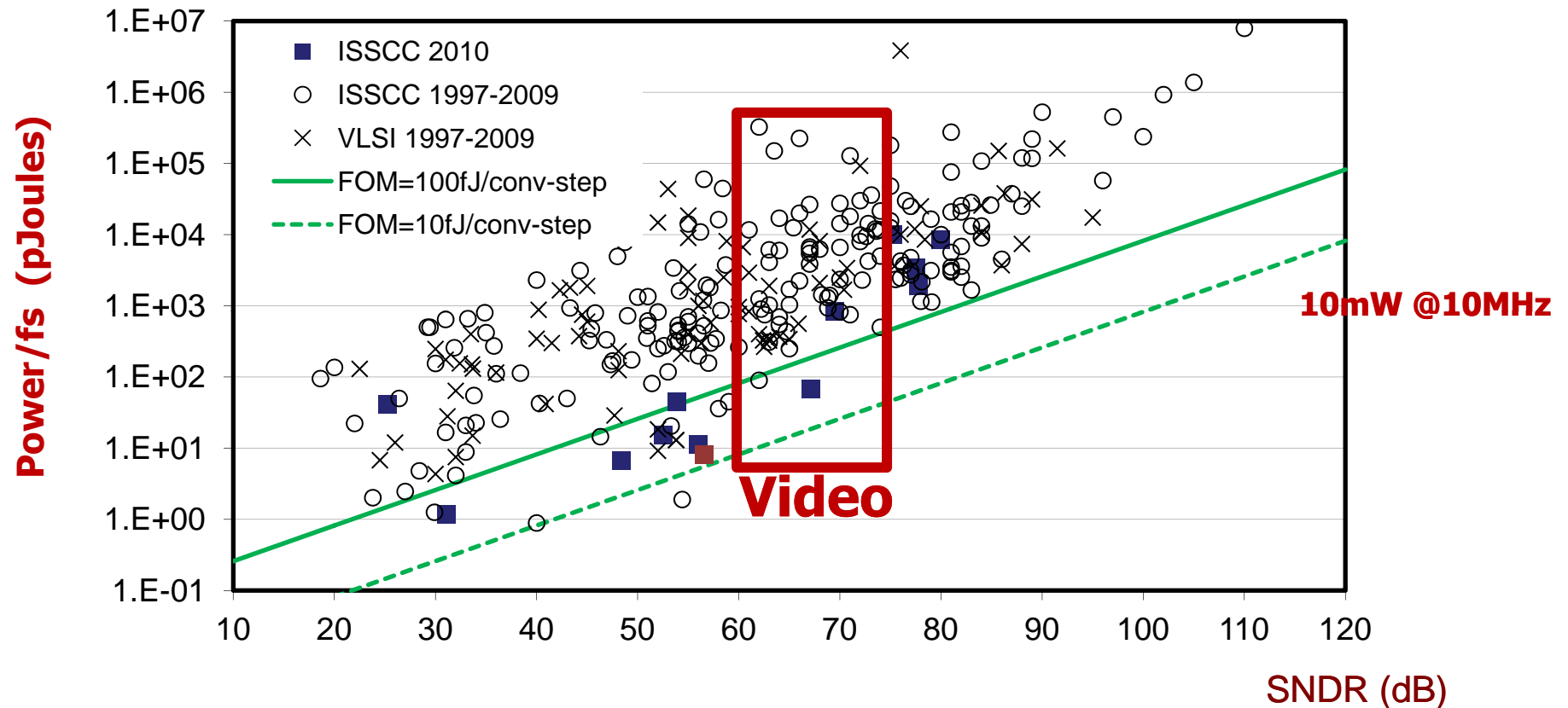
Neighbor channels are quite relevant even if heavy filtering is used

Trade-offs:

Light filtering in front demands an ADC with higher SNR and higher SDR

Higher SNDR-ADC implies more power and more circuit complexity

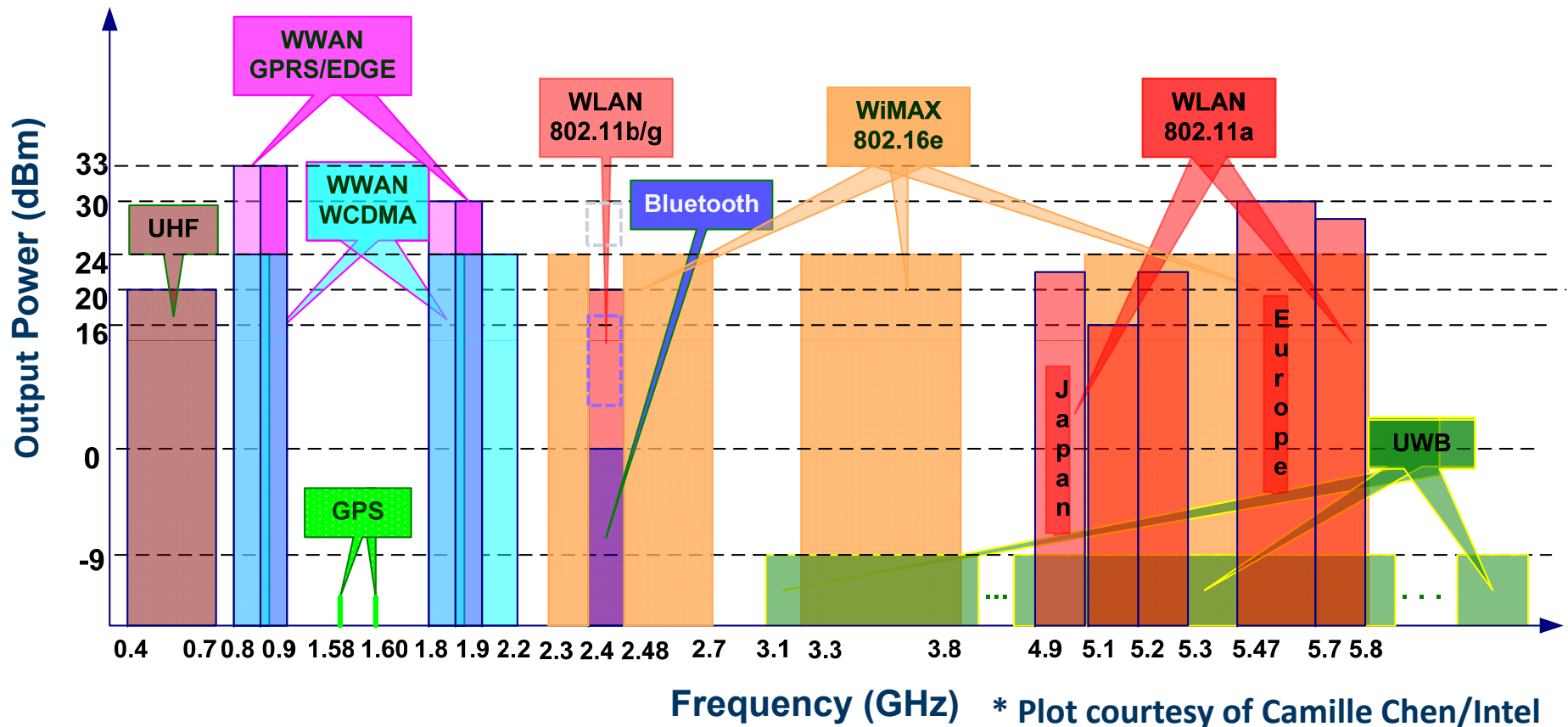
State of the art



B. Murmann, <http://www.stanford.edu/~murmann/adcsurvey.html>.

Challenge 1: Jitter Tolerance

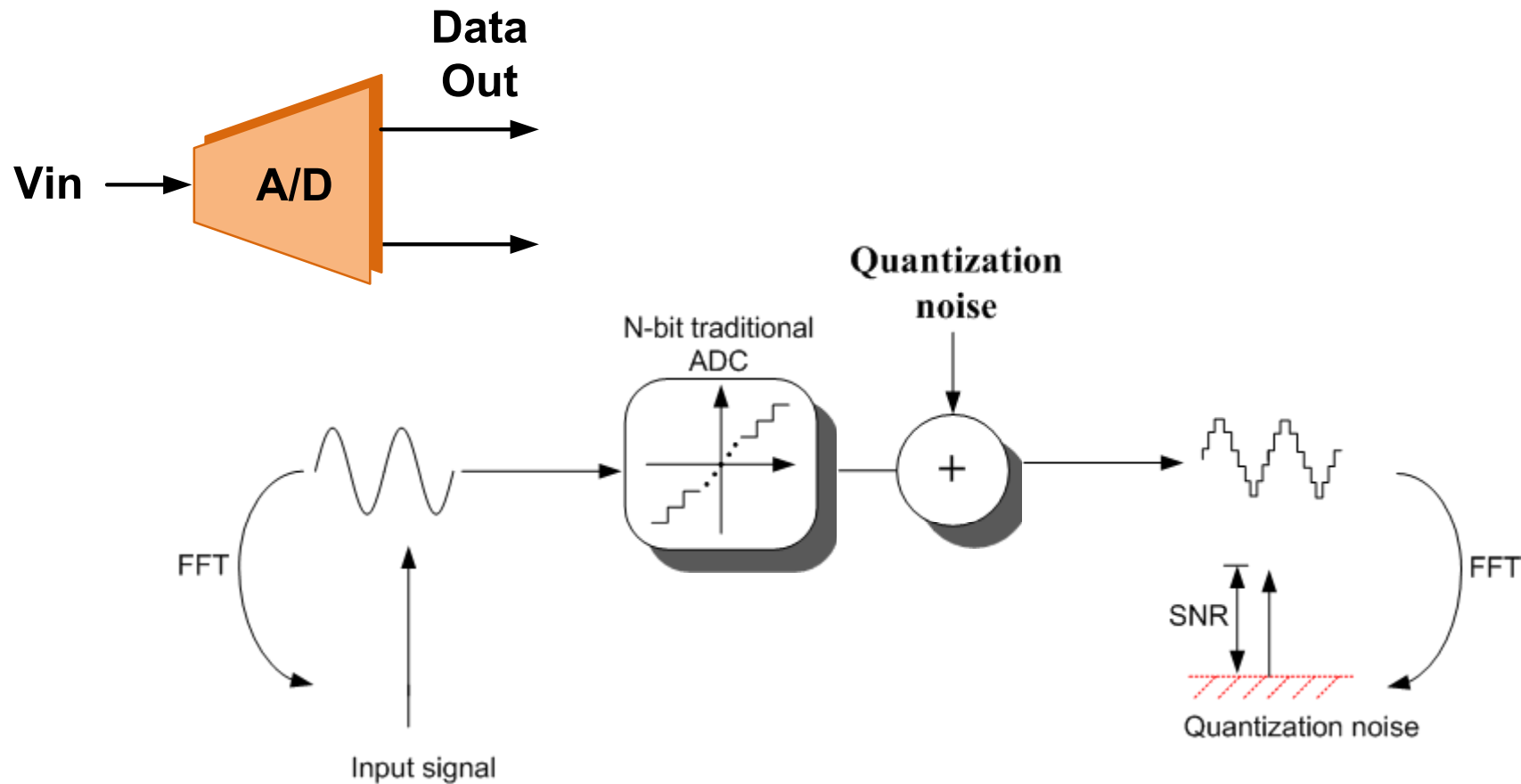
Challenge 2: Co-existence Simultaneous Usage of Radio Bands



**RF Interference: Frequency Overlap,
Out-of-Band Emissions, Receiver Saturation**

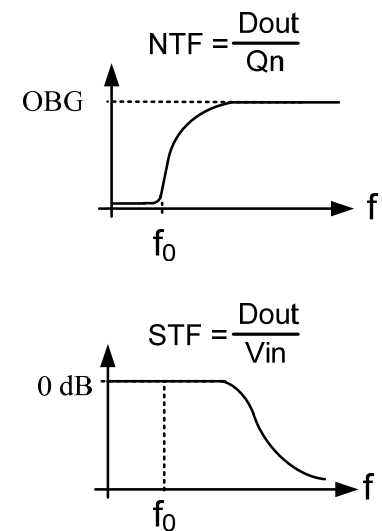
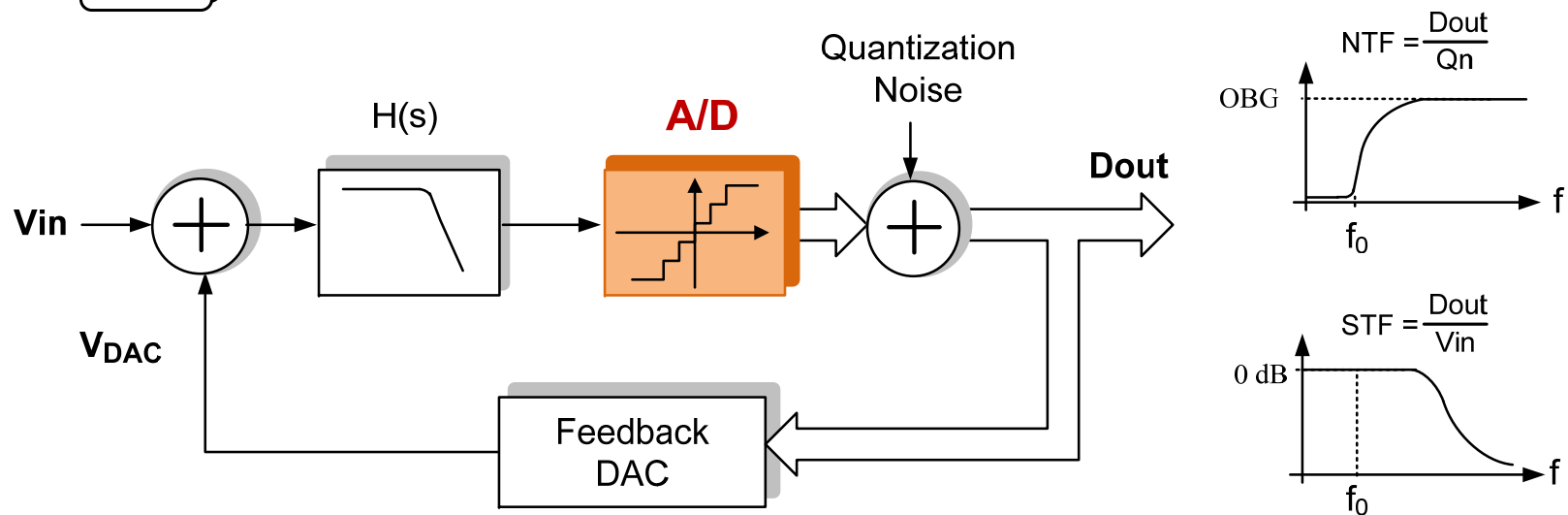
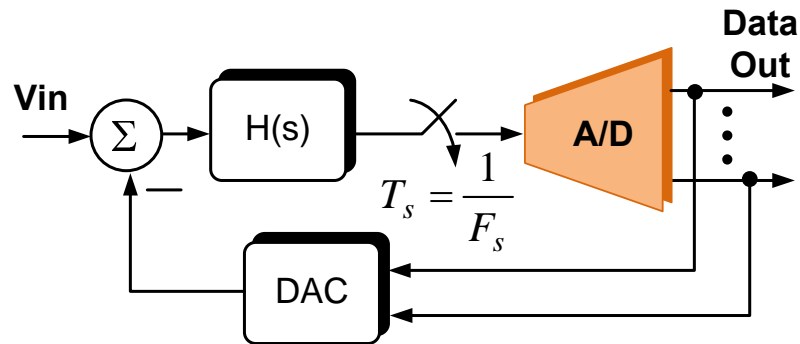
Sigma-Delta Modulators: Practical Design Issues

Conventional (Nyquist) ADC



$$\text{SQNR} = 6.02 * n + 1.76$$

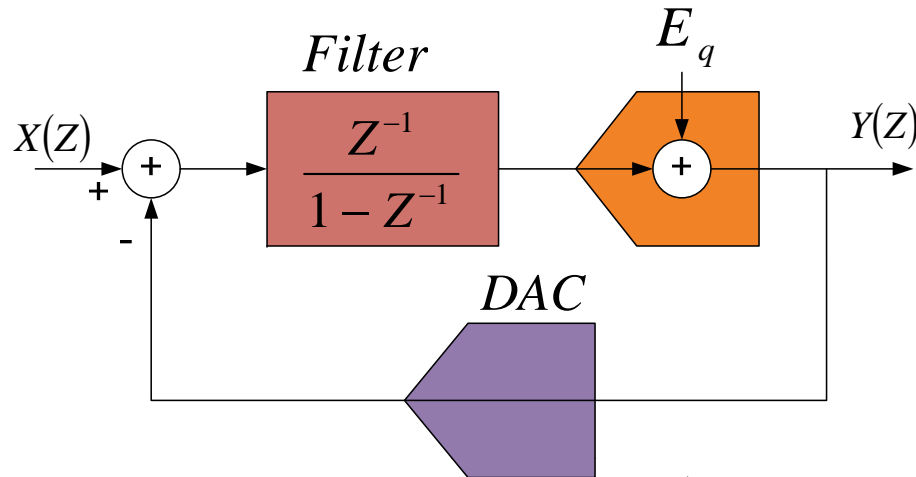
Basic concepts in $\Sigma\Delta$ Modulators



$$STF = \frac{H(s)}{1 + H(s)}$$

$$NTF = \frac{1}{1 + H(s)}$$

Fundamentals of Oversampled A/D Conversion



$$Y(z) = E(z) \frac{1}{1 + \frac{1}{z-1}} + X(z) \frac{\frac{1}{z-1}}{1 + \frac{1}{z-1}}$$

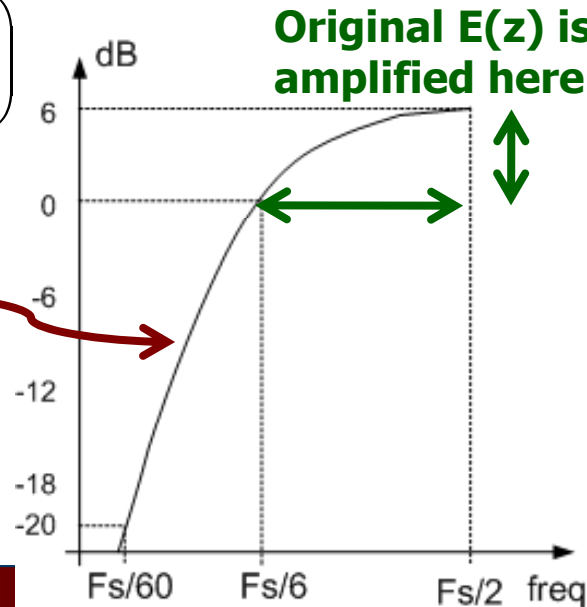
$$= E(z)(1 - z^{-1}) + X(z)z^{-1}$$

Check the input-output trajectories
Original E(z) is shaped by NTF

$$H_e(z) = 1 - Z^{-1} = 1 - e^{-j\omega T} = e^{-j\frac{\omega T}{2}} \left(e^{+j\frac{\omega T}{2}} - e^{-j\frac{\omega T}{2}} \right)$$

$$H_e(z) = e^{-j\frac{\omega T}{2}} \left(2j \sin\left(\frac{\omega T}{2}\right) \right)$$

$$|H_e(z)| = 2 \sin\left(\frac{\omega T}{2}\right)$$

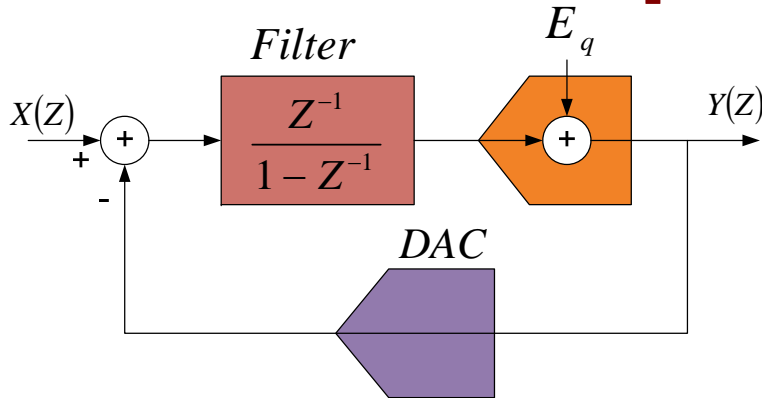


Spot SQNR

$$SQNR = \left| \frac{X(z)Z^{-1}}{E(z)H_e(z)} \right|^2$$

$$SQNR = \left| \frac{X(z)}{E(z)} \right|^2 * \left| \frac{1}{2 \sin\left(\frac{\omega T}{2}\right)} \right|^2$$

Oversampled A/D Conversion



$$SQNR \cong 1.5 * (2^N - 1)^2 * \left(3 * \frac{OSR^3}{\pi^2} \right)$$

$$SQNR \cong 1.76 + 6.02 * N - 5.2 + 30 * \log_{10}(OSR) \text{ dB}$$

$$SQNR = \frac{|X(z)Z^{-1}|^2}{\left| \int_0^{f_b} (E(z)H_e(z))^2 df \right|} = \frac{|X(z)|^2}{\left| E(z) \int_0^{f_b} (H_e(z))^2 df \right|}$$

$$SQNR = \left| \frac{X(z)}{E(z)} \right|^2 * \left| \frac{1}{\int_0^{f_b} \left(2 \sin \left(\frac{\omega T}{2} \right) \right)^2 df} \right|$$

If $f_b \ll f_s$, then

$$SQNR \cong \frac{\frac{1}{2} \left| \left(\frac{2^N - 1}{2} \right) (\Delta V_q) \right|^2}{\frac{\Delta V_q^2}{12} * \frac{2}{f_s}} * \left| \frac{6 * \left(\frac{f_s}{2 f_b} \right)^3}{\pi^2 * f_s} \right|$$

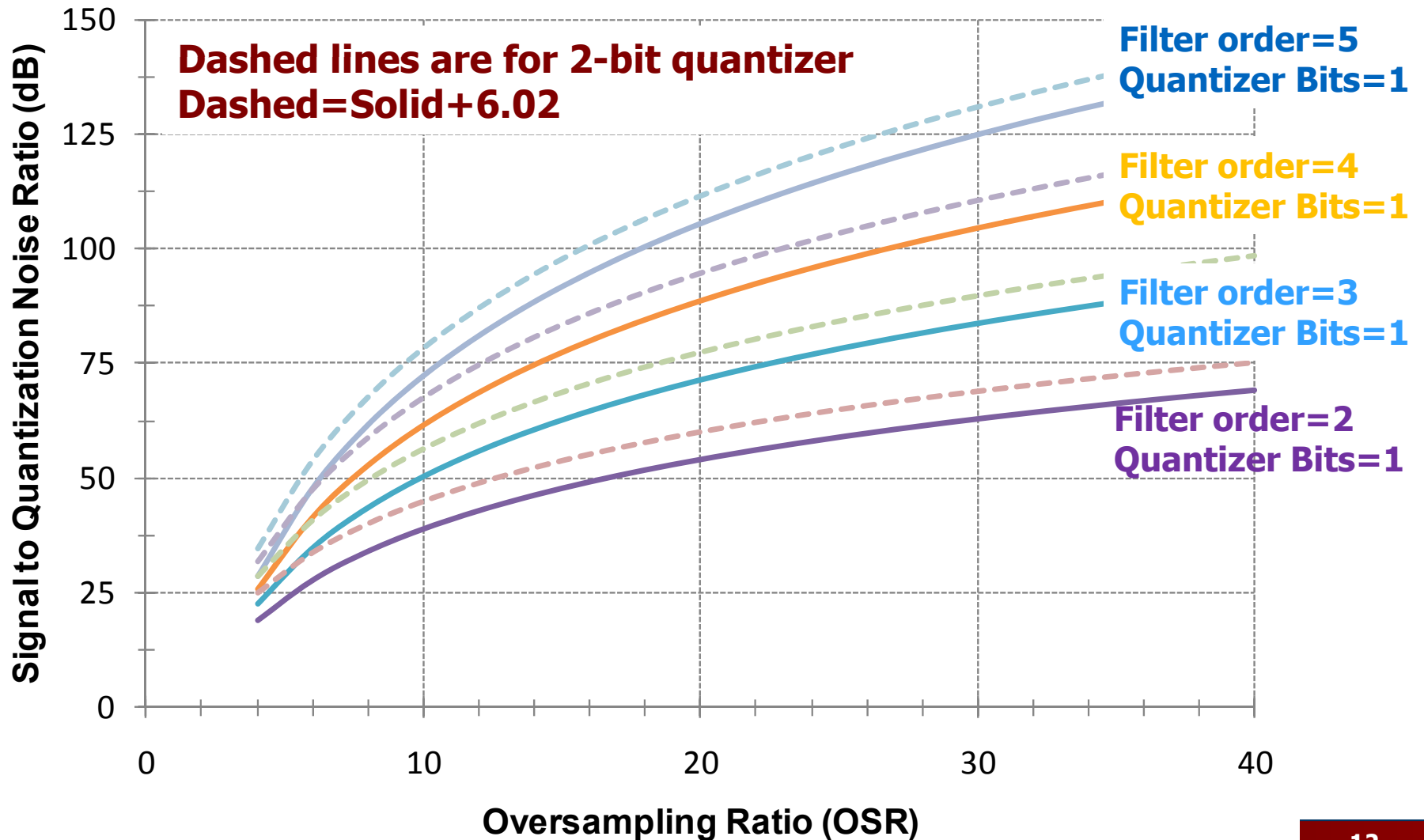
$$SQNR \cong 1.5 * (2^N - 1)^2 * \left(3 * \frac{OSR^3}{\pi^2} \right)$$

Signal to Quantization Noise Ratio (SQNR)

- **N=number of bits**
- **OSR=fs/2fb**
- **SQNR improves by 30dB when OSR increases by 10**
- **Or 9dB SQNR improvement when doubling OSR**

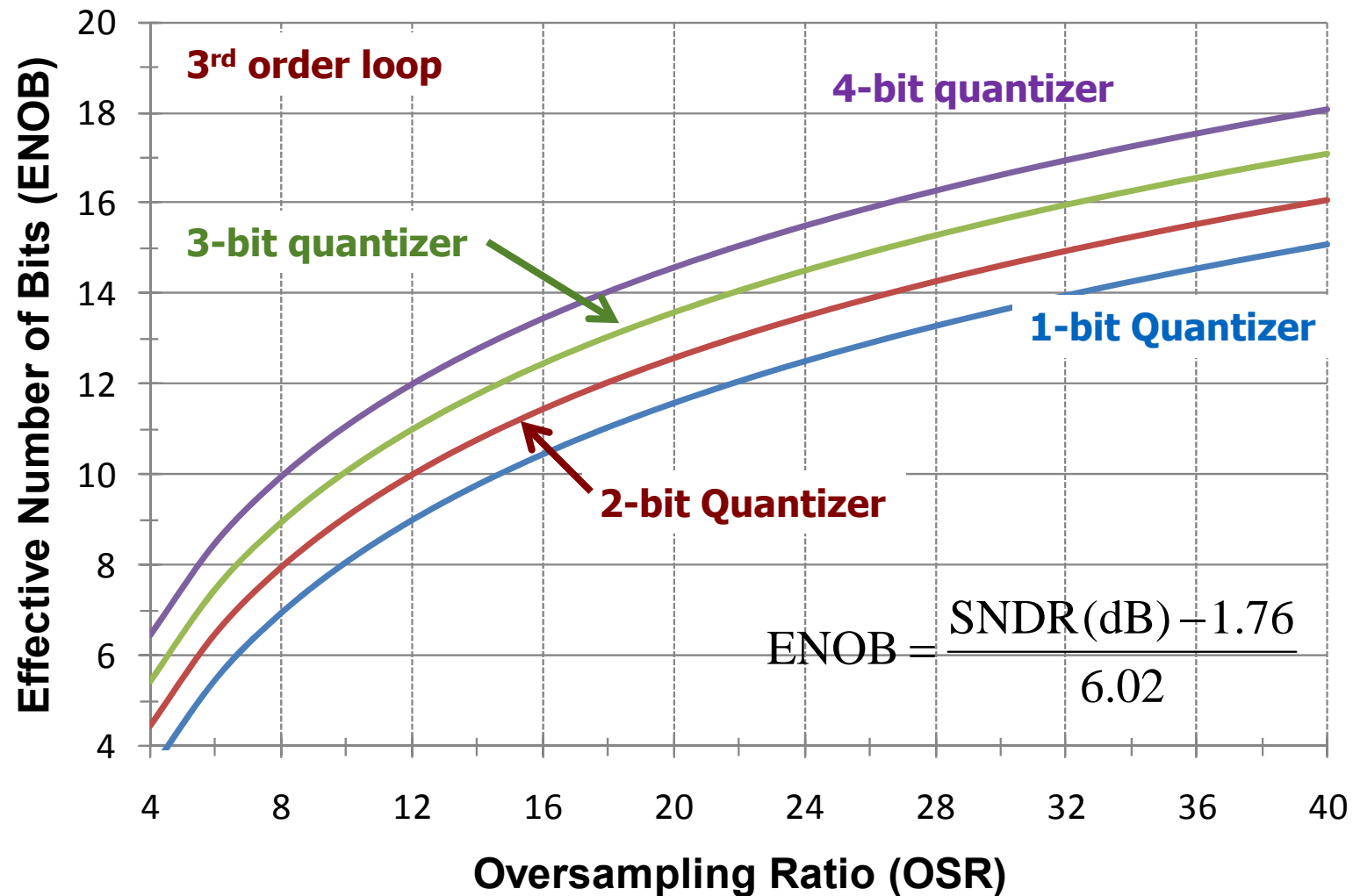
System Design Considerations

$$SQNR(dB) = 6.02N + 1.76 + (2L + 1)10\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L + 1}$$



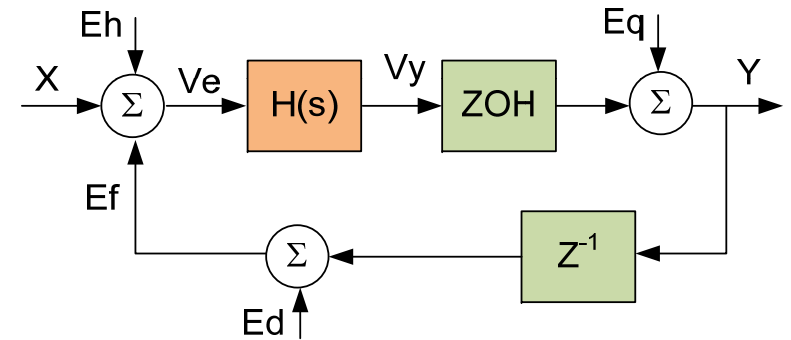
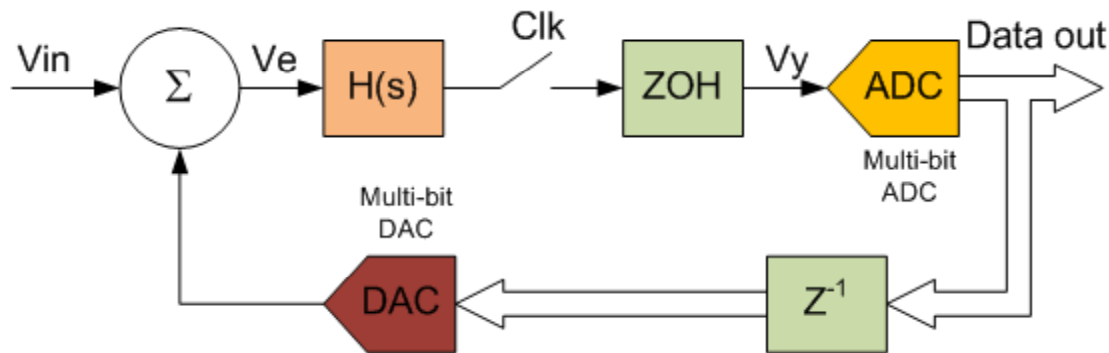
Design Considerations: 3rd order loop

$$SQNR(dB) = 6.02N + 1.76 + (2L + 1)10\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L + 1}$$



Oversampled A/D Conversion Feedforward Architecture

- E_q stands for the quantization noise
- E_d stands for DAC non-idealities (jitter + thermal noise)
- Filter's thermal noise is accounted in E_h



- The modulator's output becomes

$$Y = STF * (X + E_d + E_h) + NTF * E_q$$

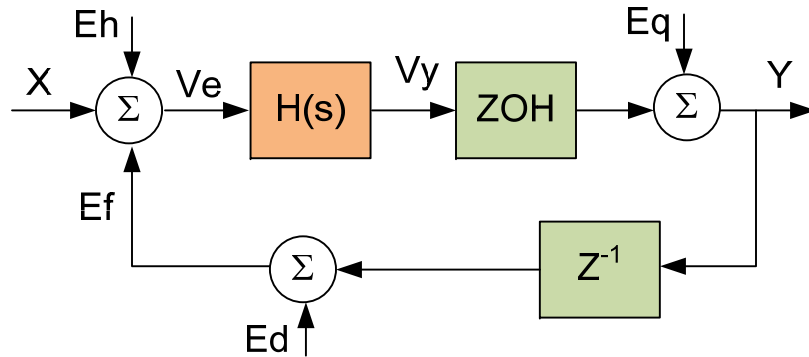
- The error signal (Filter's input) is

$$V_e = NTF * \left\{ H(s) ZOH(X + E_d + E_h) + Z^{-1} * E_q \right\}$$

$$STF = \frac{H(s) * ZOH(s)}{1 + H(s) * ZOH(s) * Z^{-1}}$$

$$NTF = \frac{1}{1 + H(s) * ZOH(s) * Z^{-1}}$$

Oversampled A/D Conversion: Effects of ZOH

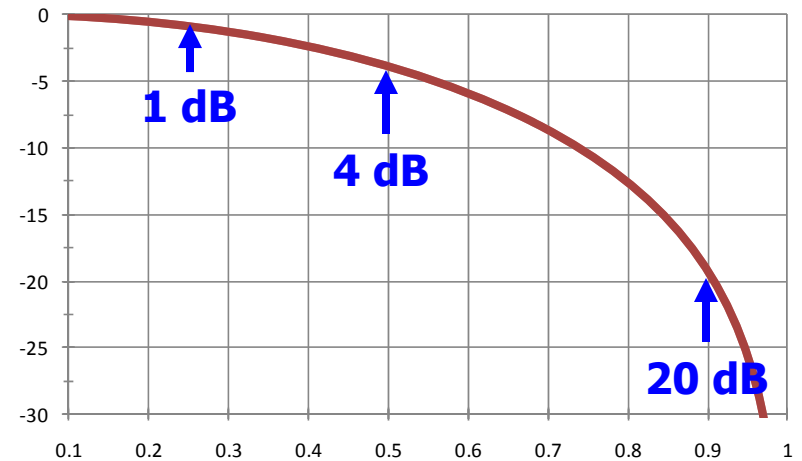
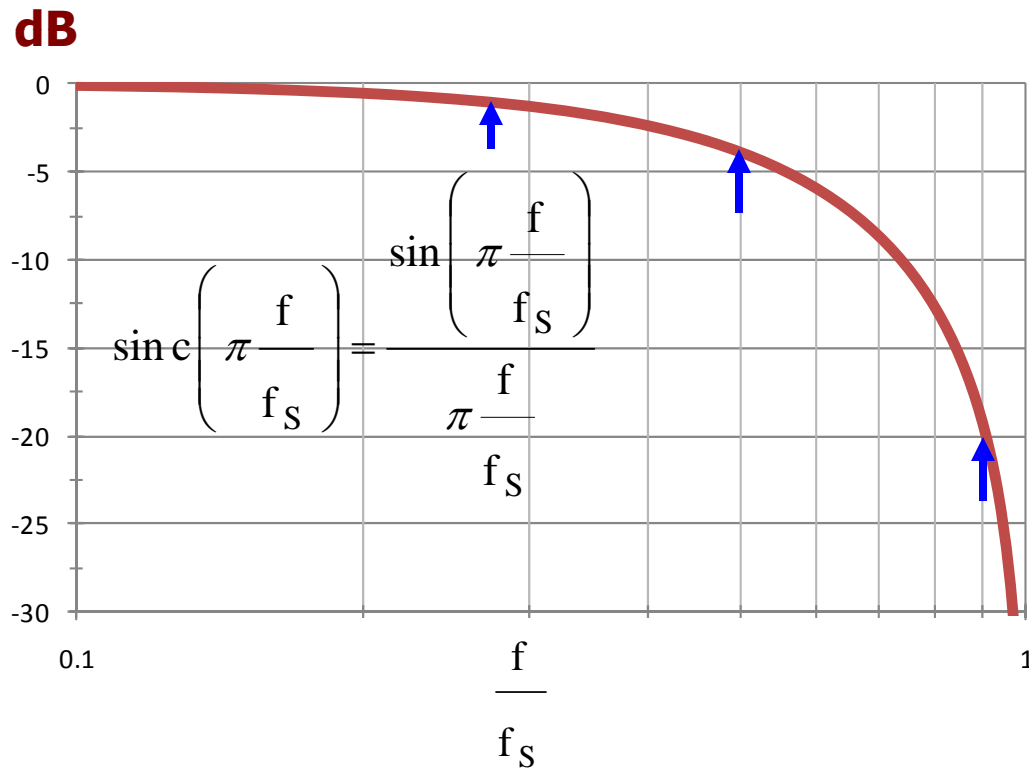


$$Z^{-1} = e^{-j\omega T_s}$$

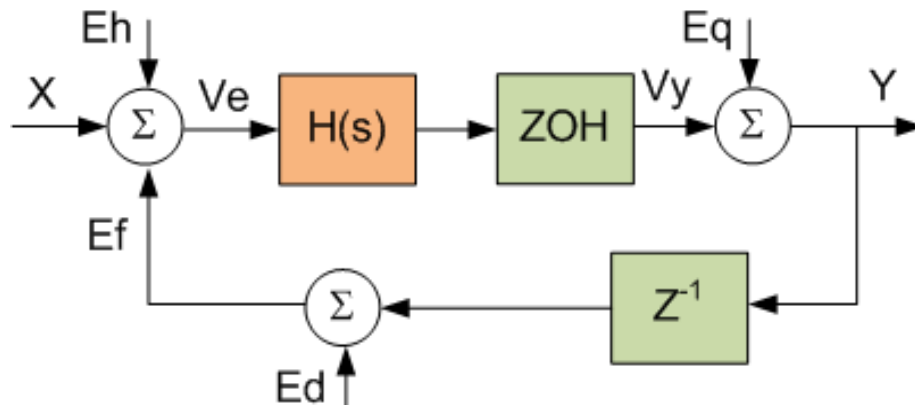
$$\text{Phase}(z) = -\omega T_s$$

➤ Notice that

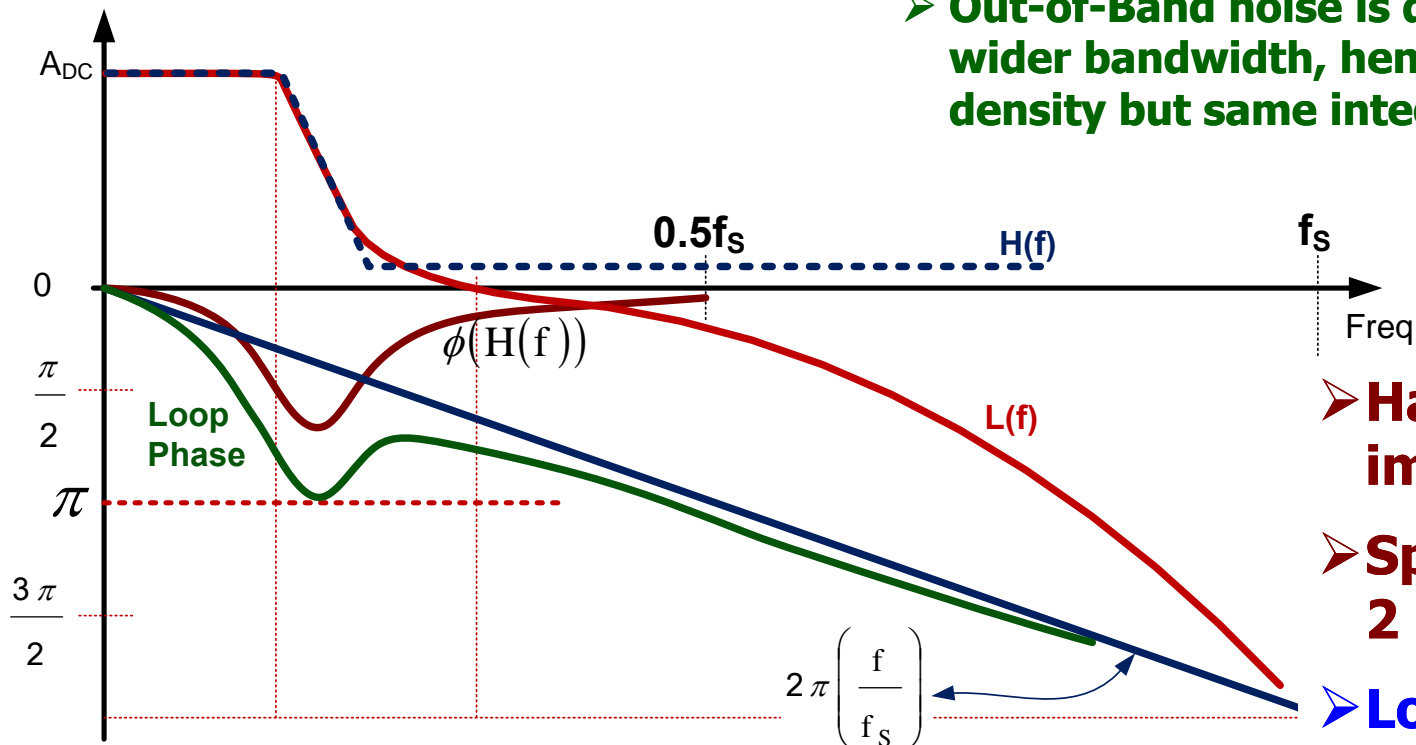
$$|ZOH(f)| = \text{sinc}\left(\pi\left(\frac{f}{f_s}\right)\right)$$



Stability Issues: $\Sigma\Delta$ Modulators



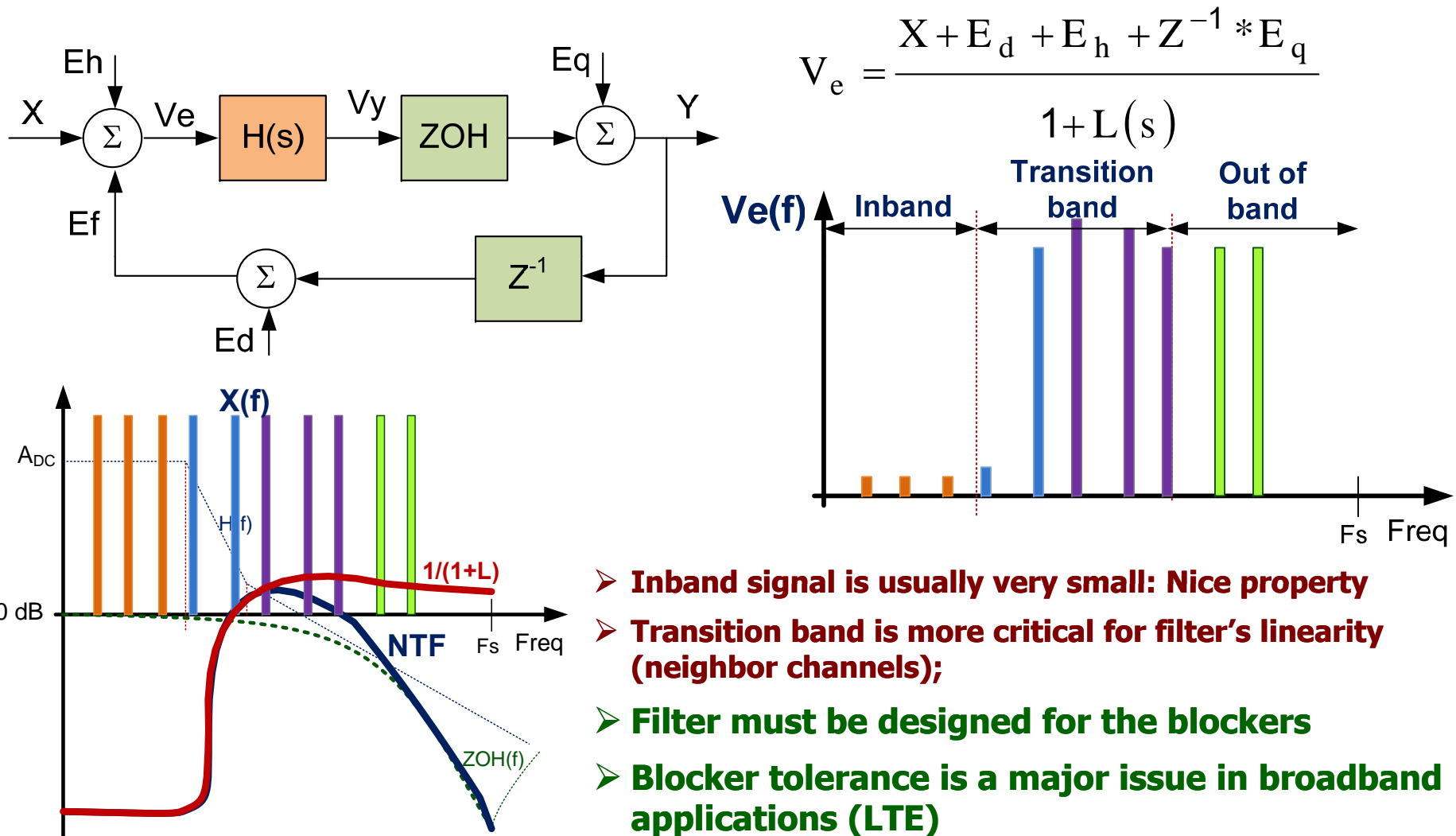
- Not very difficult to stabilize the loop if the unity gain frequency is below $F_s/4!$ (not very Low OSR); e.g. around 100MHz if clock frequency is 400MHz
- Notice that larger OSR allow you to reduce the filter gain at high-frequency
- Out-of-Band noise is distributed in wider bandwidth, hence smaller noise density but same integrated noise



- Hard to implement $H(s)$
- Split the filter in 2 parts
- Loop filter and fast path

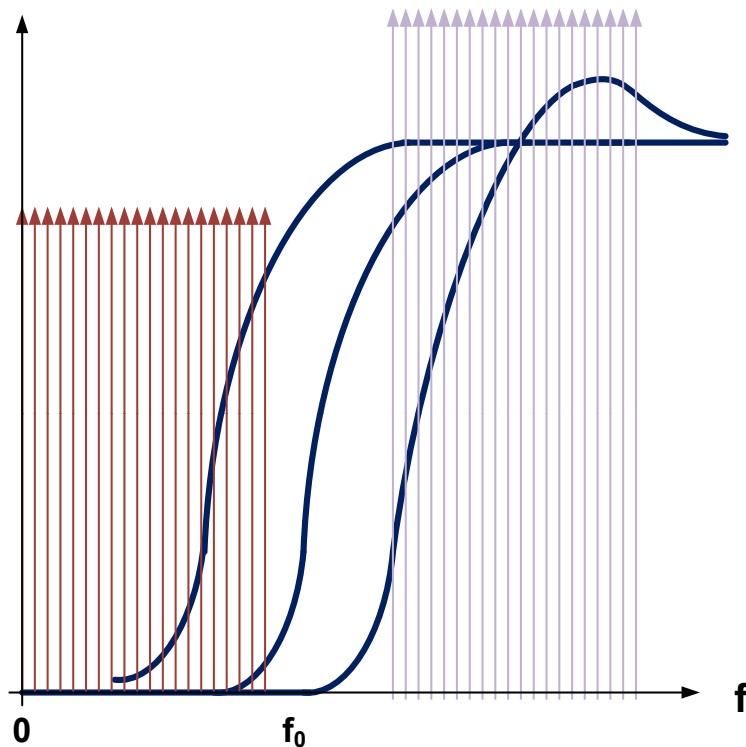
Effect of the blockers on loop operation

➤ Remarks on Filter's operation: Filter's input signal

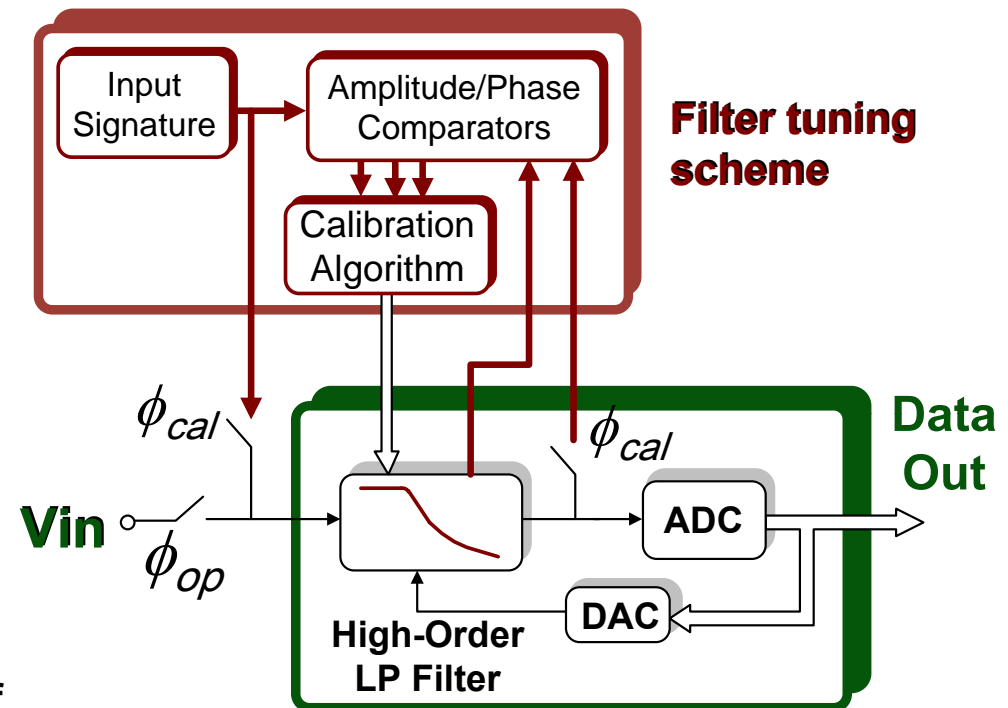


- **Inband signal is usually very small: Nice property**
- **Transition band is more critical for filter's linearity (neighbor channels);**
- **Filter must be designed for the blockers**
- **Blocker tolerance is a major issue in broadband applications (LTE)**

System Optimization: Tuning Filter Parameters



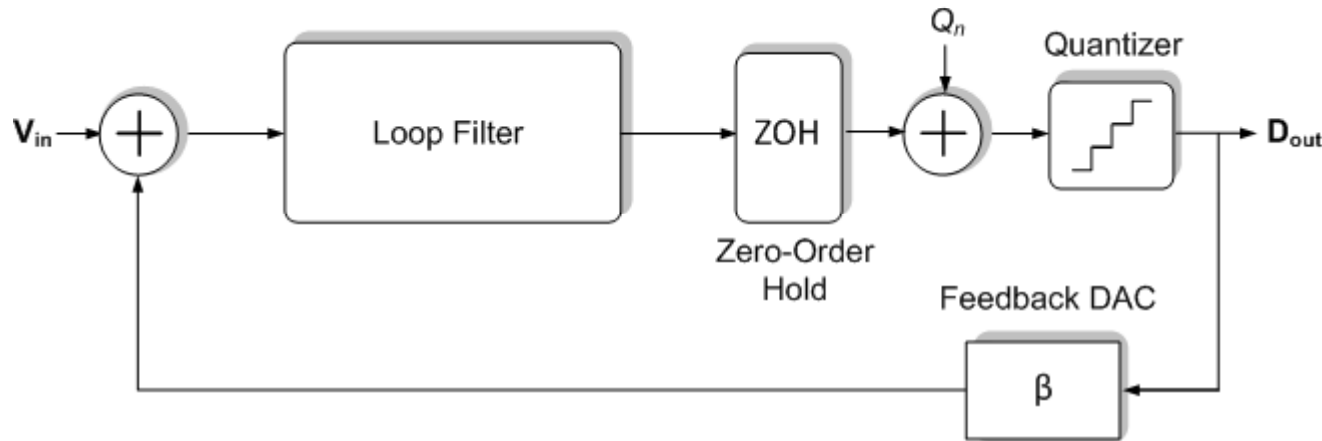
Effect of PVT Variations



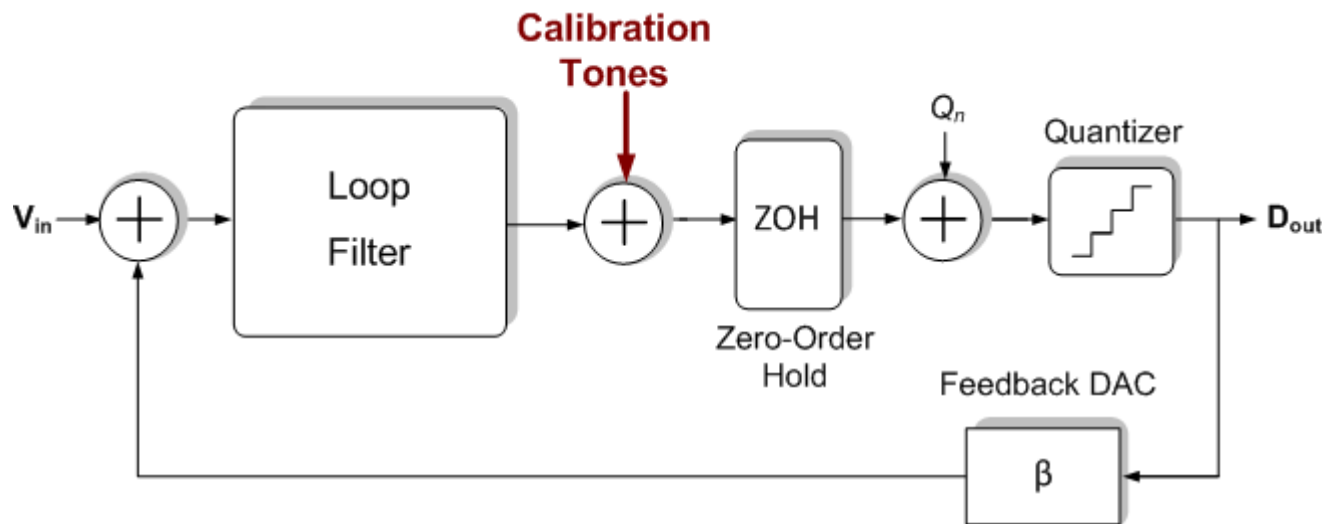
Filter Tuning; reconfiguration or Master slave techniques could be used

- **Calibration of (standalone) building blocks:**
- **Does not guarantee loop stability (excess loop delay)**
- **Does not guarantee best NTF (Coefficient adjustments)**

System Optimization: Global Tuning Scheme



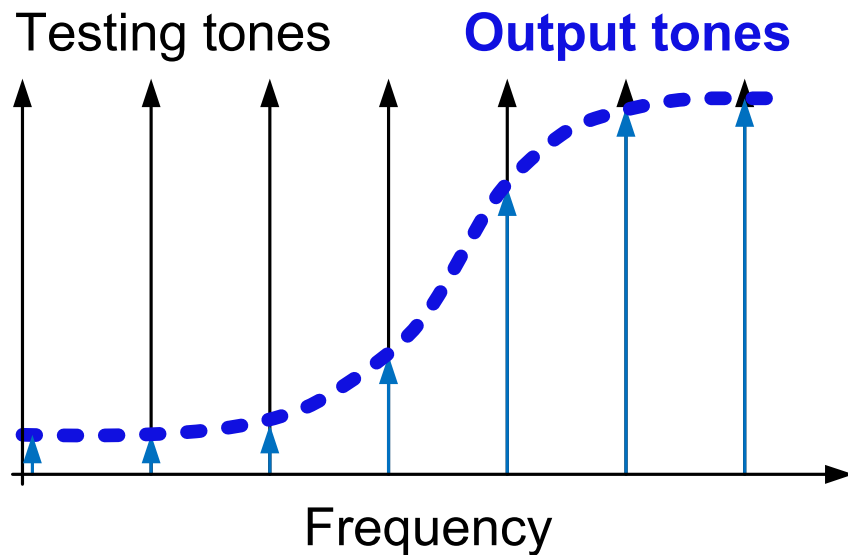
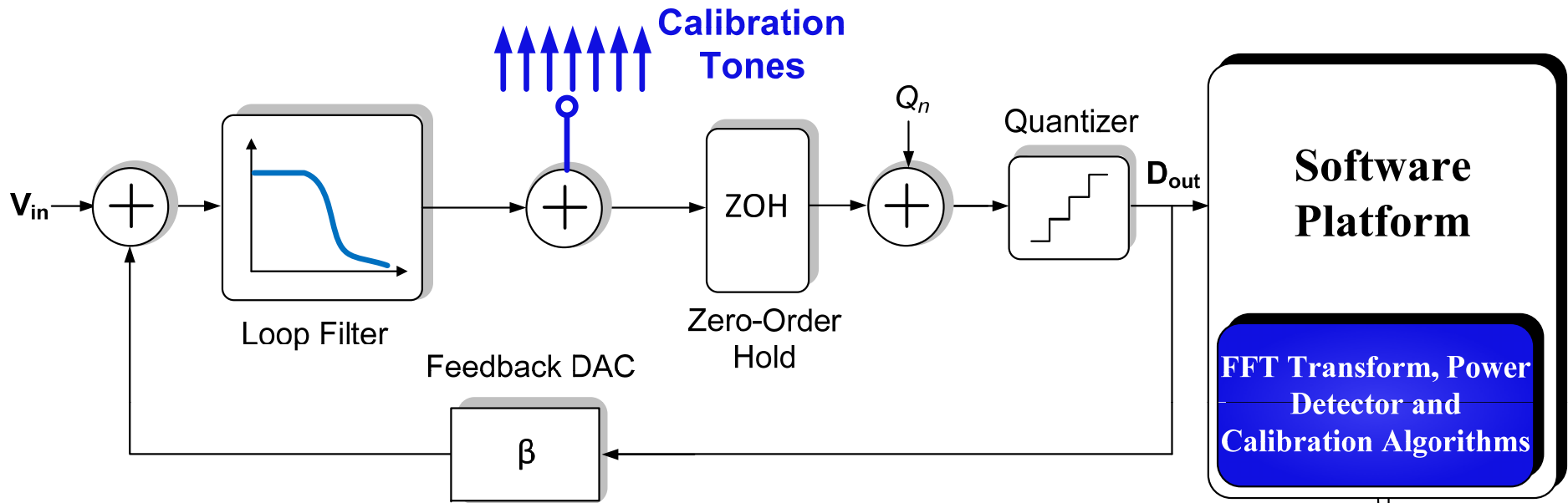
**Linear model
used to find
NTF**



- **Model used to calibrate NTF**
- **Loop response to calibration tones is analyzed in digital domain**

- **F. Silva-Rivas, et. al., "Digital Based Calibration Technique for Continuous-Time Bandpass Sigma-Delta Analog-to-Digital Converters," Analog Integrated Circuits and Signal Processing, April-09.**
- **C.Y. Lu, et. al., "A Sixth-Order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth," IEEE J. Solid-State Circuits, June 2010.**

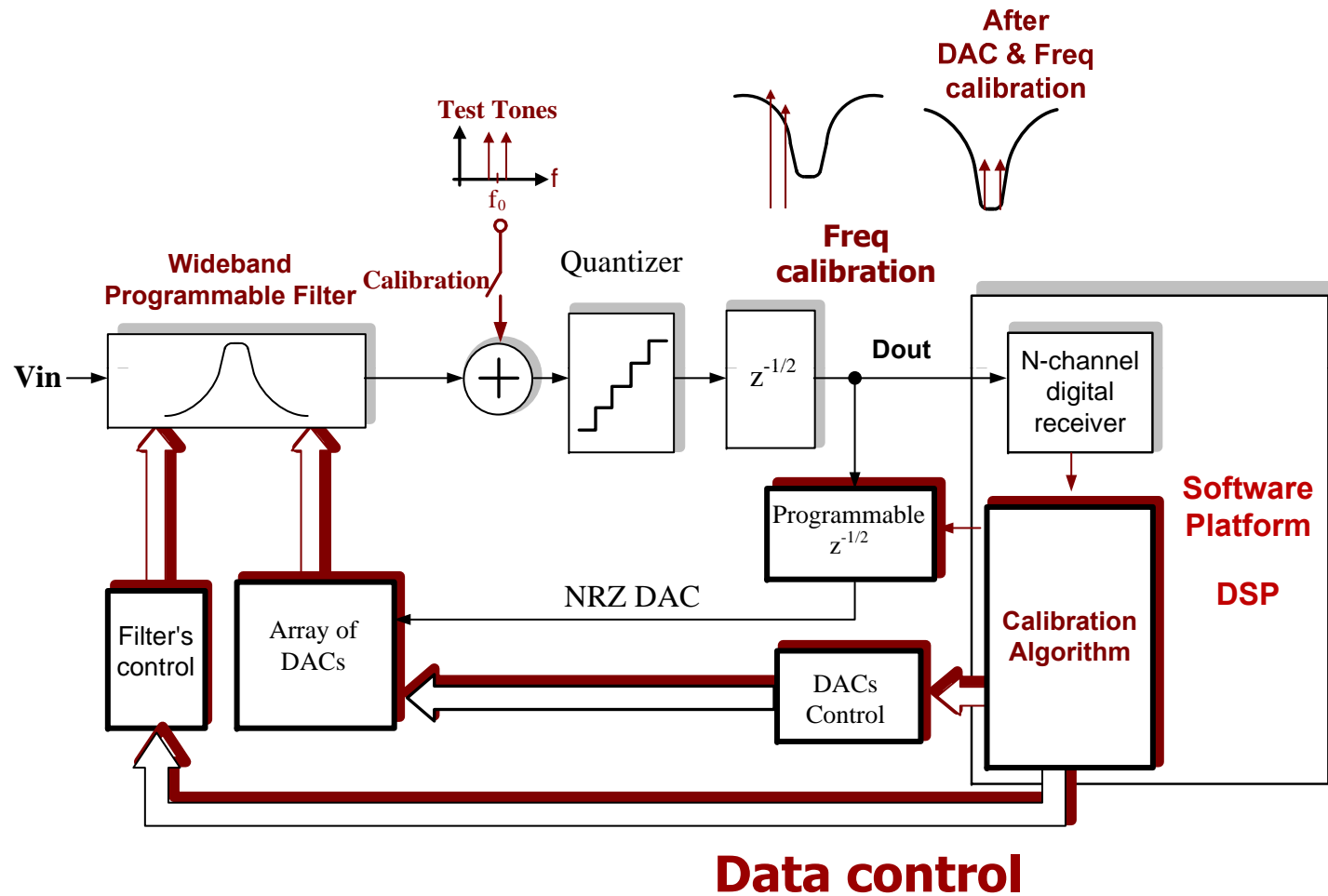
Global Tuning Scheme for NTF Parameters: Digital



A set of strategic tones are used to optimize:

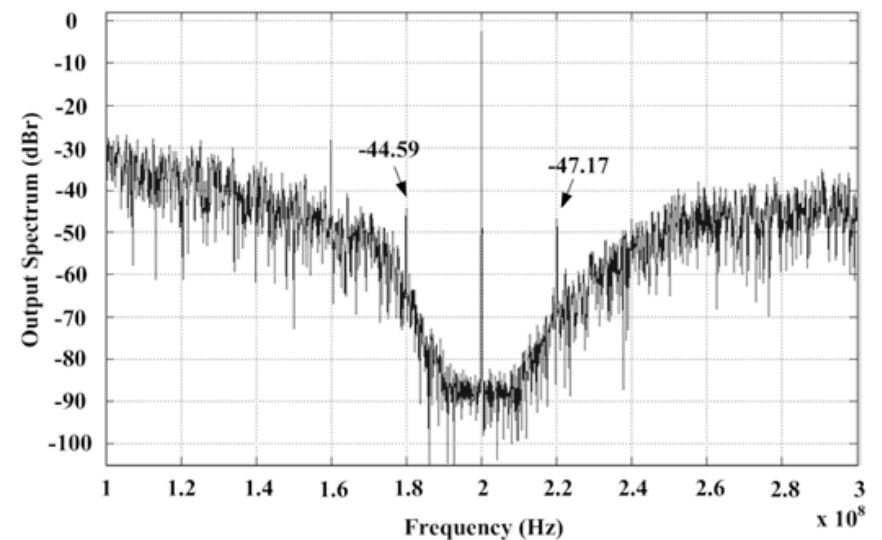
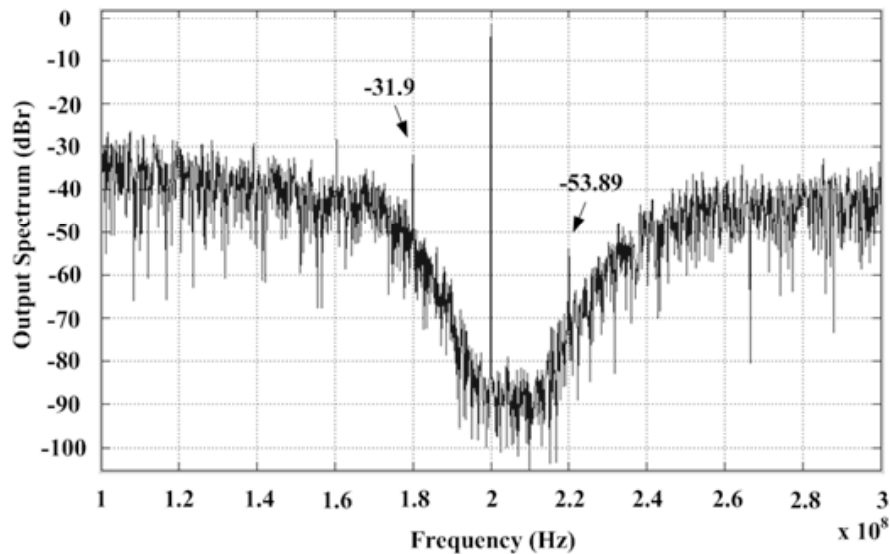
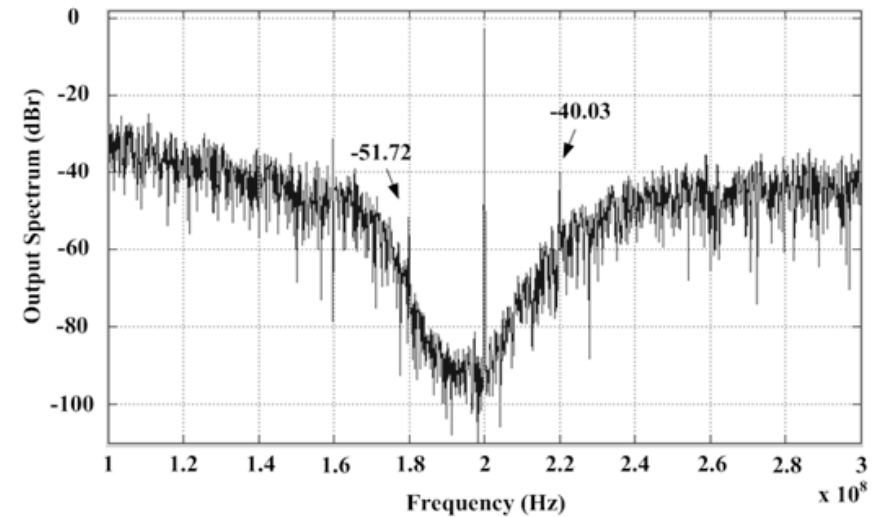
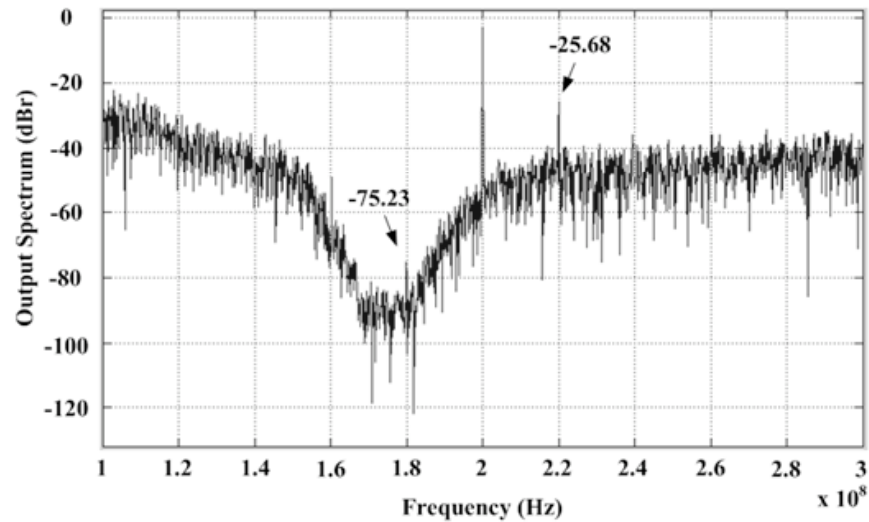
- Loop Stability
- Best NTF
- Bandwidth

Digitally assisted calibration scheme



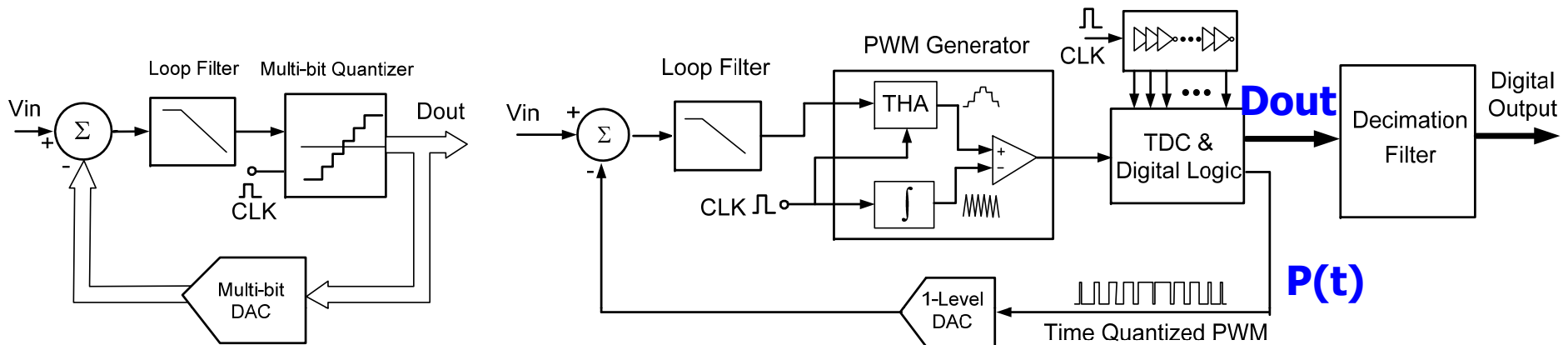
A 6th-Order 200MHz IF Bandpass Sigma-Delta Modulator With over 68dB SNDR in 10MHz Bandwidth, C.Y. Lu, et.al., *IEEE J. Solid-State Circuits*, June 2010.

ADC Calibration: Experimental results



Design Examples

ADC Architecture Employing a TDC as Quantizer

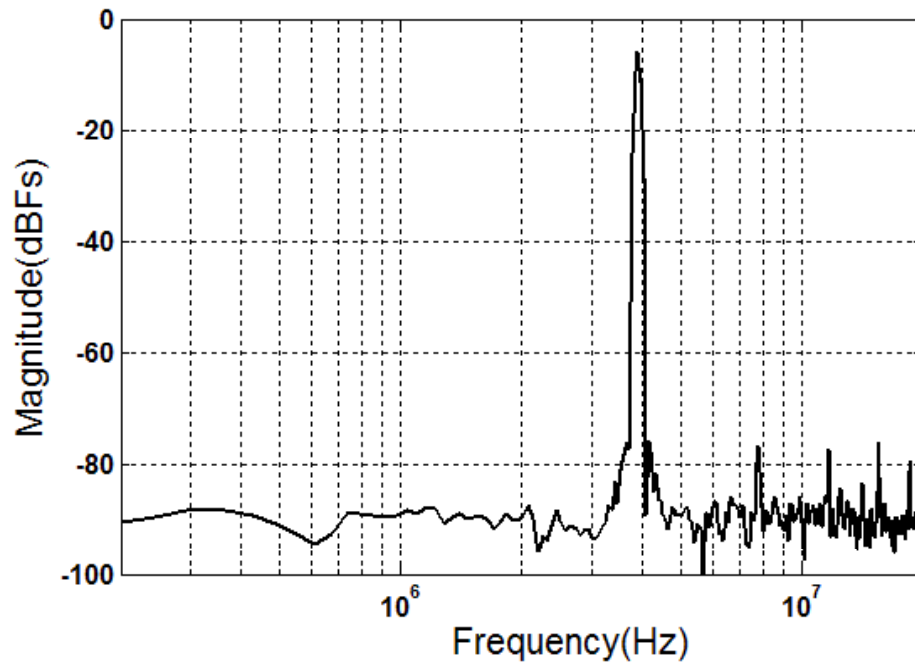


Conventional $\Delta\Sigma$

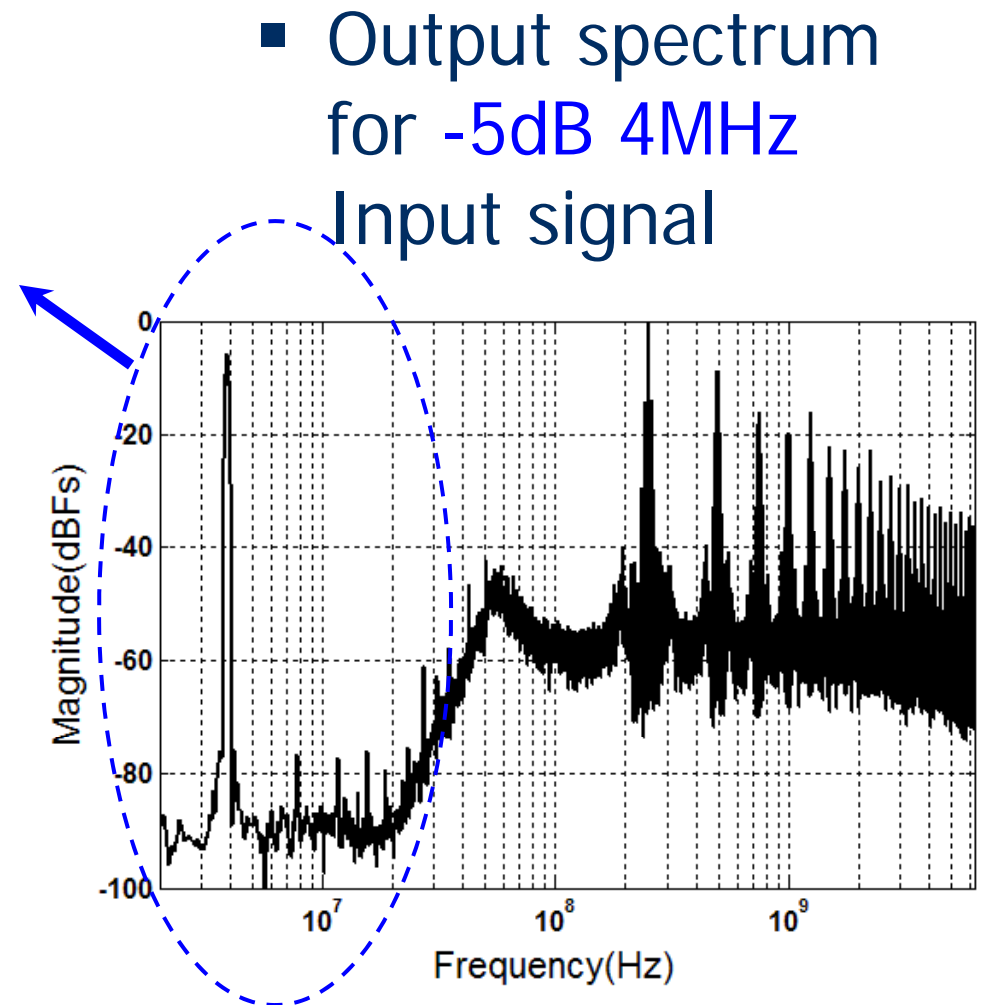
Time domain Quantizer-DAC

- Multi-level quantizer and Digital to Analog Converter (DAC) are replaced by PWM generator and Time to Digital Converter (TDC)
- Width of $p(t)$ is proportional to the amplitude of the signal in a given clock period
- Output code (Dout) represents “quantized pulse” edges with a quantization step size = T_Q

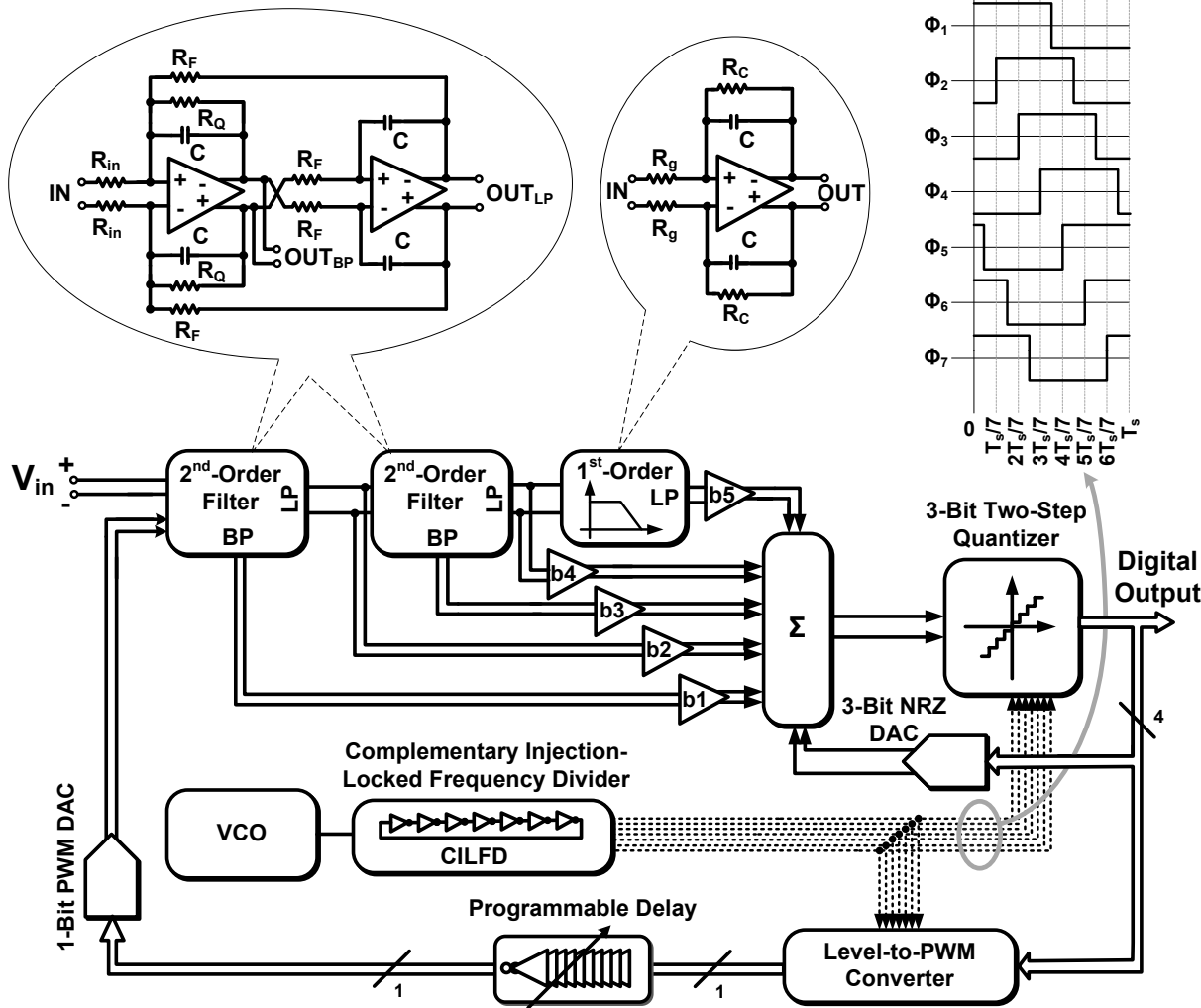
Output Spectrum: -5dB Input



- SNR=62dB
- THD=-65dB



Second ADC: System Architecture: Injection Locking



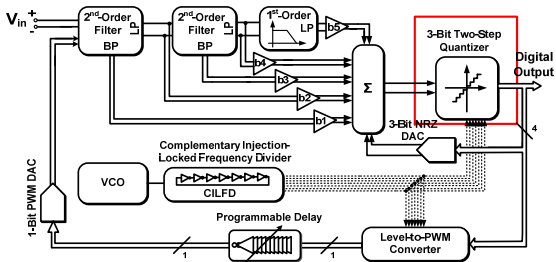
- 5th-order 3-bit feedforward architecture

- Local feedback is to compensate the excess loop delay

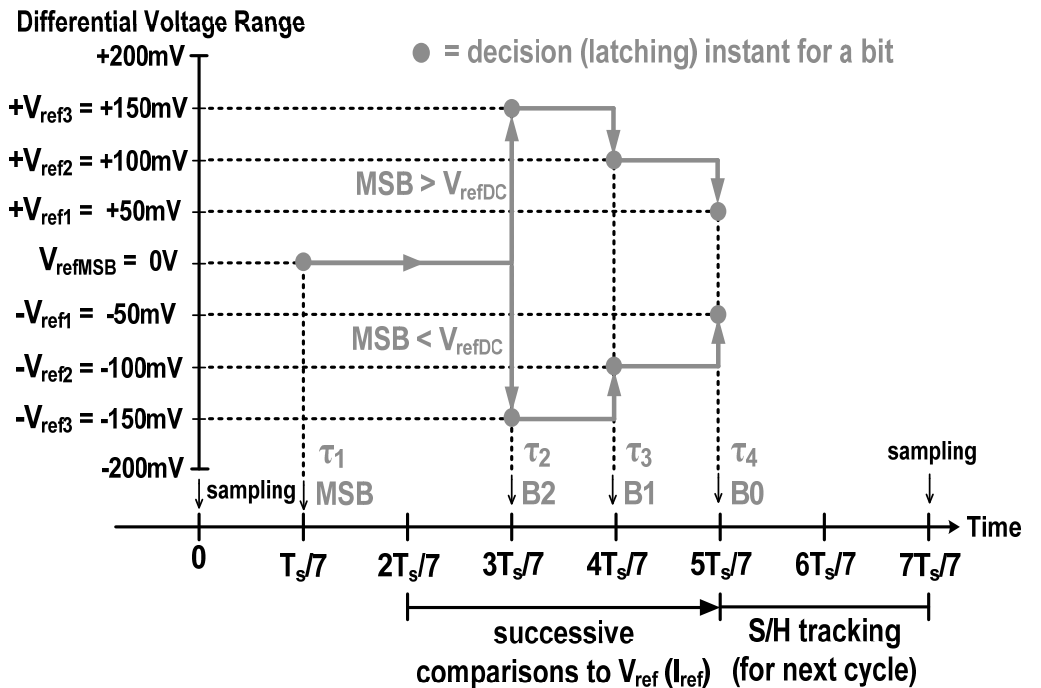
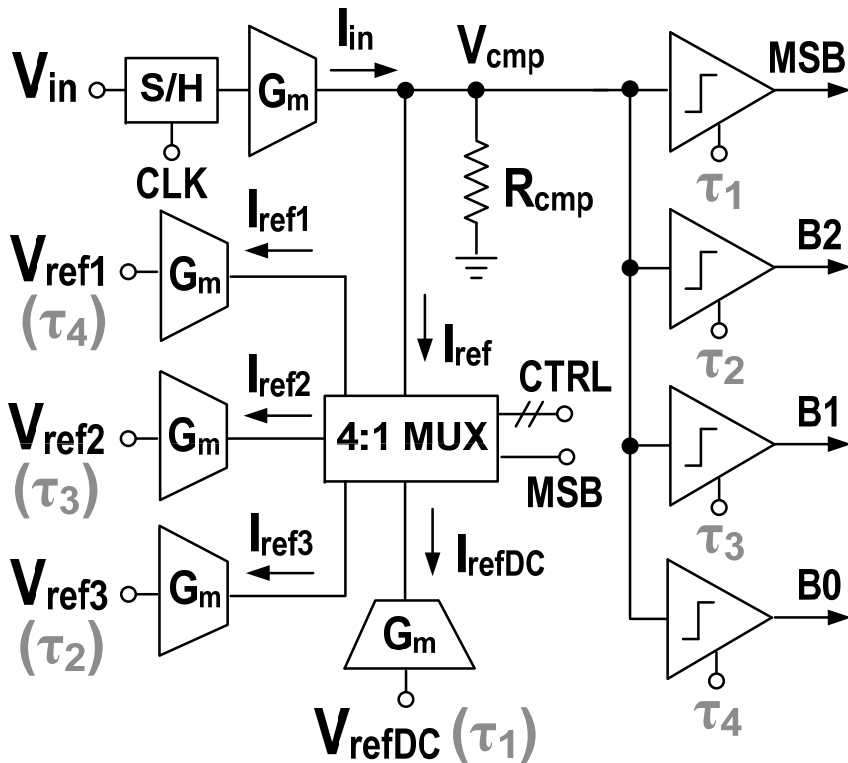
- LC-VCO+CILFD are used to generate clean reference clocks

"25MHz Bandwidth (BW) Continuous-Time Lowpass $\Sigma\Delta$ Modulator with Time-Domain 3-bit Quantizer and DAC" Cho-Ying Lu, et.al., Sept 2010, JSSC

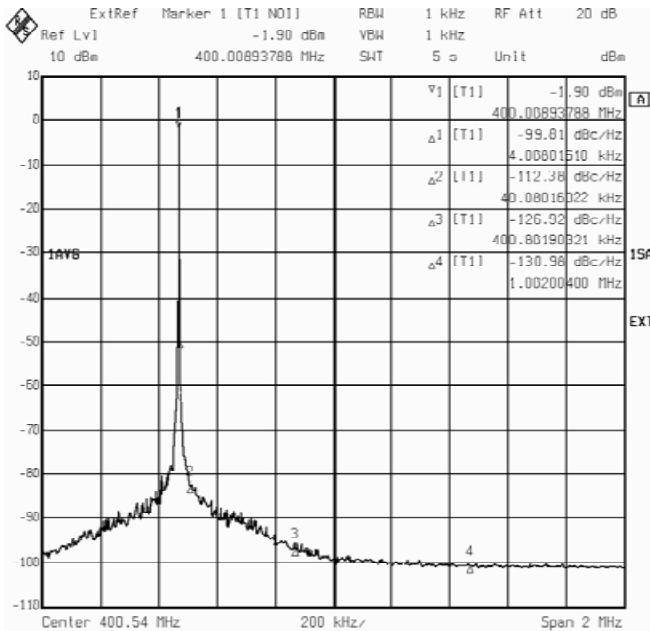
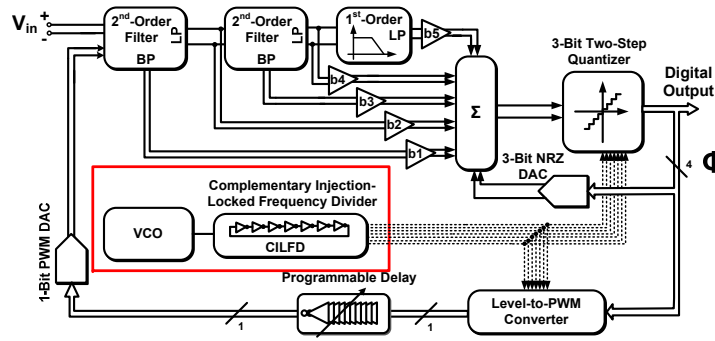
3-bit Algorithmic Quantizer



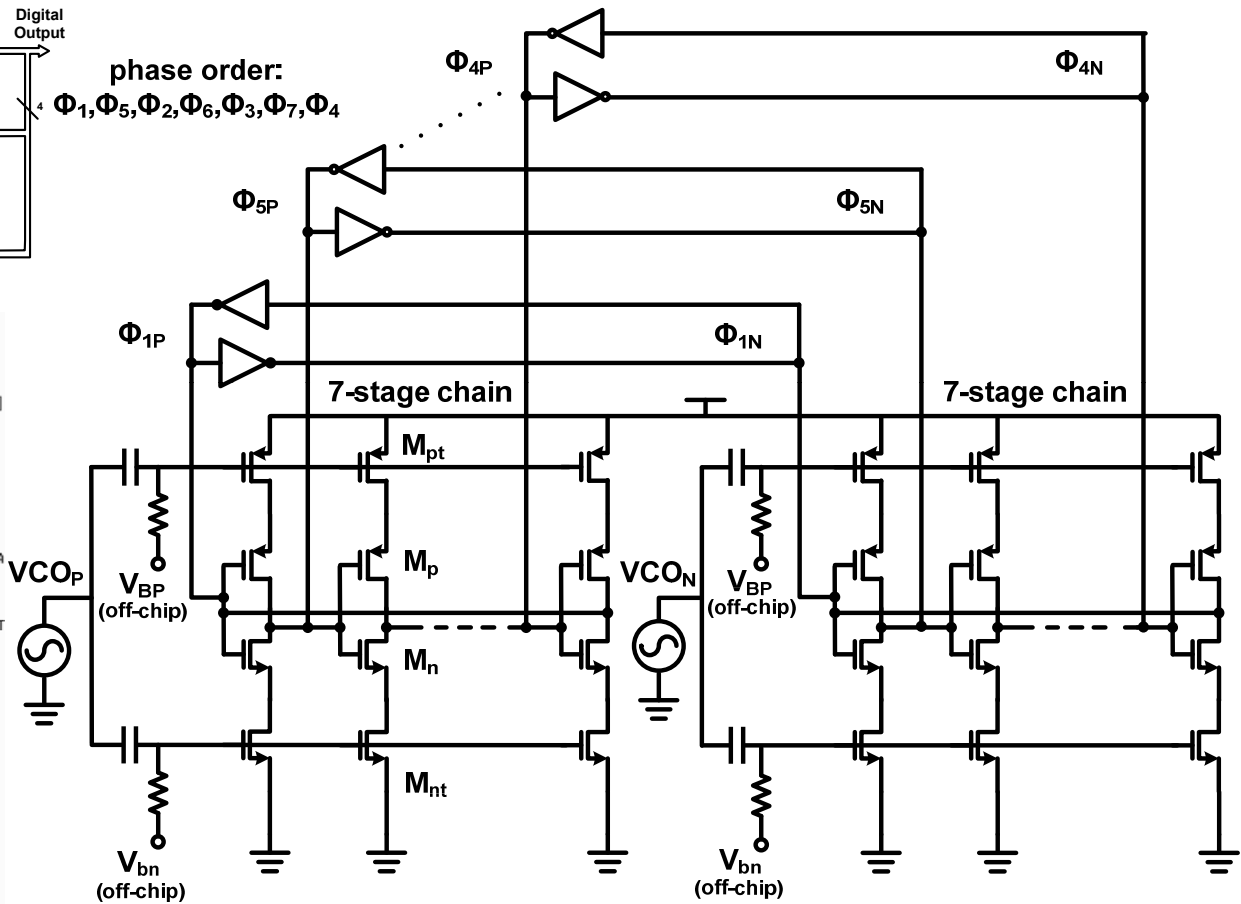
- The output is composed by **1 MSB + 3LSB**
- The MSB is determined first



LC-VCO + CILFD



phase order:
 $\Phi_1, \Phi_5, \Phi_2, \Phi_6, \Phi_3, \Phi_7, \Phi_4$

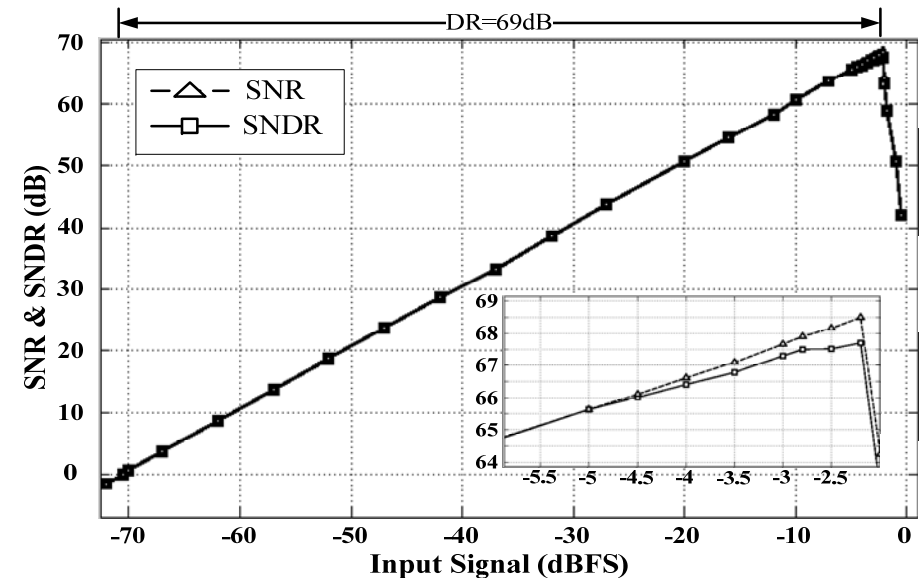
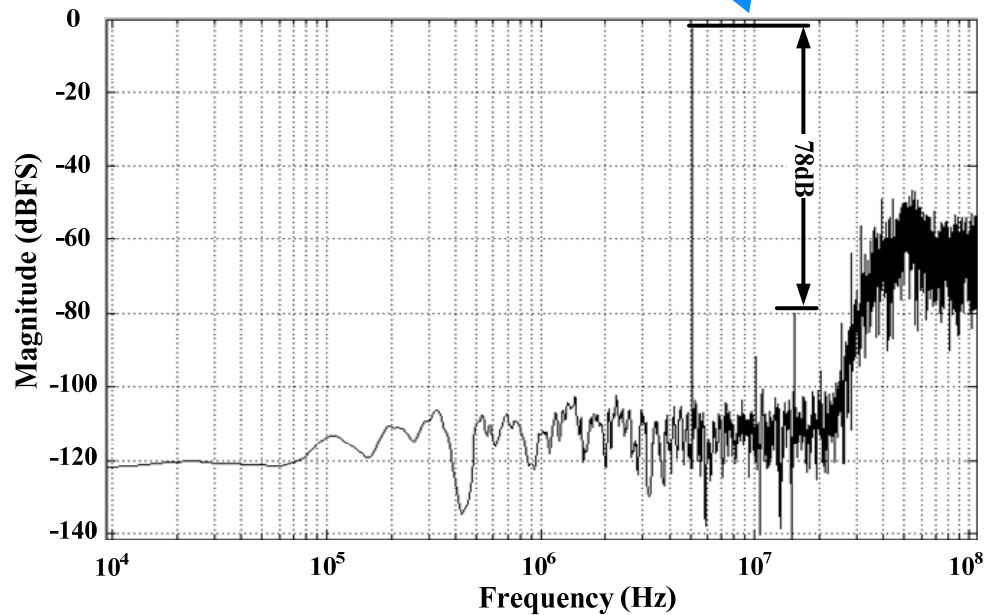


- Phase noise of VCO is -119dBc/Hz @ 1MHz
- CILFD phase noise is -136dBc/Hz @ 1MHz

Jitter among phases is highly correlated

Output Spectrum of the Modulator

-2.2dBFS @ 5.08MHz



- **Peak SNR= 68.5dB @25MHz BW**
- **Peak SNDR= 67.7dB @25MHz BW**
- **SFDR>70dB**

***Current-mode Quantizer**

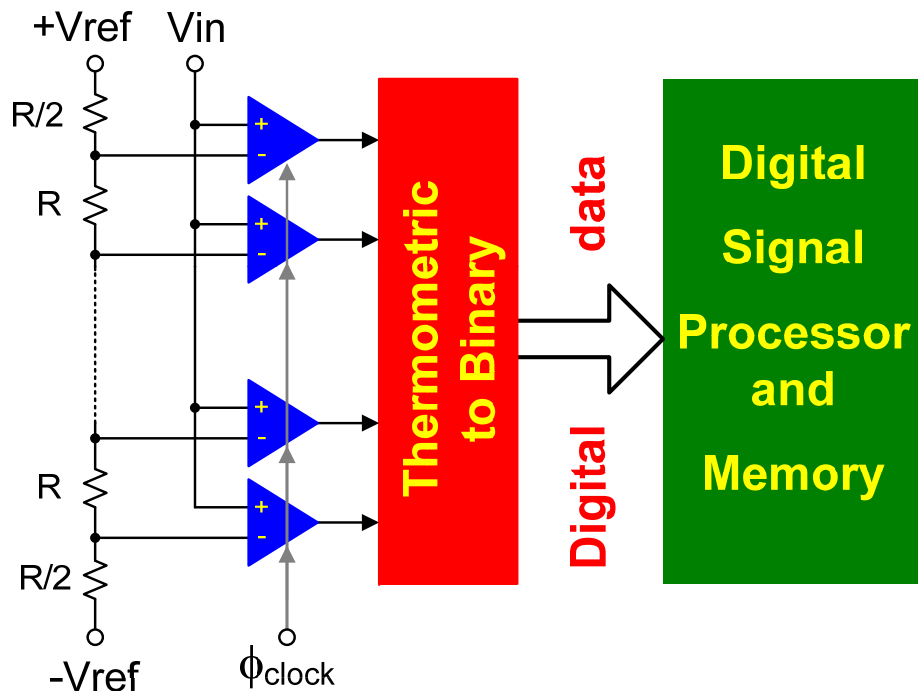
C. J. Park, **M. Onabajo, H. M. Geddada, J. Silva-Martinez, and A. I. Karsilayan

Paper under evaluation

***Partially sponsor by SRC**

**** Currently with Northeastern University**

Typical Quantizer: Flash Architecture

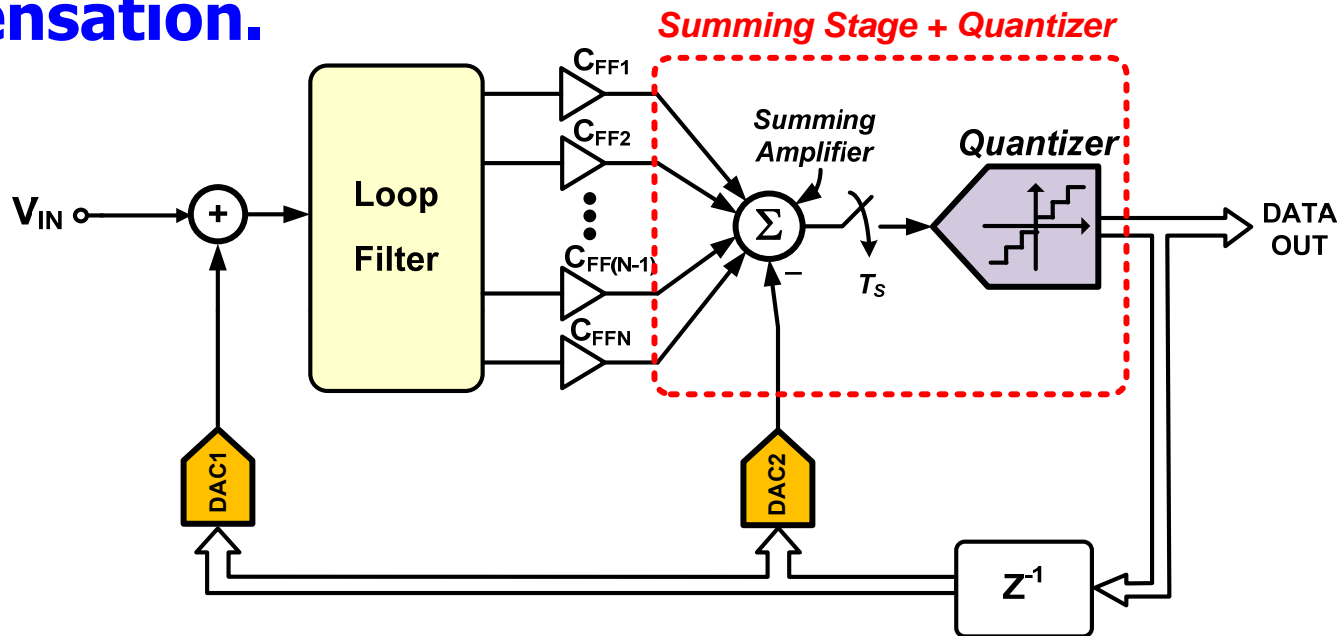


- S/H operates at clock rate
- Huge input capacitance if $N > 6$
 - Kick back noise
- Requires a precise low-impedance resistive ladder:
 - Power-accuracy-Speed tradeoff
- Limited by comparator
 - Speed and accuracy
 - Offset voltage
- Hard to improve its resolution

State of the art: $\sim > 2.4$ GS/s 6 bits resolution

Conventional ADC Architecture

- A CTSD modulator with feed-forward (FF) compensation.



- Summing stage and quantizer in the conventional continuous-time sigma-delta modulator with feed-forward compensation.
- Excess loop delay (in addition to z^{-1}) should be minimized.
- The direct path around the quantizer should be very fast.
- The summing amplifier must have a high unity-gain frequency.

Voltage Mode Quantizer

- Flash ADC architecture generally achieve the highest sampling rate and is used as integrated quantizers in sigma-delta modulator
- Performance summary of prior Adder-Quantizer in CT $\Sigma\Delta$ Modulators

	[23]	[29]		
Technology (nm)	180nm CMOS	180nm CMOS		
Supply voltage	1.8V	1.8V		
Quantizer Resolution	3 bits	4 bits		
Sampling rate	400MHz	800MHz		
Input range	400mV _{pp}	3V _{pp}		
Power	Adder*	10mW	Adder*	8.5mW
	Flash ADC**	24mW	Flash ADC	N/A

* Power consumption of the summing amplifier only.

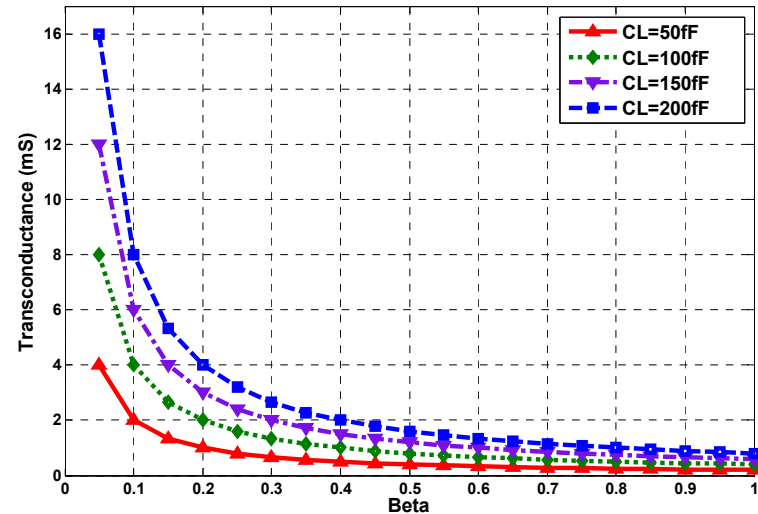
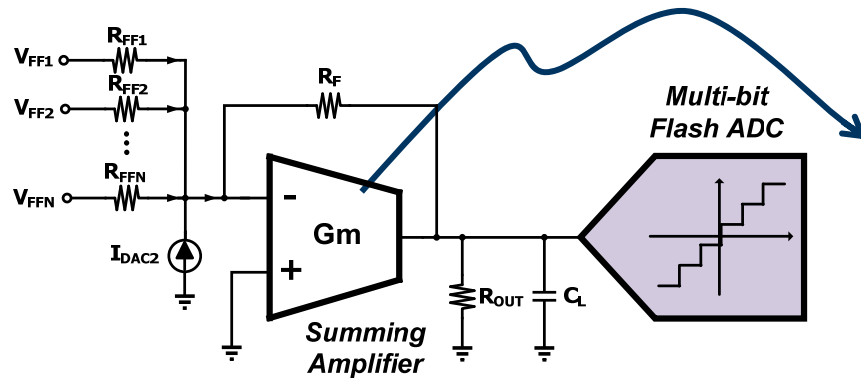
** 3-bit two-step Flash ADC.

[23] C.-Y. Lu, M. Onabajo, V. Gadde, Y.-C. Lo, H.-P. Chen, V. Periasamy, and J. Silva-Martinez, "A 25MHz bandwidth 5th-order continuous-time lowpass sigma-delta modulator with 67.7dB SNDR using time-domain quantization and feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795-1808, Sep. 2010.

[29] V. Singh, N. Krishnapura, S. Pavan, B. Vignanam, D. Behera, and N. Nigania, "A 16MHz BW 75dB DR CT $\Sigma\Delta$ ADC compensated for more than one cycle excess loop delay," *IEEE J. Solid-State Circuits*, vol. 47, no. 8 pp. 1884-1895, Aug. 2012.

- Demand for low power consumption
- Make the architecture robust to process-voltage-temperature (PVT) variations

Conventional Voltage-Mode Summing and Flash ADC



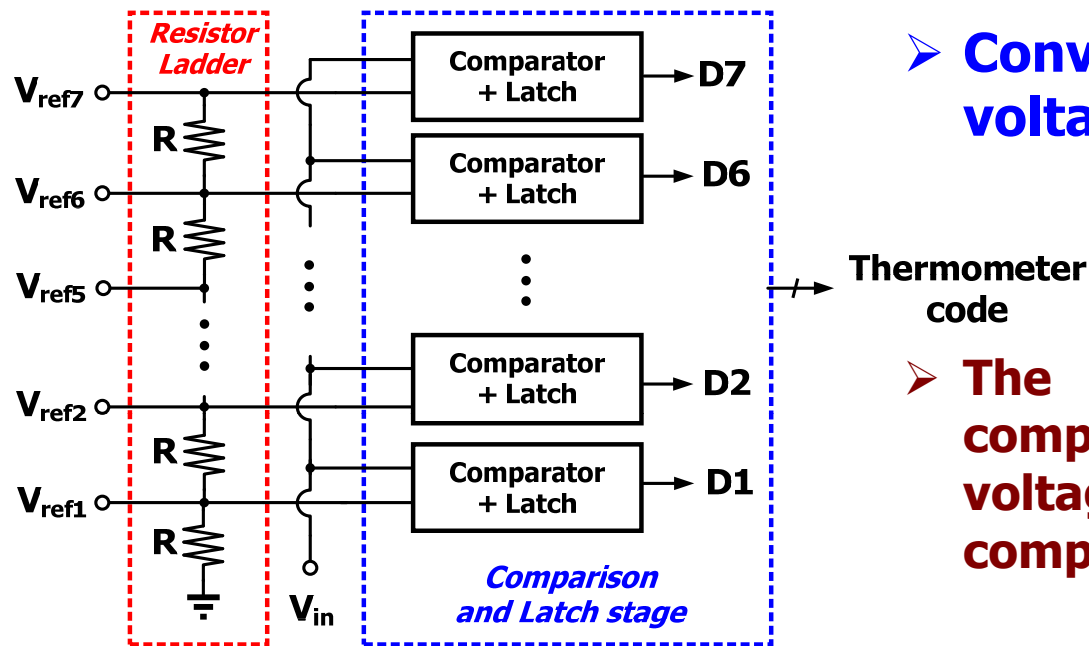
- The cap
- The five

✓ The minimum transconductance required is usually dictated by the value of DC loop gain requirement

✓ As an example, the case of 26dB DC loop gain with $R_{FF1} || \dots || R_{FFN} = 500\Omega$ demands $G_m > 40\text{mA/V}$

han

Conventional Voltage-Mode Flash ADC

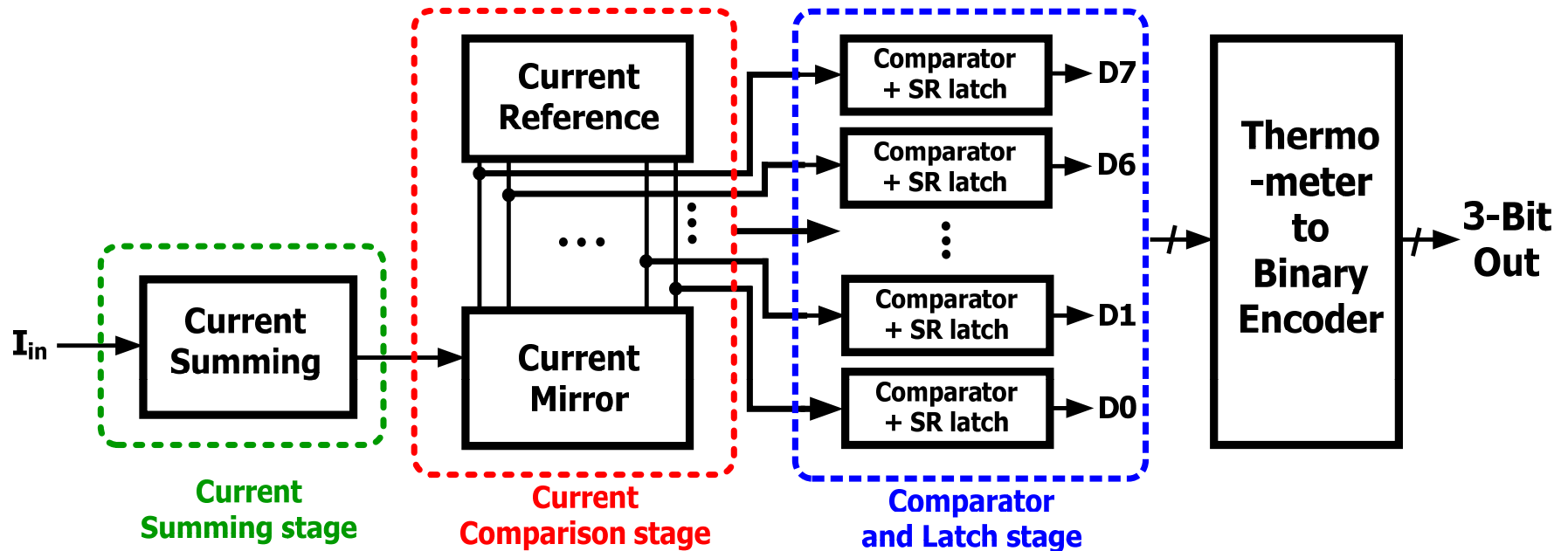


➤ Conventional 3-bit voltage-mode flash ADC

- The input signal (V_{in}) is compared to seven reference voltage levels using seven comparators followed by latches.

- To minimize the impact of PVT, large area resistors (R) and intricate layout matching techniques are required
- Larger transistor dimensions would be counterproductive with regards to the maximum achievable speed
- To minimize the effects of the kickback noise, relative small values are preferred for the resistors (R) at the expense of larger static power consumption

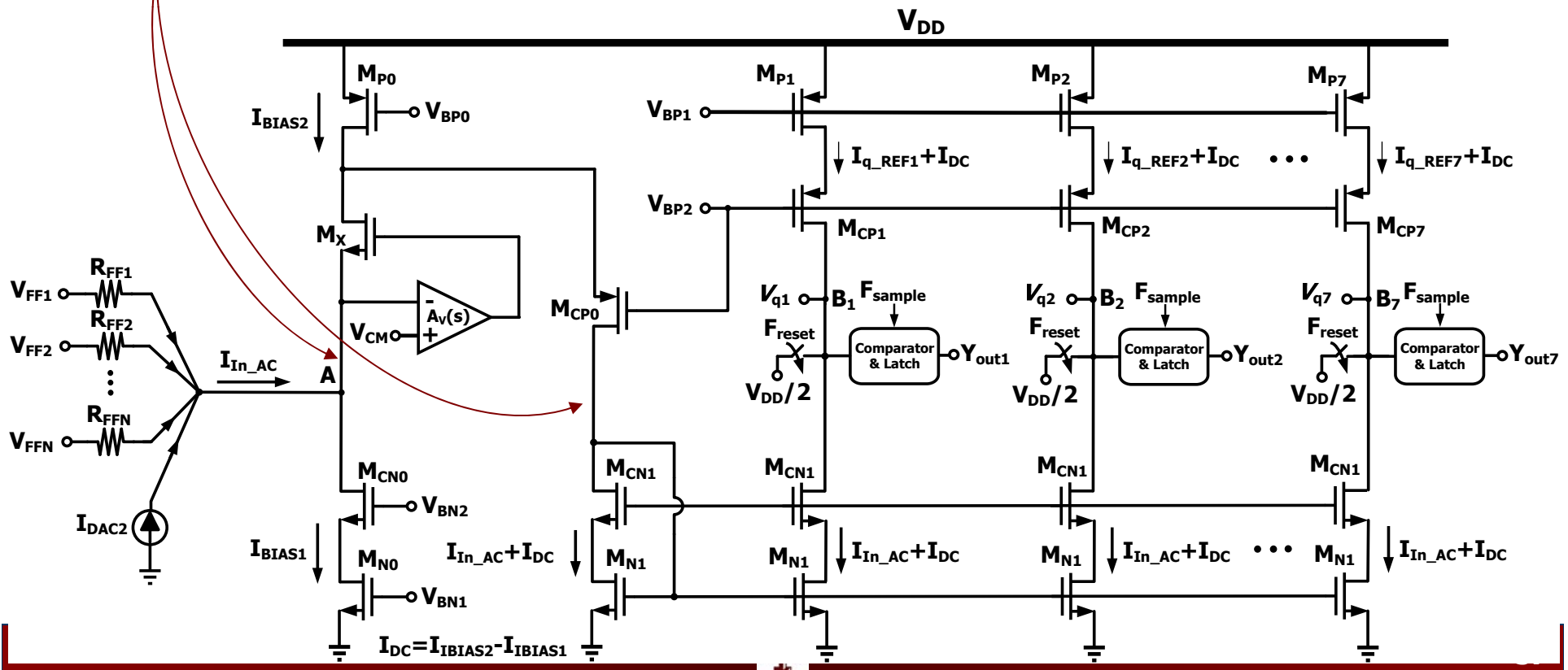
Proposed Current-Mode Flash ADC Architecture



- **Incoming signals are added at the source of a common-gate stage**
- **Input signals are replicated through NMOS current mirrors and compared with reference currents at high impedance nodes**
- **The difference between input signal replicas and reference currents are converted to voltages at high impedance nodes**
- **The different voltages are processed by seven comparator-latch combinations**

Current-Mode Adder-Quantizer

- ❑ Minimum input impedance
 - ❑ Easy to interface it with loop filter and easy to implement the addition of filter coefficients
- **Main design challenges:**
- ❑ Two relevant parasitic poles limit its frequency response: Still can operate at GHz
 - ❑ Resolution is limited by current mirror mismatches



Voltage-Mode Summing vs. Current-Mode Summing

Table II. Voltage-Mode Summing vs. Current-Mode Summing.

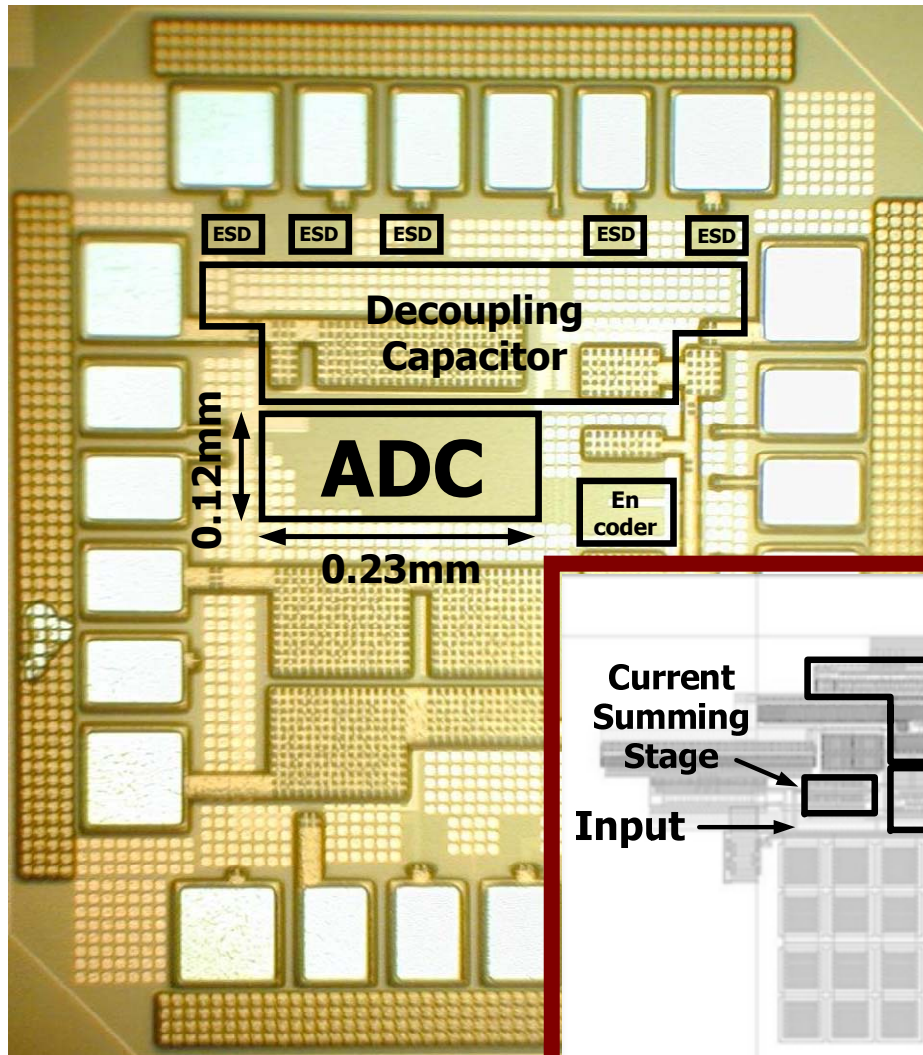
	Voltage-Mode Summing	Current-Mode Summing
Technology (nm)	90nm CMOS	90nm CMOS
Power Consumption(mW)	6.6mW*	3.1mW**
Input referred integrated noise (in 20MHz)	31.2 μ V	39 μ V
Delay (@ $V_{LSB/4}$)	0.396ns	0.35ns

* Power consumption of the summing amplifier only.

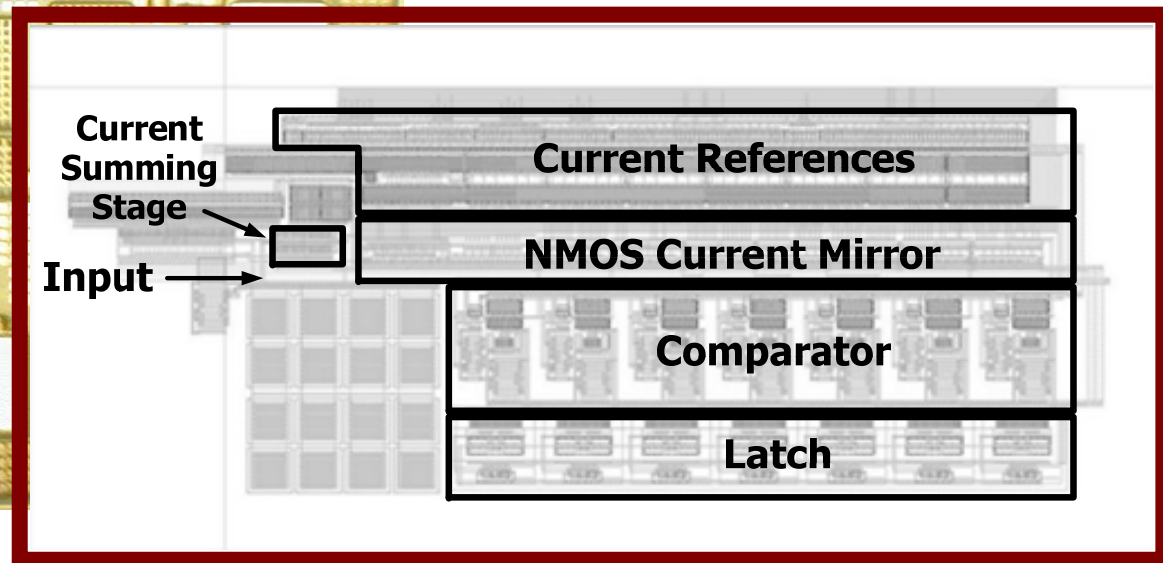
** Power consumption includes common-gate (CG) stage, Gm-boosting block and current mirroring stages.

- **The most remarkable advantages of the Current-Mode approach:**
 - **Superior performance with <50% power consumption.**
 - **Less silicon area**
- **In the Voltage-Mode case:**
 - **Additional power should be added to account for the reference voltages generator**
 - **The dual differential pair required at the input of each comparator.**

Chip Microphotograph



- The ADC area including bias circuitry: 0.0276mm^2
- The thermometer-to-binary encoder: 0.0072mm^2 .



State of the art

➤ Performance summary of the Proposed Current-Mode Adder-Quantizer and comparison with prior Quantizer in CT $\Sigma\Delta$ Modulators

	[23]	[29]	This Work		
Technology (nm)	180nm CMOS	180nm CMOS	90nm CMOS		
Supply voltage	1.8V	1.8V	1.2V		
Quantizer Resolution	3 bits	4 bits	3 bits		
Sampling rate	400MHz	800MHz	up to 2GHz		
Input range	400mV _{pp}	3V _{pp}	$\pm 40\mu\text{A}_{pp}$ (equivalent to 400mV _{pp})		
Power	Adder*	10mW	Adder	1.1mW	
	Flash ADC**	24mW	Flash ADC	N/A	Flash ADC

* Power consumption of the summing amplifier only.

** 3-bit two-step Flash ADC.

[23] C.-Y. Lu, et.al., "A 25MHz bandwidth 5th-order continuous-time lowpass sigma-delta modulator with 67.7dB SNDR using time-domain quantization and feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795-1808, Sep. 2010.

[29] V. Singh, N. Krishnapura, S. Pavan, B. Vignraham, D. Behera, and N. Nigania, "A 16MHz BW 75dB DR CT $\Sigma\Delta$ ADC compensated for more than one cycle excess loop delay," *IEEE J. Solid-State Circuits*, vol. 47, no. 8 pp. 1884-1895, Aug. 2012.

State of the art

	[20]*	[21]**	This Work
Technology	CMOS 0.13 μ m	CMOS 0.18 μ m	CMOS 90nm
Supply voltage	1.2V	Analog: 1.8V Digital: 2.1-2.5V	1.2V
Resolution	5 bits	4 bits	3 bits
Sampling rate	up to 3.2GS/s	up to 4GS/s	up to 2GS/s
Input range	400mV _{pp}	± 460 mV _{pp}	± 40 μ A _{pp}
Power	120mW	Analog	78mW
		Digital (Including Clock Buffer)	530mW
DNL (INL)		Analog	3.34mW
		Digital (Including Clock Buffer)	8.94mW
	4.54 bits (3.2GS/s)	3.47 bits (3.4GS/s, 800MHz input)	2.54 bits (1.48GS/s, 118.4MHz input)
Area	0.18mm ²	0.88mm ² (excluding resistor ladder)	ADC: 0.0276mm ² (excluding encoder)

Power consumption if extrapolated to 5 bits is less than 16mW for current-mode realization

* Power consumption of output buffer was not included.

** Includes power consumptions for analog circuitry and digital encoder. For the FoM calculation, the digital power consumption for 4GS/s.

[20] Y.-Z. Lin, et. al, "A 5-bit 3.2-GS/s flash ADC with a digital offset calibration scheme," IEEE Trans. Very Large Scale Integration Systems, vol. 18, no. 3, pp. 509-513, March 2010.

[21] S. Park, et. al, "A 4-GS/s 4-bit Flash ADC in 0.18 μ m CMOS," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp.1865-1872, Sep. 2007.

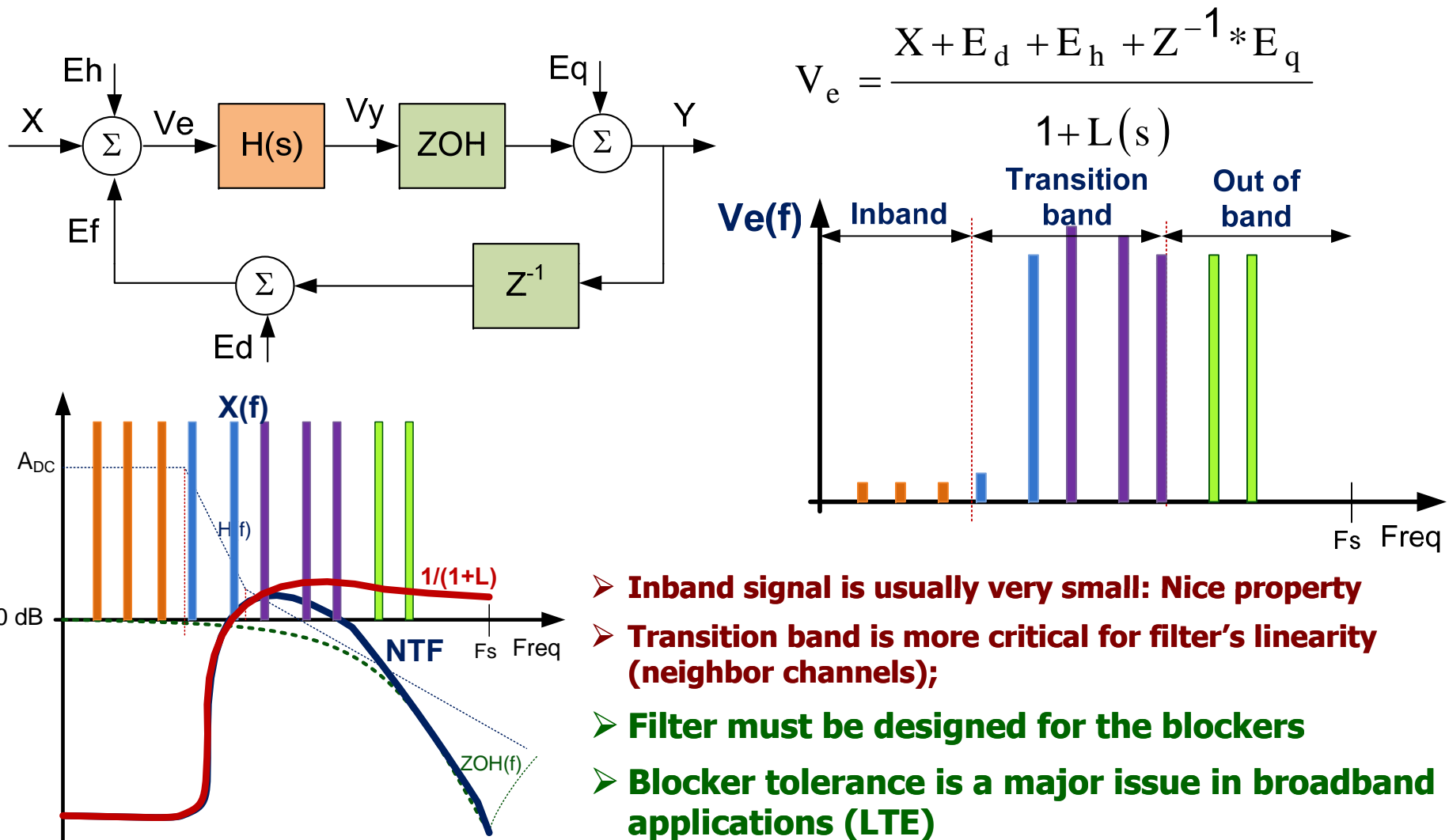
A Blocker Tolerant Continuous-Time $\Delta\Sigma$ ADC for Broadband Applications*

H. M. Geddada, C. J. Park, H.-J. Jeon**, J. Silva-Martinez, and A. I. Karsilayan

*Sponsored by SRC

Effect of the blockers on loop operation

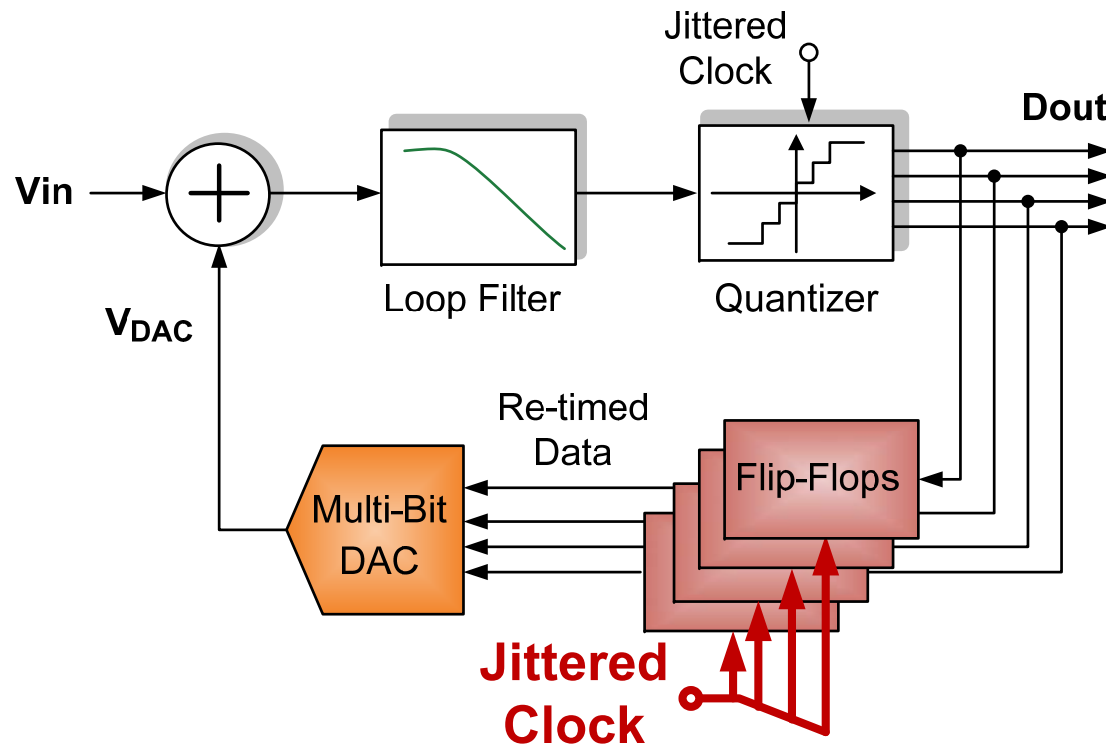
➤ Remarks on Filter's operation: Filter's input signal



- **Inband signal is usually very small: Nice property**
- **Transition band is more critical for filter's linearity (neighbor channels);**
- **Filter must be designed for the blockers**
- **Blocker tolerance is a major issue in broadband applications (LTE)**

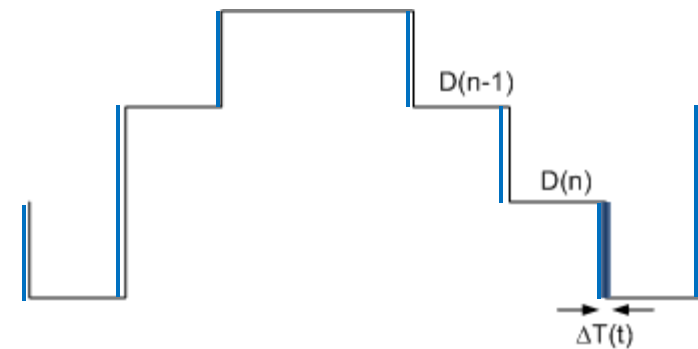
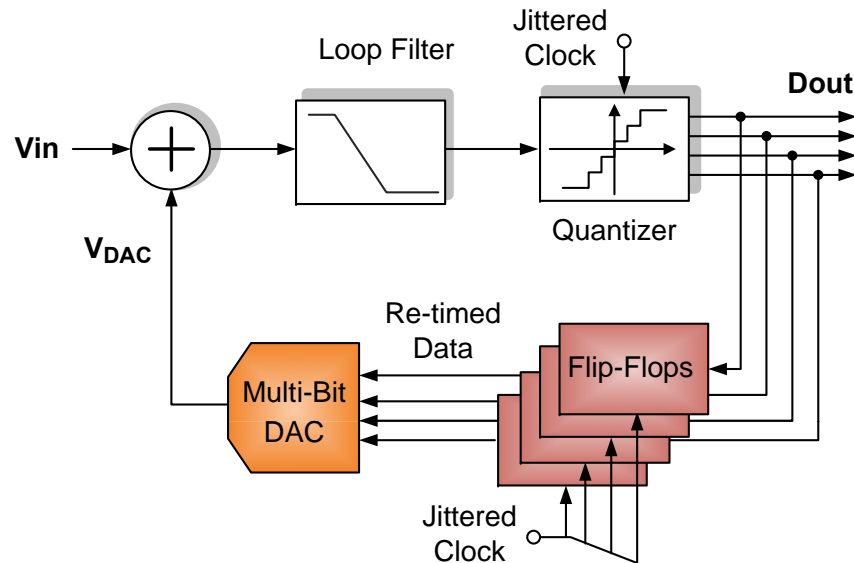
Clock Jitter Sensitivity (SJNR)

- The main effects of clock jitter is present at the input of the quantizer and DAC.
- Jitter induced noise at DAC output is processed according to the STF, which is a serious problem for continuous-time sigma-delta modulators



- Clock Jitter in quantizer is not very relevant: processed by NTF.
- Clock jitter introduce uncertainty at the DAC output (jitter induced noise) processed by STF.

Jitter Issues: High Clock Frequency



Error Function

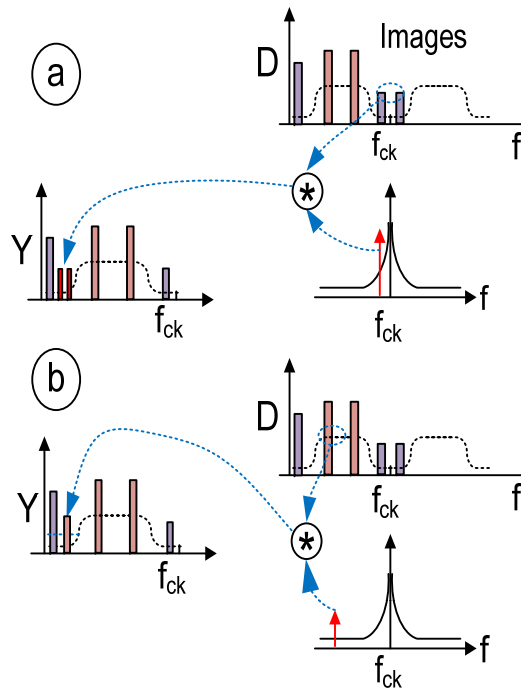
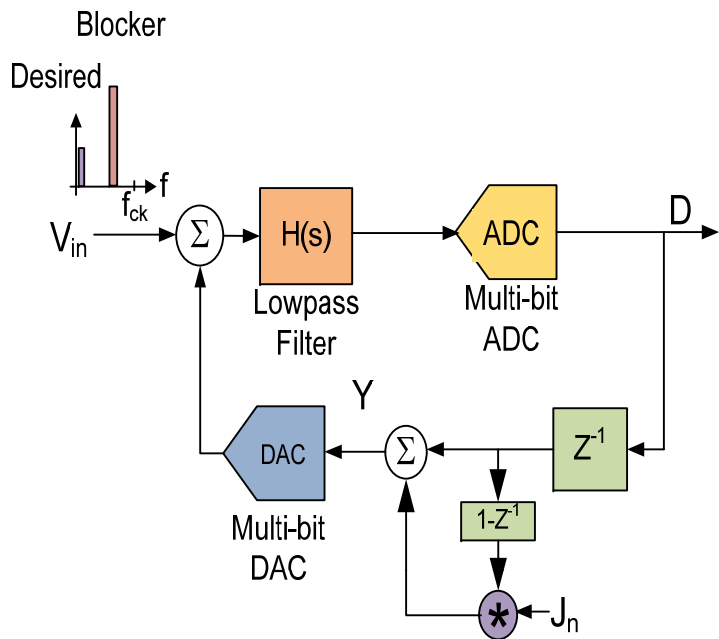
The DAC error due to clock jitter:

$$E_j(n) = (D_{out}(n) - D_{out}(n-1)) \left(\frac{\Delta T(t)}{T} \right)$$

In the frequency domain: Convolution of Differential of Dout and $J_n(\omega)$

$$E_j(\omega) = \left[(1 - Z^{-1}) D_{out}(\omega) \right] \otimes J_n(\omega) = \left[\left(2 \sin\left(\frac{\omega T_s}{2}\right) \right) D_{out}(\omega) \right] \otimes J_n(\omega)$$

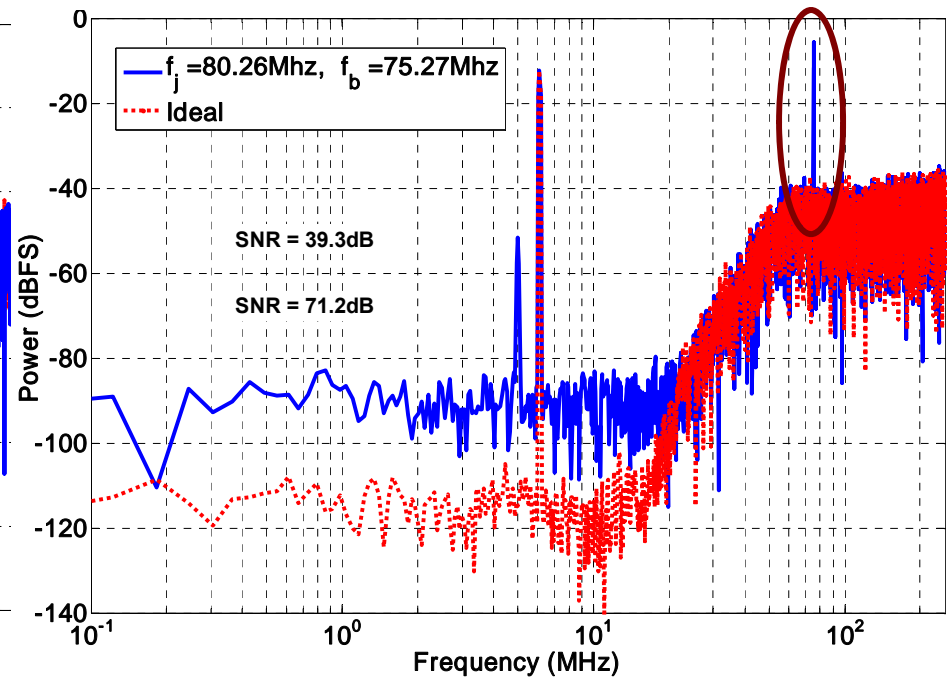
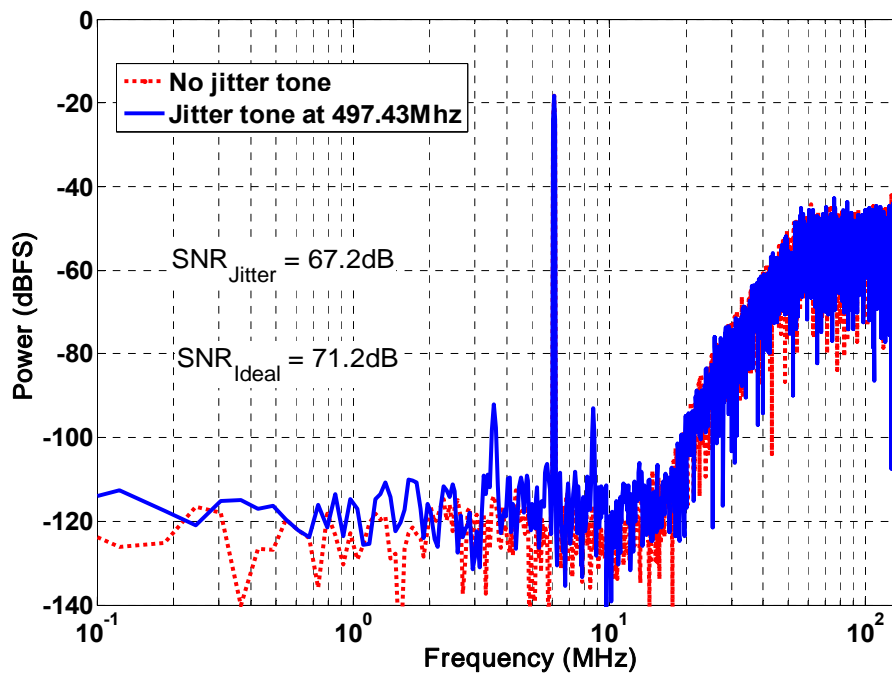
**In-band signal is shaped by $1 - Z^{-1}$, then it is not very critical
Out-of-Band quantization noise and blockers convolve with the clock jitter**



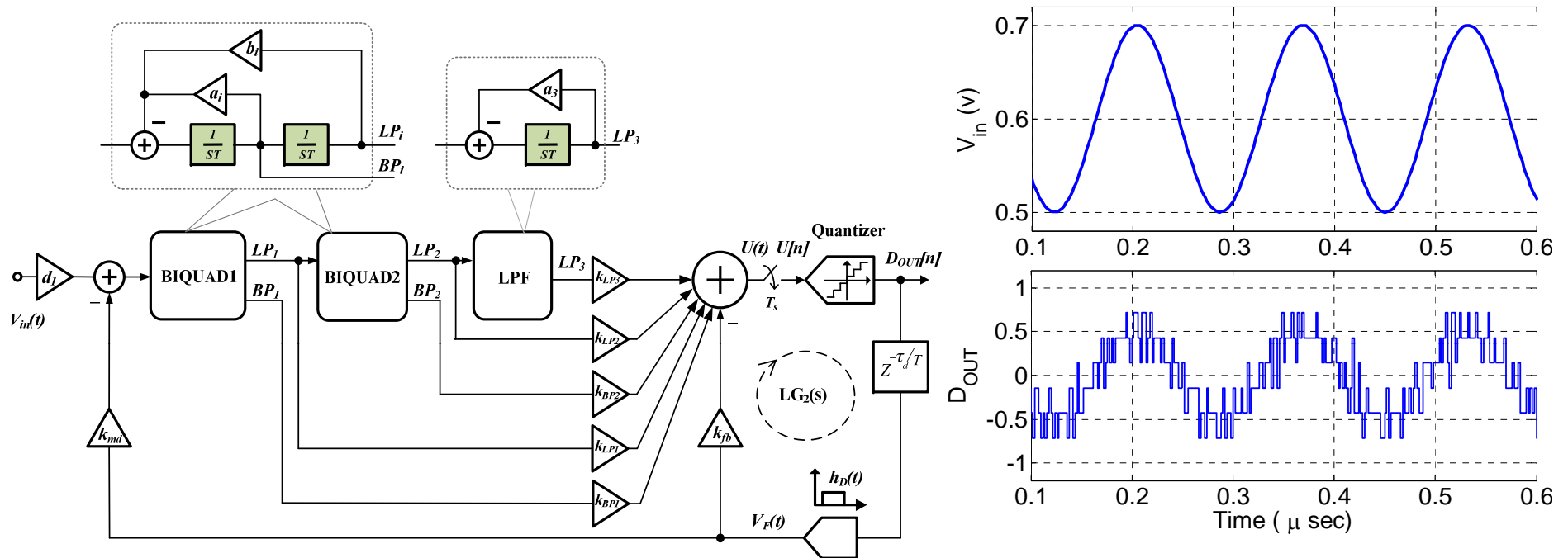
Jitter tone around F_s convolve with images of inband signal and produce in-band noise tones

➤ **Jitter and blocker convolves, producing in-band noise tones.**

➤ **Jitter also convolves with OOB quantization noise and downconverts into in-band noise.**

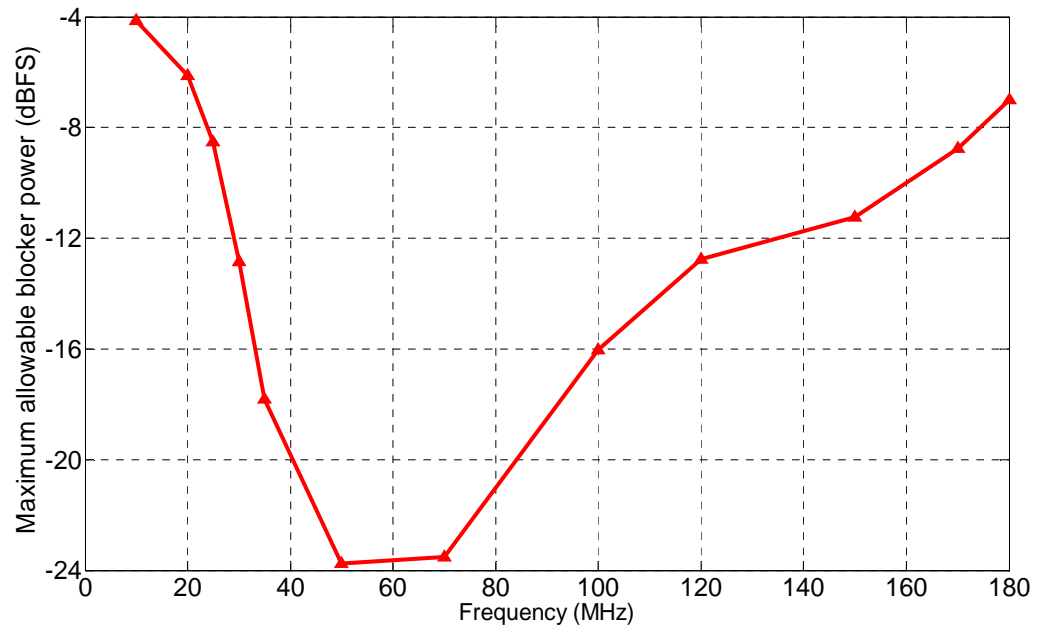
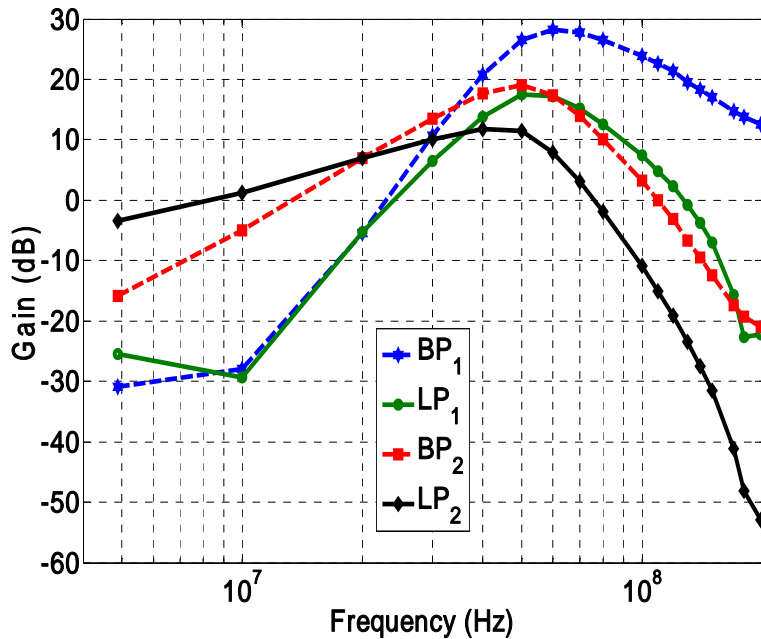
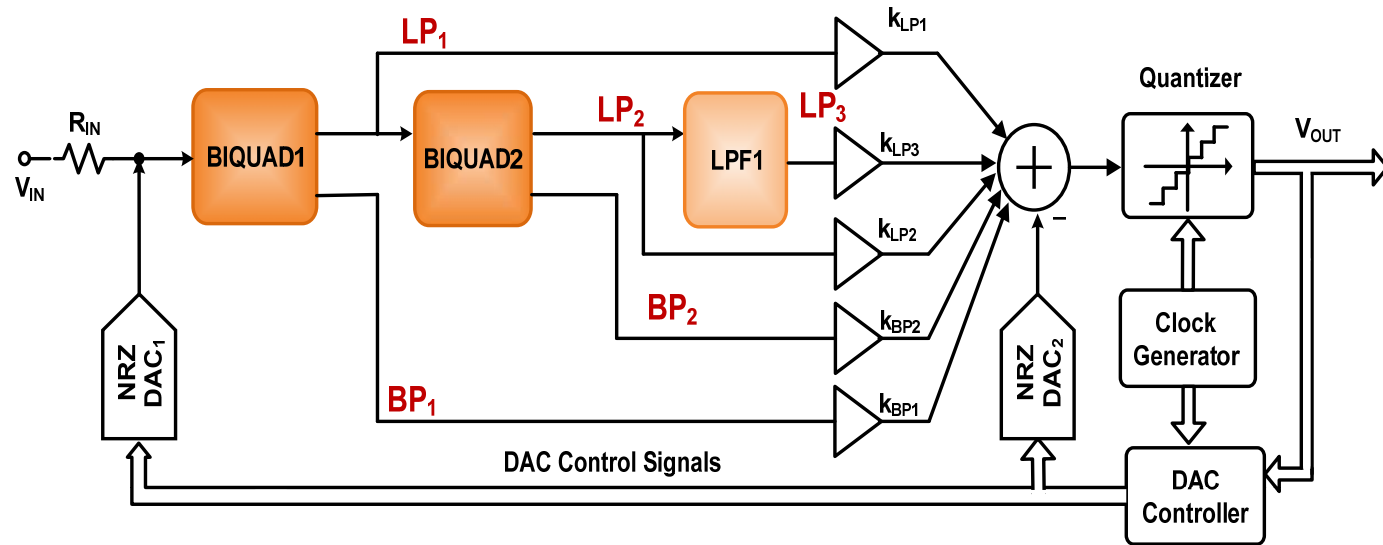


Blocker Sensitivity: Feedforward $\Delta\Sigma$ ADC



- Loop filter, ADC, DAC
- Inherent antialiasing
- $STF = FF / (1 + LG) \cong 1$ (in-band); $NTF = 1 / (1 + LG)$ (Noise shaping)
- Quantizer can have relaxed specifications
- FF architecture is power and area efficient
 - Dynamically more stable
 - OOB peaking in STF

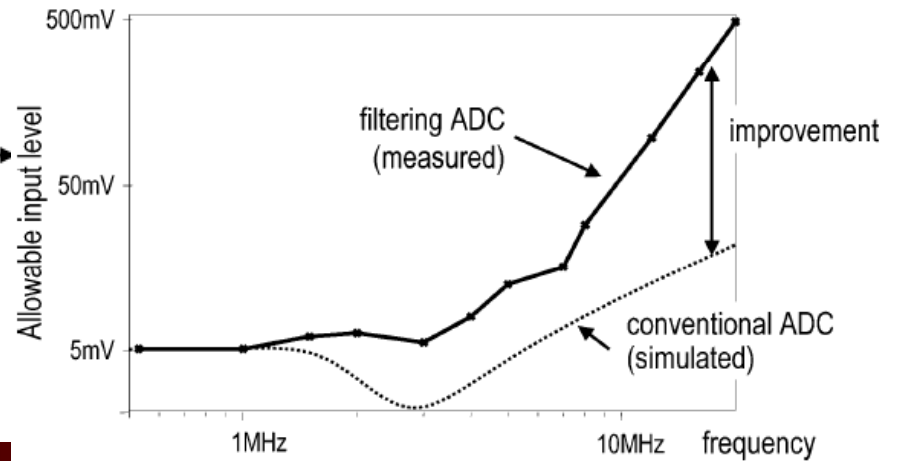
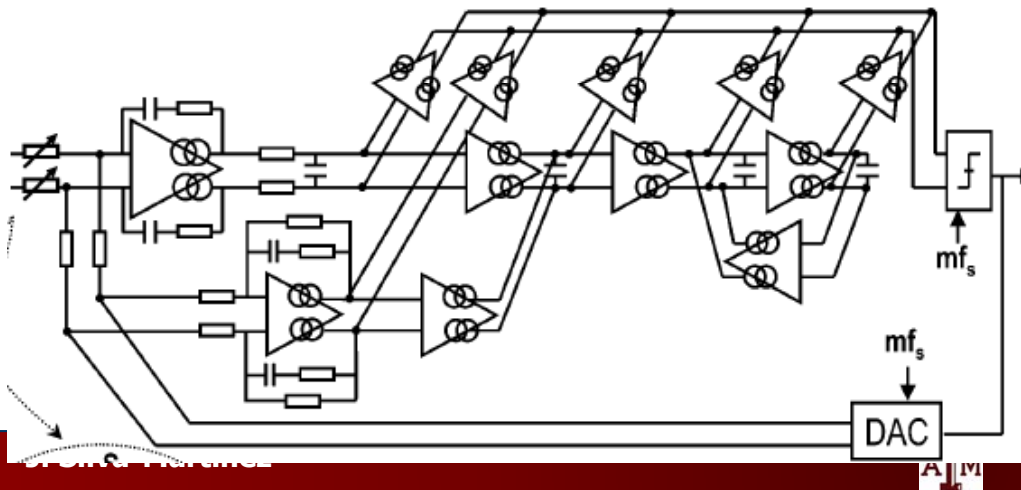
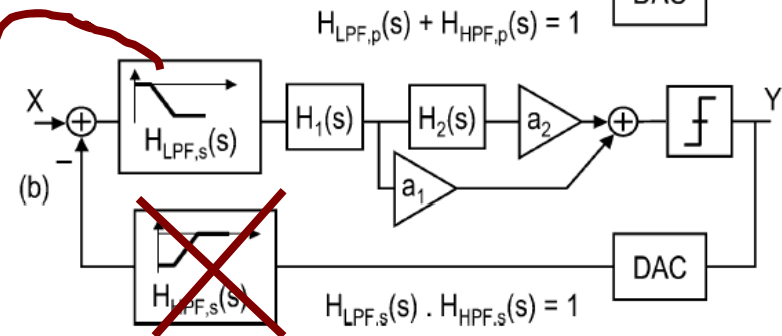
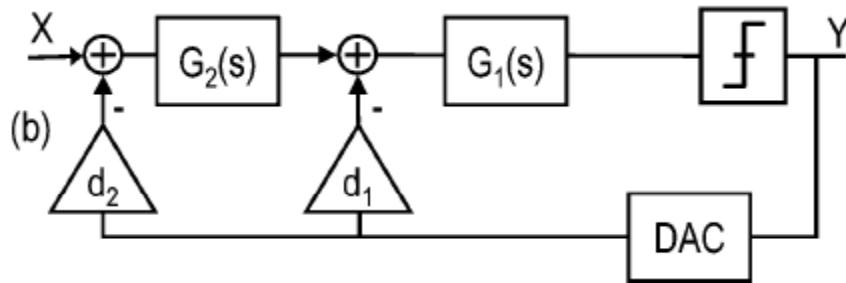
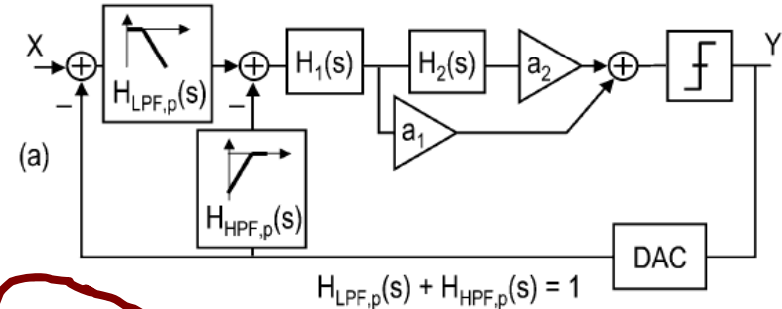
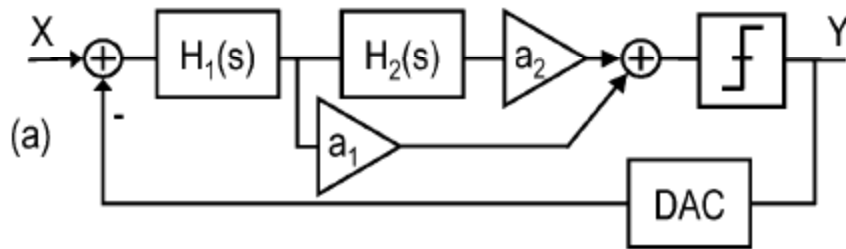
Another Major Issue: Loop Saturation



Blocker Tolerance

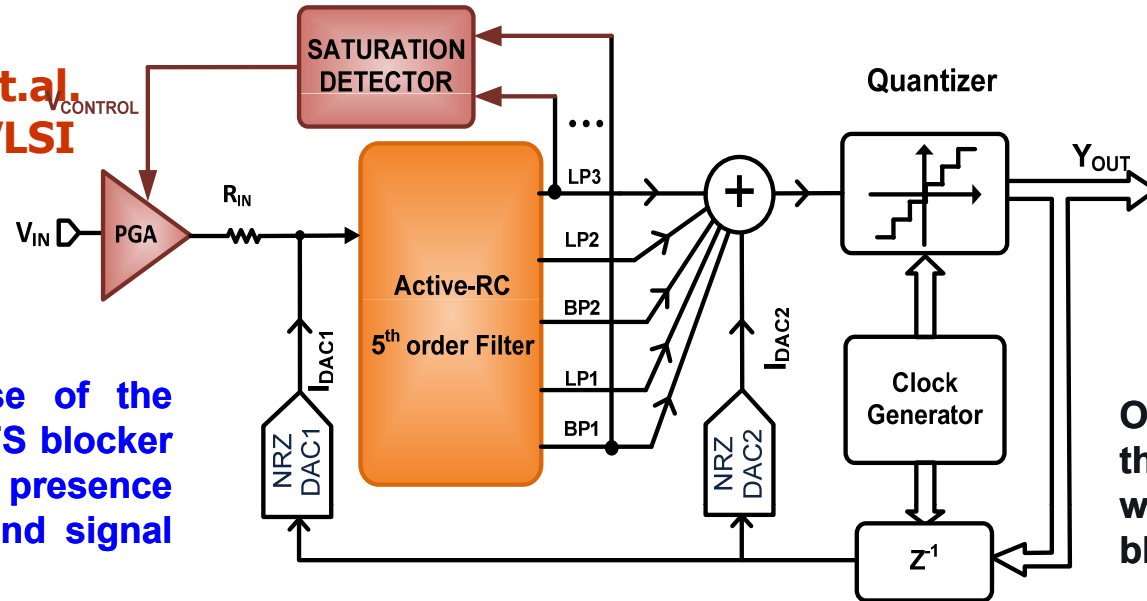
A Continuous-Time $\Sigma\Delta$ ADC With Increased Immunity to Interferers

Kathleen Philips, *Member, IEEE*, Peter A. C. M. Nuijten, Raf L. J. Roovers, *Member, IEEE*,
 Arthur H. M. van Roermund, *Senior Member, IEEE*, Fernando Muñoz Chavero,
 Macarena Tejero Pallarés, and Antonio Torralba, *Senior Member, IEEE*



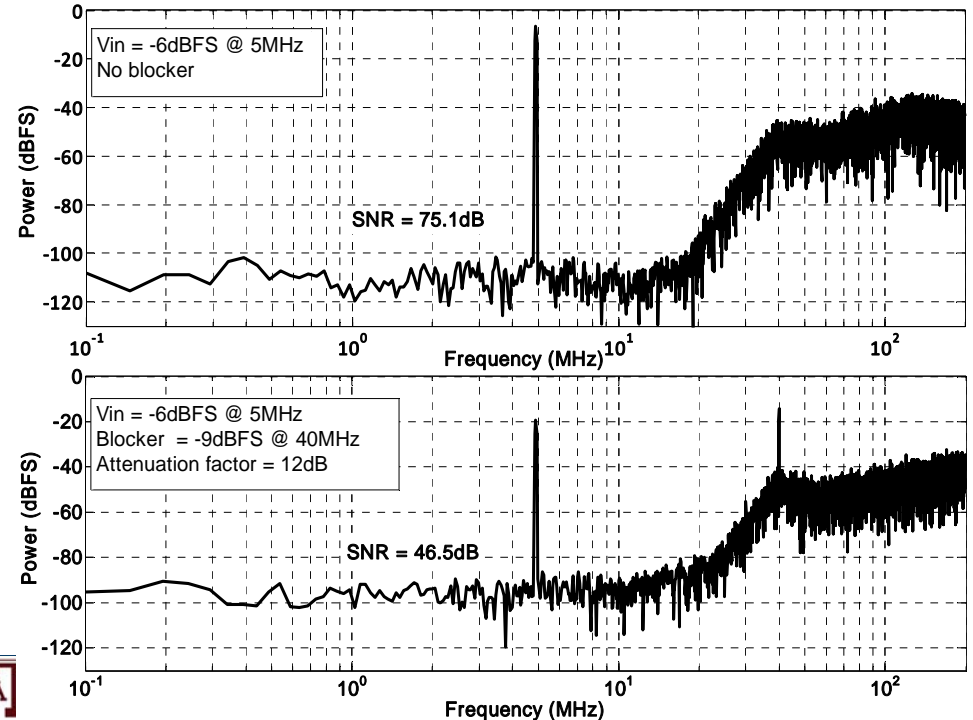
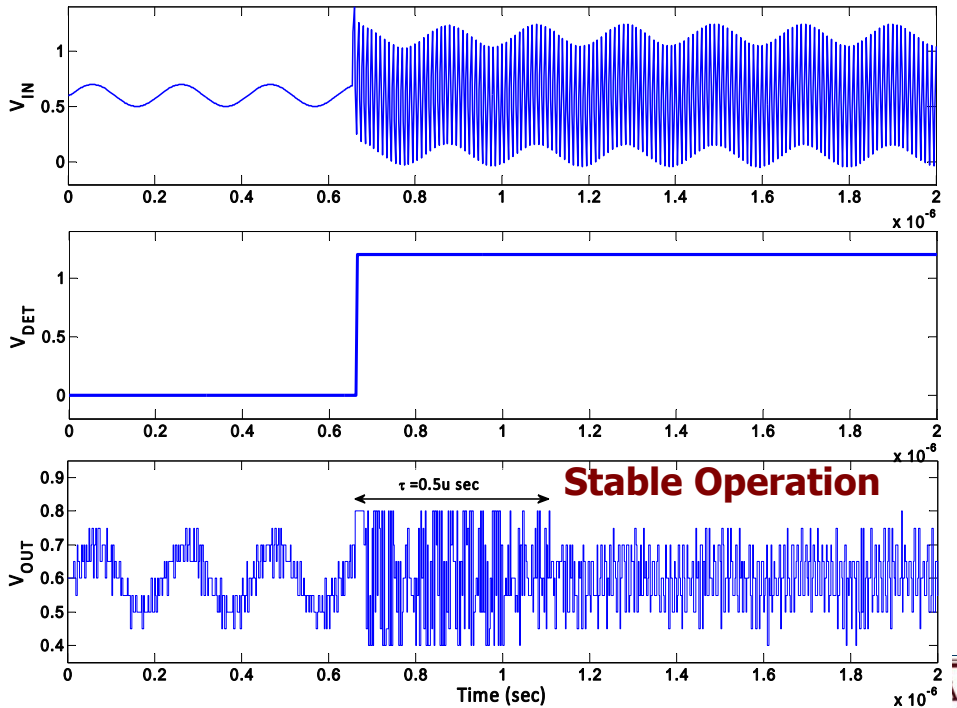
Blocker and Jitter Tolerant Wideband $\Sigma\Delta$ Modulators

H. M. Geddada, et.al.
Re-evaluation TVLSI

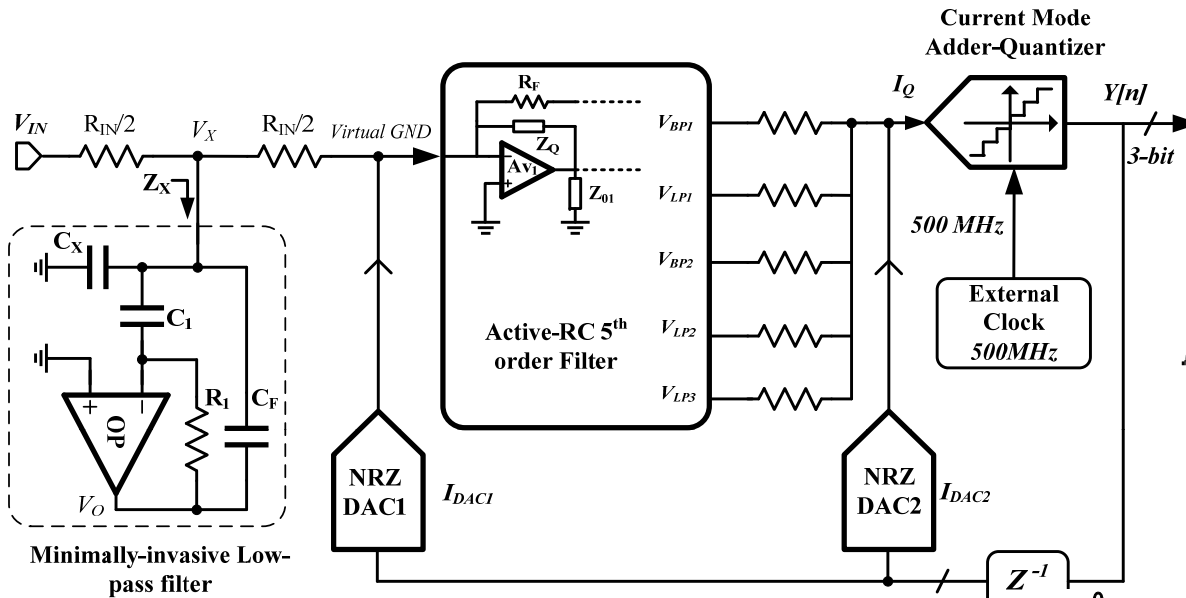


Transient response of the ADC to the 8.7dBFS blocker at 100MHz in the presence of a -6dBFS in-band signal at 5MHz

Output spectrum of the ADC with and without the -9dBFS blocker at 40MHz



Proposed minimally invasive LPF



$$\frac{V_x}{V_{tn}} = \frac{0.5\omega_{of}^2}{s^2 + \frac{\omega_{of}}{Q}s + \omega_{of}^2}$$

$$\frac{V_x}{V_{n,R1}} = \frac{1}{R_1 C_1} \cdot \frac{s}{s^2 + \frac{\omega_{of}}{Q}s + \omega_{of}^2}$$

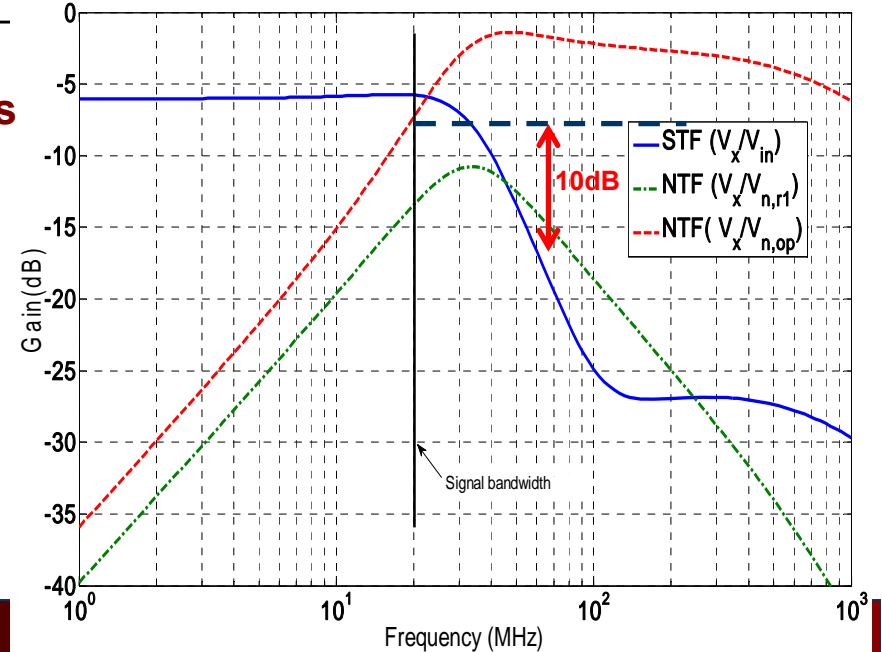
$$\frac{V_x}{V_{n,op}} = \frac{s \left(s + \frac{(C_1 + C_F)}{R_1 C_1 C_F} \right)}{s^2 + \frac{\omega_{of}}{Q}s + \omega_{of}^2}$$

$f_0 = 30\text{MHz}$
 $Q=0.7$

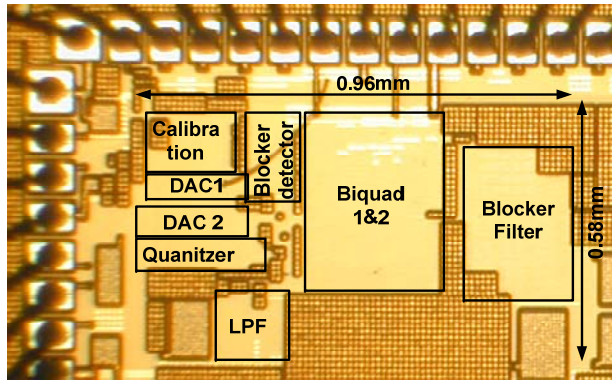
Signal & Noise transfer functions

$$V_{x,n} = \left[\frac{1}{\sqrt{3}R_1 C_1 \omega_{of}} \right] \cdot \sqrt{(V_{n,r1}^2 + V_{n,op}^2)} f_{of} = 0.2 \cdot V_{n,TOT}$$

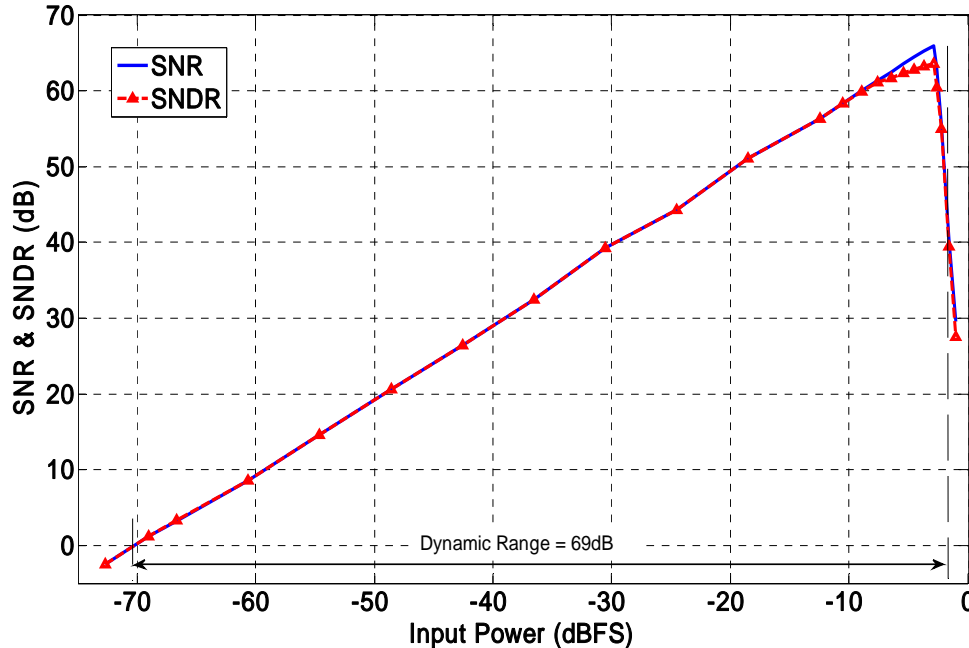
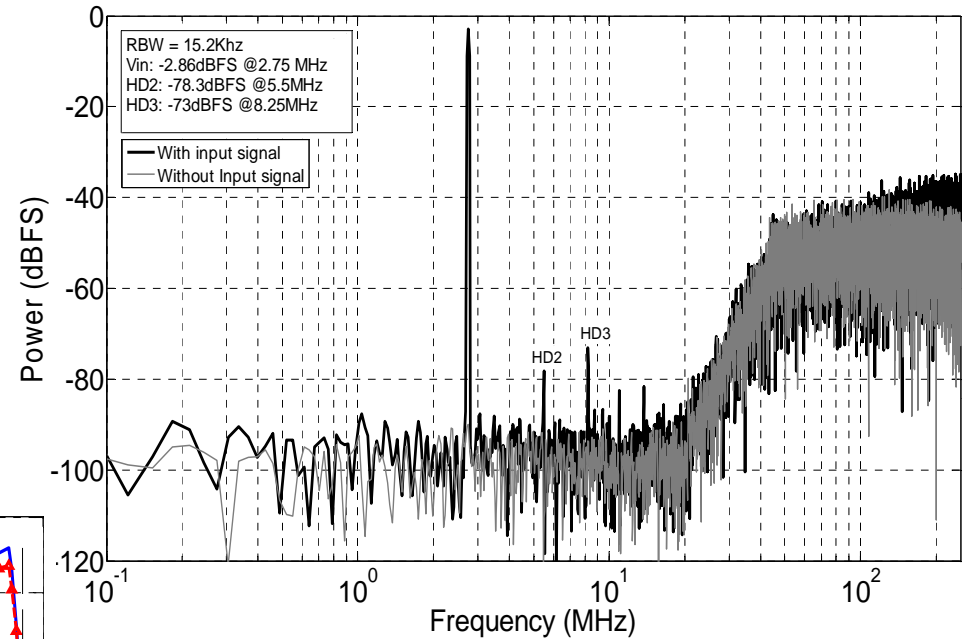
- 10dB attenuation at 60MHz
- In-band noise 15 $\mu\text{V-rms}$ which is well below the ADC noise level



Measurement results



**5th Order CT LP $\Delta\Sigma$ ADC,
Active area < 0.43mm²**



- In 20MHz BW, Input of -2.86dBFS at 2.75 MHz
- Peak SNR= 66dB, Peak SNDR= 64 dB
- HD3= -73 dBFS, HD2= -78.3 dBFS
- DR=69dB

Summary: Blocker Tolerance

- LPF provides blocker rejection especially at the critical frequencies.
- Overload detector and PGA prevents the ADC saturation during transients.
- Blocker reduction techniques
 - Power overhead < 6%
 - Area overhead < 20 %
- **Advantages**
 - Less power
 - Loop parameters are not disturbed so fast settling times
 - Protects the ADC from instantaneous/temporary blockers
 - Moderate SNR is better than no communication or no SNR

Performance Summary of the ADC

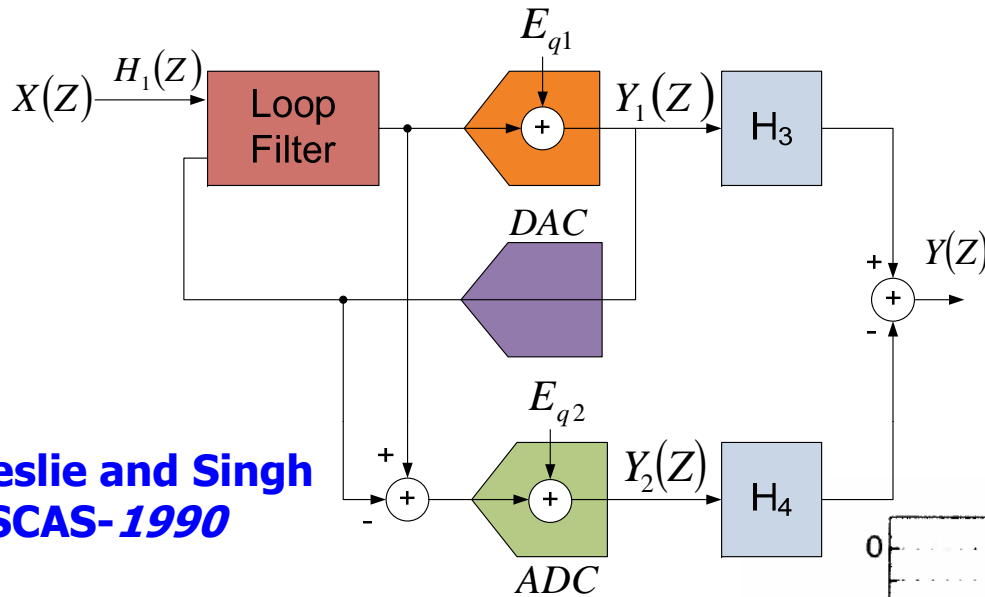
	[9]	[10]	[11]	This work
Fs [Mhz]	250	64	160	500
BW [MHz]	10	1	5	20
SNDR/SNR [dB]	65/68	NA/75.5	69.5	64/66
Dynamic Range [dB]	71	65 [#]	76	69
Blocker reduction [dB] adjacent/alternate channels	8/15	9.5/20 ⁺	10	15/18
Settling time (μ sec)*	51	-	-	< 0.3
Power consumption [mW]	18	4.1	6	17.1
Area(mm ²)	1.35	0.14	0.56	0.43
Technology (nm)	130	180	130	90

fixed input resistor * switching input resistors

* * Blocker adaptation time

+ Extracted from a plot comparing measured and simulated performance, no in-band signal

Fundamentals on MASH architectures



**Analog Intensive
MASH topology**

**Leslie and Singh
ISCAS-1990**

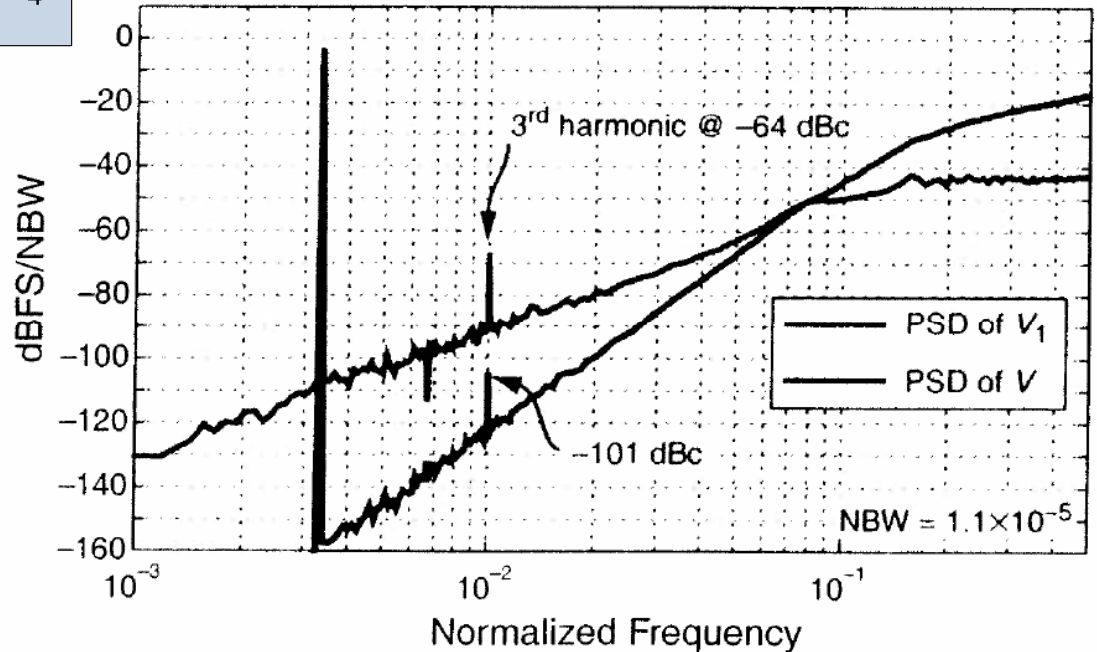
Schreier-Temes

If $H_3 * NTF_1 - H_4 * STF_2 = 0$

Then

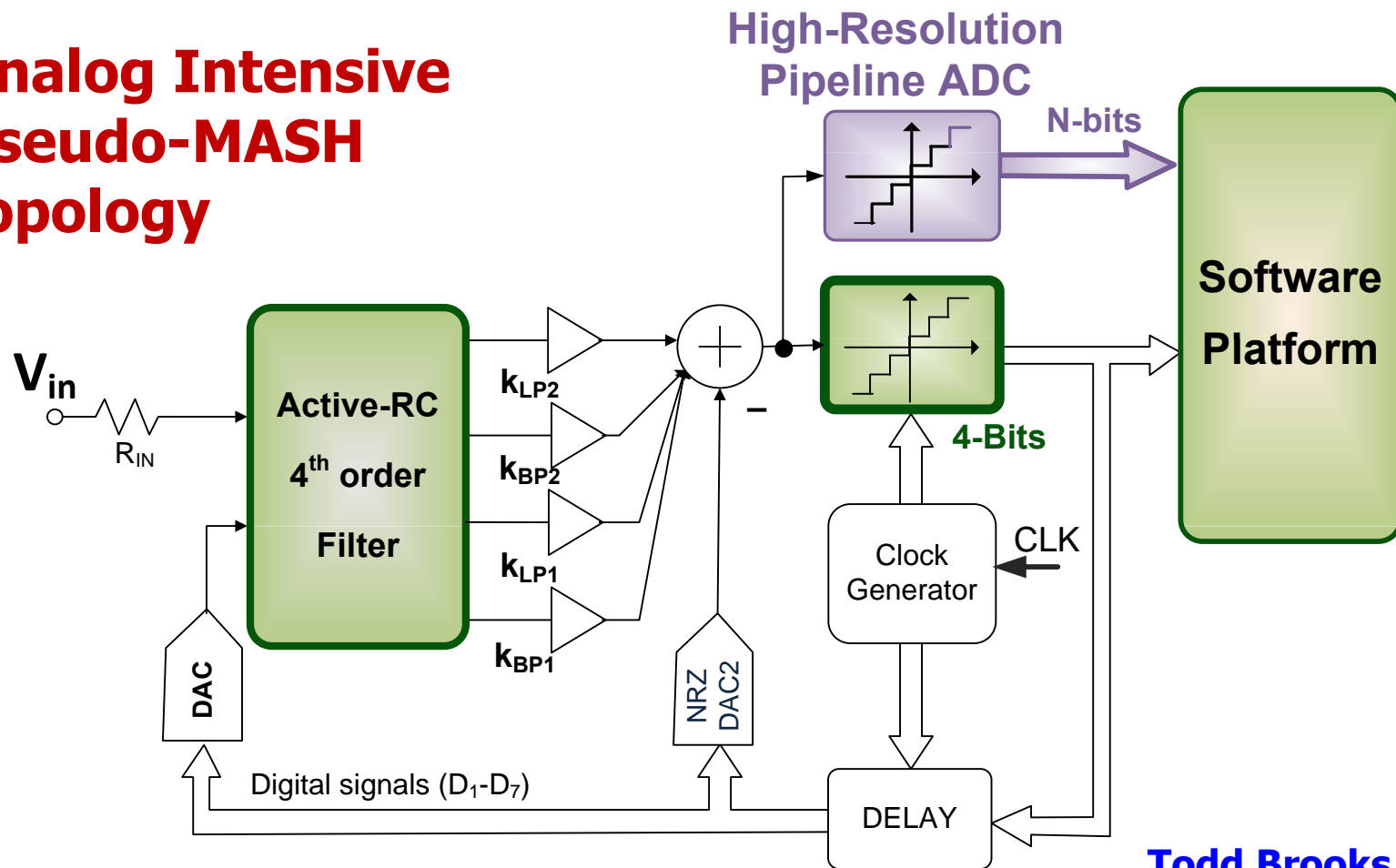
$$Y(z) = \{H_3 * STF_1\}X - \{H_4 * NTF_2\}E_{q2}$$

$$SQNR = \left\{ \frac{E_{q1}}{E_{q2}} \right\}^2 \left\{ \frac{STF_2}{NTF_2} \right\}^2 \left\{ \frac{STF_1 * X}{NTF_1 * E_{q1}} \right\}^2$$



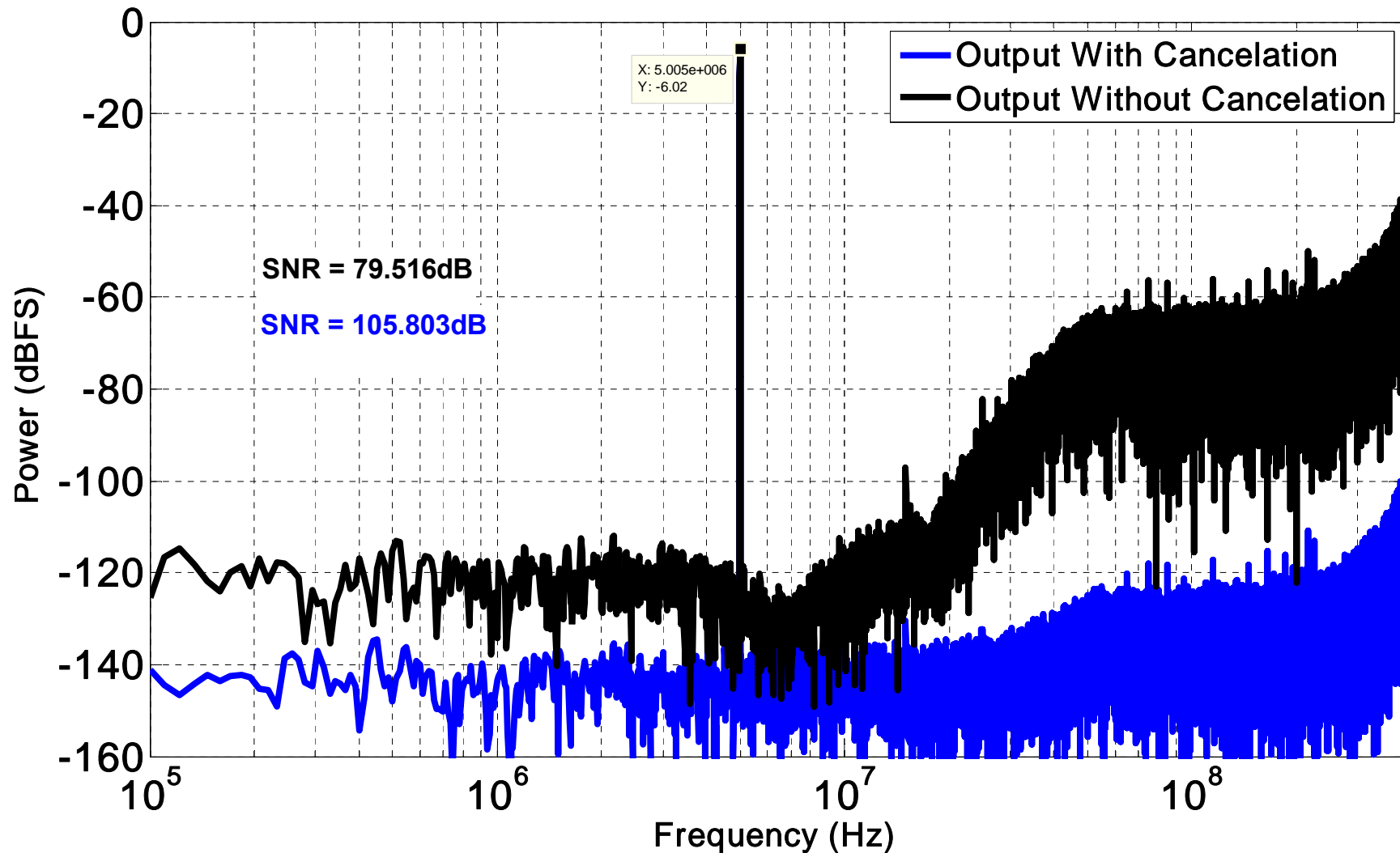
Fundamentals on MASH architectures

Analog Intensive Pseudo-MASH topology



Todd Brooks, et. al.,
JSSC, Dec 1997

Target: SNDR Improvement by 3 bits



- SQNR improvement should be around 18dB (3 bits)
- Power overhead, area overhead < 20%

Conclusions

- **Minimization of filtering functions in the receiver chain demands innovative ADC solutions;**
- **SNDR > 80 dB will be frequently needed in wireless applications;**
- **Jitter and Blocker tolerant architectures are needed;**
- **DAC calibration techniques for fast and high-resolution applications;**
- **Global tuning strategies (for stability)**
- **Advanced LTE applications require high-resolution for signal BW as high as 200MHz**

Recommended Readings

S. Norsworthy, R. Schreier and G. Temes, *Delta-Sigma Data Converters: Theory, Design and Simulation, IEEE Press*

R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters, IEEE Press*

J. Cherry, M. Snelgrove, *Theory, Practice, and Fundamental Performance Limits of High-Speed Data Conversion Using Continuous-Time Delta-Sigma Modulators, Kluwer Academic Press.*

J. M. de la Rosa, *Sigma-Delta Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey, TCAS-I, Jan 2011.*

Other tutorials: IECE-2012