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ISSCC 2013 RF Highlights

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Outline

- 60th anniversary of ISSCC
- Paper Statistics
- RF Techniques
- Frequency Generation Techniques

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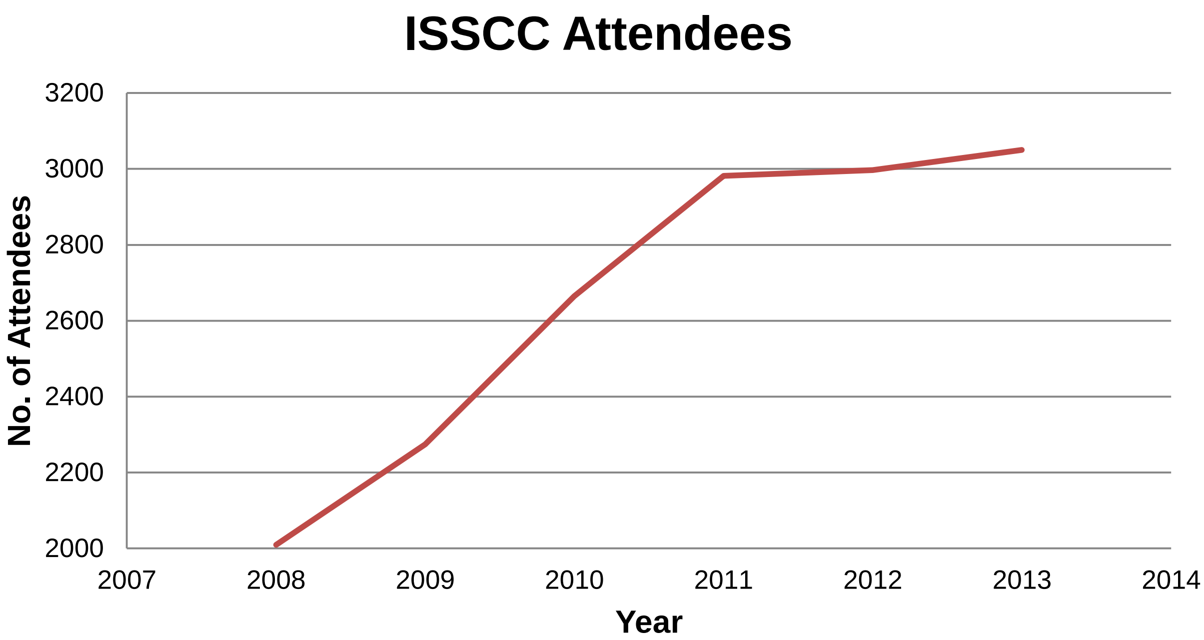
Special Celebrations

- 60th anniversary of ISSCC (1954-2013)
- Lots of nostalgic anecdotes and statistics



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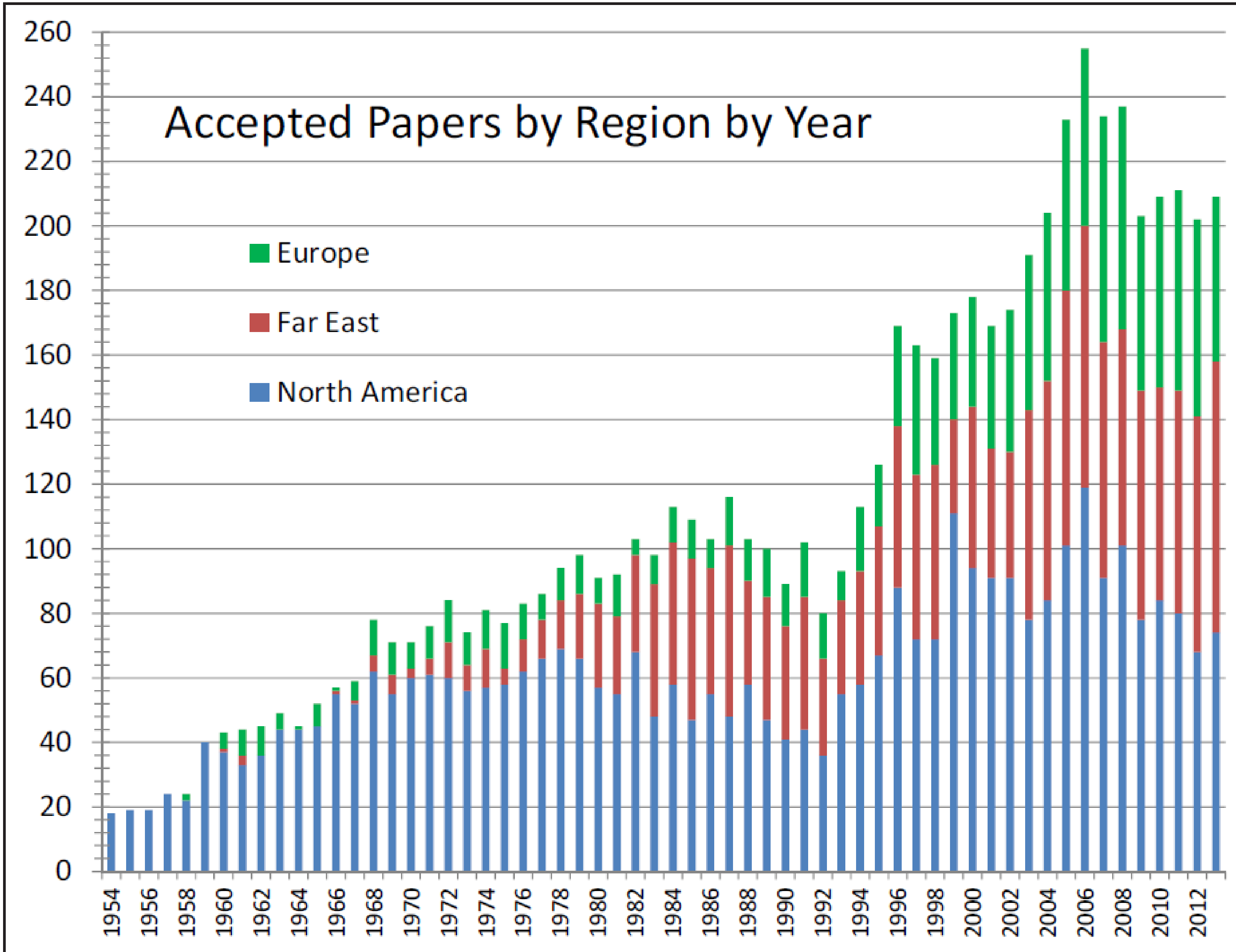
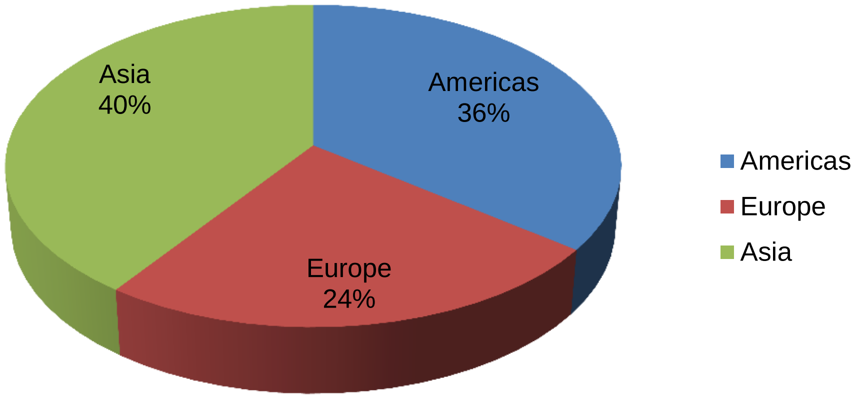
Special Celebrations (cont.)



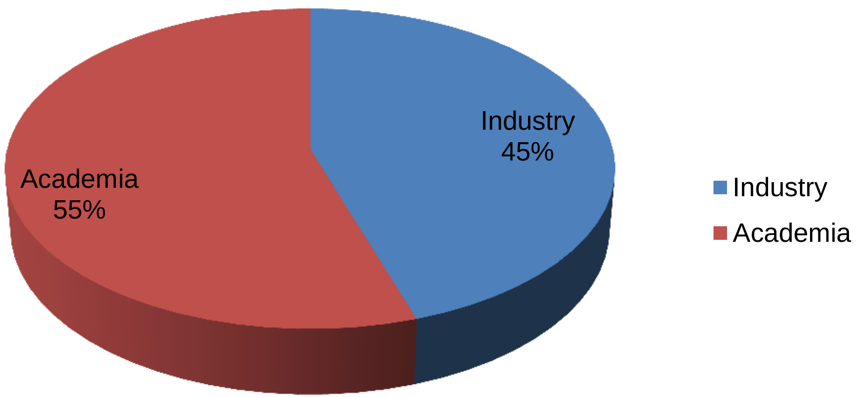
Overall papers statistics

- **209 papers were presented**
  - About the same as last year (206)
  - Organized in 27 sessions



- **Out of the 94 papers from industry, 16 were from the institutes**

- **The papers were uniformly distributed**
  - Geographically
  - Academy vs. industry



- **Number of papers from Asia is increasing appreciably**

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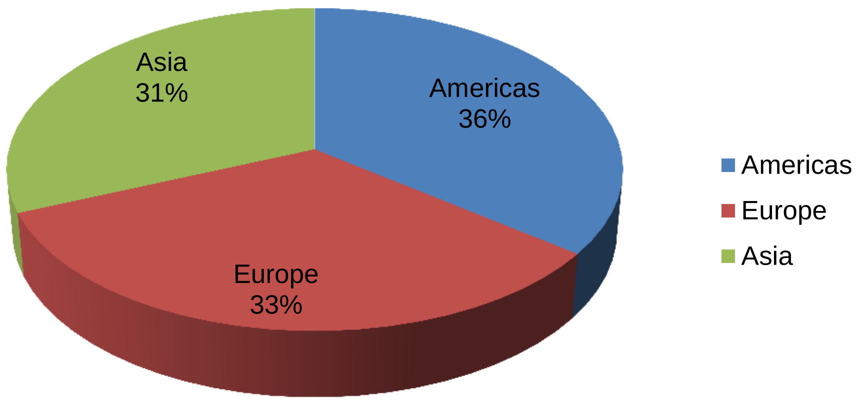
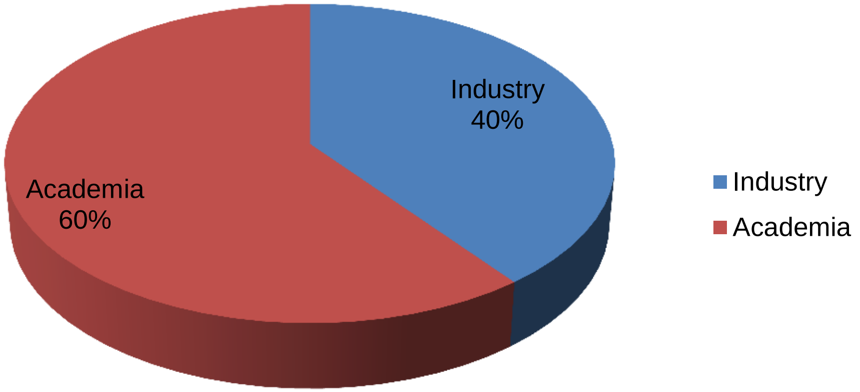
RF paper statistics

- **RF session titles:**
  - RF Techniques
  - mm-wave Techniques
  - High Performance Wireless
  - Wireless Transceivers for Smart Devices
  - Frequency Generation
  - Energy Efficient Wireless



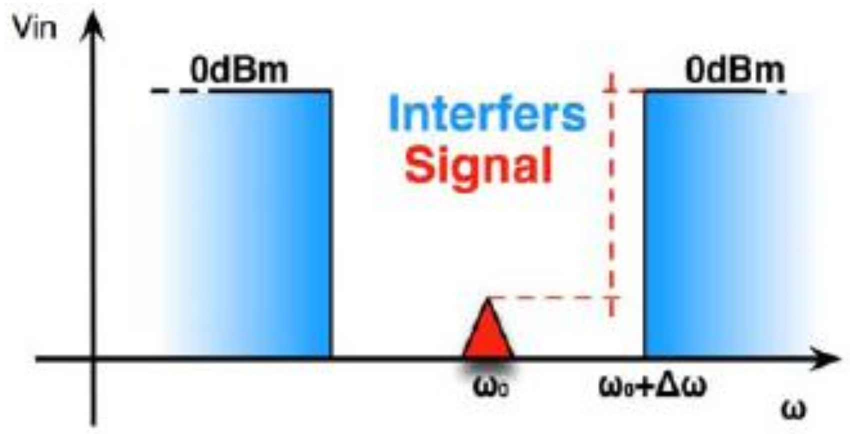
- **US and Academia had a larger share**

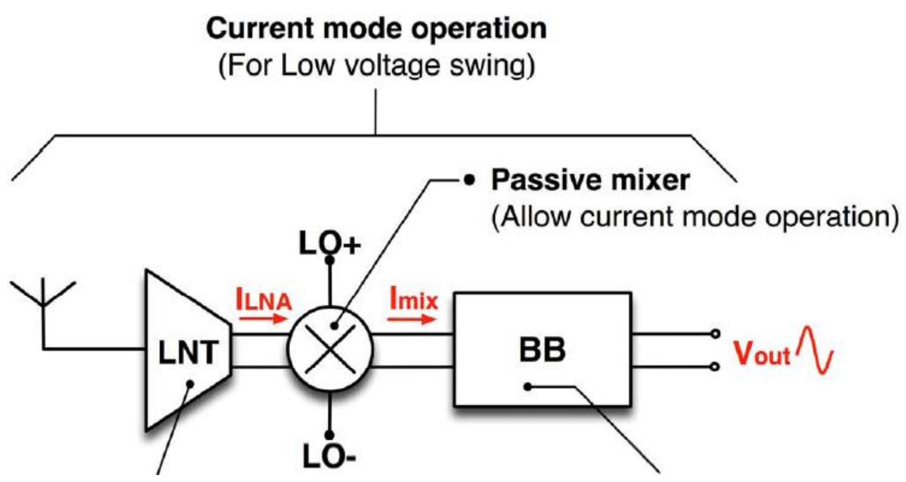
- **RF Forums**
  - Advanced RF Transceiver Design Techniques
  - Mixed Signal/RF Design and Modeling in Next Generation CMOS RF Short courses



5.1: SAW-less Front-End for TDD/FDD

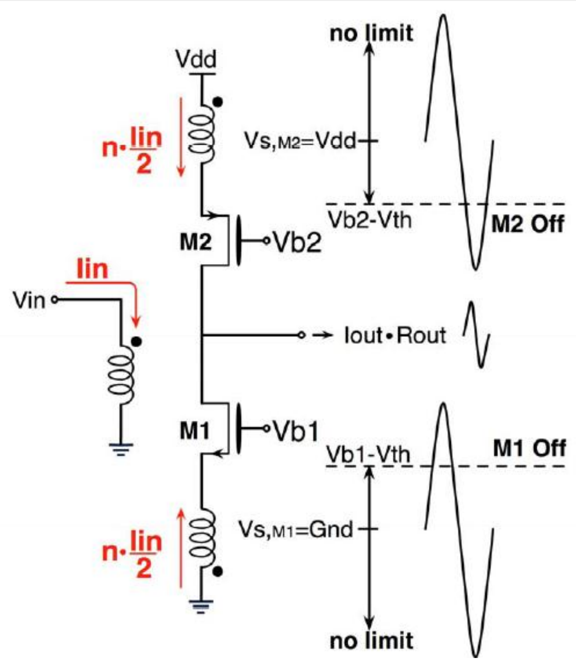
- **Out-of-band interferes**
  - Dynamic Range (De-sentization)
  - LO Harmonics
  - Reciprocal Mixing
- **External SAW filter**
  - Resolves the above issues
  - Single-ended to differential
  - Cost
- **Current-mode signal processing**
  - LNA acts as a V/I converter
  - I/V conversion after BB filtering
    - Blockers removed in current domain

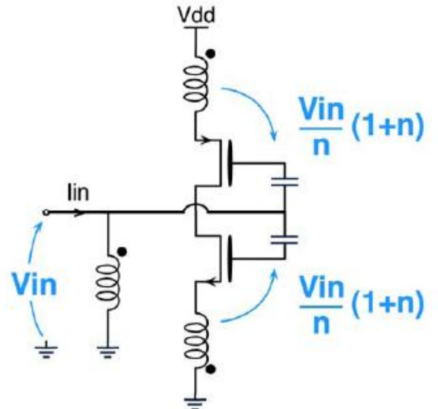




5.1: SAW-less Front-End for TDD/FDD (cont.)

- **The bottle neck is the LNA V/I**
  - Linearity is set by this Gm
- **CG for Wide-band Zin**
  - No current gain
  - NF = 1 + Gamma = 3 (too high)
- **On-chip transformers**
  - Allows SE/Diff conversion
  - Provides maximum headroom
  - Provide current gain and negative Vin
- **Use gate boosting**
  - Apply the signal to the gate
  - Improve NF





$$Z_{in} = \frac{n^2}{2g_m(1+n)} \qquad NF = 1 + \frac{\gamma}{1+n}$$

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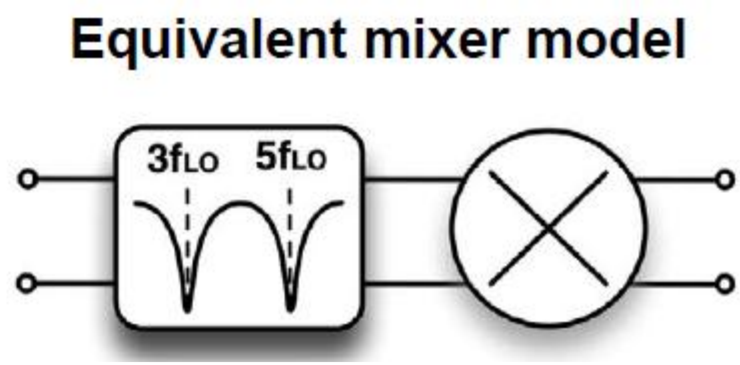
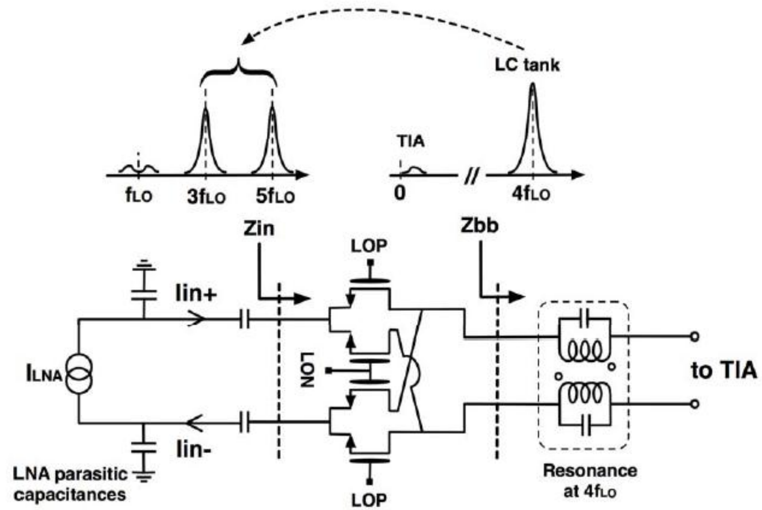
5.1: SAW-less Front-End for TDD/FDD (cont.)

- **LO Harmonics are still an issue**
- **One approach is harmonic-Rejection Mixer**
  - Needs higher VCO frequencies
- **25% duty-cycle mixer is used**
  - The down converted mixer current is passed through an LC network
  - Resonance at $4{*}f_{LO}$
  - Mixing at f_{LO} converts the notches to
    - $3{*}f_{LO}$ and $5{*}f_{LO}$
- **Some debate though**
  - LO harmonic rejection seems to be limited
  - Mixing also with $3{*}f_{LO}$ and $5{*}f_{LO}$
- **40nm CMOS process**





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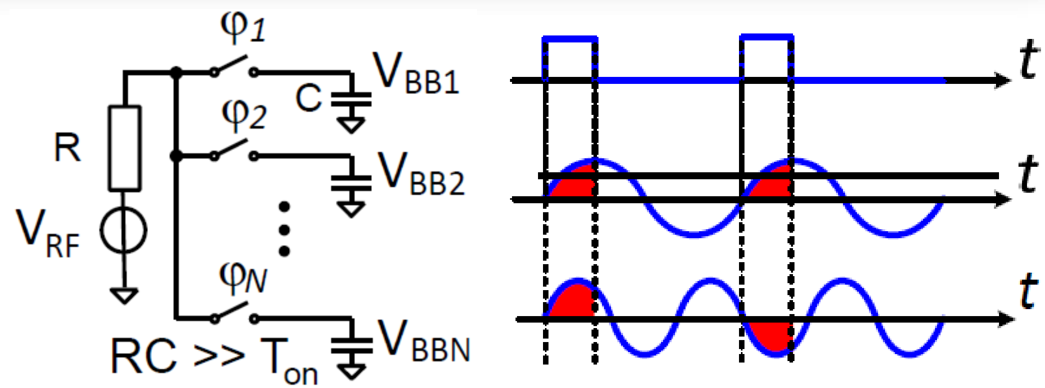
5.2: Spatial and Frequency Filtering

N-path filtering

- High-Q tunable RF filters
- High RF Imp. for $f_{RF} = f_{LO}$
- Low RF Imp. for $f_{RF} \neq f_{LO}$

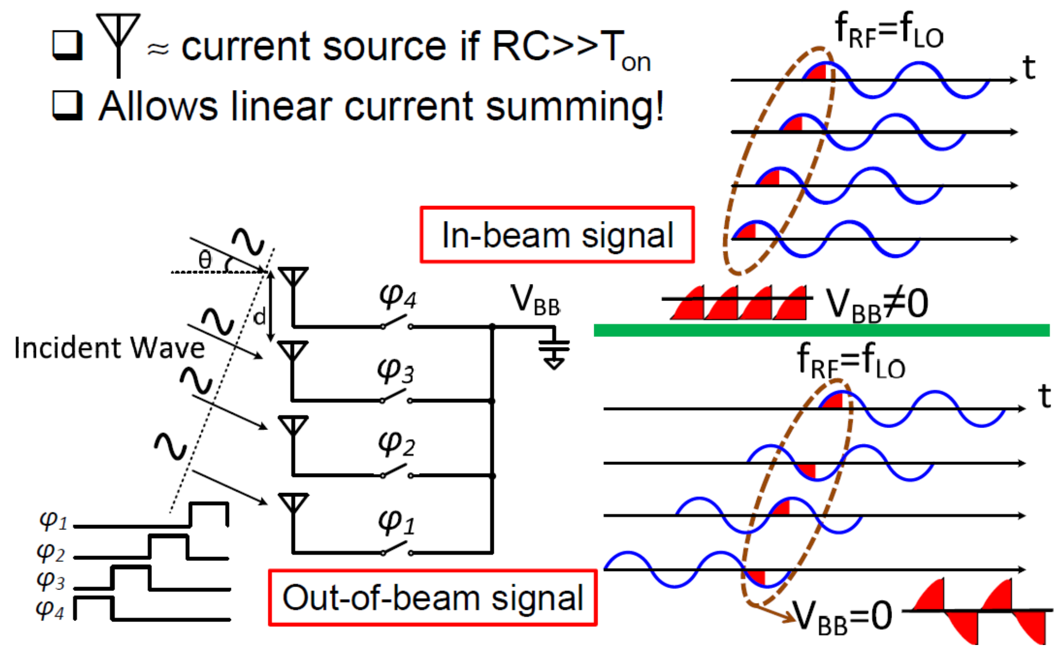


Better Linearity

- No active component at RF

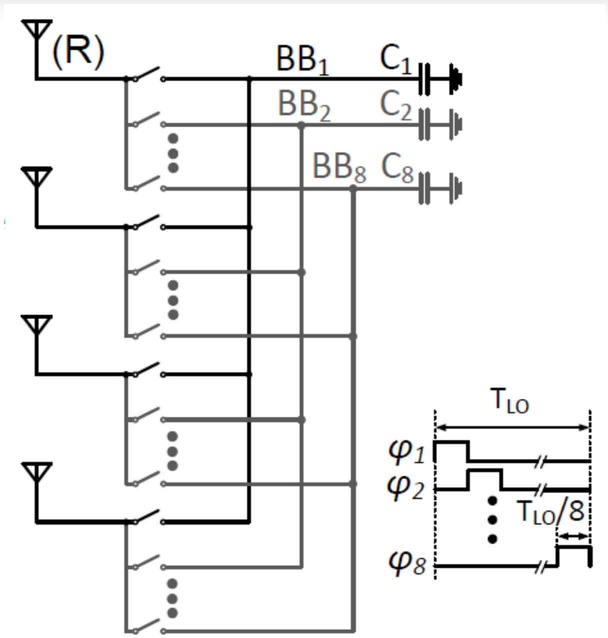
Extend to phase-array

- RC > T_{on}
- Antenna is a current source
- Signals add up in C_{BB}
  - Constructively for in-beam
  - Destructively for out-of-beam
- SNR improvement
  - Signals are correlated, noise is not



5.2: Spatial and Frequency Filtering (cont.)

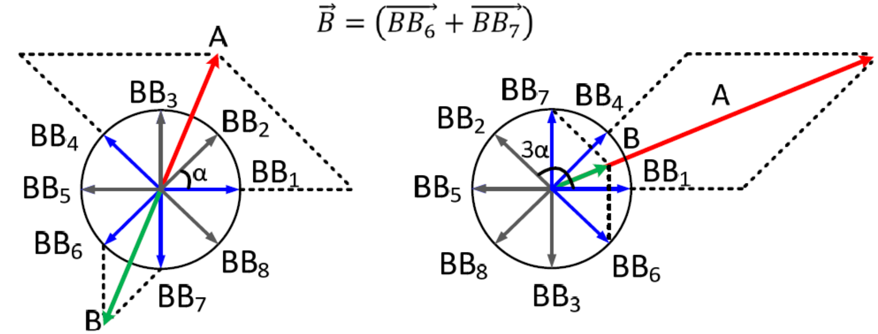
- **Combine the two ideas**
  - Four antennas
  - 8-path filtering for each
  - 8-phase mixer
  - Steer the beam at N*90/8
- **Harmonic rejection is still an issue**
  - N*f_{LO} goes through
- **In this case, 3*f_{LO} is targeted not f_{LO}**
- **Use base-band weights**
  - 3*f_{LO} phase is three times that of f_{LO}
  - Apply BB weights
    - Constructively add for 3*f_{LO}
    - Destructively add for f_{LO}
- **65nm CMOS**



Basis: 3rd harmonic = 3 x phase @ fundamental

$$\vec{A} = (1+\sqrt{2})(\overrightarrow{BB_1} + \overrightarrow{BB_4})$$

$$\vec{B} = (\overrightarrow{BB_6} + \overrightarrow{BB_7})$$

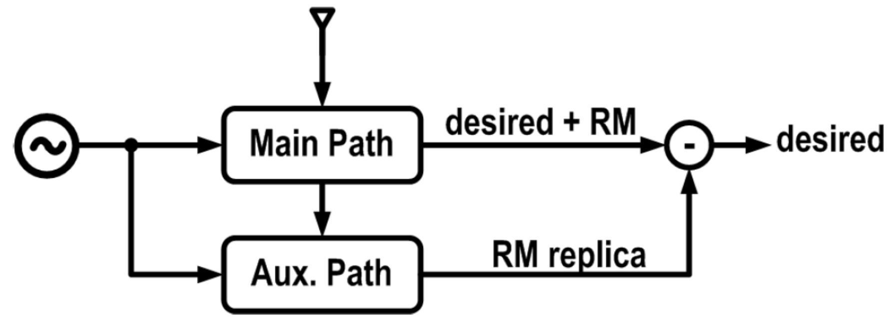


1st Harmonic $\vec{A}+\vec{B}=0$ 3rd Harmonic $\vec{A}+\vec{B}\neq 0$

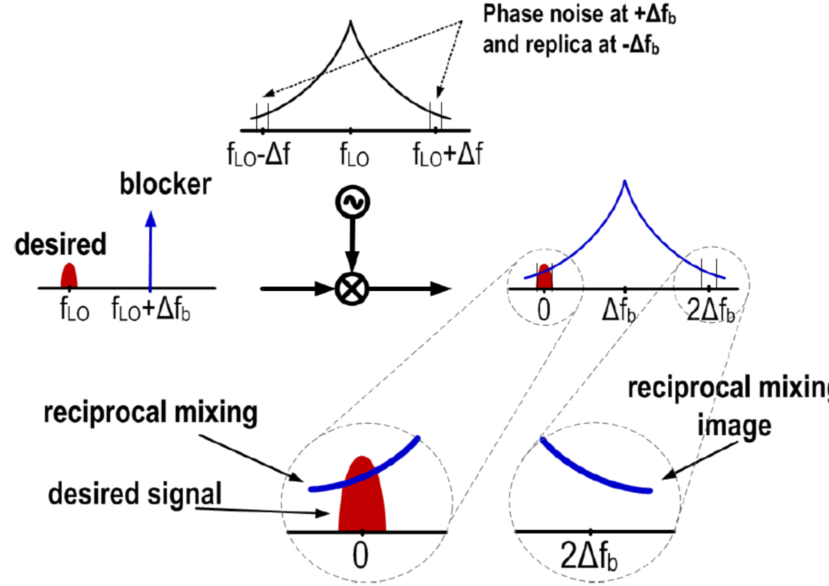
3rd harmonic received & 1st harmonic rejected

5.3: Phase noise cancellation

- **If Phase noise can be cancelled, then**
  - Use R.O. instead of LC Osc.
  - But how?



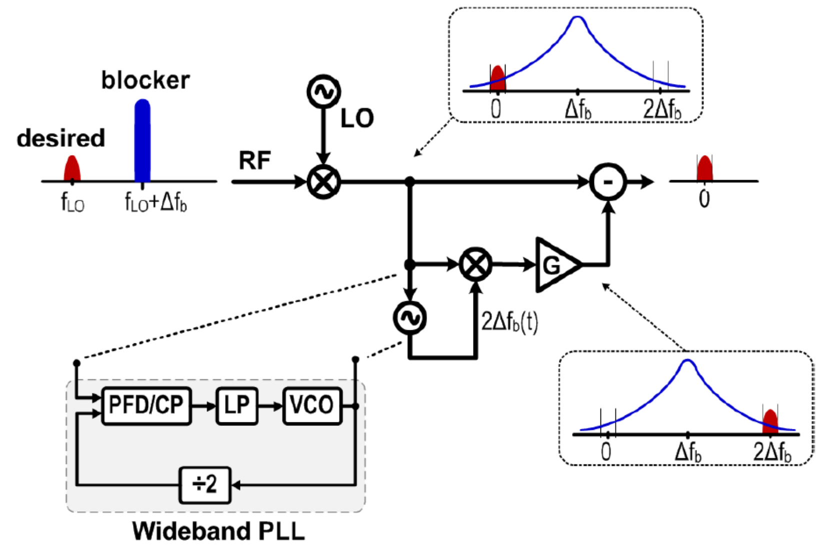
- **Use a replica path**
  - But replica of what?
- **Phase noise is symmetric**
  - A copy of the phase noise exists
  - Extract it and subtract it
  - Let's see how it is done



5.3: Phase noise cancellation (cont.)

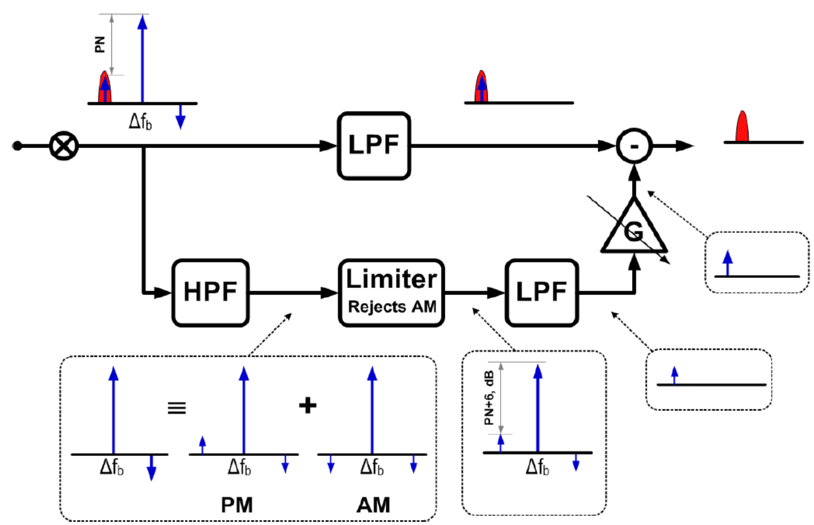
➢ Overall Concept

- Main path: Direct down conversion
- Aux path: Down convert the image
- Not vey practical
  - Needs a second synthesizer
  - Phase noise of 2nd synthesizer



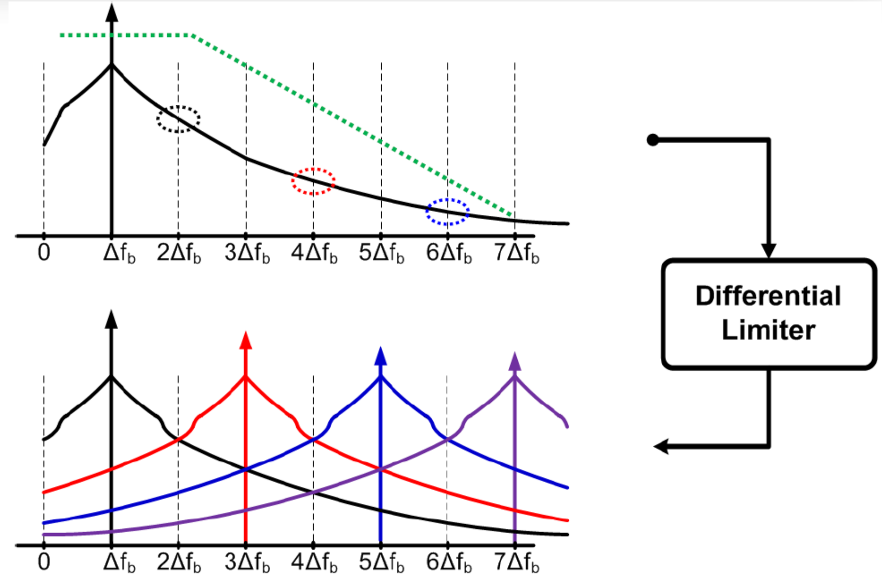
➢ Use a limiter based approach

- Symmetric spurs → AM
- Anti-symmetric spurs → PM
- Limiter only allows PM through
- Adjust gain and delay for proper cancellation

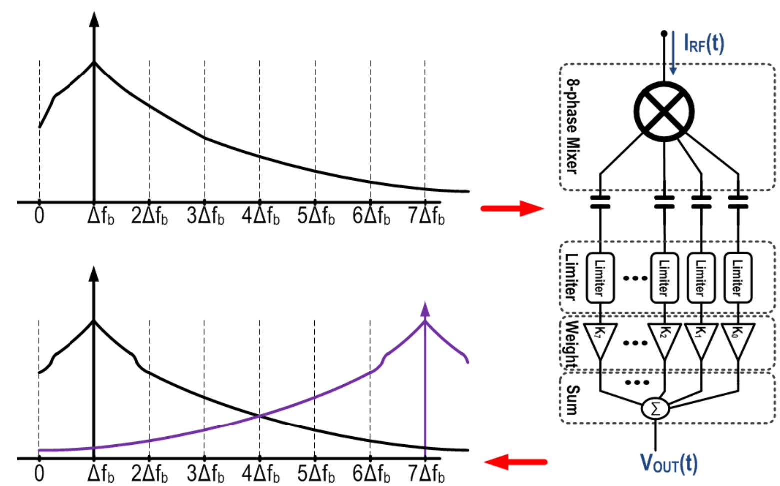


5.3: Phase noise cancellation (cont.)

- **Limiter acts as a PN mixer**
  - Sampling at zero-crossings ($2\Delta f_b$)
  - Folding and images will emerge
  - This will impact the PM subtraction

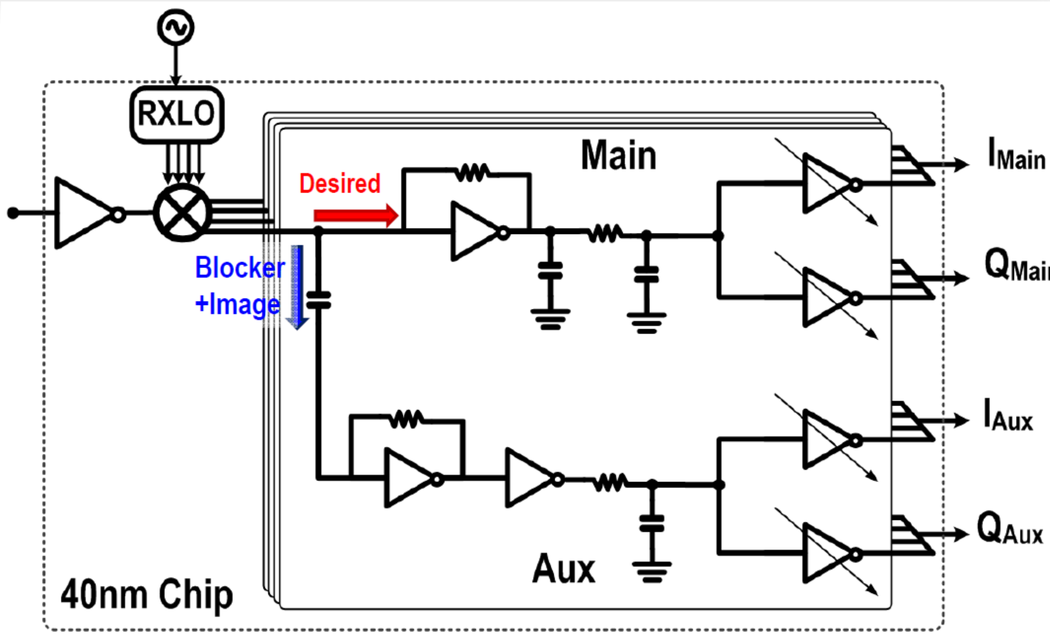


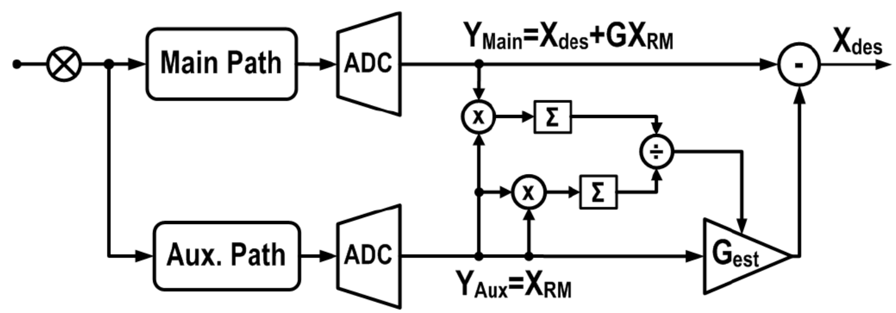
- **Use an N-phase approach**
  - With proper weighting the first N-2 images will be cancelled.
  - The first image is then at N-1 (smaller impact)



5.3: Phase noise cancellation (cont.)

- **Final Design**
  - All circuits are differential
  - Inverters are used for all TIA's
  - Inv. Also act as limiters
  - What about gain calibration?
- **Digitize both paths**
  - Off chip LMS algorithm
  - X_{RM} exists in both paths
    - Causes correlation
    - Provides proper G
  - Rest is uncorrelated
    - Long enough averaging will remove this extra signal
- **Blocker detector**
  - If no blocker, turn off Aux path
- **40nm CMOS**





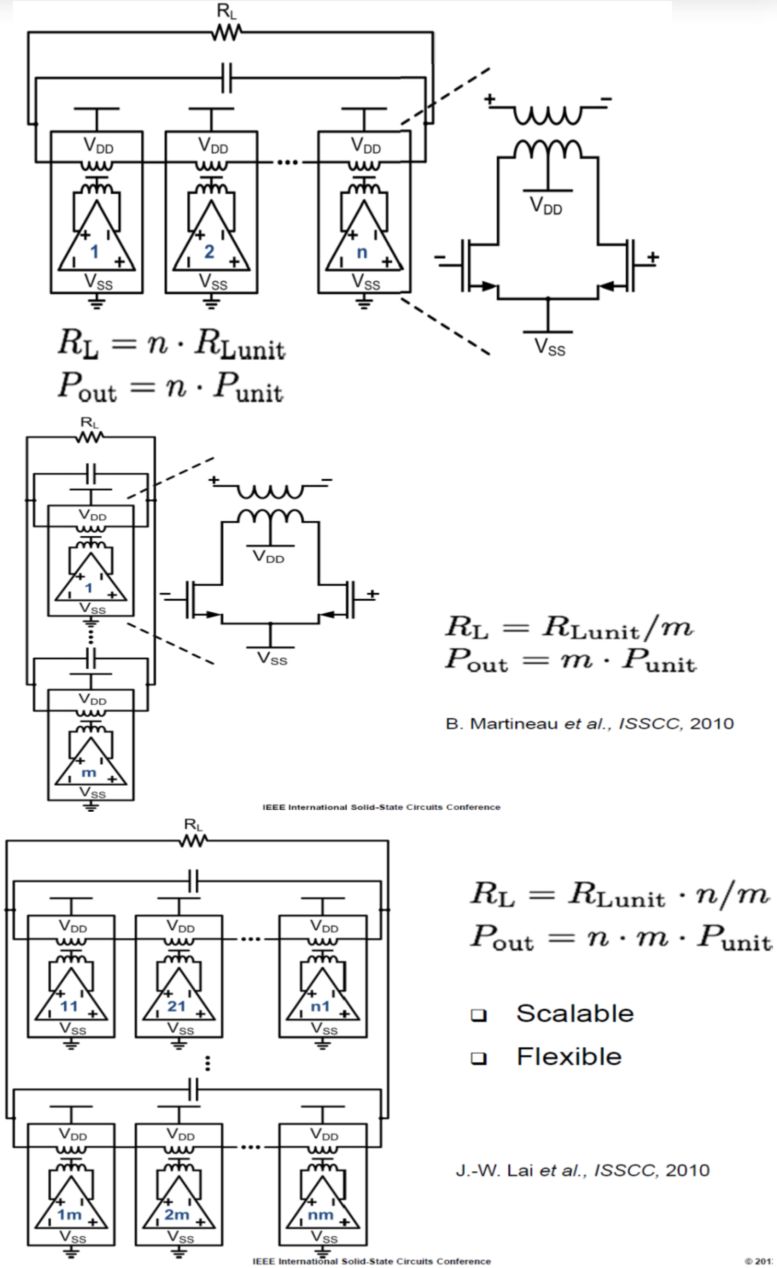
$$G_{est}=\frac{\sum_n Y_{Main}[n]*Y_{Aux}[n]}{\sum_n Y_{Aux}[n]*Y_{Aux}[n]}=G+\frac{\sum_n X_{des}[n]*X_{RM}[n]}{\sum_n X_{RM}^2[n]} \rightarrow 0$$

Because X_{RM} and X_{des} are statistically independent

5.4: Stacked Array PA

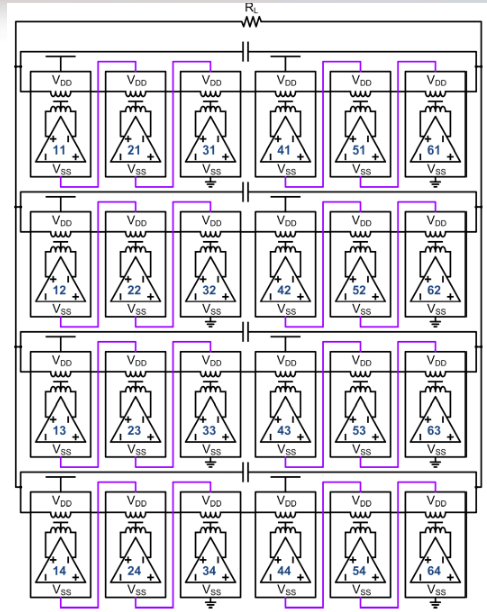
- **Array PA's**
  - Serial
    - Too high an output impedance
  - Parallel
    - Too low an output impedance
  - Both inefficient due to large impedance ratios
    - High Q → High IL (for a given Q_{comp})

- **Use arrays of S/P instead**
  - Can provide better matching
    - Lower impedance ratio
    - Better efficiency

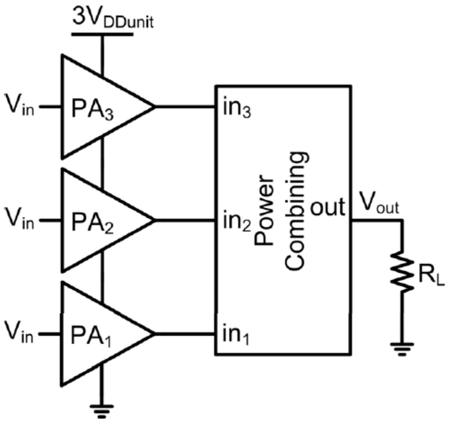


5.4: Stacked Array PA (cont.)

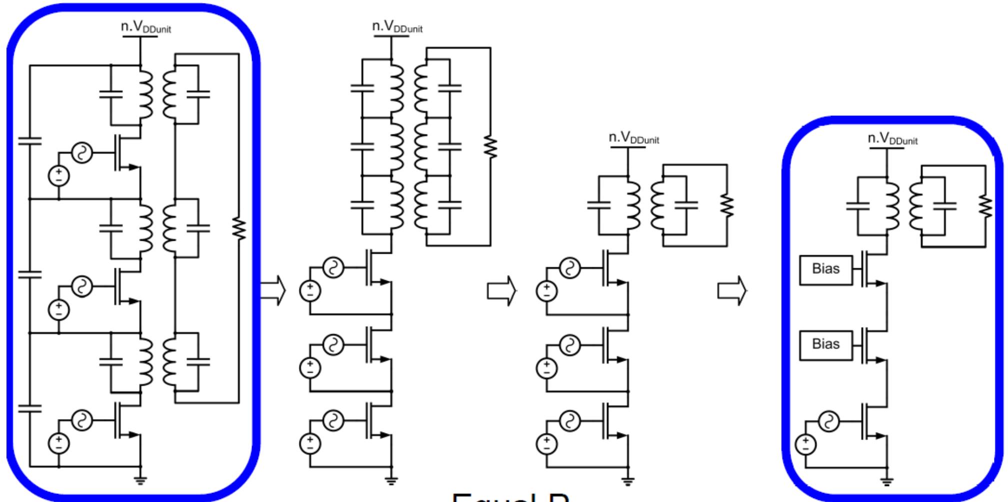
- **Large swing is an issue**
  - Hot Carrier Injection
  - Oxide dielectric breakdown
- **Use stacking**
  - Distribute the swing and supply across several series devices
  - Too many transformers
  - Hard to route
- **Merge transformers into one**
  - Simplify the design
  - Enhance the power routings
  - Use HV for the top most device
    - Needs to handle large Vdb
  - Parasitic S/D caps affect efficiency



- n = 6, m = 4
- Stacking 3 stages*



* A. Ezzeddine *et al.*, *MTT-S*, June 1985



Equal P_{out}
Equal V

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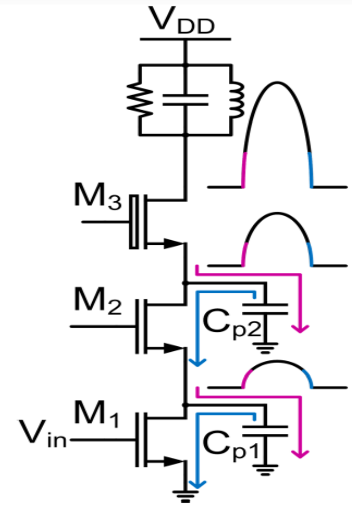
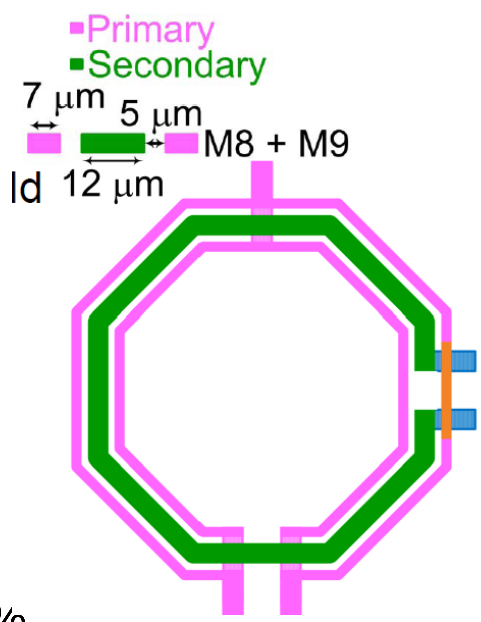
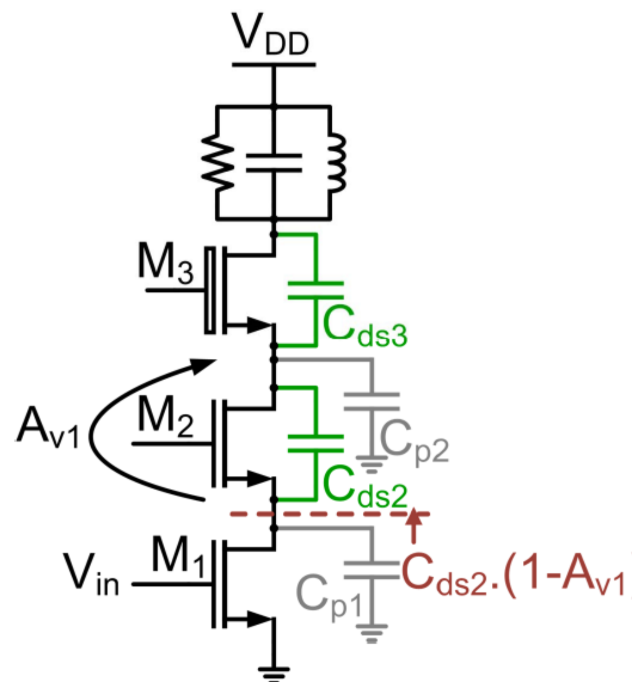
5.4: Stacked Array PA (cont.)

- **C_p along with R_{on} (when in triode) causes loss**
  - During charge and discharge
- **Often inductors are used to tune**
  - Cost
  - Narrow band
- **Use negative capacitors**
  - Wide-band
  - But how?
  - Use Miller effect
- **Transformers design**
  - Low lateral and secondary caps
- **65nm CMOS**
  - Pout = 28dBm, PAE = 20.6%



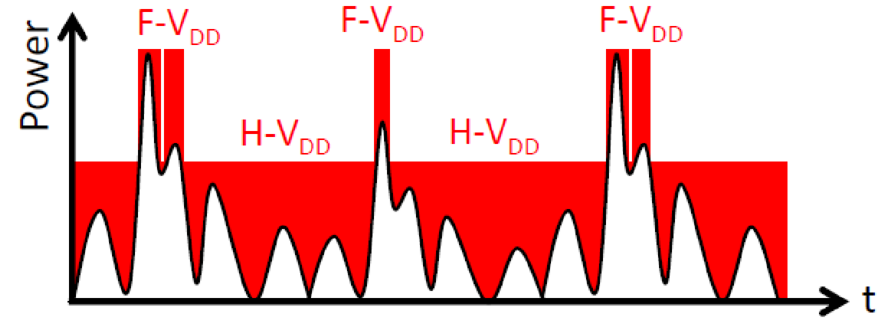


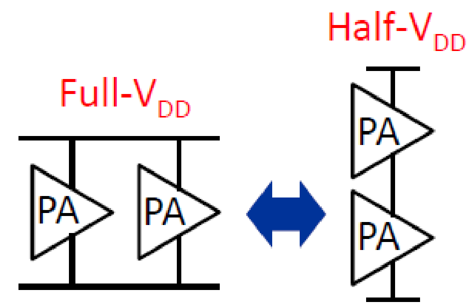


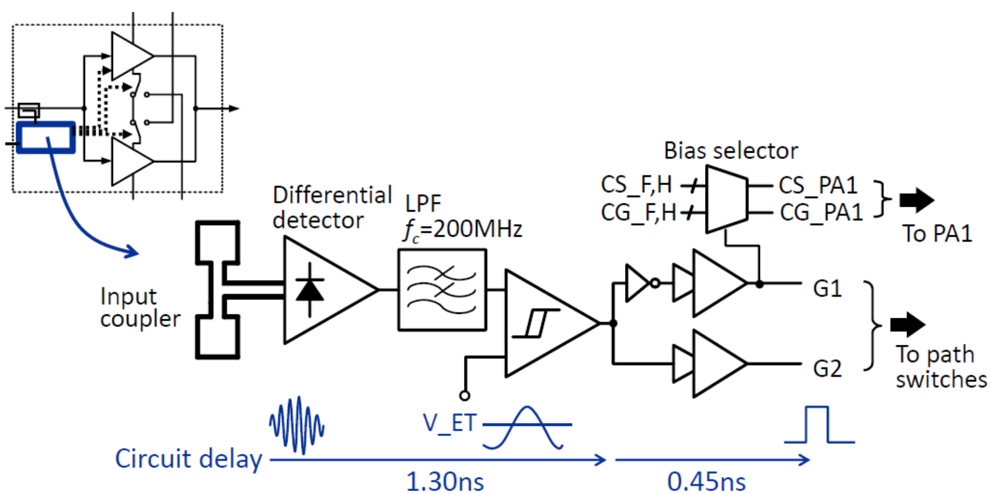
5.5: Supply switching PA

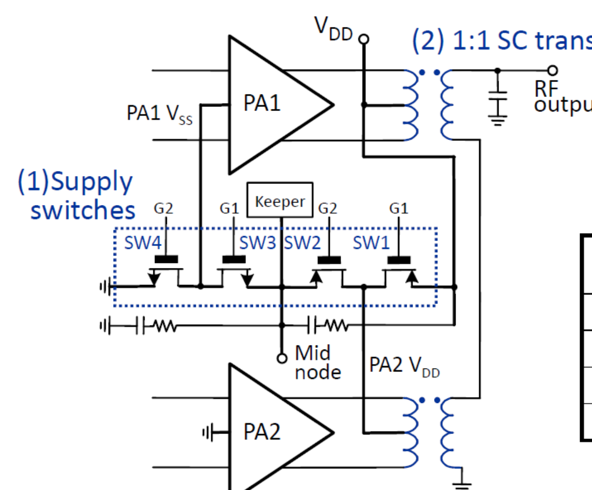
- **Efficiency degrades when PA B.O.**
- **What is supply drops when signal drops?**
  - Needs DC/DC converters
  - Use stacked PA for Vdd/2 case
    - Mid point needs to be around Vdd/2
    - Use a keeper
- **<2ns threshold detector (EVM Impact)**
  - Some switching noise issues

- Dynamic Operation (Envelope Tracking)





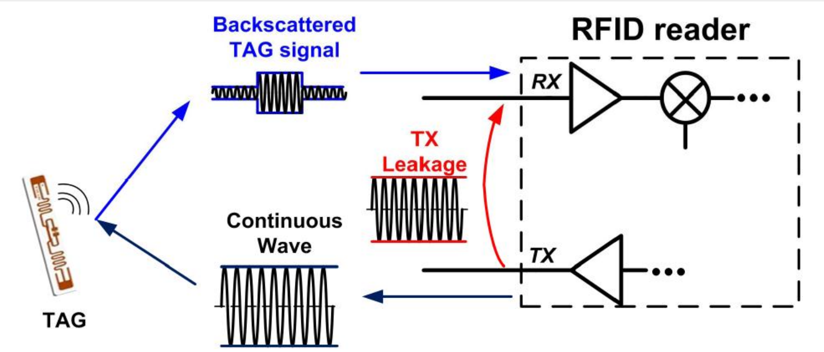


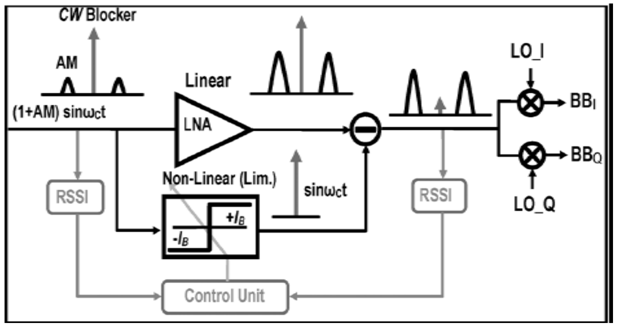


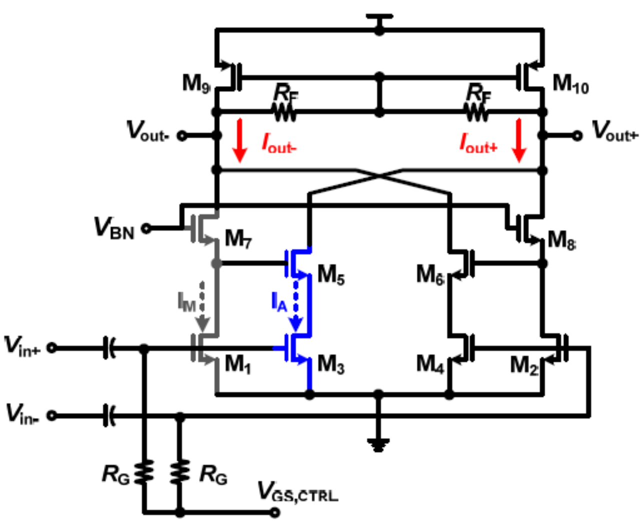
Switch	Channel width (mm)
SW1	7.5
SW2	25.5
SW3	7.5
SW4	5.0

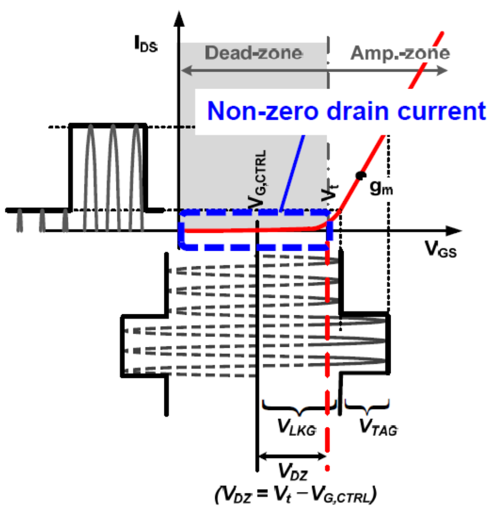
5.6: TX leakage suppression

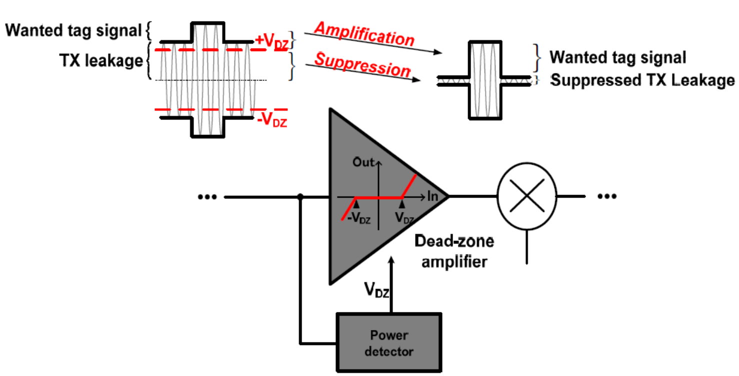
- **RFID system**
  - Back scatter and AM modulate an incoming CW
  - RX signal contaminated by the TX CW
- **Current techniques**
  - Active blocker injection
  - VCO cancellation
- **Proposed solution**
  - Non-linear amplification with a dead zone











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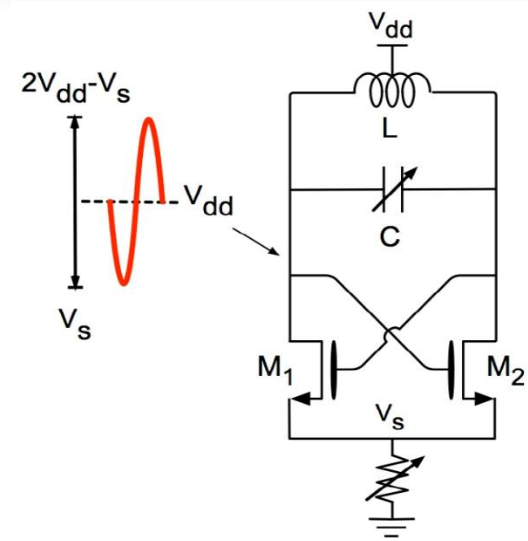
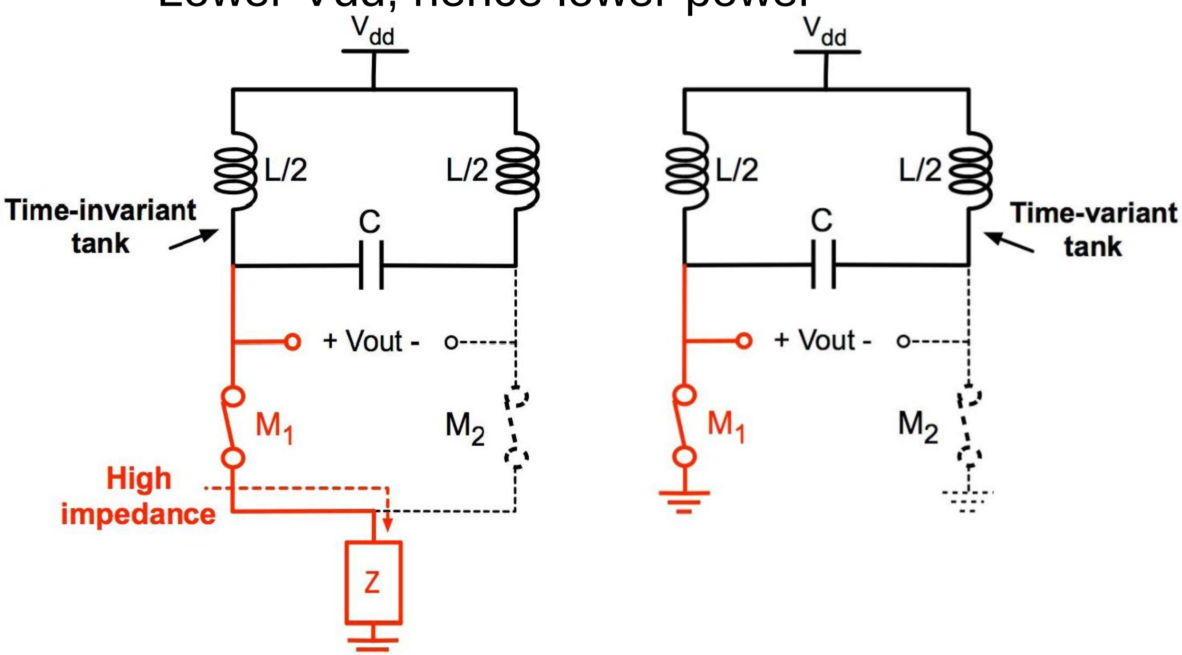
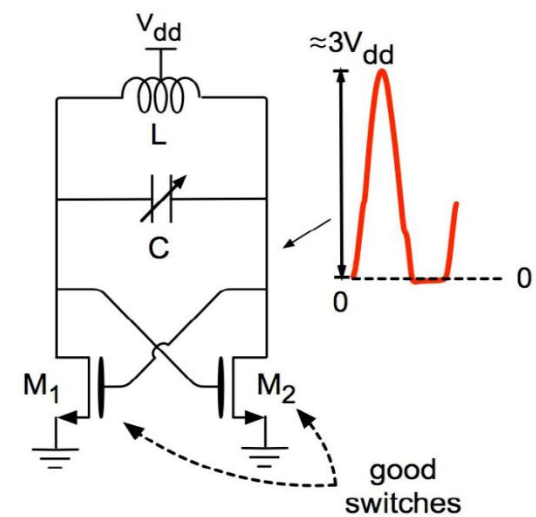
20.1: Class-D VCO

- **Class-B VCO**
  - Large swing (+-Vdd)
  - Need Tail current source (or resistor)
    - Due to R_{on} losses
- **What if we have very low R_{on}?**
  - Go for even higher swings
  - Loss in R_{on} is negligible (good switch)
  - Lower Vdd, hence lower power

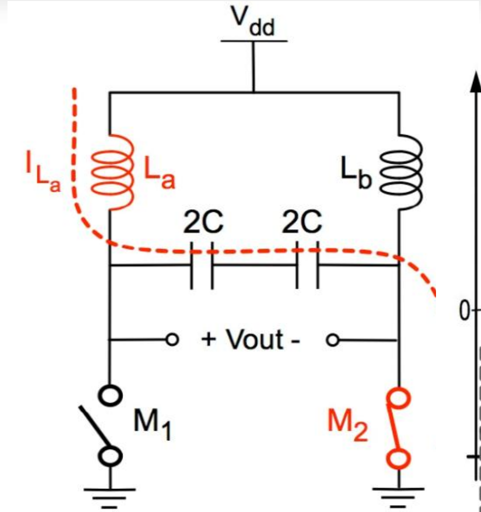


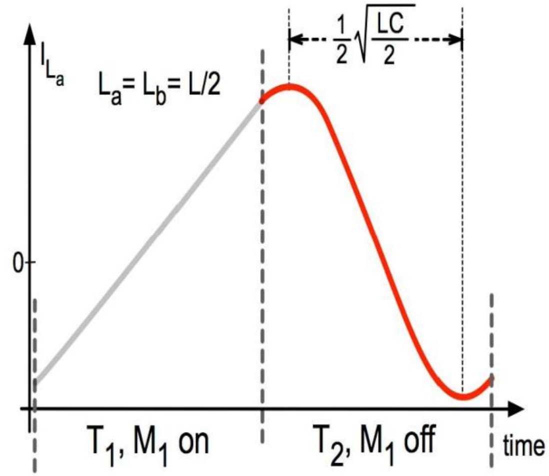


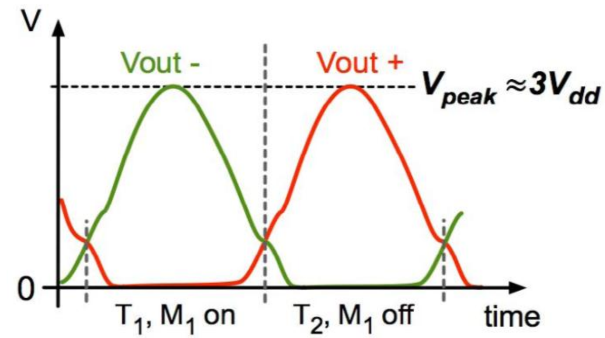


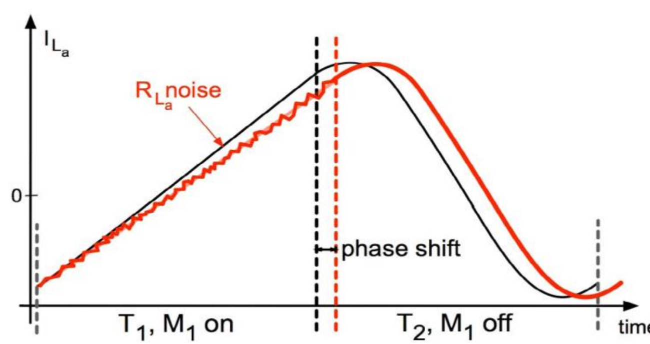
20.1: Class-D VCO (cont.)

- **Operation**
  - T1: The I_{La} charges up
  - T2: La resonates with C
- **Circuit equations**
  - Continuous I_{La} and its derivative
  - T1 = T2 (due to symmetry)
  - $V_{peak} = V_{dd}\left(1 + \sqrt{\frac{\pi^2\alpha^2}{4} + 1}\right) \approx 3.27V_{dd}$
  - $\omega_D = \frac{1}{\sqrt{LC}}\frac{\sqrt{2}}{\alpha} \quad \alpha = \frac{1}{2} + \sqrt{\frac{1}{4} + \frac{4}{\pi^2}} \approx 1.3$
- **Note that the tank is time variant**
  - Makes phase noise calculation even more difficult
- **Very large (1.35mm) switches were used**
  - Poor $1/f^3$ and supply pushing



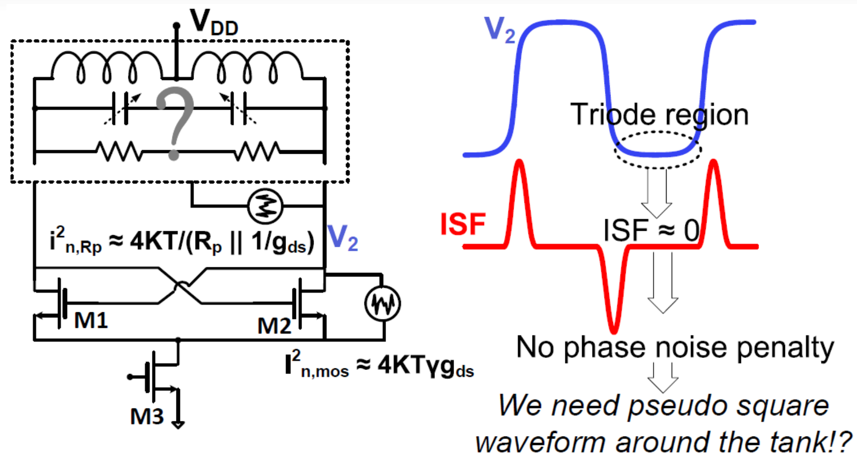


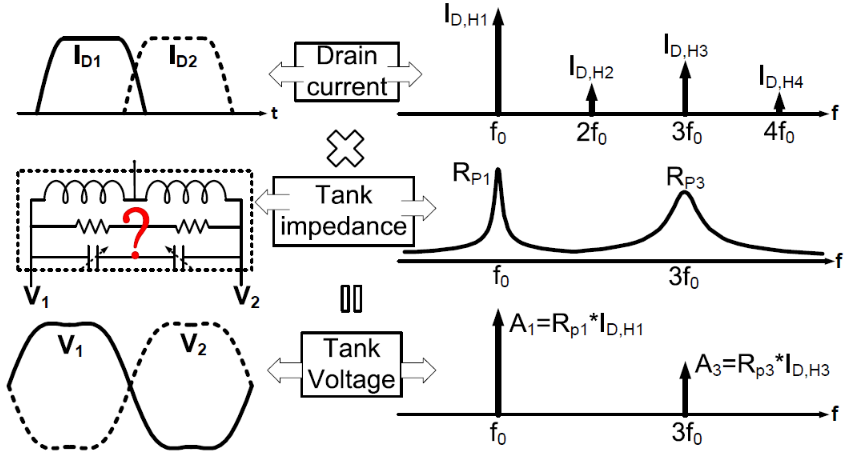




20.2: Class F VCO

- **Motivation: Reduce power**
  - Larger tail current help PN
  - Until the devices go in triode
- **Basic idea: Improve ISF**
  - Noise injection when V is flat
    - Not during zero crossing
  - But how?
- **Make the tank to have high impedance at f_o and $3f_o$**
- **Make $Z(3f_0) = \frac{Z(f_0)}{X}$**
  - A more advanced tank is required

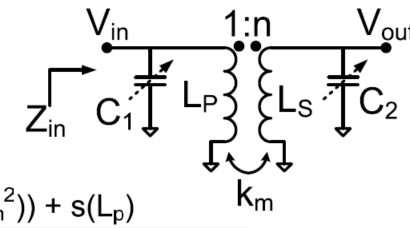




20.2: Class F VCO (cont.)

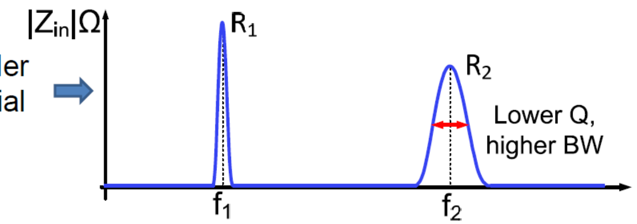
- A transformer-based tank will provide two pair of complex poles
- By setting the proper coupling factor, the intended impedance can be achieved
- Oscillation at higher frequency
  - Lower loop gain
  - Injection locking to $3f_1$
- Very large gate voltages
  - Use thick-oxide devices

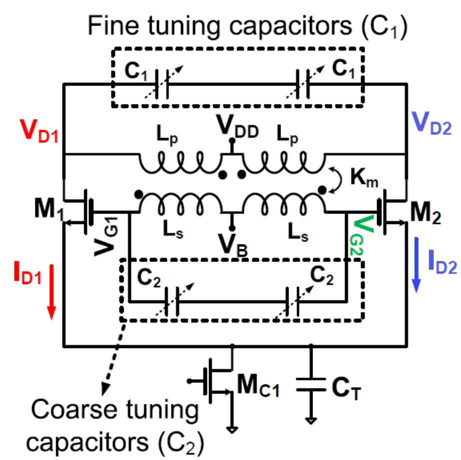
• Transformer based tank has two resonance frequency for imperfect coupling factor.

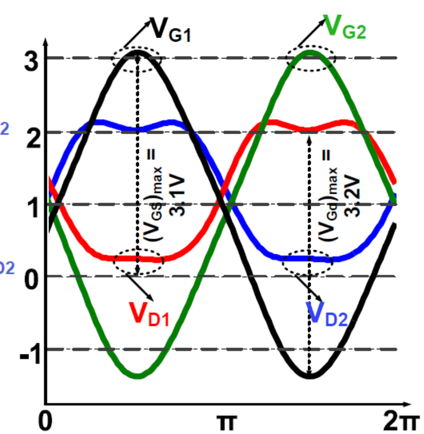


$$Z_{in} = \frac{s^3(L_pL_sC_2\,(1-K_m^2)) + s(L_p)}{s^4(L_pL_sC_1C_2\,(1-K_m^2)) + s^2(L_sC_2+L_pC_1)+1}$$

Forth-order polynomial







• M1 & M2 thick oxide devices → More than 10 years operation www.silabs.com

www.silabs.com/redirect