Continuous-time $\Delta\Sigma$ Modulators with Improved Linearity and Reduced Clock Jitter Sensitivity using the SCRZ DAC

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- Work of my M.S students
  - Timir Nandi, now at TI, India
  - Karthikeya Boominathan
- Part of this presented at
  - CICC 2012

Outline

- Introduction
- Limitations of conventional DAC pulses
- Switched-C Return-to-Zero Principle
- Modulator Architecture
- Circuit Design
- Measurement Results
- Conclusion

Motivation

- Continuous-time DSMs
  - Resistive input impedance
  - Relaxed opamp gain requirements
- Most high performance CTDSMs
  - Multibit loops
- Focus of this research
  - Can we do better with single-bit loops ?
- Case study
  - 14 bit ENOB, 2 MHz Bandwidth, 0.18μm CMOS

Multibit versus Single-bit Modulators

Design Targets

Dynamic Range	86dB (14 ENOB)	
Bandwidth	2 MHz	
Order	4	
Quantizer	1 bit	4 bit
Out of Band Gain		
OSR Needed		
Sampling Rate		

Design Targets

Dynamic Range	86dB (14 ENOB)	
Bandwidth	2 MHz	
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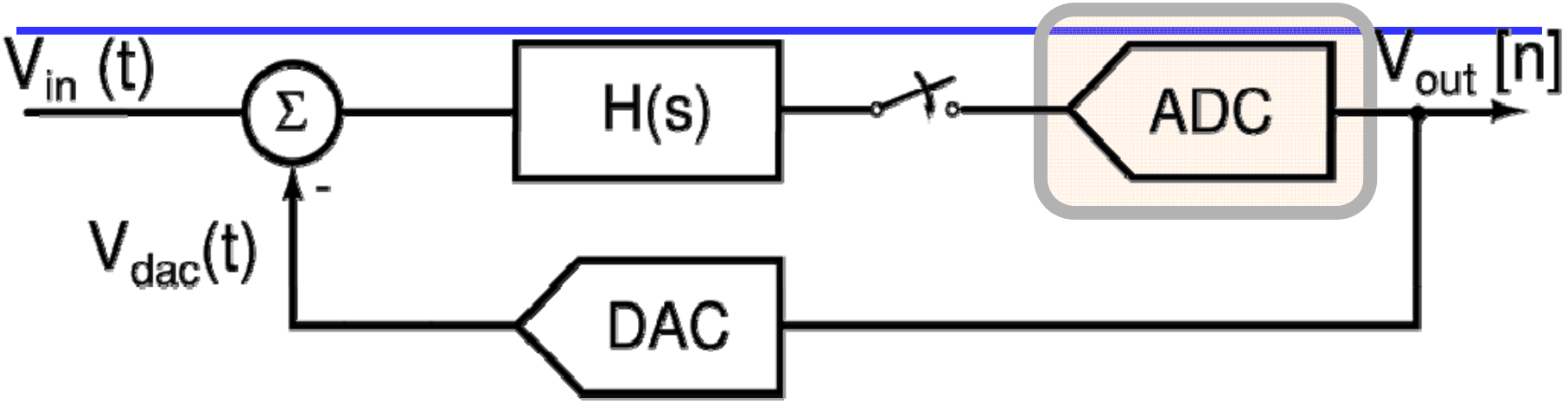
Quantizer	1 bit	4 bit
Out of Band Gain	1.5	
OSR Needed	64	
Sampling Rate	256 MHz	

Design Targets

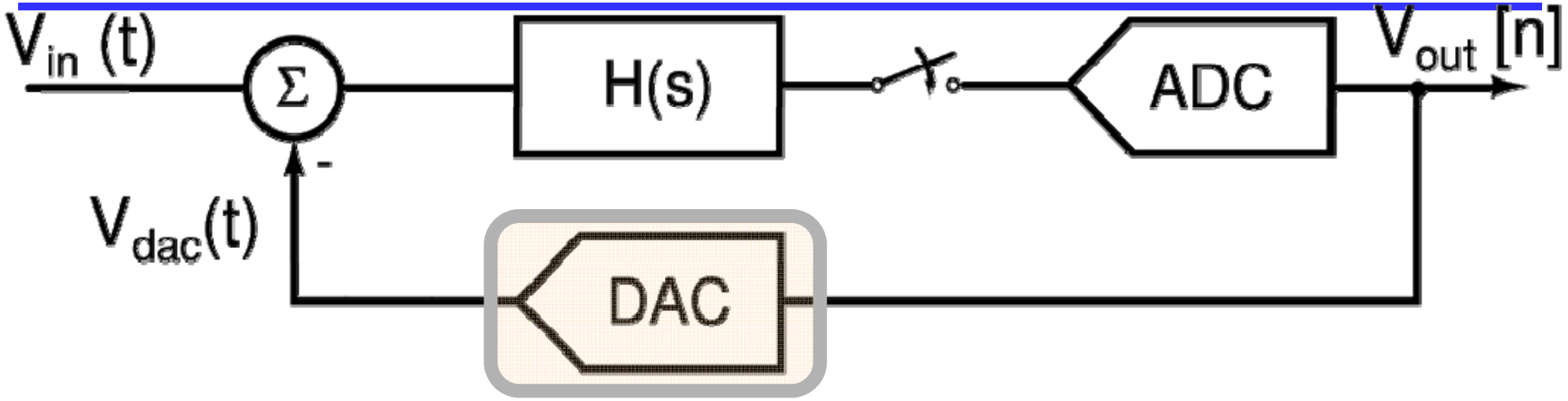
Dynamic Range	86dB (14 ENOB)	
Bandwidth	2 MHz	
Order	4	
Quantizer	1 bit	4 bit
Out of Band Gain	1.5	2.5
OSR Needed	64	20
Sampling Rate	256 MHz	80 MHz

ADC : 1 bit versus 4 bit



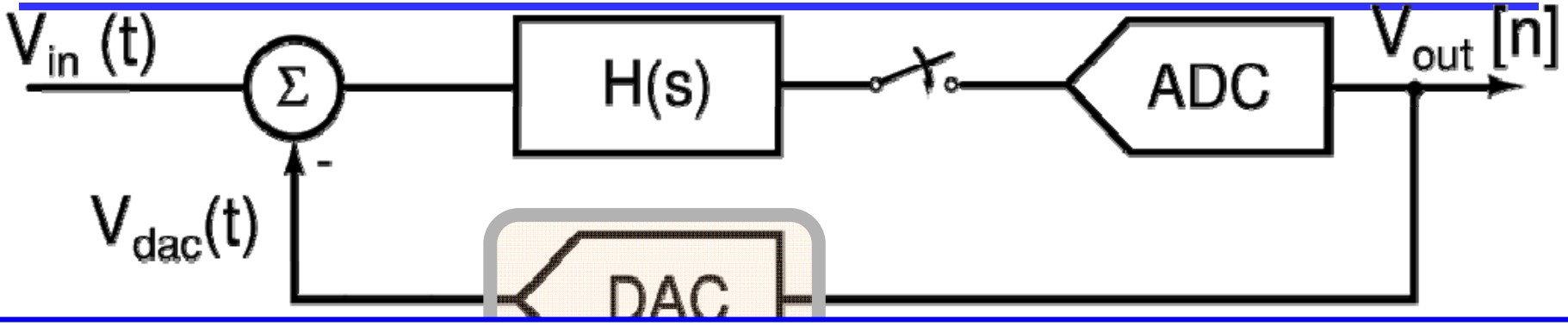
- 4 bit ADC
  - 15x more comparators @ 1/3rd speed
  - 5x more ADC power, 15x more area
  - 15x loop filter & clock path loading

DAC : 1 bit versus 4 bit



- 4 bit DAC
  - Needs Dynamic Element Matching
  - DEM adds excess delay & power
  - Not very effective @ low OSR

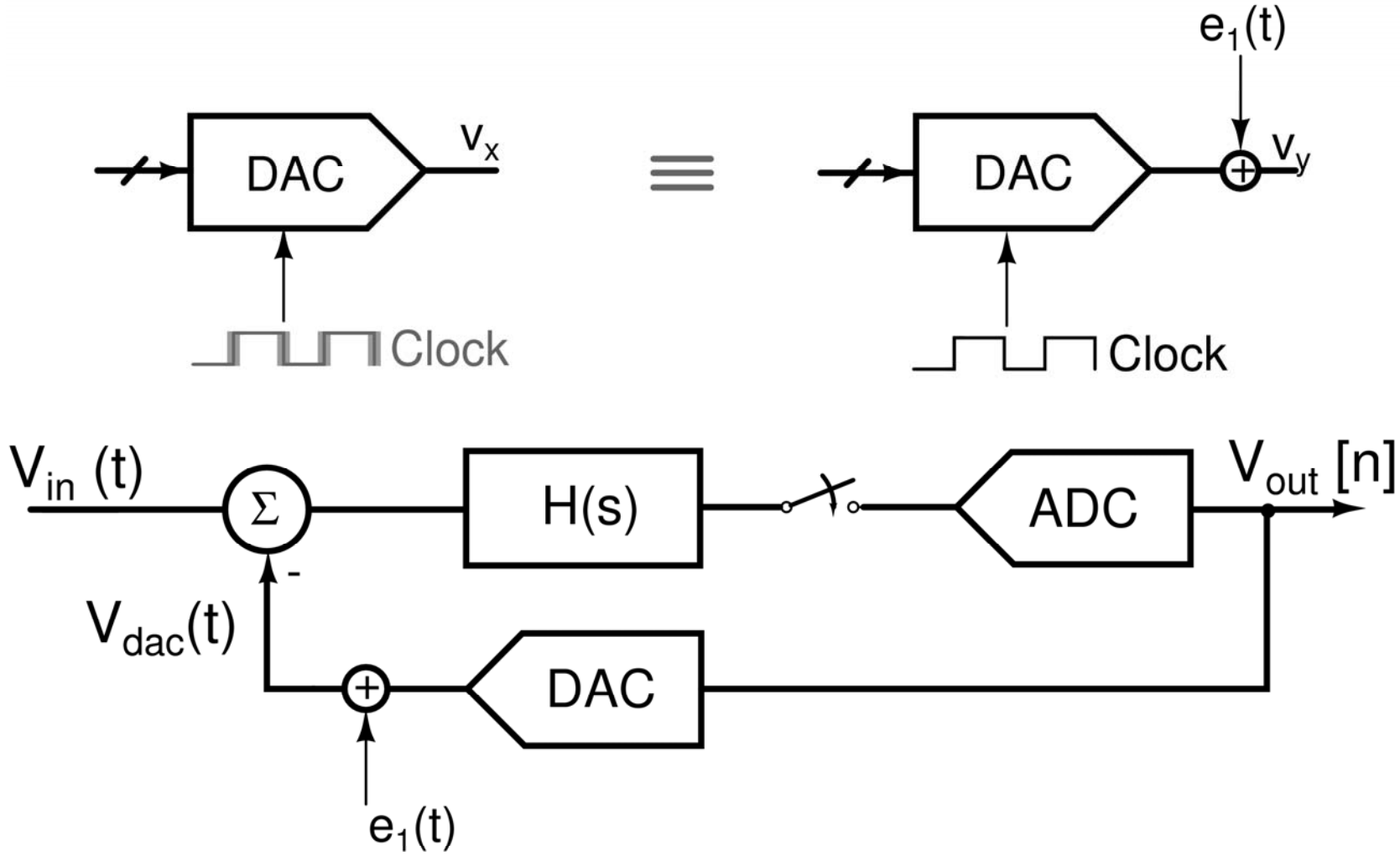
DAC : 1 bit versus 4 bit



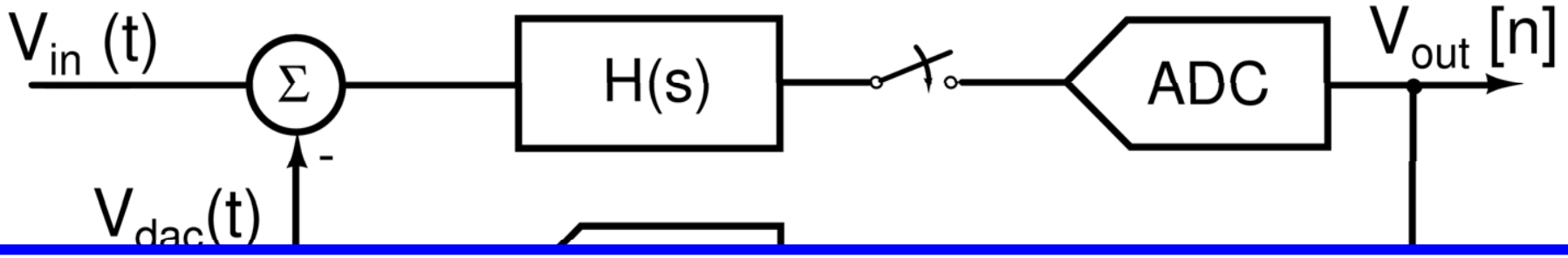
A single bit quantizer consumes
lesser power
though it operates at 3x the speed

Complex logic

Modeling Clock Jitter

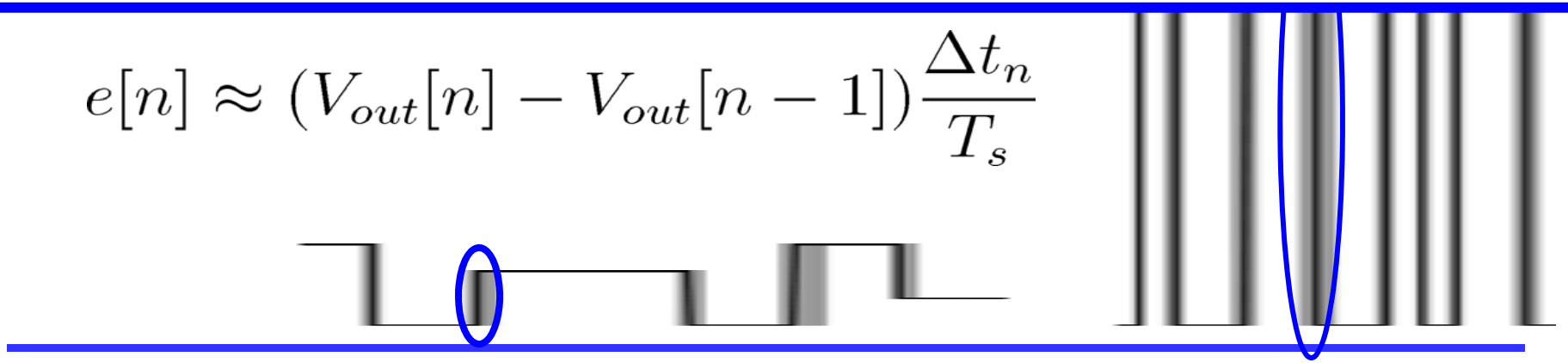


Clock Jitter Comparison

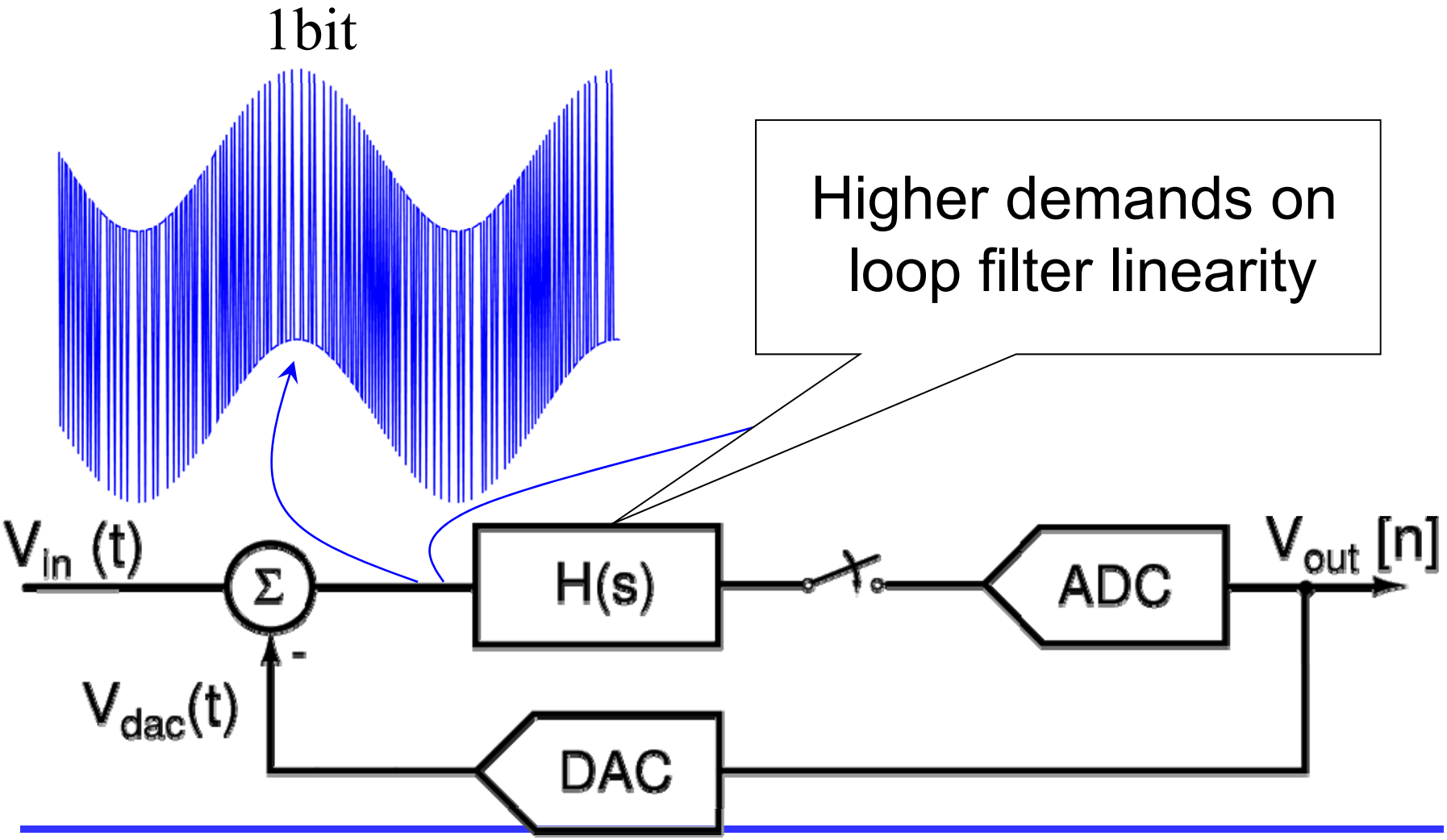


A 4-bit modulator can tolerate 15 times more RMS white jitter compared to a single bit design

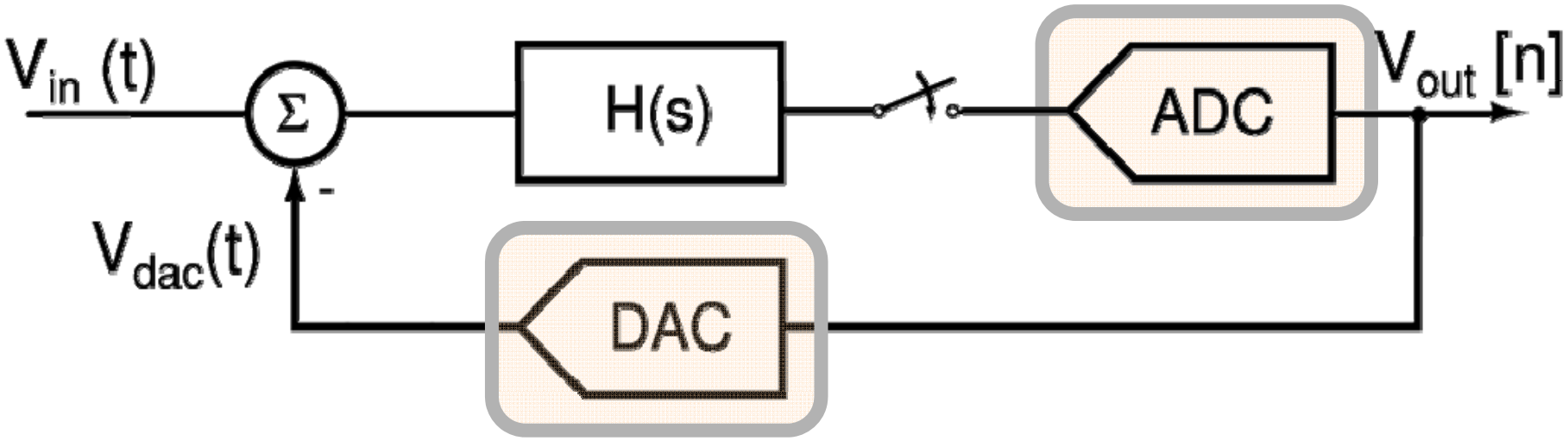
$$e[n] \approx (V_{out}[n] - V_{out}[n-1])\frac{\Delta t_n}{T_s}$$



Loop Filter Linearity



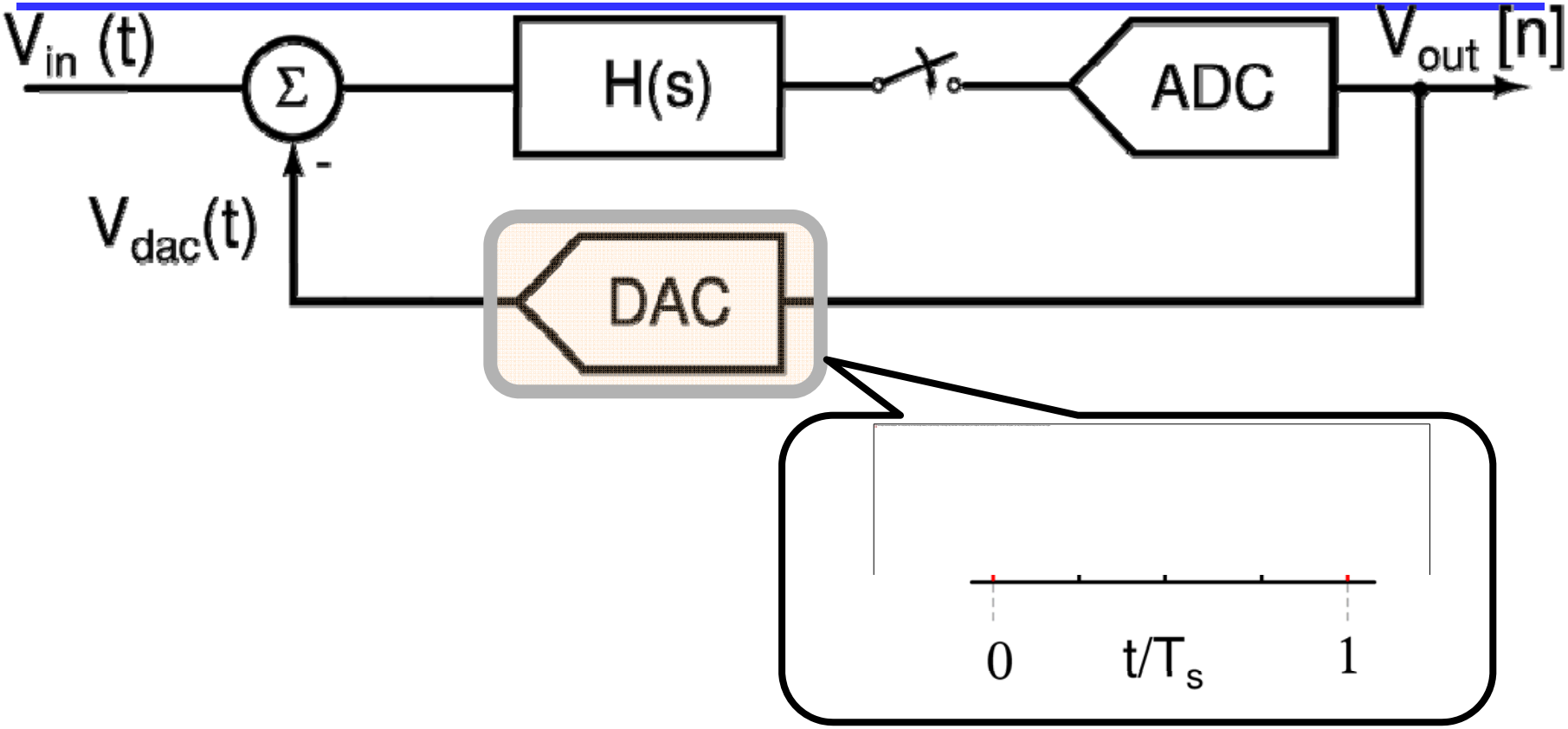
Choice of Quantizer



- Single bit quantizer
  - Lower power ADC
  - No DEM needed
  - Sensitive to clock jitter
  - Loop filter needs to be extremely linear

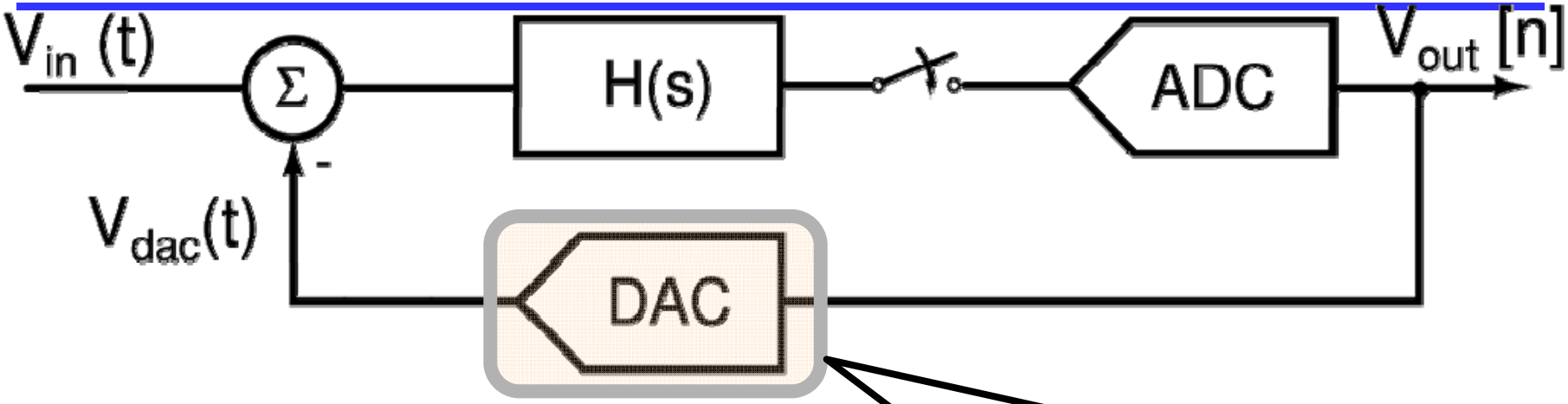
Try to fix this

DAC Pulse Shapes : NRZ



Inherently nonlinear (rise-fall asymmetry)

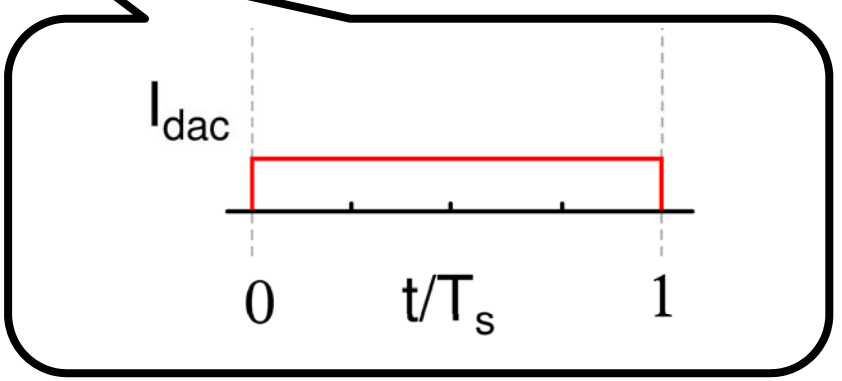
DAC Pulse Shapes : NRZ



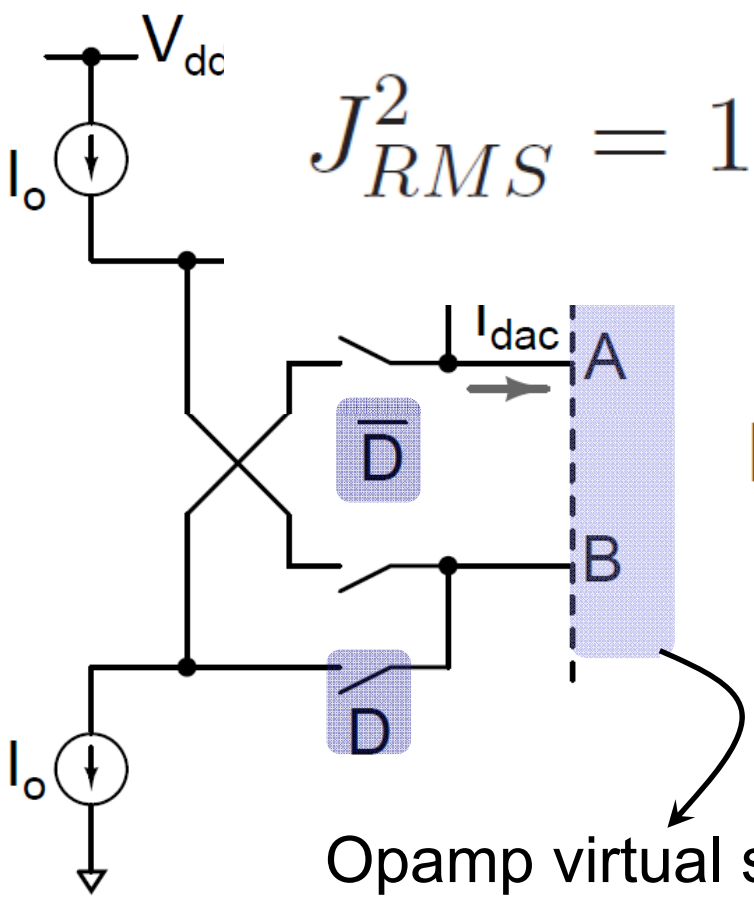
$$\frac{T_{rise} - T_{fall}}{T_s} = 1\%$$

$$HD_2 \approx 55\,\mathrm{dB}\,!$$

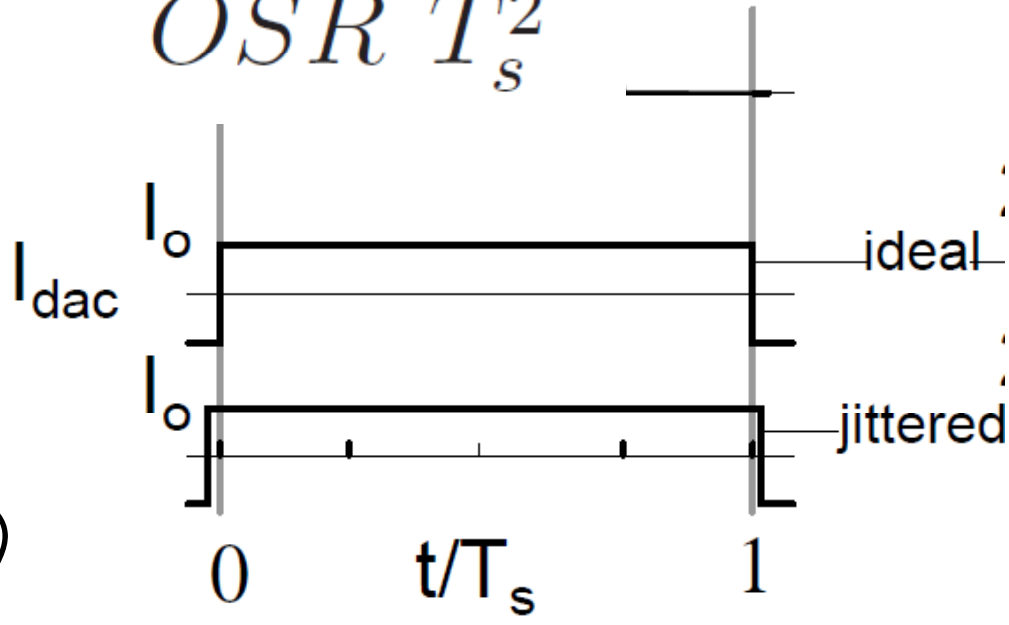
$$HD_2 \approx 90\,\mathrm{dB}\,(\mathrm{diff.operation})$$



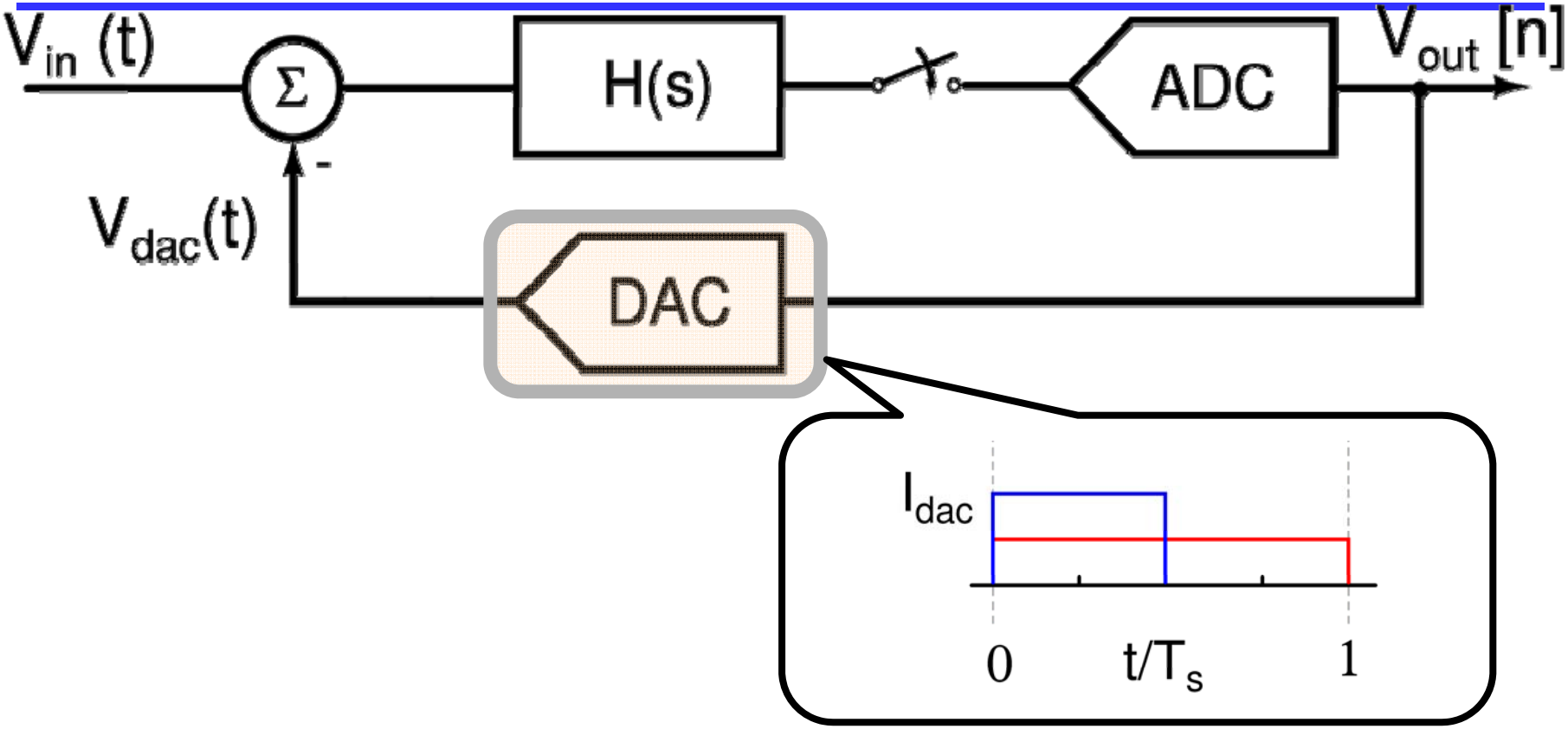
DAC Pulse Shapes : NRZ



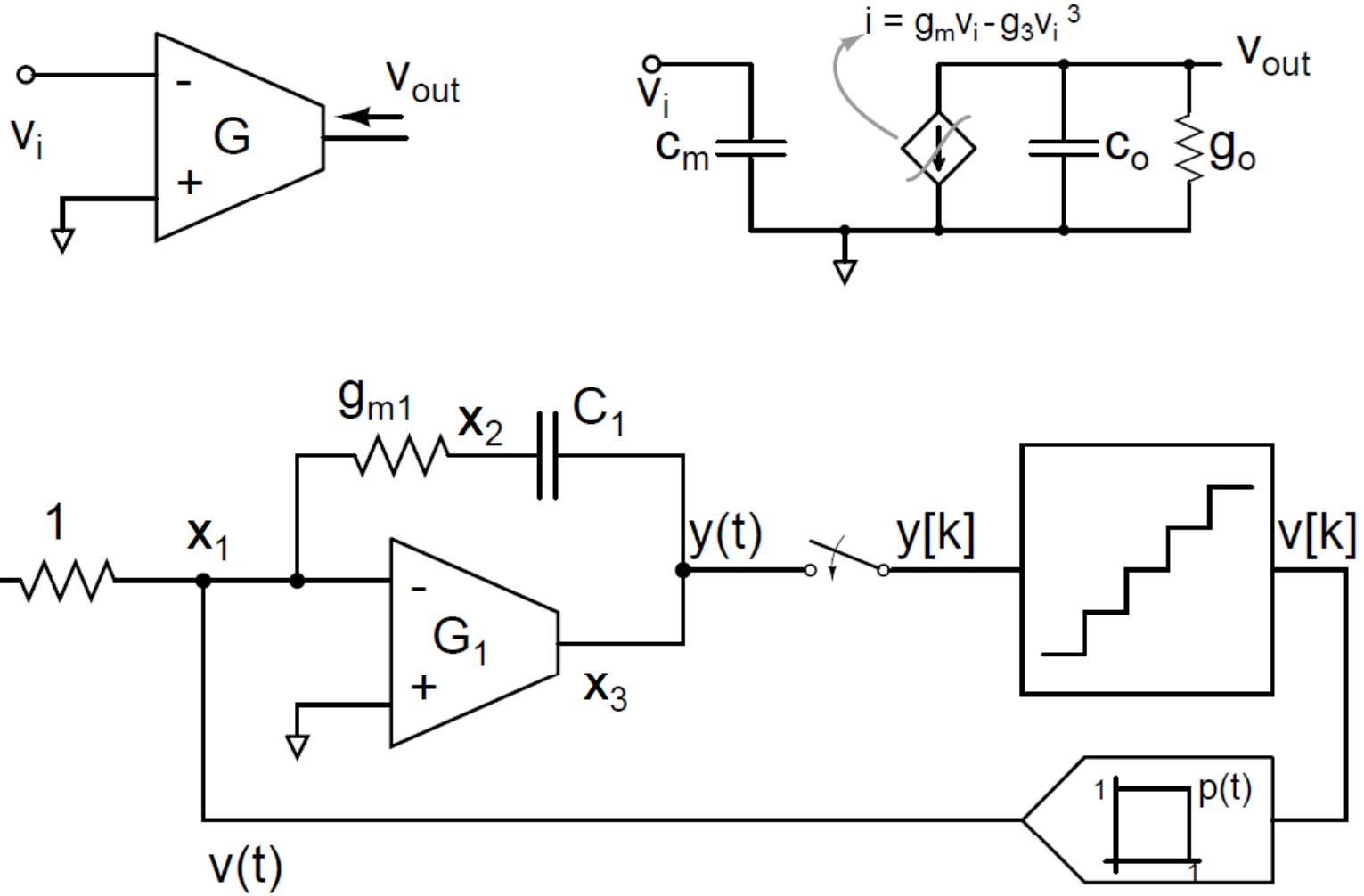
$$J^2_{RMS} = 16\lambda \frac{I_o^2}{OSR} \frac{\sigma^2_{\Delta t}}{T_s^2}$$

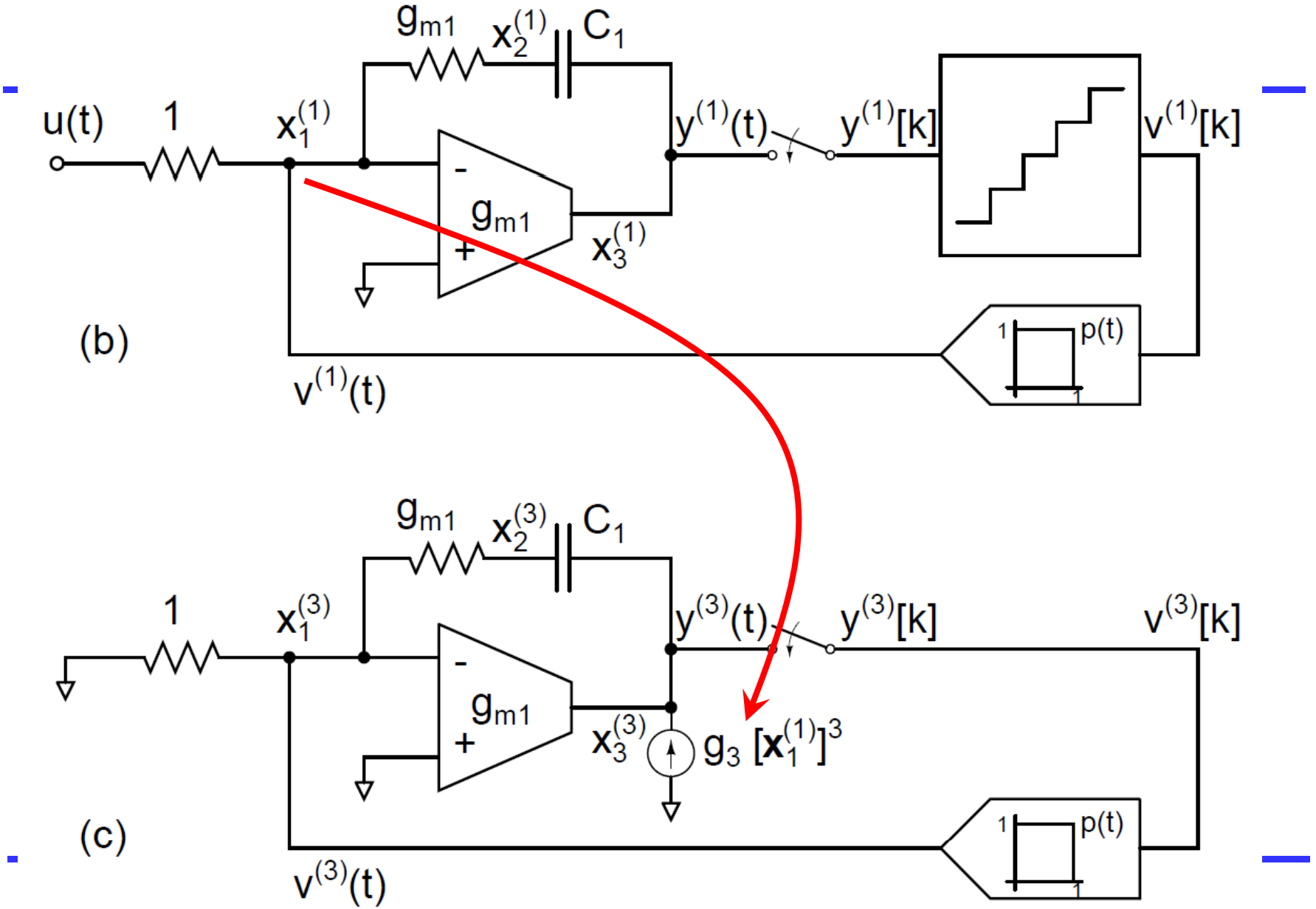


DAC Pulse Shapes : RZ

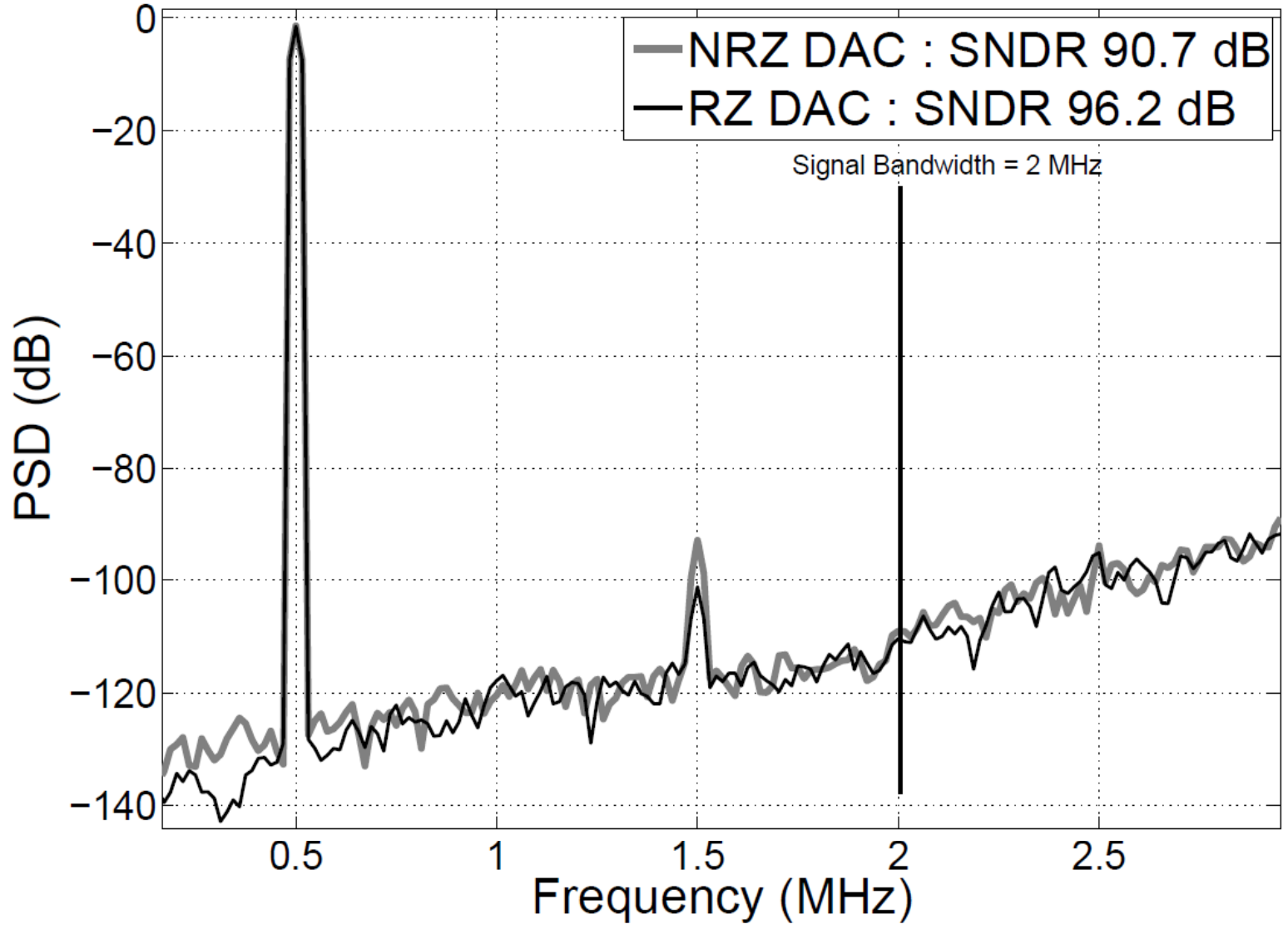


Digression : Weak Nonlinearities in CTDSMs




g_{m1}
$x_2^{(1)}$
C_1
u(t)
1
$x_1^{(1)}$
$y^{(1)}(t)$
$y^{(1)}[k]$
$v^{(1)}[k]$
-
g_{m1}
+
$x_3^{(1)}$
(b)
$v^{(1)}(t)$
1
p(t)
g_{m1}
$x_2^{(3)}$
C_1
1
$x_1^{(3)}$
$y^{(3)}(t)$
$y^{(3)}[k]$
$v^{(3)}[k]$
-
g_{m1}
+
$x_3^{(3)}$
g_3 $[x_1^{(1)}]^3$
(c)
$v^{(3)}(t)$
1
p(t)

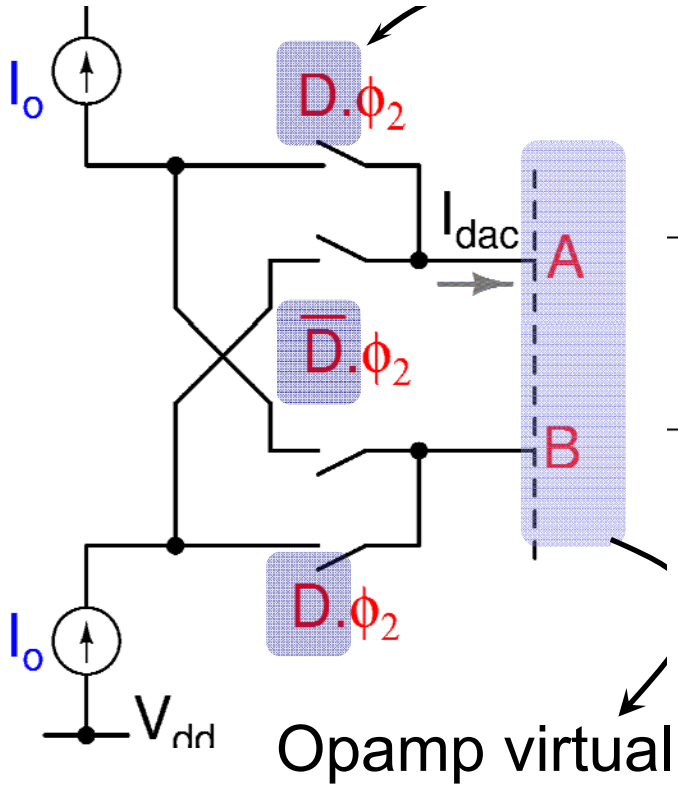
RZ DAC : Linearity



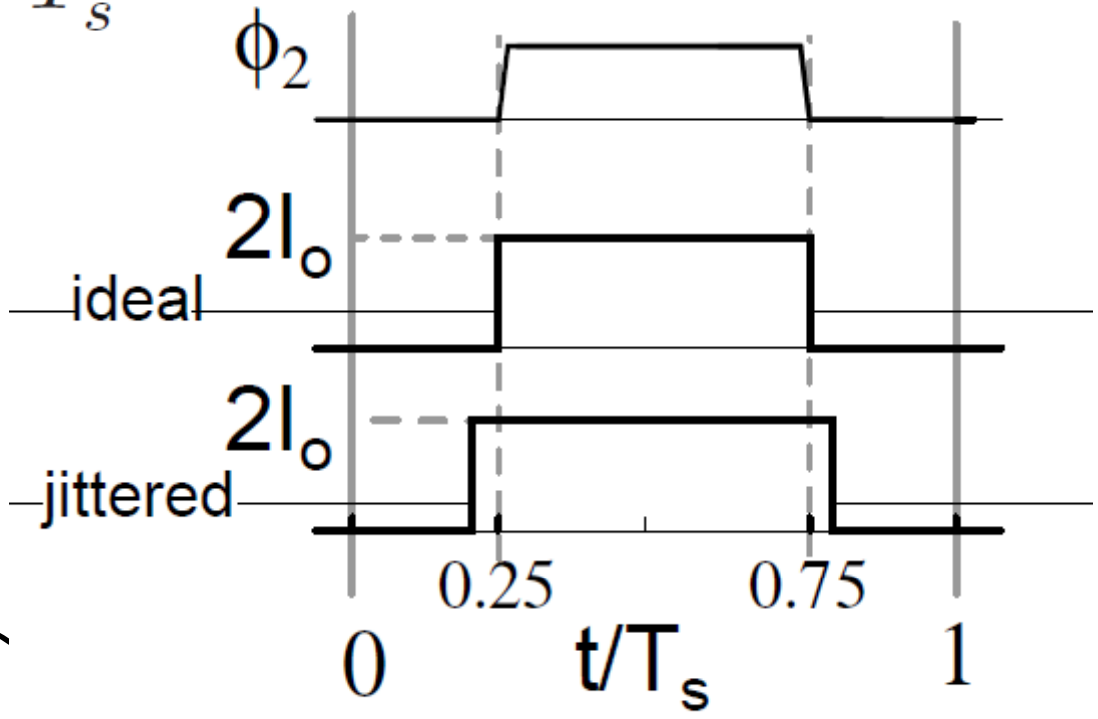
RZ DAC : Jitter

$$J^2_{RMS} = 32 \frac{I_o^2}{OSR} \frac{\sigma^2_{\Delta t}}{T_s^2}$$

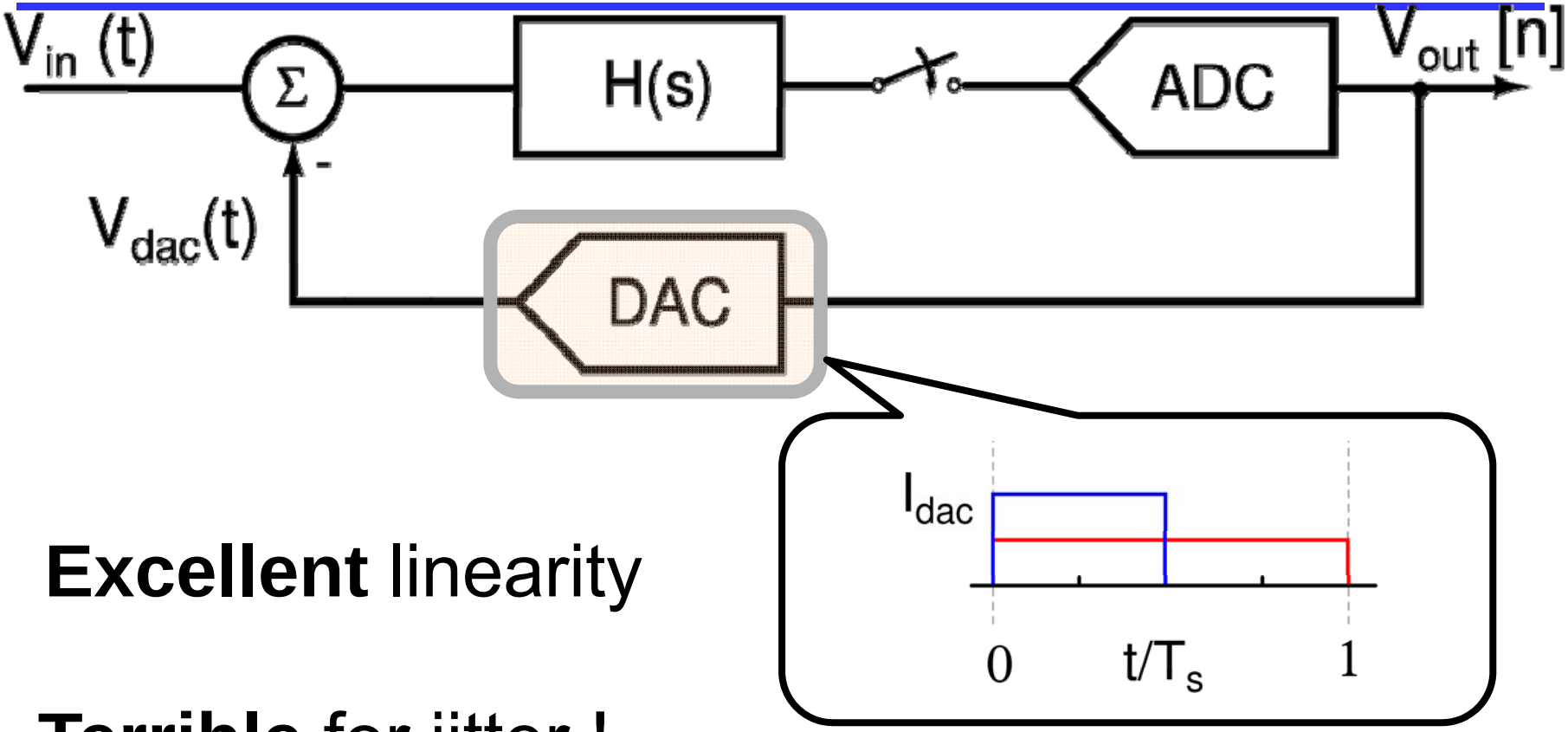
4.5 dB worse than an NRZ DAC



Opamp virtual short



DAC Pulse Shapes : RZ

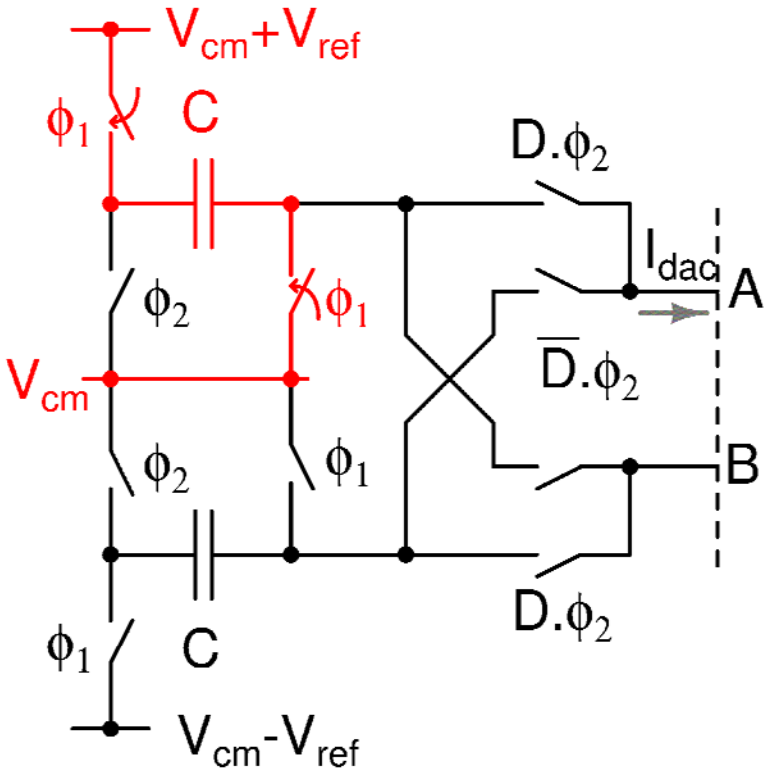


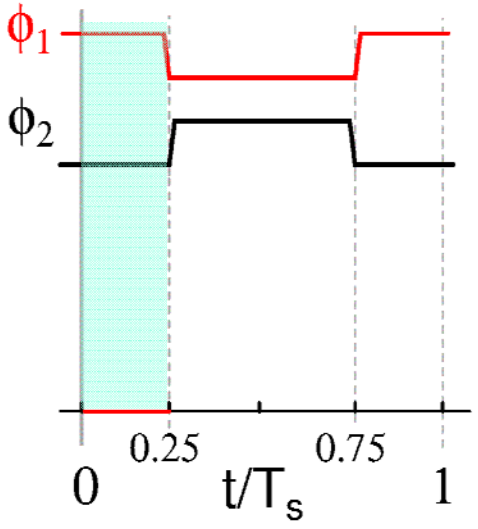
Excellent linearity

Terrible for jitter !

SC DAC

- Capacitors are charged to $\pm V_{ref}$ during Φ_1
- They are discharged into the loopfilter during Φ_2
- Charge transferred = $\pm CV_{ref}$





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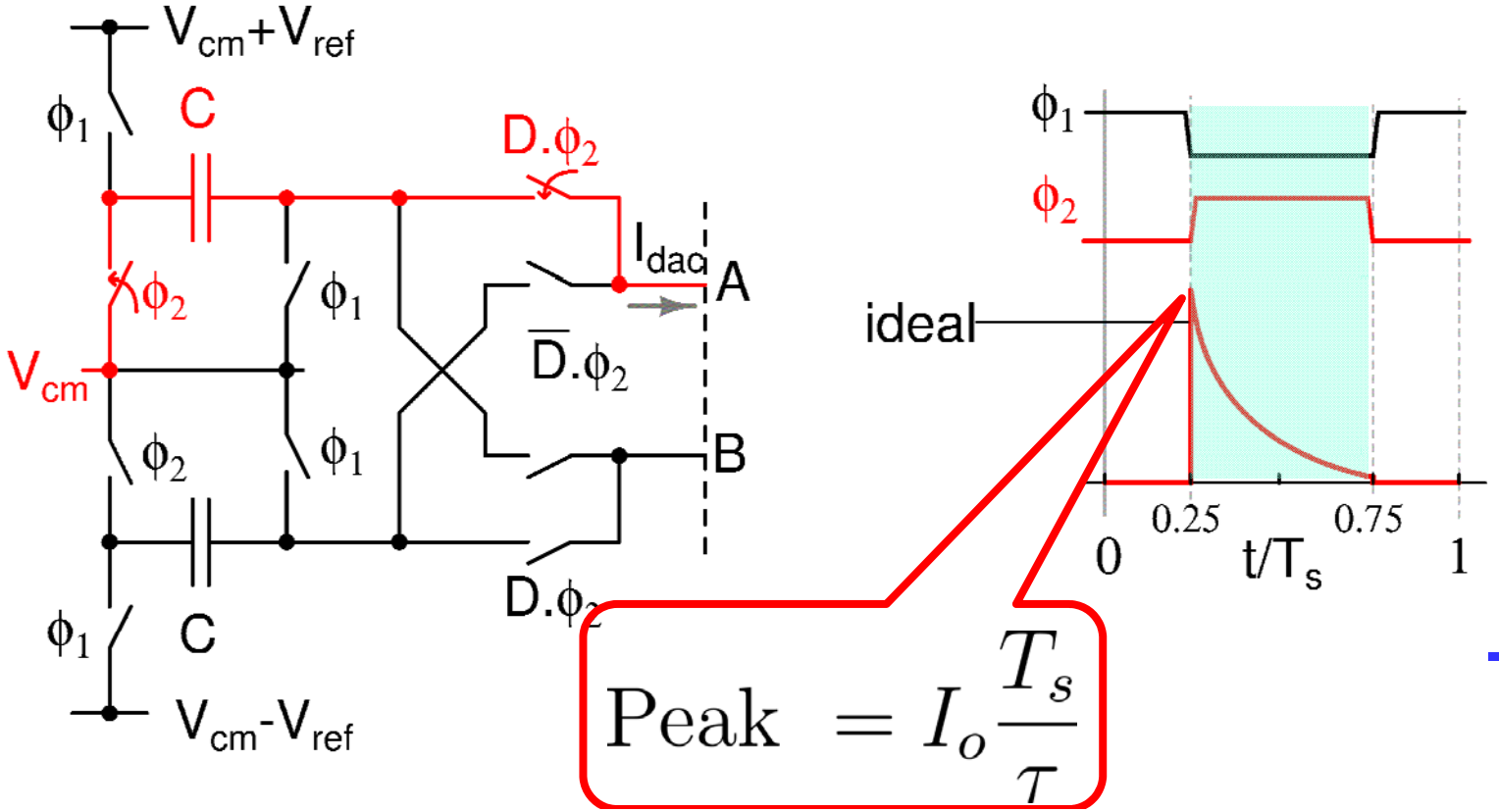
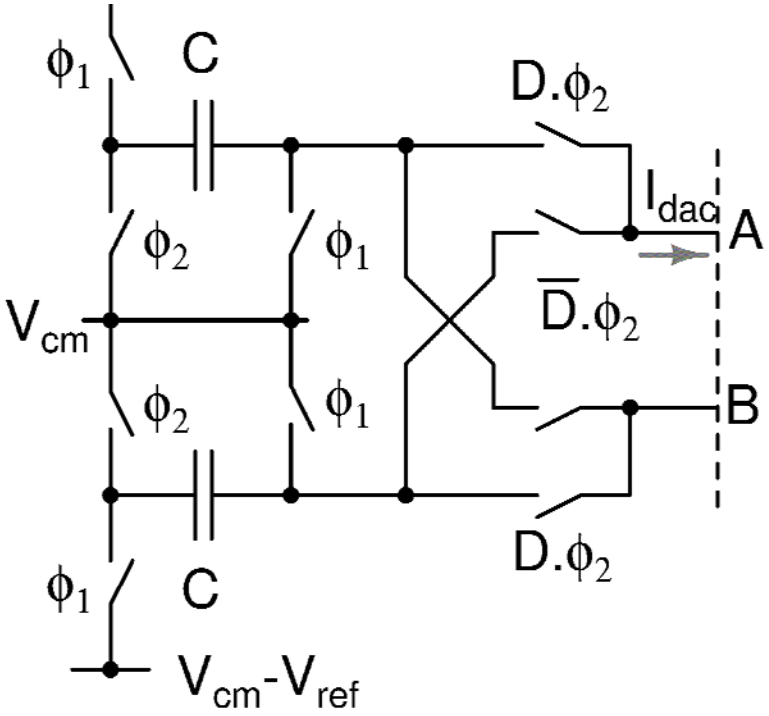


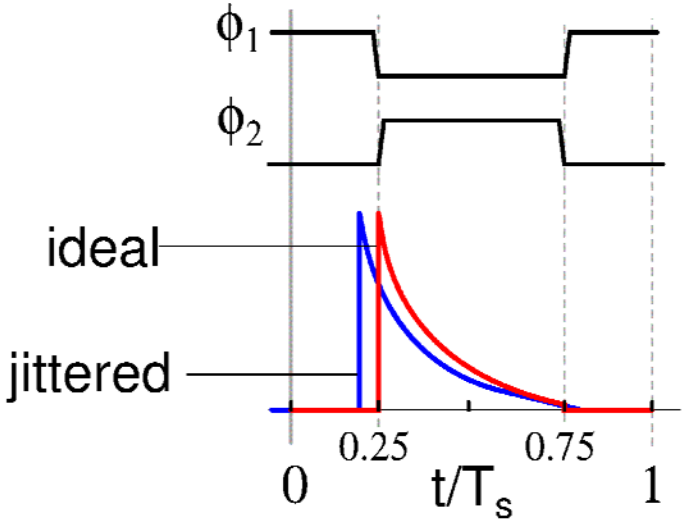
$$\text{Peak} = I_o \frac{T_s}{\tau}$$

SC DAC with Jitter

- Transfers most of the charge in a short period

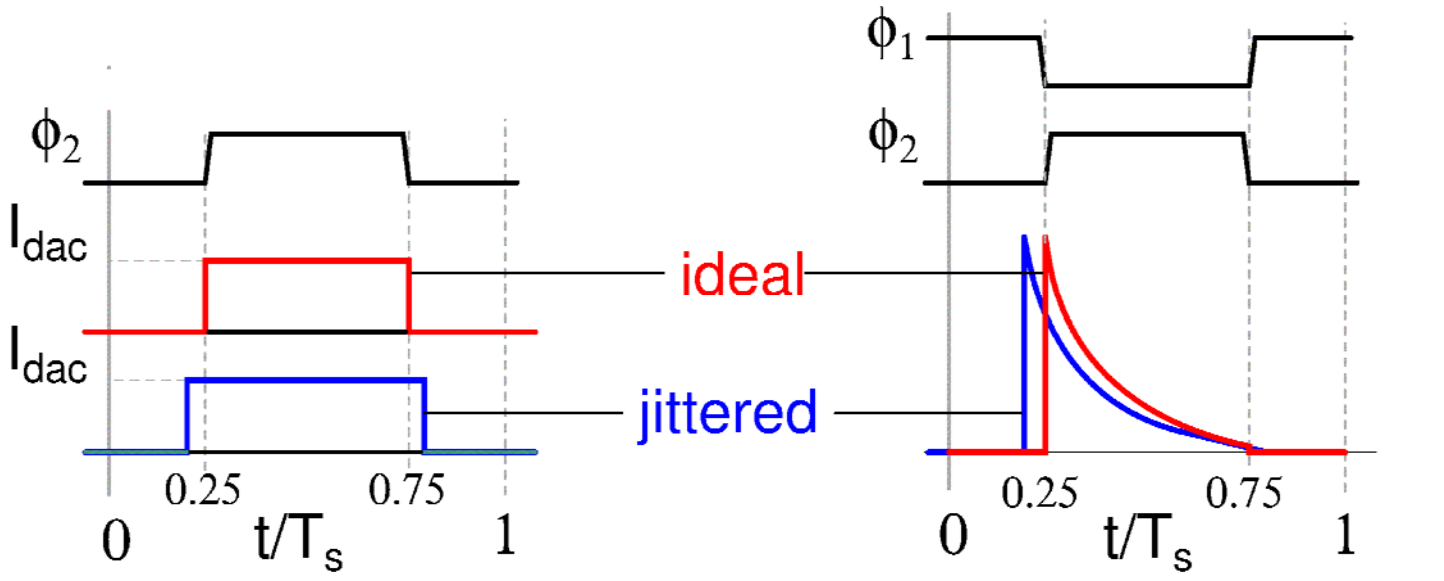
$$J_{RMS}^2 = 8\frac{I_o^2}{OSR}\left(\frac{T_s}{\tau}\right)^2 \exp\left(-\frac{T_s}{\tau}\right)\frac{\sigma_{\Delta t}^2}{T_s^2}$$





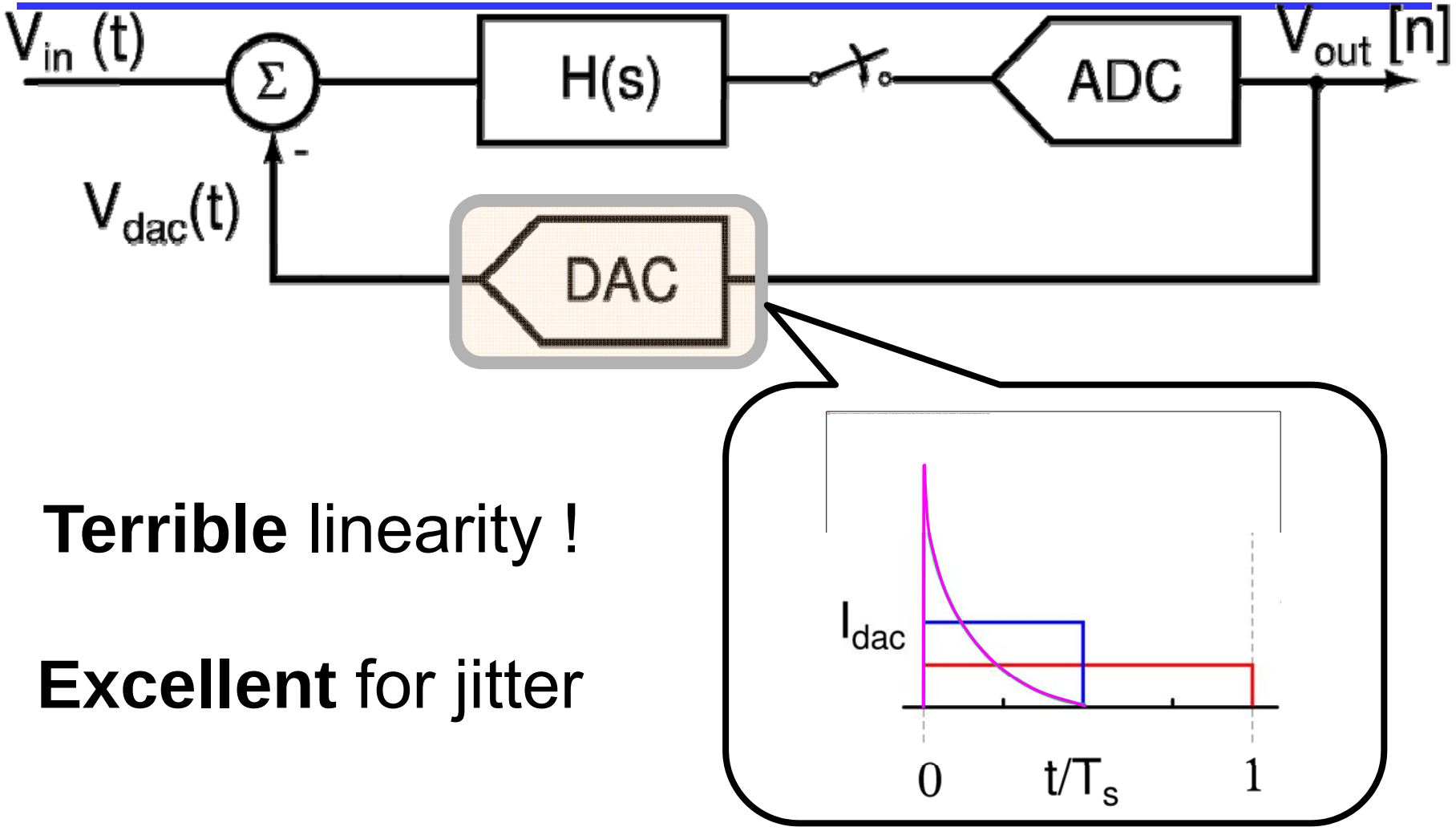
SC DAC

- DAC output peak current is higher
- Higher demands on the linearity of the loop filter



(a) RZ DAC waveform (b) SC DAC waveform

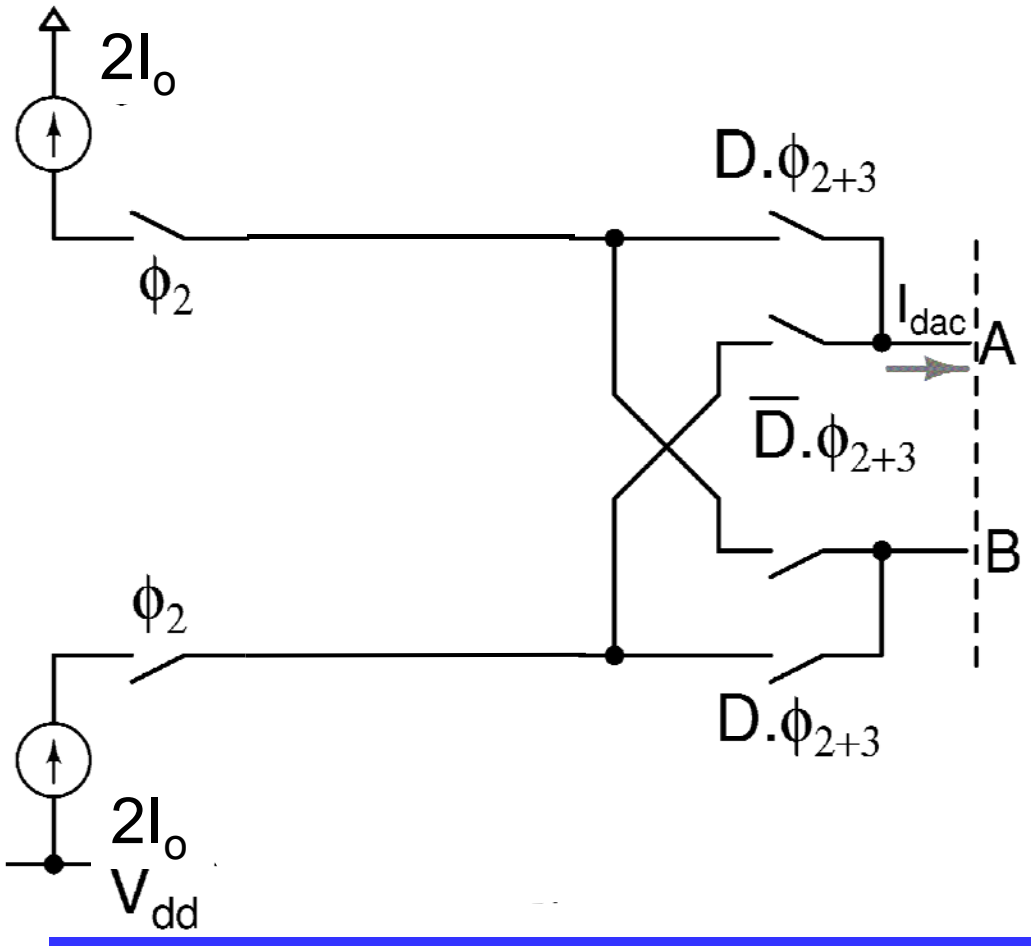
DAC Pulse Shapes : SC



Terrible linearity !

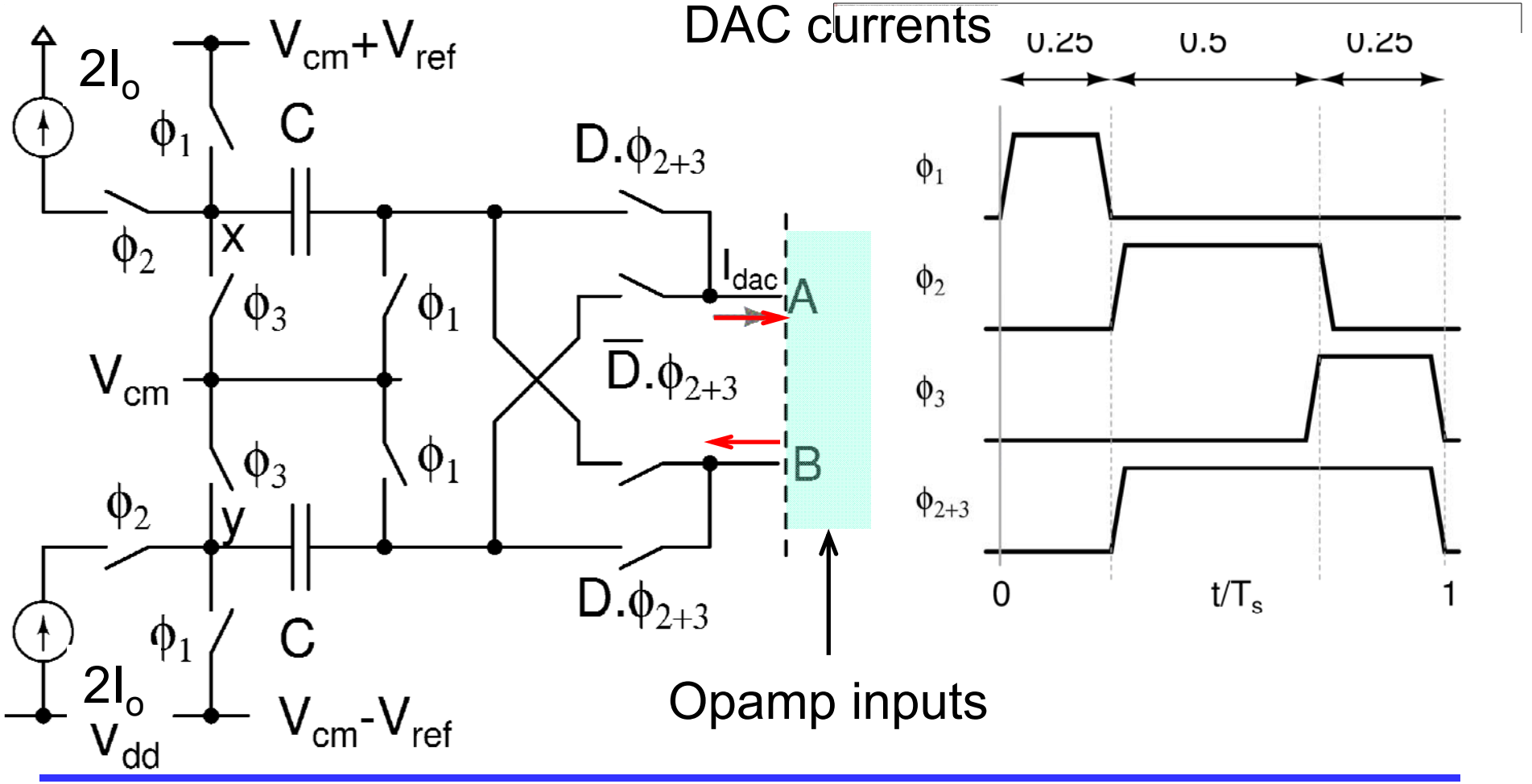
Excellent for jitter

Introducing the SCRZ DAC

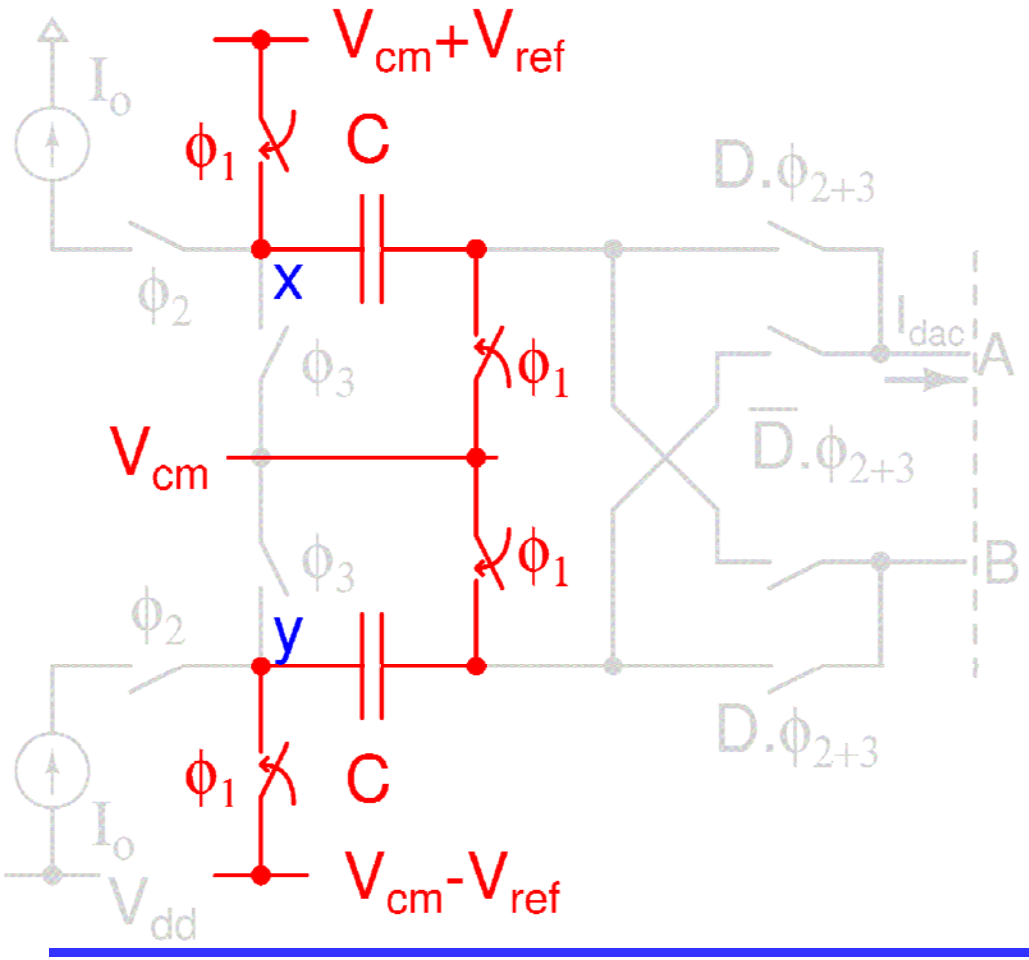


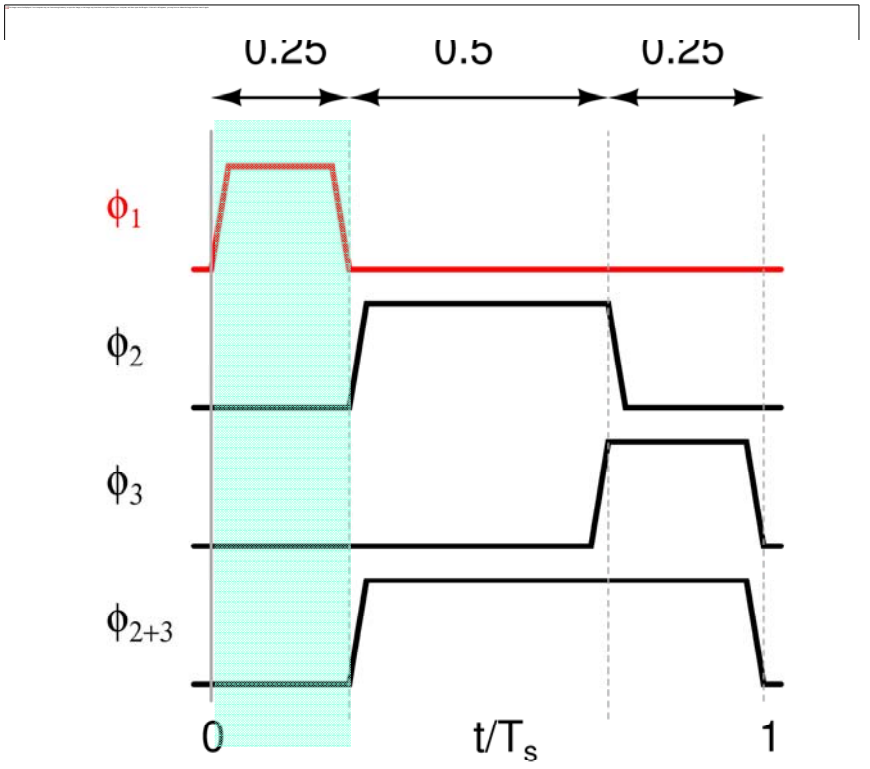
- RZ DAC
  - Excellent linearity
  - High jitter sensitivity
- SC DAC
  - Low jitter sensitivity
  - Poor linearity
- SCRZ DAC

Introducing the SCRZ DAC

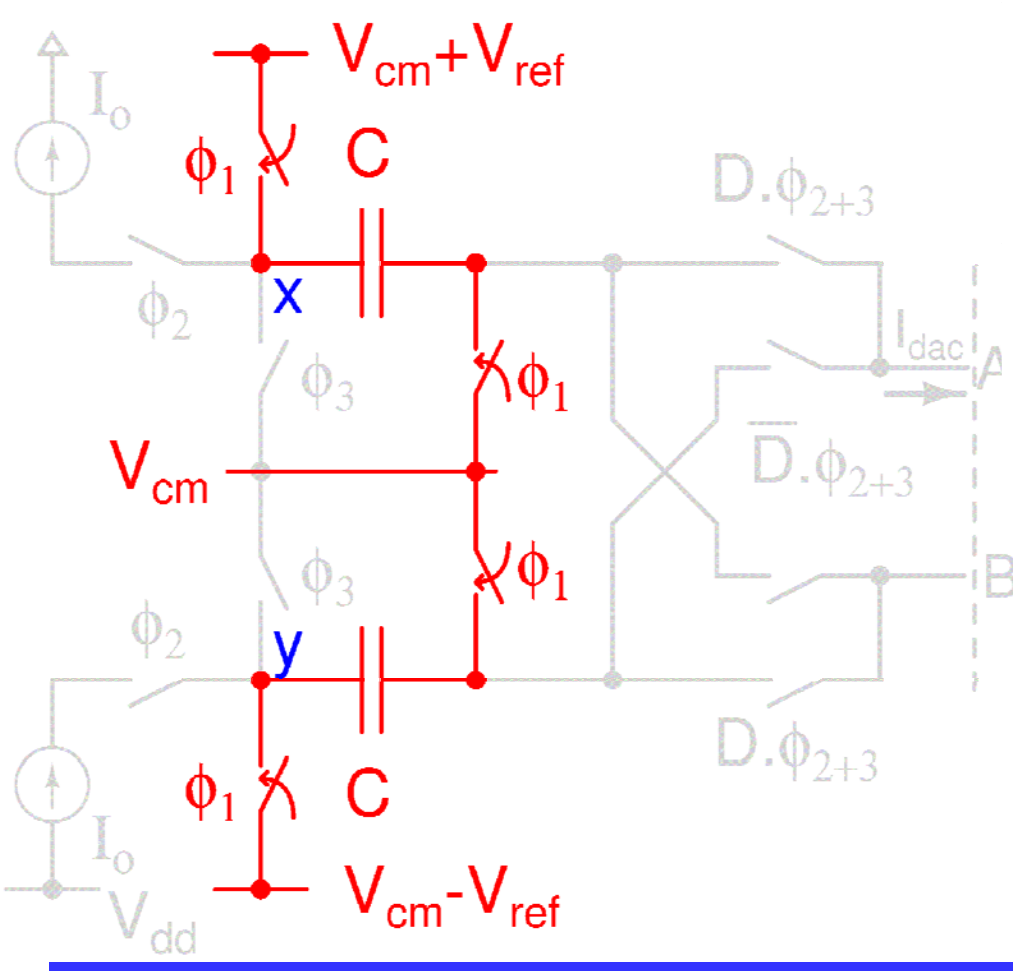


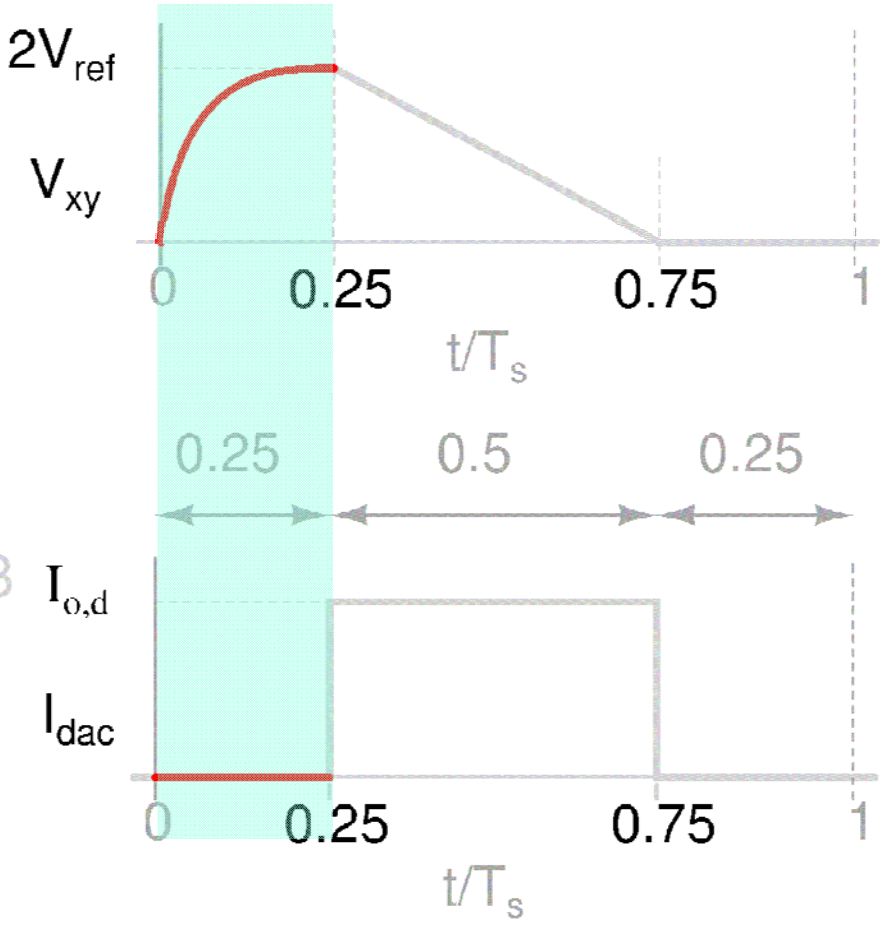
SCRZ DAC operation (Φ_1)



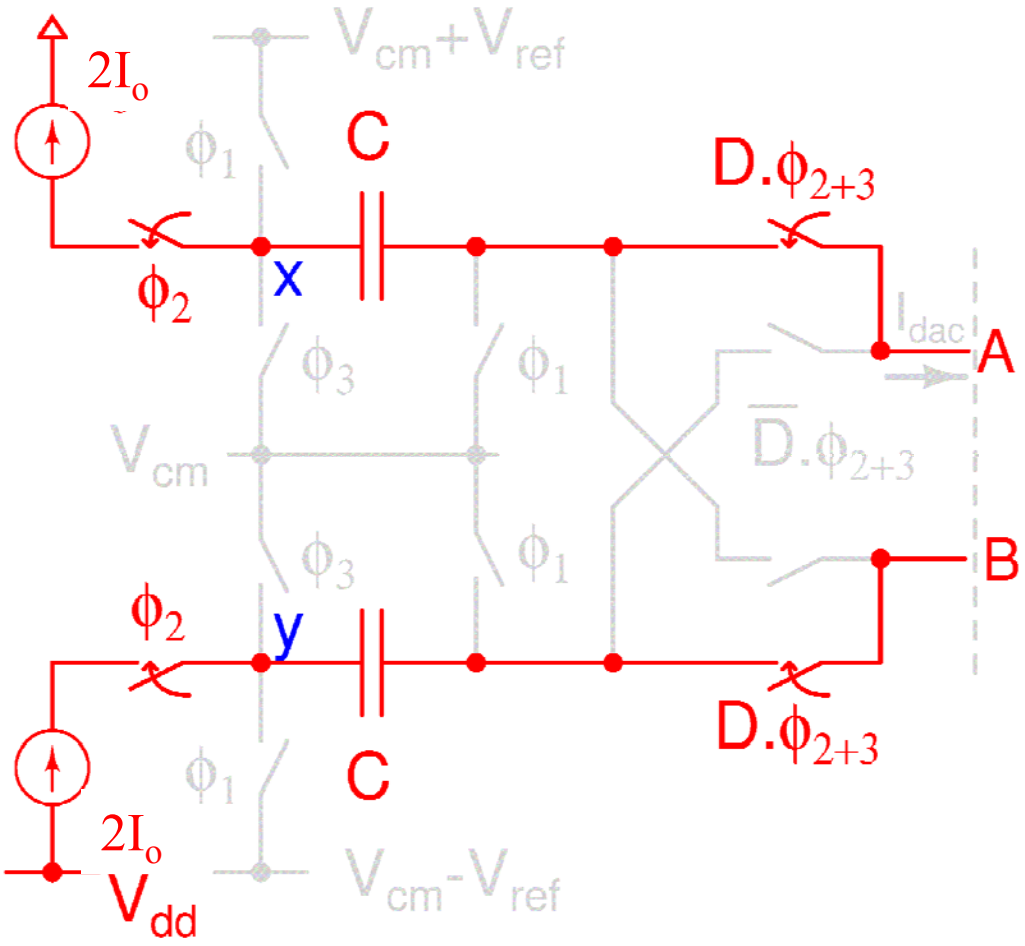


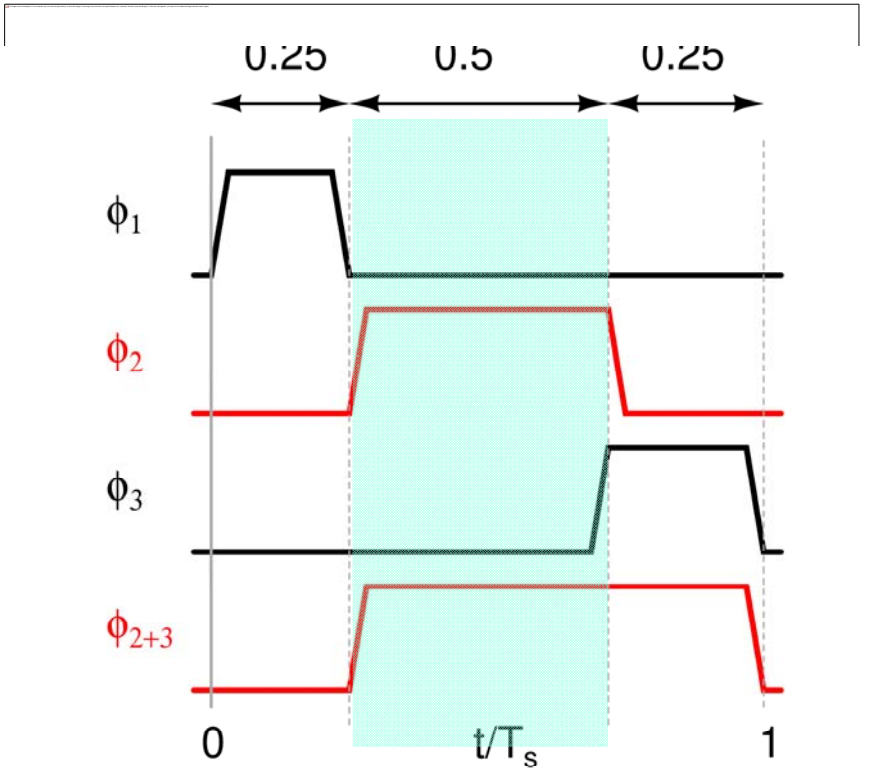
SCRZ DAC operation (Φ_1)





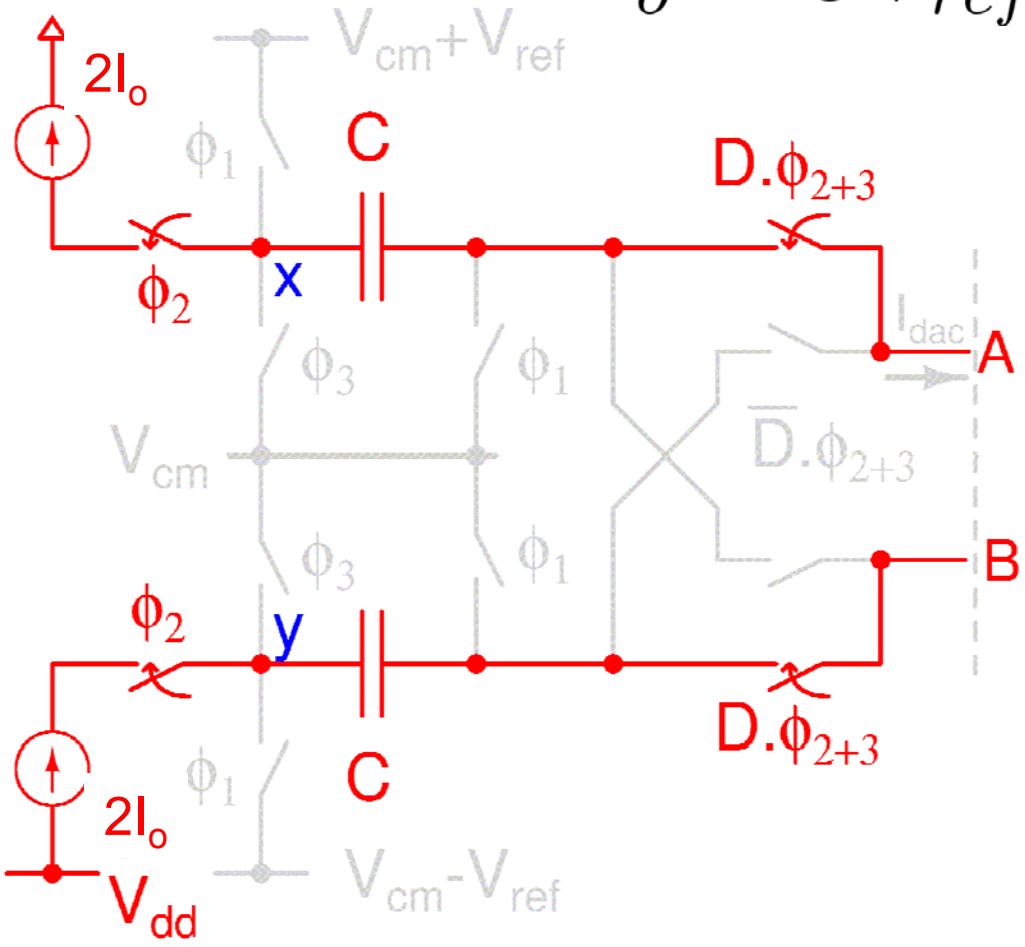
SCRZ DAC operation (Φ_2)

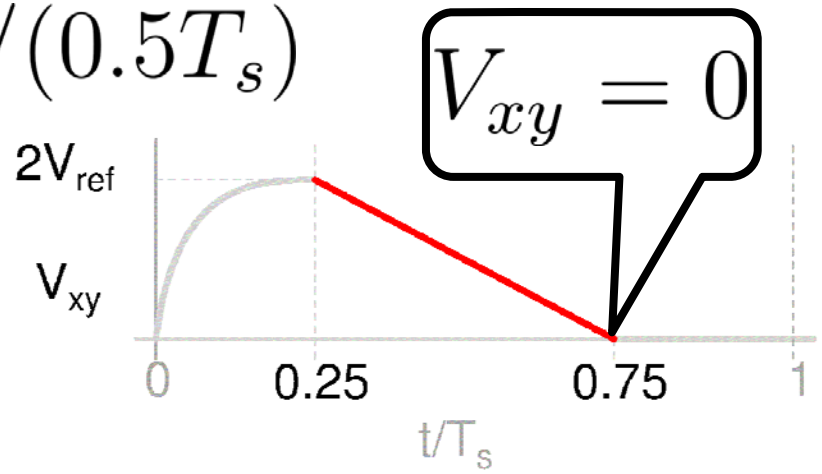


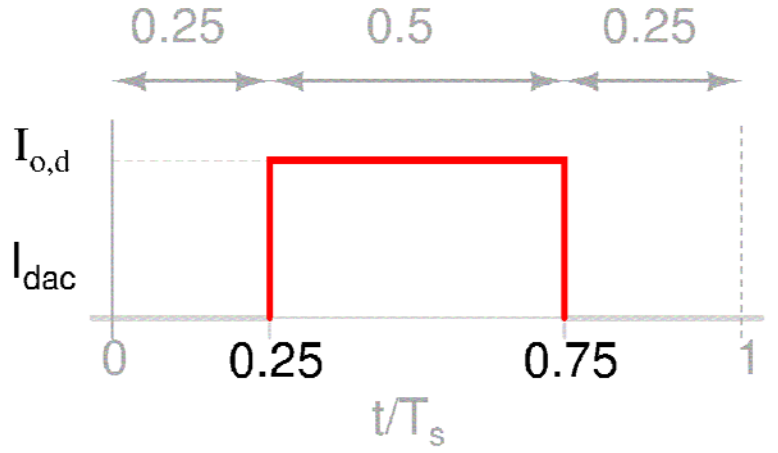


SCRZ DAC operation ($\Phi_2 = 0.5T_s$)

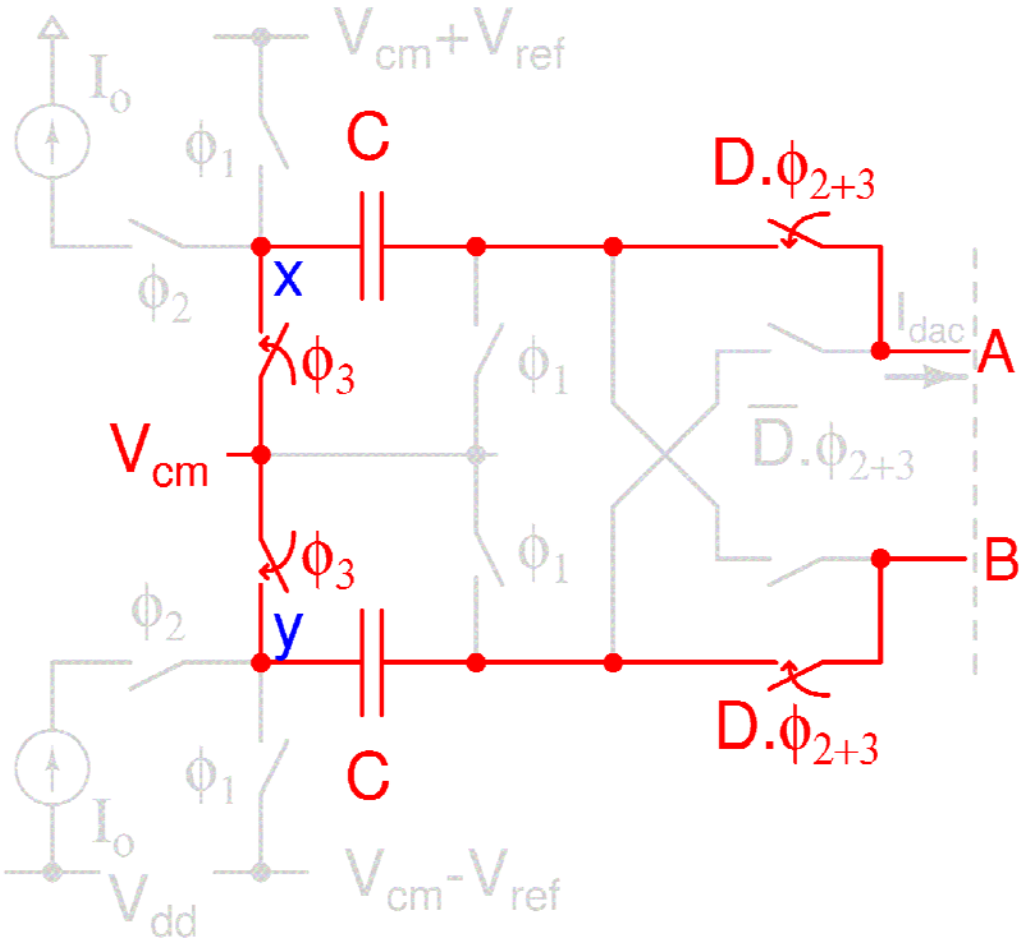
$$2I_o = CV_{ref}/(0.5T_s)$$

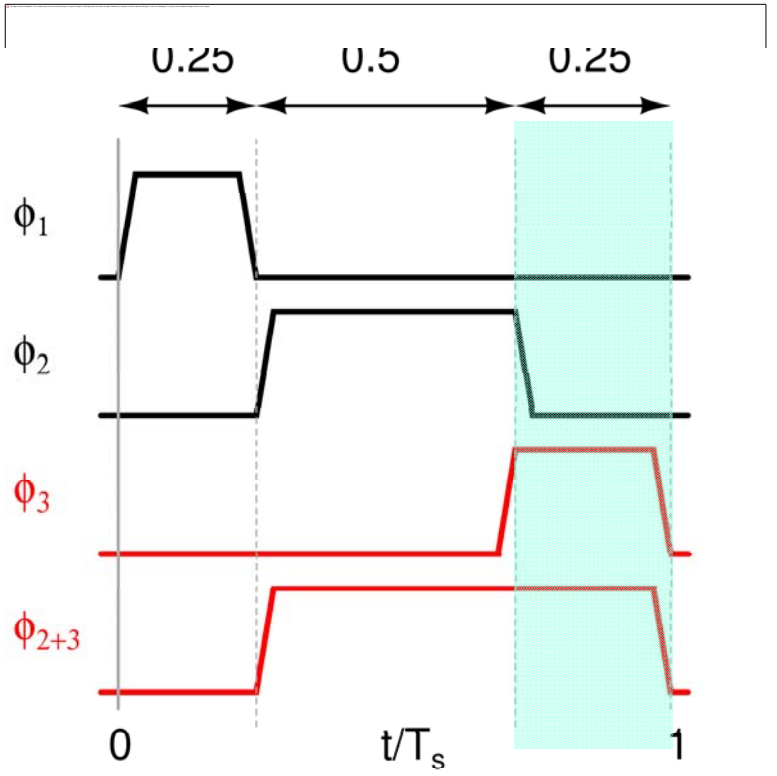




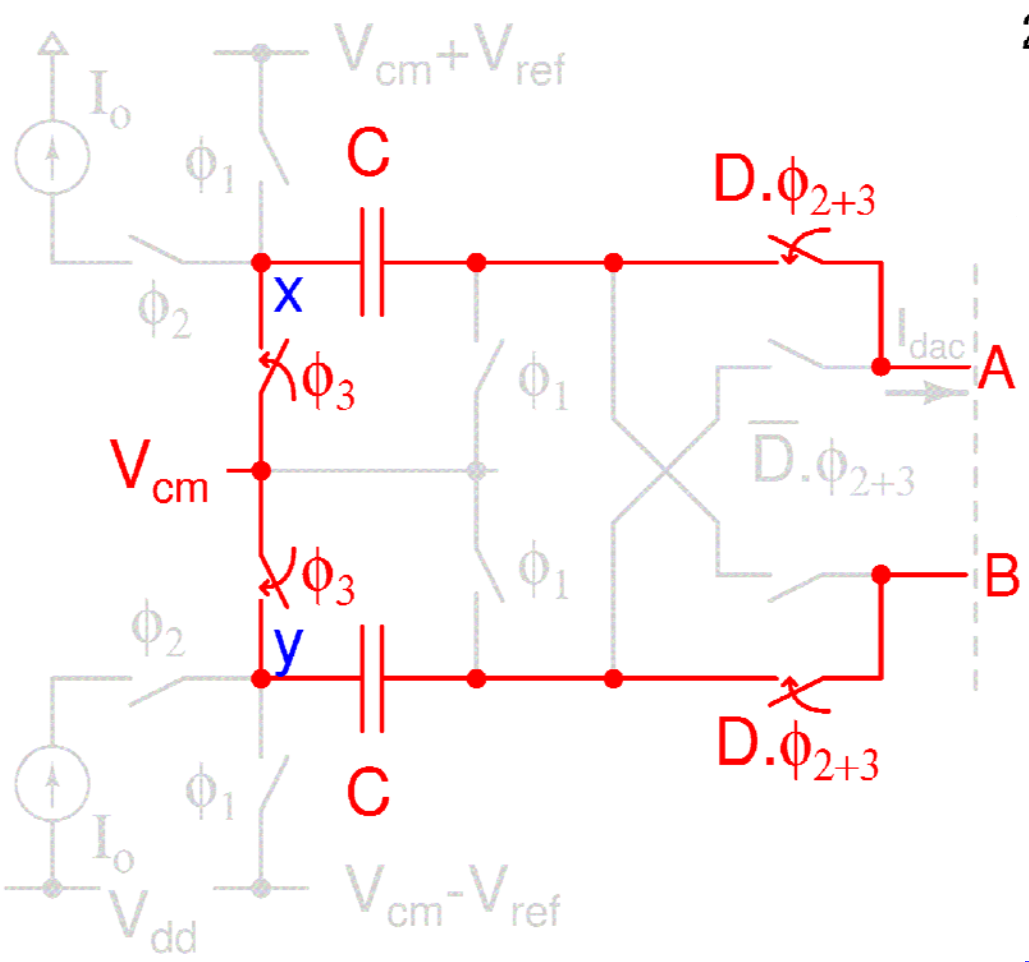


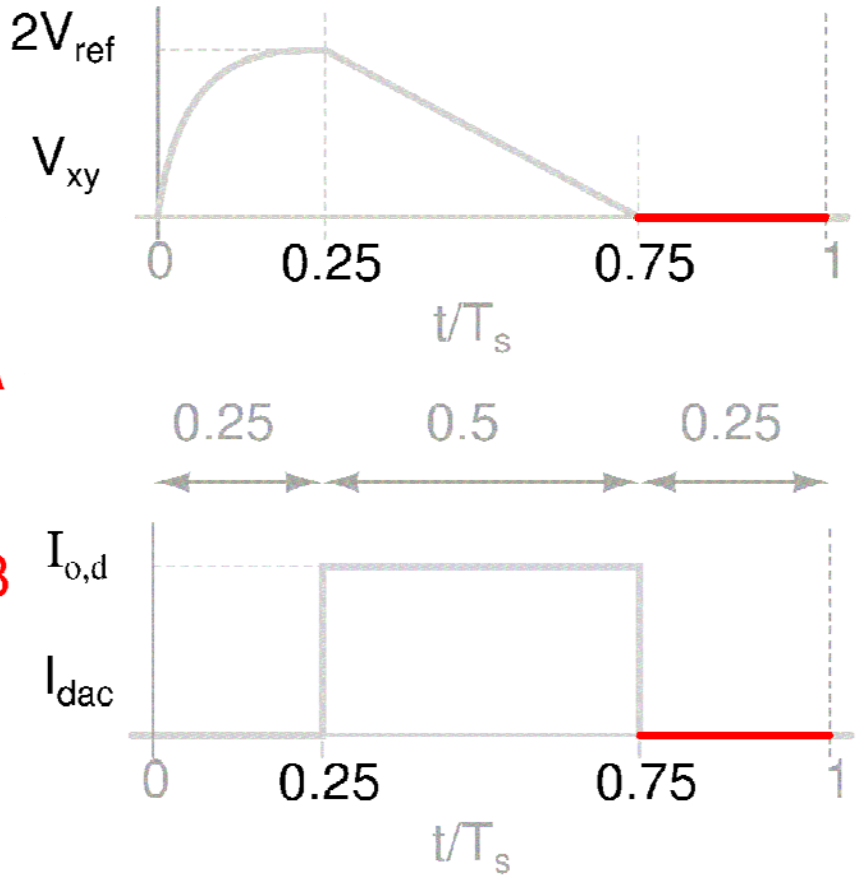
SCRZ DAC operation (Φ_3)





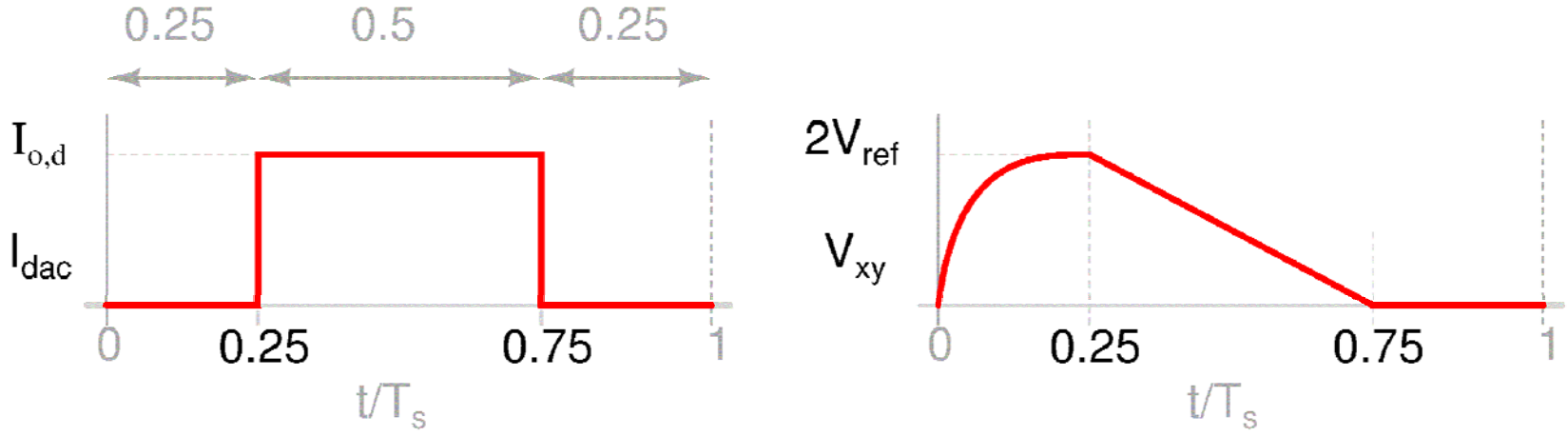
SCRZ DAC operation (Φ_3)





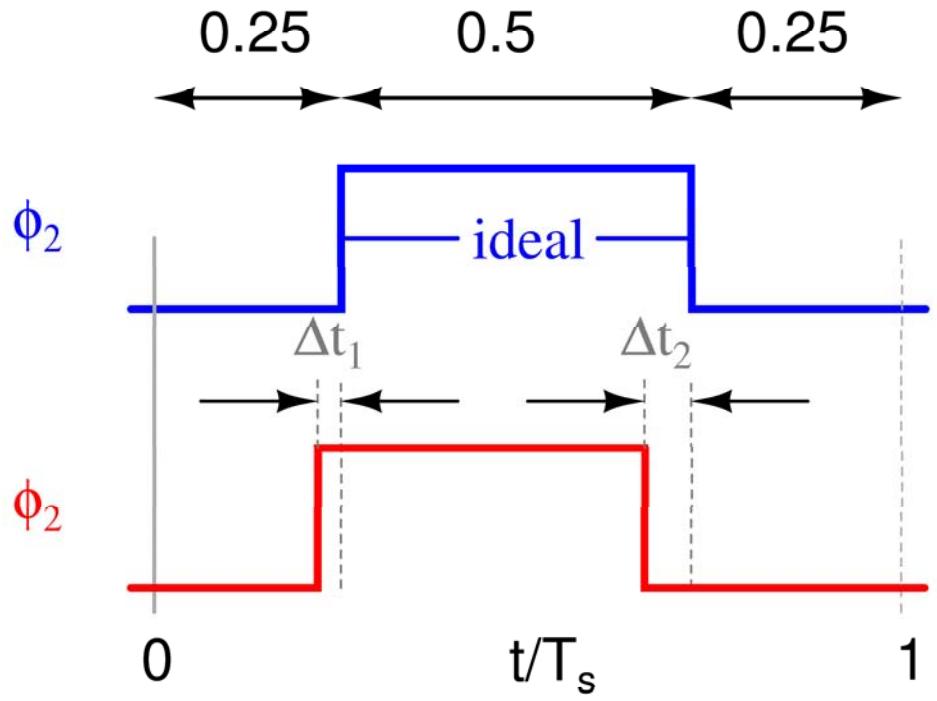
Summary : Ideal Waveforms

- With an ideal clock
- With ideal current $2I_o = CV_{ref}/(0.5T_s)$
  - I_{dac} has an RZ pulse shape

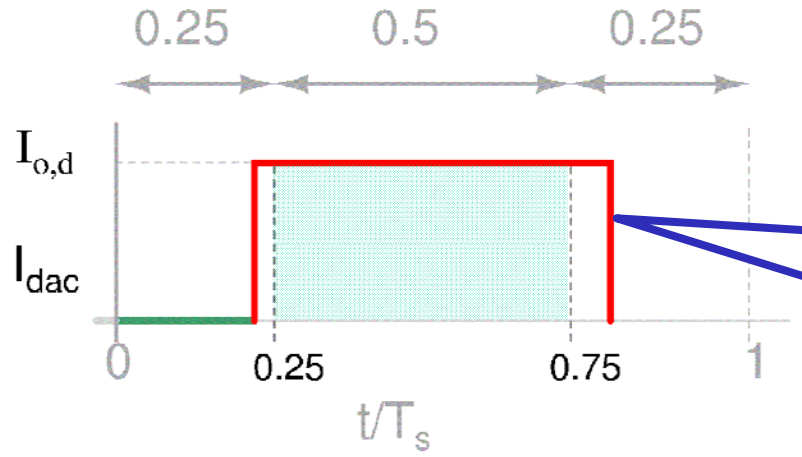


Effect of jitter

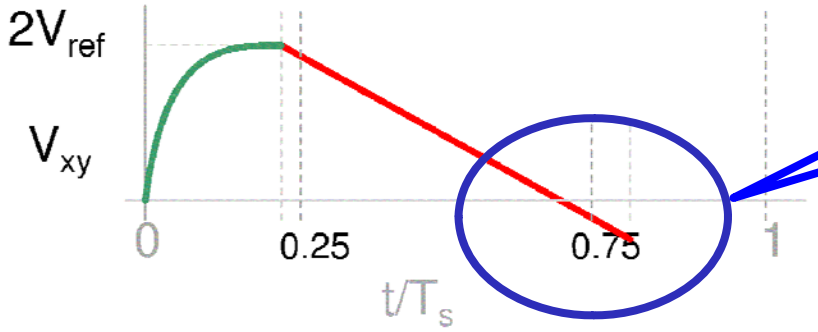
- Ideal – ϕ_2 half clock cycle wide
- Jittered - $0.5T_s + \tau$



Effect of jitter

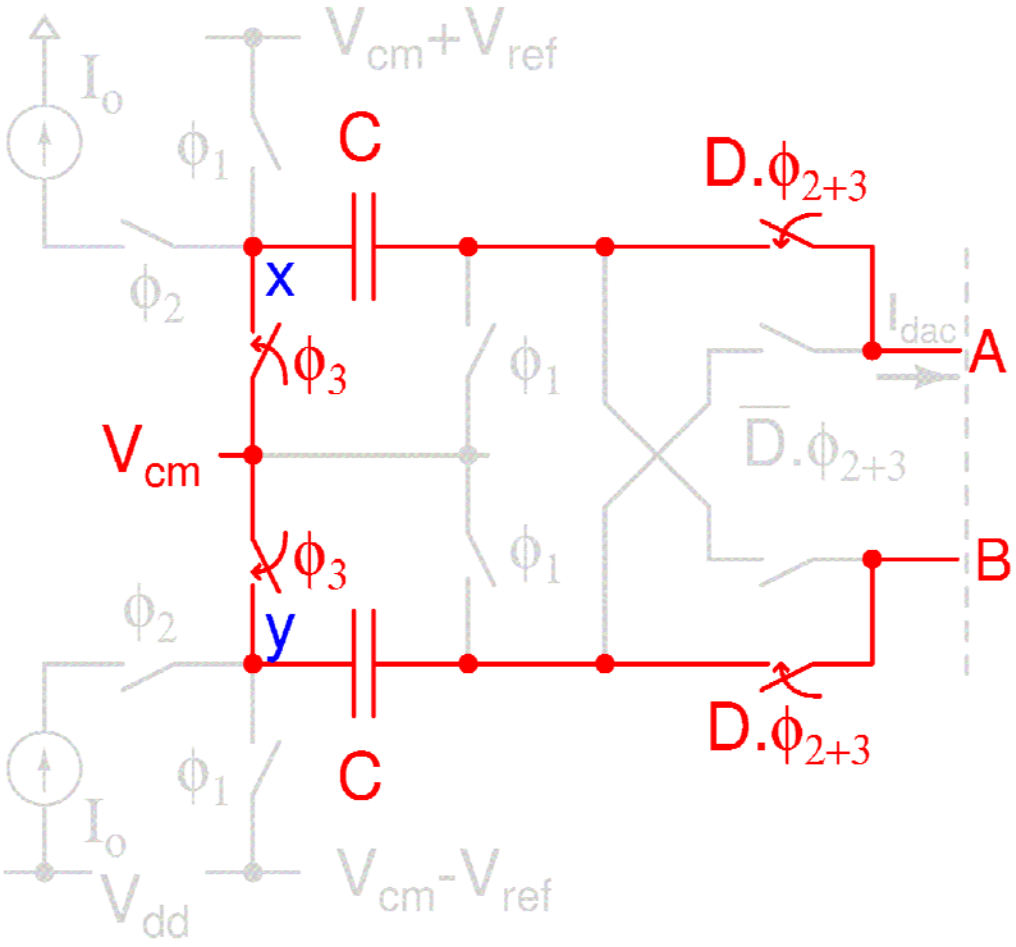


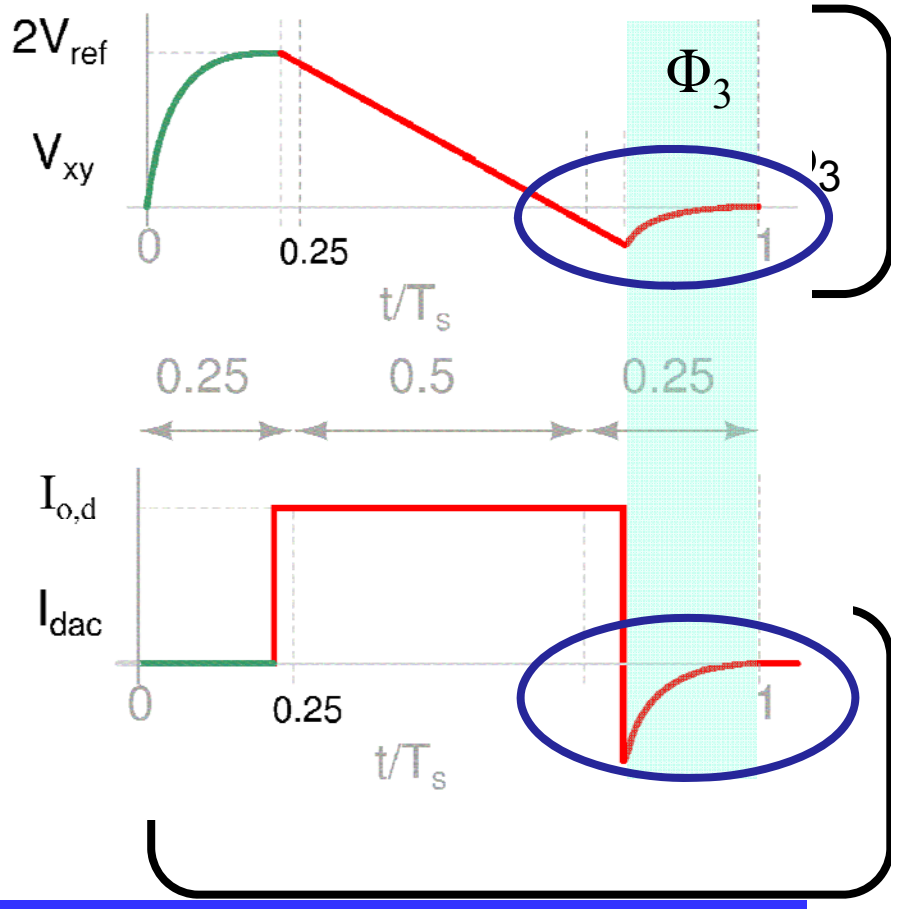
I_{dac} lasts longer than $0.5T_s$



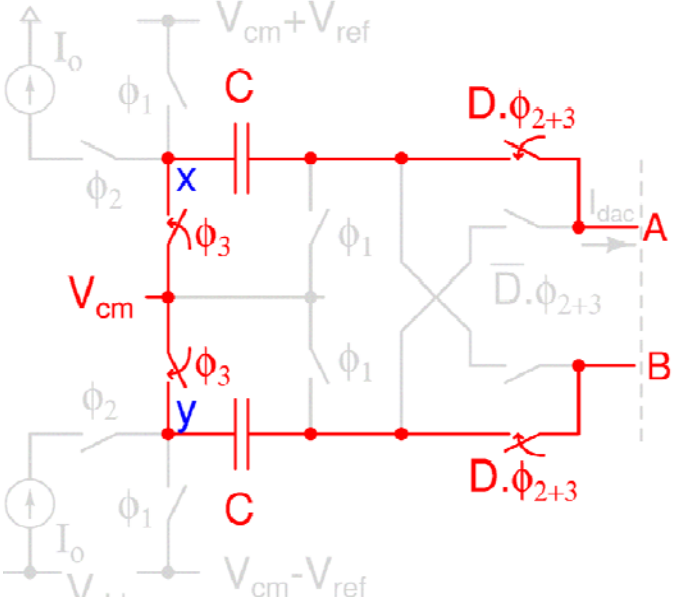
$V_{xy} < 0$ at end of ϕ_2

Waveforms (Φ_3)

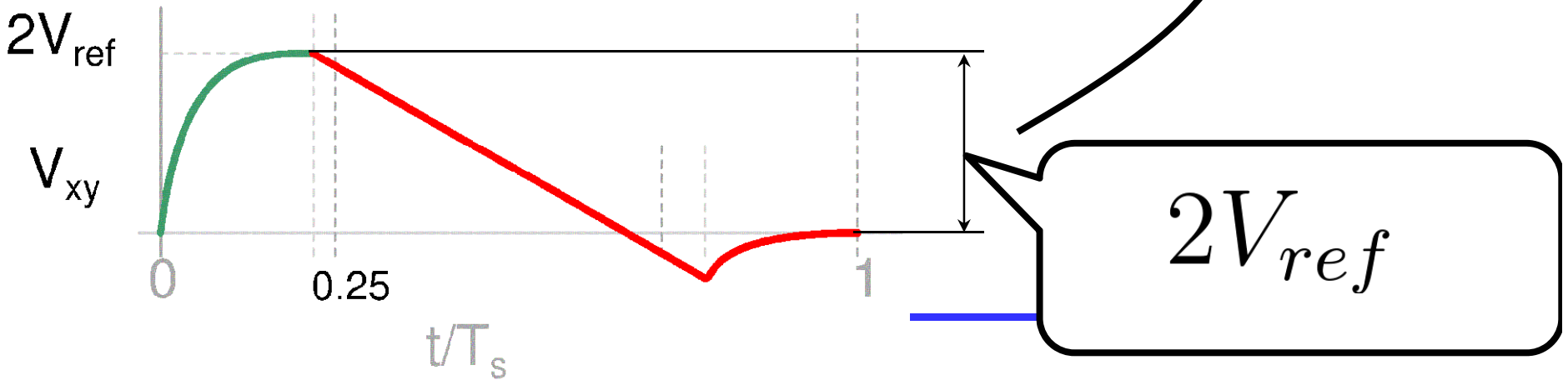




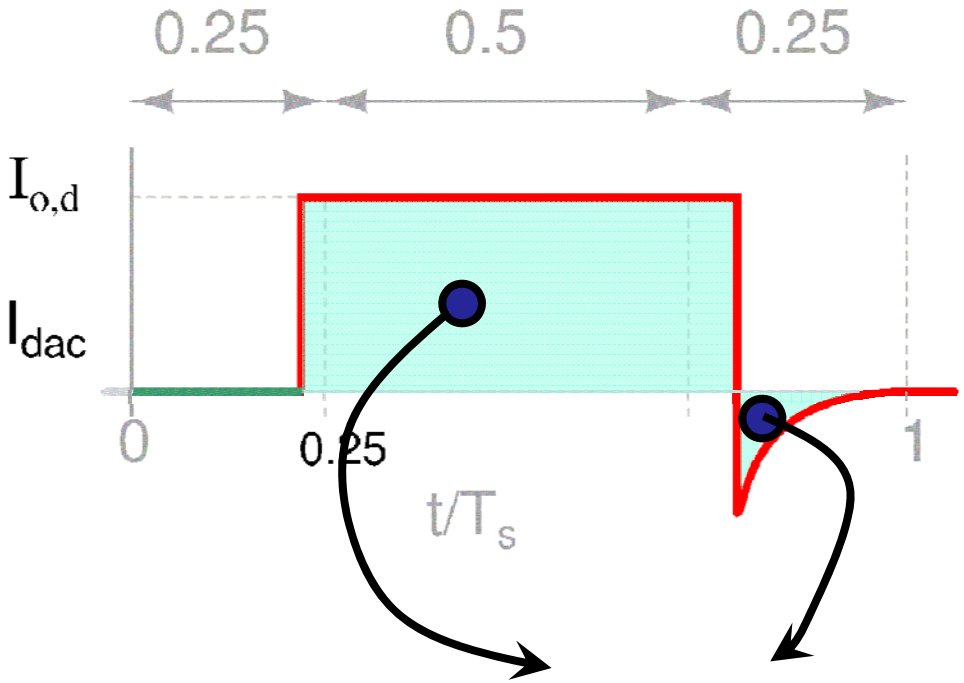
Total DAC Charge



$$Q_{dac} = C(V_{xy,initial} - V_{xy,final})$$



Total DAC Charge

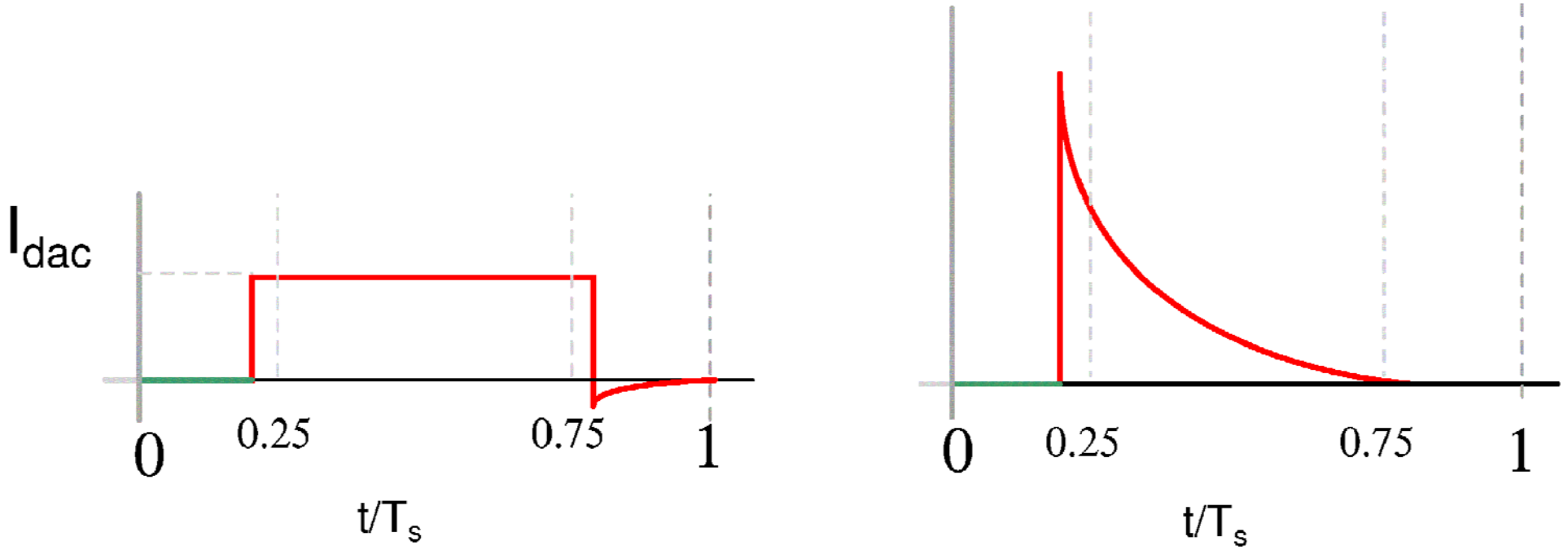


Irrespective of Jitter !

$$A_1 - A_2 = CV_{ref}$$

Role of current source

- Shapes the capacitor discharge pulse
- Smaller peak current
- Relaxed requirement - linearity of the loop filter

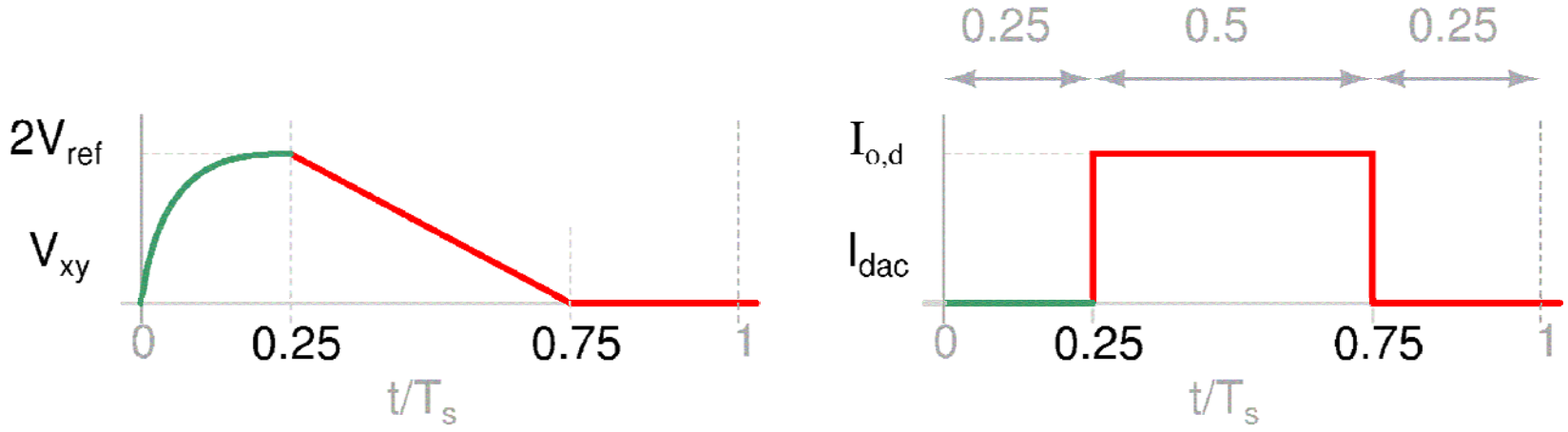


(a) SCRZ Waveform

(b) SC Waveform

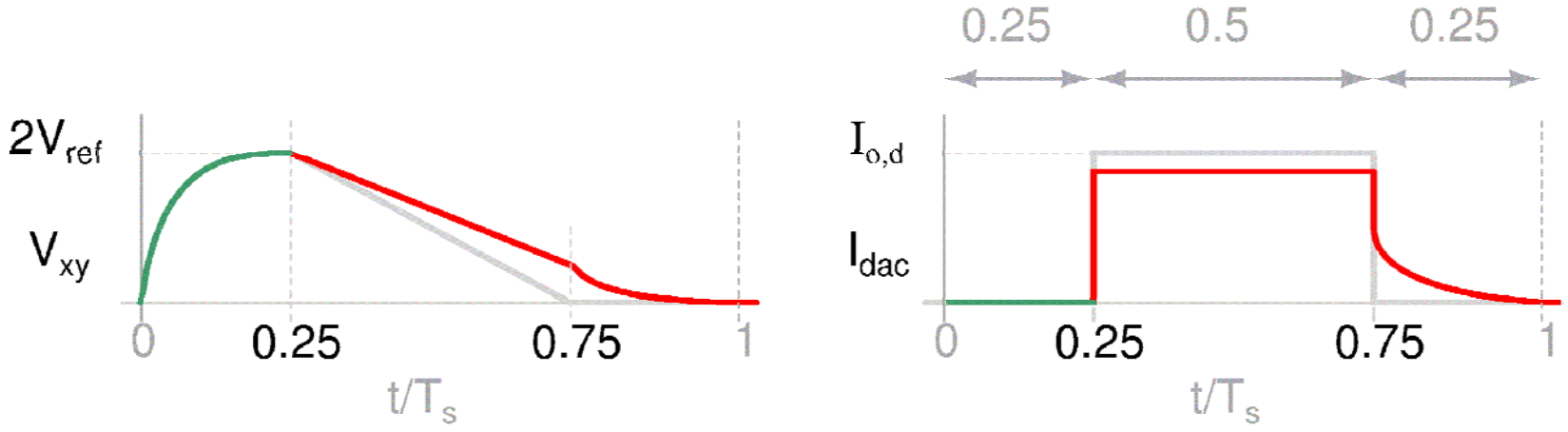
Non ideality - Deviation of $2I_o$

- $2I_o(0.5T_s) = CV_{ref}$
- $I_{o,d} = 2CV_{ref}/T_s$
- Capacitors completely discharged at the end of Φ_2
- $I_{dac} = 0$ during Φ_3



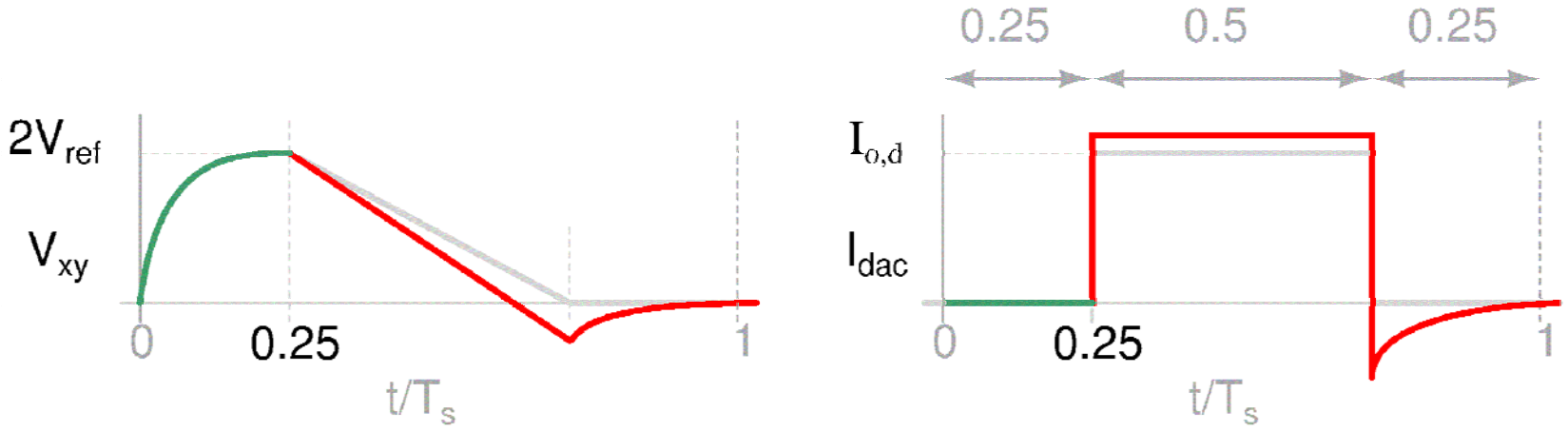
If $2I_o < I_{o,d}$

- Capacitors are incompletely discharged
- The residual charge is discharged during Φ_3
- I_{dac} is positive during Φ_3
- Net charge supplied by the DAC remains $\pm CV_{ref}$

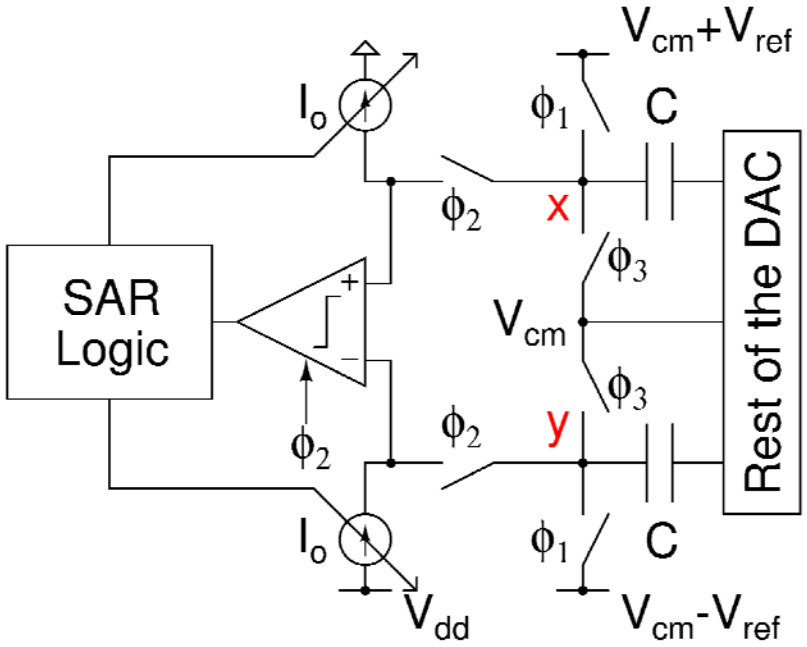


If $2I_o > I_{o,d}$

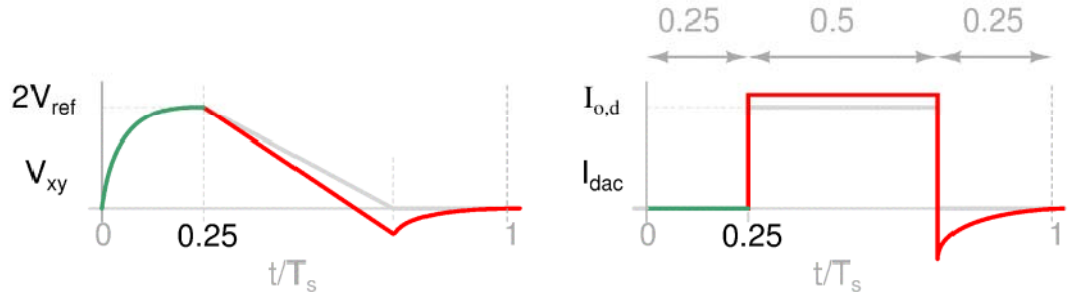
- Capacitors are over discharged
- The capacitors are charged during Φ_3
- I_{dac} is negative during Φ_3
- Net charge supplied by the DAC remains $\pm CV_{ref}$



Tune $2I_o$

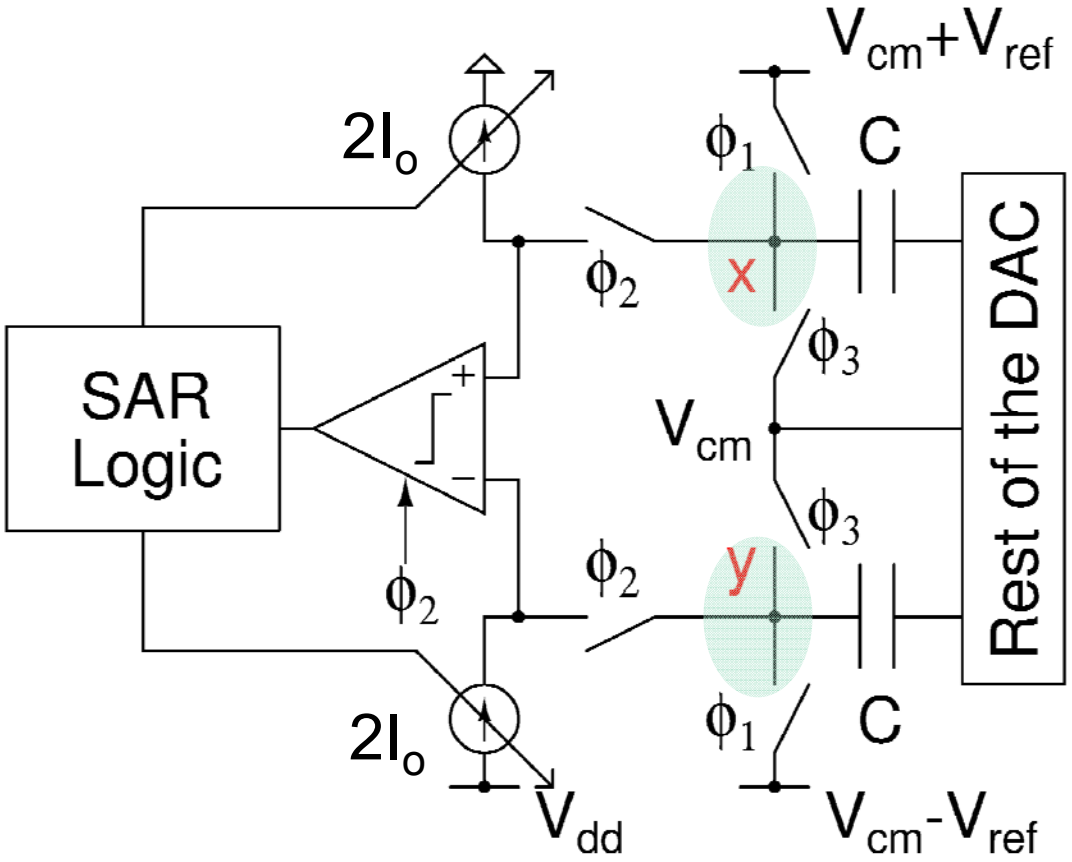


- $2I_o = I_{o,d}$, $V_{xy} = 0$
- $V_{xy} < 0$, $2I_o > I_{o,d}$

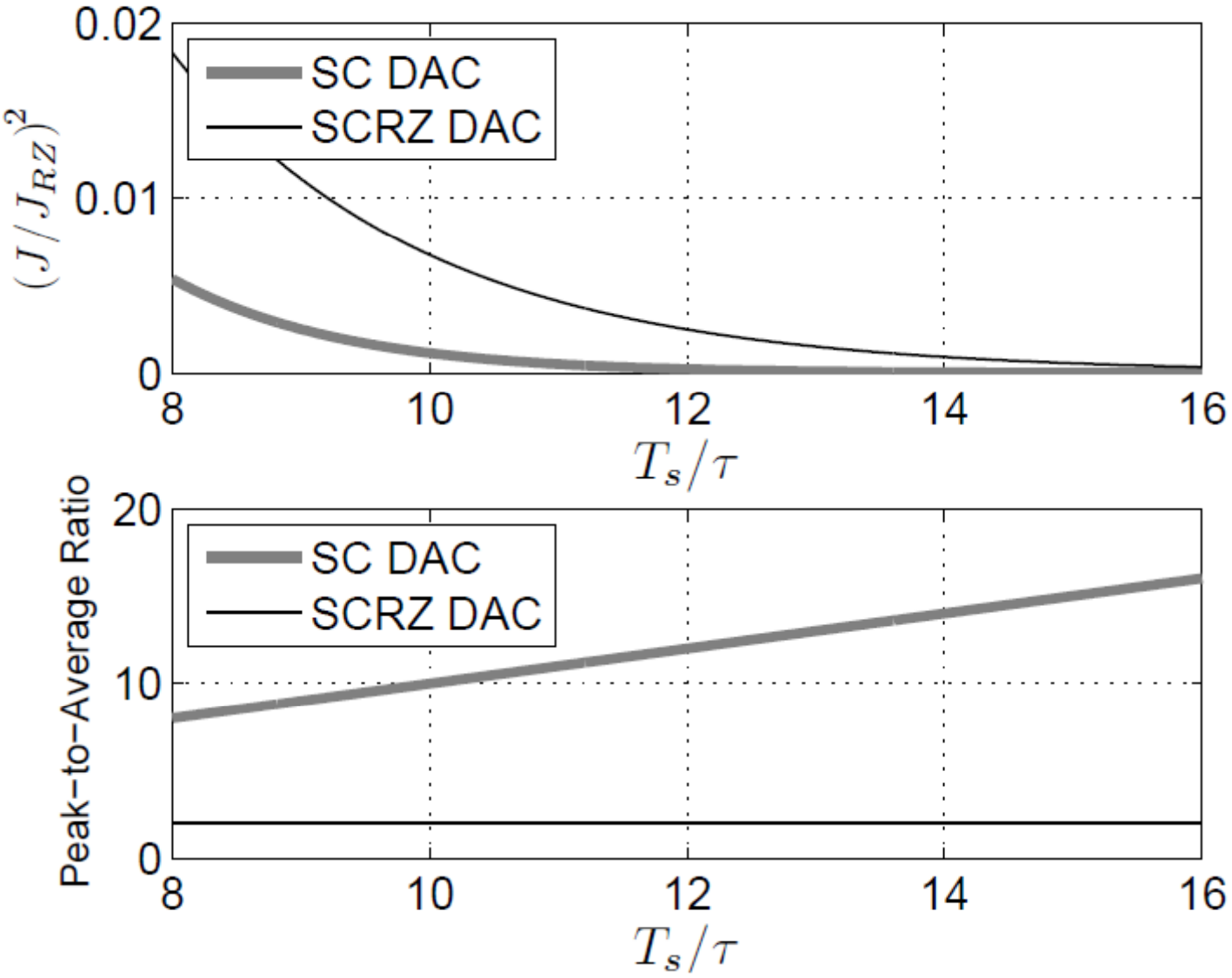


Tune $2I_o$

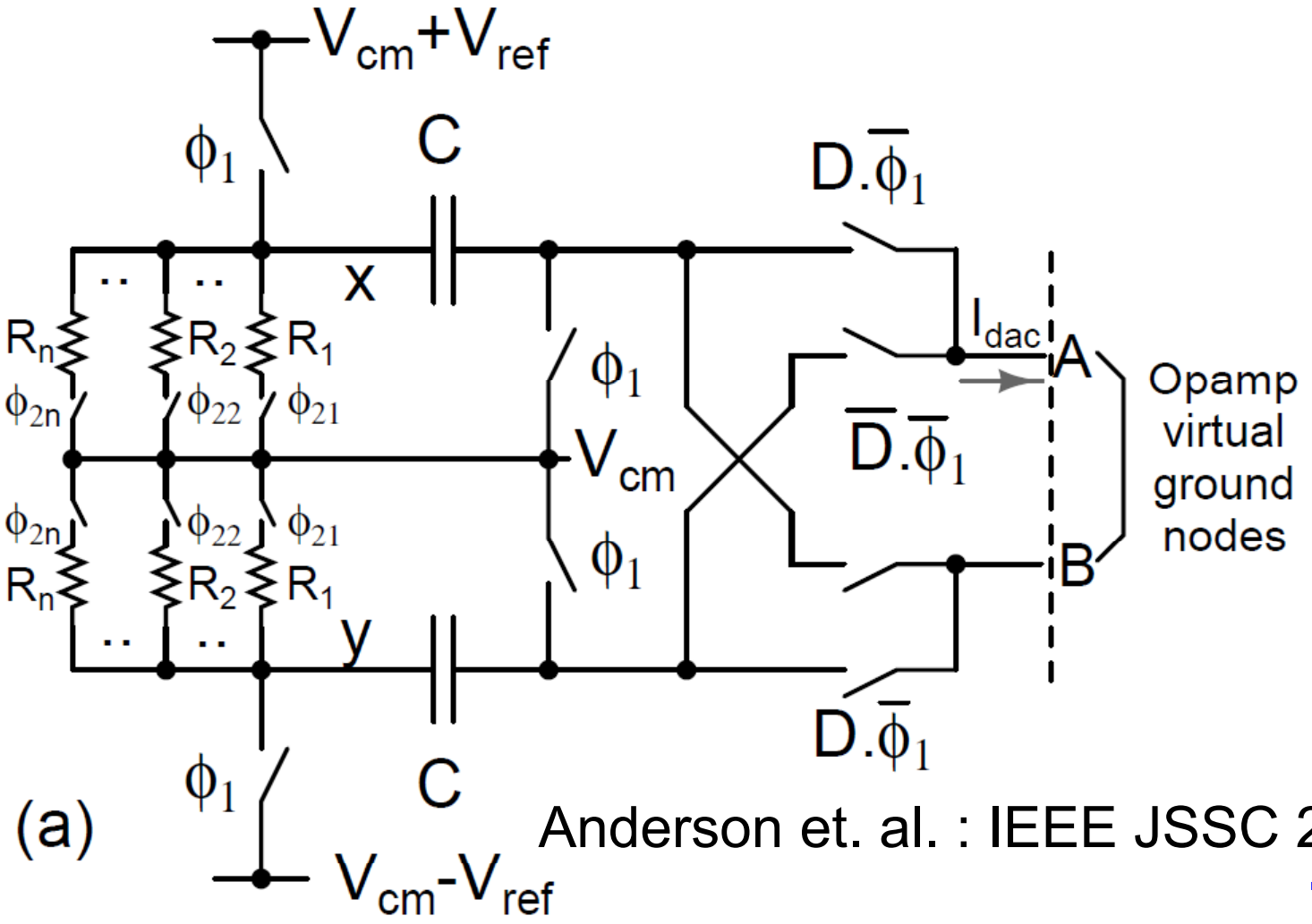
- Comparator- sign of V_{xy} at the end of Φ_2
- Control I_o to 6-bit accuracy



Compare : SC versus SCRZ DAC

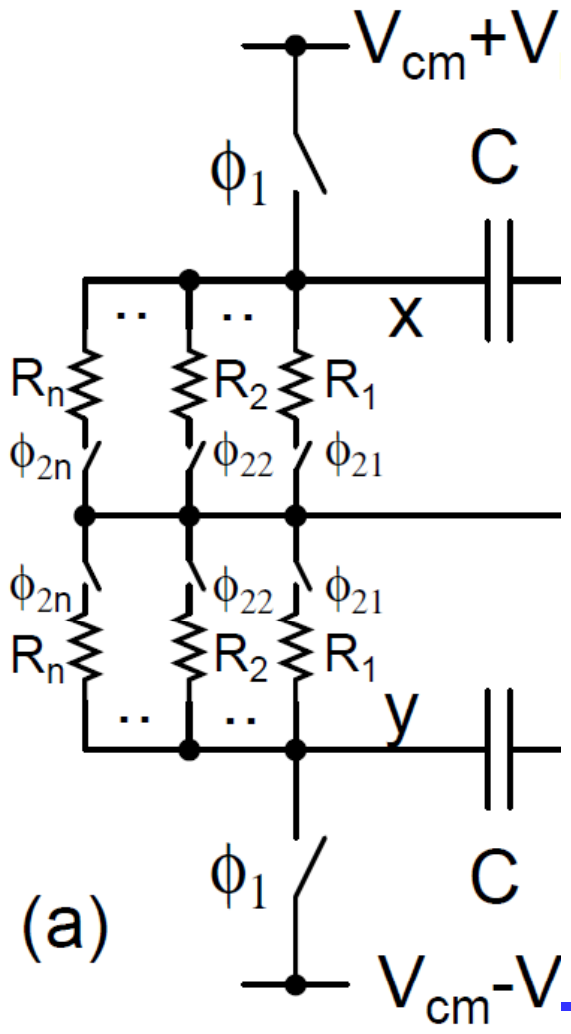


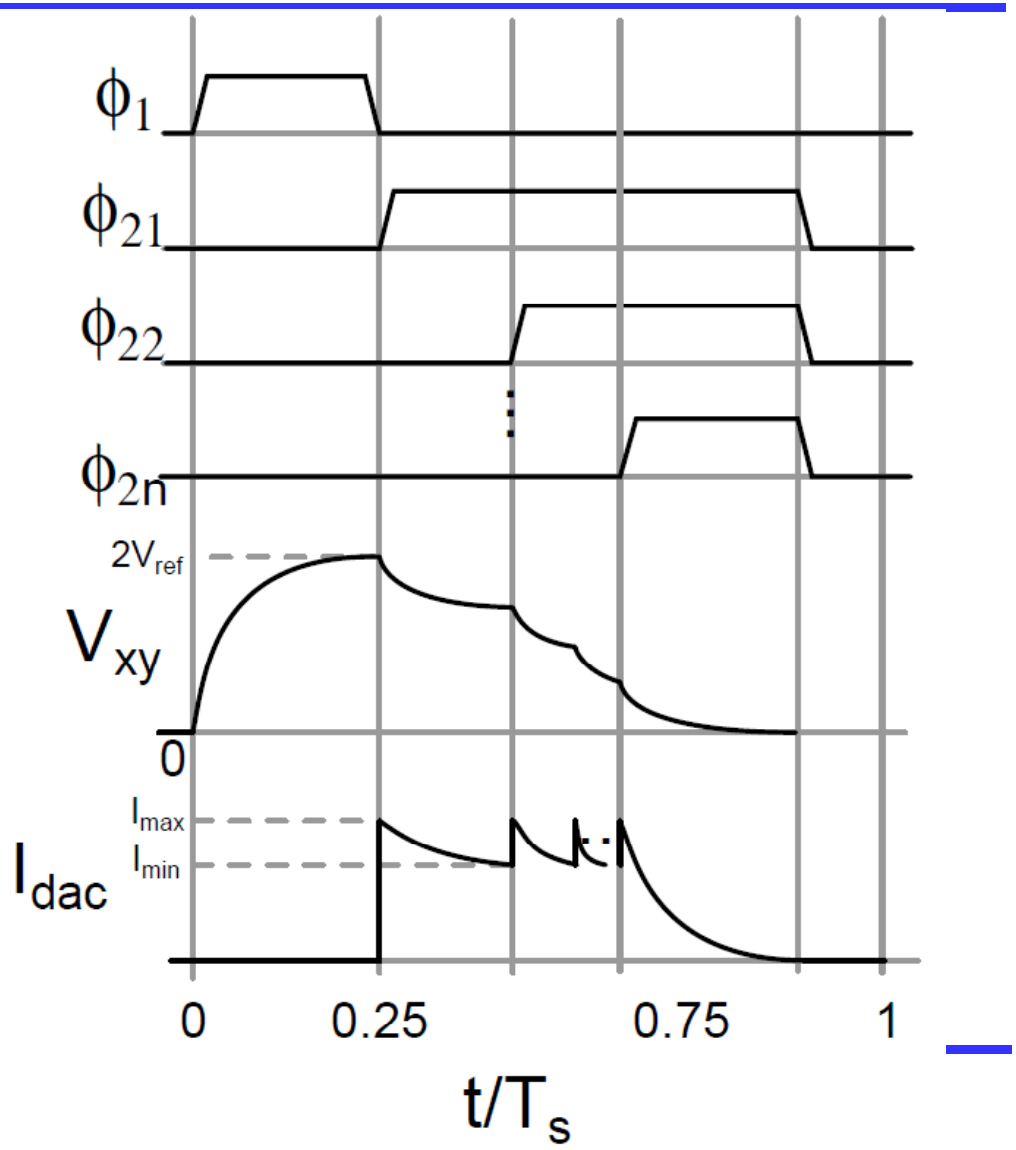
Related Work : The SCSR DAC



Anderson et. al. : IEEE JSSC 2009

Related Work : The SCSR DAC

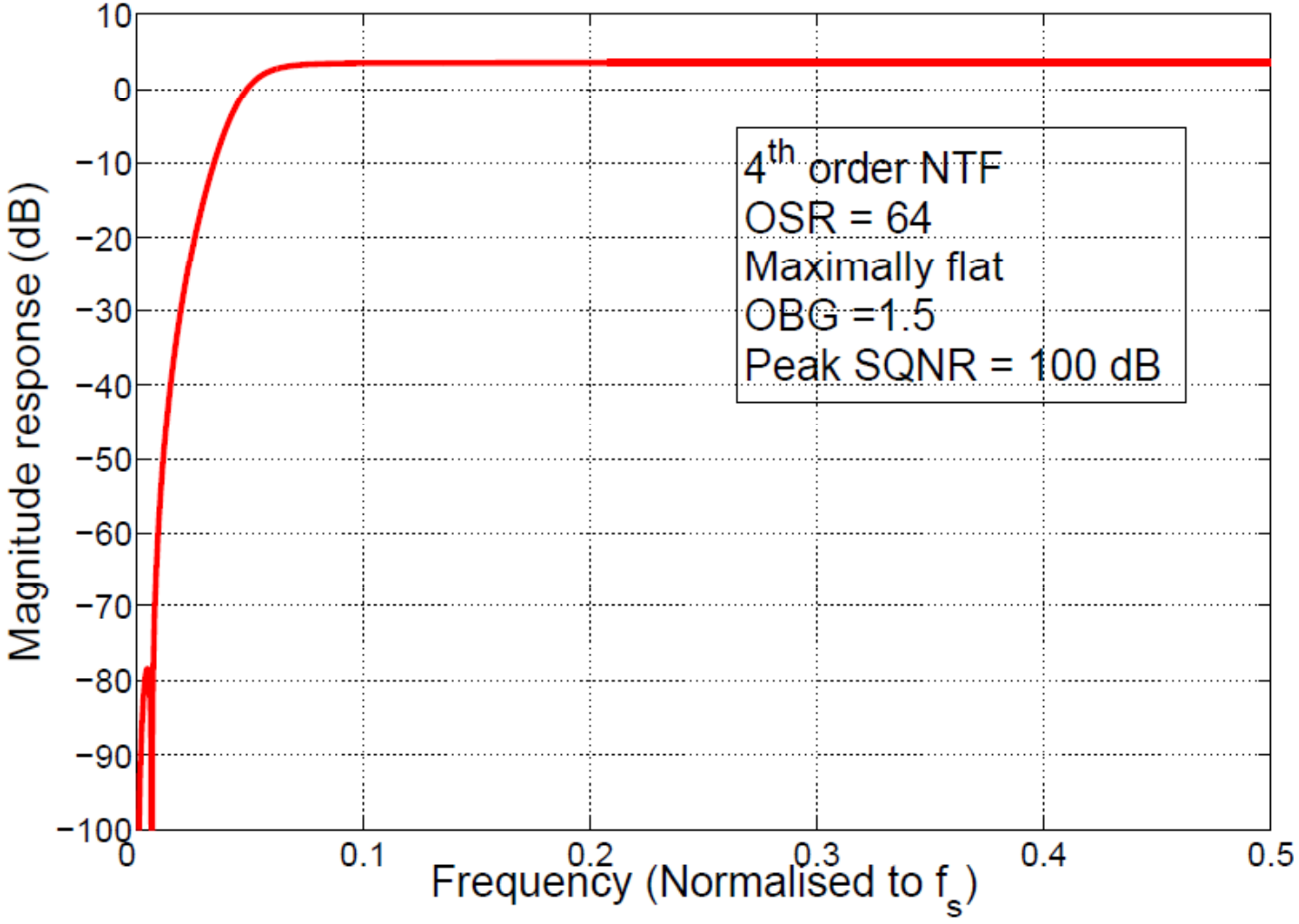




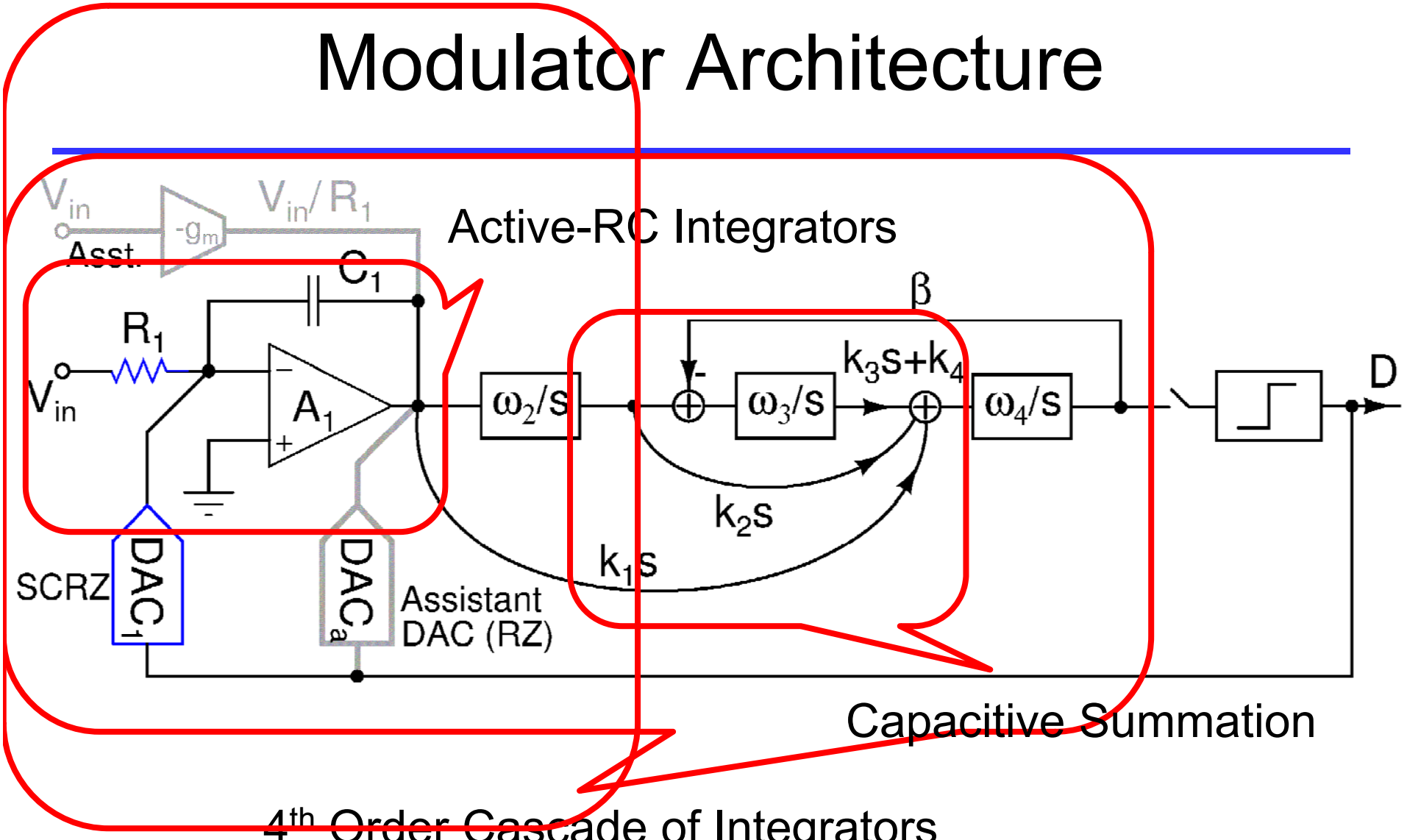
Target Modulator Specifications

- Signal Bandwidth = 2 MHz
- Sampling frequency = 256 MHz
- Quantizer range = 3.6 $V_{pp,d}$
- Target resolution = 14 Bits
- 0.18 µm CMOS process

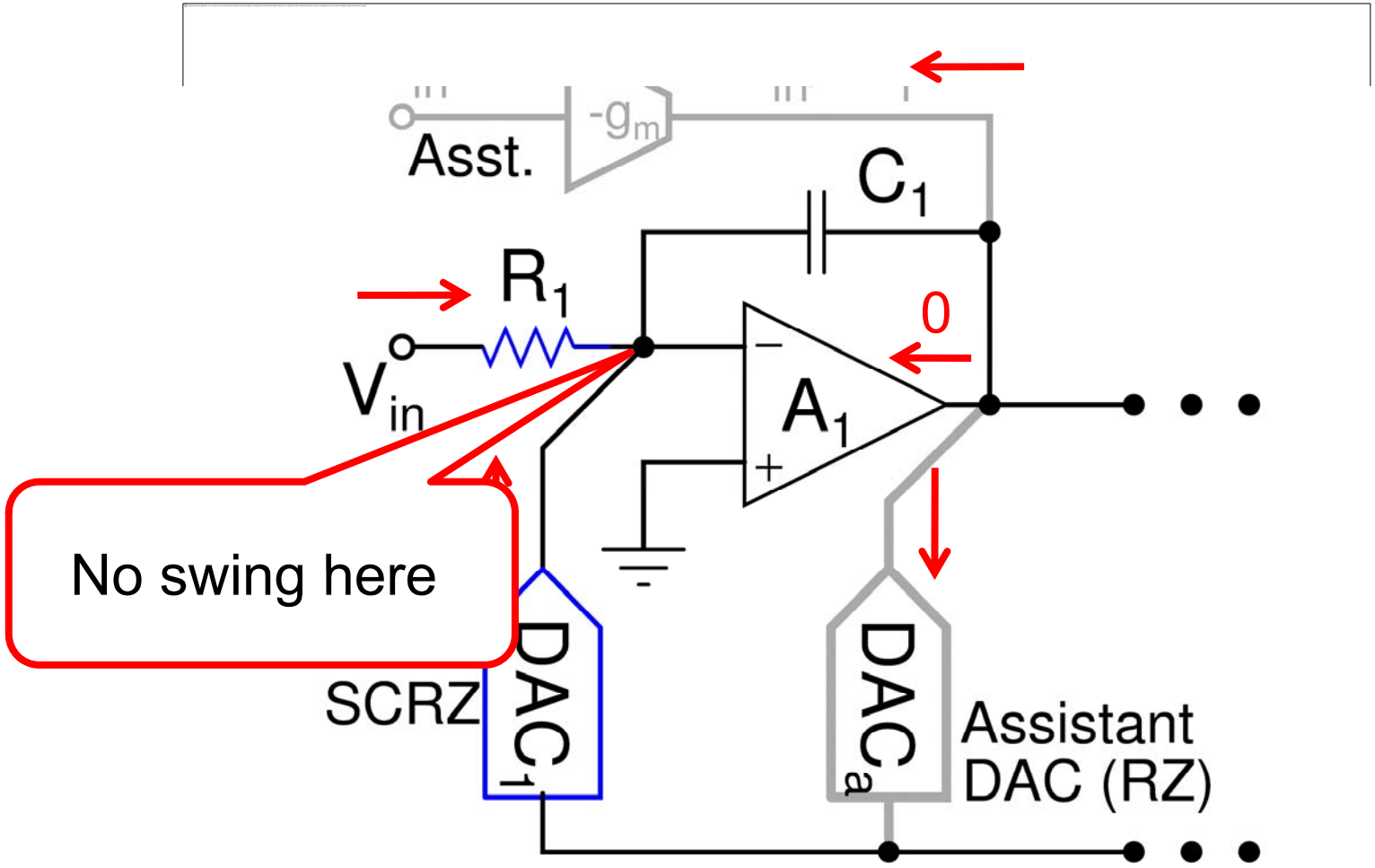
Noise Transfer Function



Modulator Architecture

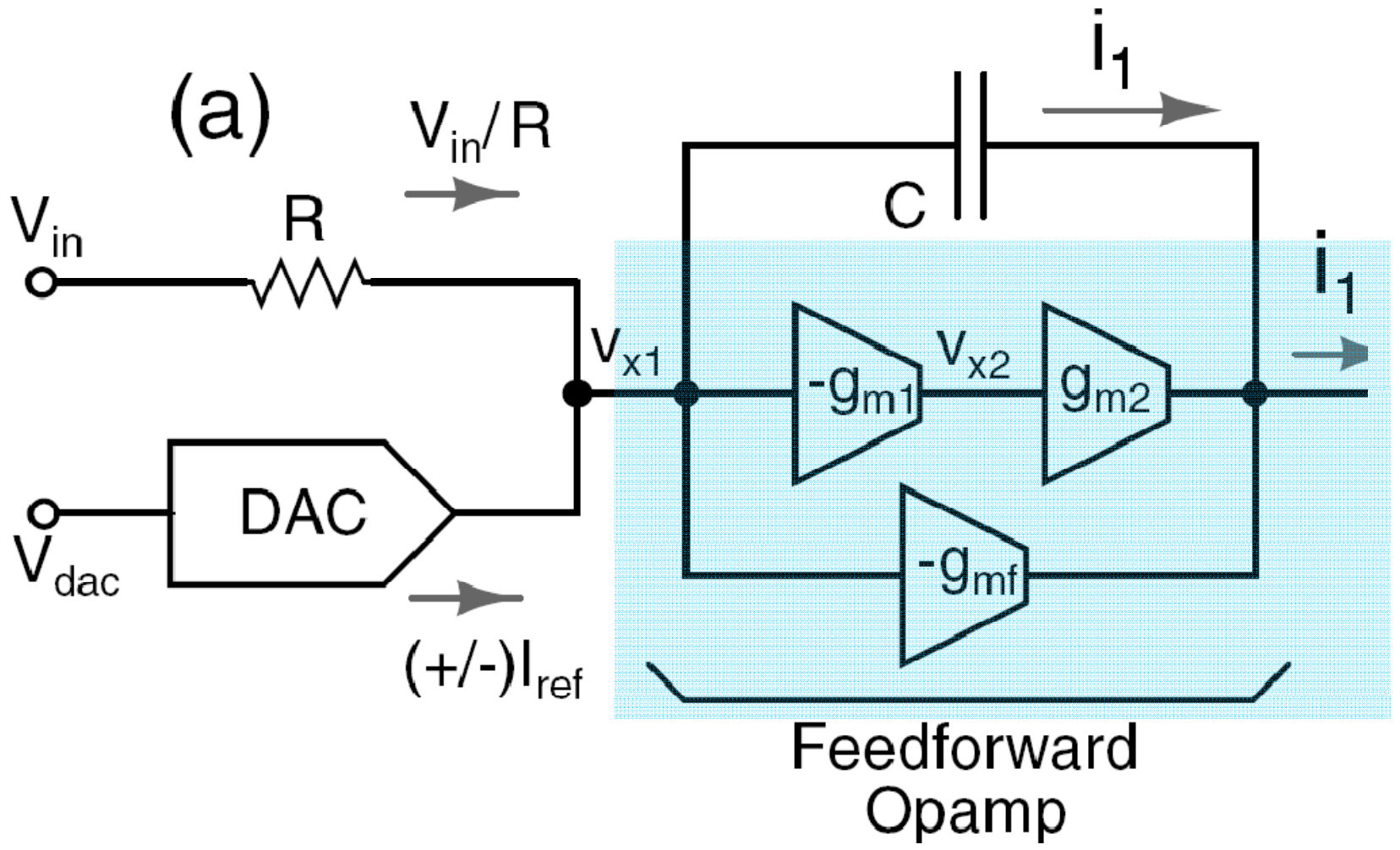


Assisted Opamp Technique

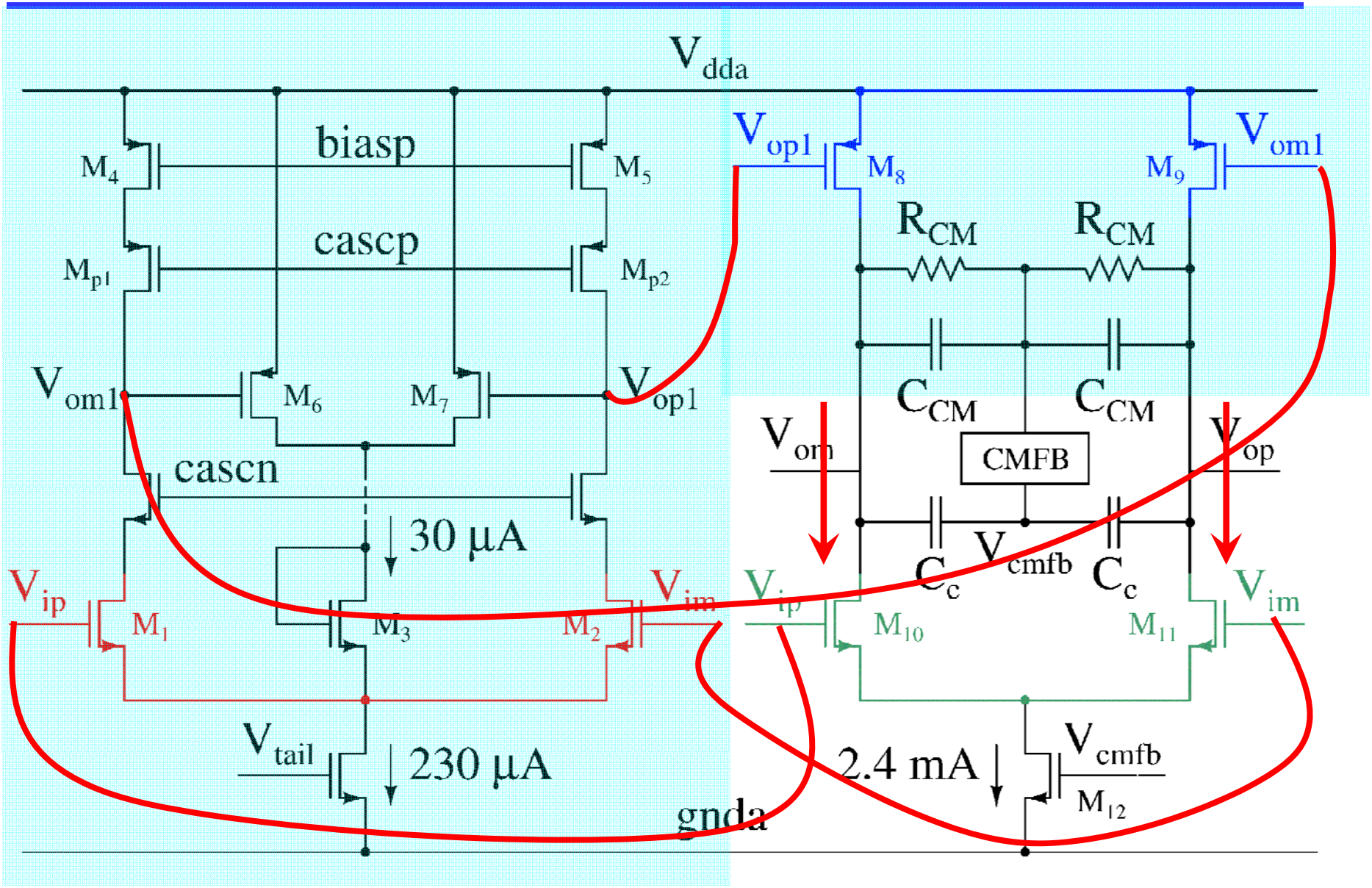


[1] S. Pavan and P. Sankar, “Power reduction in continuous-time delta sigma modulators using the assisted opamp technique,” IEEE Journal of Solid-State Circuits., vol. 45, no. 7, pp 1365-1379, July 2010

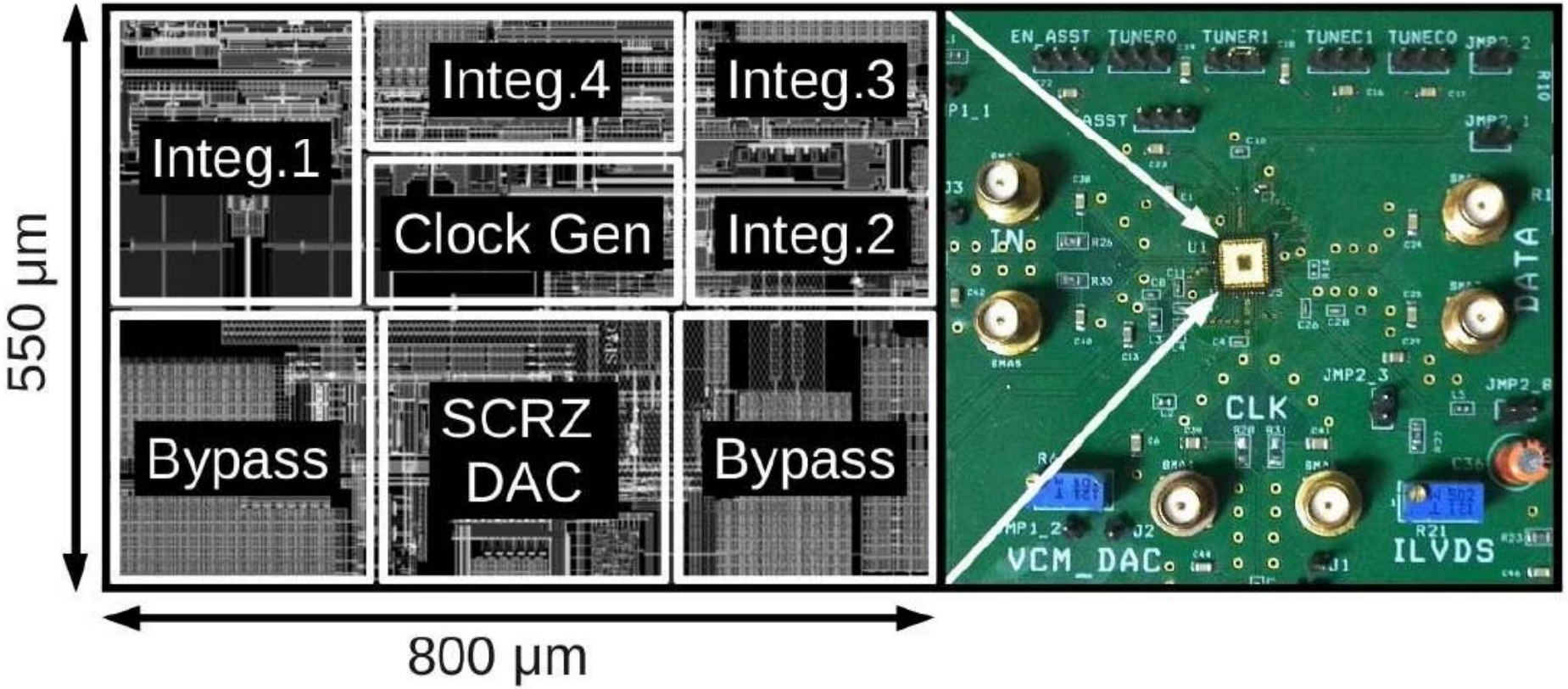
Opamp Design



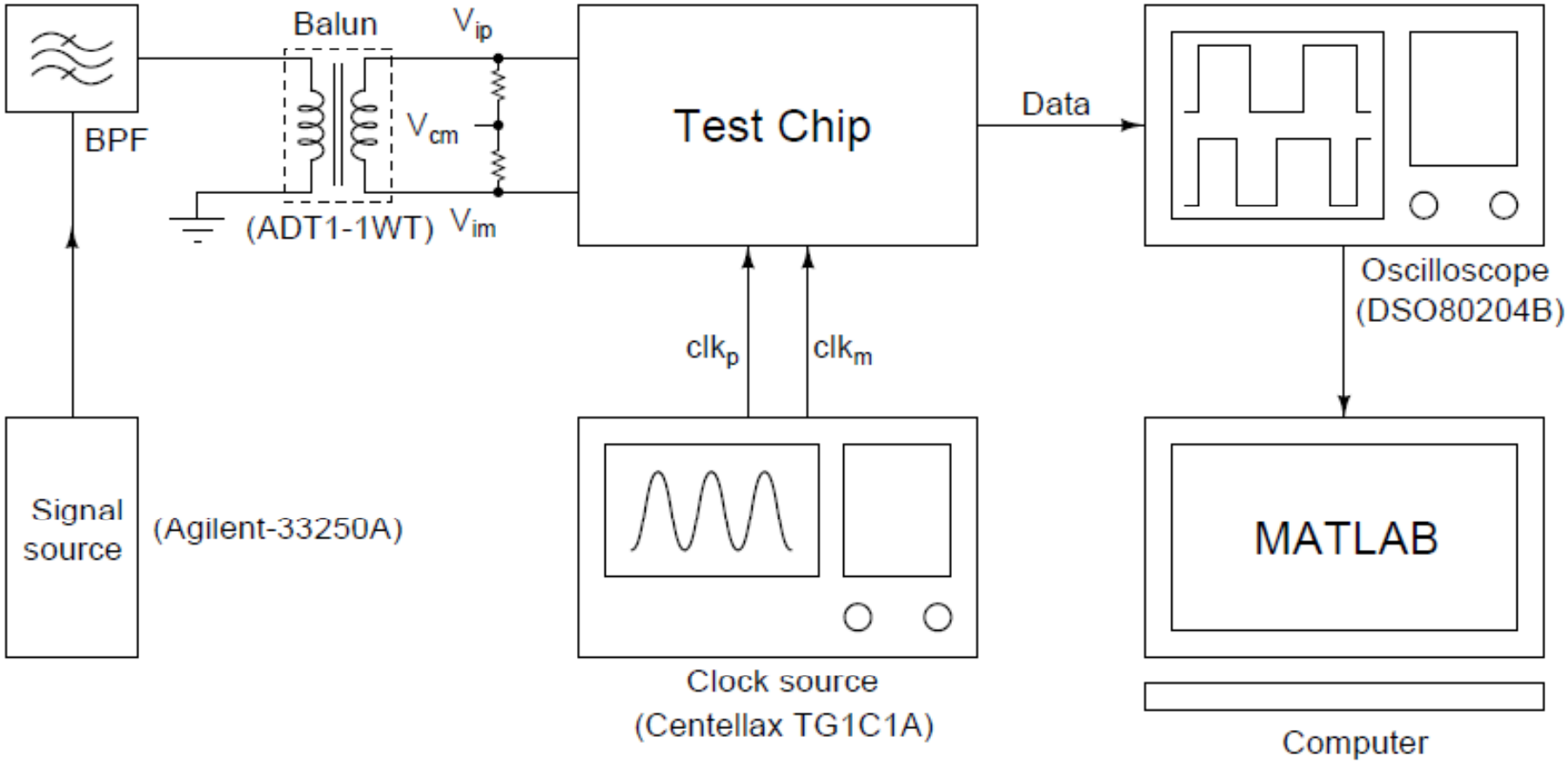
Two Stage Feedforward Compensation



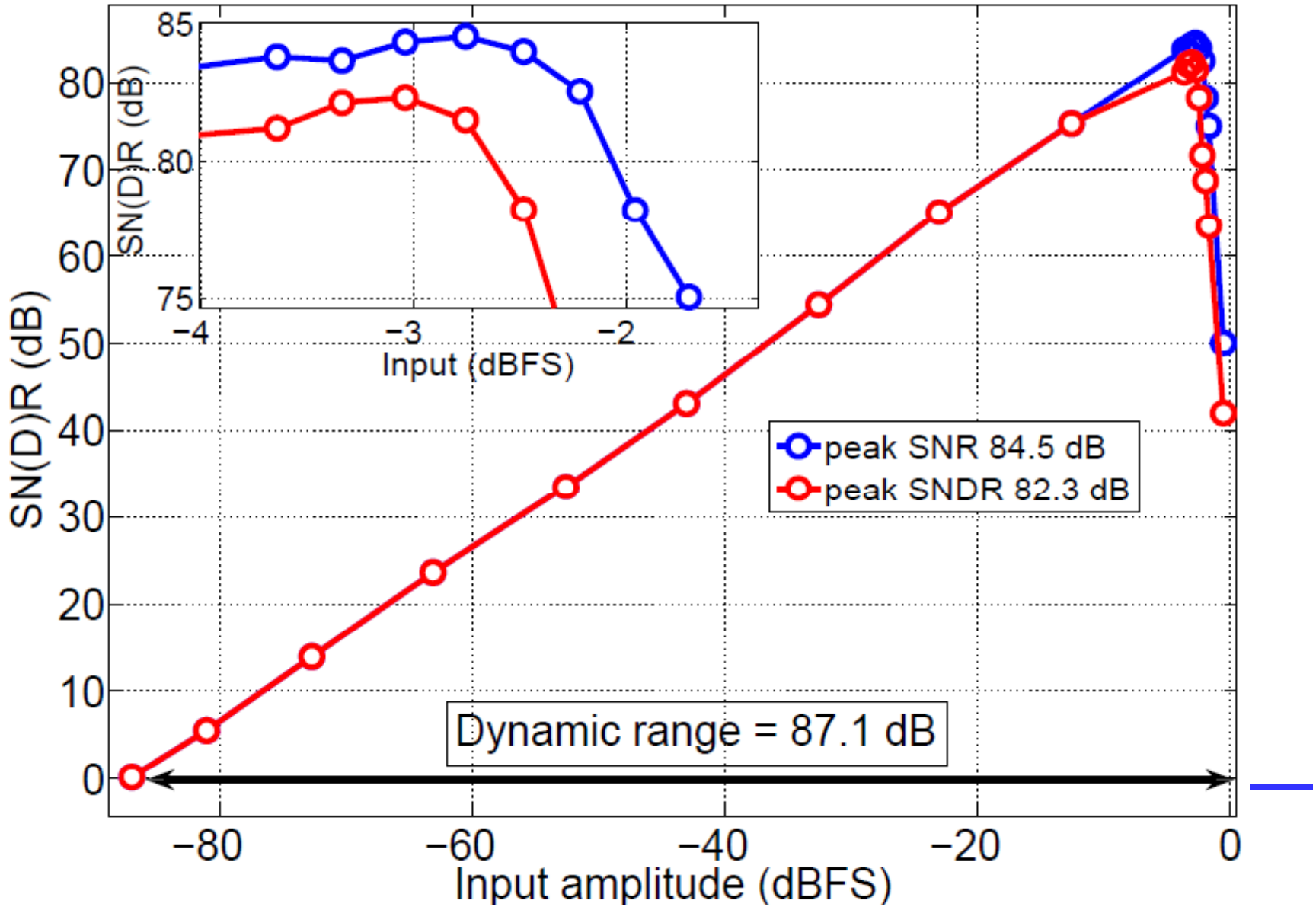
Chip layout and test board



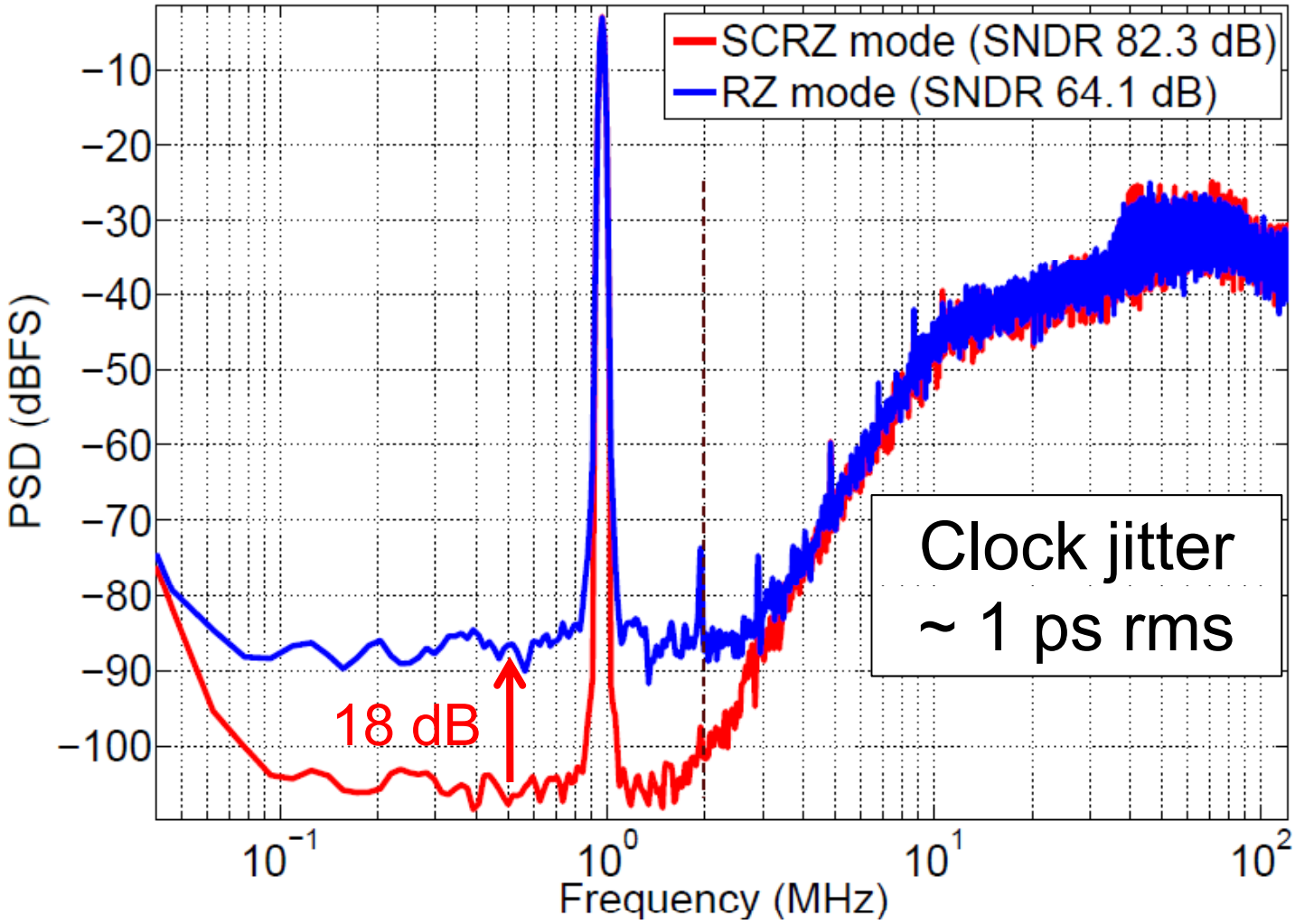
Test Setup


Balun
V_{ip}
V_{cm}
V_{im}
BPF
(ADT1-1WT)
Test Chip
Data
Oscilloscope
(DSO80204B)
clk_p
clk_m
Signal source
(Agilent-33250A)
Clock source
(Centellax TG1C1A)
MATLAB
Computer

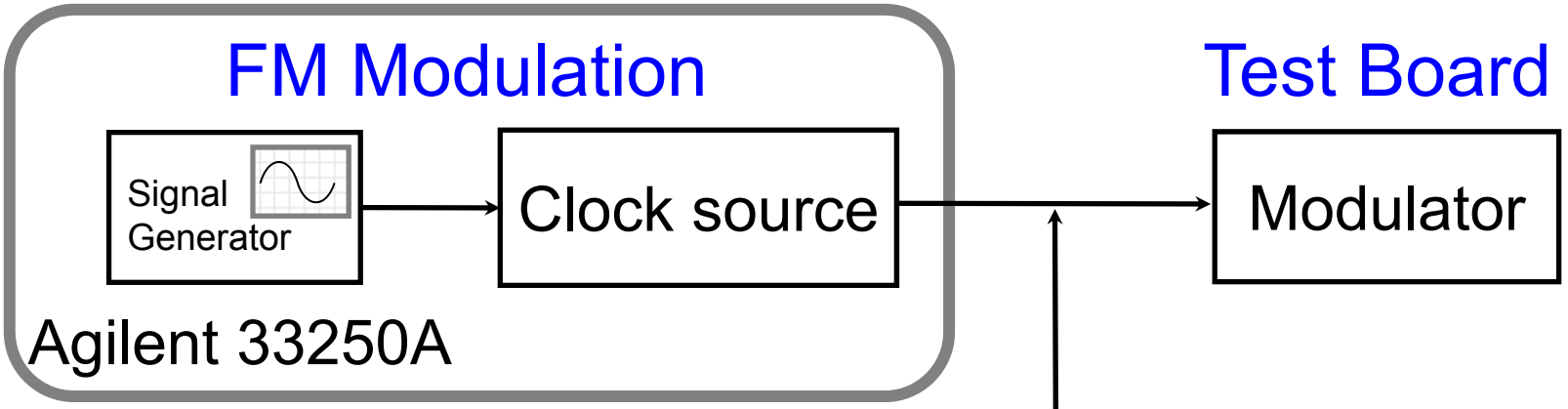
SN(D)R vs Input Amplitude



PSD of modulator



Controlled jitter experiment



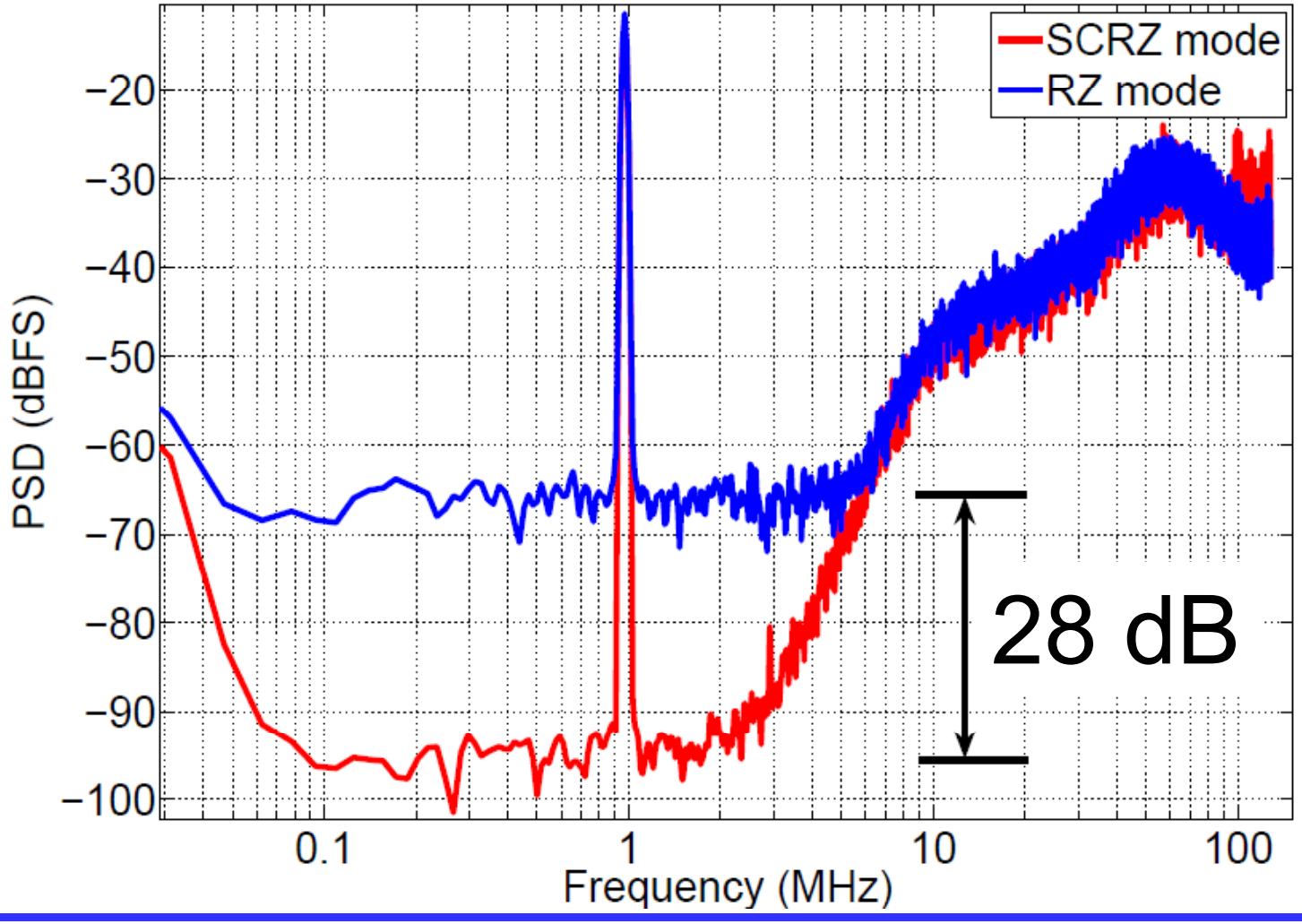
FM modulated sampling clock

$$\cos\left[2\pi f_s t + A\cos(2\pi f_m t)\right]$$

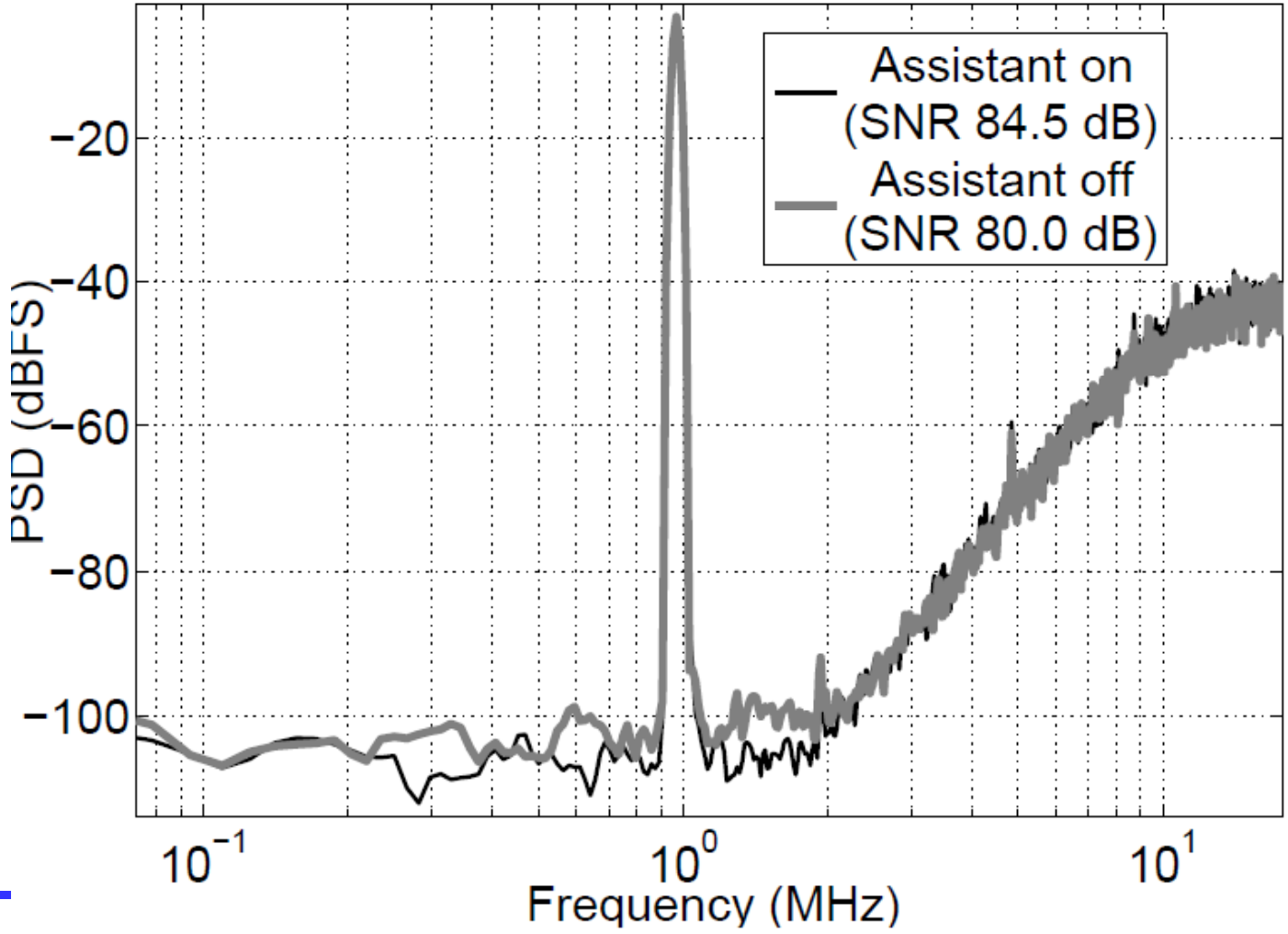
60 MHz

Chosen so that RMS jitter is 50 ps

PSD of modulator (jittery clock)



Effect of opamp assistance



Performance Summary

Signal Bandwidth / Clock Rate	2 MHz / 256 MHz
Full Scale	3.6 $V_{pp,diff}$
Input Swing for peak SNR	-2.75 dBFS
Dynamic Range/ SNR/ SNDR	87.1 dB/ 84.5 dB/ 82.3 dB
Active area	0.38 mm^2
Process / Supply Voltage	180 nm CMOS / 1.8 V
Power (including references)	16.5 mW
FoM (SNR)	300 fJ/lvl
FoM (SNDR)	387 fJ/lvl
FoM (DR)	168 dB

Comparison with other works

Reference	This Work	Anderson JSSC09	Veldho JSSC03	Gealow VLSI11	Kim VLSI11
BW (MHz)	2	1.92	1.23	1.92	1.95
DR (dB)	87	70	83	83	79
SNR (dB)	84.5	66.4	83	-	74.3
SNDR (dB)	82.3	62.4	-	78	73.3
Power (mW)	16.5	5.0	4.1	2.8	8.55
FoM_{DR} (dB)	168	156	168	171	163
FoM_{SNR}(fJ/lvl)	300	768	145	-	517
FoM_{SNDR}(fJ/lvl)	387	1218	-	110	580
Tech. (nm)	180	90	180	40	65
Supply (V)	1.8	1.2	1.8	2.4/1.4	2.5
Sampling (MHz)	256	312	76.8	245.76	124.8
Feedback DAC	SCRZ	SCSR	SCR	CT-SI	CT-SC

Conclusions

- Conventional feedback DACs have problems
  - NRZ DAC : Rise-fall asymmetry
  - RZ DAC : Jitter sensitivity
  - SC DAC : Poor linearity
- The SC-RZ DAC
  - Good marriage of the SC and RZ DACs
- A high performance CTDSM incorporating an SC-RZ DAC
  - 87 dB DR in a 2MHz bandwidth
  - 16.6mW in a 180nm CMOS process