High Voltage Devices on Scaled Technologies for RF and Power Management

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SJT Micropower

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Outline

- SJT Micropower and the SBIR program
- Silicon MESFET Overview
- High Voltage Capability
- Modeling and Measured MESFETs
- Power Management Applications
- RF Applications

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SJT Micropower Overview

Company:

- *SJT Micropower is a fabless design house based in Phoenix, AZ*
- *Startup out of Arizona State University*
- *Multiple SBIR and STTR contracts awarded in past 4 years (~$3M)*

Technology:

- Patented high voltage MESFETs which can be fabricated on SOI CMOS with **no additional cost**

Status:

- Devices taped out down to 45nm
- Technology has been demonstrated at multiple foundries on both partially and fully depleted SOI and on both SOI and SOS
- Cutoff Frequency ~40GHz on 150nm technology, suitable for RF

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SBIR Funding

Small Business Innovative Research:

Each year, Federal agencies with extramural research and development (R&D) budgets that exceed $100 million are required to allocate 2.5 percent of their R&D budget to these programs. Currently, eleven Federal agencies participate in the program:

Three Phase Program:

- ***Phase I.*** The objective of Phase I is to establish the technical merit, feasibility, and commercial potential of the proposed R/R&D efforts $150,000 total costs for 6 months.
- ***Phase II.*** The objective of Phase II is to continue the R/R&D efforts initiated in Phase I. $1,000,000 total costs for 2 years.
- ***Phase III.*** The objective of Phase III, where appropriate, is for the small business to pursue commercialization objectives resulting from the Phase I/II R/R&D activities. The SBIR program does not fund Phase III

http://www.sbir.gov/

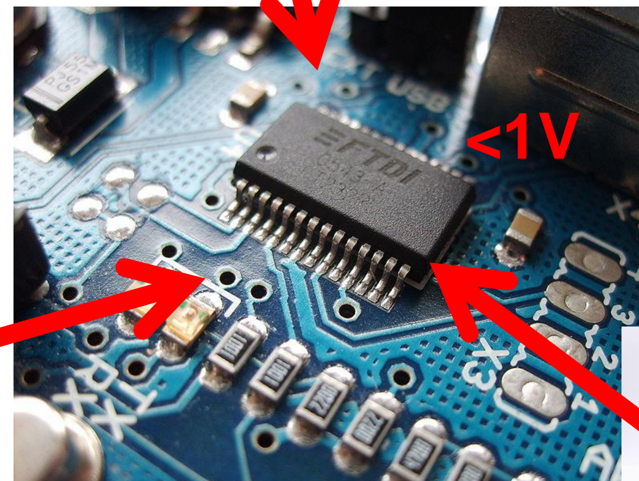
The Problem with CMOS

The Problem

Existing Scaled Transistors are Low Voltage <1V

How do you connect these common items to new chips?

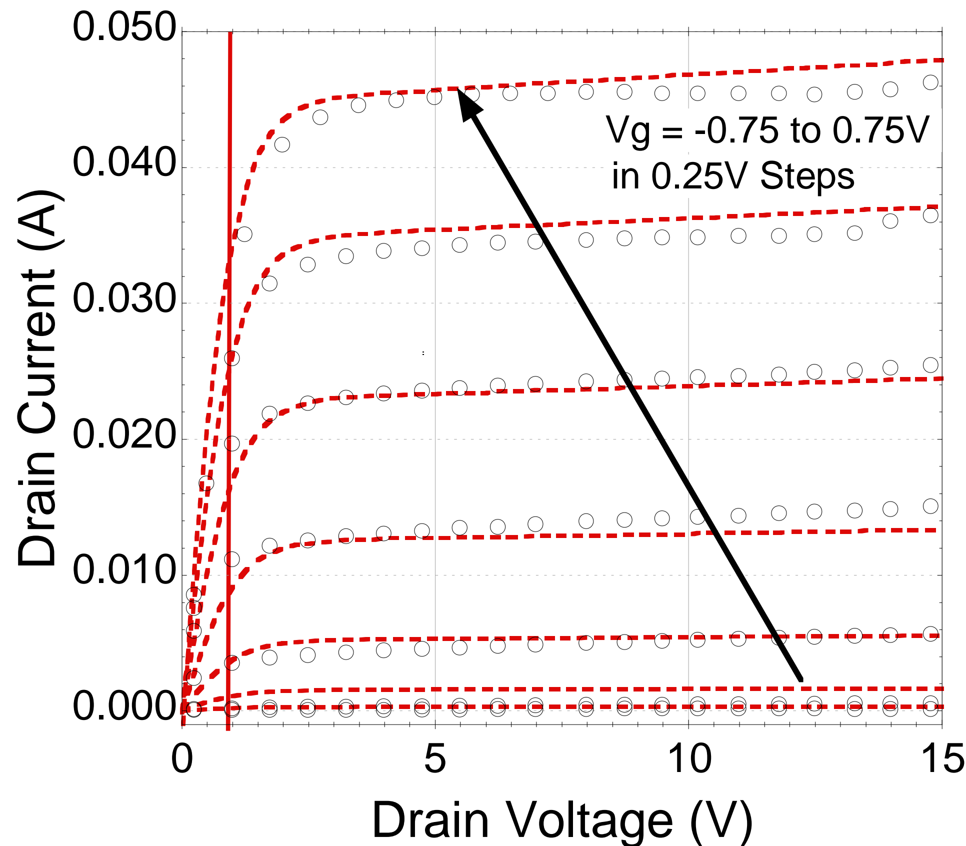
How do you make these common items work with new chips?



High Voltage on Low Voltage CMOS

Device fabricated on a 45nm process where CMOS limited to ~1V drain voltage

No changes required to the CMOS Process Flow



ASU/SJT Micropower Si-MESFET Milestones

- Successful at 5 different foundries & 6 CMOS processes (45nm – 800nm) without **changing any of the process flow**
- IBM, Honeywell, Peregrine, SPAWAR, MIT Lincoln Labs
- Highest breakdown 55 V (350nm PD-SOI CMOS)
- Peak f_T ~ 45 GHz (150nm PD-SOI CMOS)
- Peak f_{max} > 55 GHz (45nm PD-SOI CMOS)
- Have developed calibrated TOM3 and VerilogA models
- MESFETs based circuits that we have designed and tested:
  - LNA, LDO, Buck Regulator, PA, Polar Modulated PA, opamp, and voltage reference

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Technology Benefits

Easy to Implement with existing SOI CMOS

- No additional cost to use technology
- Existing CMOS already has steps required to fabricate device

Helps combat obsolescence

- Use existing, older technology high voltage parts with modern low voltage digital CMOS
- Use Existing 5V supply rails
- Conversion of voltages on chip

Extreme Environment

- High Temperature
- Radiation Hardened, Schottky interface is less susceptible to radiation induced damage than MOSFET metal-oxide-semiconductor interface

Simpler RF PA Development

- Larger voltage swing allows higher power and easier, more efficient matching to 50Ω

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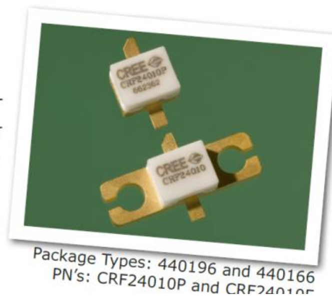
MESFET: Metal Semiconductor Field Effect Transistor

More common to have SiC or GaAs but a MESFET can be Silicon as well

CRF24010

10 W, SiC RF Power MESFET

Cree's CRF24010 is an unmatched silicon carbide (SiC) RF power Metal-Semiconductor Field-Effect Transistor (MESFET). SiC has superior properties compared to silicon or gallium arsenide, including higher breakdown voltage, higher saturated electron drift velocity, and higher thermal conductivity. SiC MESFETs offer greater efficiency, greater power density, and wider bandwidths compared to Si and GaAs transistors.



Package Types: 440196 and 440166
PN's: CRF24010P and CRF24010F

FH101

High Dynamic Range FET

Product Features

- 50 – 4000 MHz
- 18 dB Gain
- +18 dBm P1dB
- +36 dBm OIP3
- Low Noise Figure
- Single or Dual Supply Operation
- MTTF > 100 years
- Lead free/green/RoHS-compliant SOT-89 Package

Applications

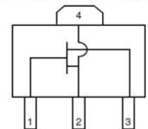
- Mobile Infrastructure
- CATV / DBS
- WLAN / ISM
- Defense / Homeland Security

Product Description

The FH101 is a high dynamic range FET packaged in a low-cost surface-mount package. The combination of low noise figure and high output IP3 at the same bias point makes it ideal for receiver and transmitter applications. The device combines dependable performance with superb quality to maintain MTTF values exceeding 100 years at mounting temperatures of +85°C. The FH101 is available in the environmentally friendly lead-free/green/RoHS-compliant SOT-89 package.

The device utilizes a high reliability GaAs MESFET technology and is targeted for applications where high linearity is required. It is well suited for various current and next generation wireless technologies such as GPRS, GSM, CDMA, and W-CDMA. In addition, the FH101 will work for other applications within the 50 to 4000 MHz frequency range such as fixed wireless.

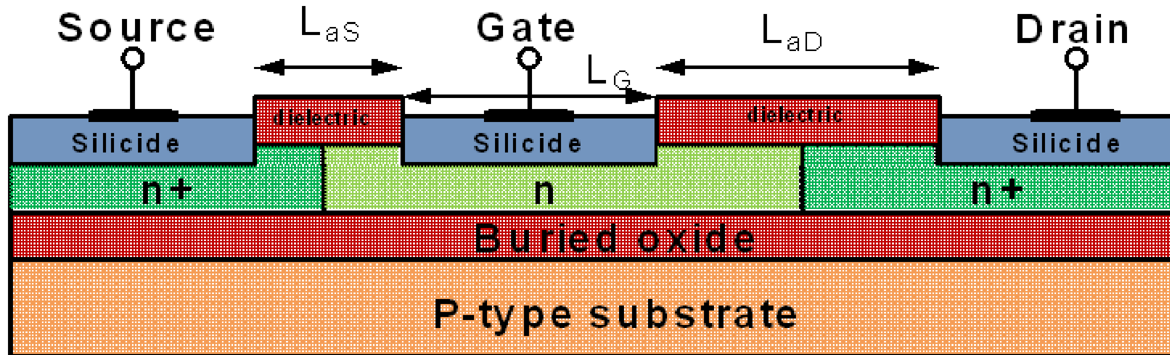
Functional Diagram



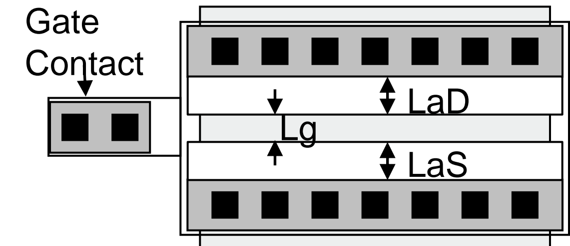
Function	Pin No.
Gate	1
Drain	3
Source	2, 4

Si-MESFET Structure and Background

Cross-Sectional View



Top View



- Majority carrier device—does not suffer from floating body effects
- Schottky gate created by a silicided contact on lightly doped n-well
- Controlled by vertically depleting the channel
- Depletion Mode—Vt is usually in the range of -0.5V to -1V
- Gate Length (Lg) is limited by the separation of the oxide spacers
  - Typically contact the gate outside of LaS & LaD to shorten Lg
- Can size LaS and LaD to give optimal RF performance and breakdown

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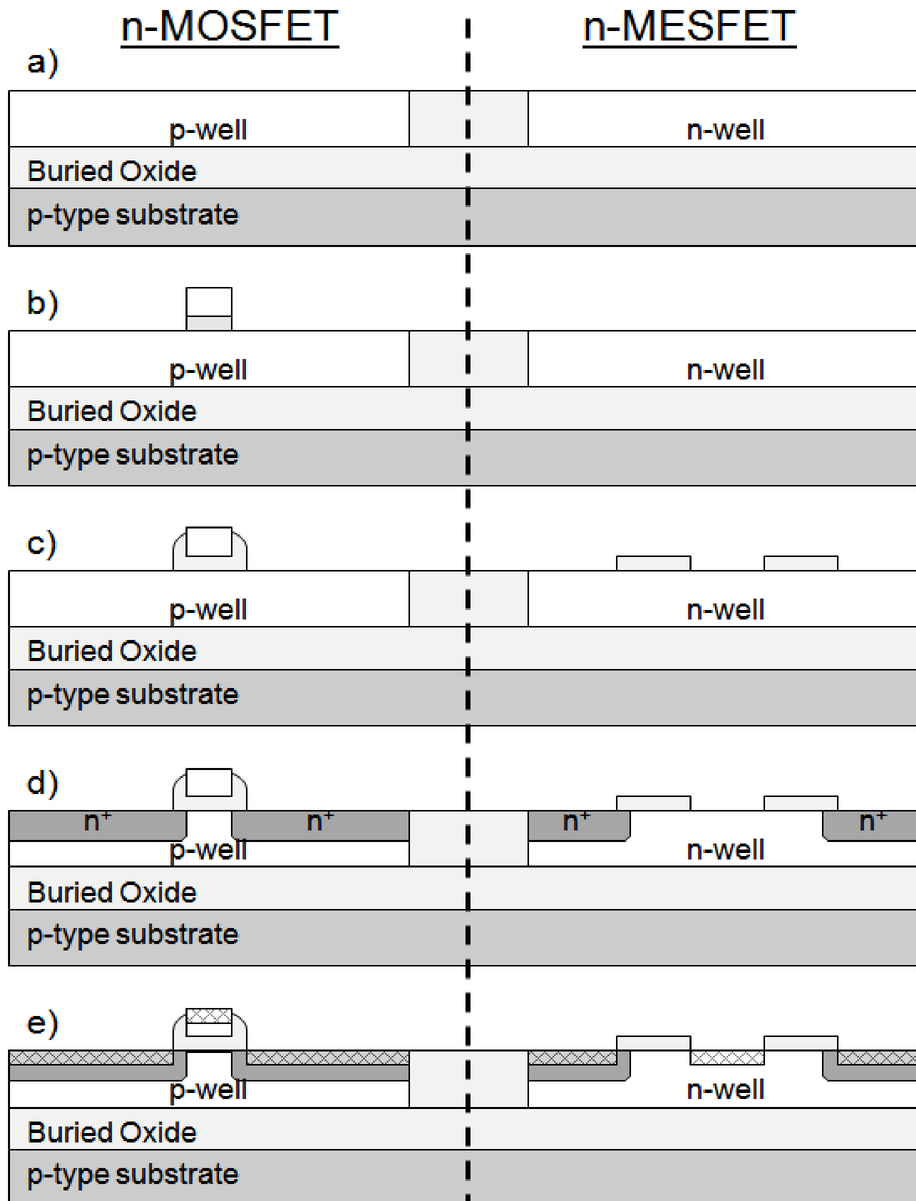
Fabrication: n-MOSFETs vs.n-MESFETs



a) Fabrication steps are the same through the LOCOS step

b) MOS gate is defined

c) SB used to pattern the oxide spacers of a MOSFET is used to define the gate length of the MESFET

d) Source/drain implant step is same for the MOSFET & MESFET.

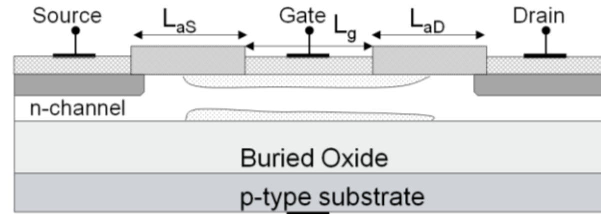
e) $CoSi_2$ salicide used to form the low-resistance contacts is used to form a Schottky contact over the lightly doped channel

***Back-end processing steps same as SOI/SOS CMOS

Cross-Section MESFETs

Regions of Operation

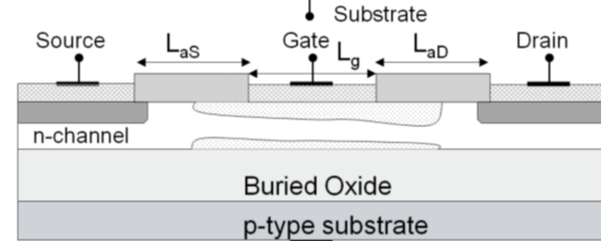
$V_{GS} = 0$ V & $V_{DS} = 0$ V

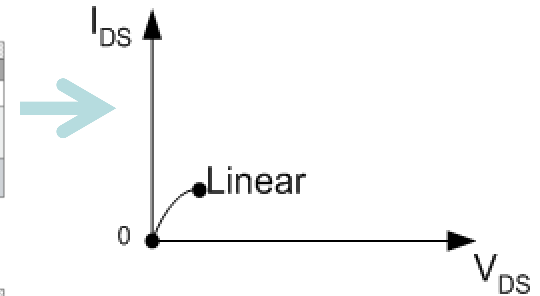


*Note: Due to the relatively thin buried oxide layer, a depletion region controlled by V_{BS} will form at the bottom interface

Linear Region:

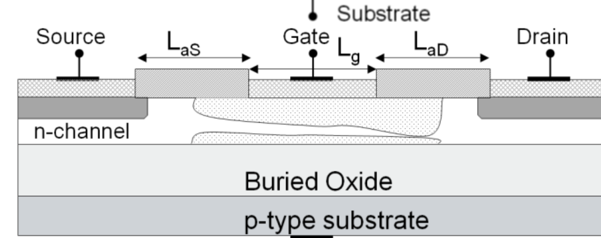
$V_{GS} = 0$ V & small V_{DS}

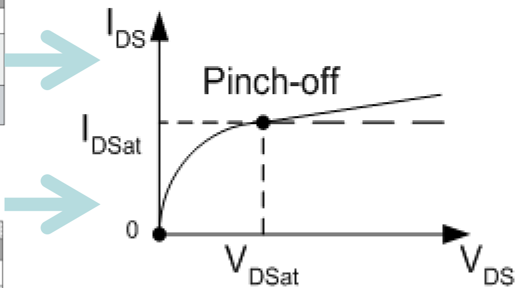




Pinch-off:

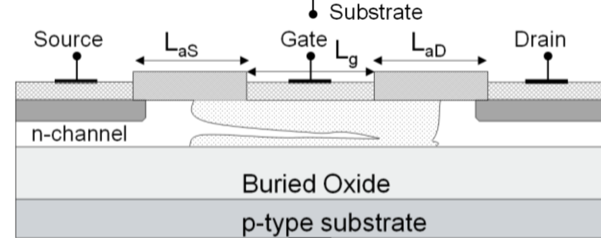
$V_{GS} = 0$ V & $V_{DS} = V_{DSAT}$





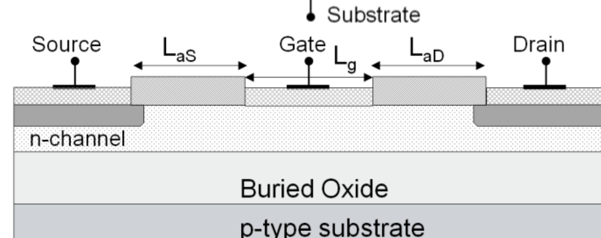
Saturation Region:

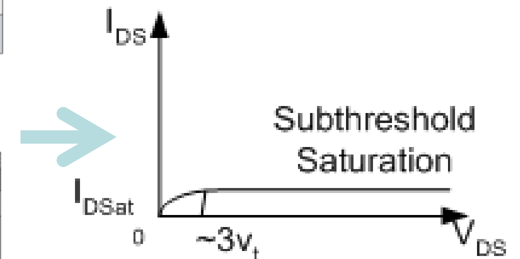
$V_{GS} = 0$ V & $V_{DS} > V_{DSAT}$



Subthreshold Region:

$V_{GS} < V_t$ & $V_{DS} = 0$ V





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Major Differences between SOI MOSFETs and MESFETs

	MOSFET	**MESFET**	MESFET Advantages
Threshold Voltage, V_{th}	Enhancement mode (normally-off) e.g. V_{th} = +0.6V for N-MOSFET	**Depletion mode (normally-on) e.g. V_{th} = -0.5V for N-MESFET**	The availability of depletion mode devices alongside traditional enhancement mode devices allows for greater flexibility in circuit design
Conduction Type	Minority carrier, inversion channel	**Majority carrier, depletion channel**	MESFET does not suffer from floating body effects such as the kink effect. It does not require the body-tie contacts often used as part of SOI CMOS.
Self-aligned	Yes	**No**	The extended drift region from the gate to the drain (L_{aD}) gives the MESFET a high breakdown voltage.
Gate Material	Metal-Oxide-Semi	**Metal Silicide**	The Schottky gate of the MESFET can support significant current flow. It is tolerant of high voltage excursions, radiation and wide temperature variations

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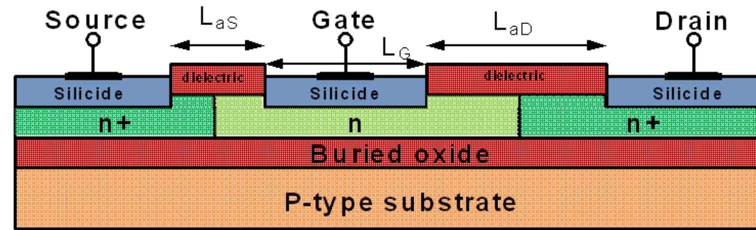
Family of Curves

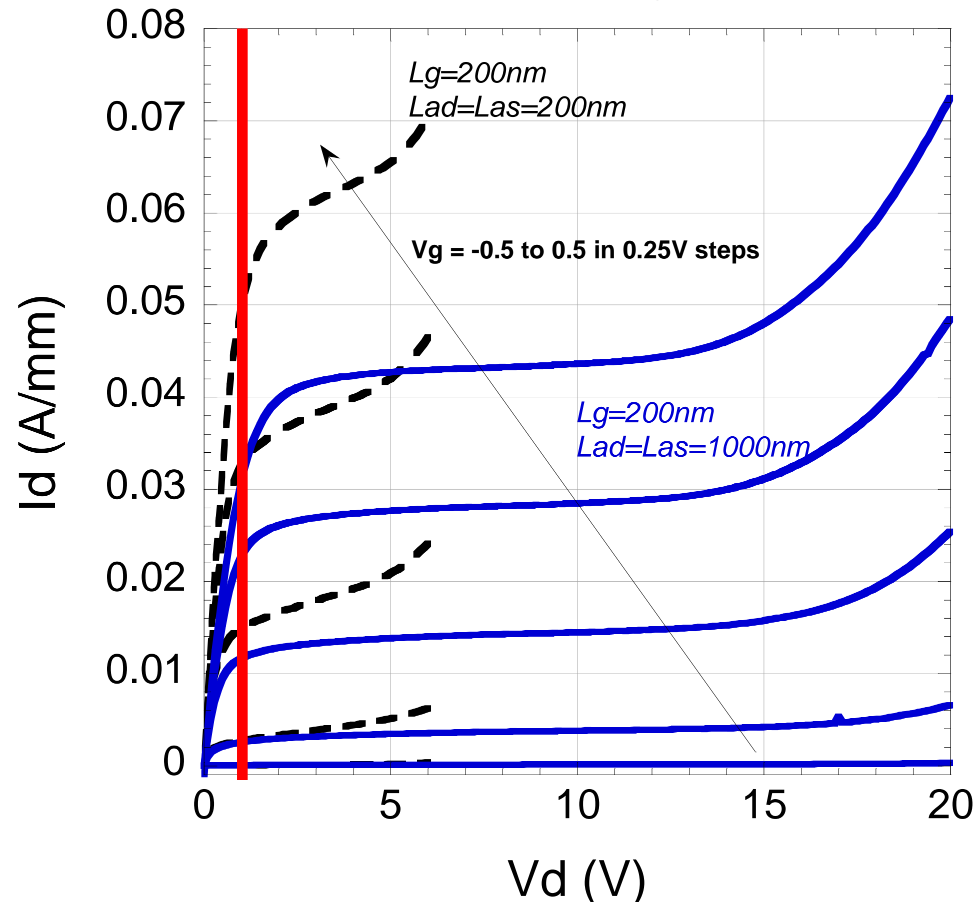
LaS=LaD=200nm
gives highest
current drive

but

LaS=LaD=1000nm
allows for higher
voltage drive **(>20V)**

Note that the red line shows an approximate breakdown voltage of a MOSFET





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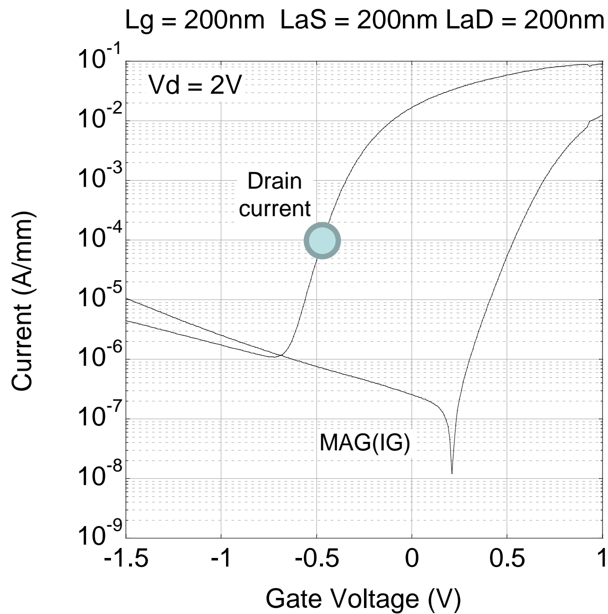
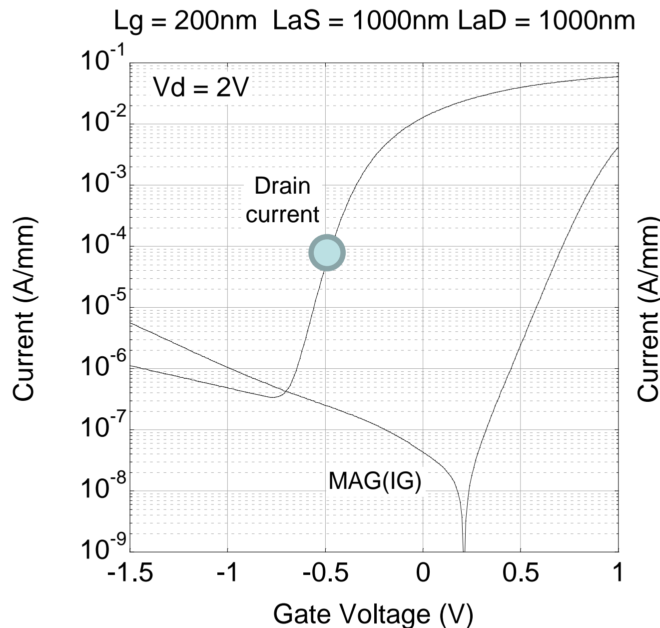
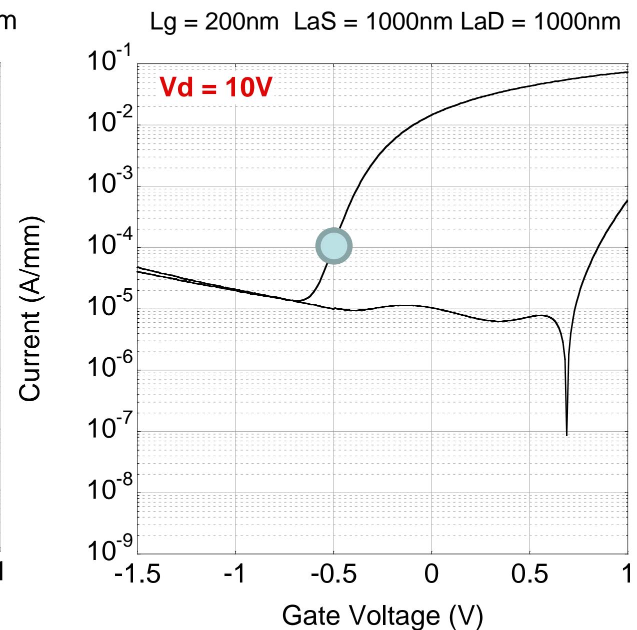
Turn-on Characteristics / Gummel Curves

The threshold voltage is relatively independent of LaS and LaD

Vth close to -0.5V for both LaS=LaD=200nm and LaS=LaD=1000nm







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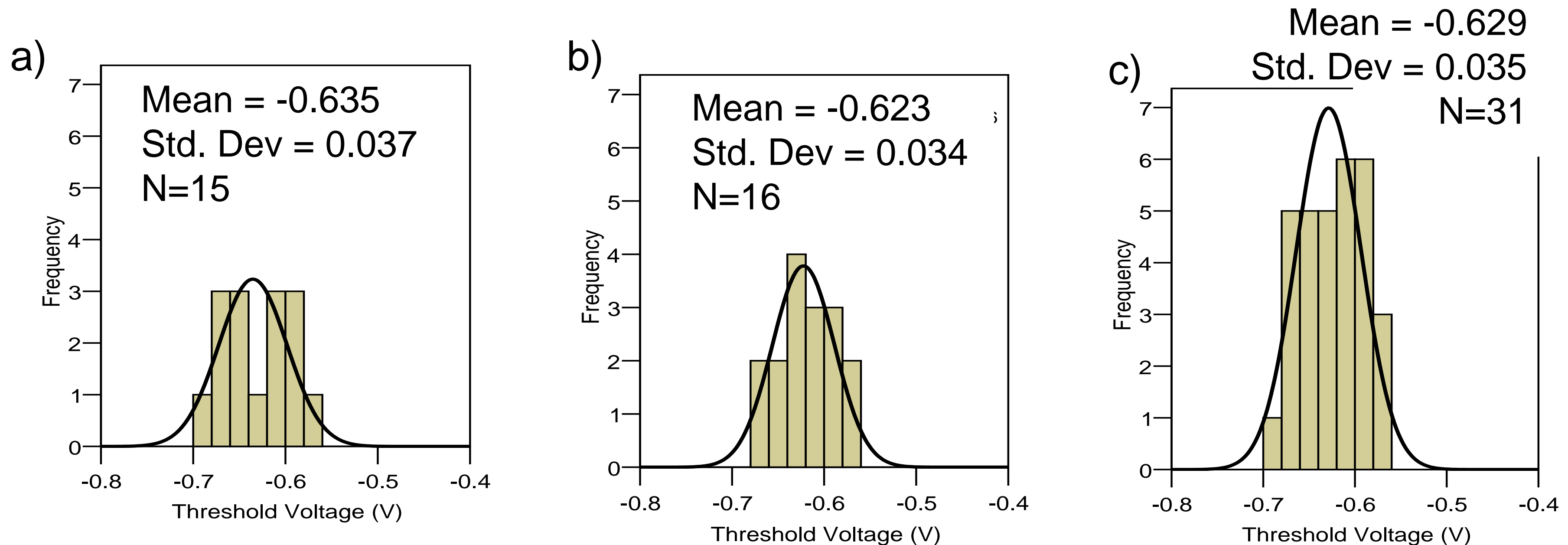
Statistical Analysis

MESFETs structures have been fabricated on multiple foundry runs. Key parameters such as Vt (shown here) have been measured across the different runs on multiple die.



The threshold voltage distributions for (a) Run 1 (b) Run 2. The distribution across all 31 devices is shown in (c). We are currently adding to these statistics.

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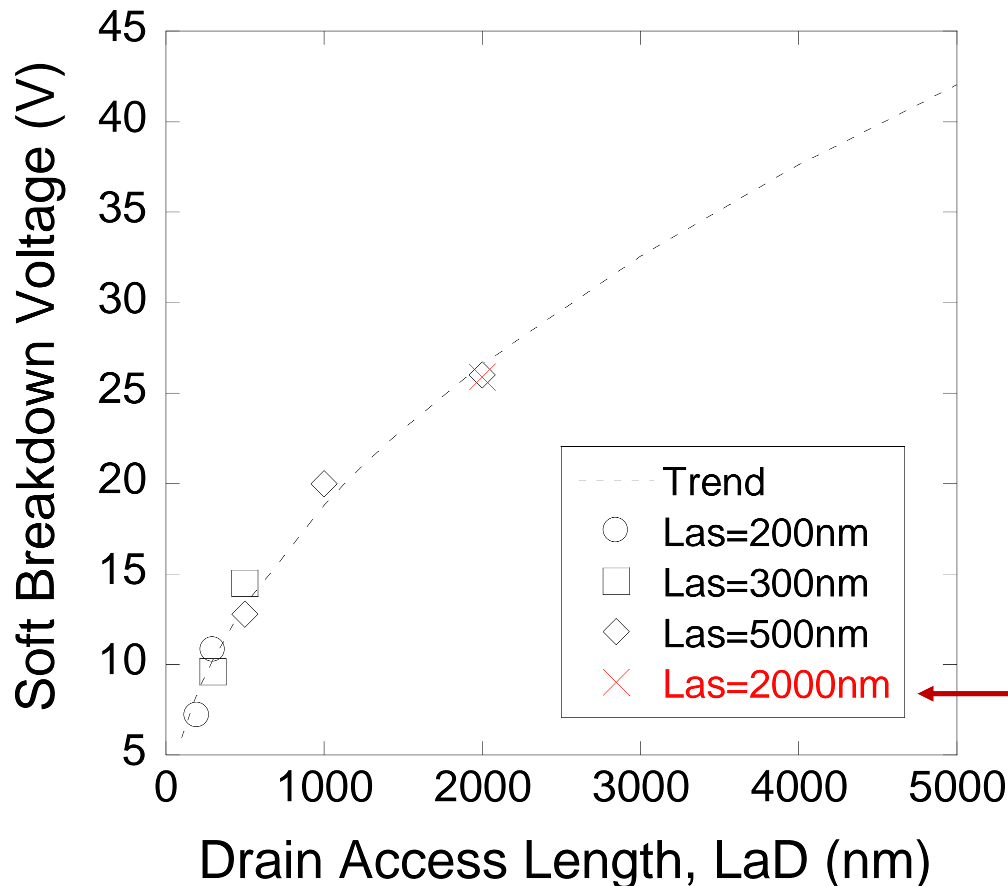
Soft Breakdown Characteristics – 45nm Technology

- **The (soft) breakdown voltage appears to be proportional to LaD/ln(LaD) which suggests avalanche breakdown**



- Largest LaD fabricated was 2µm
- Predicting V_{BD} > 40V for LaD=5µm
- Longer LaD recently fabricated

Breakdown remained the same before and after stress testing

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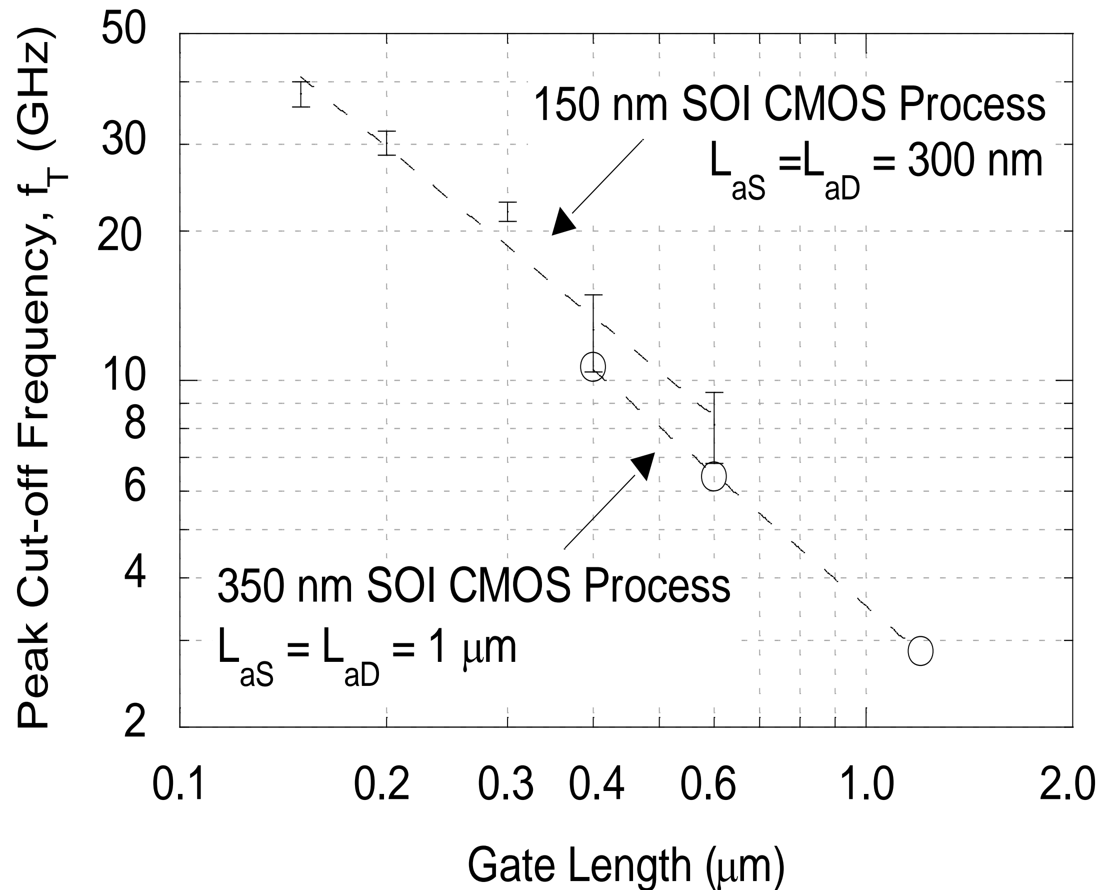
Ft of MESFETs at different Nodes



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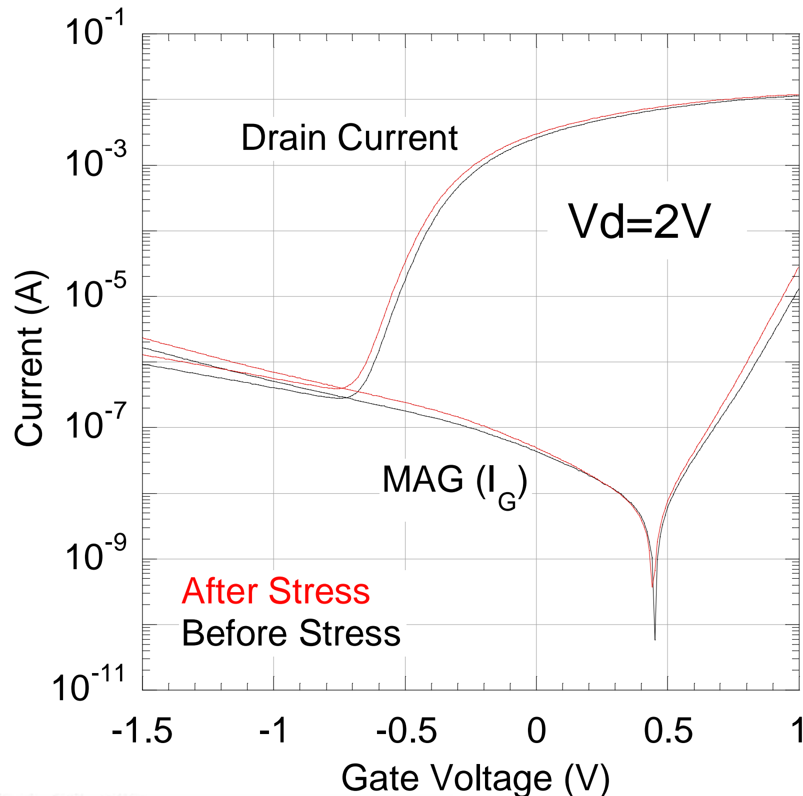
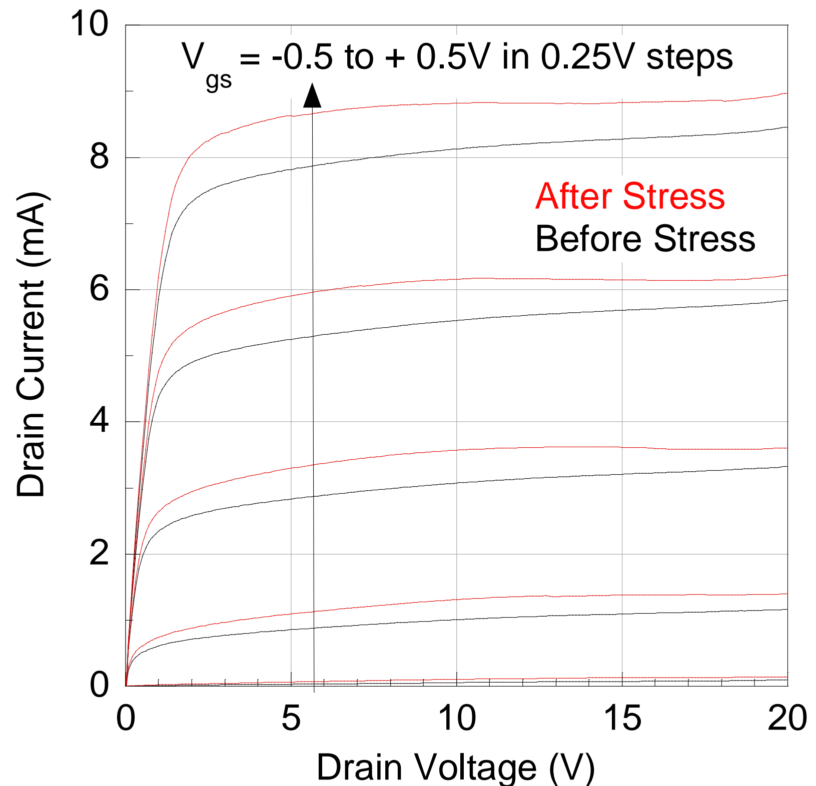
Accelerated Lifetime Test

- MESFET measured had Lg=200nm and LaS=LaD=2000nm
- Stress Conditions: 160ºC at a fixed bias of Vd=10V, Vg=0.5V for 168 hours.
- Small increase in drain current and marginal shift in Vt was observed after stress but otherwise there were few changes in the MESFET's operation.
- Off-state breakdown voltage remained at ~25V after the stress test.





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SPICE Model

- Square-law model [I_{DS} α$(V_{GS}-V_{th})^2$] in saturation.
- Exponential characteristics [I_{DS} α exp $(V_{GS}-V_{th})$] in sub-threshold.
- Well-defined extraction procedure.
- Correlated to analytical models to ease the development of higher level models.
- Sub-circuits for leakage effects, breakdown voltage and short-channel effects.
- Charge-based capacitance model.

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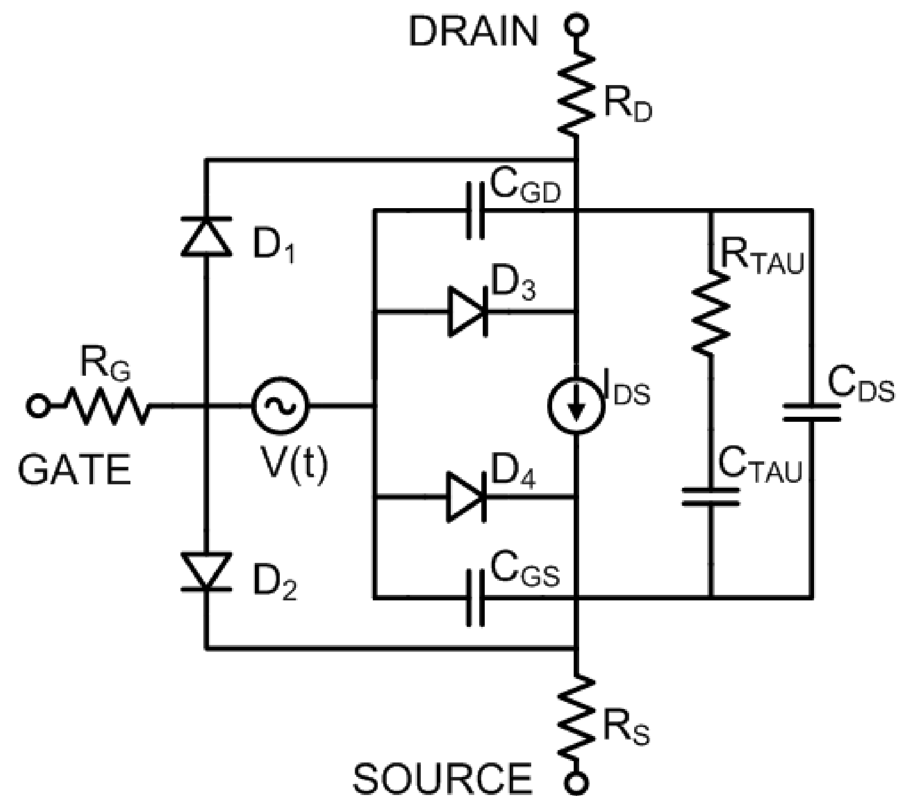
Availability of Model in Cadence and ADS Important

MESFET modeling consists of :

- DC Measurements
- S-parameter measurements of GSG devices at different bias conditions
- Pad de-embedding
- Extrinsic parameters extraction using a ColdFET method
  - VDS=0 and gate is turned on very hard
- Intrinsic parameter extraction based on DC and S-parameters measurements

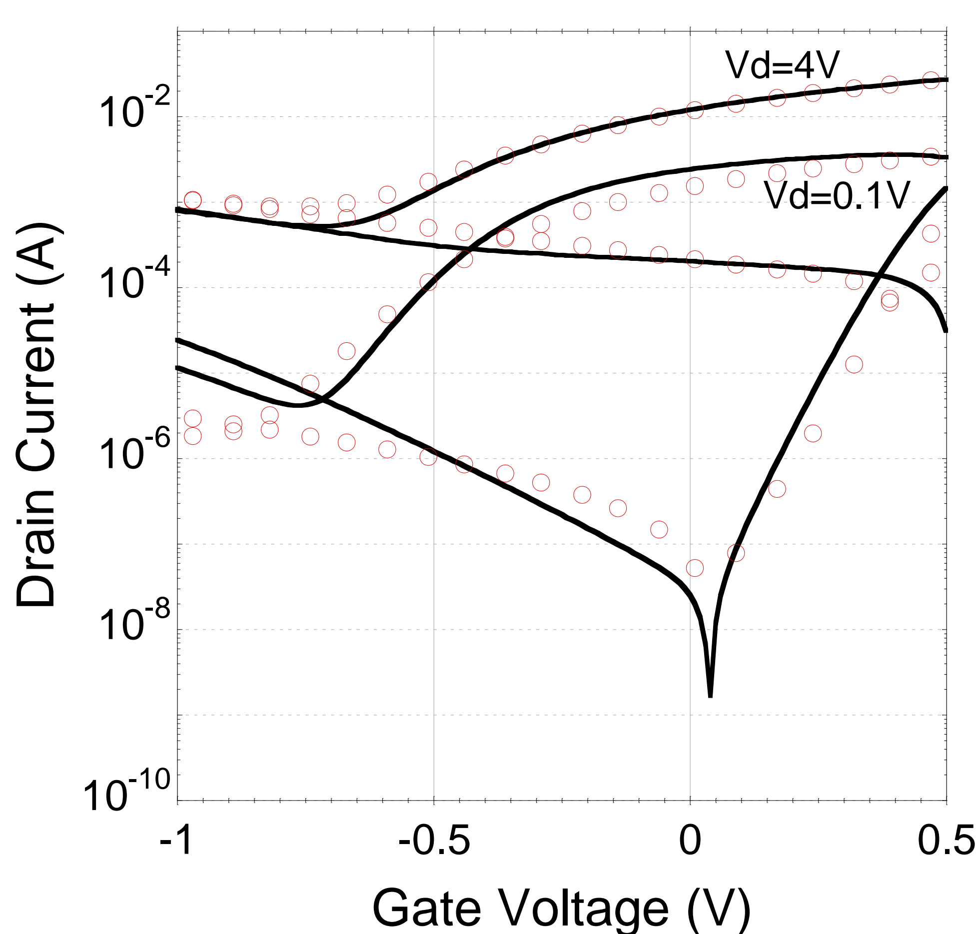
$$I_{ds} = \beta \times (V_G)^Q \times f_k \times (1 + \lambda V_{ds})$$

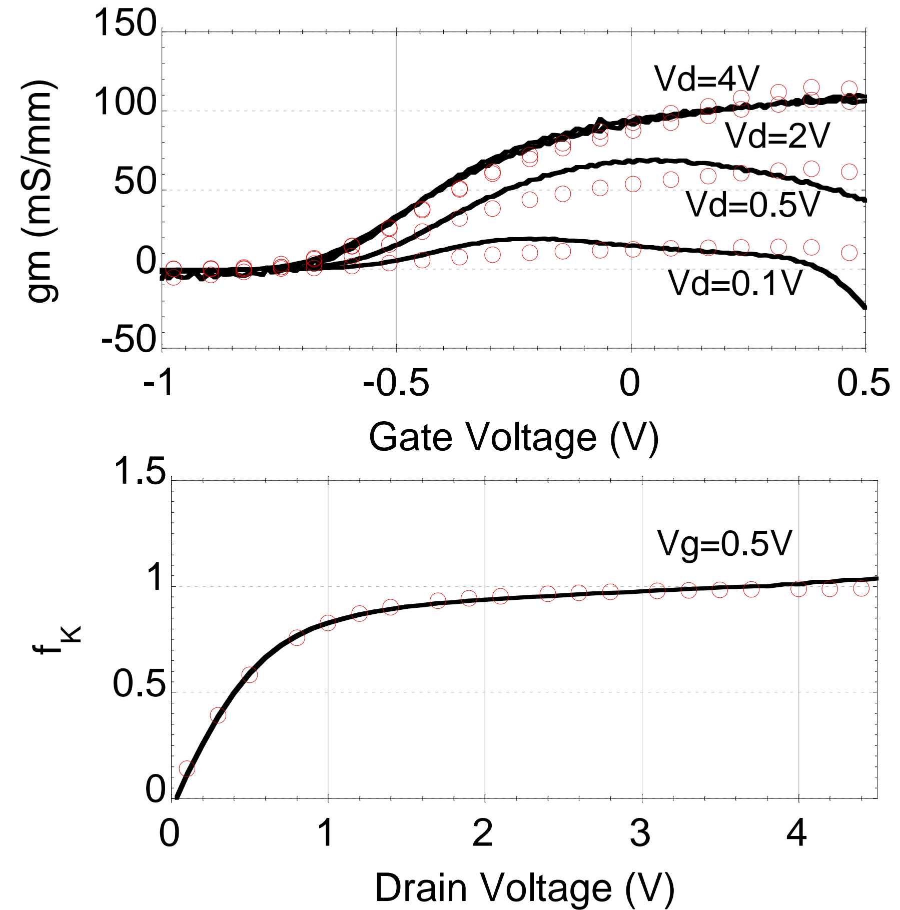
$$f_k \approx \tanh(\alpha V_{ds})$$



Turn-on Characteristics

TOM3 Model shows a good fit across different drain and gate bias conditions





S. J. Wilk *et al.*, "Characterization and modeling of enhanced voltage RF MESFETs on 45nm CMOS for RF applications," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2012*, pp.413-416, 17-19 June 2012

Black = Measured

Red = Simulation

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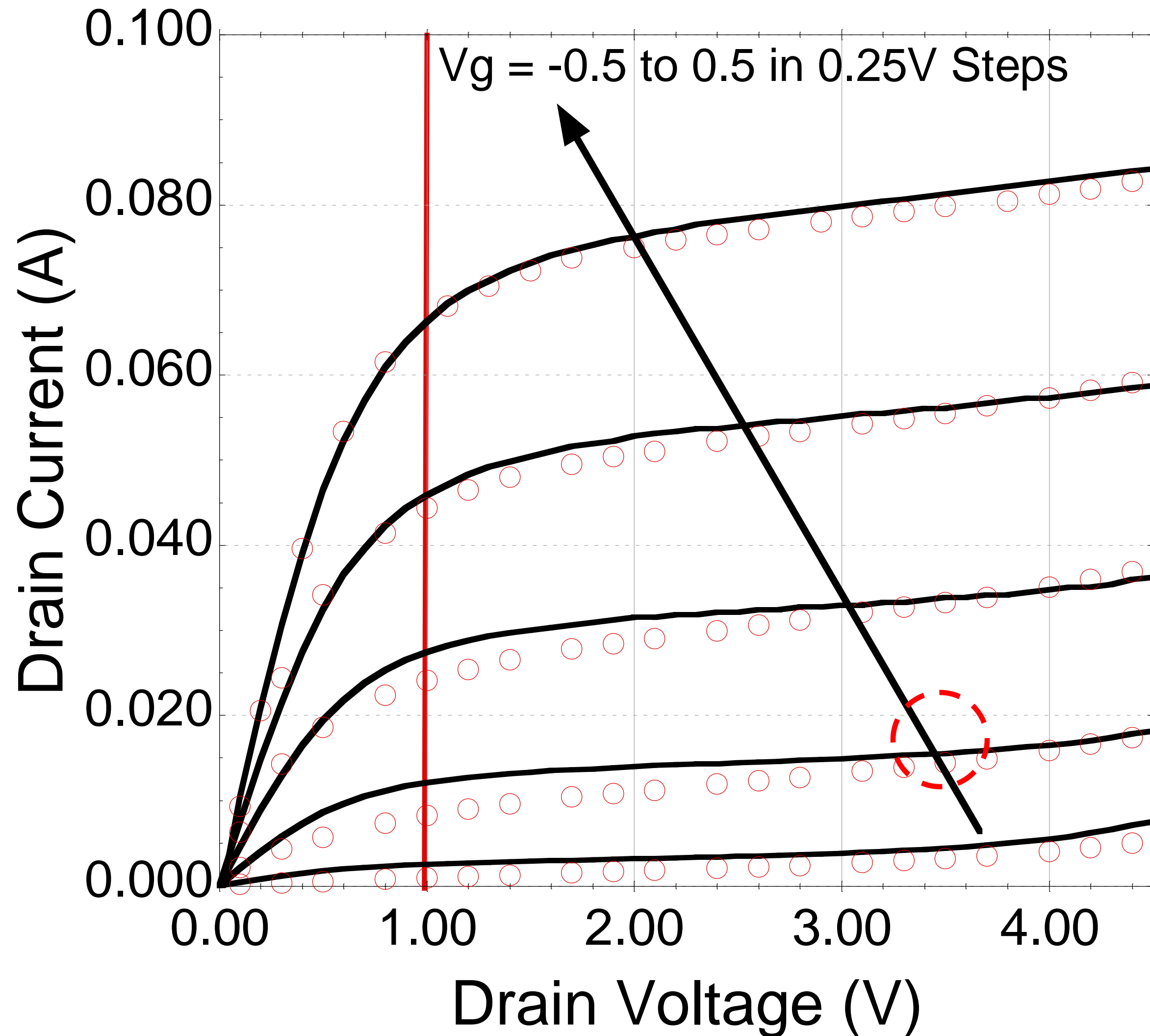
Family of Curves



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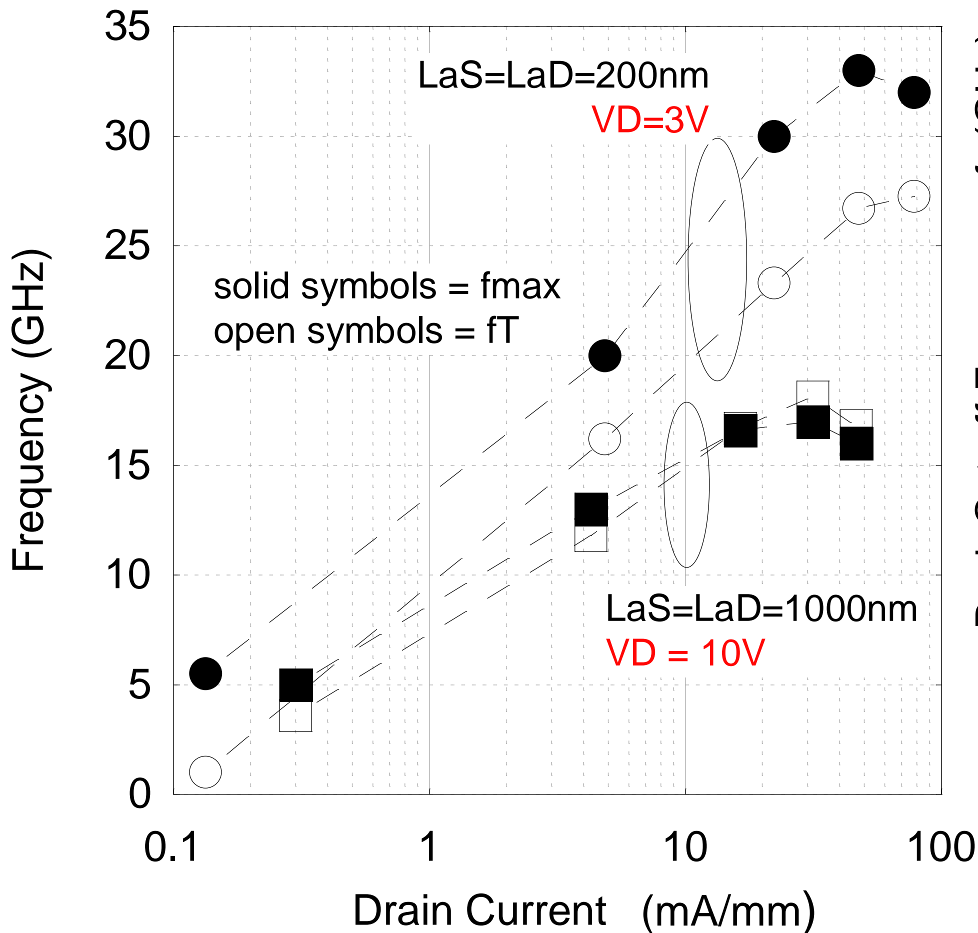
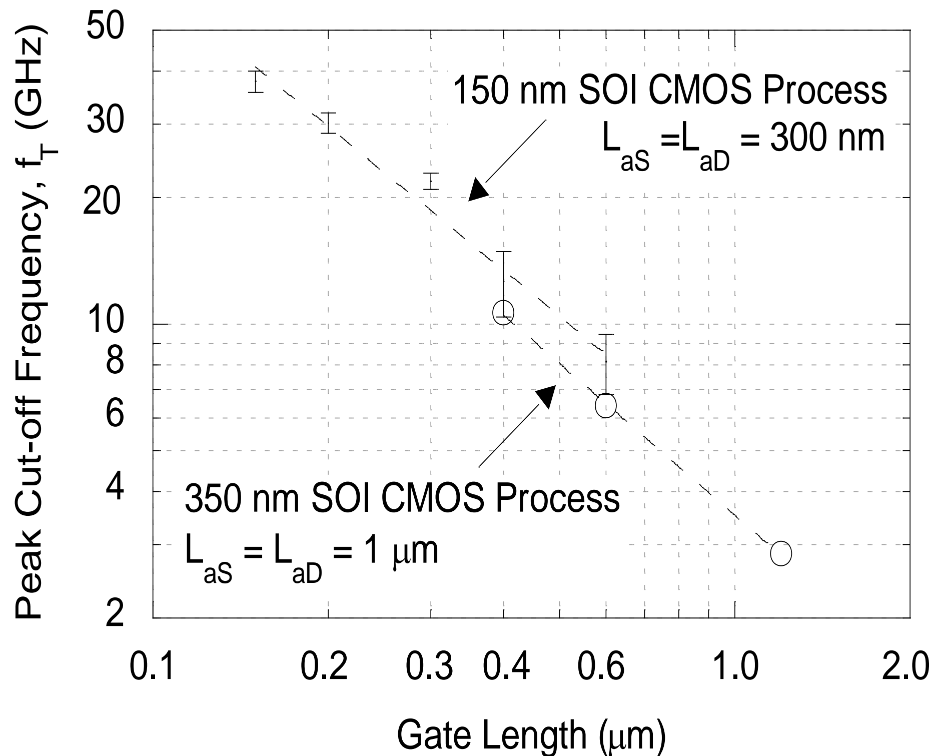
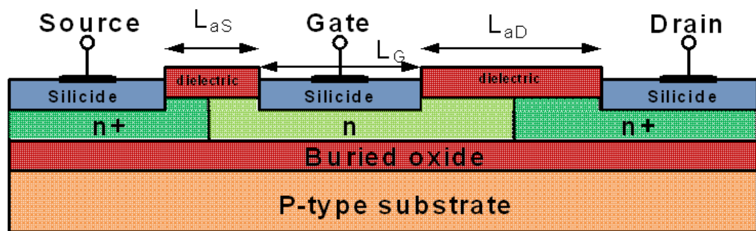
RF Characteristics







- LaS=LaD=200nm gives higher f_T and f_{max},
- L_{aS}=LaD=1000nm allows for higher drain bias

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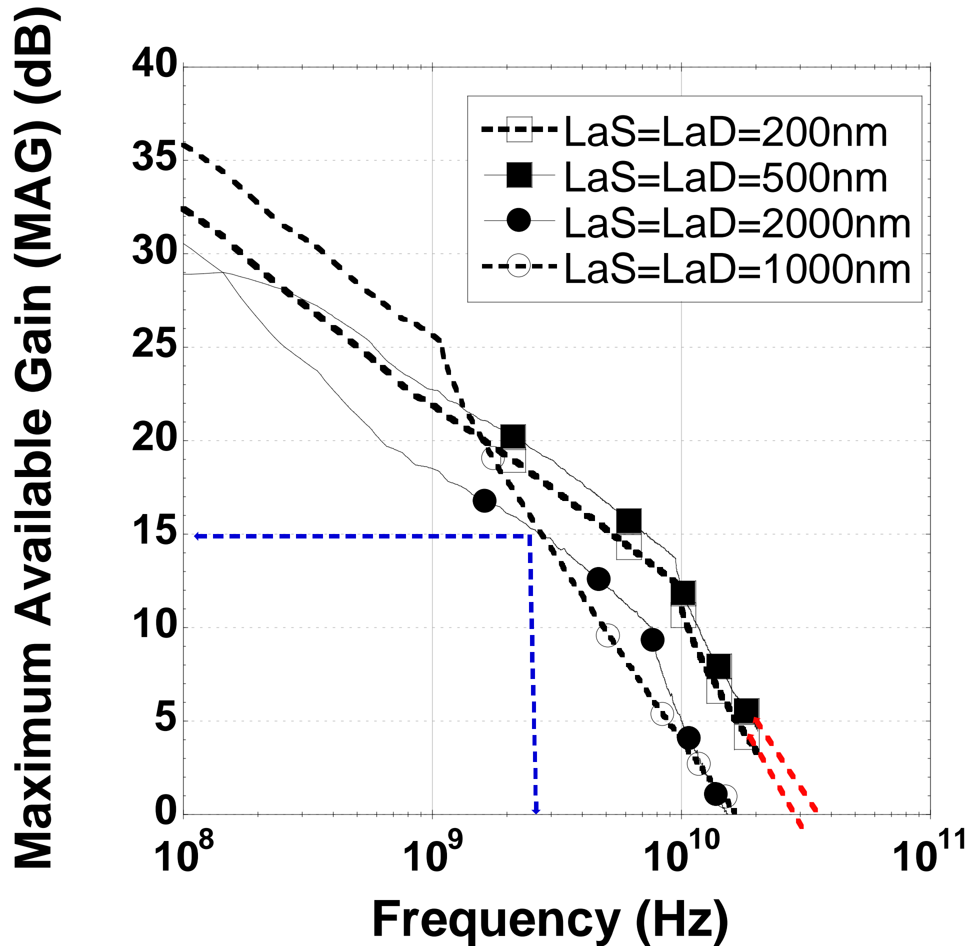
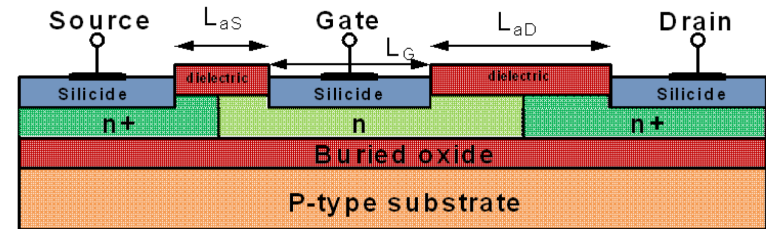
Maximum Available Gain of MESFETs on 45nm Process

- All MESFETs measured thus far have more than 15 dB gain below 2.5GHz
- Can improve fmax by optimizing LaS
- LaS can be equated to source degeneration of an amplifier





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S Parameter Measurements and Model

Cut-off Frequency

$$f_T \cong \frac{gm}{2\pi C_{GG}}$$

Model the Gate Charge

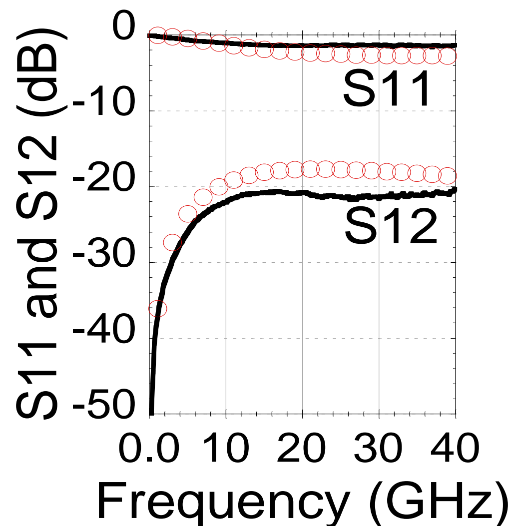
$$Q_{GG} = Q_{GL} \times T + Q_{GH} \times (1 - T)$$

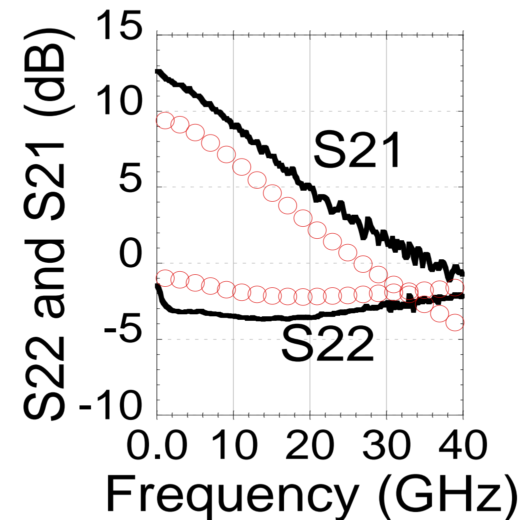
Where
Q_{GL} *is the low power region*
And
Q_{GH} *is the highpower region*

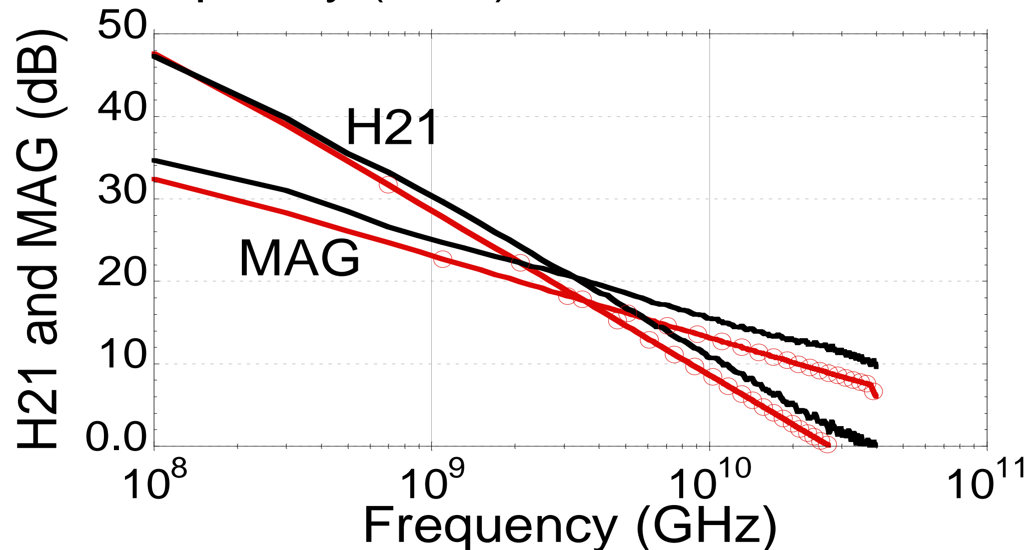
T describes the transition between regions

$$T = \exp(-Q_{GGB} \times I_{ds} \times V_{ds})$$

Vd=2V and Vg=0.25V







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Linear Regulator

linear regulator *is a circuit used to maintain a steady output voltage*

Pros:
Steady Output Voltage
High PSRR

Cons:
Inefficient as input voltage becomes much higher than output voltage because transistor must dissipate the difference

Buck Converter

A ***buck converter*** *is a step-down DC to DC converter*

Pros:
Efficient for larger voltage steps

Cons:
High ripple and noise can be too much for system requirements

Buck Converter and Low Dropout Linear Regulator

Efficient for larger voltage steps and can maintain output voltage

Want low dropout regulator so that the buck output can be close to the desired output voltage for best efficiency

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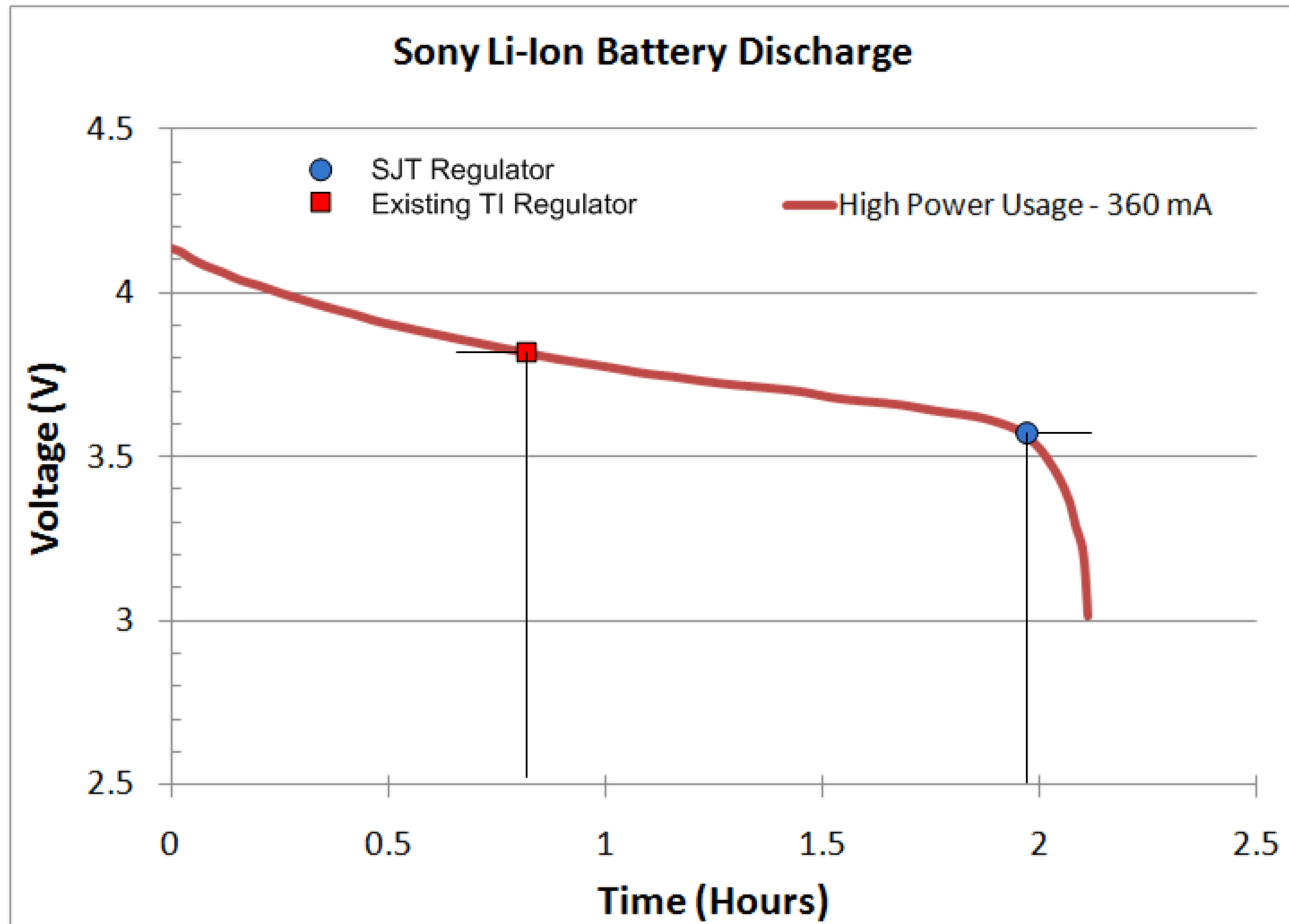
Why Low Dropout?

The less overhead your power management needs, the longer the device can work on a single battery charge



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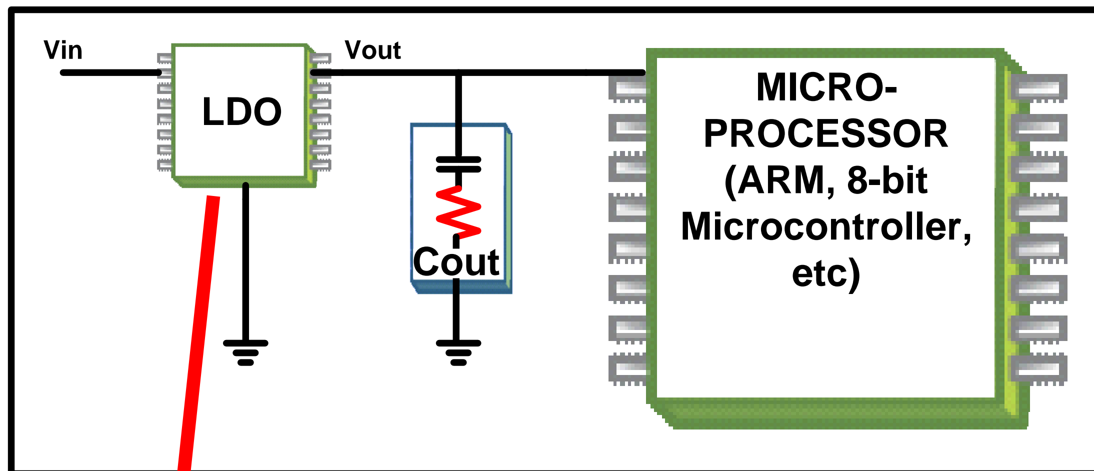
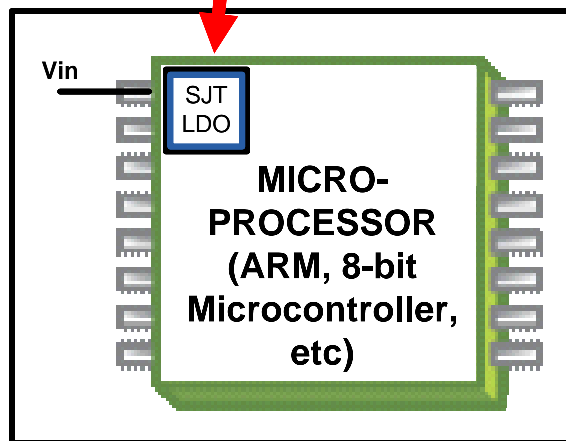
Integrating Power Management - Processors

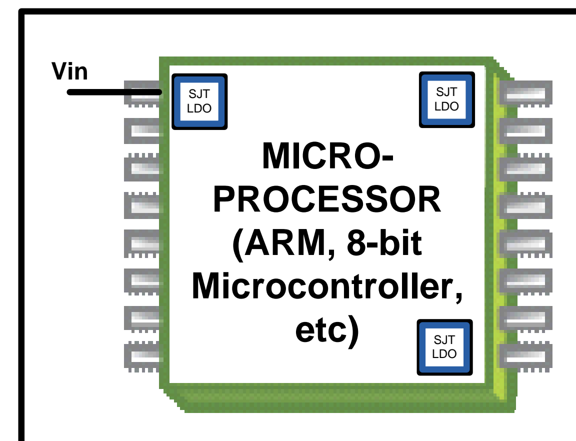
Ideally, integrate power management because designers are pin constrained

How to connect the supply to the integrated circuit if the on chip transistors are low voltage?

Pin constrained if you need a specific capacitor at the output



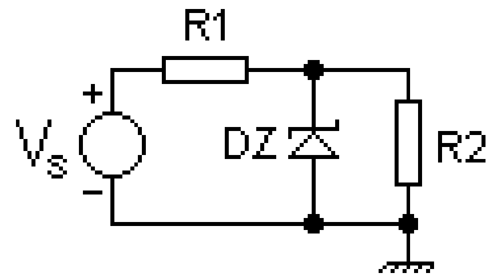




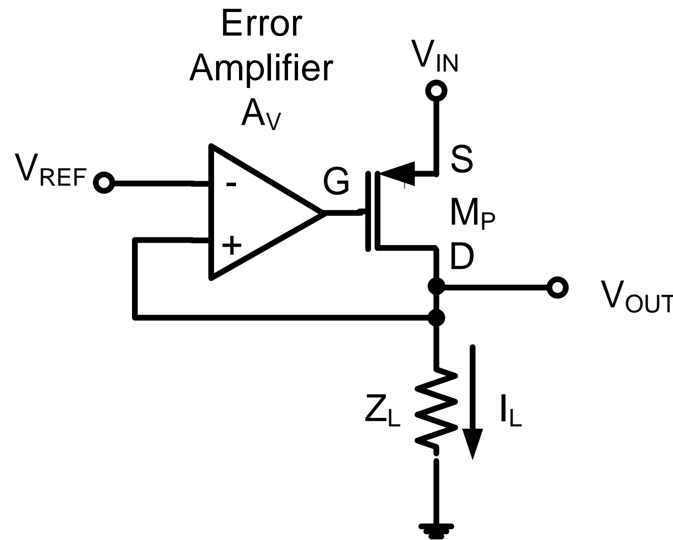
SJT Solution **Pinpoint Load Placement**

Contact: info@sjtmicropower.com

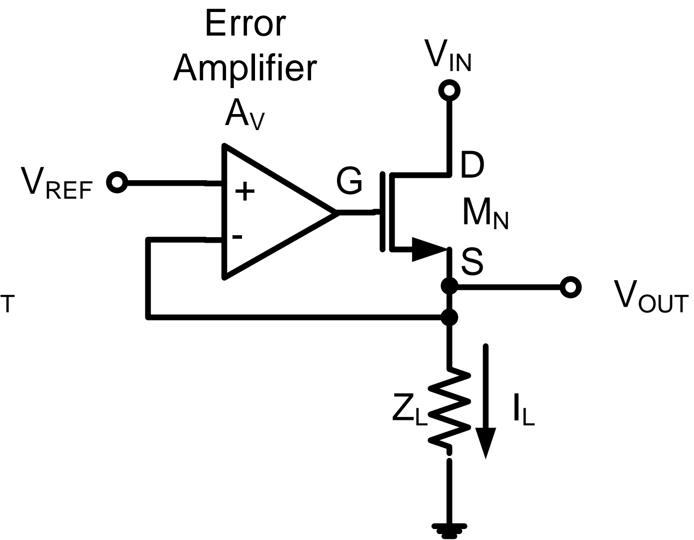
Common Linear Regulator Topologies



Zener Diode



PMOS Voltage Regulator
Common Source



NMOS Voltage Regulator
Source Follower

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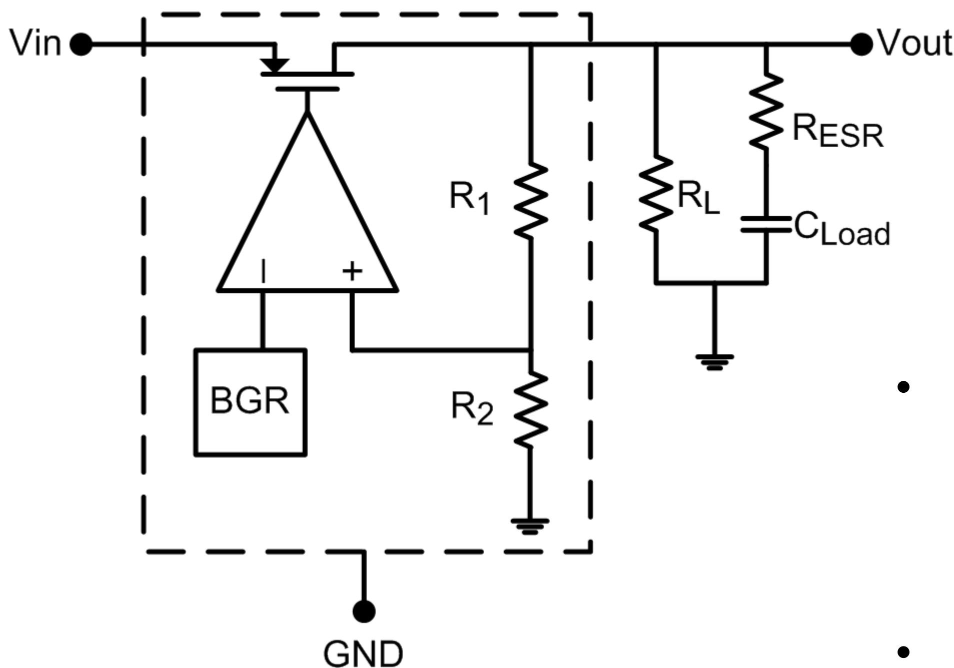
PMOS LDO Implementation



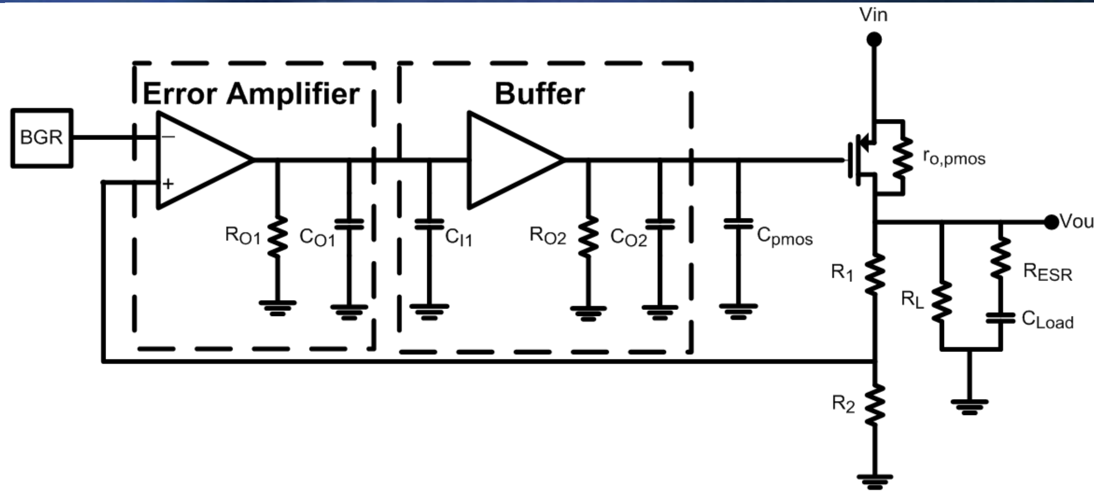
Advantages

- Common source (CS) configuration allows error amp to drive gate of PMOS below V_{out}
- Can achieve very low dropout voltages
  - $V_{DO} = R_{on} * I_{load} = V_{DSAT}$
    - Note: Ideal dropout—does not include the parasitic voltage drop from metal lines

Disadvantages

- Stability concerns arise from CS configuration
  - High R_{out} at V_{out} node
  - Need load cap with its associated ESR
- PMOS has 2-3x lower mobility than NMOS
  - Need 2-3x larger pass device to achieve a given current drive

PMOS LDO Implementation (Cont)

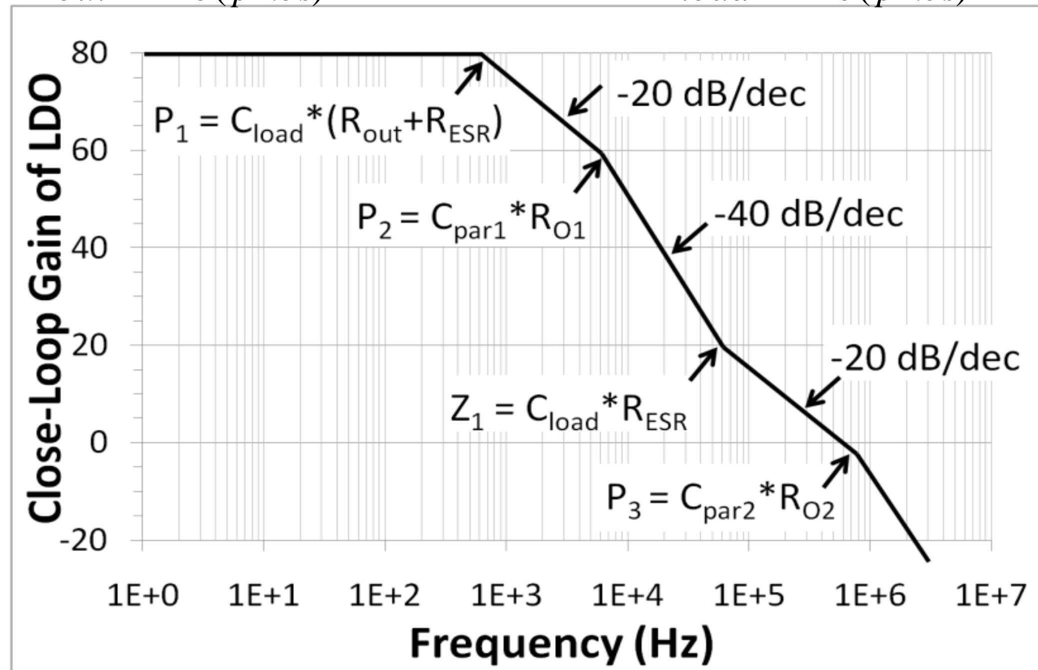


Common source (CS)

$$C_{par1} = C_{O1} // C_{I2}$$

$$C_{par2} = C_{O2} // C_{PMOS}$$

$$R_{out} = r_{o(pmos)} //(R_1 + R_1) // R_{load} \approx r_{o(pmos)}$$



$$f_{P1} \approx \frac{1}{2\pi C_{load}(R_{out} + R_{ESR})}$$

$$f_{P2} \approx \frac{1}{2\pi C_{par1} R_{O1}}$$

$$f_{Z1} \approx \frac{1}{2\pi C_{load} R_{ESR}}$$

$$f_{P3} \approx \frac{1}{2\pi C_{par2} R_{O2}}$$

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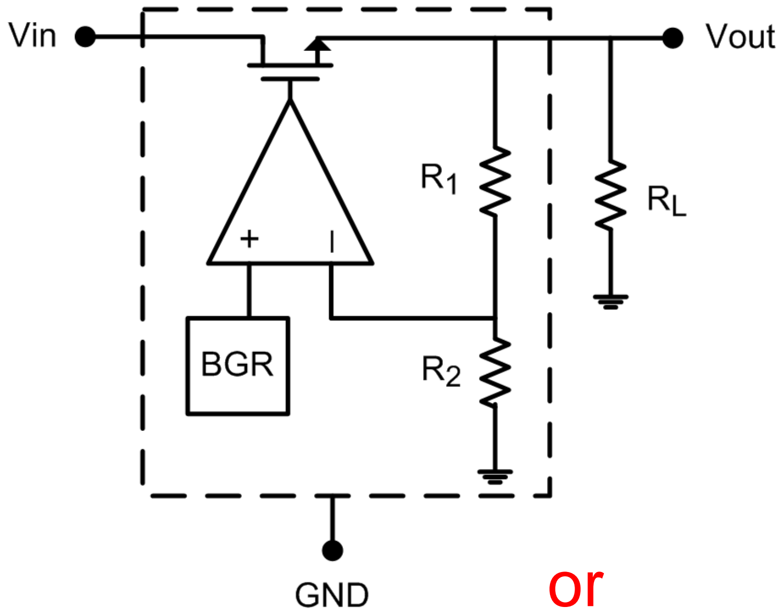
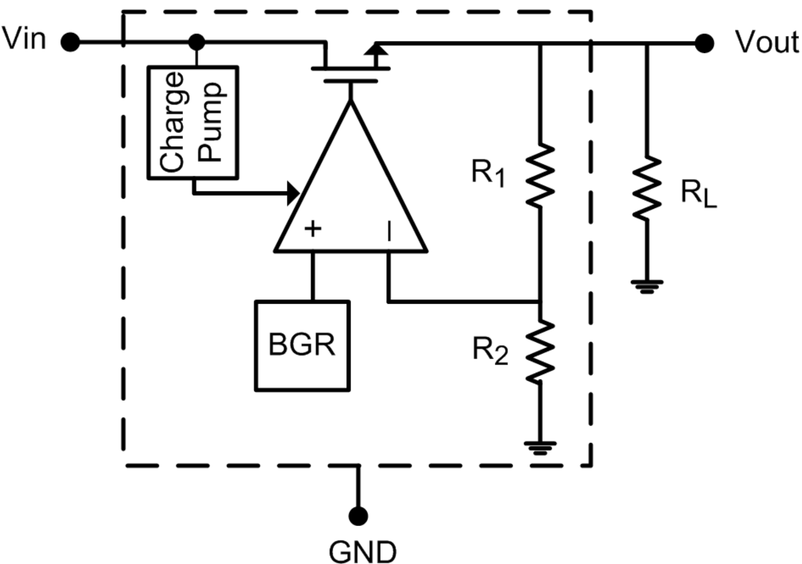
NMOS (Enhancement Mode) LDO Implementation



or



Advantages

- Source follower configuration
  - $R_{out} \sim 1/gm$
    - Significantly improves stability
- NMOS device has higher current drive than PMOS
- Smaller input capacitance since smaller device is needed for given current drive
  - Improved transient response

Disadvantages

- Without charge pump (CP), gate must be driven to overcome V_t
  - Dropout is dependent on V_t
    - $V_{DO} = V_t + V_{DSAT}$
- Including CP negates dependence of V_t but increases die size and noise

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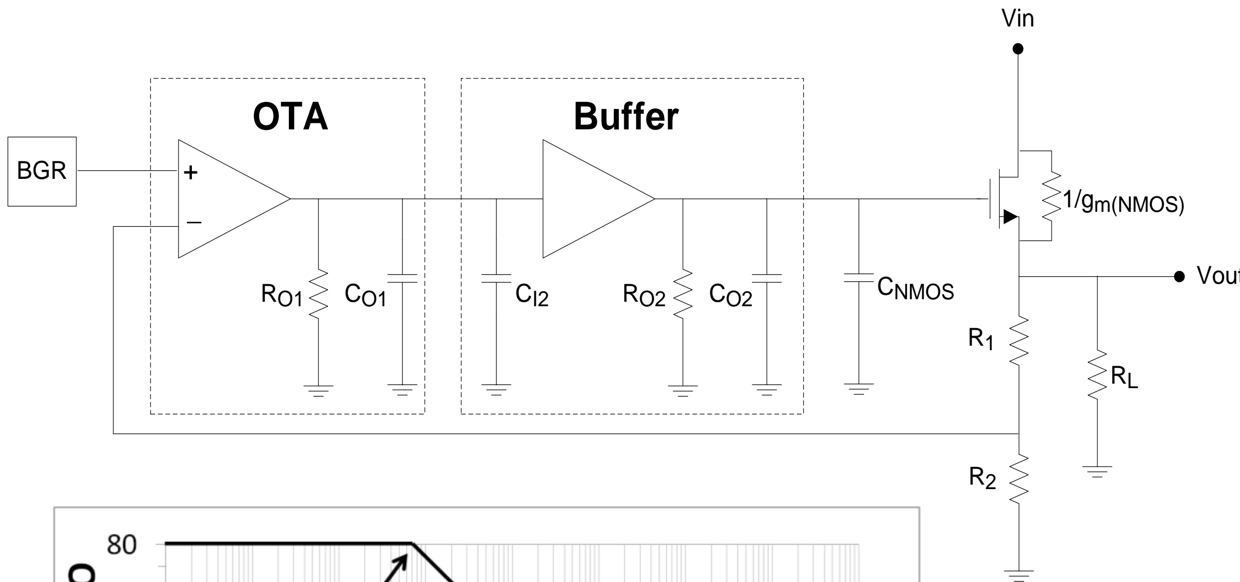
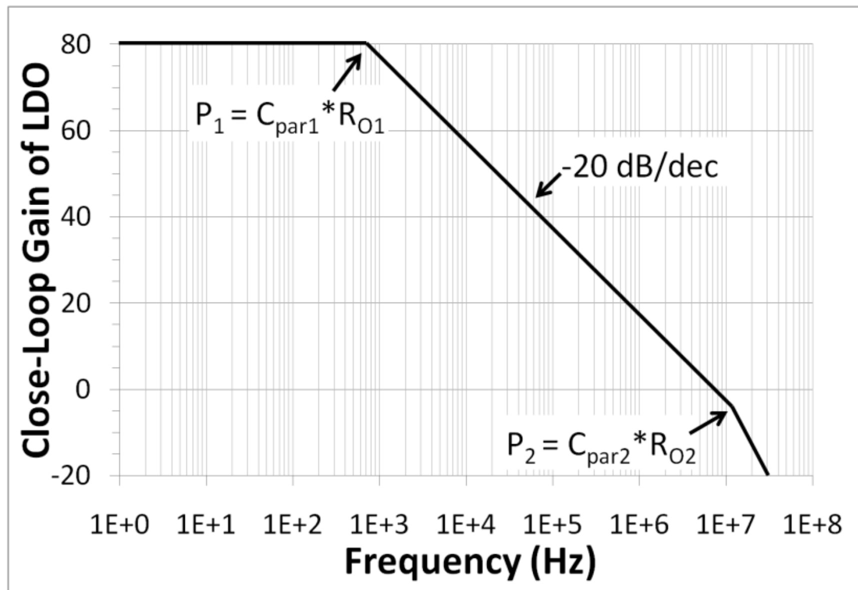
NMOS (Enhancement Mode) LDO Implementation



$$C_{par1} = C_{O1} // C_{I2}$$

$$C_{par2} = C_{O2} // C_{NMOS}$$

Source follower configuration



$$f_{P1} \approx \frac{1}{2\pi C_{par1} R_{O1}}$$

$$f_{P2} \approx \frac{1}{2\pi C_{par2} R_{O2}}$$

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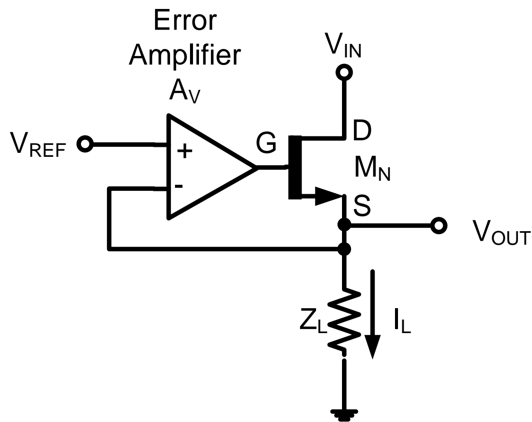
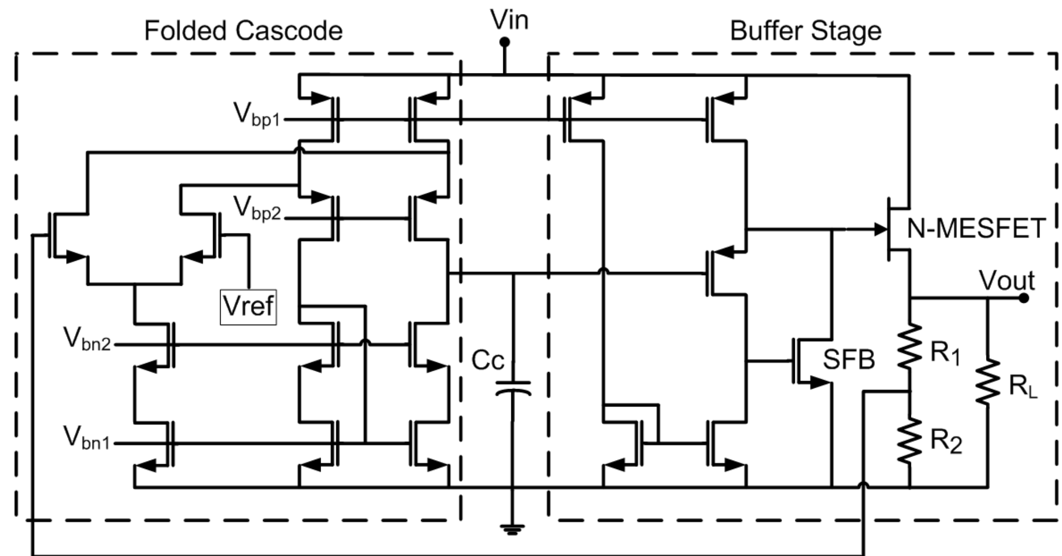
MESFET LDO



MESFE T Regulator
Source Follower Configuration



Advantages

- Combines attributes of NMOS and PMOS LDOs
- Depletion mode operation allows pass transistor to be orientated in source follower configuration without a charge pump
- Closed loop frequency response is similar to NMOS LDO

Disadvantages

- Depletion mode means MESFET will conduct under most bias conditions
- Gate leakage of MESFET

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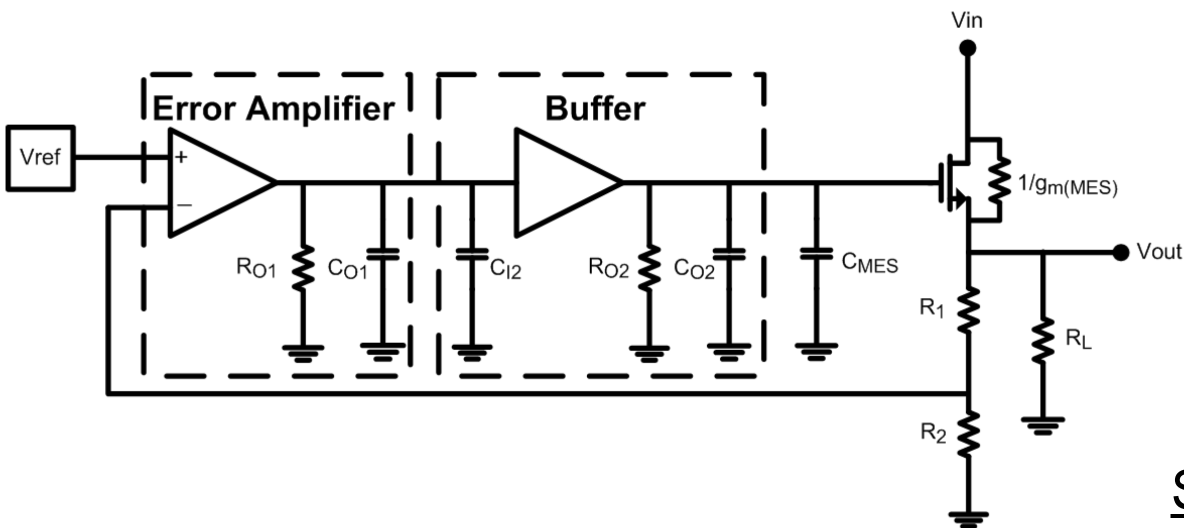
MESFET LDO (Cont)

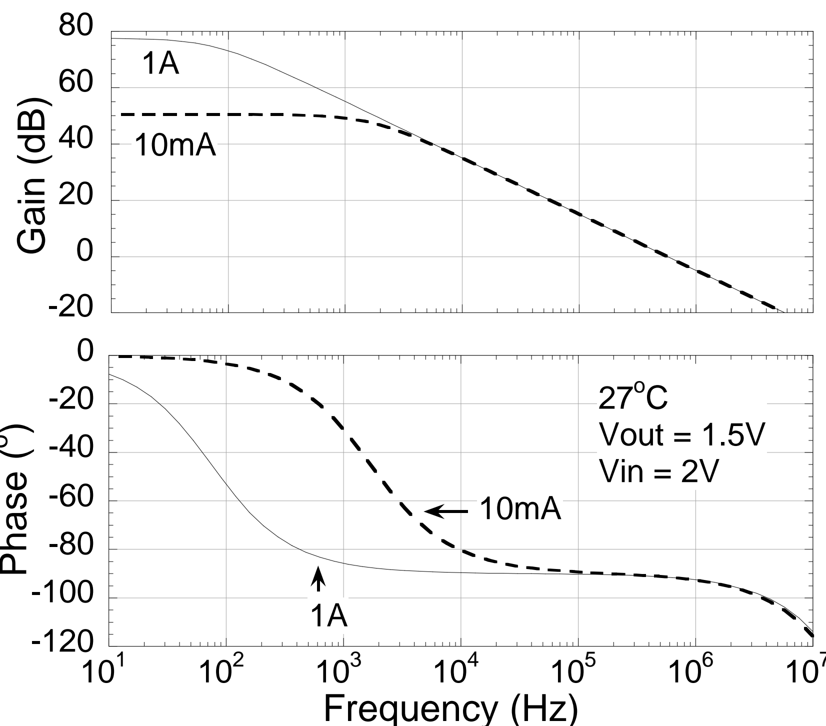


$$f_{P1} \approx \frac{1}{2\pi(C_{O1} + C_C + C_{I2})R_{O1}}$$

$$f_{P2} \approx \frac{1}{2\pi(C_{O2} + C_{MES})R_{O2}}$$

- Can be treated as single pole system if:
  - P1 is appropriately placed
  - Output capacitance is not large

Simulated Gain/Phase



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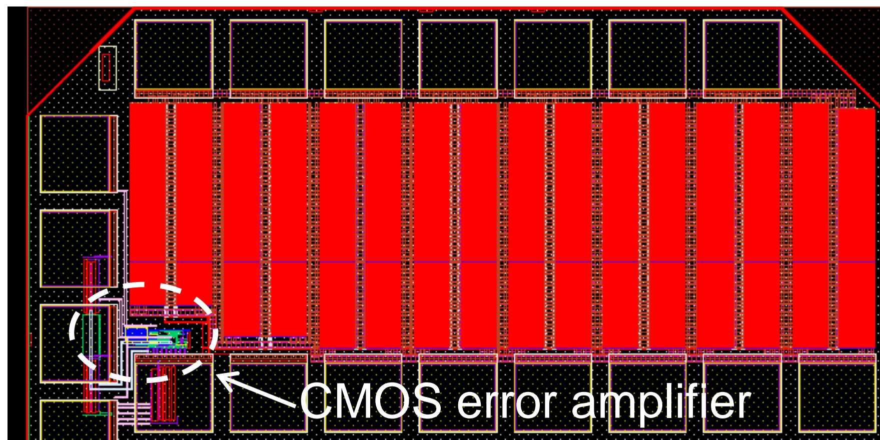
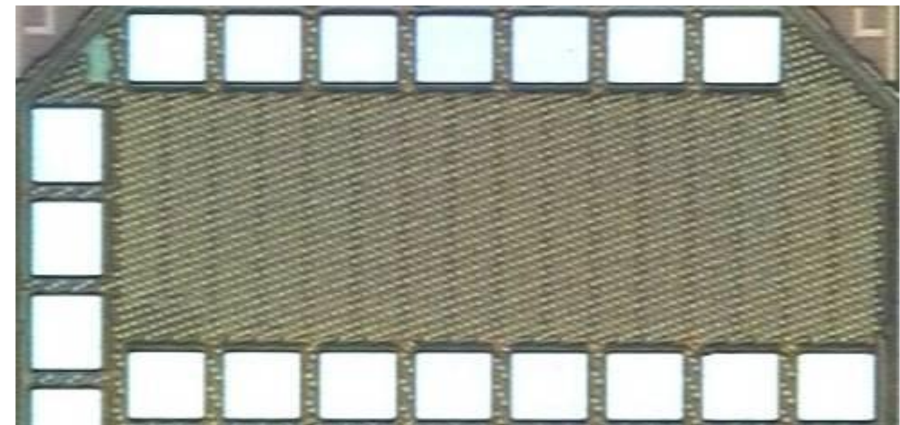
IBM MESFET Linear Regulator

- Design includes a high current drive MESFET integrated with a CMOS error amplifier
- MESFET width of 152.2 mm with gate length of 200nm and LaD=LaS=200nm
- Die size of ~ 0.5mm x 1mm
- Regulator area is 0.245 mm^2 without the bond pads

CAD Layout

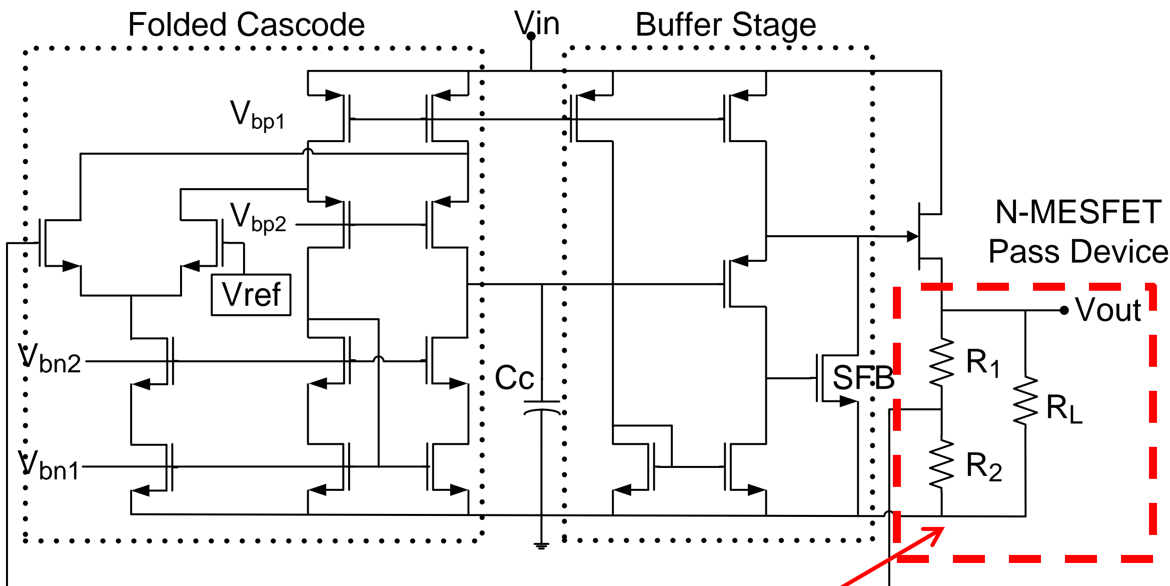


Die Photograph



Summary of Measurements

- High current drive > 3A
- Low on resistance, R_{on} < 10 $m\Omega \cdot mm^2$
- Low dropout voltage V_{DO}< 170mV for a 1A load
- Low quiescent current, I_Q < 75 μA



off-chip components

External feedback resistors R1 and R2 chosen to give V_{out} =1.5V

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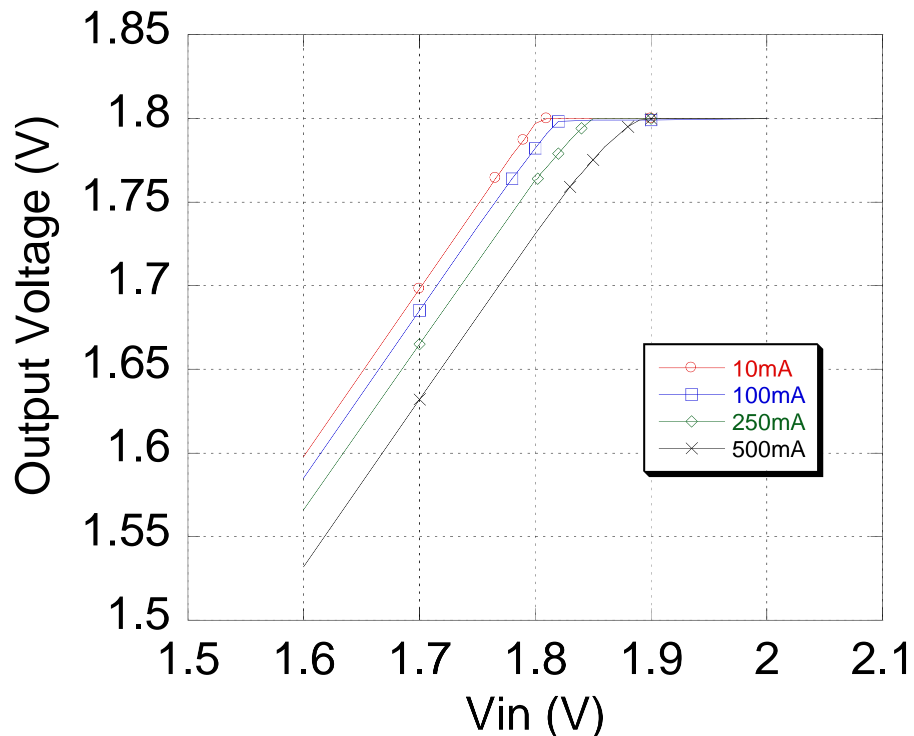
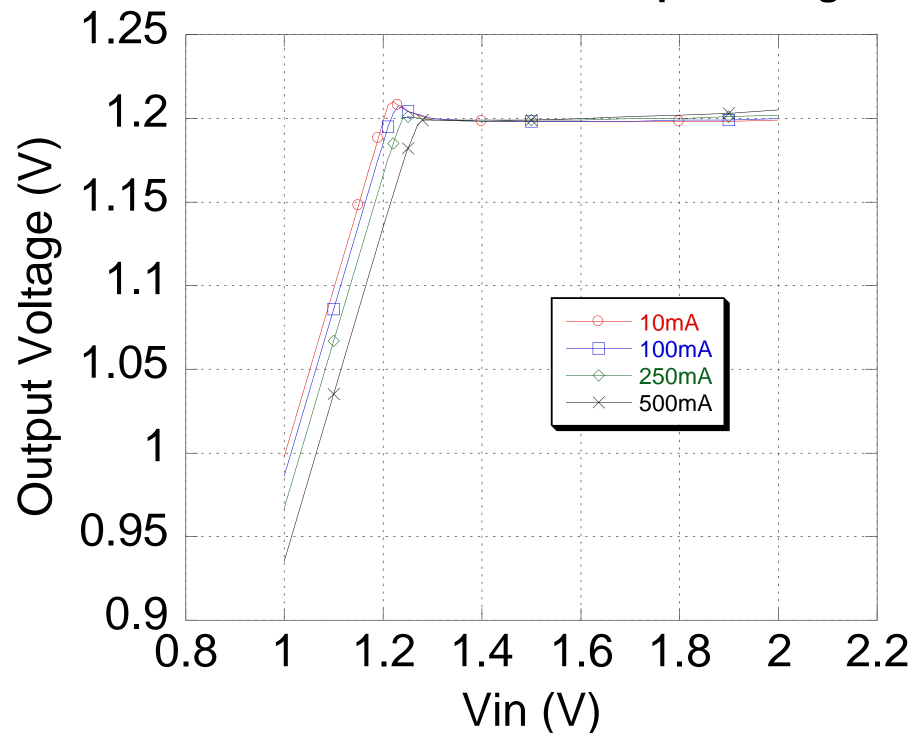
MESFET Linear Regulator (cont.)

Line Regulation

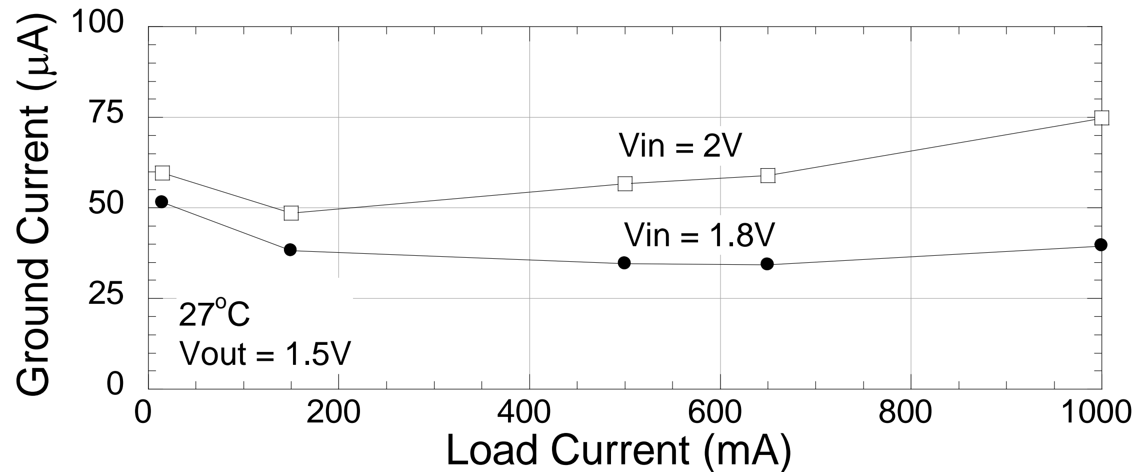




W. Lepkowski, et al., "An integrated MESFET voltage follower LDO for high power and PSR RF and analog applications," *Custom Integrated Circuits Conference (CICC), 2012 IEEE* , vol., no., pp.1-4, 9-12 Sept. 2012

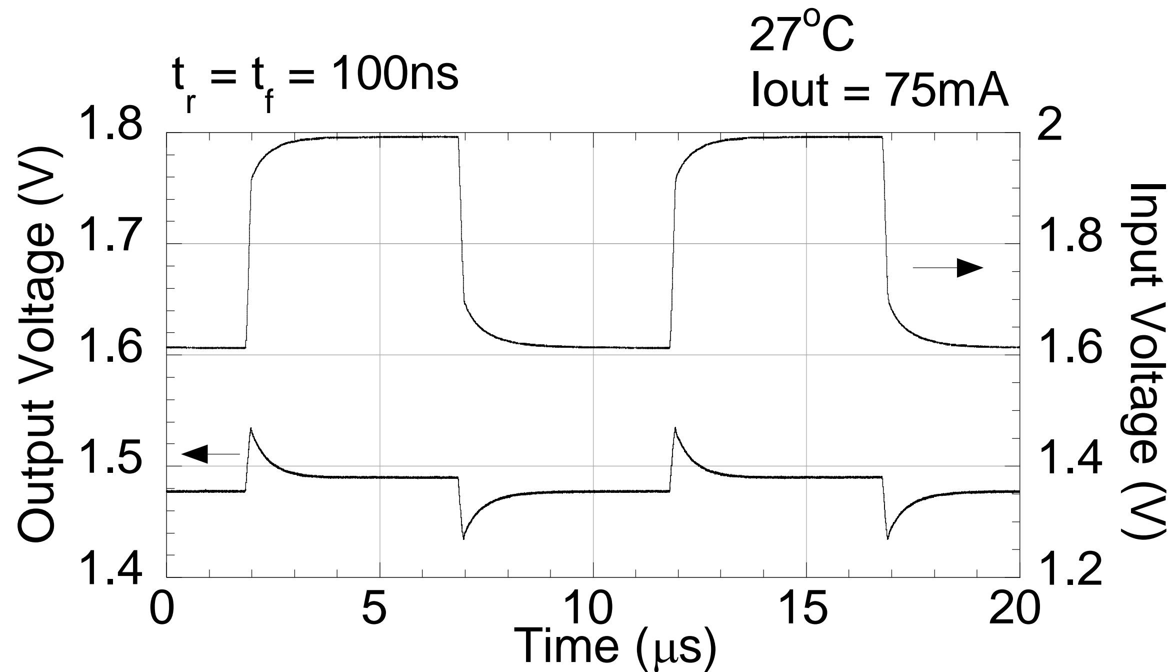
Contact: info@sjtmicropower.com

Quiescent current



W. Lepkowski, et al., "An integrated MESFET voltage follower LDO for high power and PSR RF and analog applications," *Custom Integrated Circuits Conference (CICC), 2012 IEEE* , vol., no., pp.1-4, 9-12 Sept. 2012

MESFET LDO: Transient Line Regulation



- Vout settles in ~2µs w/ single overshoot and undershoot
- Suggests high level of phase margin
- No output cap other than 12pF parasitic cap from scope probe

W. Lepkowski, et al., "An integrated MESFET voltage follower LDO for high power and PSR RF and analog applications," *Custom Integrated Circuits Conference (CICC), 2012 IEEE* , vol., no., pp.1-4, 9-12 Sept. 2012

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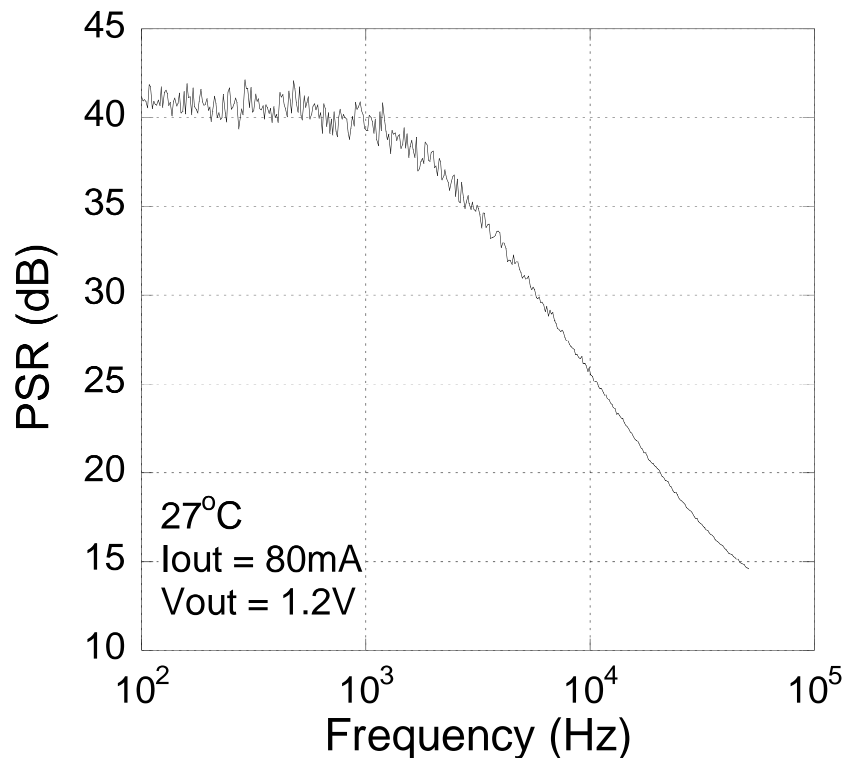
MESFET LDO: PSR



- PSR measurement includes integrated BGR
- > 40dB performance at 80mA load.
- Expect PSR to be higher at increased load currents due to higher simulated open loop gain

W. Lepkowski, et al., "An integrated MESFET voltage follower LDO for high power and PSR RF and analog applications," *Custom Integrated Circuits Conference (CICC), 2012 IEEE* , vol., no., pp.1-4, 9-12 Sept. 2012

Outline

- SJT Micropower and the SBIR program
- Silicon MESFET Overview
- High Voltage Capability
- Modeling and Measured MESFETs
- Power Applications
- RF Applications

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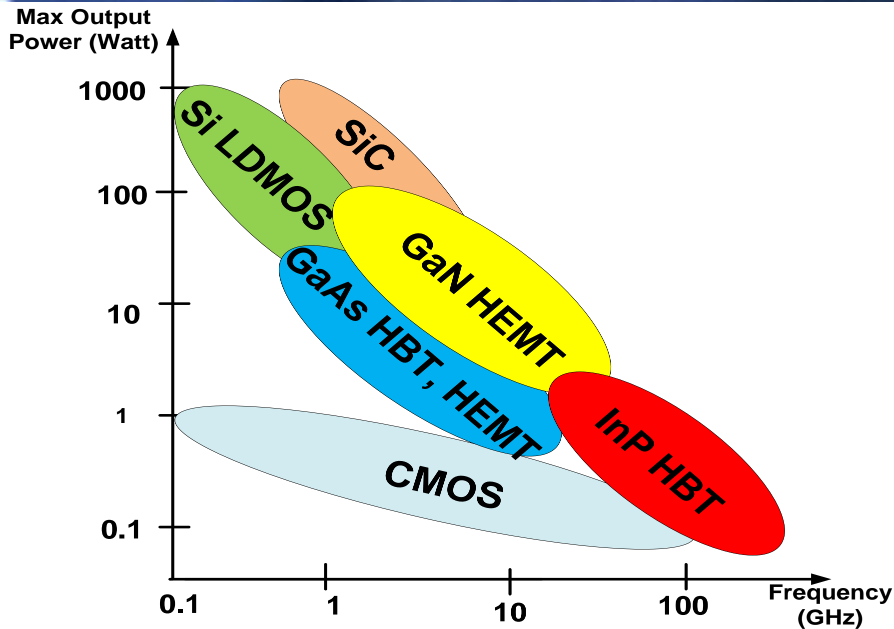
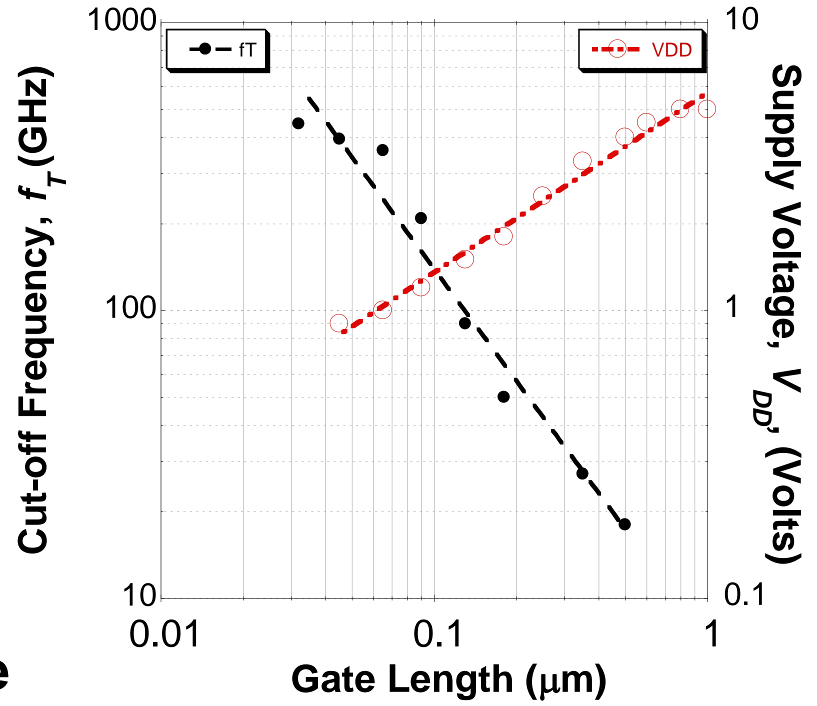
PA Integration





Standard CMOS scaling trend
(Data collected from different sources)

CMOS technology is drawing more attention for handset applications:

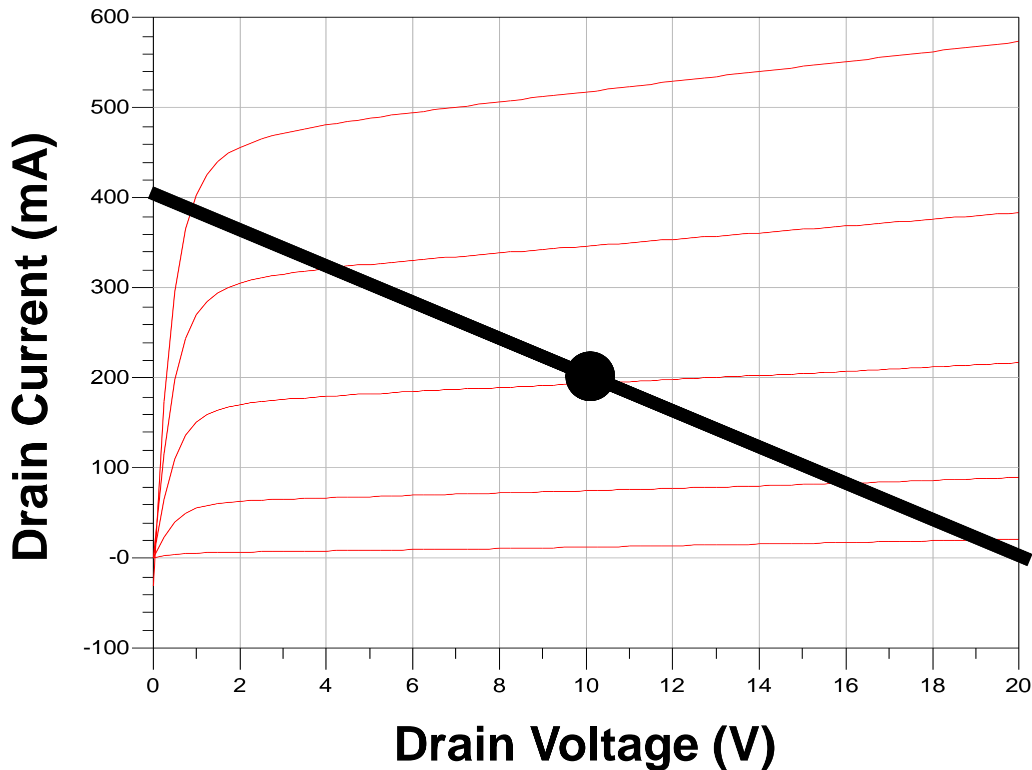
- Low cost solutions
- High integration with digital circuits
- Single chip transceiver solutions
- Easy to redesign after technology scaling
- Good modeling of silicon based components

But …It has power limitations

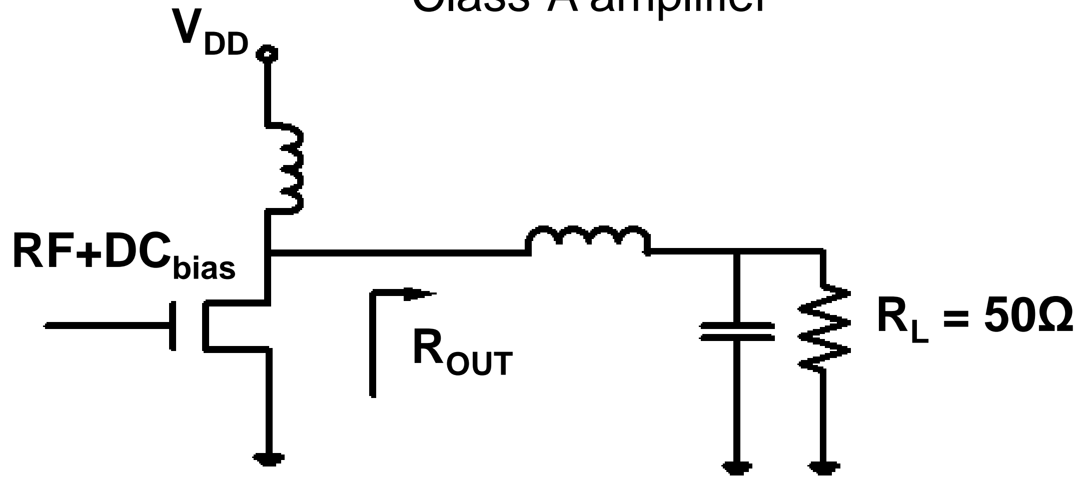
Contact: info@sjtmicropower.com

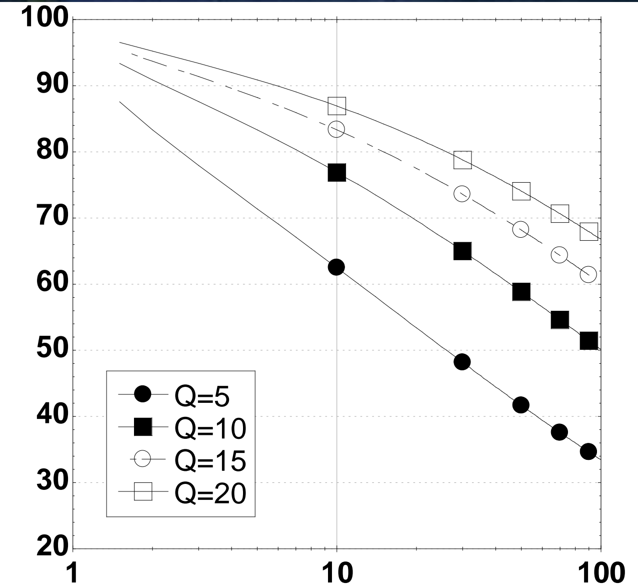
Simple Class A Amplifier Design

- P_{out} Class A = ½*i_{dc}*V_{dc} = ½* 0.2A*10V= 1W, R_{load} = V_{dc}/i_{dc} = 50Ω
- Note that if Vd of the transistor goes down, current must go up and R_{load} goes down
- For 1W if V_{dc} = 1V, i_{dc} = 2A and R_{load} = 0.5 Ω

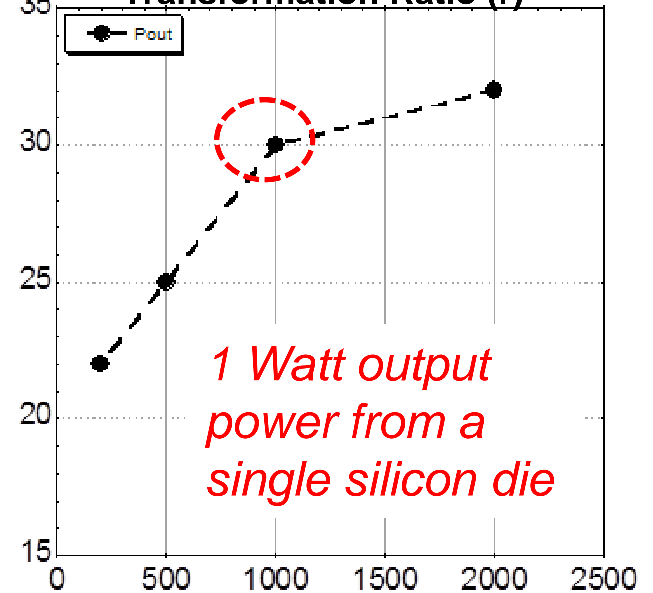


PA Efficiency Reduced by Large Impedance Transformations





- CMOS PAs may need to use large transformation ratios, $r = R_L/R_{OUT} > 10$
- A MESFET PA with $P_{out} > 1W$ can be designed to have $R_{OUT} \sim 50\ \Omega$



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There are several techniques to overcome VBD issue in CMOS technology:

- Cascode architecture (less than ~2 times improvement)
- Thick oxide transistors (~factor of 2 improvement)
- Parallel amplification (lowers the PAE)
- High voltage devices such as BiCMOS (cost, not always available on digital processes)

Proposed SOI-MESFET

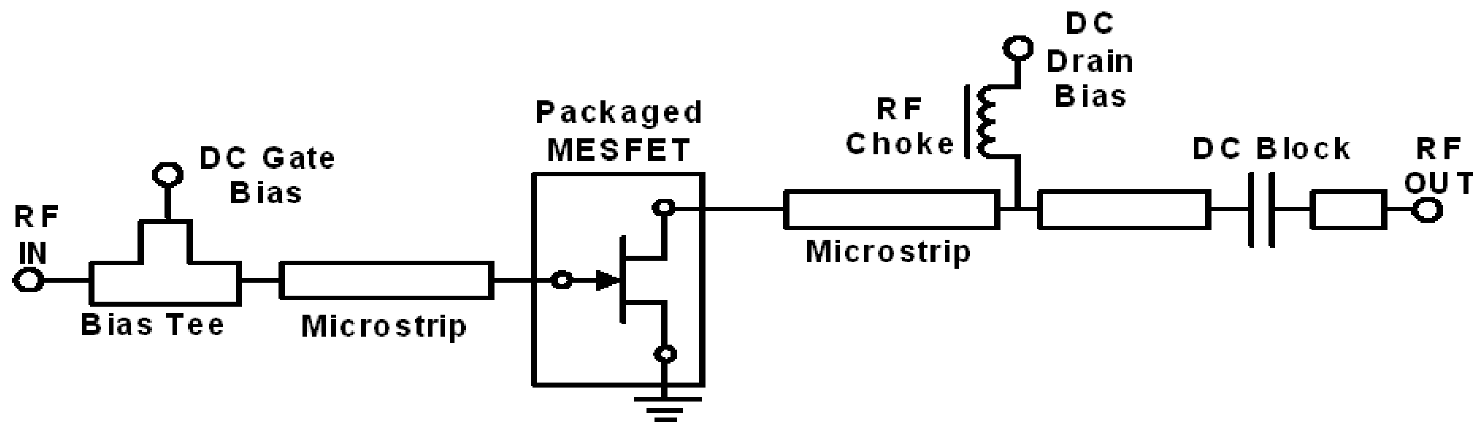
- ~2-to-10 times improvement in VBD
- No additional cost
- Available on any SOI digital process
- High enough cut-off frequency for PA design at f0<5GHz

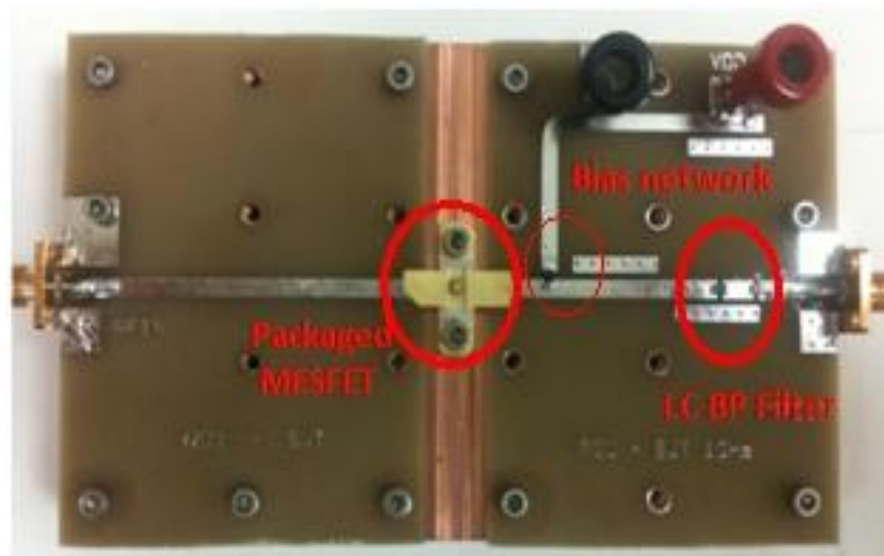
MESFET Breakdown Voltage and Cutoff Frequency

- There is a tradeoff between V_{BD} and f_T
  - Optimum device geometries found to be
    - L_{aD}=L_{aS}=500nm, L_{aS}=200nm =>> f_T=24GHz, V_{BD}=15V
    - L_{aD}=L_{aS}=2000nm, L_g=200nm =>> f_T=9GHz, V_{BD}=28V

Parameter	LAS=LAD= 500NM	LaS=LaD= 1000nm	LaS=LaD= 2000nm
Gate oxide	*No Gate Oxide*	*No Gate Oxide*	*No Gate Oxide*
L_G *(nm)*	200	200	200
L_{ext}/L_{Spacer} *(nm)*	500	1000	2000
W_{finger} *(μm)*	15	15	15
V_{BD} (V)	15	21	28
f_T (GHz)	24	17.5	9
f_{MAX} (GHz)	35	25	20
V_T (V)	-0.5	-0.5	-0.5

Simplified Circuit and Board Design





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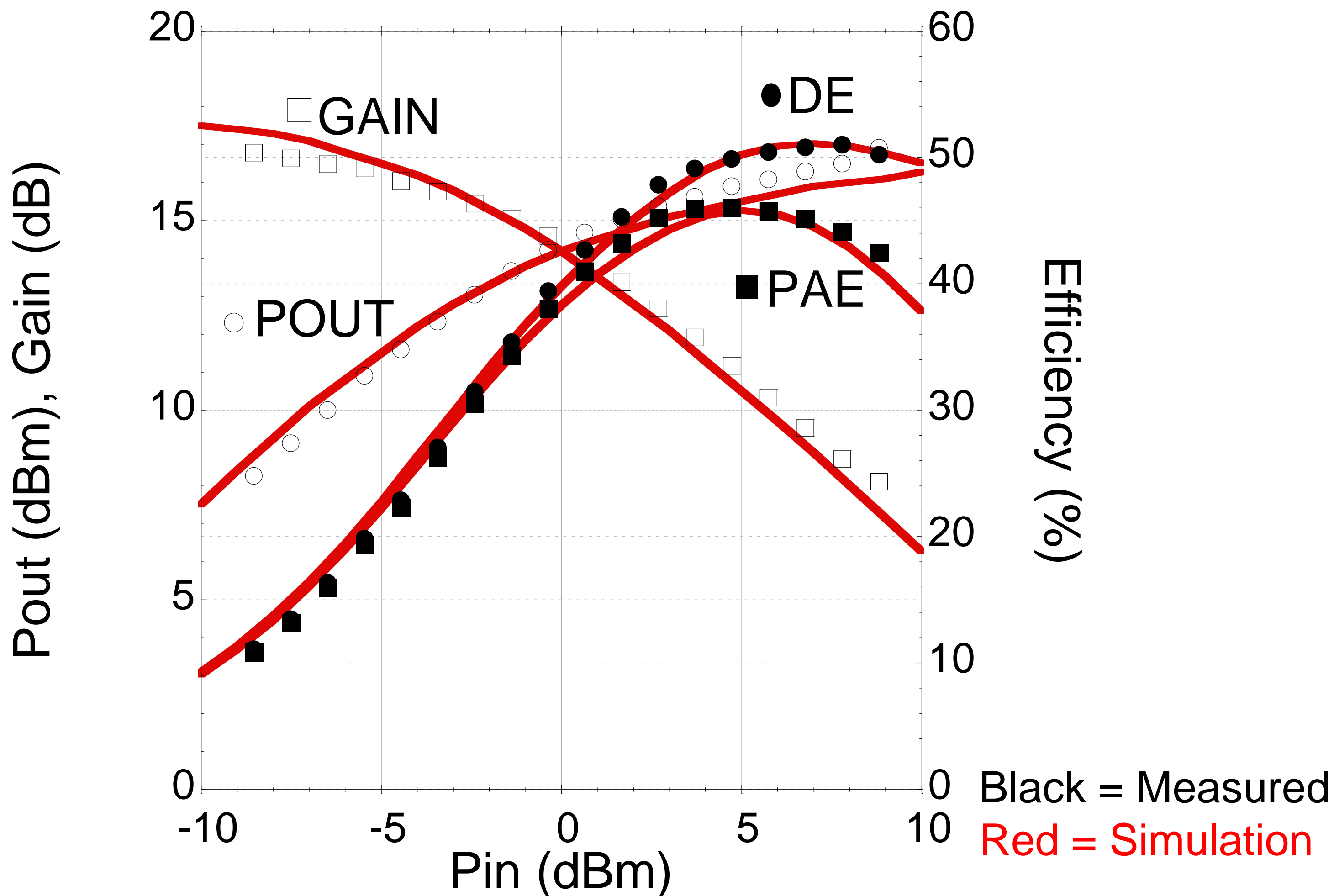
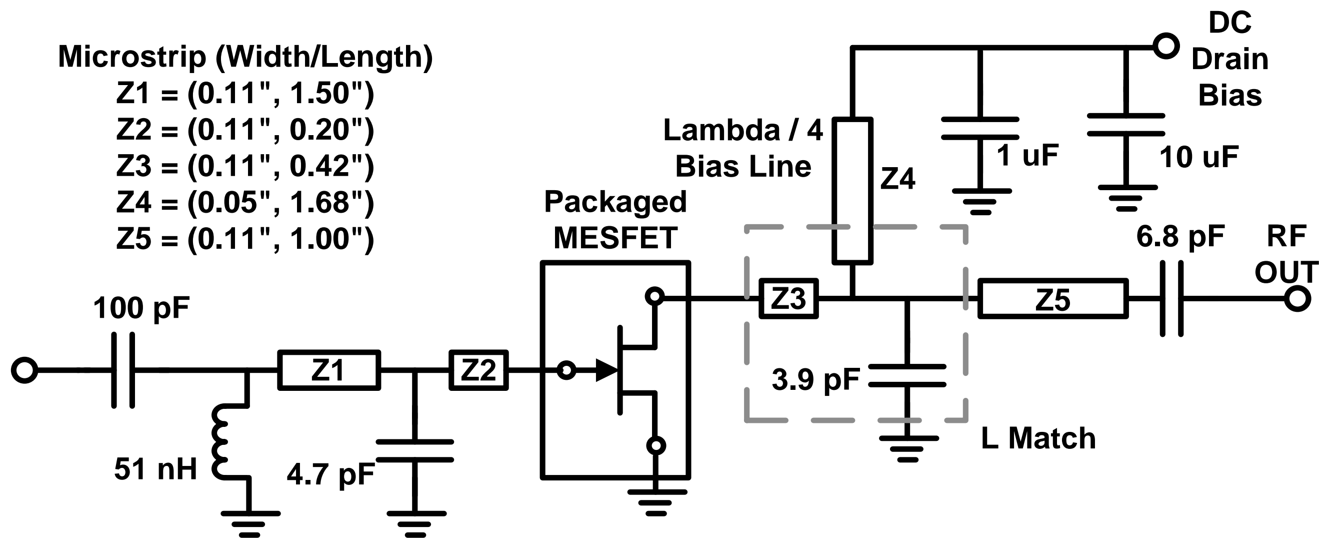
MESFET 433MHz PA Demonstration – Cont.

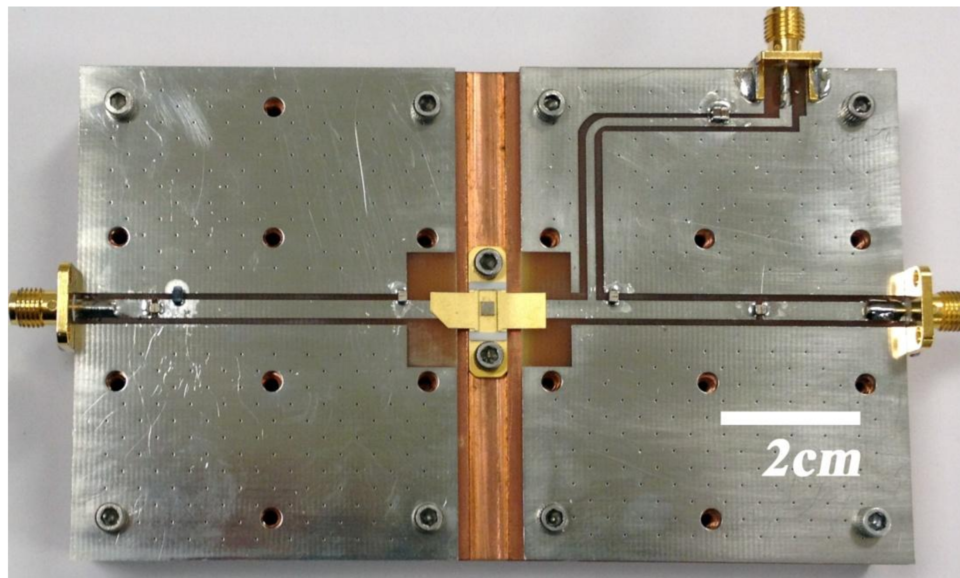


Black = Measured
Red = Simulation

- **Gain of 16.8dB**
- **Peak Pout of 17dBm with PAE of 42.5%**
- **Peak PAE 46% at Pout of 15.9dBm**

MESFET 900MHz PA Demonstration





S. J. Wilk, W. Lepkowski and T. J. Thornton, "32 dBm Power Amplifier on 45 nm SOI CMOS," IEEE Microwave and Wireless Components Letters, Accepted for publication Jan 2013.

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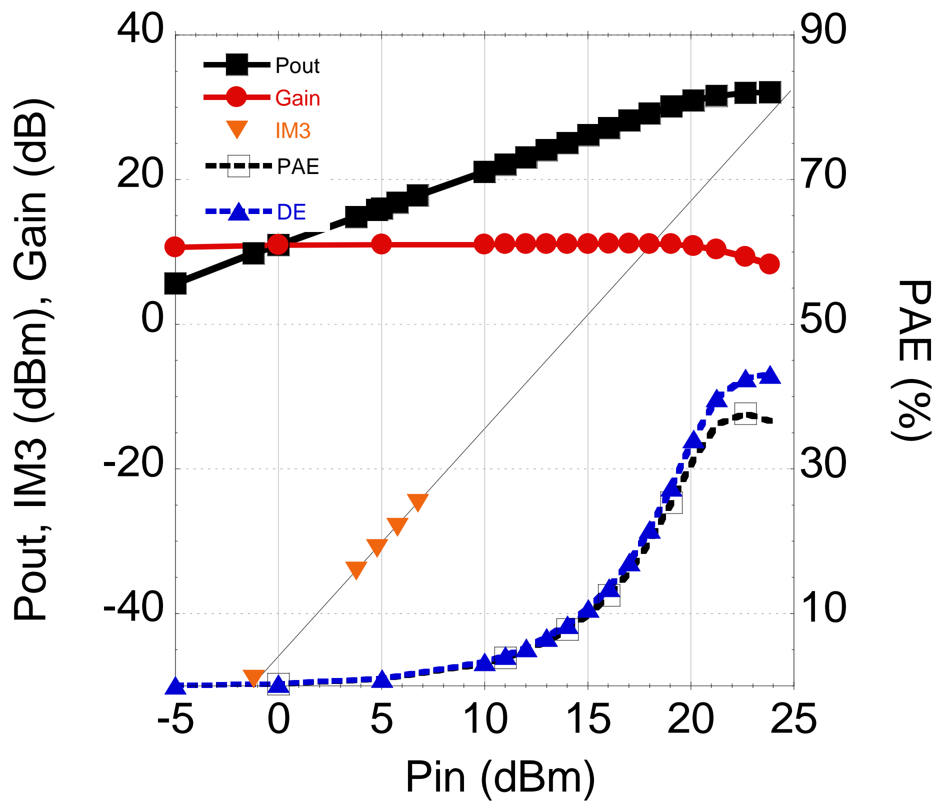
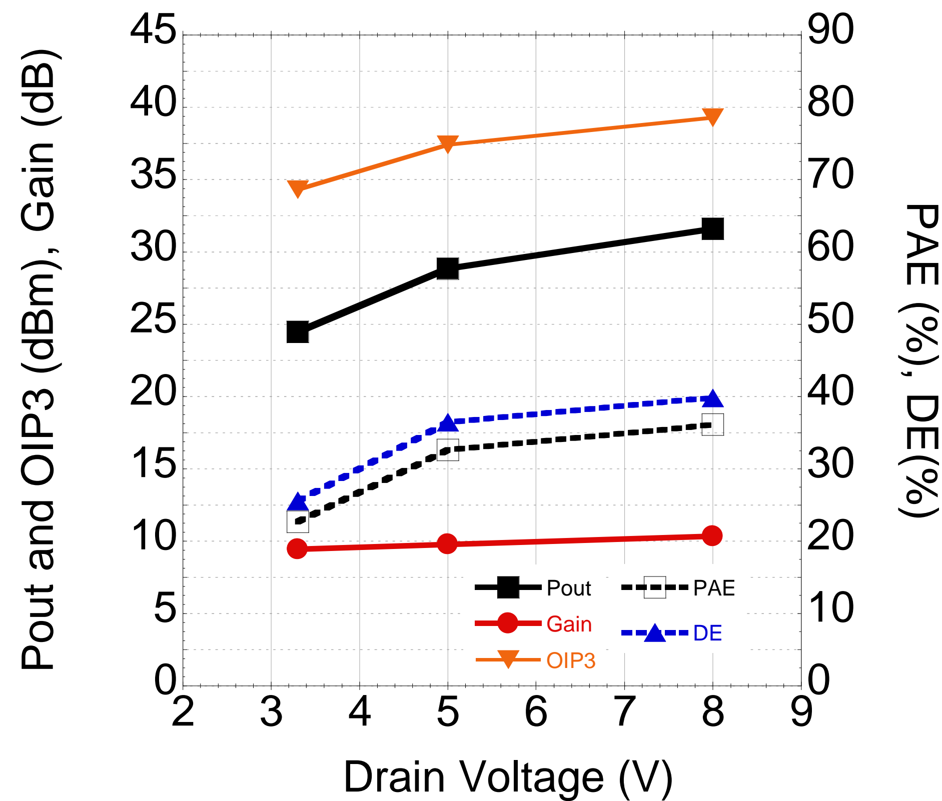
MESFET 900MHz PA Demonstration – 1.5W





- **Gain of 11.1dB**
- **Peak Pout of 32dBm**
- **Peak PAE 37.6%**
- **OIP3 of 39.3dBm**

S. J. Wilk, W. Lepkowski and T. J. Thornton, "32 dBm Power Amplifier on 45 nm SOI CMOS," IEEE Microwave and Wireless Components Letters, Accepted for publication Jan 2013.

Ongoing Research and Development Efforts

- Higher Frequency PA Measurements – Working on >2GHz and 1W PA designs along with Polar Modulation
- Development of integrated low dropout linear regulators for defense applications (supported by NASA and DARPA Phase 2 SBIR projects)
- Continued development of MESFETs on 45nm and 32nm process nodes
- Continued statistical analysis of MESFET devices and model development.

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References

S. J. Wilk, W. Lepkowski and T. J. Thornton, “32 dBm Power Amplifier on 45 nm SOI CMOS,” *IEEE Microwave and Wireless Components Letters,* Accepted for publication Jan 2013.

M.R.Ghajar, S. J. Wilk, W. Lepkowski, B. Bakkaloglu and T. J. Thornton “Backgate Modulation Technique for Higher Efficiency Envelope Tracking*” IEEE Transactions on Microwave Theory and Techniques, accepted for publication* Jan 2013.

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QUESTIONS?

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