VCO-Based Quantizers – Has Their Time Arrived?

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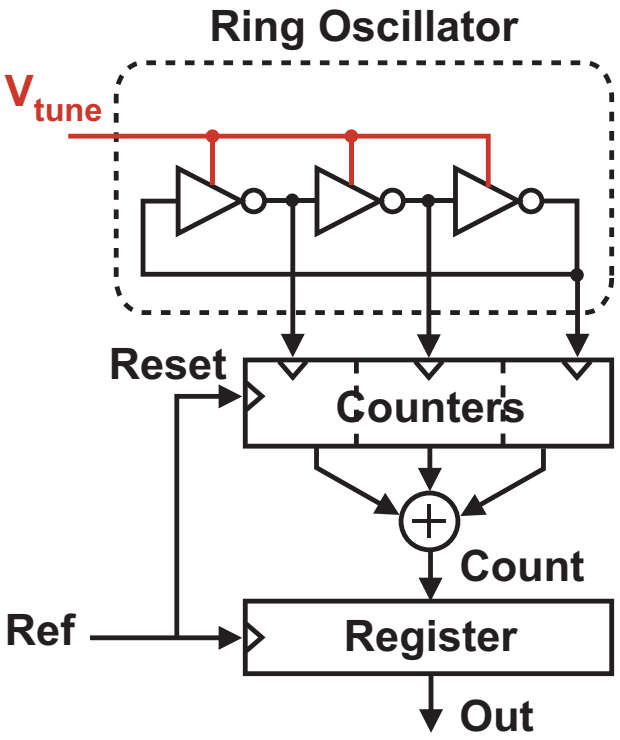
Why Should We Consider VCO-Based Quantizers?

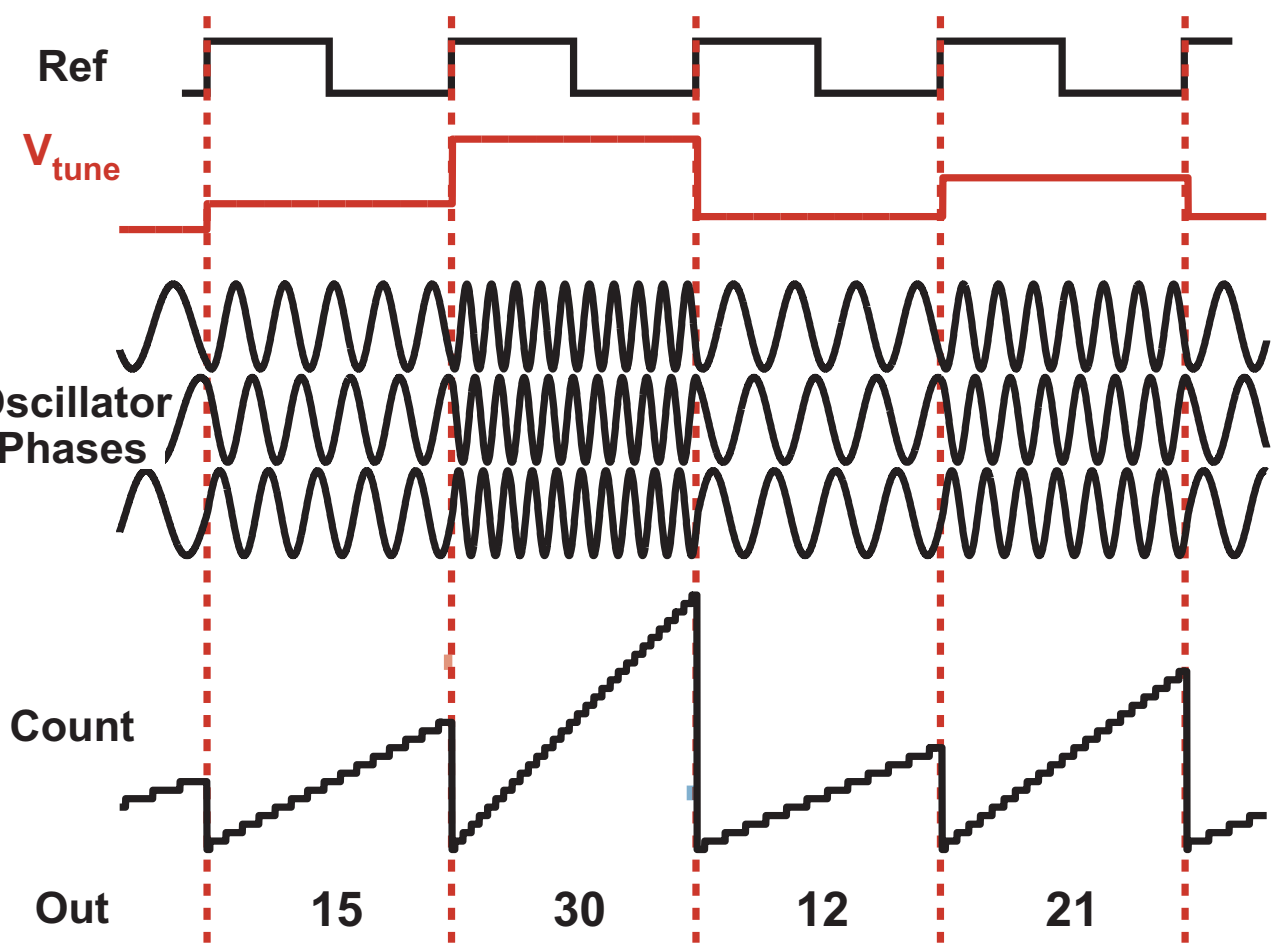
- **Advanced CMOS processes improve digital circuits**
  - **Faster speed, higher density**

- ***But,* analog circuits suffer**
  - **Reduced intrinsic device gain ($g_m r_o$)**
  - **Reduced supply voltages**

- **VCO-based quantizers utilize *time* as the signal**
  - **Take advantage of digital improvements**
  - **Offer a simple design that is high speed, multi-bit**

Using a Voltage Controlled Oscillator as an ADC

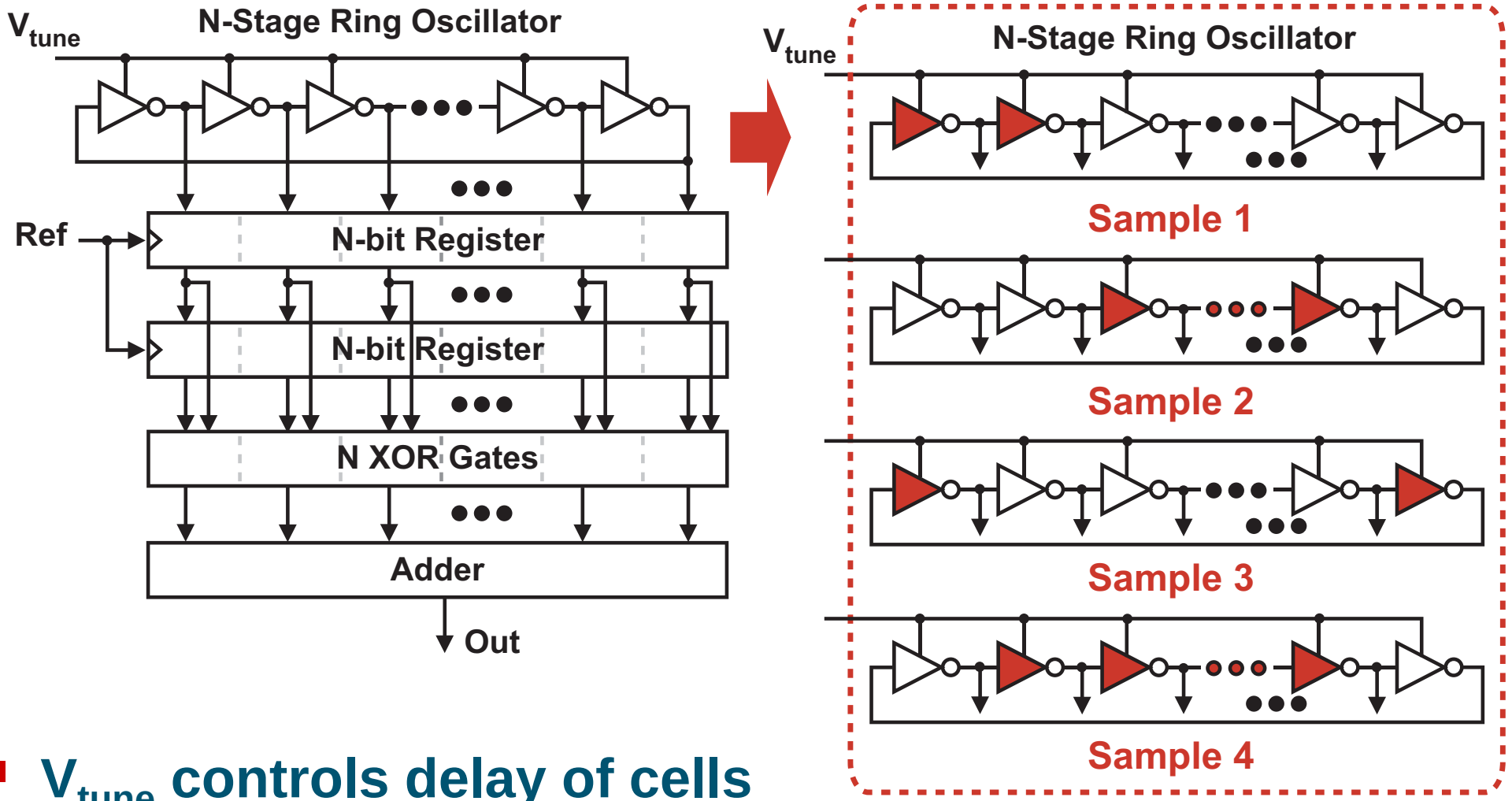




Wismar, ESSCIRC 2006
Kim, ISCAS 2006
Alon, JSSC 2005

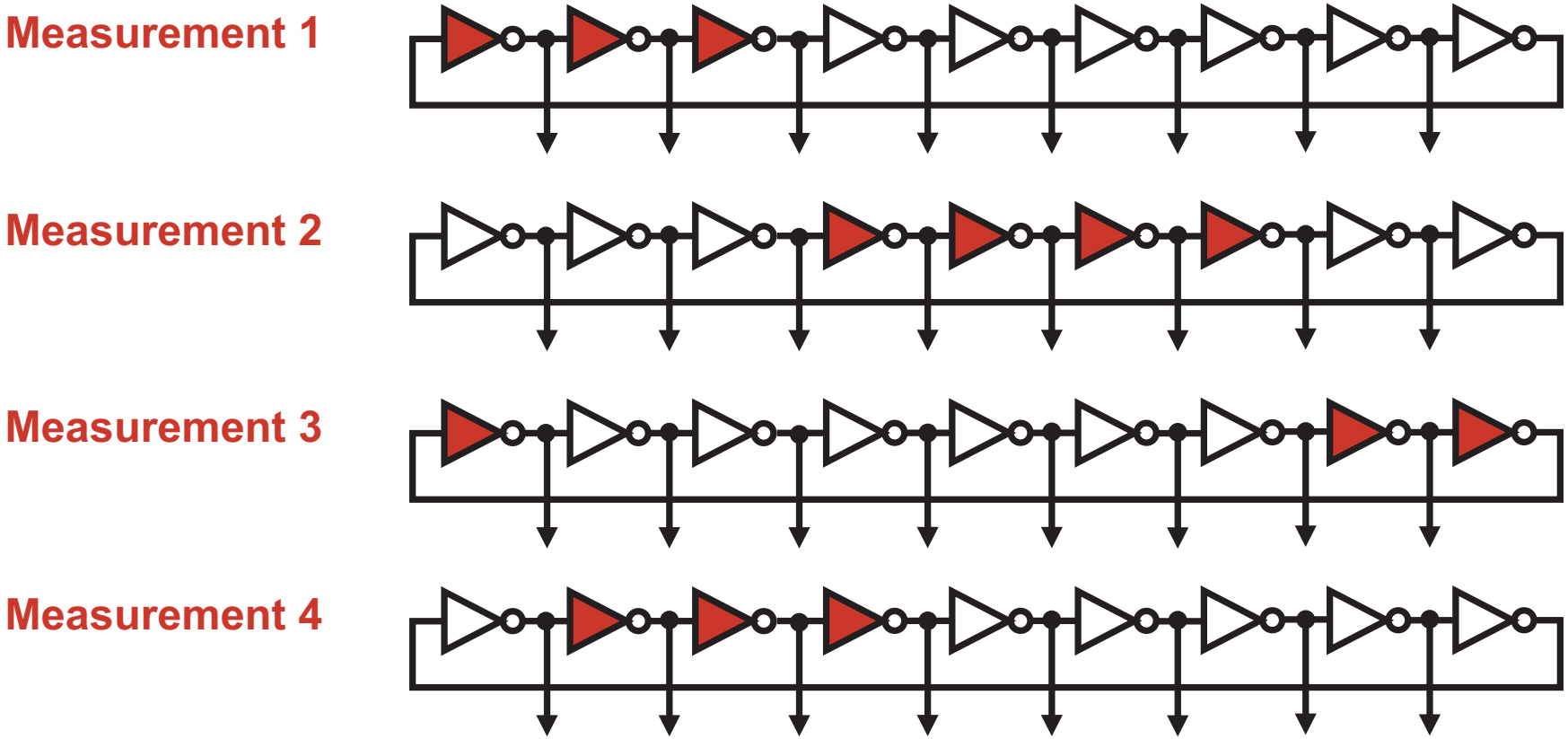
- Input: analog tuning of ring oscillator frequency
- Output: count of oscillator cycles per Ref clock period

Phase Sampling Can Be More Efficient than Counting



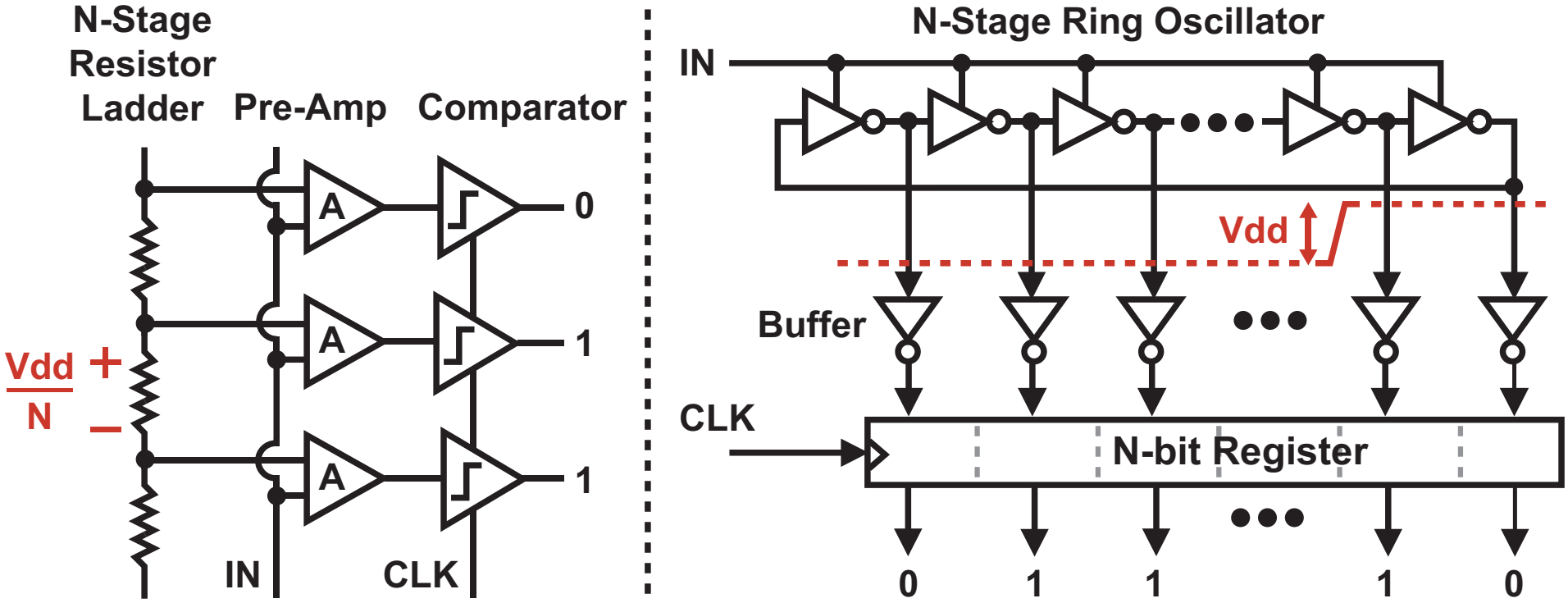
- V_{tune} controls delay of cells
  - Alters the number of transitions per ref clock period
- Digital circuits compute transition count at each sample

VCO-Based Quantizer Shapes Delay Mismatch



- Barrel shifting through delay elements
  - Mismatch between delay elements is first order shaped

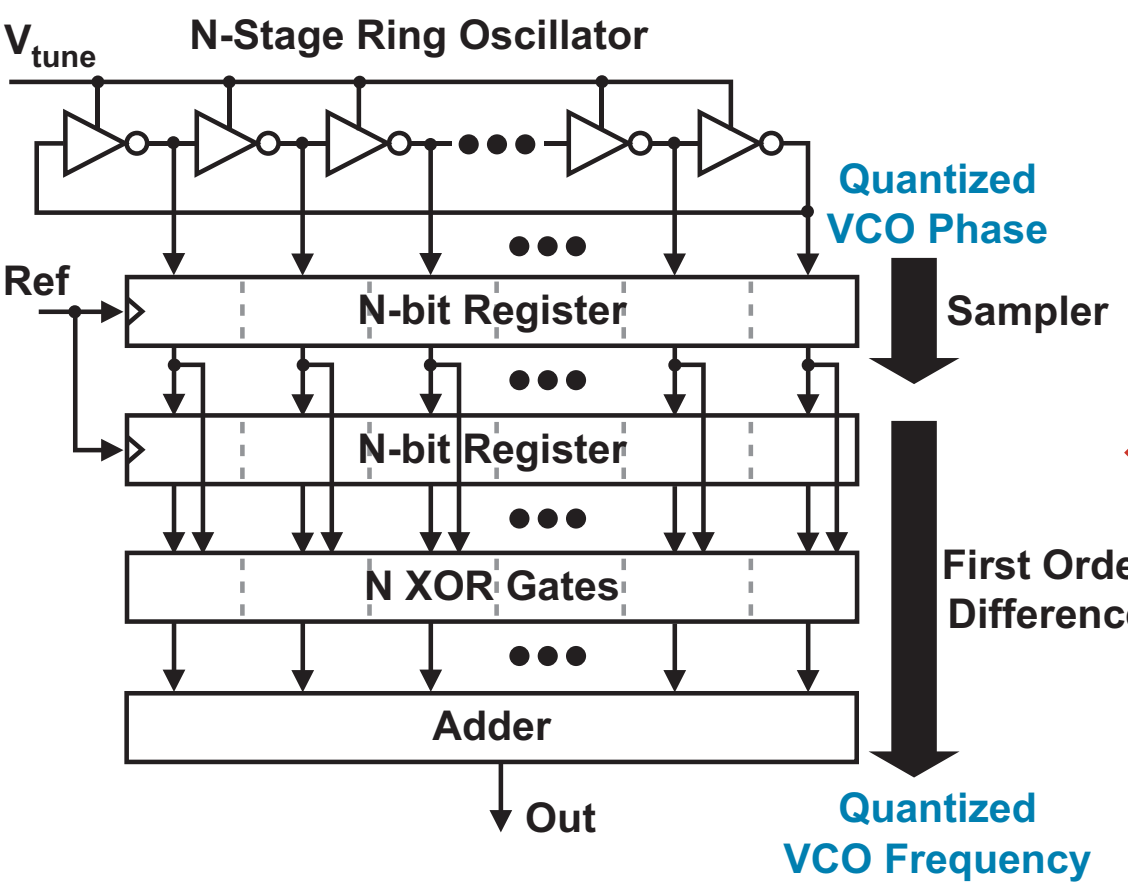
Advantages of VCO-based Quantization

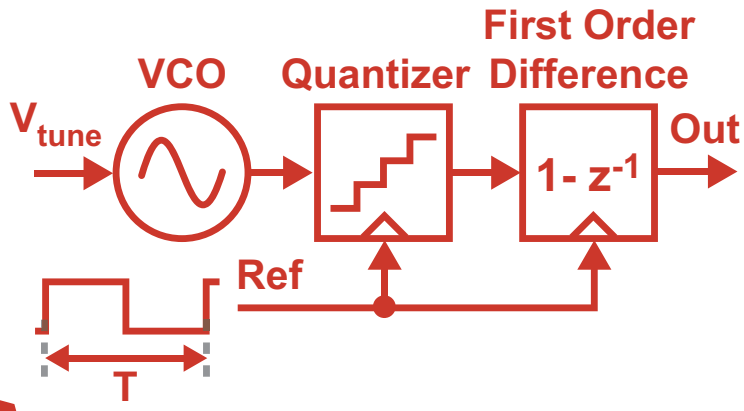


- Highly digital implementation
- Offset and mismatch is not of critical concern
- Metastability behavior is potentially improved
- SNR improves due to quantization noise shaping

Implementation is high speed, low power, low area

Modeling a VCO-Based Quantizer



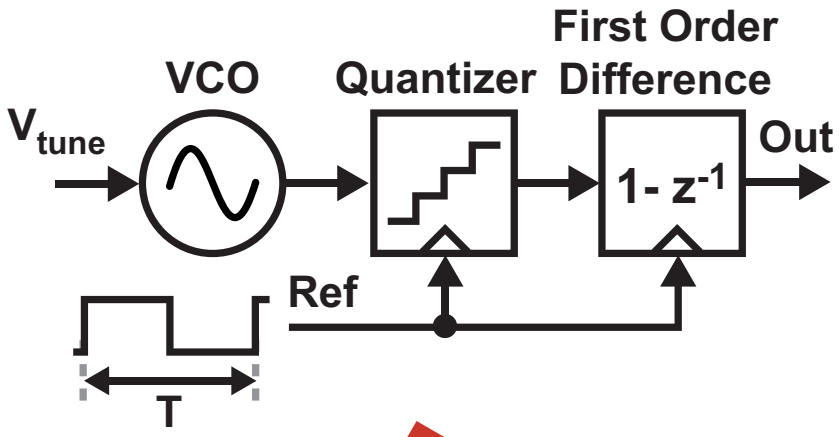


Wismar, Wisland, Andreani, ESSCIRC 2006

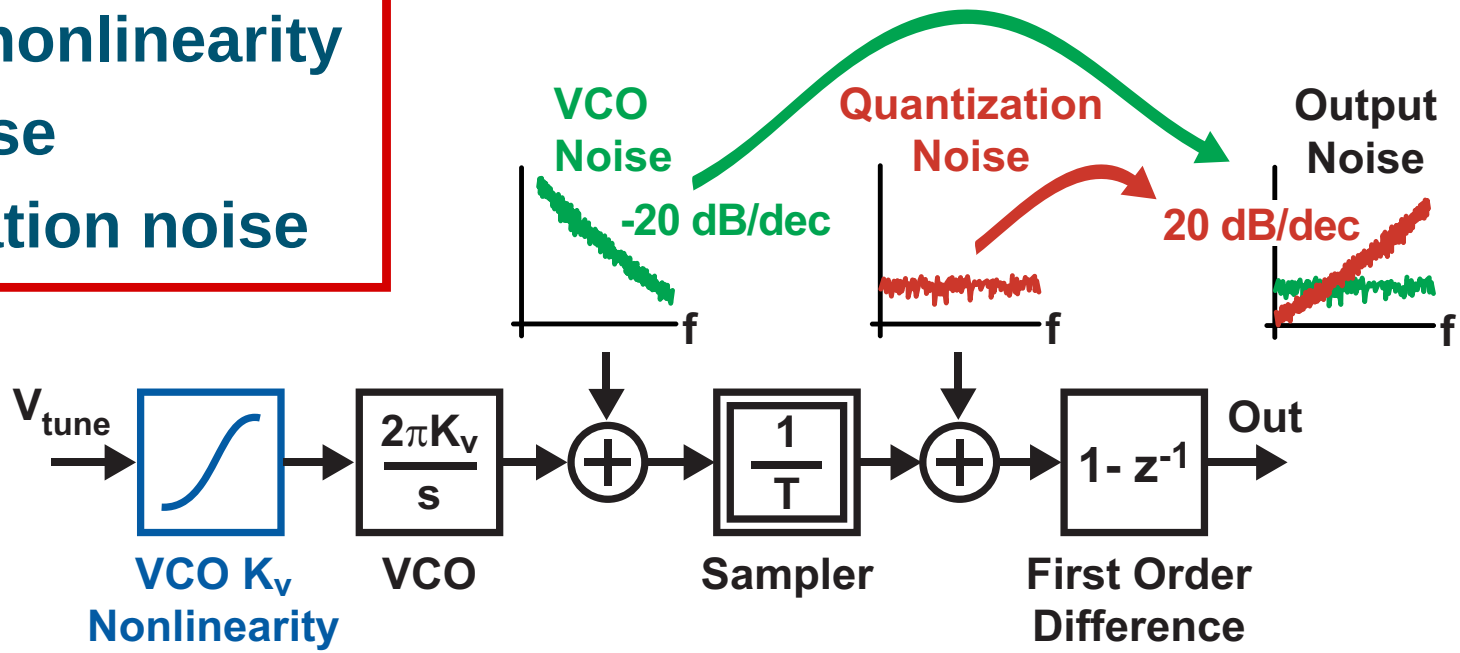
- VCO provides quantization, register provides sampling
  - Model as separate blocks for convenience
- XOR operation yields first order difference operation
  - Extracts VCO frequency from sampled VCO phase

Corresponding Frequency Domain Model

- VCO: nonlinear integrator
- Phase sampler: scale by 1/T
- Quantizer: adds noise
- First order diff: shapes noise

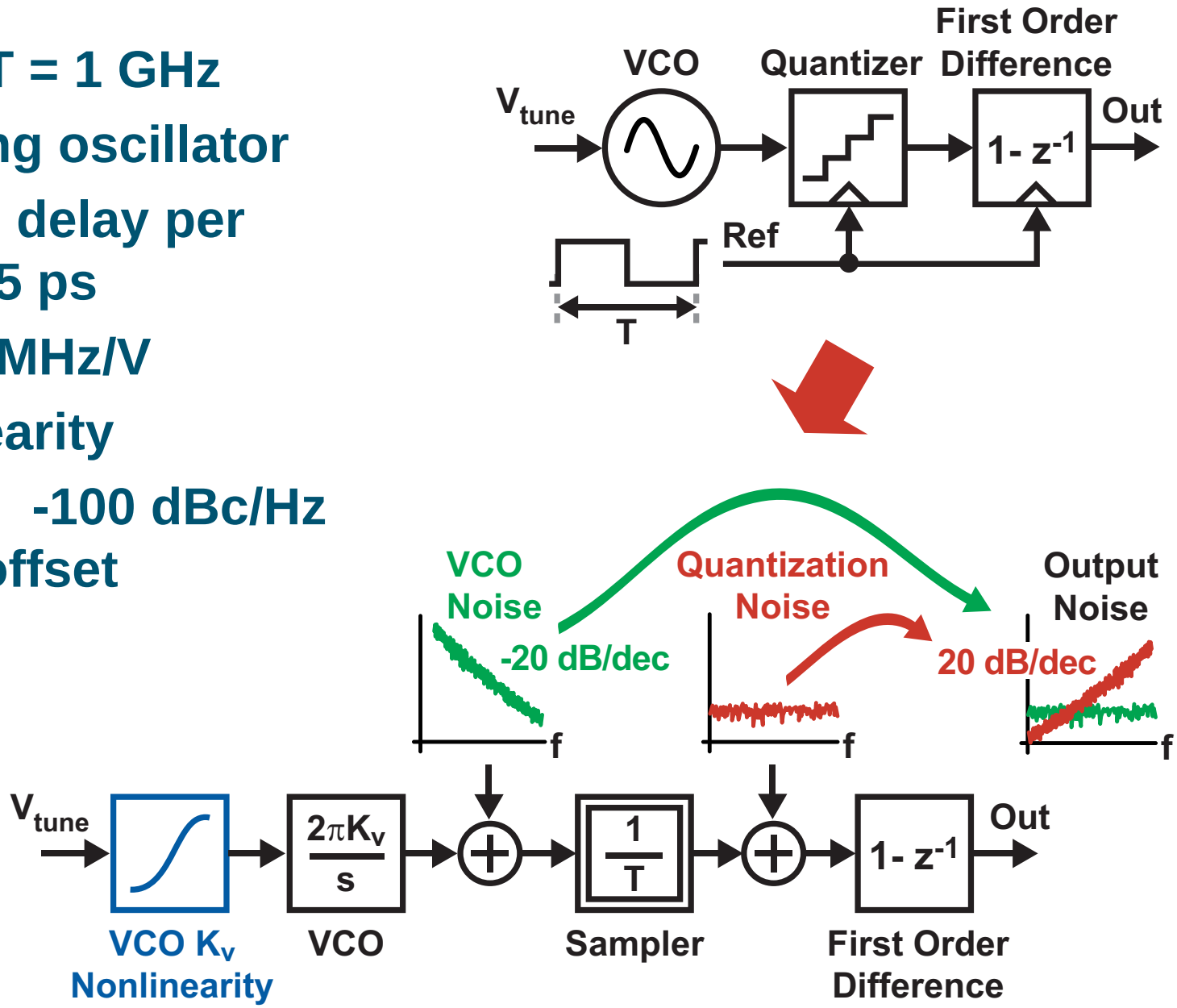


- Key non-idealities:
  - VCO K_v nonlinearity
  - VCO noise
  - Quantization noise

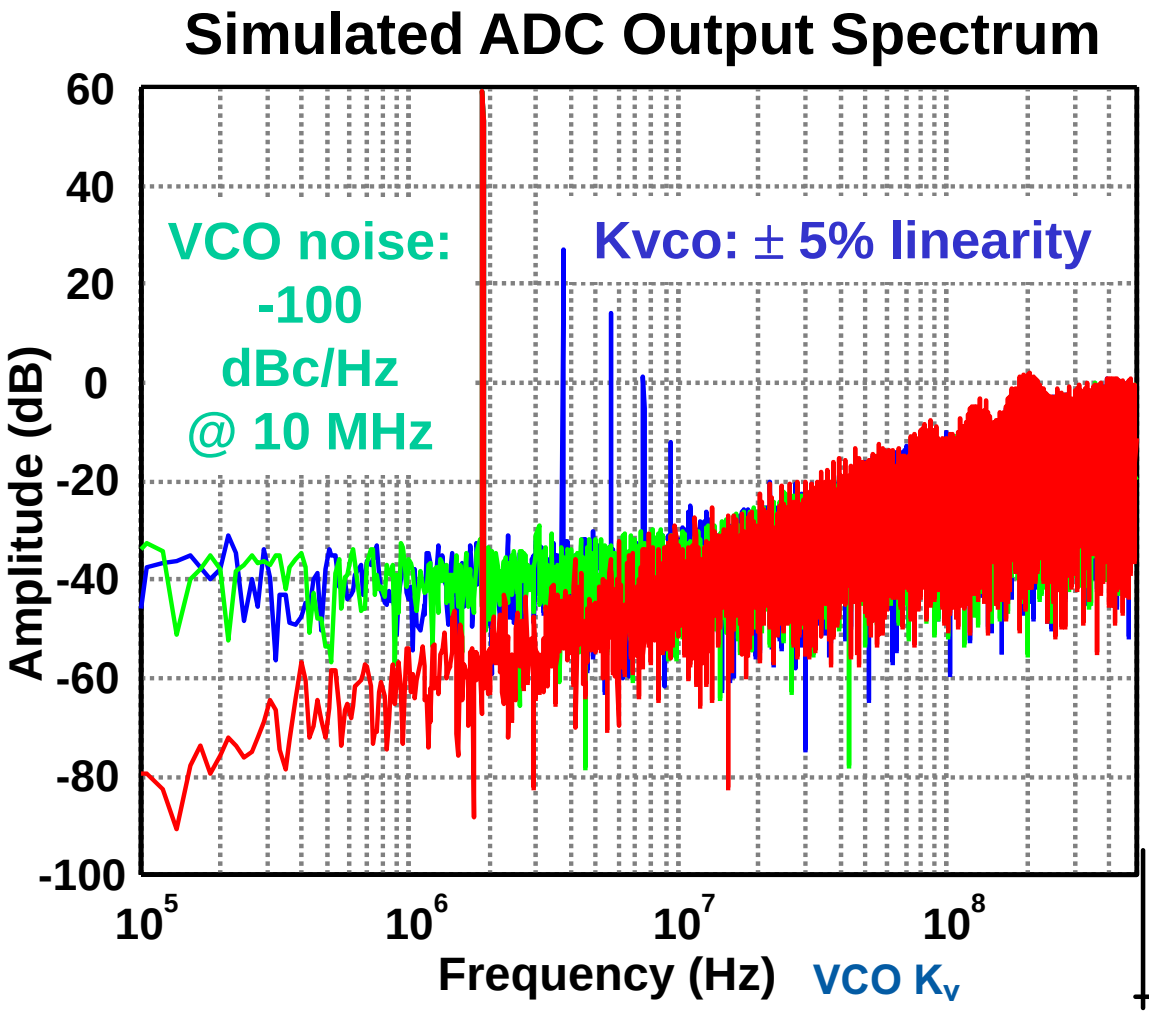


Example Design Point for Illustration

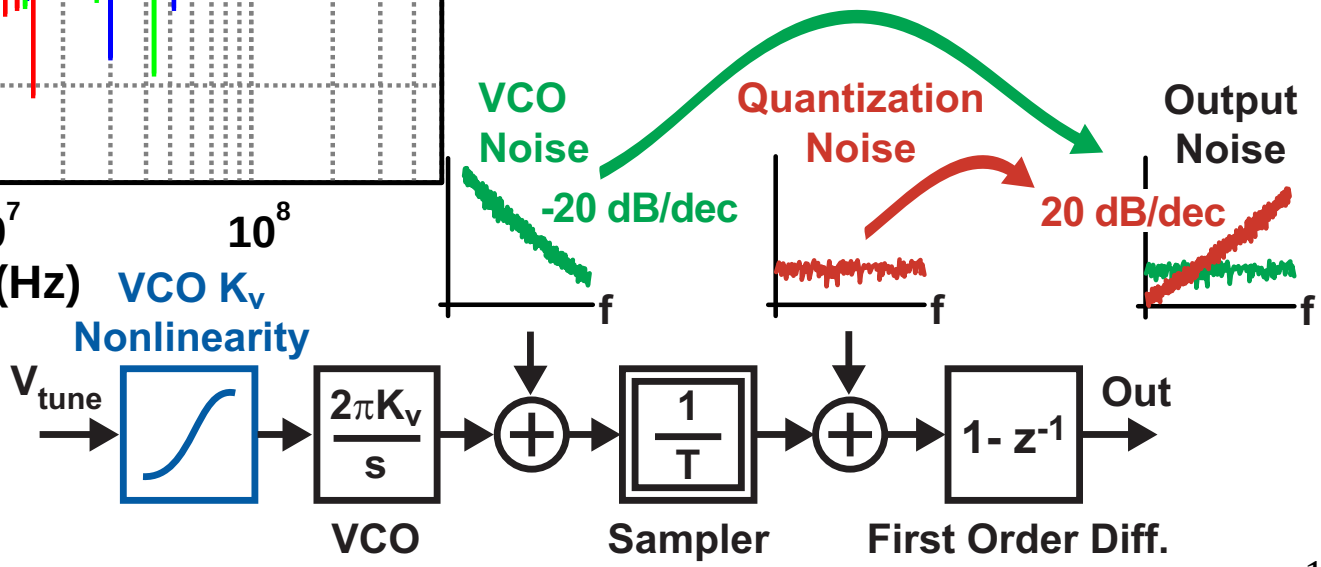
- Ref clk: 1/T = 1 GHz
- 31 stage ring oscillator
  - Nominal delay per stage: 65 ps
- K_{VCO} = 500 MHz/V
  - ±5% linearity
- VCO noise: -100 dBc/Hz at 10 MHz offset



Example SNDR with 20 MHz BW (1 GHz Sample Rate)



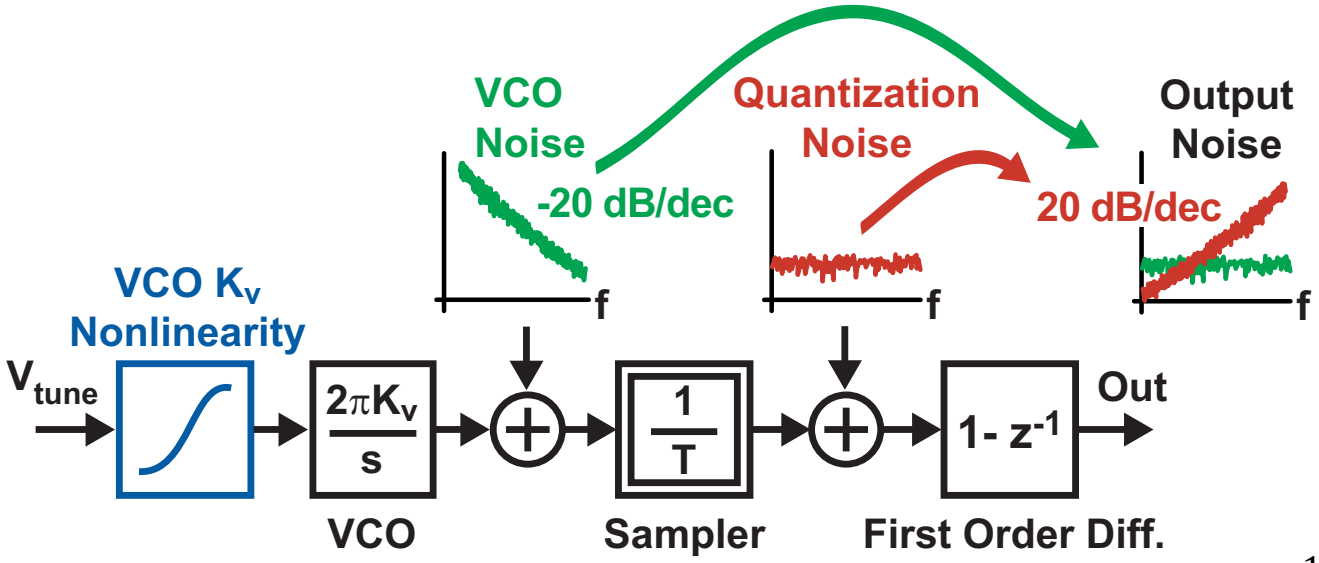
Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB



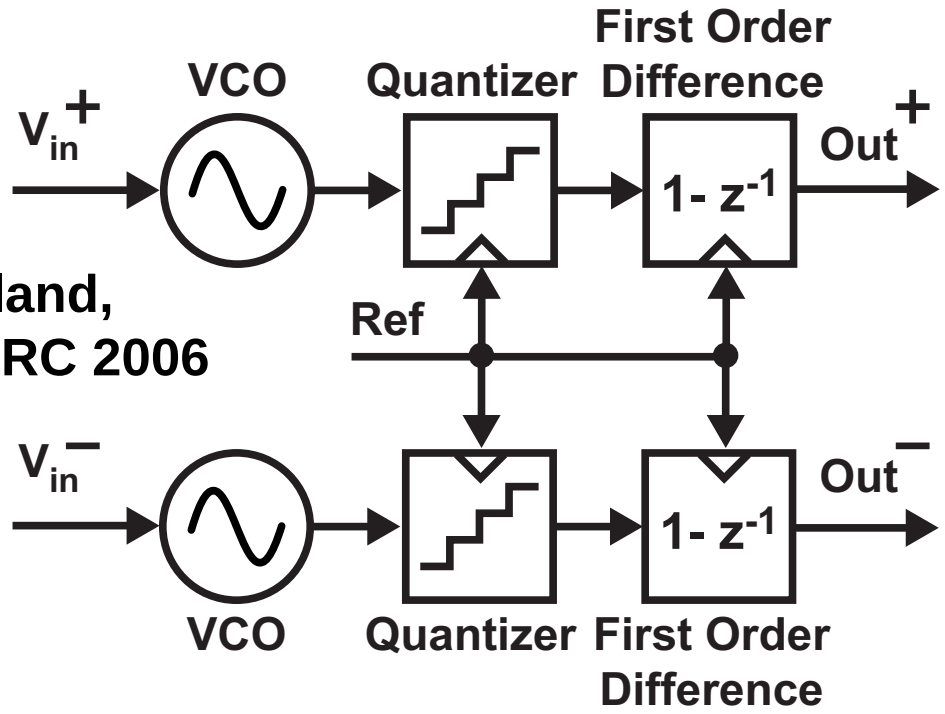
Key Issues: Nonlinearity and VCO Phase Noise

- **VCO K_v nonlinearity**
  - Limits SNDR with distortion
  - Linear K_v oscillator difficult
- **VCO phase noise**
  - Degrades SNR and SNDR
  - Improves with area/power

Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB

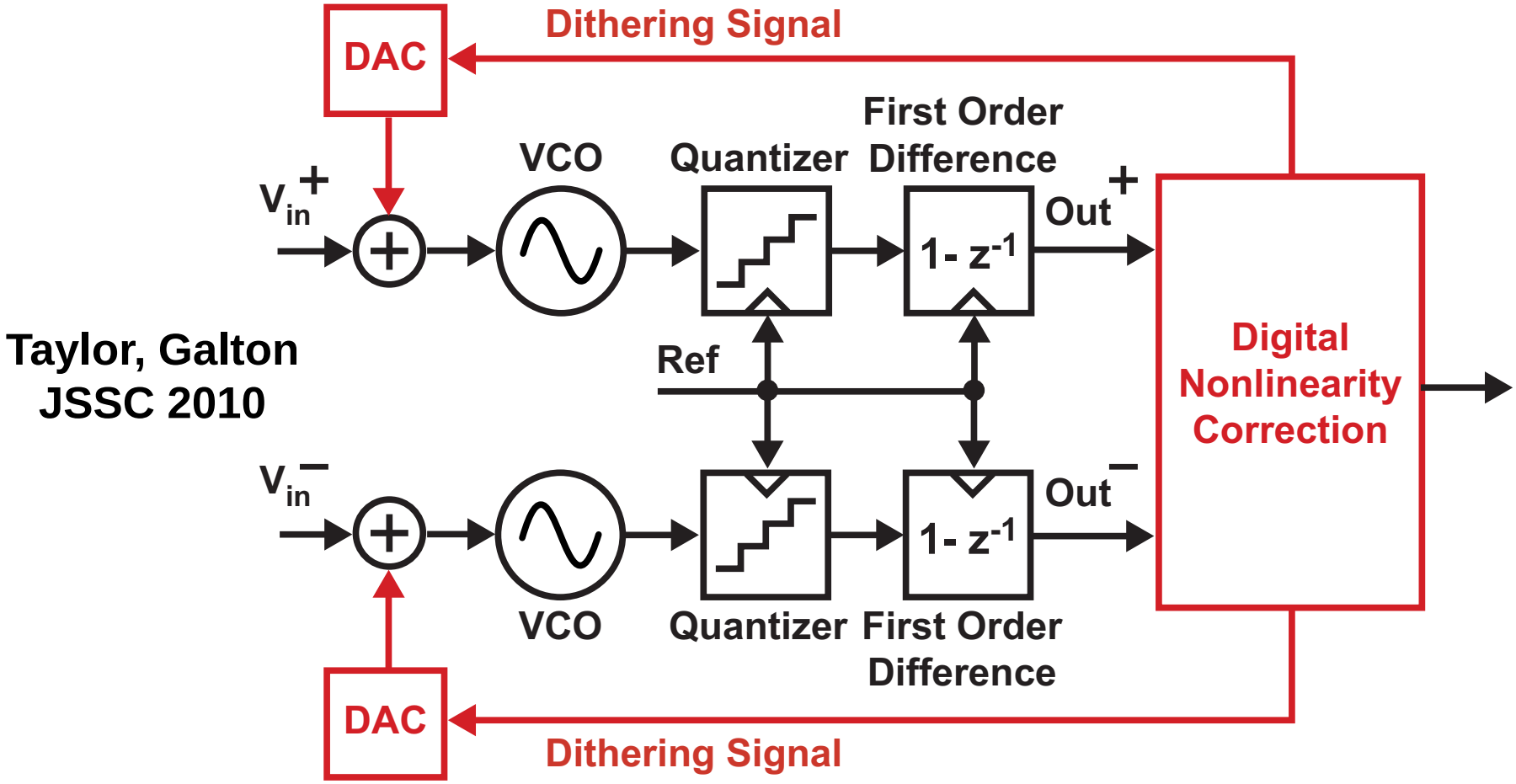


Pseudo-Differential Implementation



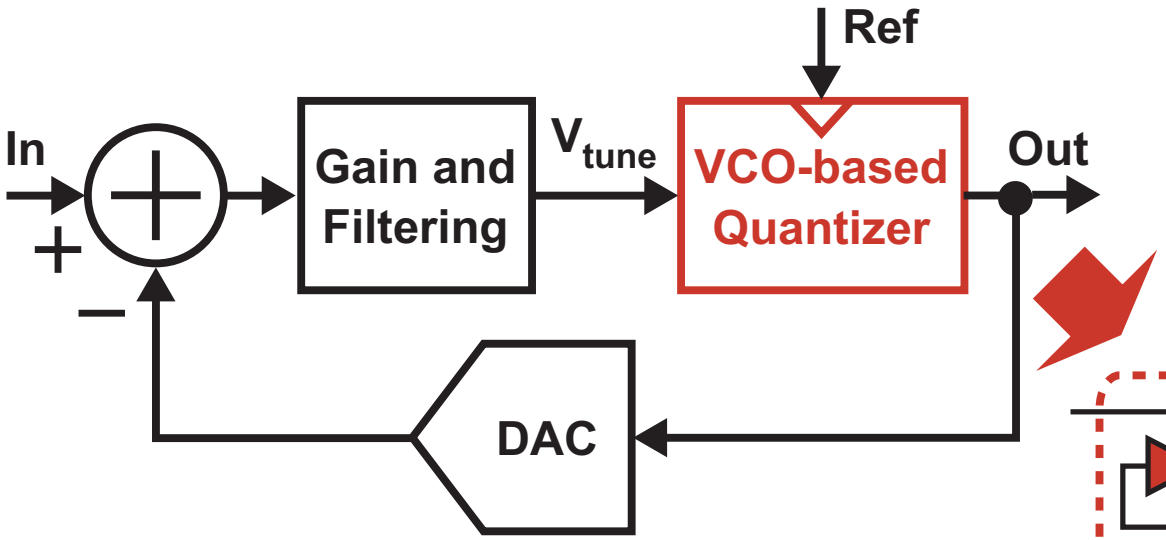
- Even order nonlinearity reduced
- VCO phase noise reduced 3dB (double area/power)
- Benchmark: 44 dB SNDR with 20 kHz BW
  - Impressive 0.2V supply, 440 nW power in 90nm CMOS

Digital Correction of Nonlinearity

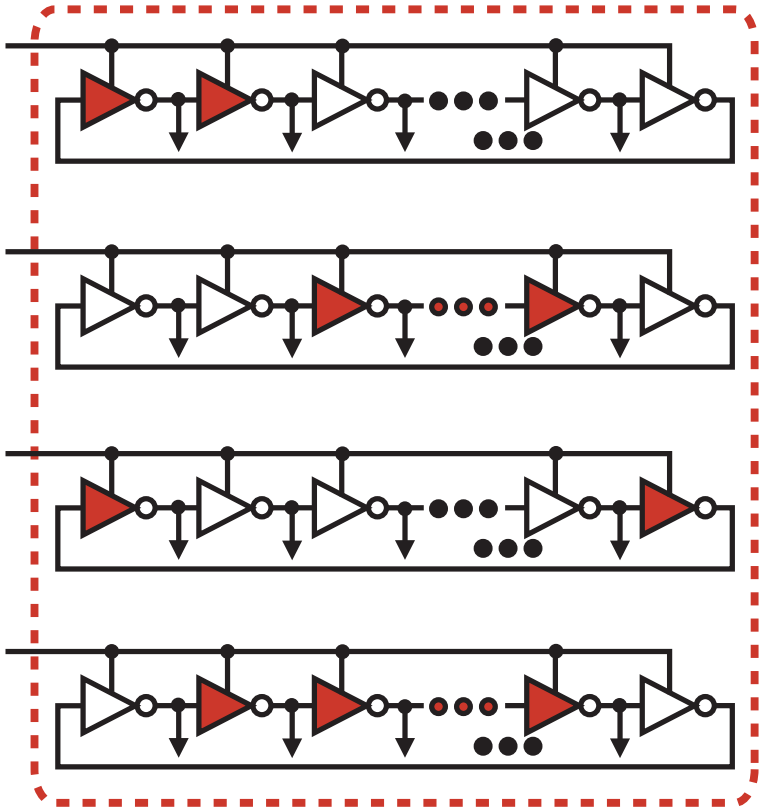


- Highly digital implementation (65nm CMOS)
  - ~70/78 dB SNDR at 18/4.5MHz BW (FOM: 297fJ/conv)
- Issues: calibration time, only first order noise shaping

Reducing the Impact of Nonlinearity using Feedback

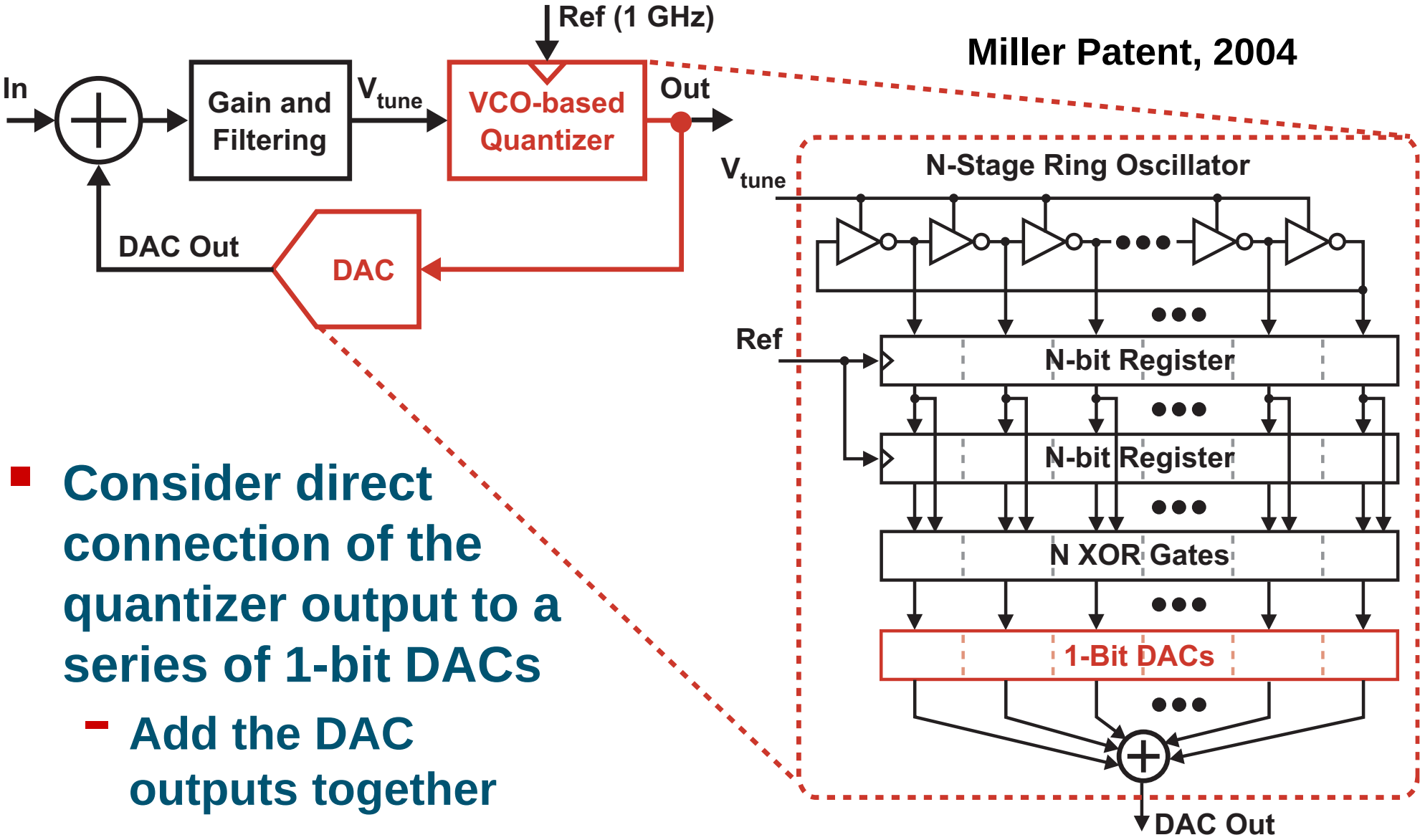


Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000



- **Continuous-time Δ–Σ ADC**
  - **VCO-based quantizer provides multi-bit implementation with first order noise shaping**
- **Gain before VCO quantizer**
  - **Suppresses VCO nonlinearity**
  - **Suppresses VCO phase noise**

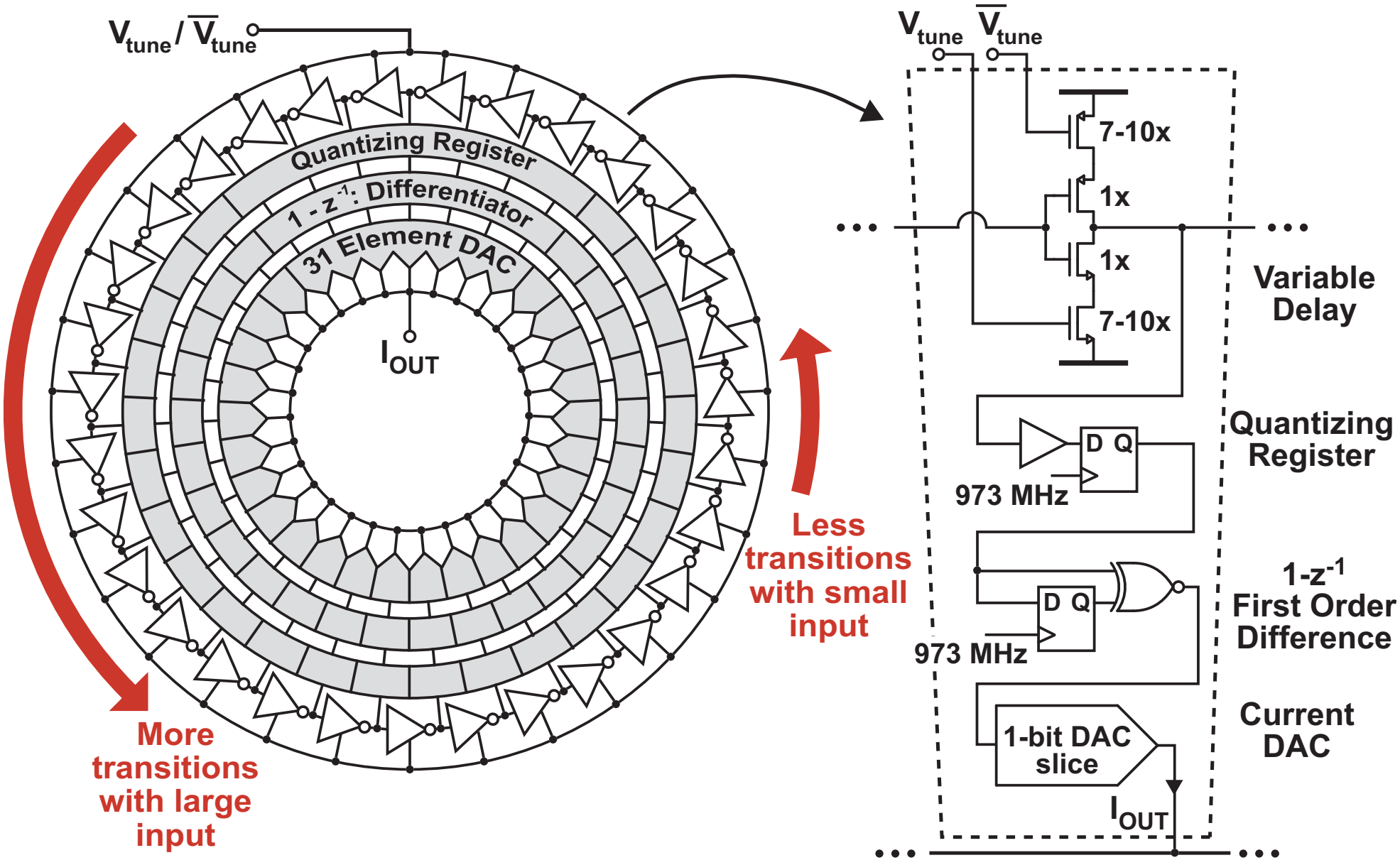
Leveraging Barrel Shifting in the Quantizer



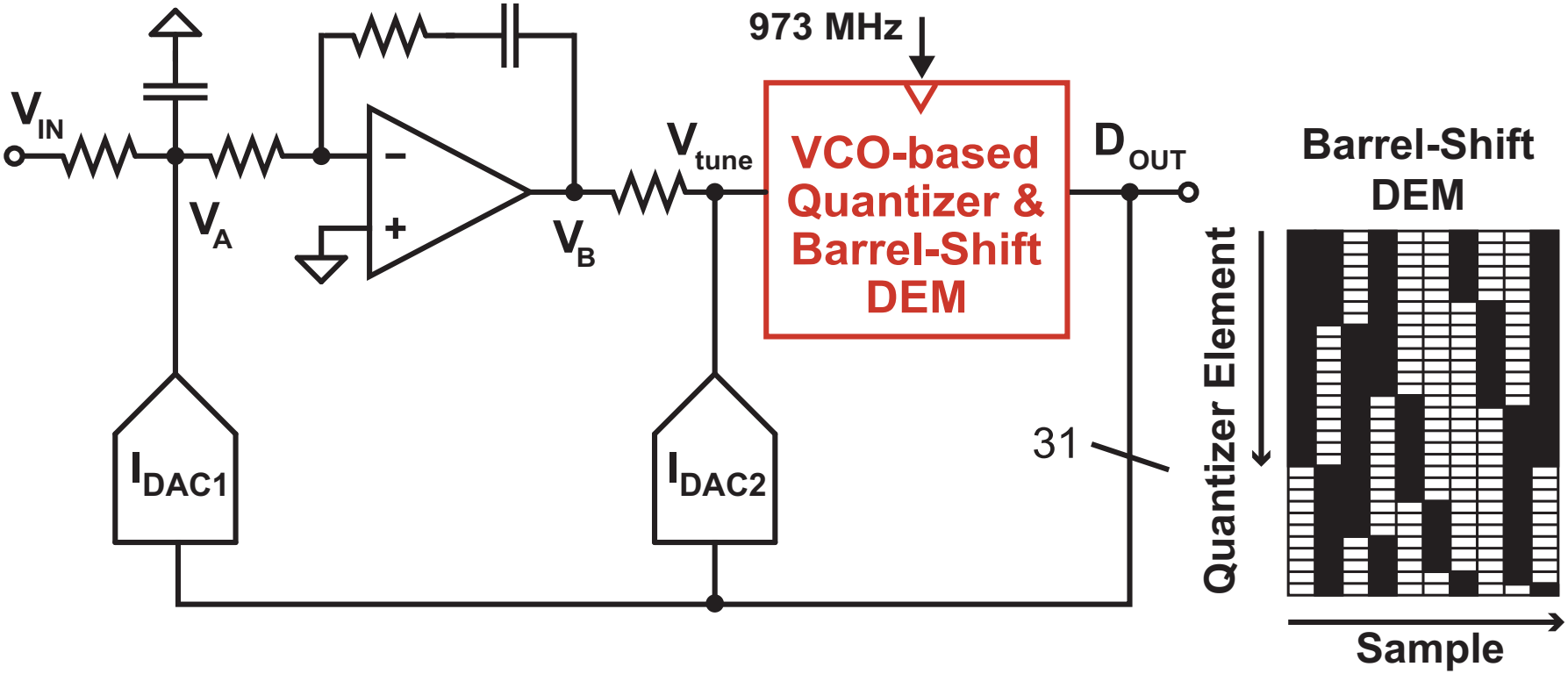
- Consider direct connection of the quantizer output to a series of 1-bit DACs
  - Add the DAC outputs together

Intrinsic barrel shifting of the DAC elements is achieved!

A Geometric View of the VCO Quantizer/DEM and DAC

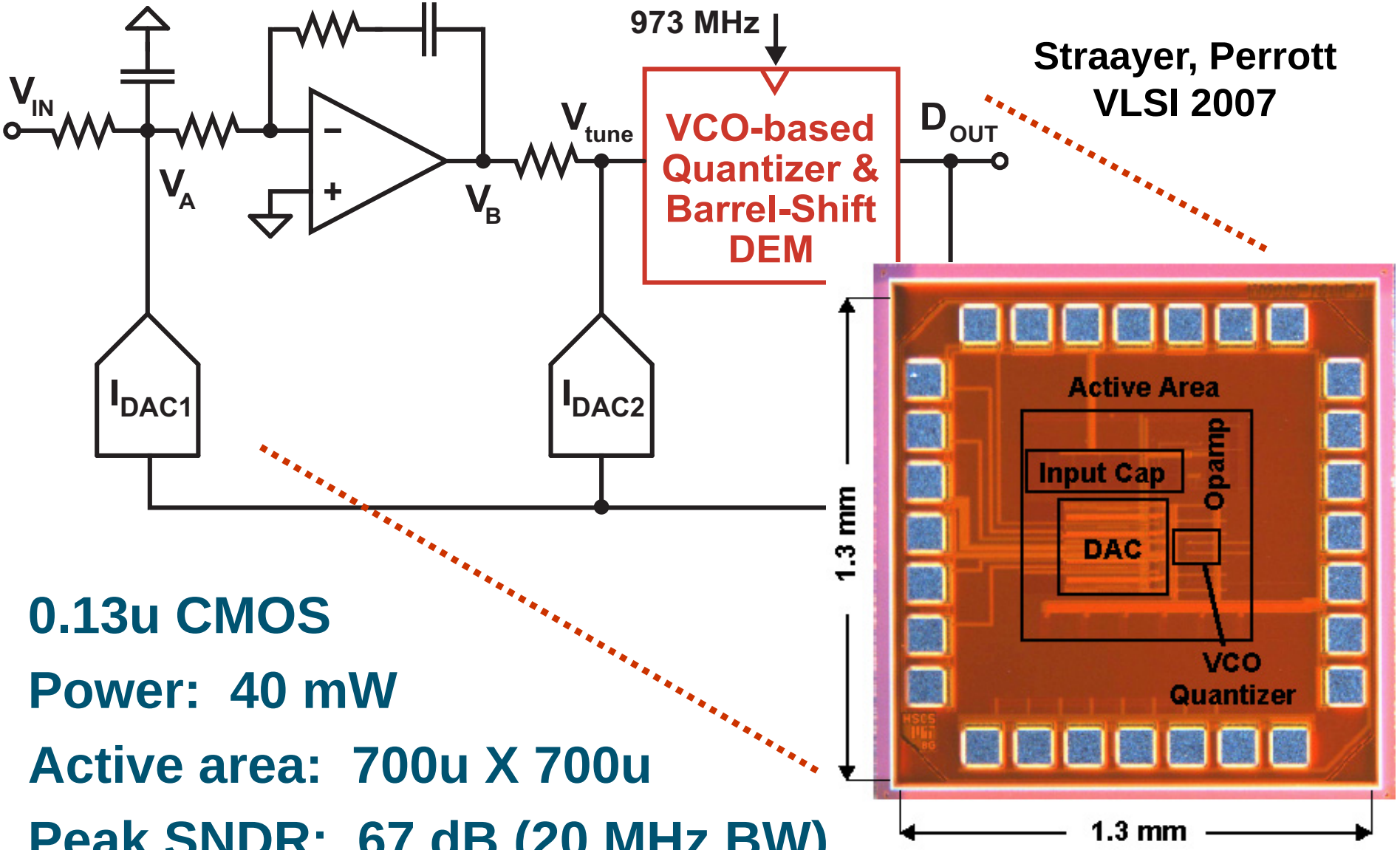


A Second Order Continuous-Time Delta-Sigma ADC



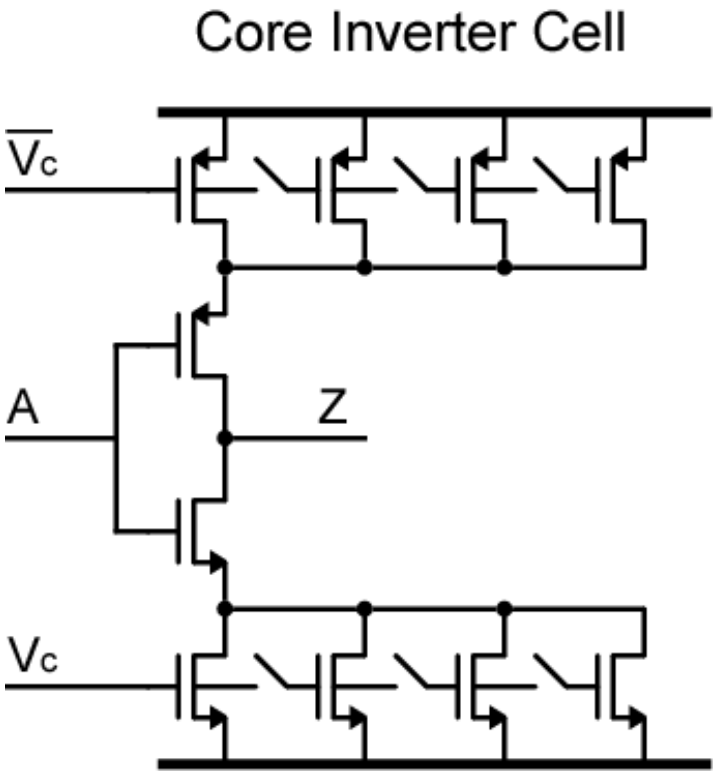
- ***Second order dynamics*** **achieved with only** ***one*** **op-amp**
  - **Op-amp forms one integrator**
  - **I_{dac1} and passive network form another (lossy) integrator**
  - **Minor loop feedback compensates for quantizer delay**
- ***Third order noise shaping*** **due to VCO-based quantizer**

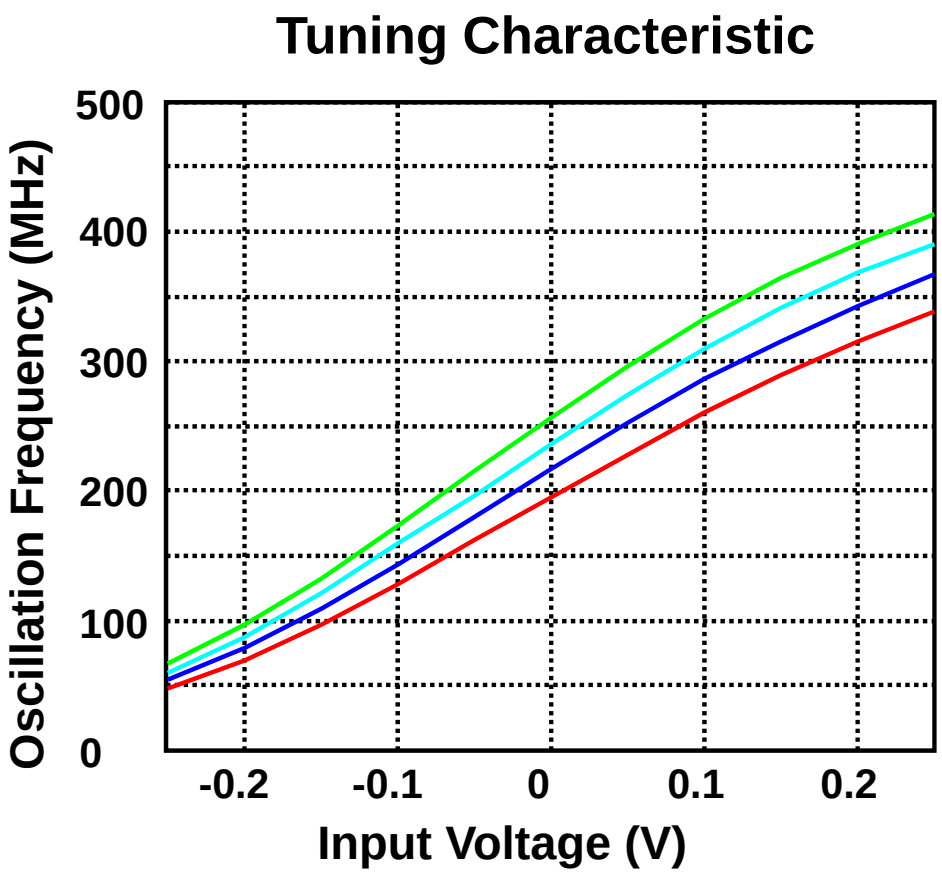
Custom IC Implementing the Prototype



- 0.13u CMOS
- Power: 40 mW
- Active area: 700u X 700u
- Peak SNDR: 67 dB (20 MHz BW)
- Efficiency: 0.5 pJ/conv. step

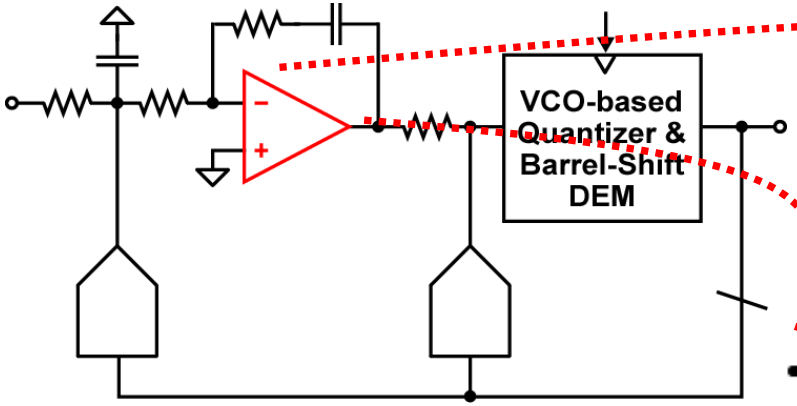
Design of the VCO Core Inverter Cell





- 31 stages
- Fast for good resolution (< 100 psec / stage)
- Large K_{VCO} (600-700 MHz) with good dynamic range
- 2 bits of coarse tuning for process variations
- < 8 mW for 1 GSPS 5-bit quantizer / DEM

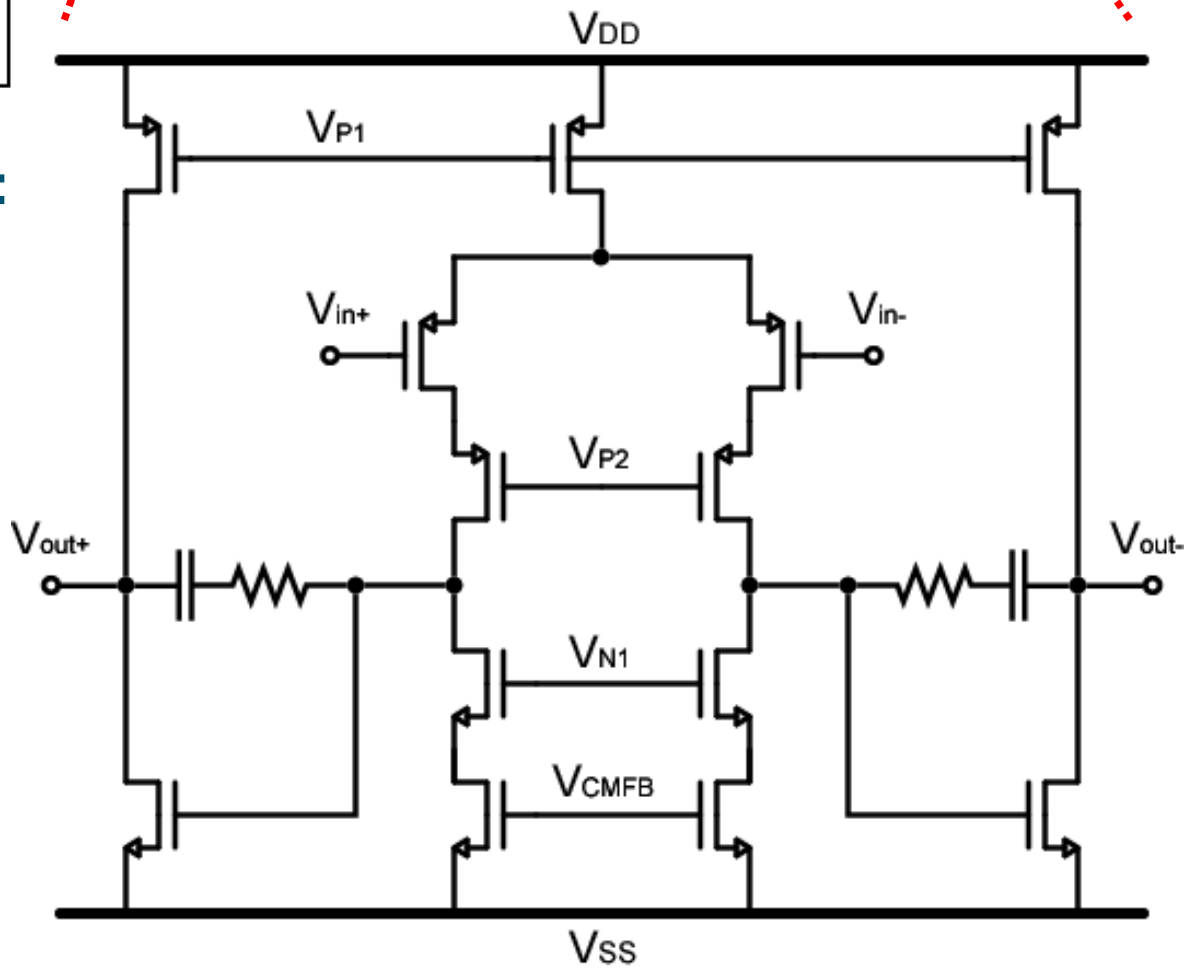
Opamp Design is Straightforward



Simulated Performance:

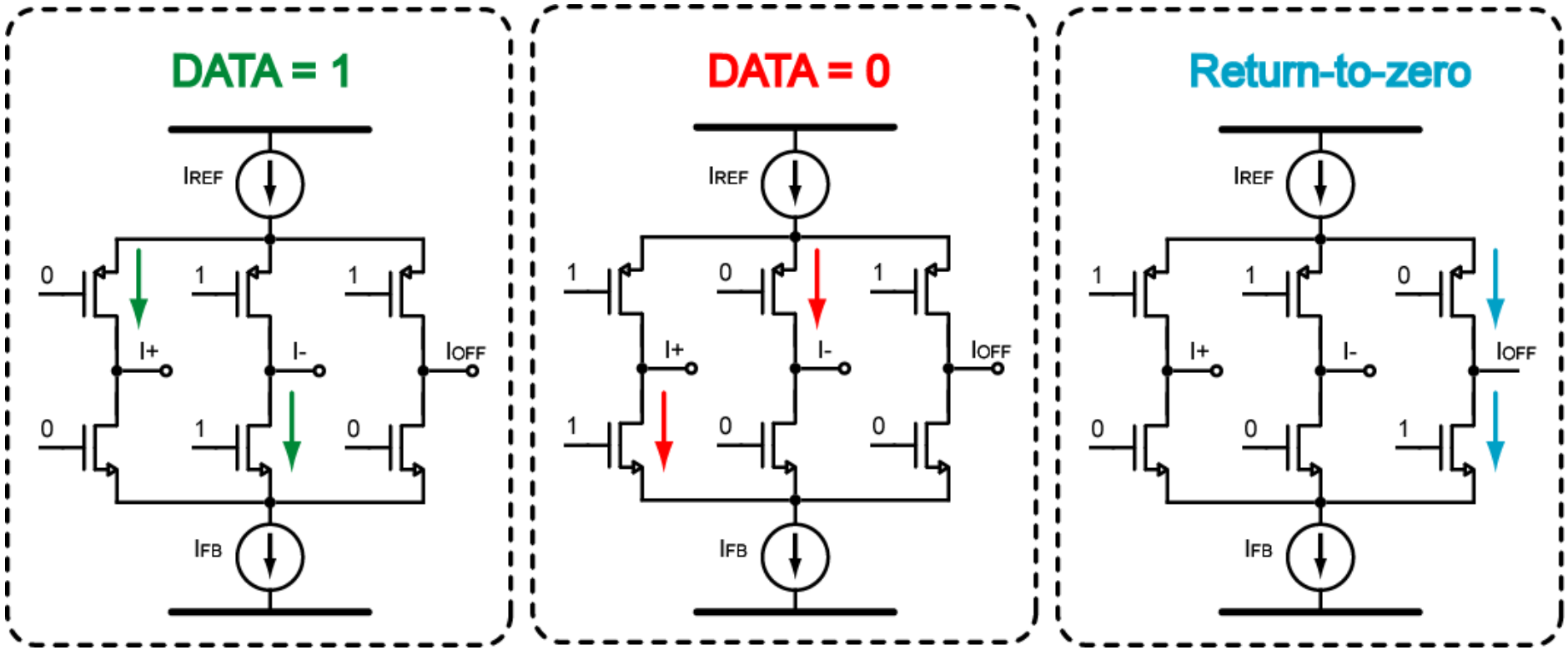
- A_V = 55 dB
- GBW = 2 GHz
- P_{DISS} = 15 mW

High SNR of VCO-based quantizer allows reduced opamp gain (A_v)

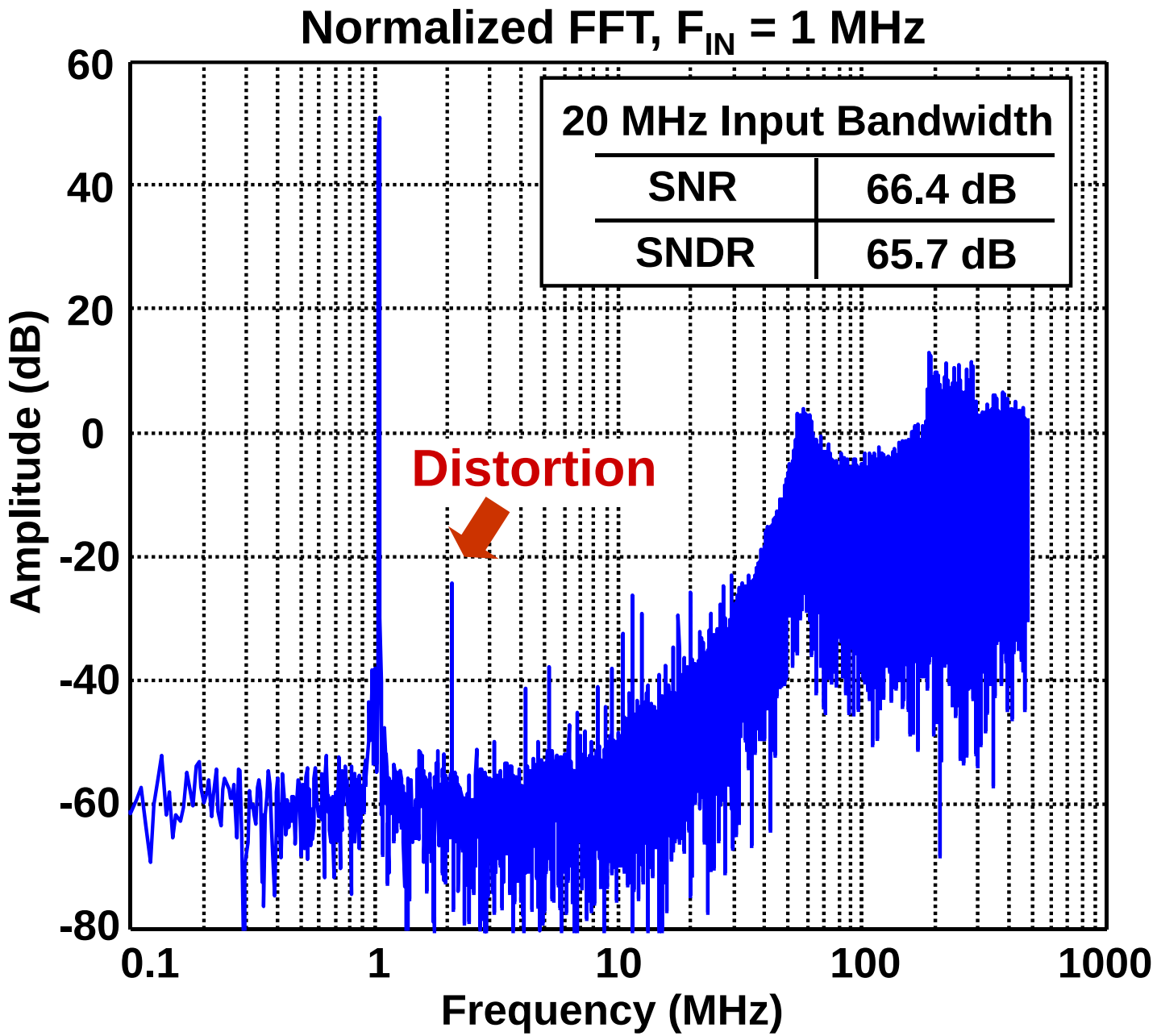


Primary Feedback DAC Schematic

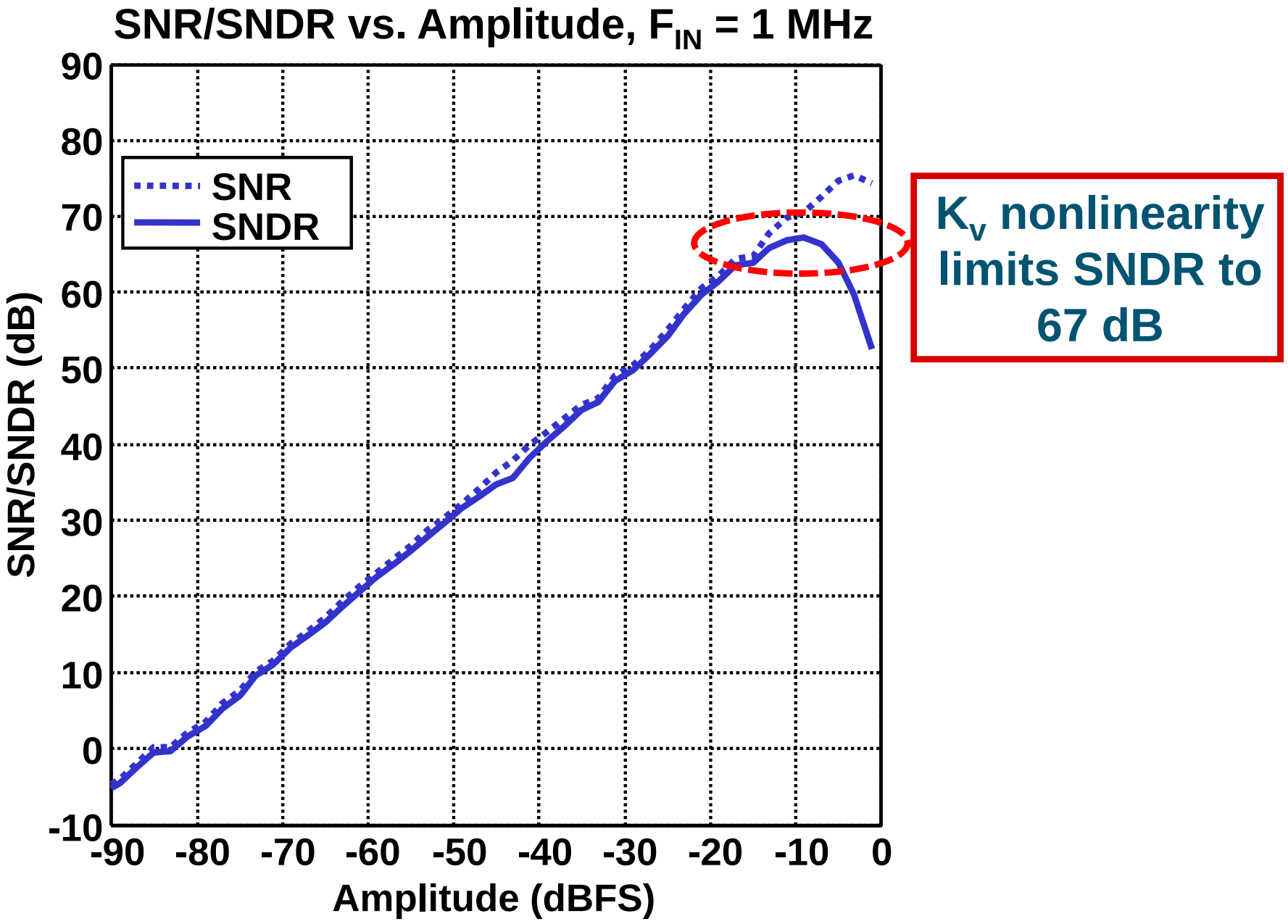
- **Fully differential RZ pulses**
- **Triple-source current steering**
- **I_{OFF} is terminated off-chip**



Measured Spectrum From Prototype

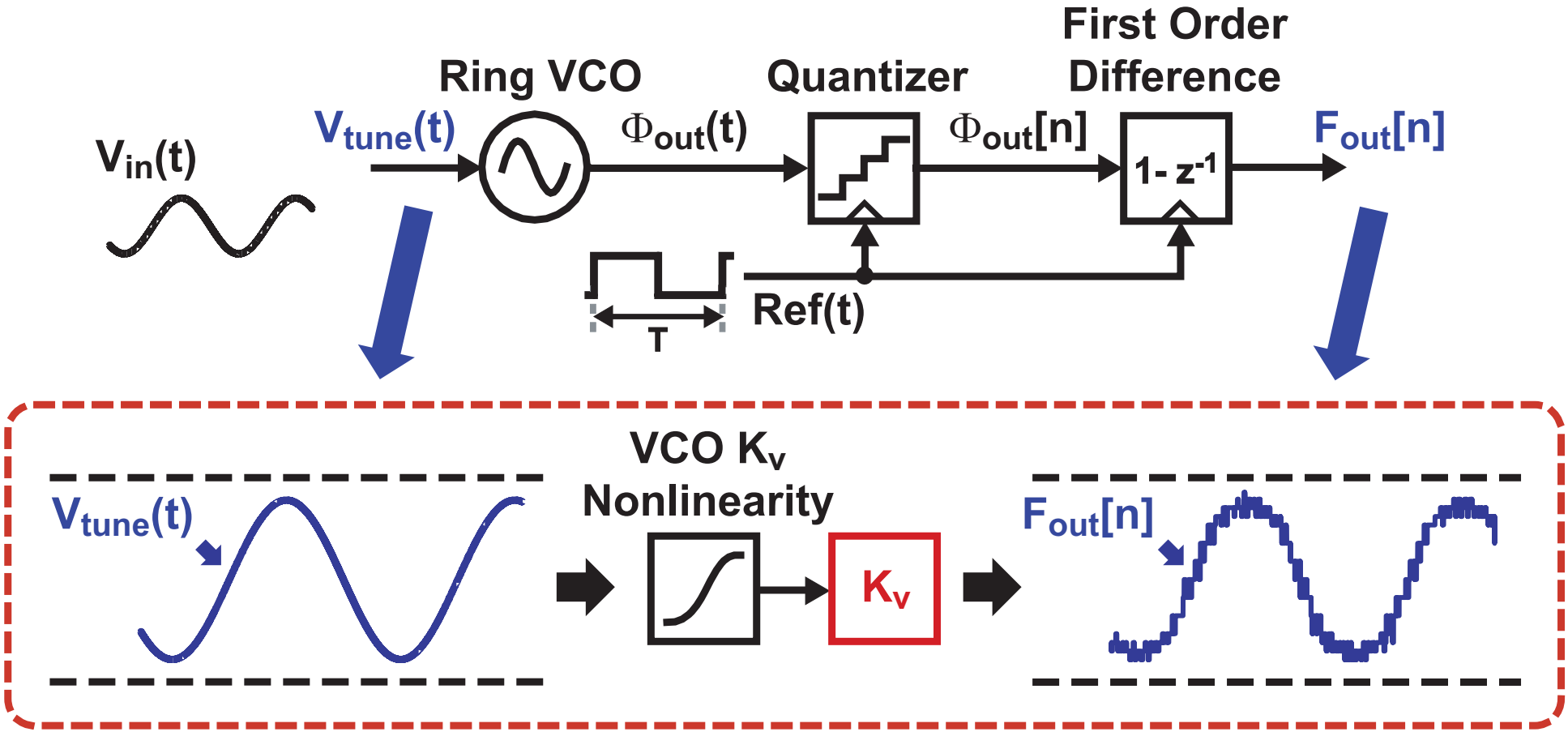


Measured SNR/SNDR Vs. Input Amplitude (20 MHz BW)



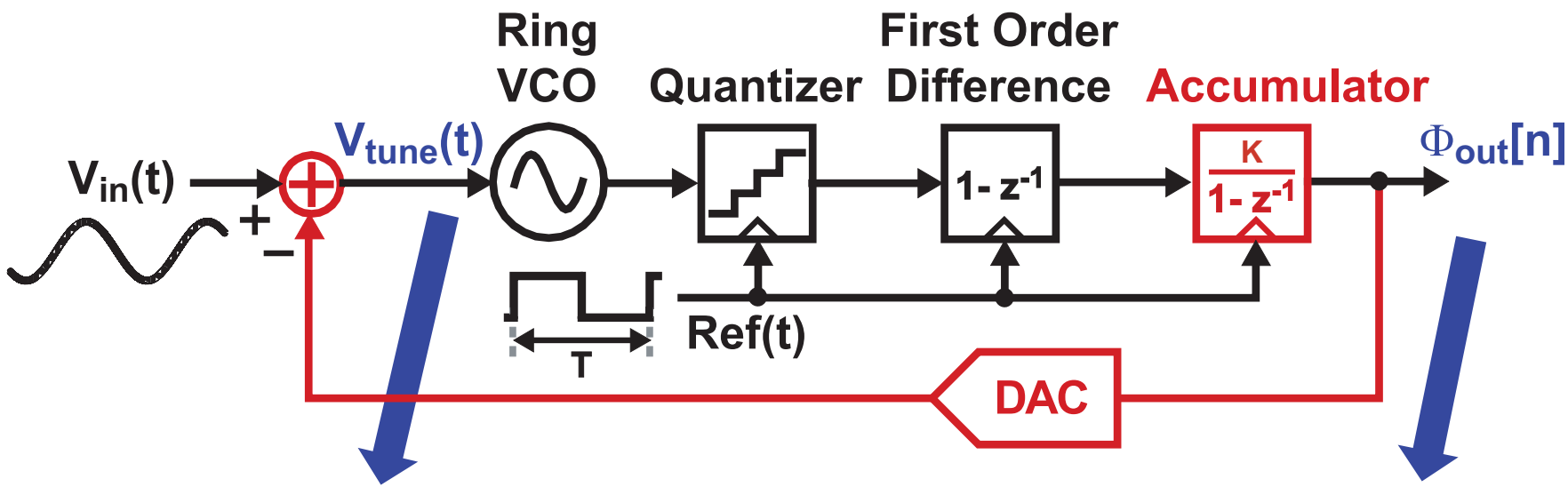
How Do We Overcome K_v Nonlinearity to Improve SNDR?

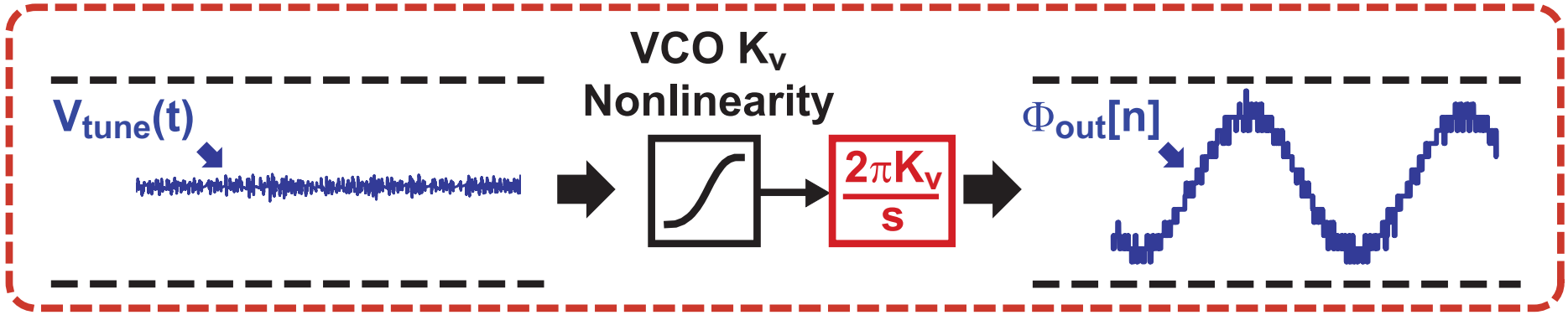
Voltage-to-Frequency VCO-based ADC (1st Order Δ–Σ)



- Typically, VCO *frequency* is desired output variable
  - Input uses full voltage-to-frequency (K_v) characteristic
  - Strong distortion at extreme ends of the K_v curve

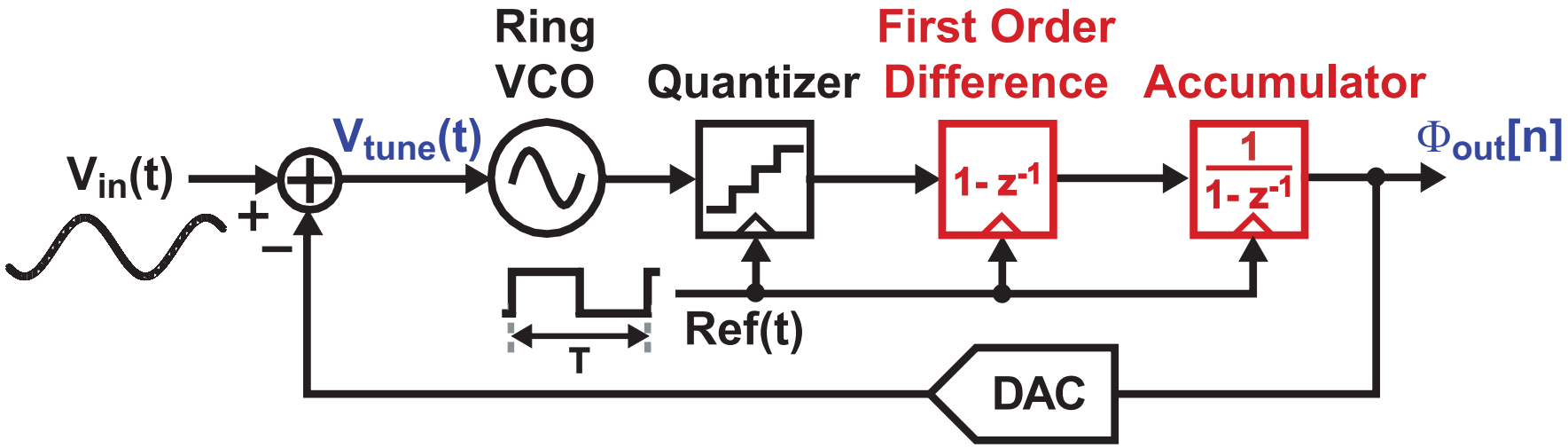
Voltage-to-Phase Approach (1st Order Δ–Σ)



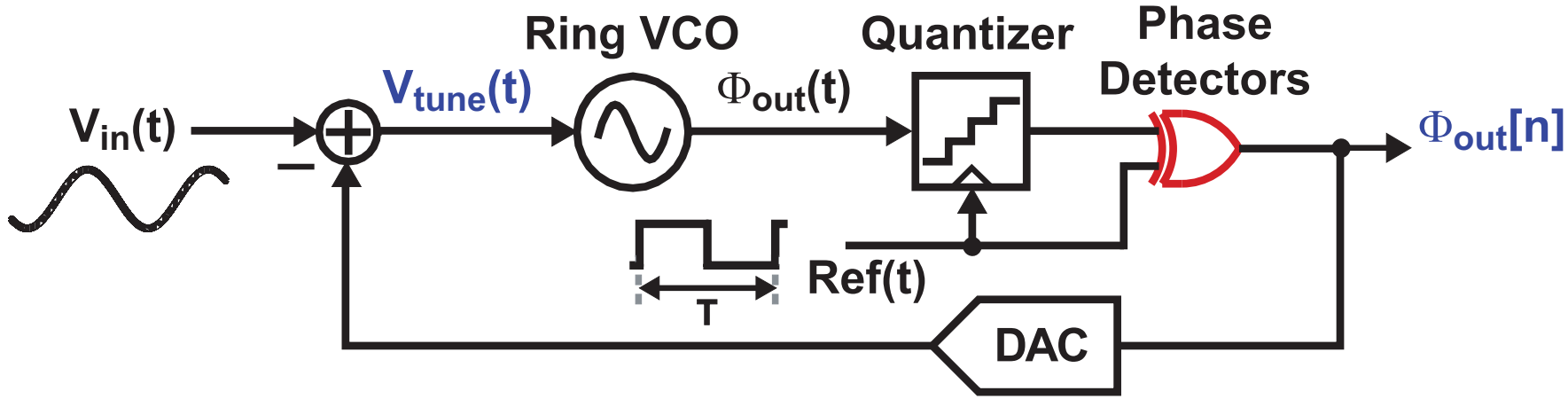


- VCO output *phase* is now the output variable
  - Small perturbation on V_{tune} allows large VCO phase shift
  - VCO acts as a CT integrator with *infinite* DC gain

High Speed Implementation of Phase-Based ADC

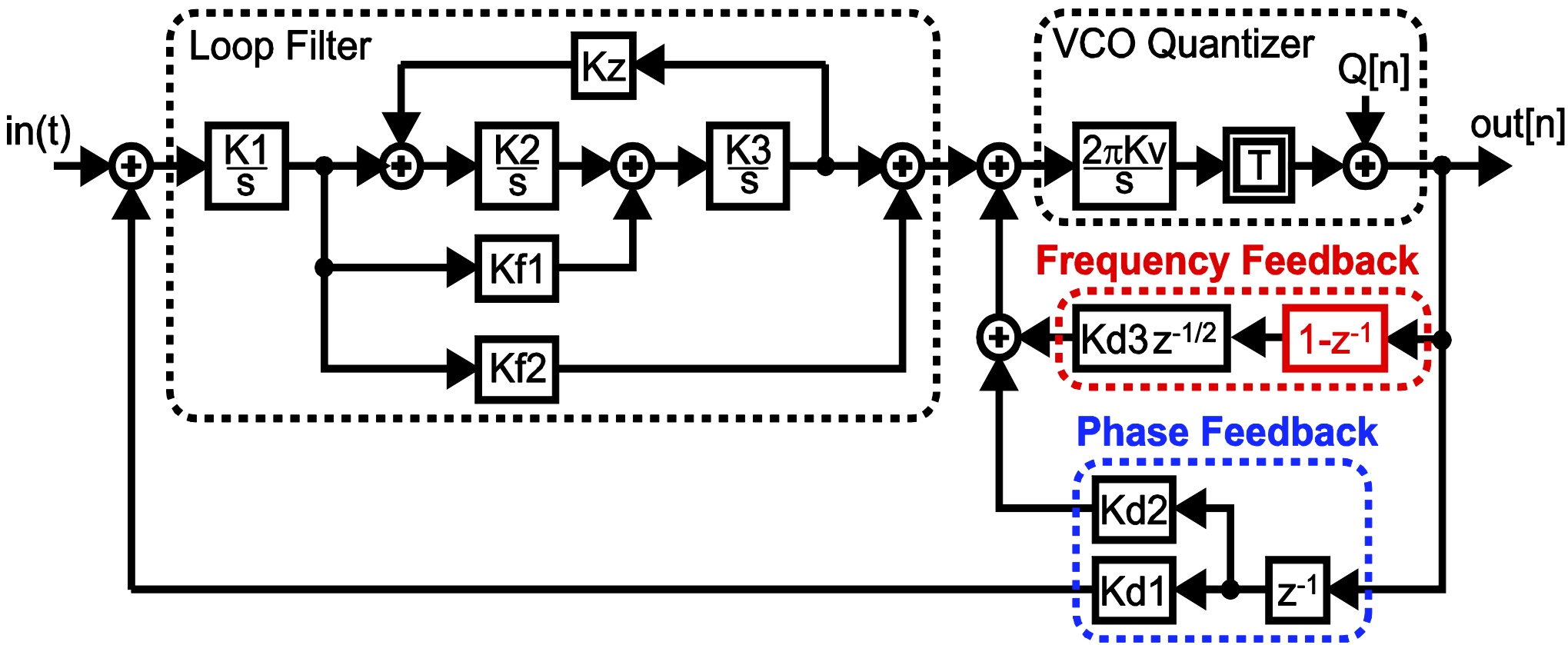


Park, Perrott
JSSC 2009



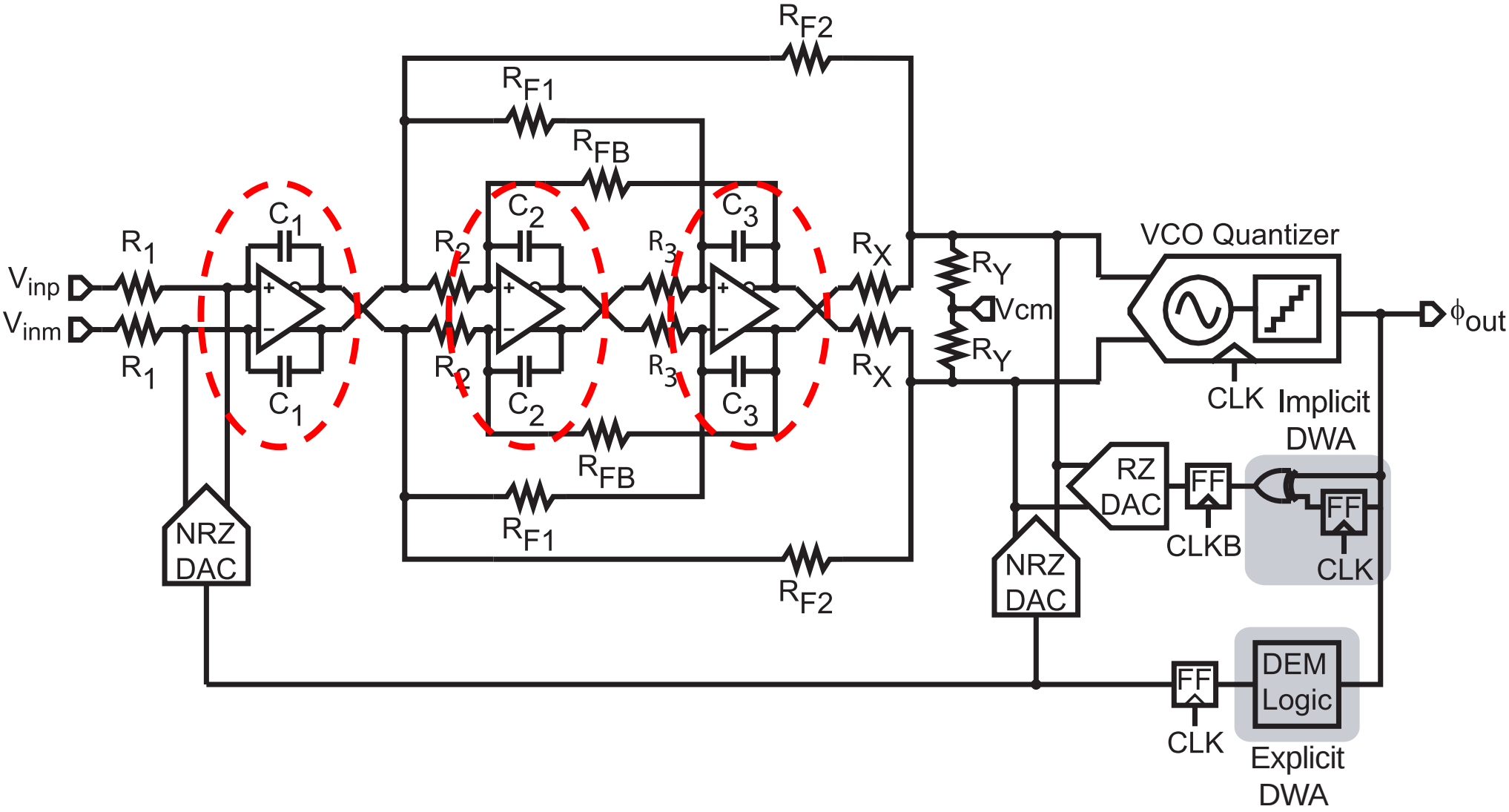
High SNDR requires higher order Δ–Σ …

Proposed 4th Order Architecture for Improved SNDR



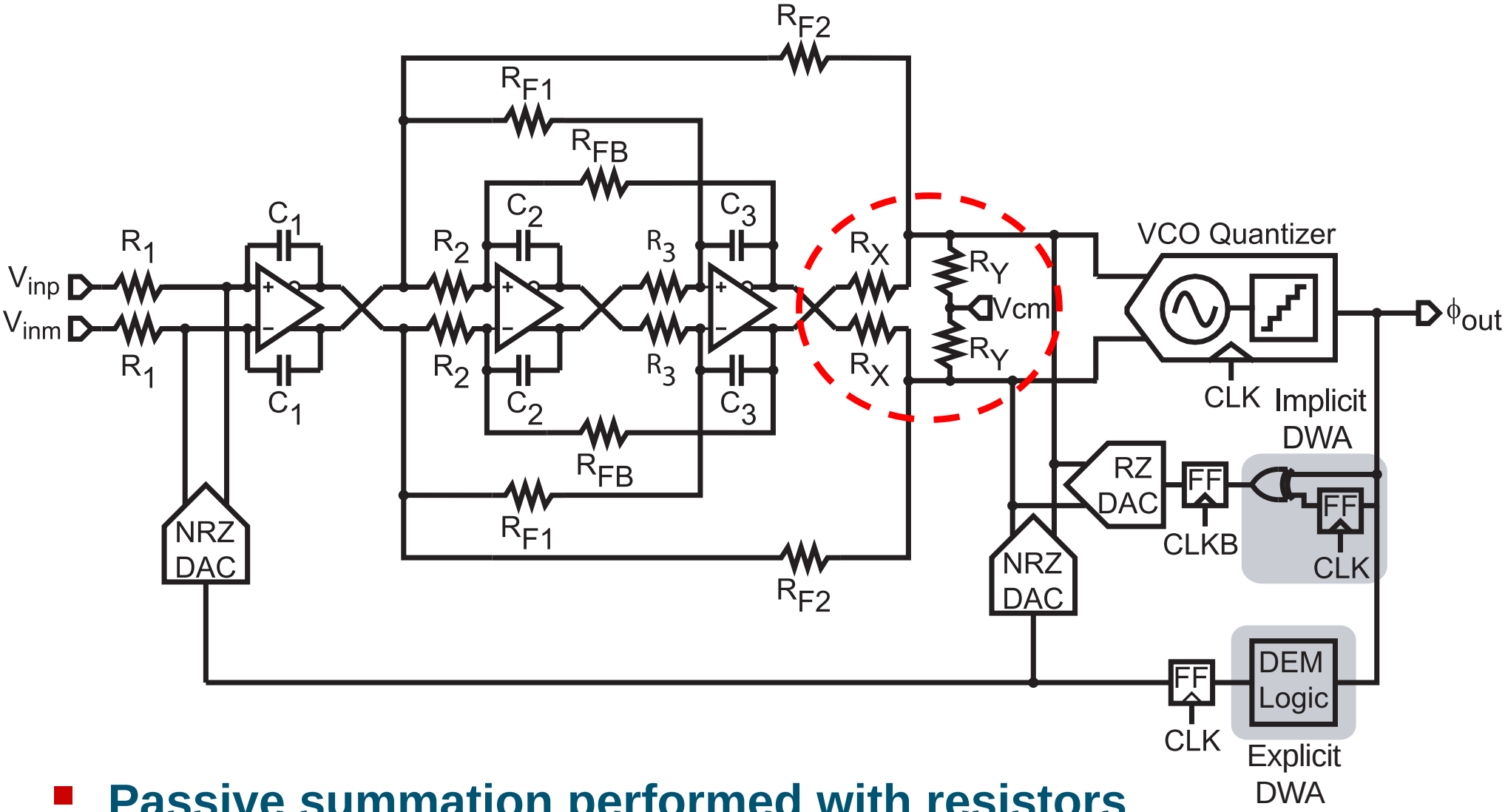
- **Goal: ~80 dB SNDR with 20 MHz bandwidth**
  - **Use 4th order loop filter, 4-bit VCO-based quantizer**
  - **4-bit quantizer: tradeoff resolution versus DEM overhead**
- **Combined frequency/phase feedback for stability/SNDR**

Schematic of Proposed Architecture



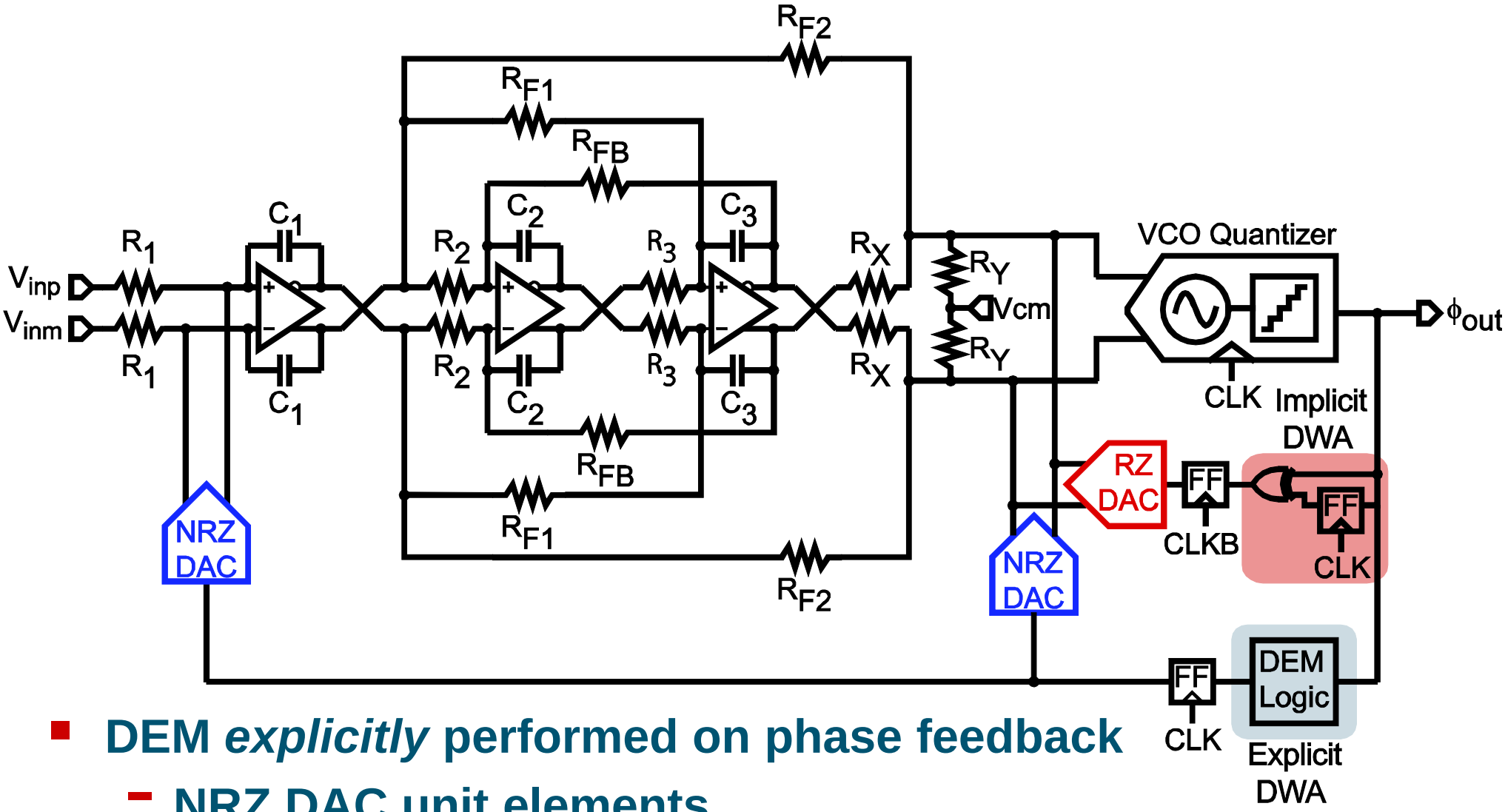
- Opamp-RC integrators
  - Better linearity than Gm-C, though higher power

Schematic of Proposed Architecture



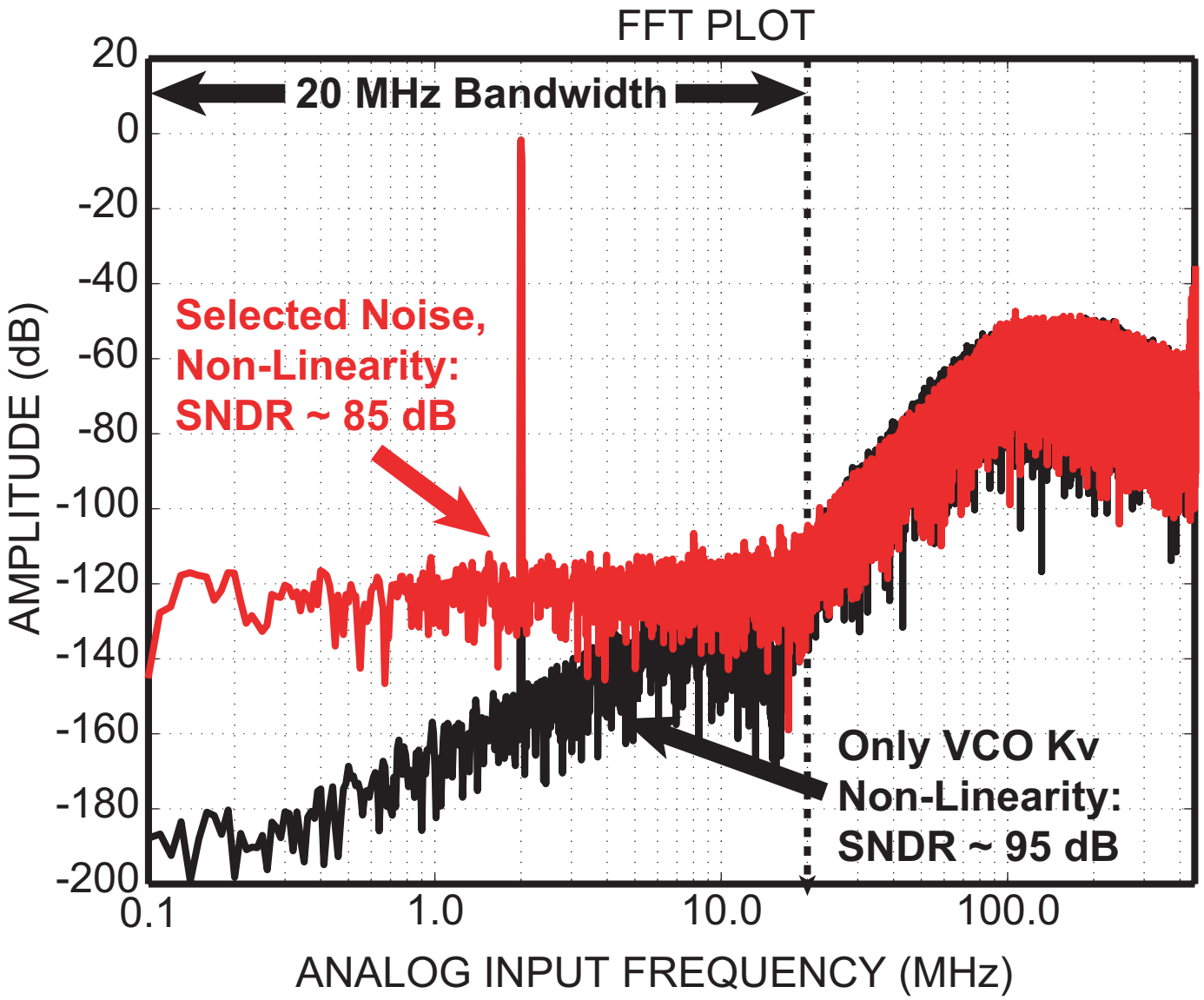
- Passive summation performed with resistors
  - Low power
  - Design carefully to minimize impact of parasitic pole

Schematic of Proposed Architecture



- DEM *explicitly* performed on phase feedback
  - NRZ DAC unit elements
- DEM *implicitly* performed on frequency feedback (Miller)
  - RZ DAC unit elements

Behavioral Simulation (available at www.cppsim.com)



Key Nonidealities

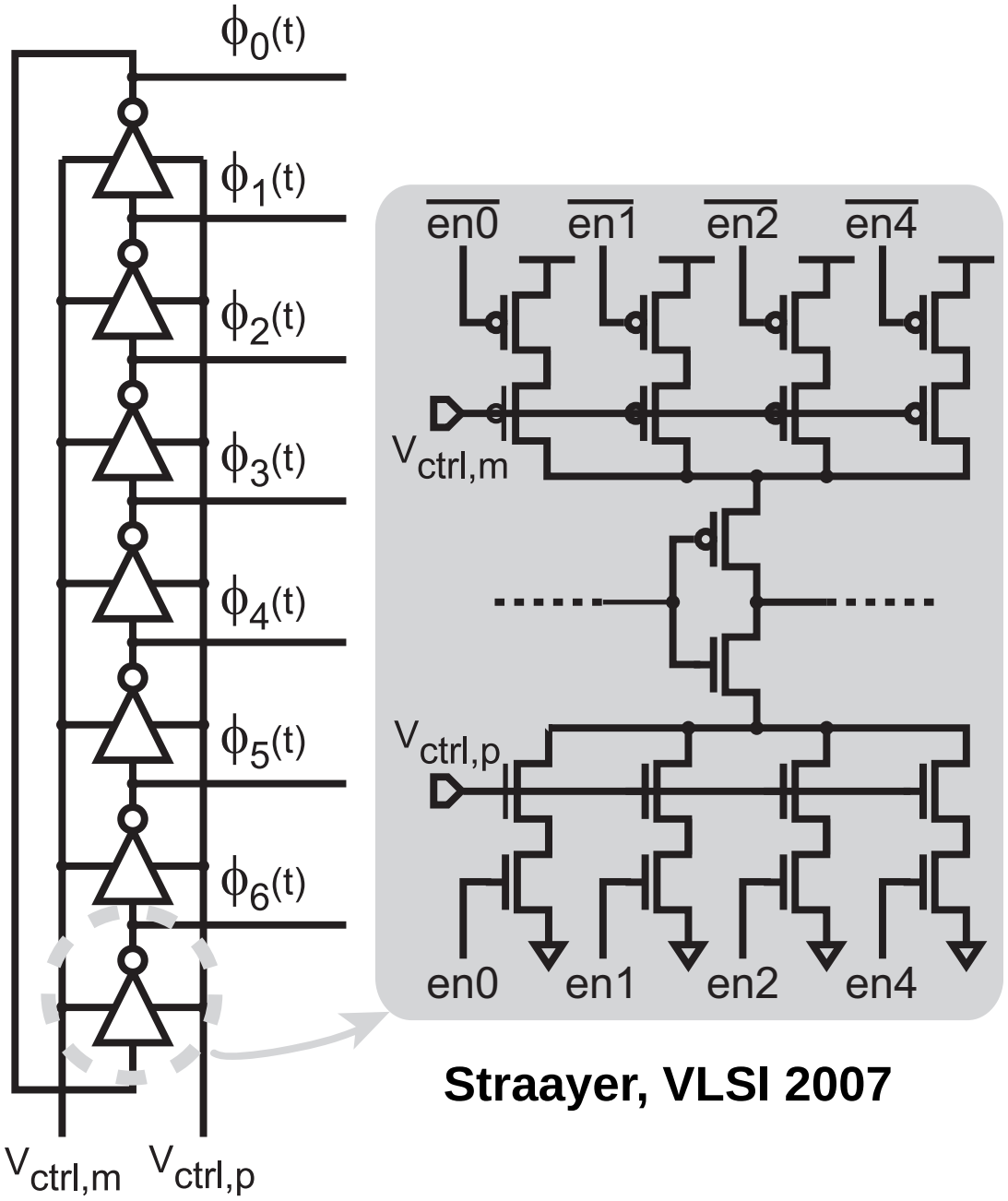
- VCO Kv non-linearity
- Device noise
- Amplifier finite gain, finite BW
- DAC and VCO unit element mismatch

85 dB SNDR!

VCO nonlinearity is *not* the bottleneck for achievable SNDR!

Circuit Details

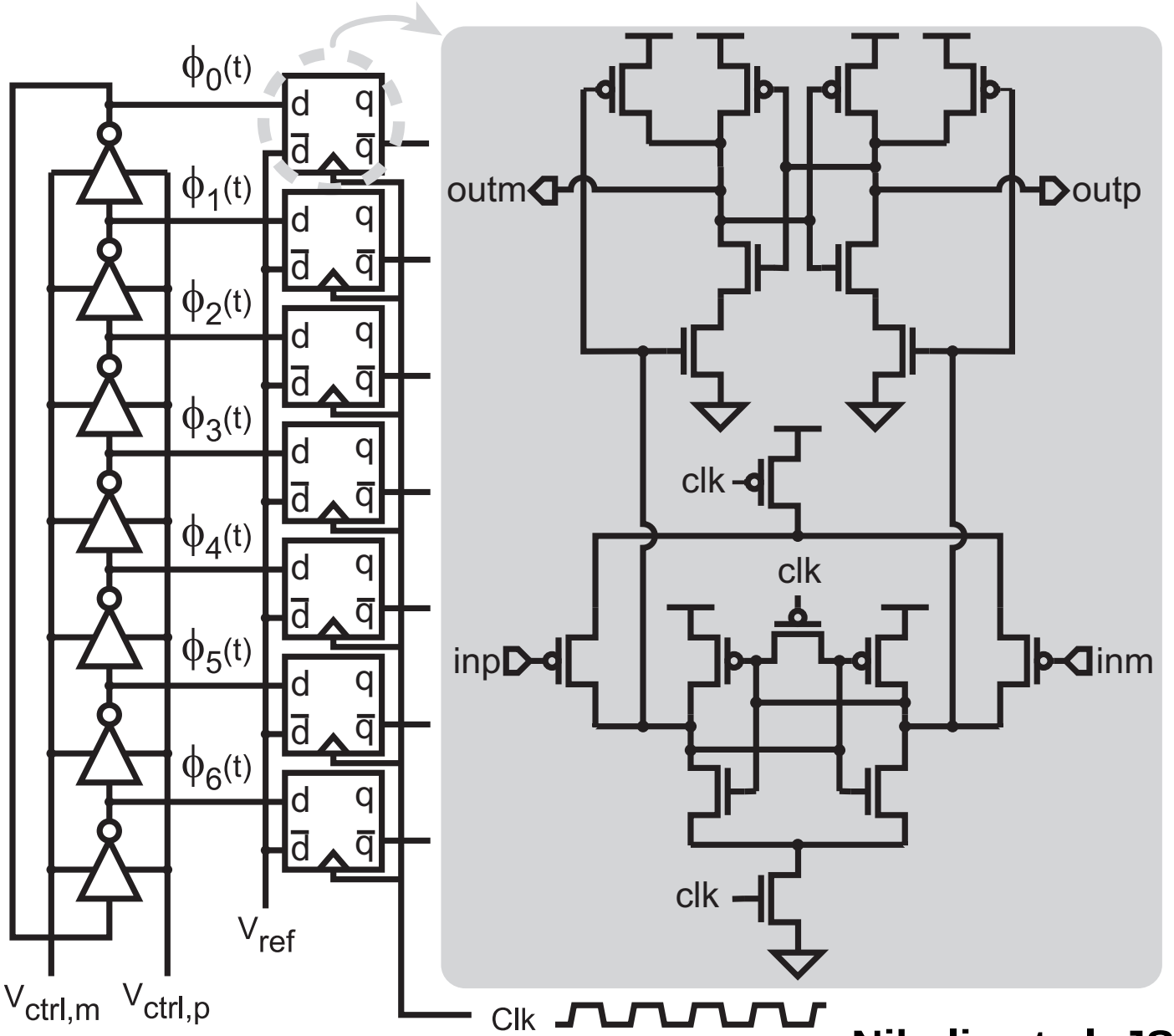
VCO Integrator Schematic



Straayer, VLSI 2007

- **15 stage current starved ring-VCO**
  - **7 stage ring-VCO shown for simplicity**
  - **Pseudo differential control**
  - **PVT variation accommodated by enable switches on PMOS/NMOS**
- **Rail-to-rail VCO output phase signals (VDD to GND)**

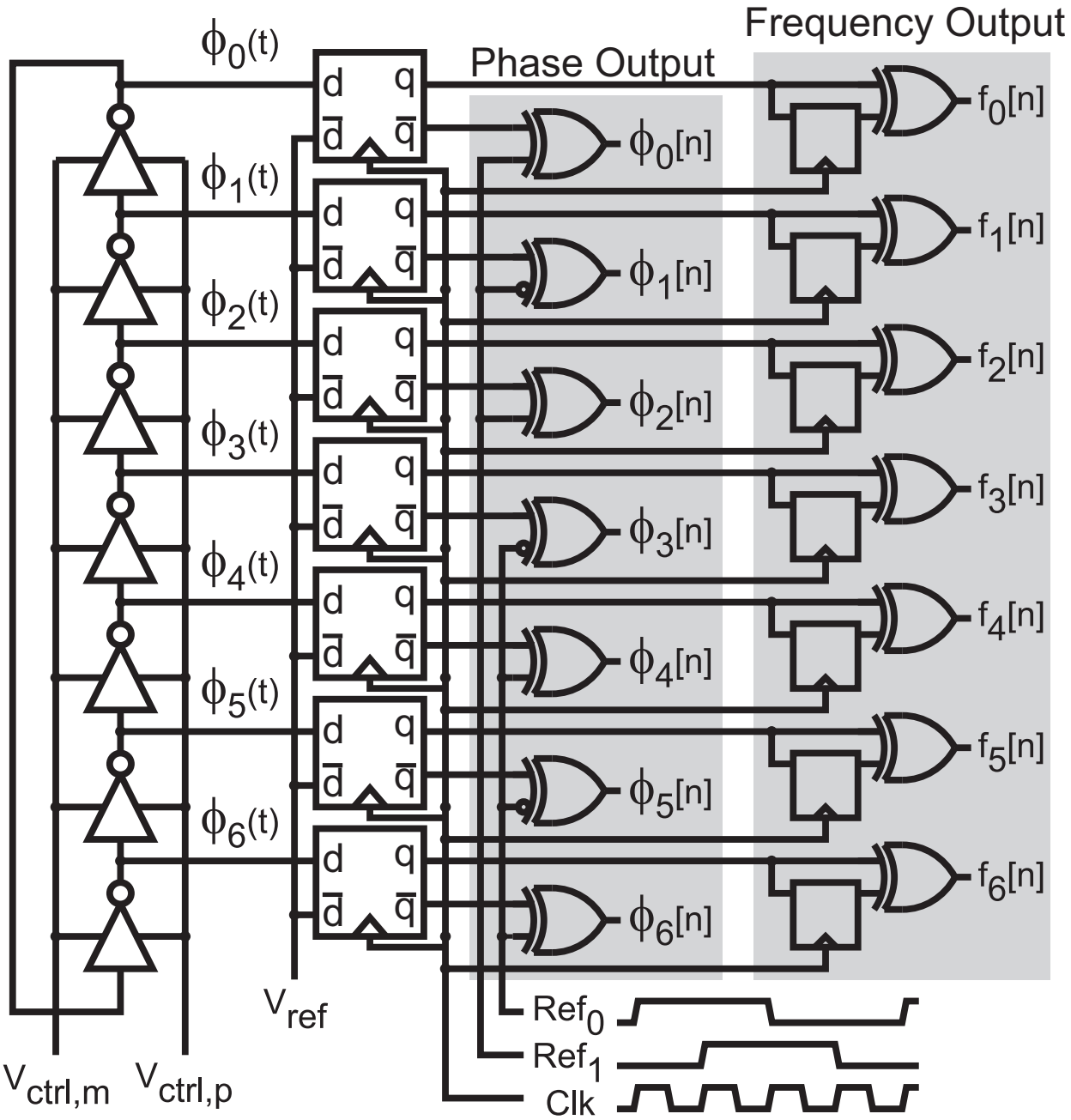
VCO Quantizer Schematic



- **Phase quantization with sense-amp flip-flop**
  - **Single phase clocking**
- **Rail-to-rail quantizer output signals (VDD to GND)**

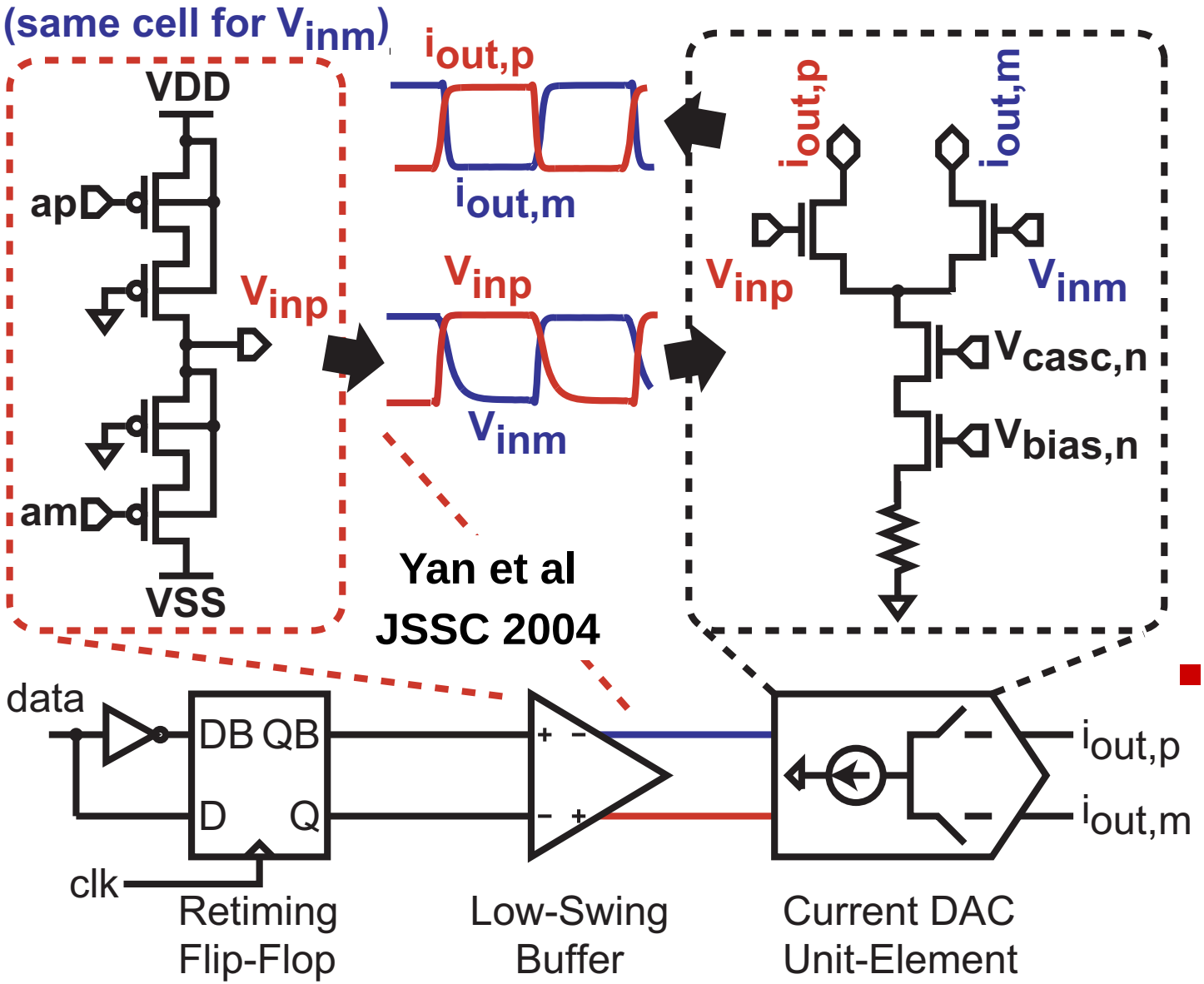
Nikolic et al, JSSC 2000

Phase Quantizer, Phase and Frequency Detector



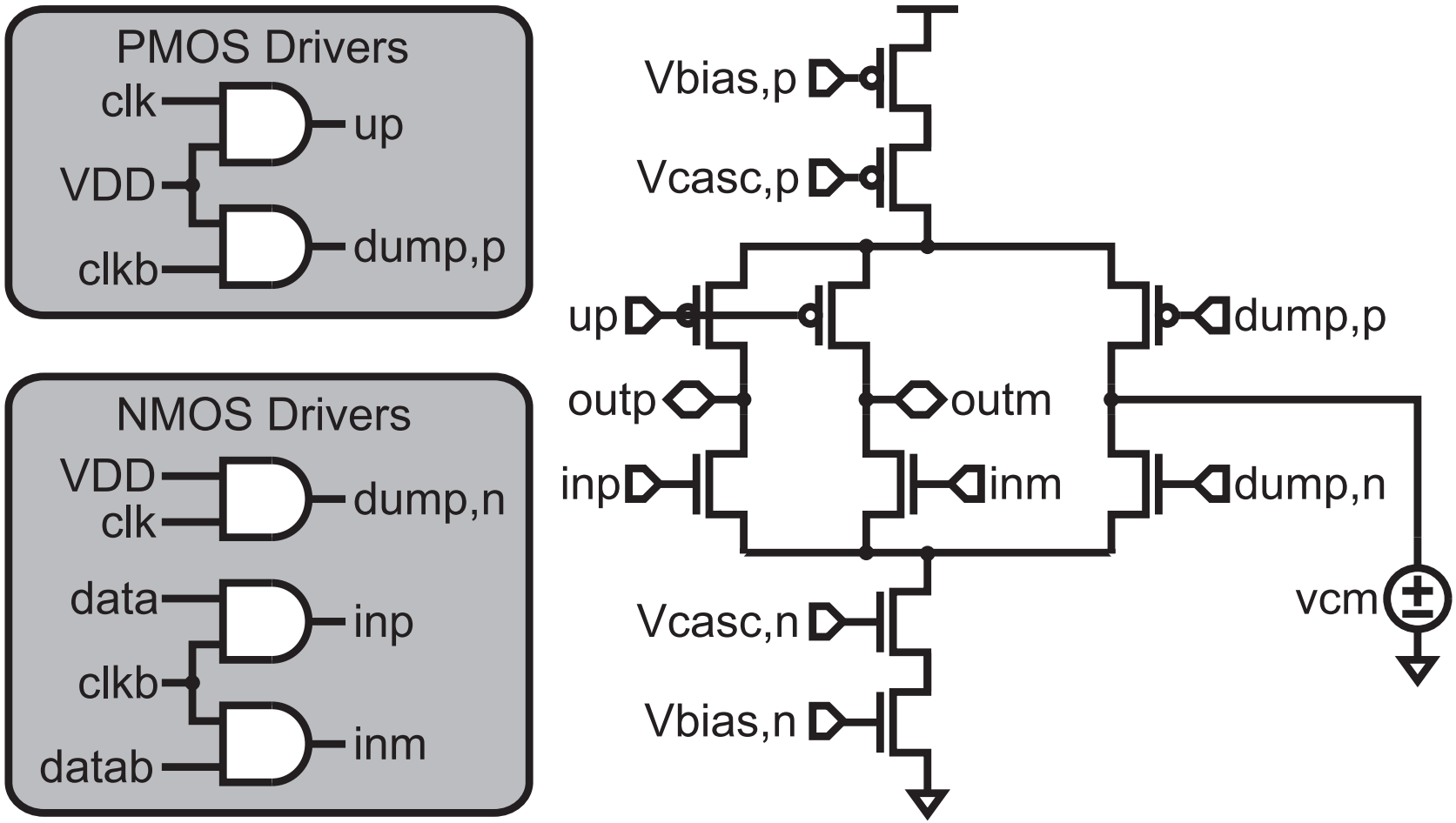
- **Highly digital implementation**
  - **Phase sampled & quantized by SAFF**
  - **XOR phase and frequency detection with FF and XOR**
- **Automatic DWA for frequency detector output code**
  - **Must explicitly perform DWA on phase detector output code**

Main Feedback DAC Schematic



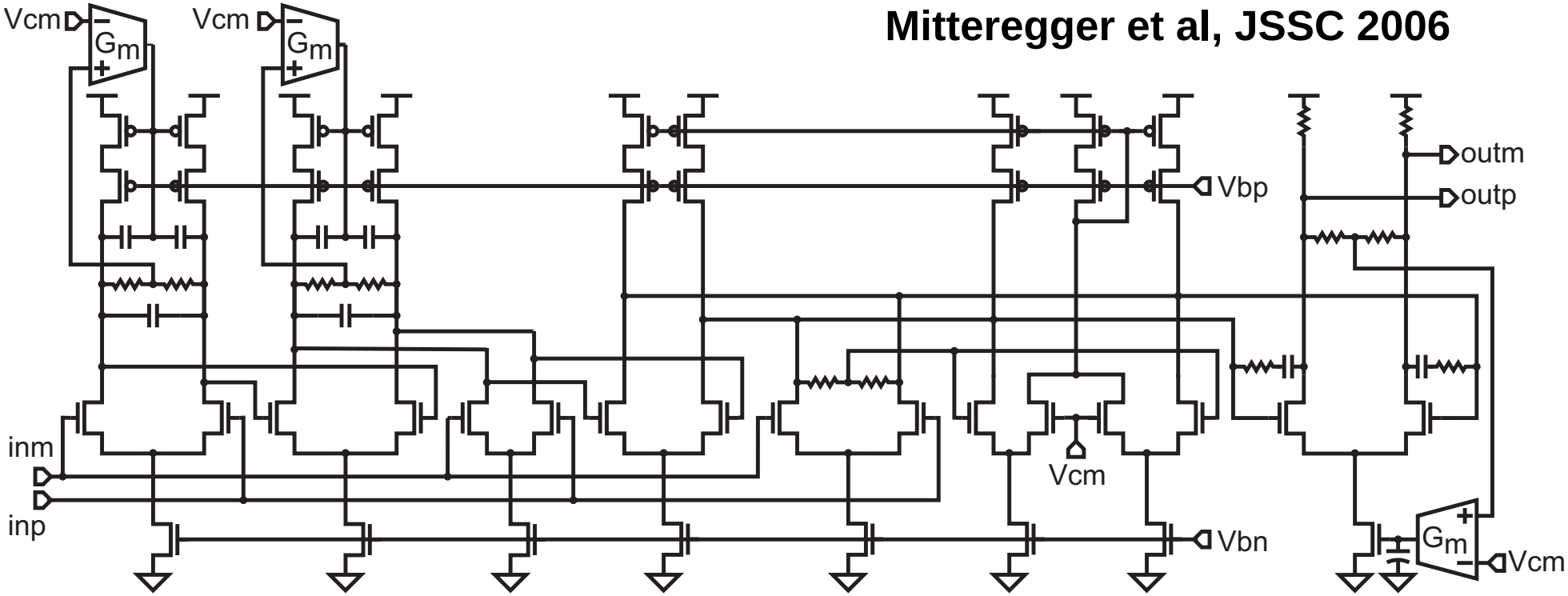
- **Low-swing buffers**
  - Keeps switch devices in saturation
  - Fast "on"/Slow "off" reduces glitches at DAC output
  - Uses external Vdd/Vss
- **Resistor degeneration minimizes 1/f noise**

Bit-Slice of Minor Loop RZ DAC



- **RZ DAC unit elements transition every sample period**
  - **Breaks code-dependency of transient mismatch (ISI)**
  - **Uses full-swing logic signals for switching**

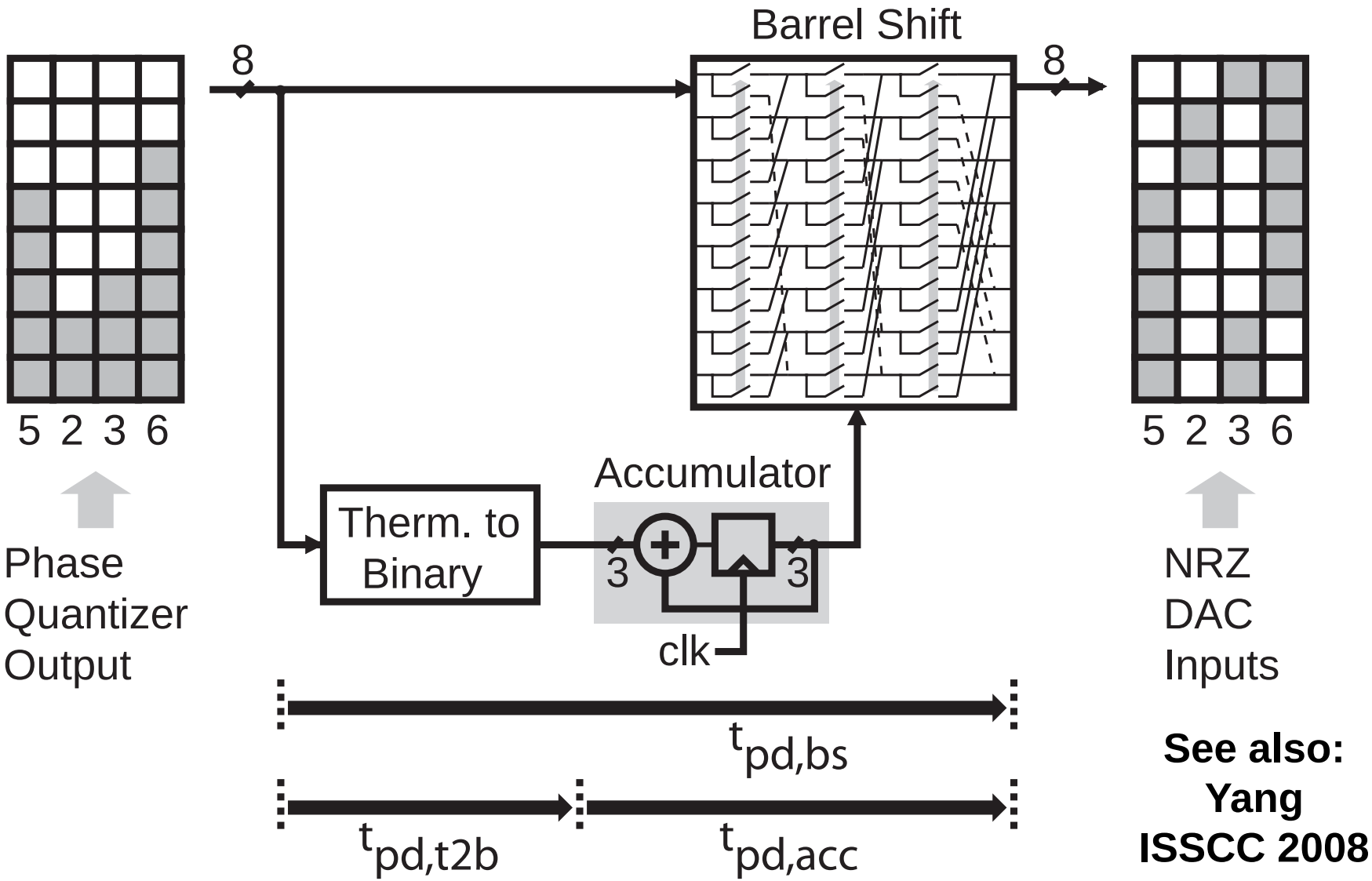
Opamp Schematic



Parameter	Value
DC Gain	63 dB
Unity-Gain Frequency	4.0 GHz
Phase Margin	55°
Input Referred Noise Power (20 MHz BW)	11 uV (rms)
Power (V_{DD} = 1.5 V)	22.5 mW

- **Modified nested Miller opamp**
  - 4 cascaded gain stages, 2 feedforward stages
  - Behaves as 2-stage Miller near cross-over frequencies
  - Opamp 1 power is 2X of opamps 2 and 3 (for low noise)

DEM Architecture (3-bit example)

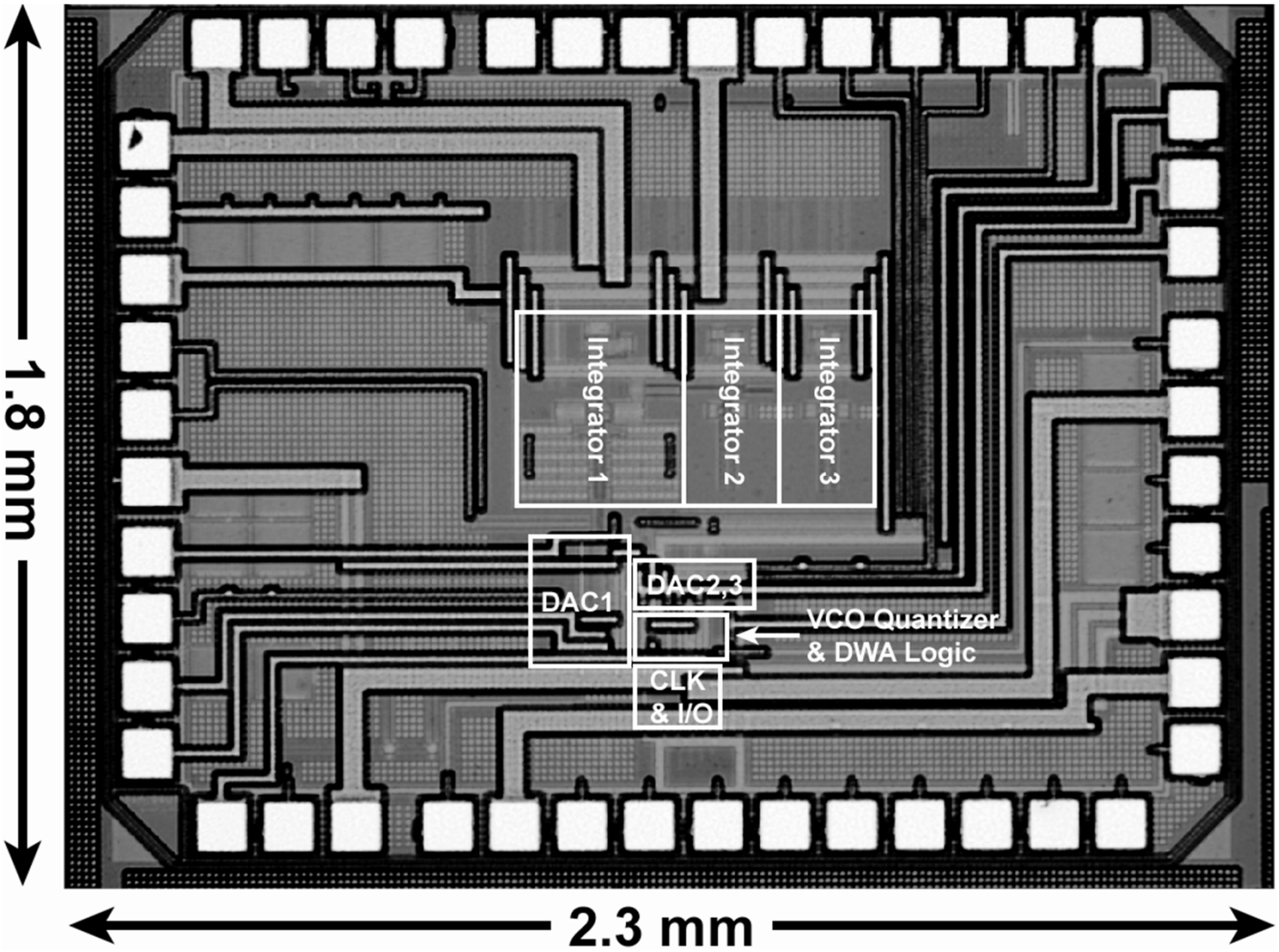


See also: Yang ISSCC 2008

- **Achieves low-delay to allow 4-bit DEM at 900 MHz**
  - **Delay is half a sample period**

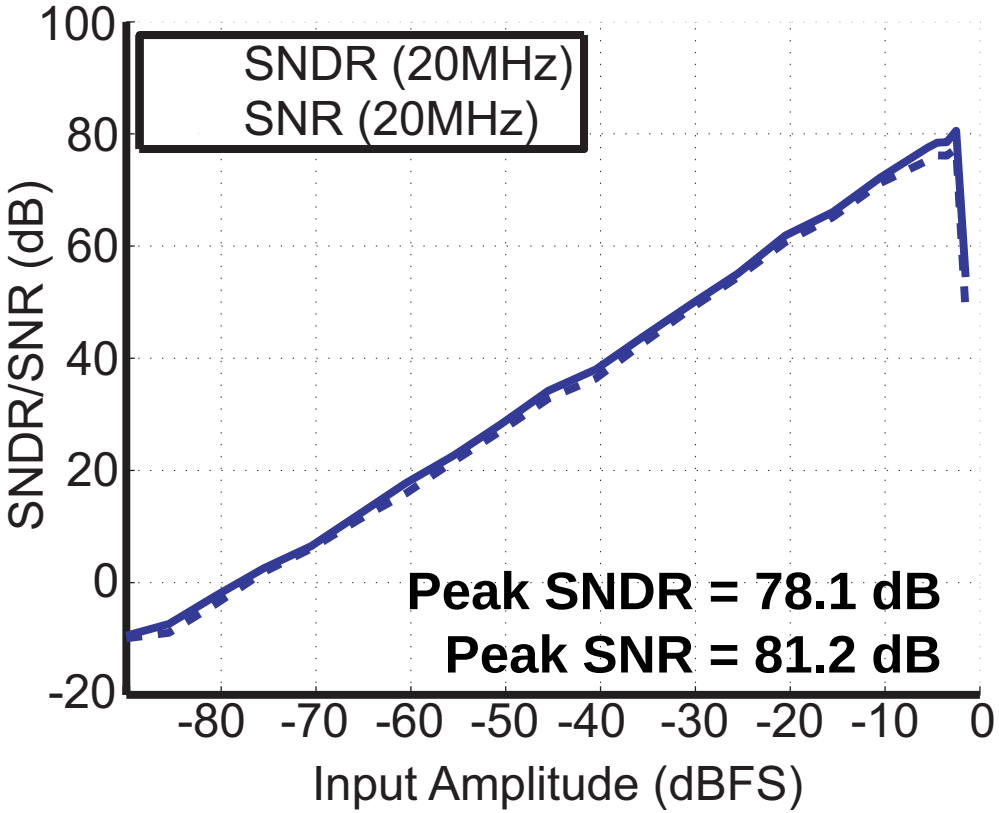
Die Photo (0.13u CMOS)

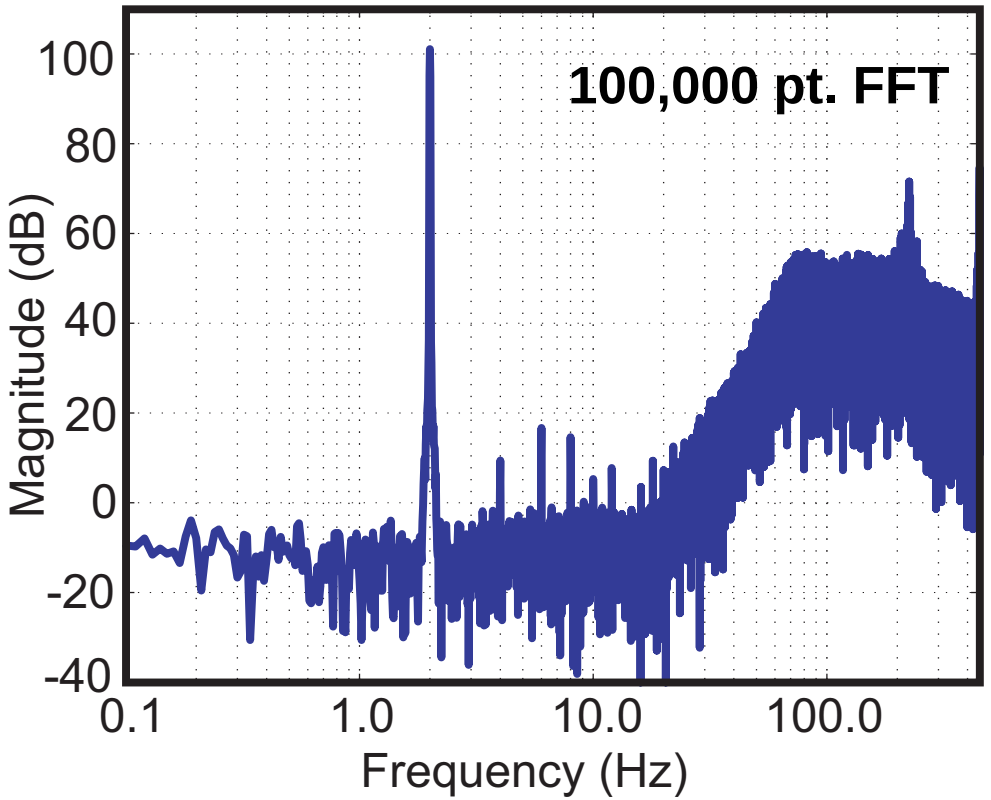
Die photo courtesy of Annie Wang (MTL)



- Active area
  - 0.45 mm^2
- Sampling Freq
  - 900 MHz
- Input BW
  - 20 MHz
- Supply Voltage
  - 1.5 V
- Analog Power
  - 69 mW
- Digital Power
  - 18 mW

Measured Results

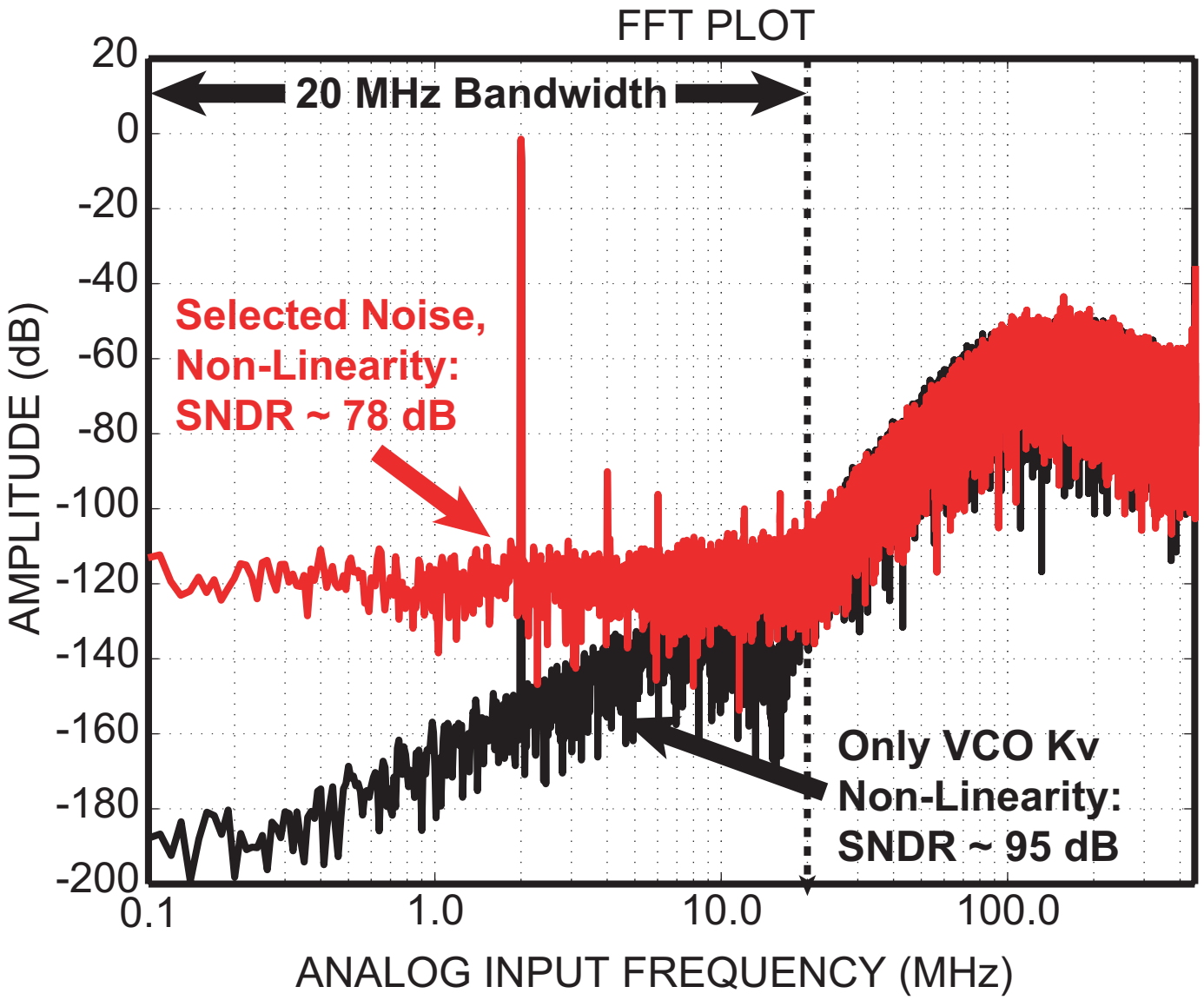




- 78 dB Peak SNDR performance in 20 MHz
  - Bottleneck: transient mismatch from main feedback DAC
- Architecture robust to VCO K_v non-linearity

Figure of Merit: 330 fJ/Conv with 78 dB SNDR

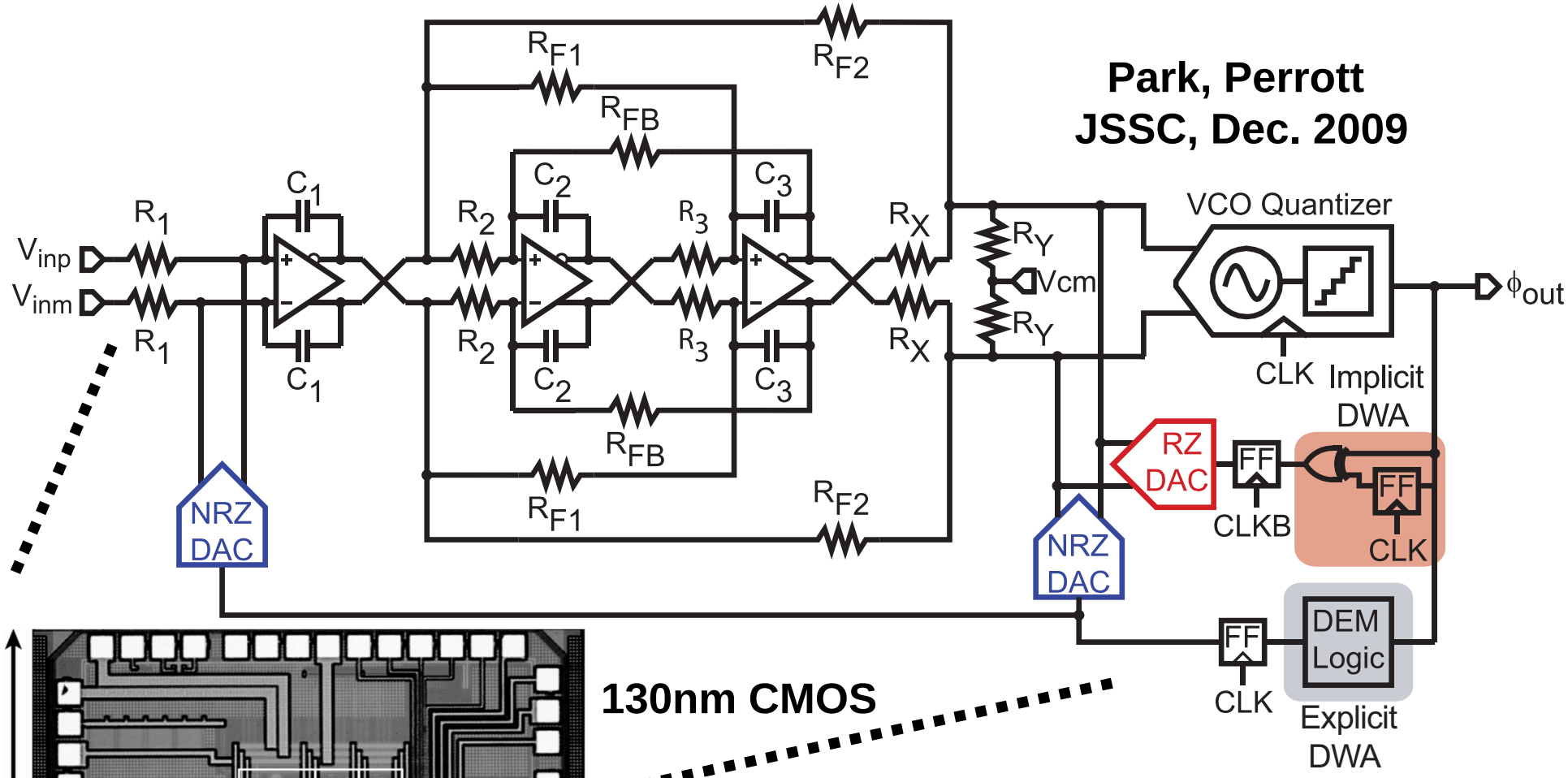
Behavioral Model Reveals Key Performance Issue

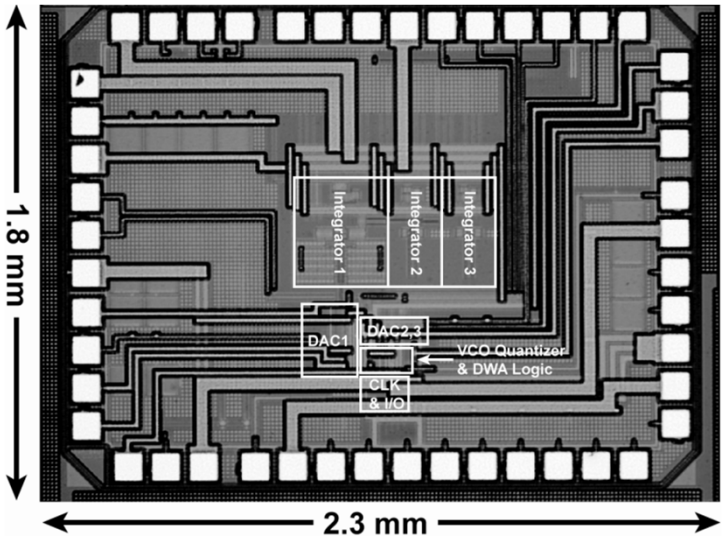


- Amplifier nonlinearity degrades SNDR to 81 dB
- DAC transient mismatch degrades SNDR to 78 dB
  - DEM does not help this
  - Could be improved with dual RZ structure

Transient DAC mismatch is likely the key bottleneck

Summary of Fourth Order CT Delta-Sigma ADC

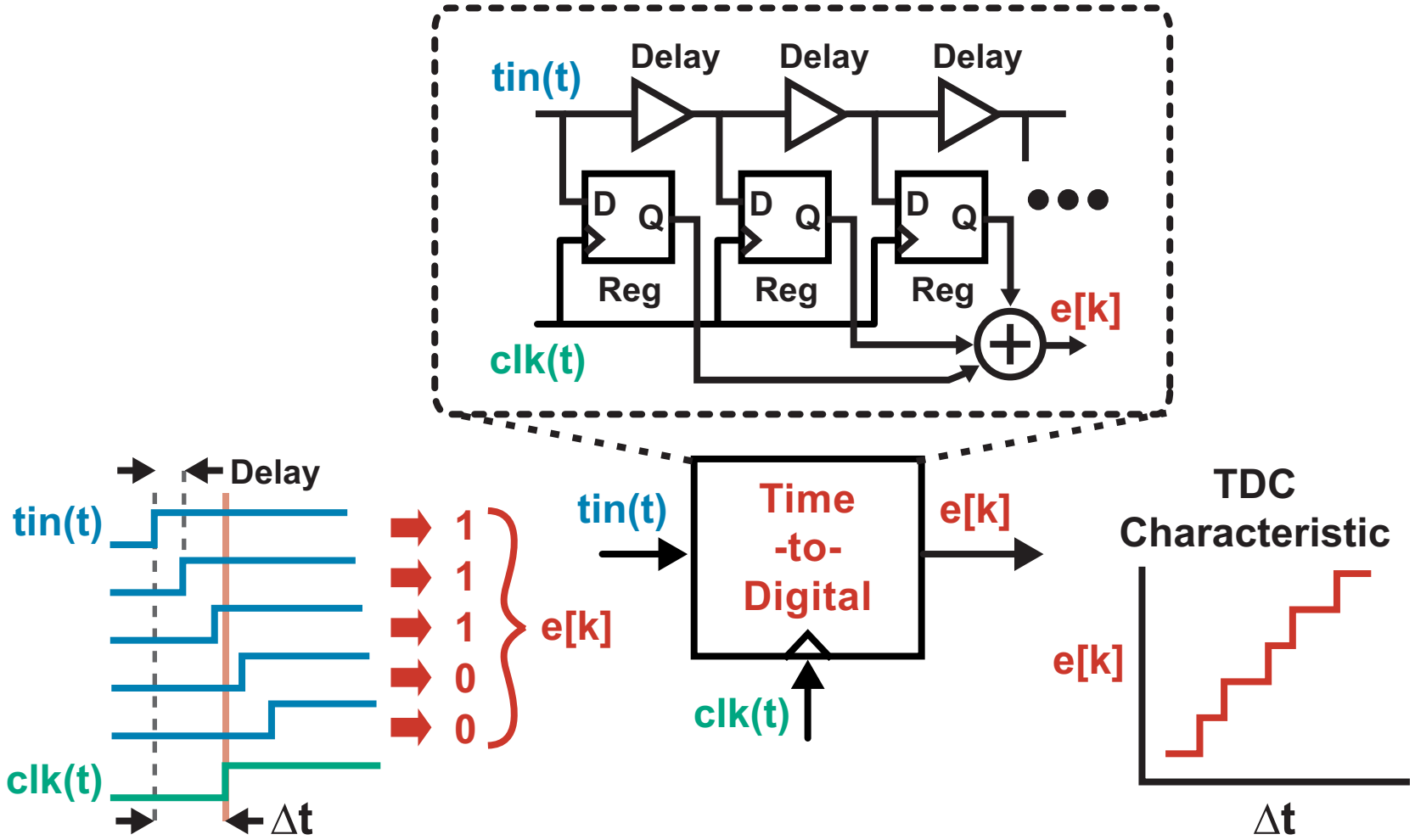




130nm CMOS

- **Peak SNDR of 78 dB with 20 MHz bandwidth**
- **Figure of merit: 330 fJ/conv**

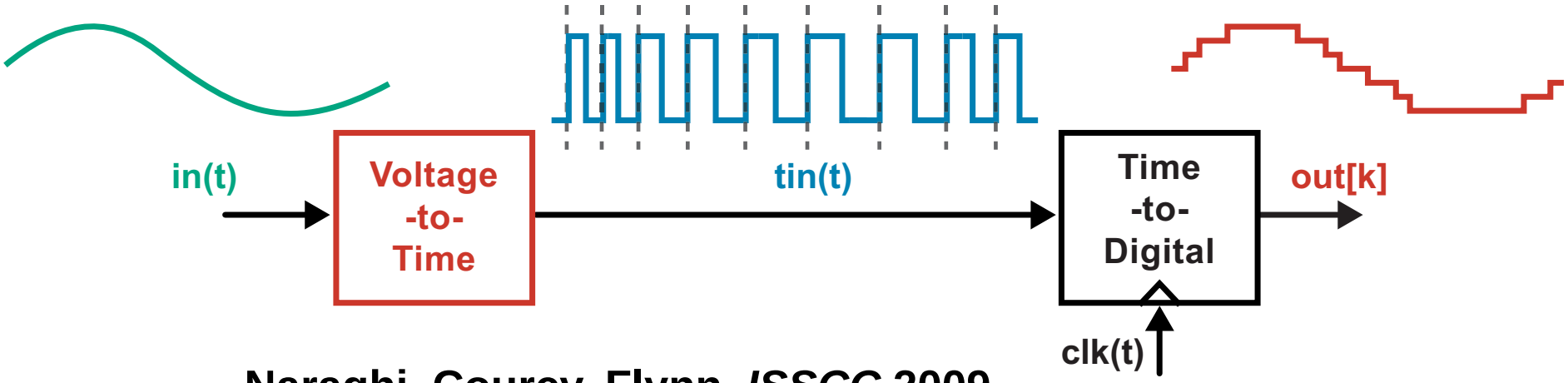
Consider Time-to-Digital Conversion



- Quantization in time achieved with purely digital gates
  - Easy implementation, resolution improving with Moore's law

How can we leverage this for quantizing an analog voltage?

Adding Voltage-to-Time Conversion

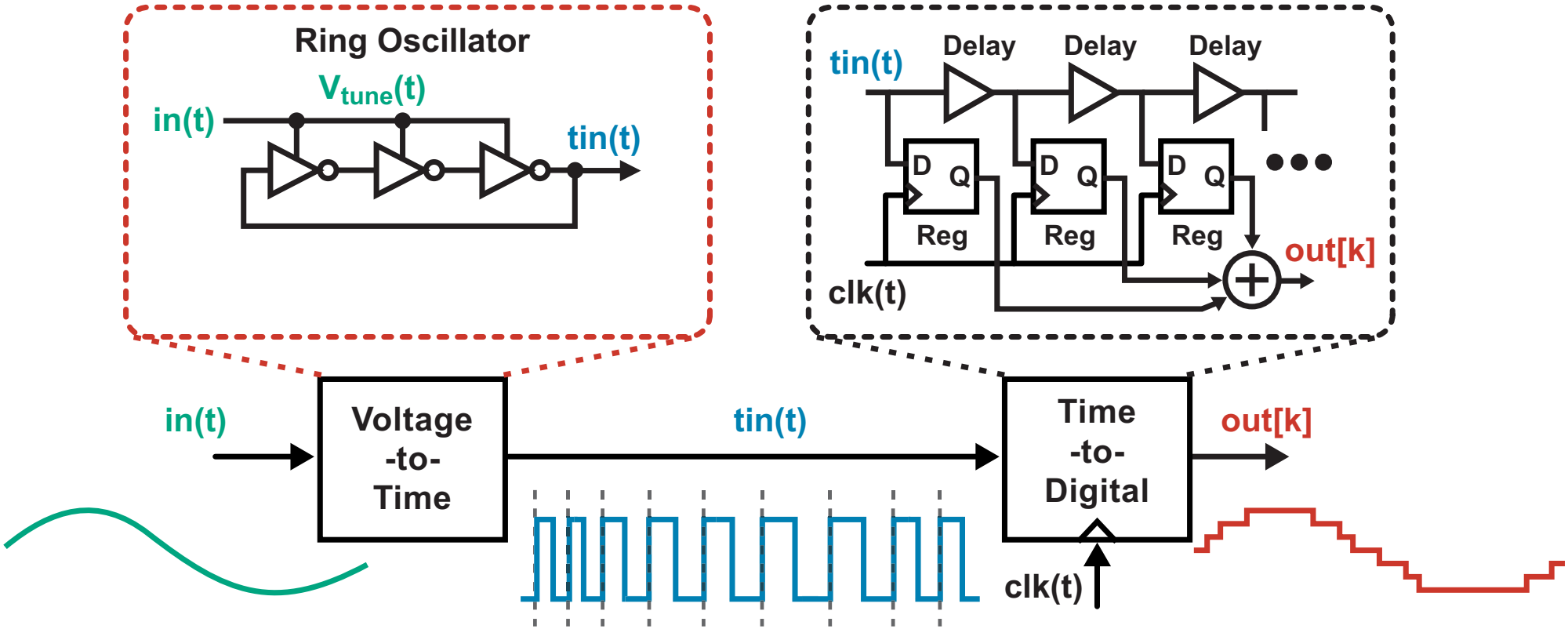


Naraghi, Courcy, Flynn, *ISSCC* 2009

- **Analog voltage is converted into edge times**
  - **Time-to-digital converter then turns the edge times into digitized values**
- **Key issues**
  - **Non-uniform sampling**
  - **Noise, nonlinearity**

Is there a simple implementation for the Voltage-to-Time Converter?

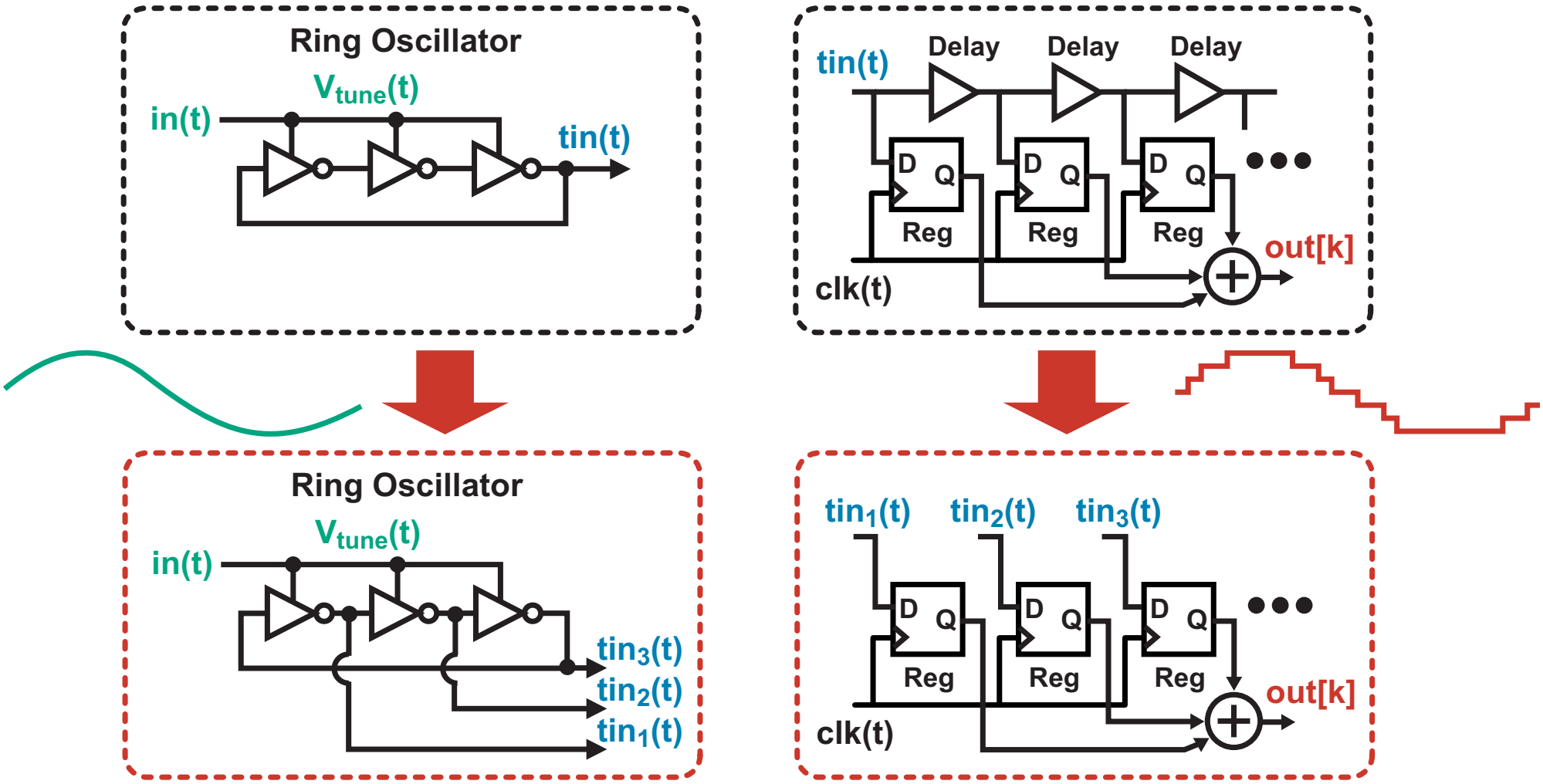
A Highly Digital Implementation



- A voltage-controlled ring oscillator offers a simple voltage-to-time structure
  - Non-uniform sampling is still an issue

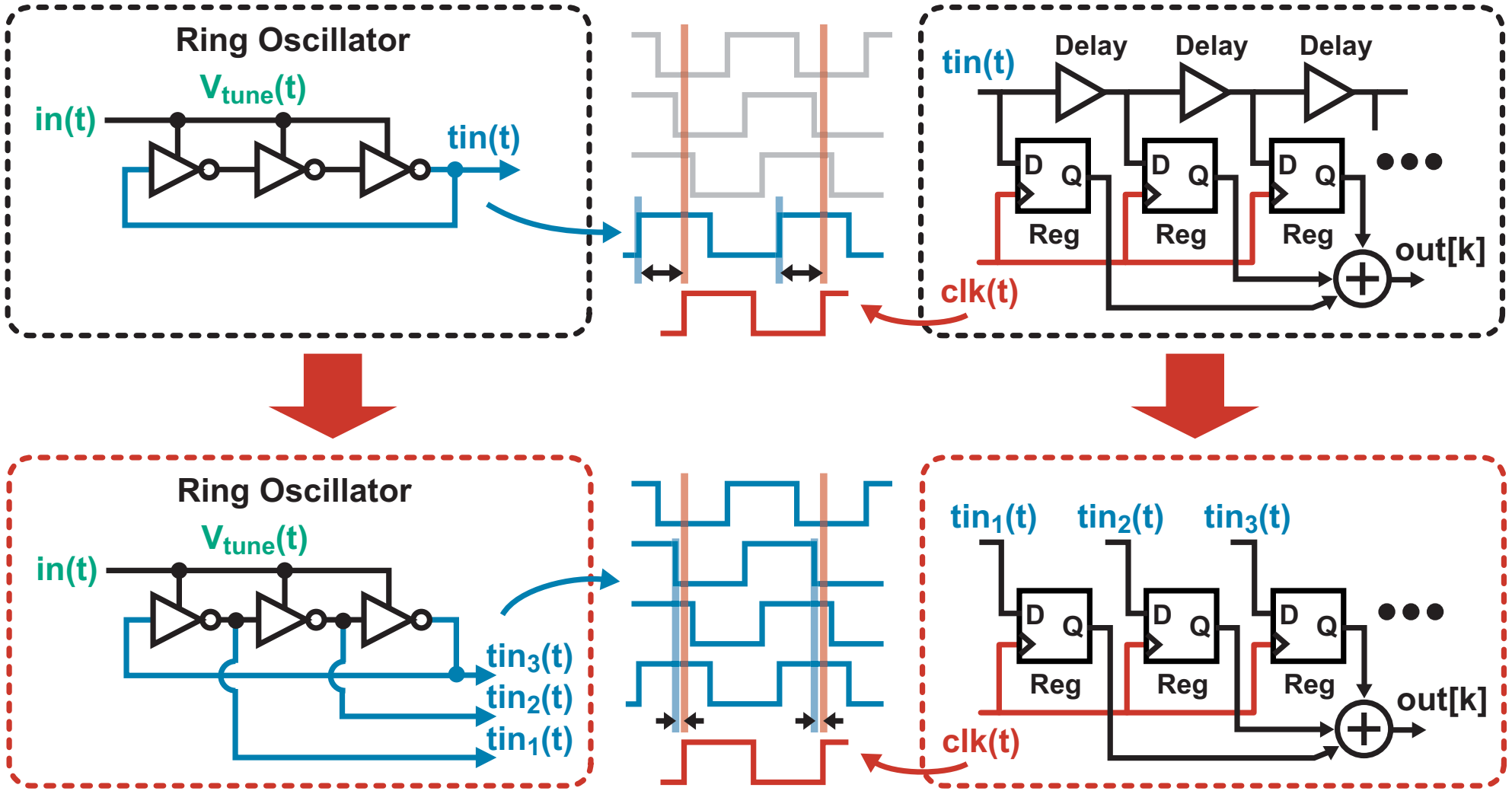
We can further simplify this implementation and lower the impact of non-uniform sampling

Making Use of the Ring Oscillator Delay Cells



- Utilize all ring oscillator outputs and remove TDC delays
  - Simpler implementation
- TDC output now samples/quantizes phase state of oscillator

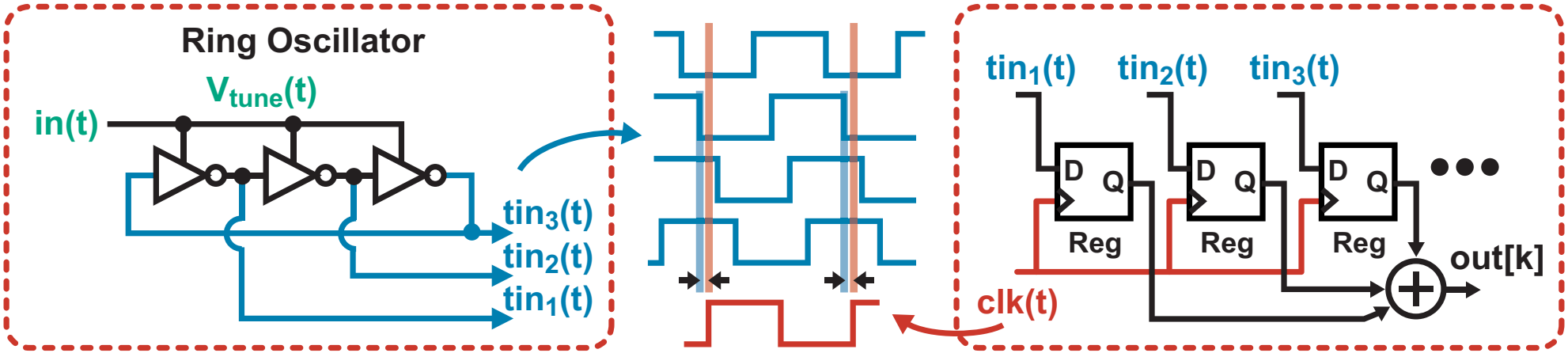
Improved Non-Uniform Sampling Behavior



- Oscillator edges correspond to a sample window of the input
- Sampling the oscillator phase state yields sample windows that are much more closely aligned to the TDC clk

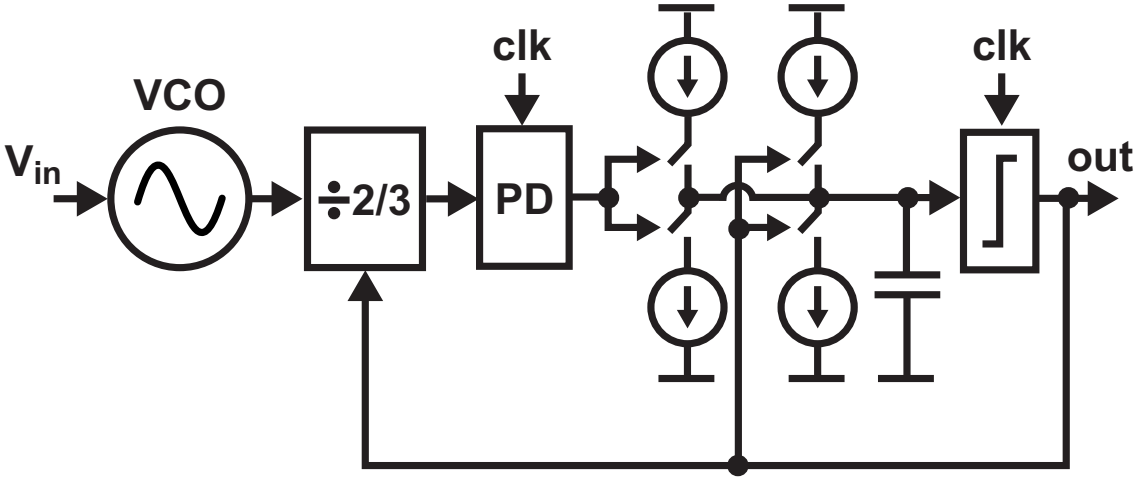
Key Observation

- **The VCO-Based ADC provides an excellent vehicle for using a conventional TDC for analog-to-digital conversion**
  - **Efficiently combines voltage-to-time and time-to-digital conversion**
  - **Minimizes issue of non-uniform sampling**



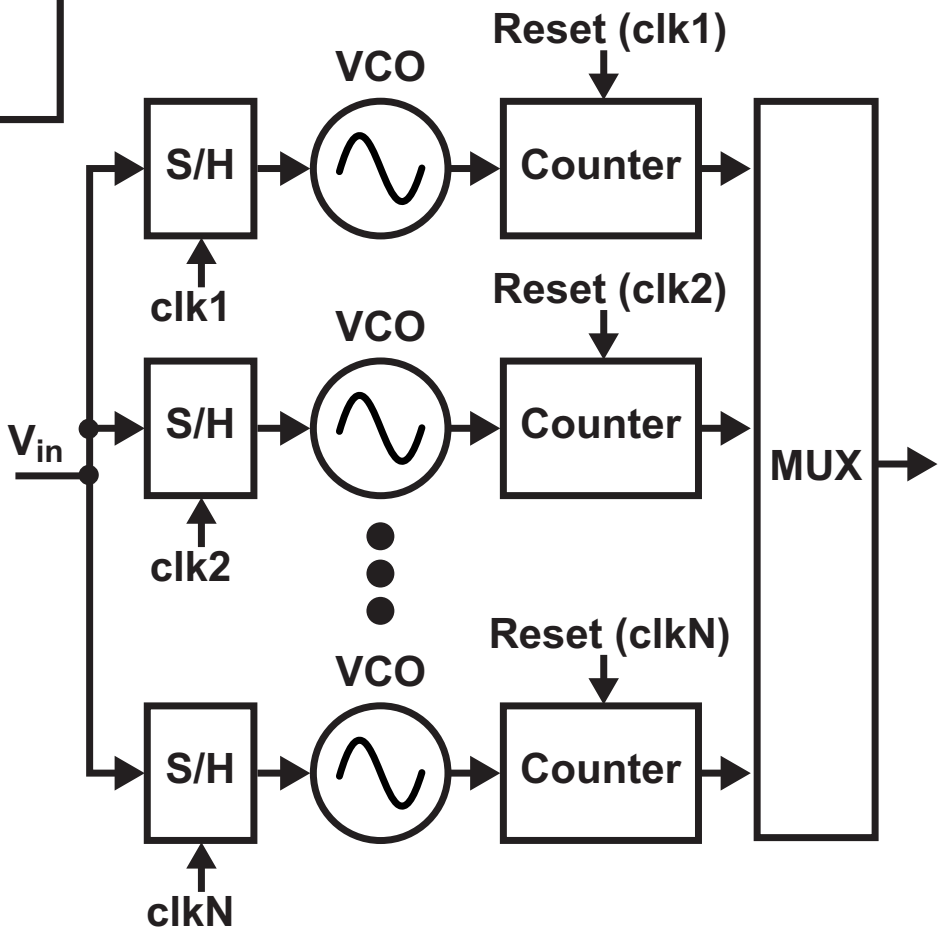
VCO-based ADCs are very efficient "time-based" circuits

Some Other VCO-based ADC Approaches



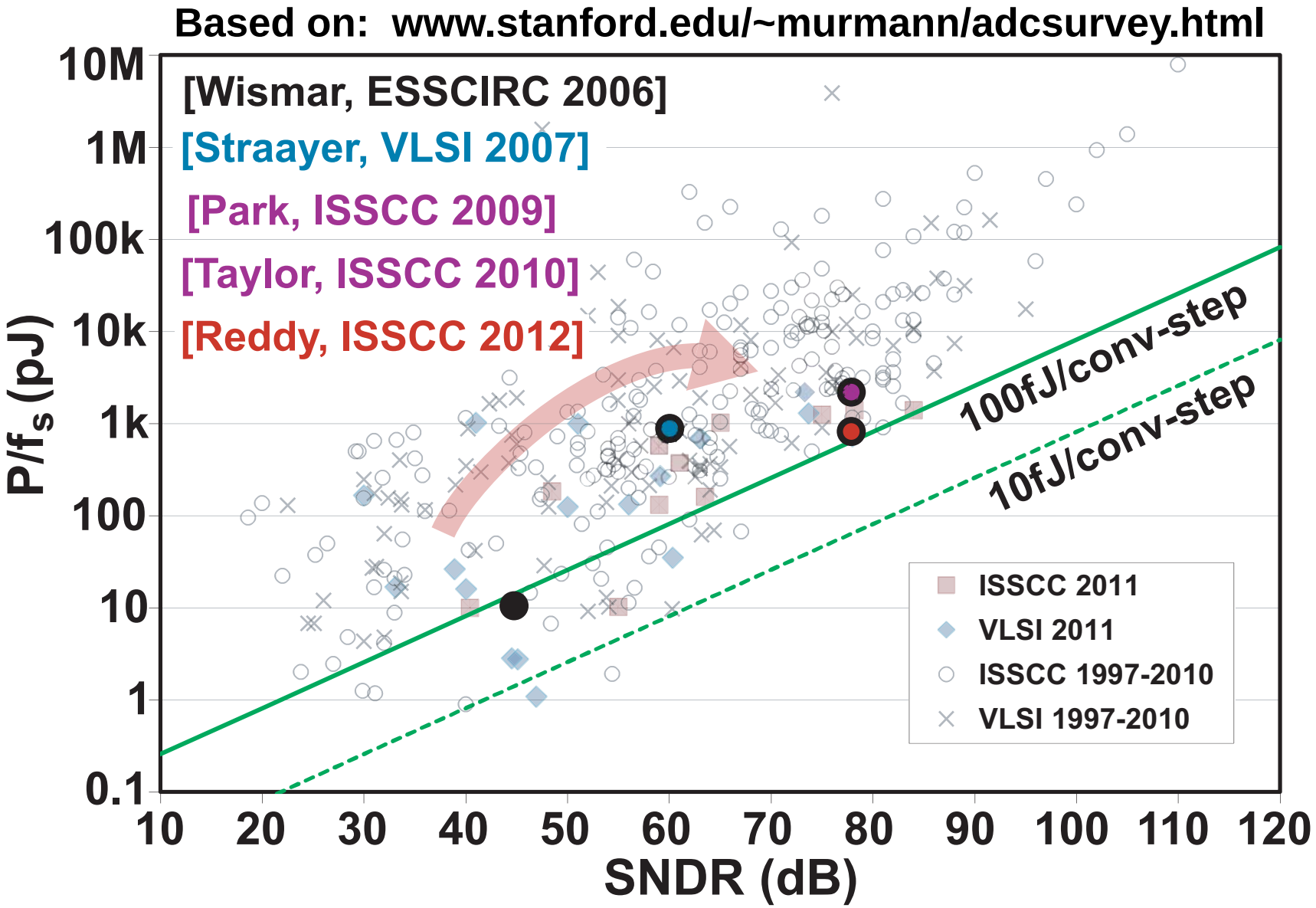
Park, Perrott
ISCAS 2009

Yoon, Kim, Jang, Cho
TCAS1 Dec 2008



- **Increase noise shaping to second order by adding frequency divider and charge pumps**
- **Use interleaved VCO quantizers to create bandpass ADC**

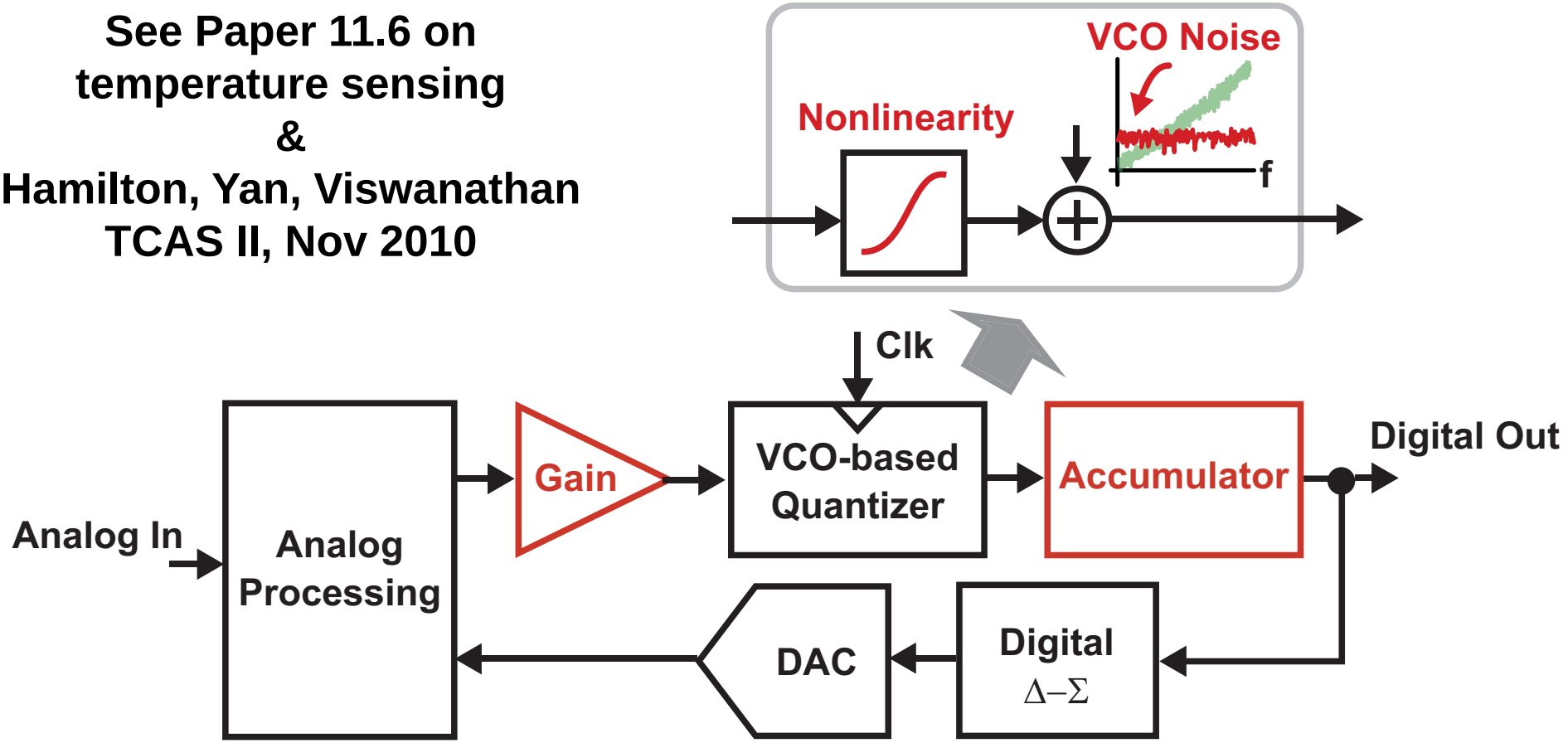
Recent Performance of VCO-Based ADCs



Approaching 100fJ/conv-step at 78dB SNDR

A Simple Interface Between Analog and Digital

See Paper 11.6 on temperature sensing & Hamilton, Yan, Viswanathan TCAS II, Nov 2010



- Accumulator reduces impact of nonlinearity
- Gain reduces impact of VCO phase noise

Plays well to the strengths and weaknesses of VCO-based quantizers

Conclusion on VCO-Based Quantizers

- **Leverage Moore's law**
  - **Consist of ring oscillator(s) and digital logic**
  - **Improved speed, power, area with advanced CMOS**
- **Are relatively easy to design**
  - **First order shaping of quantization noise and mismatch**
  - **Infinite DC gain when used as an integrator**
- **Have shortcomings that can be overcome**
  - **Nonlinearity: utilize calibration or feedback**
  - **VCO phase noise: utilize feedback**

Performance is now at state of the art at 78dB SNDR and improving steadily