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ISSCC 2012 RF and CT Delta-Sigma ADC Highlights

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Outline

- **Overall and RF Paper Statistics**
- **General Overview**
- **Trends in Wireless architectures**
- **RF Building Blocks**
- **Trends in CTDSM architectures**
- **Continuous-Time Delta Sigma Modulator ADCs**

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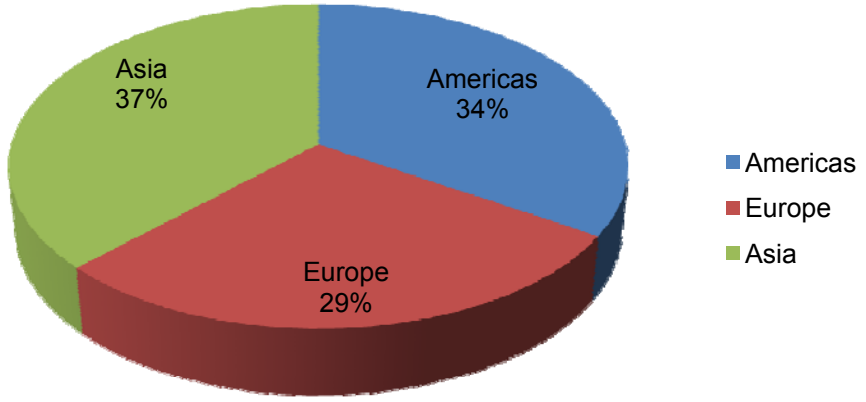
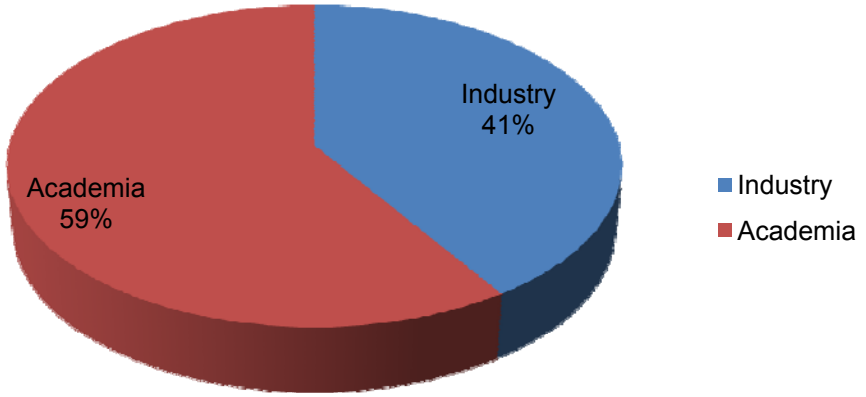
Overall papers statistics

- **206 papers were presented**
  - About the same as last year (211)
  - Organized in 28 sessions
- **More multinational than ever**
  - Australia, China, UAE, Singapore
  - Argentina, Israel, India, Canada
- **The papers were uniformly distributed**
  - Geographically
  - Academy vs industry





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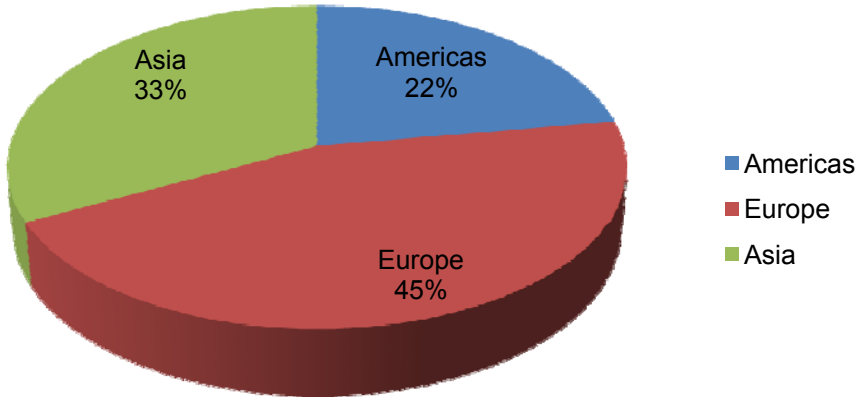
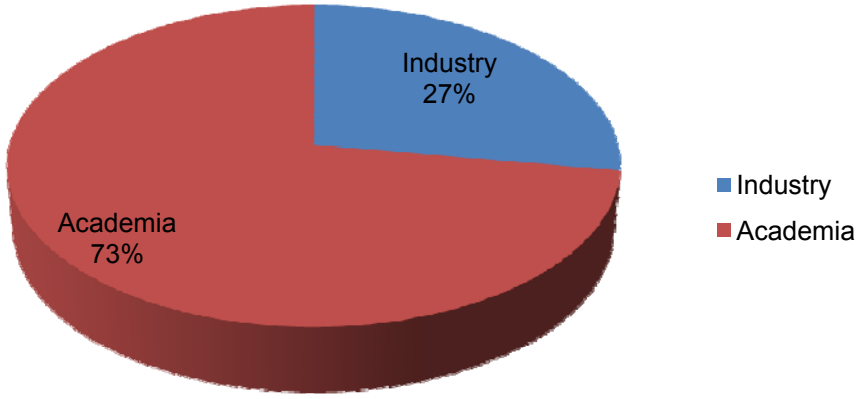
RF and CTDSM papers statistics

- **RF session titles:**
  - RF techniques
  - Wireless Transceiver Techniques
  - mm-Wave & THz Techniques
  - mm-Wave Design Techniques
  - RF frequency generation
- **Europe and Academia had a larger share**
- **CT-DSM**
  - 7 papers
- **RF Forums**
  - Beam-forming Techniques and RF Transceiver Design
- **RF Short courses**
  - Mixers: Analysis and Design
  - Digital Calibration in RF Transceivers





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General Overview

- **RF and ADC topics were fairly diversified**

- **On RF side, however, two trends stood out**
  - Blocker Tolerant Receivers
    - Current mode operation
    - RF tracking filtering at the receiver input
    - Distortion cancellation
  - Integrated CMOS Power Amplifiers

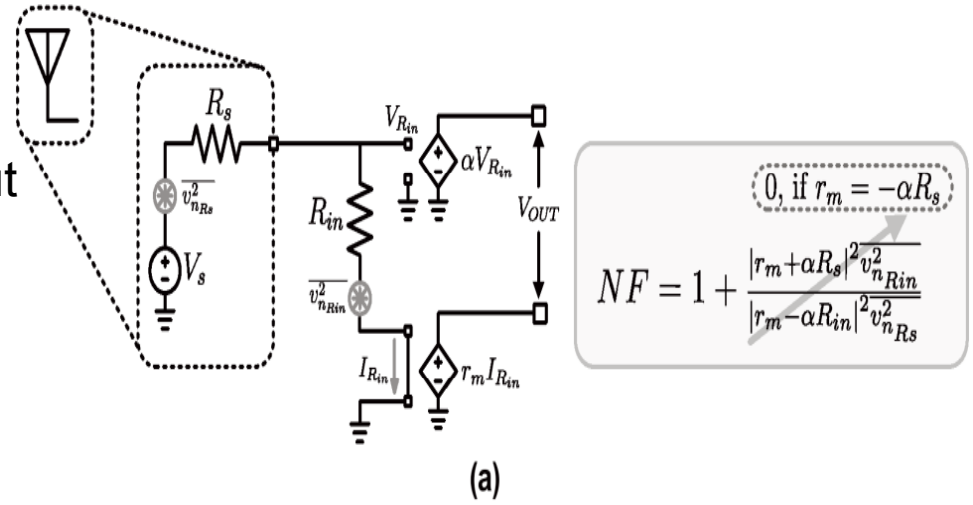
- **On the CTDSM ADC side**
  - Low power and high speed designs
    - VCO-based designs
    - FIR DAC based designs

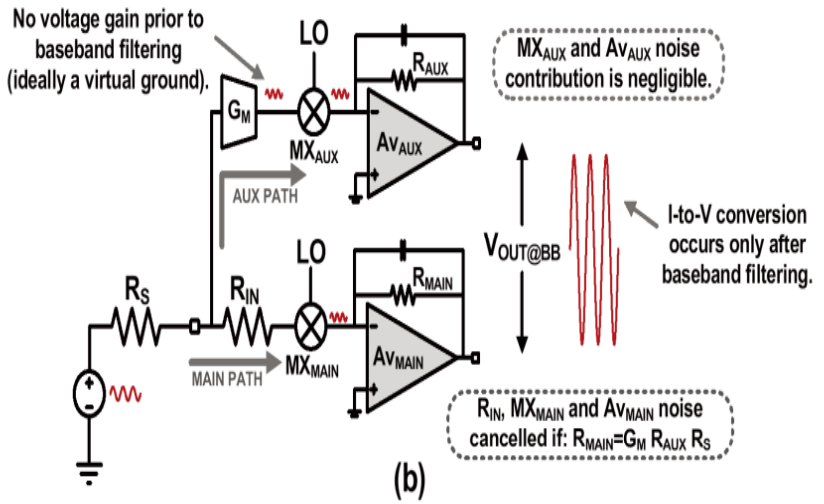
Blocker Tolerant Receivers

- **Near-Far problem**
  - Receiving weak signals in presence of large blockers
- **Conventional approaches**
  - Reduce the gain
    - NF will suffer
  - Use RF LC tracking filter
    - BOM and tuning range
- **New approaches**
  - Avoid large voltage swings till filtering has occurred in baseband
    - RF current mode operation
  - Use non-LC based RF tracking filter
    - Switched capacitor N-path filtering
  - Cancel the distortion products of different blocks
    - Match the distortion

4.1: A Blocker-Tolerant Receiver

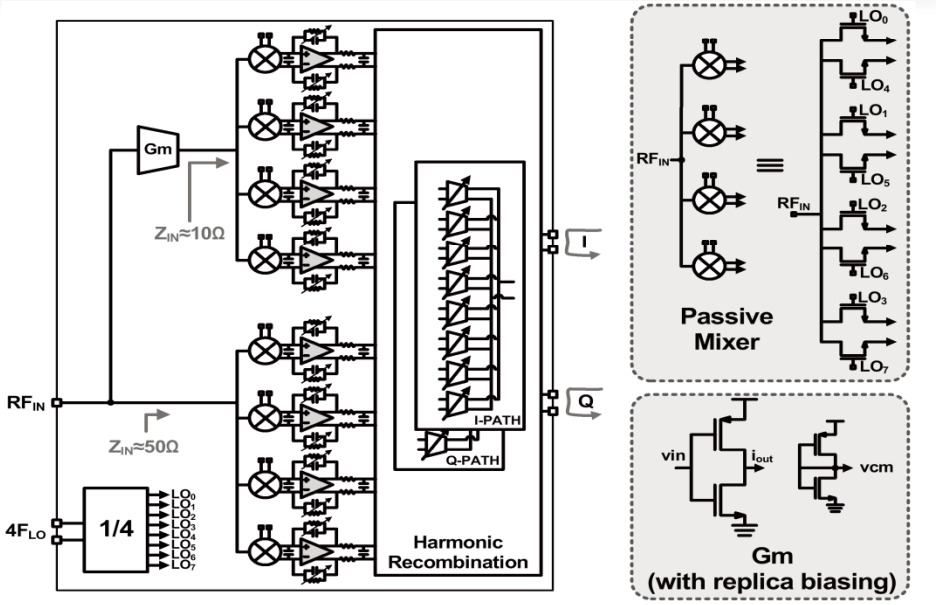
- **Based on Noise Cancelling LNA**
  - Input transistor noise sensed in two paths
  - Cancellation at the differential output
- **Nonlinearity still an issue**
  - Large output swing due to blockers
- **Key idea: RF Current mode**
  - Use linear RF V/I converters
  - Sense Rin noise in two current paths
  - Mix both current paths to baseband
  - Filter two paths before I/V
  - Subtract the two output in Baseband
- **What about the extra blocks noise**
  - Main opamp noise is cancelled
  - Aux opamp noise seems a gain of 1
  - Gm noise is not cancelled (power)





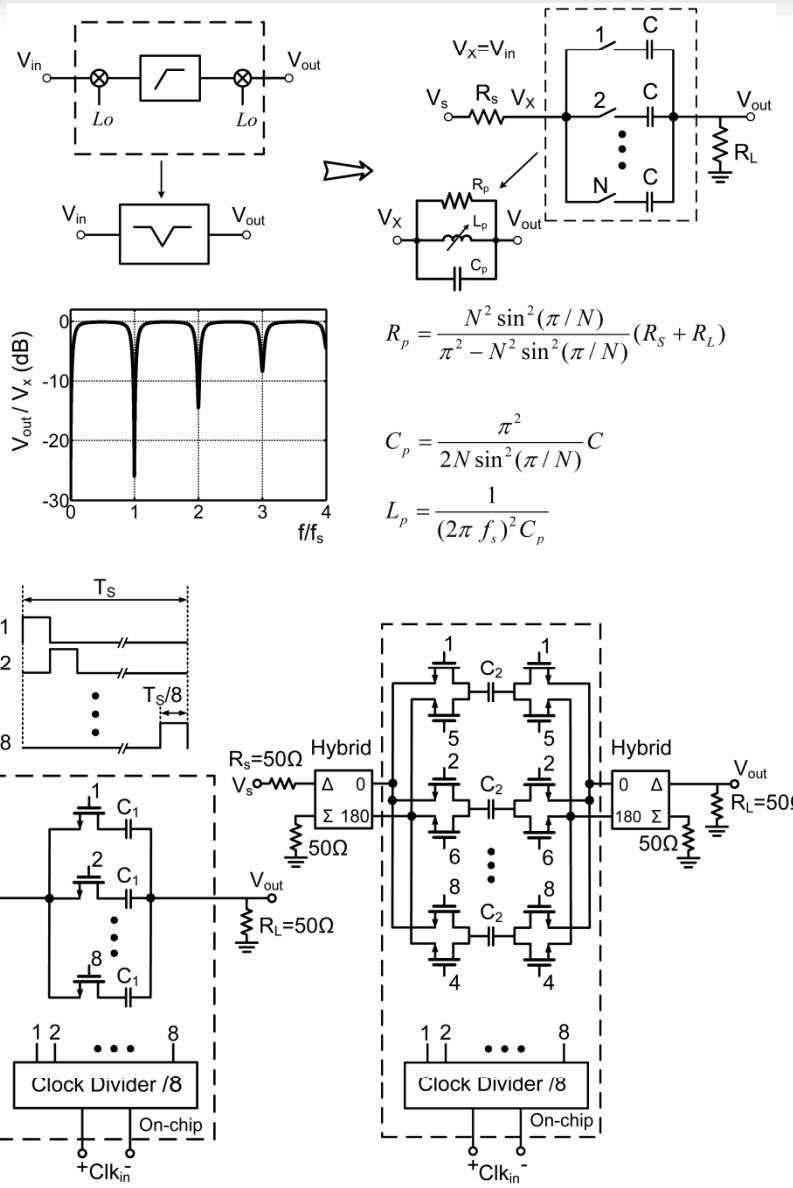
4.1: A Blocker-Tolerant Receiver (cont.)

- **All amplifiers are based on inverters**
  - Current reuse
  - Self biased replica biasing
    - Minimize DC current into mixer (1/f noise)
- **8-phase non-overlap mixing**
  - Less noise folding
  - I/Q and HRM through BB Gm weighted summation
- **Single-balanced mixing**
  - Sensitive to uncorrelated LO/LOb noise
  - Use retimed barrel shifter to correlate the noise
- **Fairly robust against gain and phase mismatch between the two paths**
- **IIP3(OOB) = 13.5dBm, IIP2 = 54dBm**



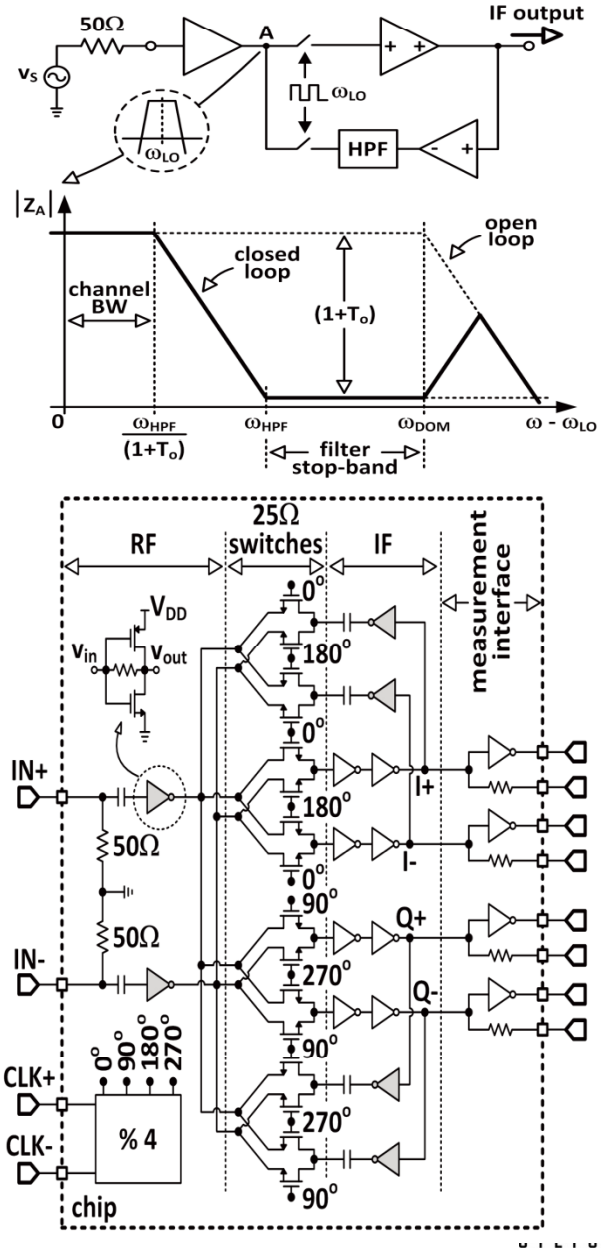
4.2 8-path tunable RF notch filter

- **Weaver architecture**
  - LPF and up and down conversion
- **All-Pass – Notch = BPF**
- **N-Path approach**
  - N non-overlapped down converters
  - C-R network for HPF
  - Shared R at the output
  - One current is on at a time
    - Output switches replaced by Current summation
- **Equivalent RLC network**
  - Fixed BW (L= α/f_0^2, R,C independent of f_s)
  - Larger N → Better Rejection
    - Folding at (N+-1)Fs.
- **Differential Mode**
  - No 2Fs rejection (Wider BW)
  - Twice the capacitor
  - Extra output switches
  - Larger antenna coupling (-60dBm)



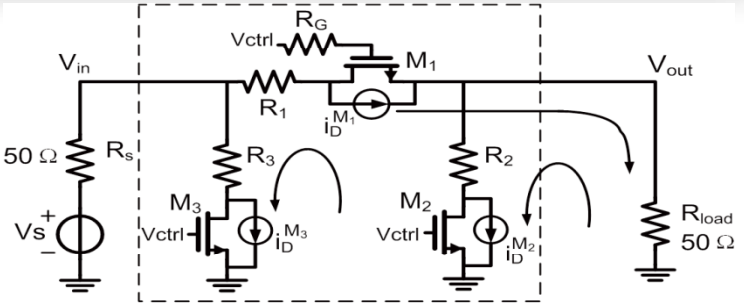
9.3: Feedback receiver with tunable filter

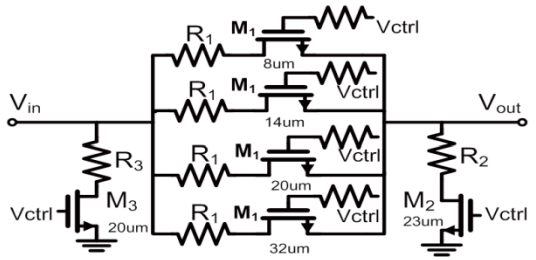
- **RF input N-Path filtering issues:**
  - Low R → Large C
  - SW's Ron affects rejection
  - Antenna LO coupling
- **Key idea: Put N-path after a Gm**
  - LO coupling is reduced (S12)
  - Synthesize BPF through FB with HPF
  - LNA output distortion improves
    - LNA output BPF rejects the blockers
  - BW = BW_HPF / Loop_Gain
    - Smaller capacitor
  - SW are in series with CS
    - Ron does not affect the rejection
  - Use self biased inverters for amps
    - Current reuse
    - No bias network
- **LNA input distortion is not cancelled**
  - The in-band IM3 product will be treated as desired and hence not cancelled.

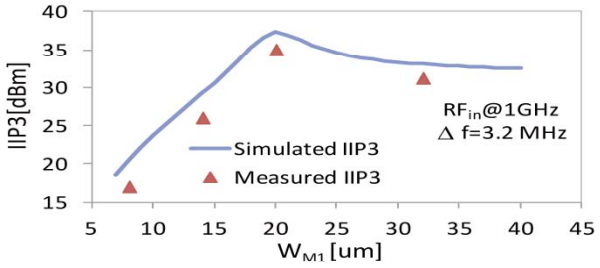


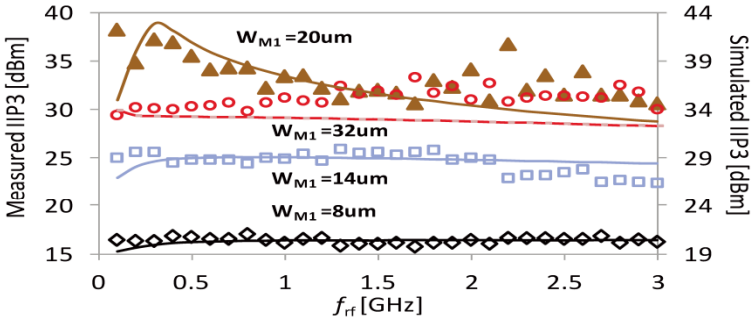
4.3: A wide-band IM3 cancelling technique

- **Dynamic range expansion using Attenuators**
  - Engage when Pin is too large
  - They become the linearity bottle neck themselves
  - Signal dependent Vgs and Vsb (Back gating)
- **Conventional Techniques**
  - Cascading (larger Tr → More nonlinear cap)
    - Used in SOI
  - Gate and bulk boot-strapping
- **Key idea: Cancellation**
  - IM3 current of main and parallel devices flow in opposite directions
  - $V_{out} = \frac{3V_{in}^3}{(1+A)^4 16R_s^3}\left[\frac{16A^4}{W^3_{M_1}} - \frac{(1-A)^4A^3}{W^3_{M_2}} - \frac{(1-A)^4A}{W^3_{M_3}}\right]$
  - Cancellation depends of W ratios (PVT tolerant)
  - Each A needs its own W ratios
  - Higher freq causes current phase shifting from 180
    - Less cancellation
  - Higher-order distortions (say 5th) are not cancelled.









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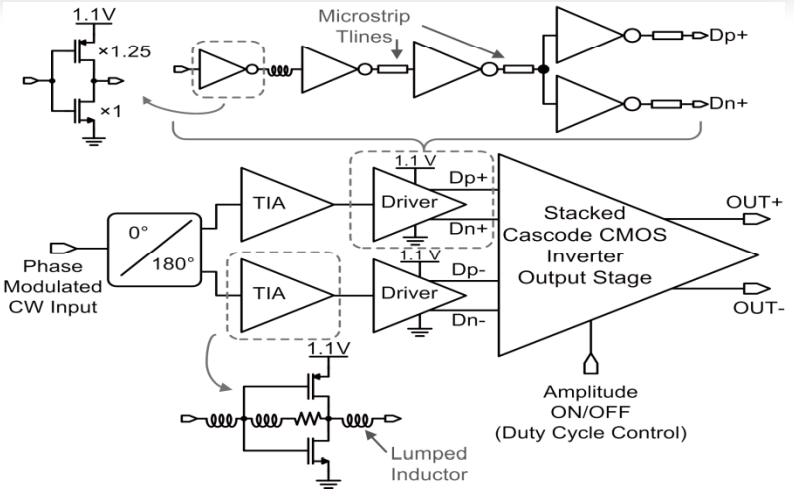
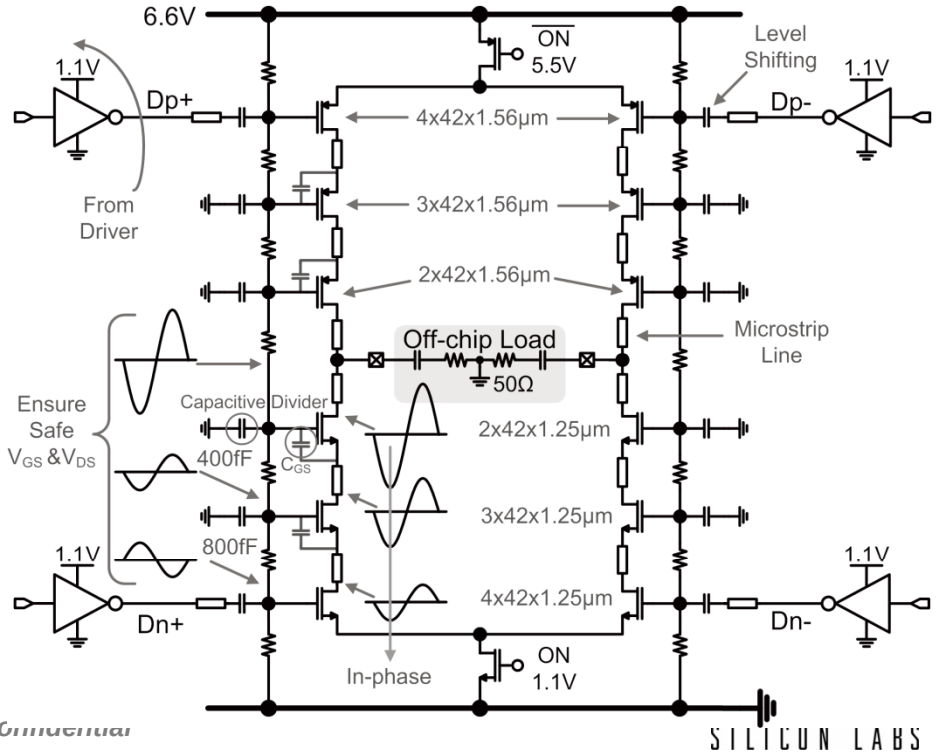
4.8: 45nm SOI Class-D mm-wave PA

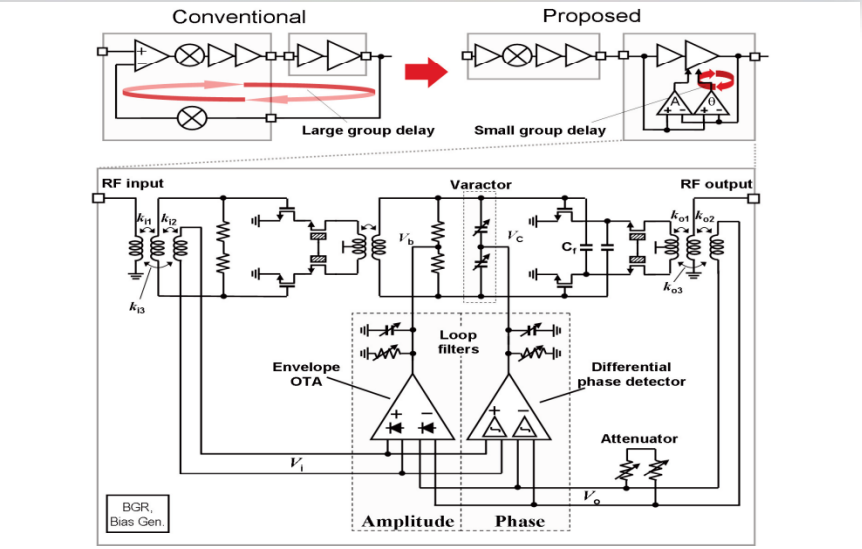
- **GaAs is the PA process of choice**
  - SOI → no Junction cap
  - Large break down voltage
- **CMOS PA**
  - Low BV → Small Vswing
  - Large current → Large Device → Cpar
  - More loss in impedance matching
- **Key idea: Cascading**
  - 6 devices between 6.6V and ground
    - 1.1V per device
  - Symmetric SOI process
    - 3 PMOS. Each 1.25x NMOS
    - >10V Vsb and Vdb
  - Resistive ladder gate biasing
  - Gm scaling for source swing settings
  - AC coupling to gates
  - In-phase G/D/S swings

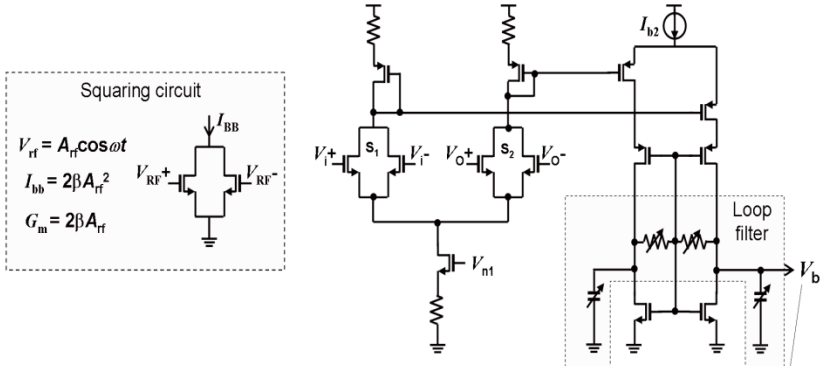


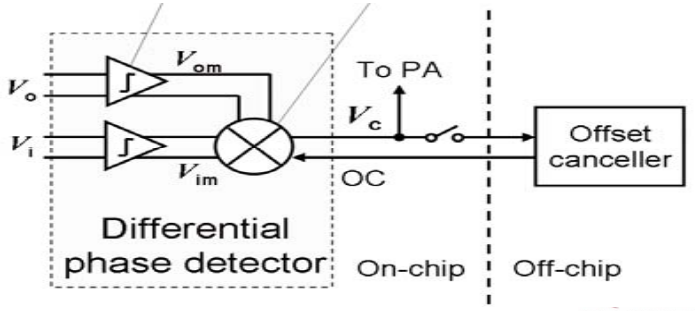


4.6: Closed Loop PA

- **PA linearity in WBCDMA**
  - ACPR due to spectral regrowth
- **Feed forward techniques**
  - LU table based
  - Sensitive to PVT and antenna load
- **Feed back based**
  - Narrow band
- **Key idea**
  - Use feedback around the PA (Wide-band)
  - Use polar feedbacks with no LO mixing
  - Pass both RF and BB through the same detector
    - Turn detector nonlinearity to CM
  - Use squarer for amplitude detection
    - Tail current controversy
  - Phase comparator uses limiter and mixing
    - No LO is used
    - DC offset at the output needs to be canceled

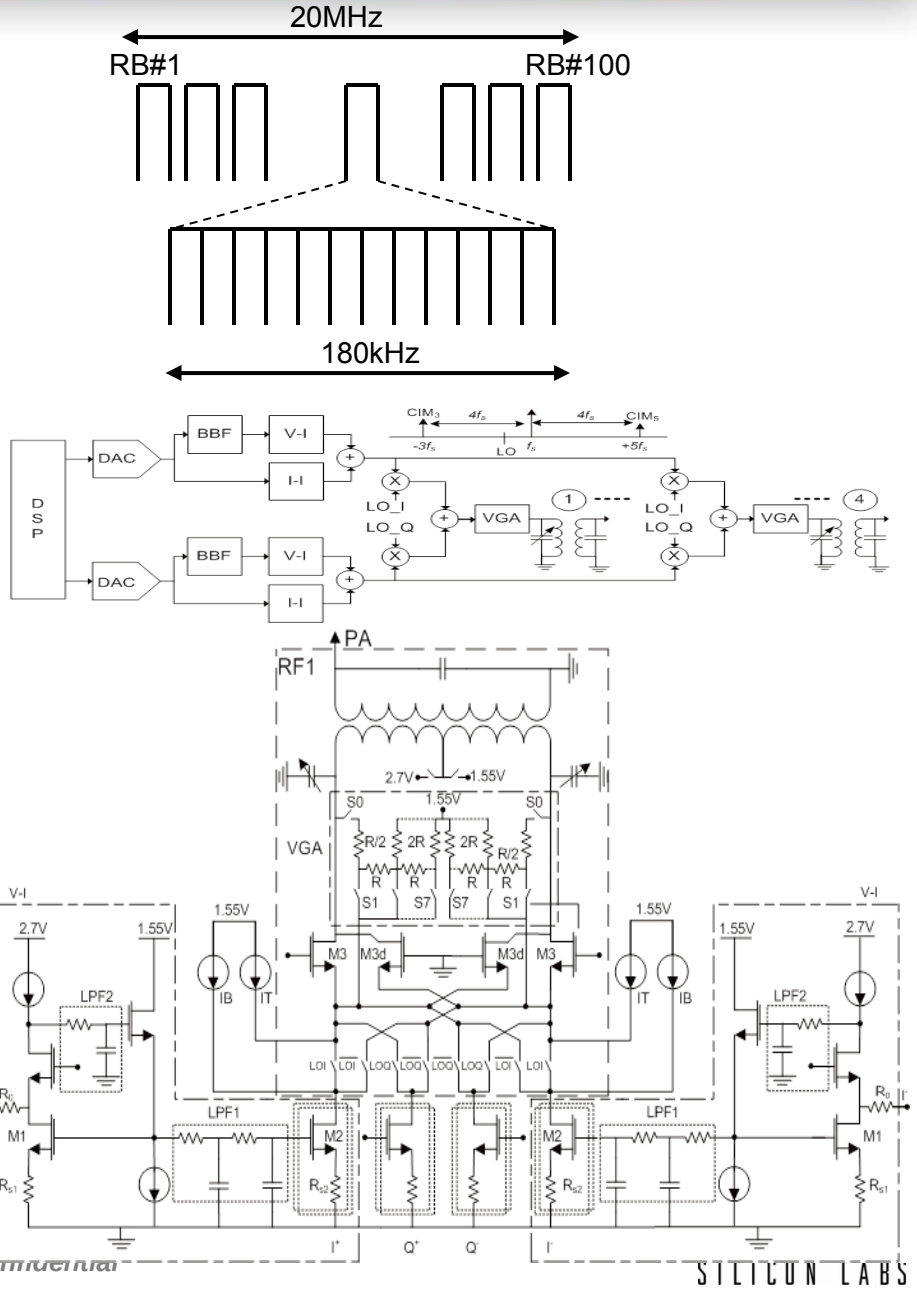






9.2: LTE multi-band TX PA

- **LTE (4G) imposes new challenges**
  - SAW-less operation
    - TX with low noise and low distortion
  - Counter inter modulation (CIM)
  - Single RB CIM falls in adjacent band
- **2G/3G/4G simultaneous operation**
- **Key idea: Remove PA driver**
  - Enhance noise and distortion
  - CS DAC directly to PA
    - In 4G use I/V filtering and R-based V/I (linearity)
    - In 2G/3G use I/I (noise)
  - Small Iac/Idc in Baseband
  - Large Iac/Idc in RF
    - Use current sources to divert Idc
  - 72dB gain range
    - BB slices provides 30dB gain
    - Another 42dB in load R/2R network
  - Use neutralization to stop RF leakage
    - Reduces the gain range

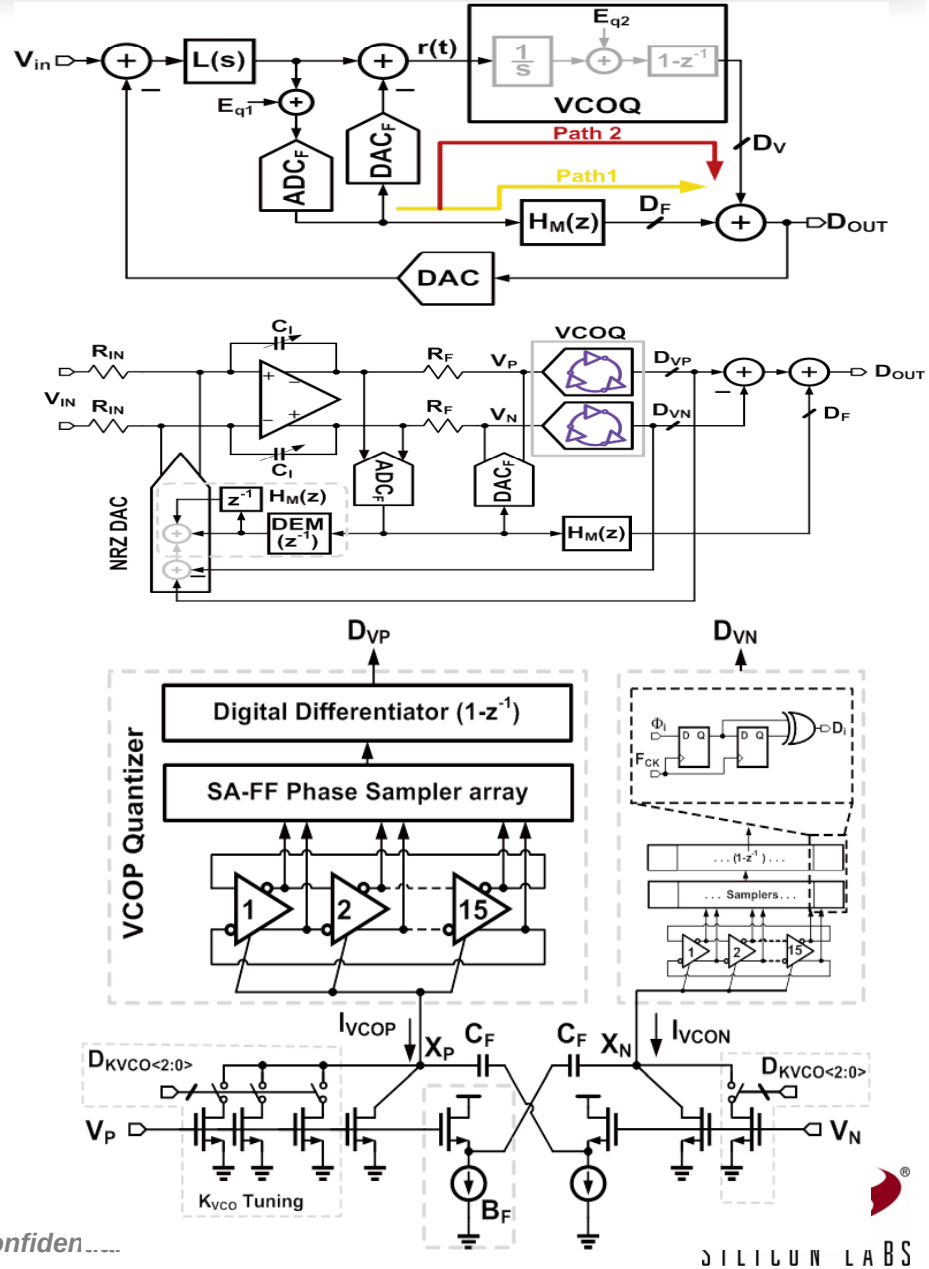


Trends in CTDSM's

- **CTDSM's are very popular**
  - Lower power
  - Higher Signal BW
- **General Issues**
  - RC variations → Calibration
  - Jitter sensitivity → Multi-bit feedback
  - Excess loop delay in high Fs application
- **New ideas:**
  - Use VCO-based ADC's for quantizer
  - FIR based DACs to reduce jitter sensitivity
  - Speed enhancement techniques

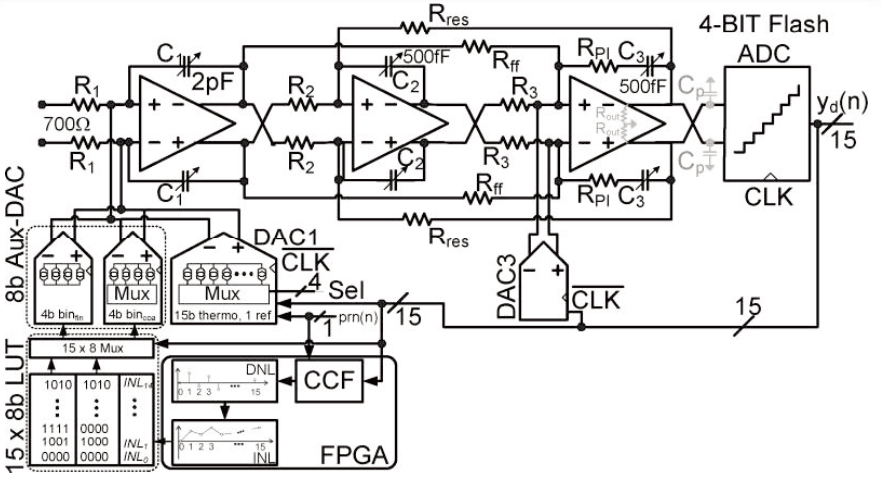
8.4: CTDSM with VCO based quantizer

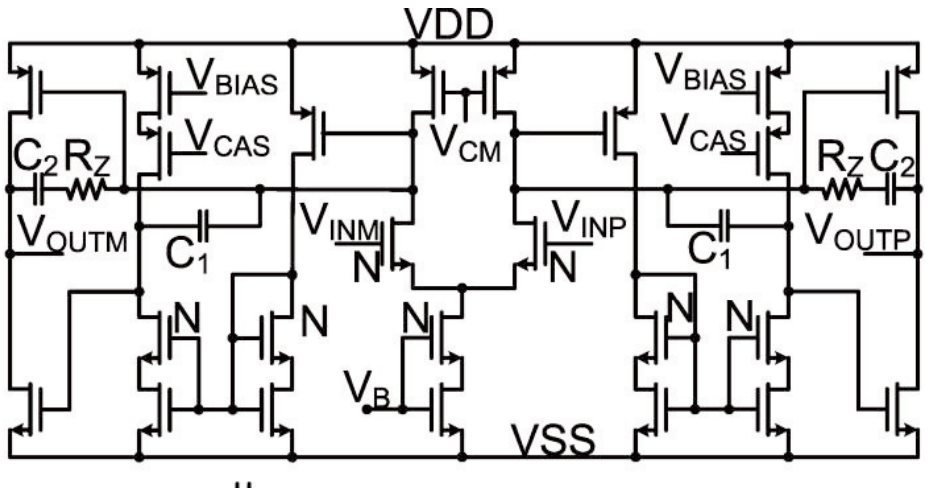
- **VCO based quantizers**
  - Small area, low Vdd
  - Resolution improving with finer line processes
- **But they are nonlinear**
  - Use calibration (sensitive to PVT)
  - Use feedback (need large GBW)
- **Key idea: Reduce swing**
  - Use a 4-bit coarse quantizer in front
  - VCO-based ADC handles only the residue
- **Feedback DACs**
  - CS with make-before-break switches
  - Use DEM to improve distortion
- **V/I delay in VCO -> Excess loop delay**
  - Pole at Xp due to Cpar and Rvco
  - Add a feed-forward path
    - LHP zero cancels the pole
    - No need for Excess loop delay feedback



8.5: Low power CTDSM with Aux ADC

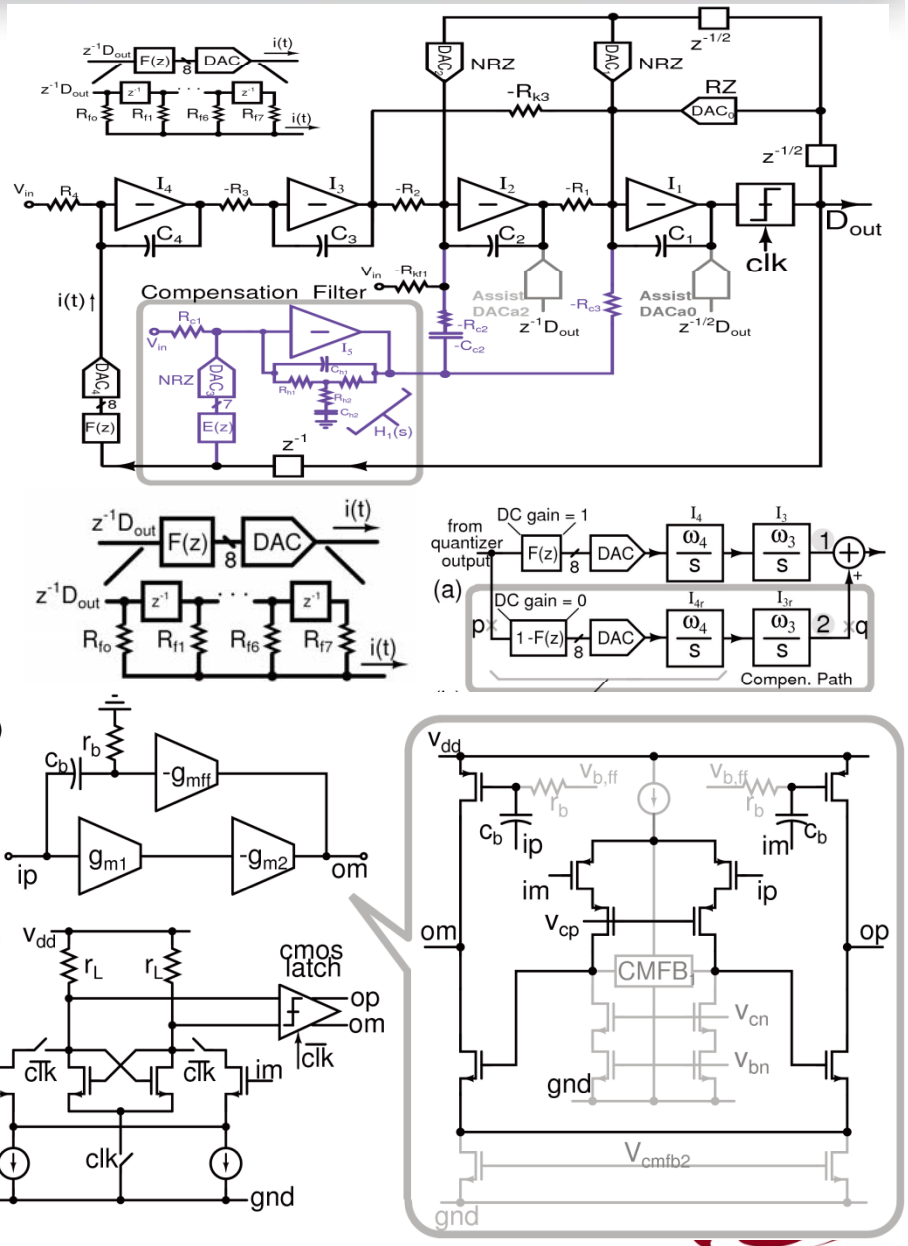
- **Low Power Multi-bit CTDSM**
  - Low OSR and Low order
  - Linearity Concerns
    - High GBW, low Excess loop delay
    - DAC INL: Often DEM is employed
      - Does not work well for low OSR
- **Key ideas:**
  - Calibrate FB DAC
    - Use smaller DAC (low Cpar)
    - Use a spare leg (Back ground Cal)
    - Use PRN sequence and correlation
    - Correct via an Aux DAC
  - ELD comp. without combiner
    - Use R in the last integrator FB
  - Use native devices in the opamp
    - Reduce headroom → low Vdd
  - Calibrate RC and Idac
    - No PVT variations





8.6: CTDSM with FIR DAC

- **A different low-power CTDSM**
  - Argues for single-bit architecture
    - Less comparators, Less ELD
    - No DEM
  - Single-bit Issues
    - Jitter, 1st opamp swing (linearity)
- **Key idea: FIR DAC**
  - Jitter and 1st OP swing issues are solved
  - Large ELD though
  - Use 1-F(z) path to compensate
- **Circuit techniques**
  - OPamps
    - Use Aux DACs to charge the caps
    - AC couple the FF path and current reuse
  - Comparator
    - Usual dual latch to combat meta-stability
    - Use CML architecture
    - No tail current for regeneration (Full swing)
  - R DACs: Low noise and distortion



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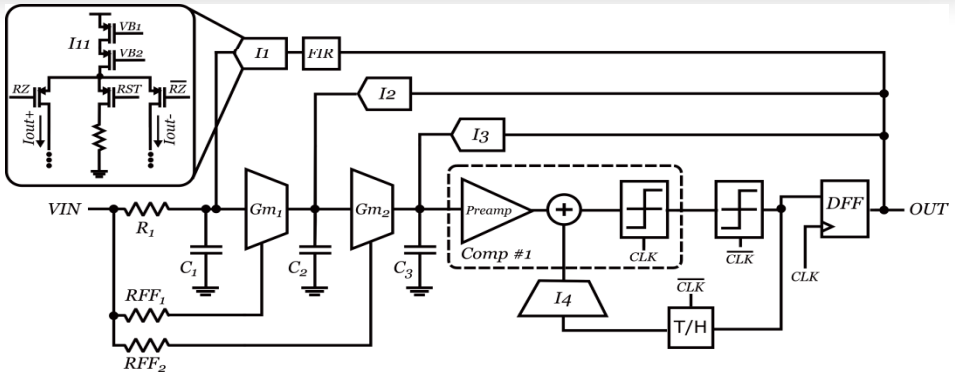
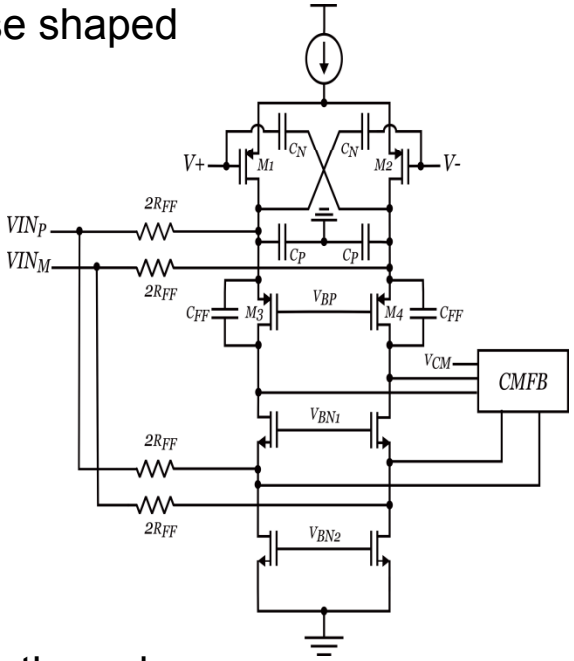
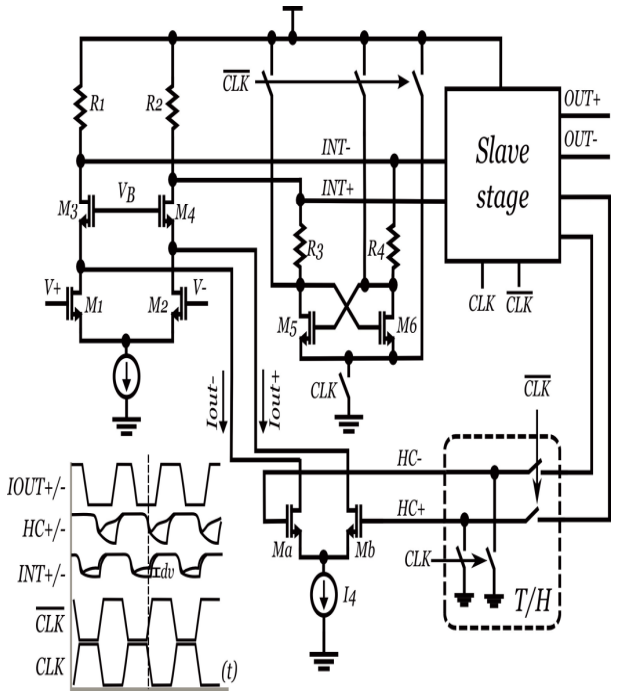
8.7: 6GHz CTDSM

- **High Speed Challenge: ELD**
- **Solution:**
  - Use a single-clock feedback
  - Meta-stability needs dual latches
    - Parasitic delay compromises ELD
- **Key idea: FB after half a cycle**
  - Main FB after full cycle
  - Meta-stability is rare and noise shaped
- **Comparators**
  - Preamp gain and BW
    - Split the load
  - Regeneration
    - Reset to remove memory
    - R3/R4 isolate Slave's Cpar
- **Opamps**
  - Resistive feed-forwards
  - Neutralization
  - C_{FF} provides a zero canceling the pole







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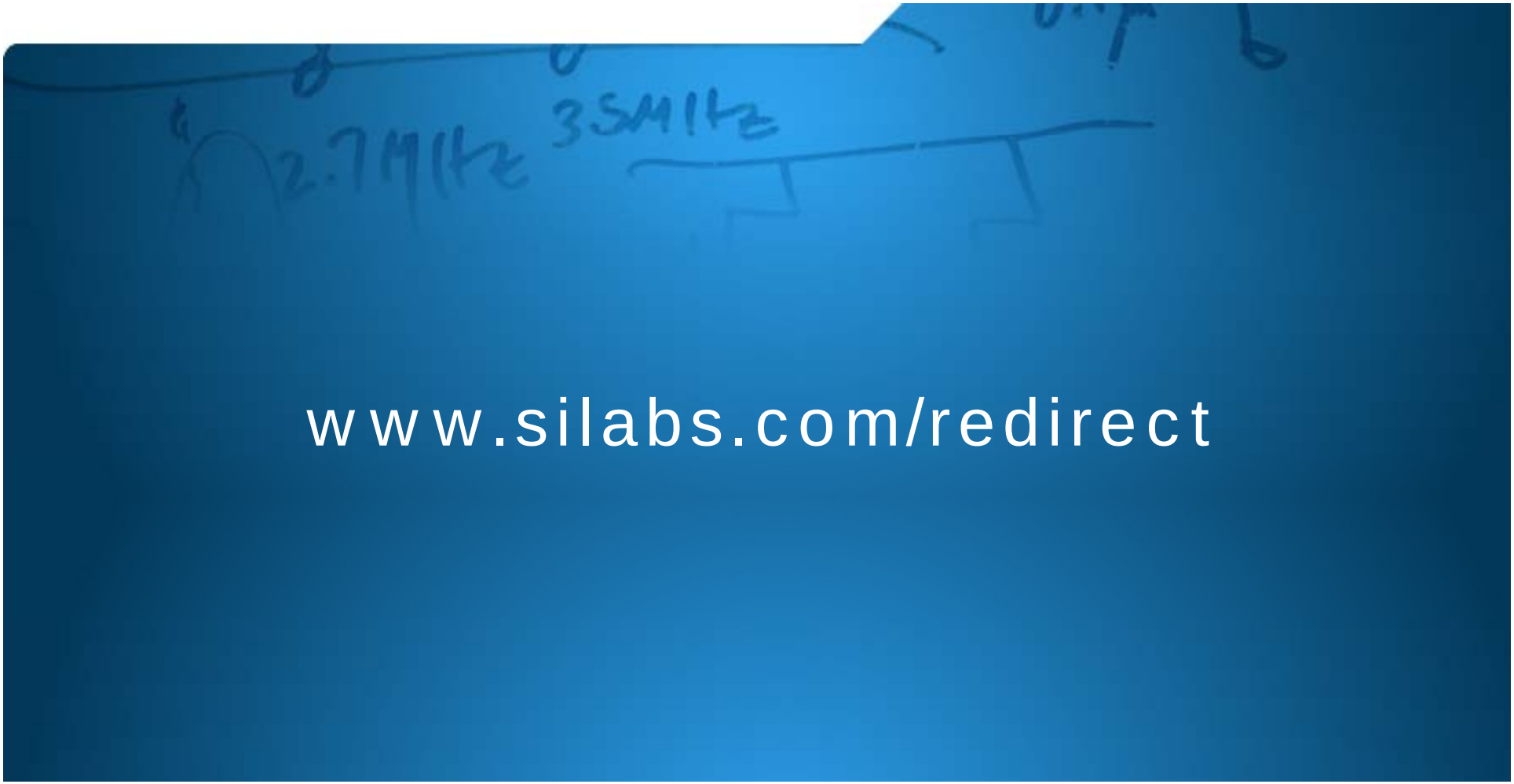

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