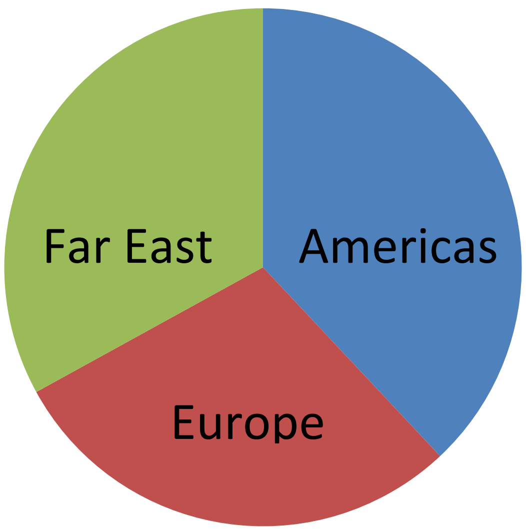
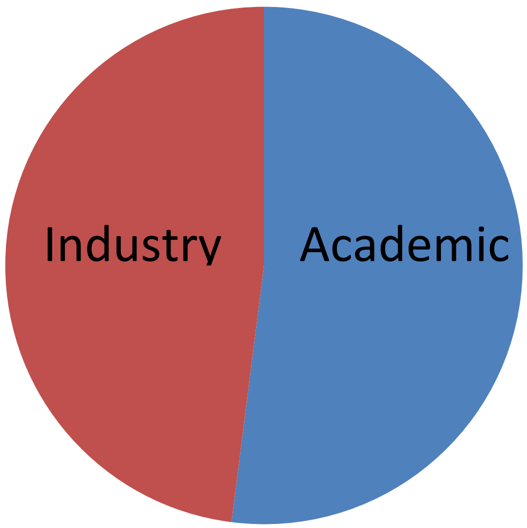
2012 ISSCC
Analog Paper Highlights

Matt Felder

ISSCC Statistics

- 628 submissions and 202 accepted papers
- 28 Sessions
- Attendance of 3,003 holding steady from last yr





Analog Paper Statistics

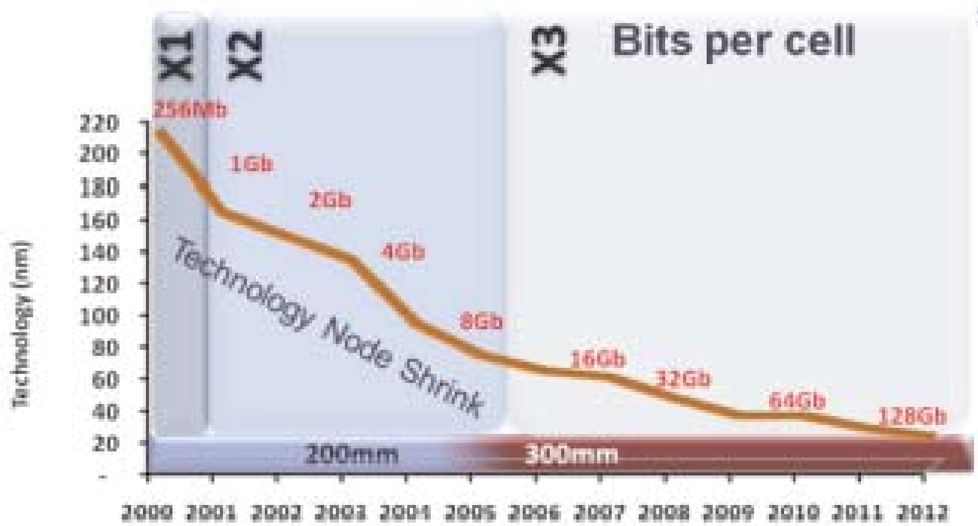
- The median analog design node is 0.13μ
- 5 analog papers in 22-45nm
- Not including RF or power converters here

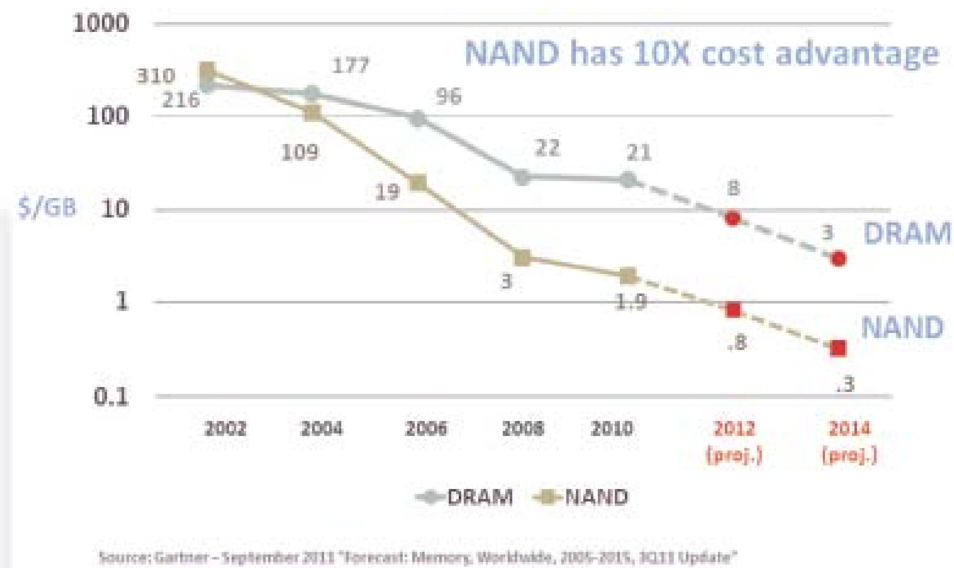
ISSCC Themes / Trends

- Quantization in time used extensively because it scales well in advanced processes
- Ring Oscillators used for everything (scale nicely)
- Not one DT Sigma-Delta presented, indicating perhaps that this has matured and is less favorable in advanced processes
- However, resolution is limited in CT ADCs, nothing above 14 bit resolution this year
- Two-stage (coarse/fine) conversions used for better power vs performance
- Noise shaping everywhere… it's not just for SigmaDelta ADCs anymore
- Extensive complexity opening new market opportunities (0.0001°C accurate temp sensor)

1.1 Flash Memory – The Great Disruptor Eli Harari of SanDisk

- Flash memory cost dropped 50,000X in 20 yrs



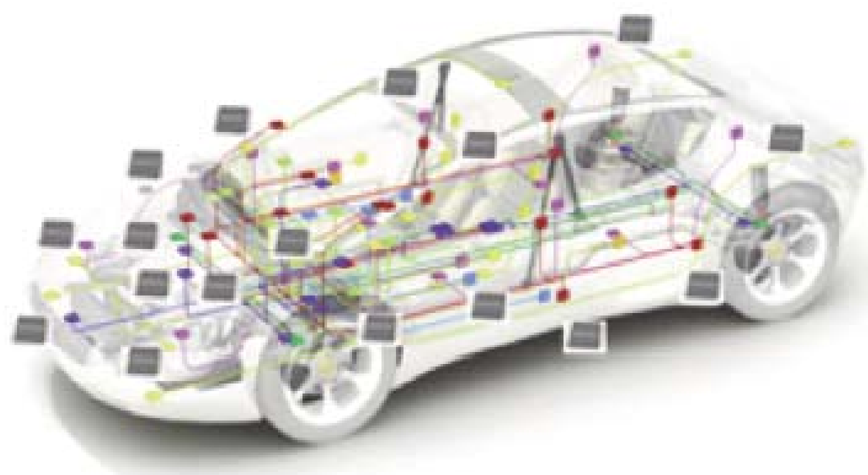


Physical scaling: 210nm→160→130→90→70→56→43→32→24→19nm

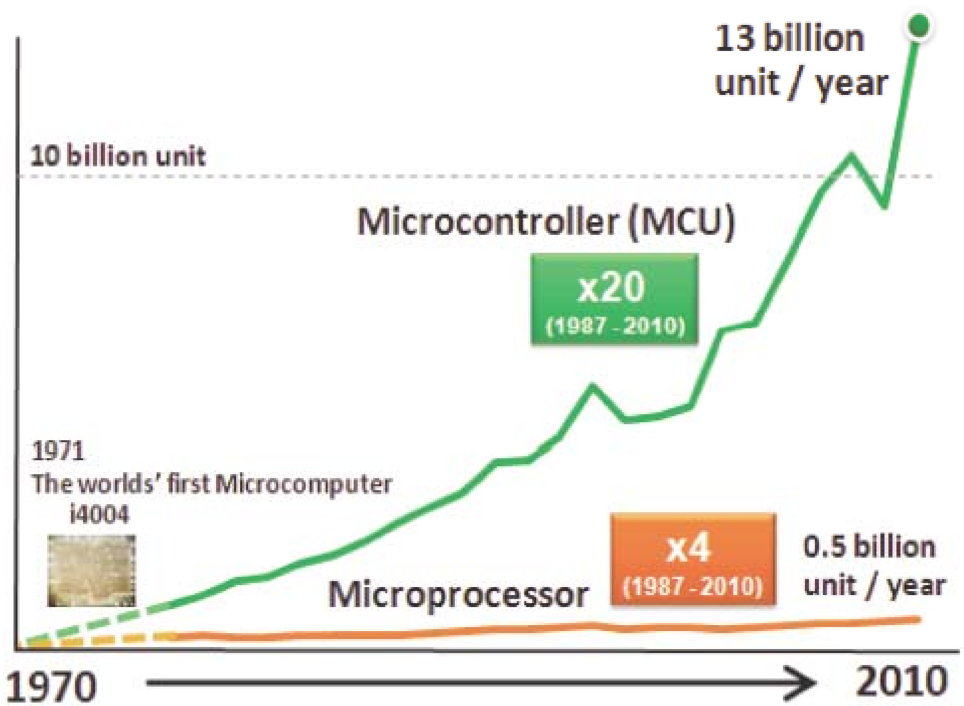
Logical scaling: X1 (SLC) → X2 (MLC)→ X3 (TLC)

1.3 Yoichi Yano of Renesas

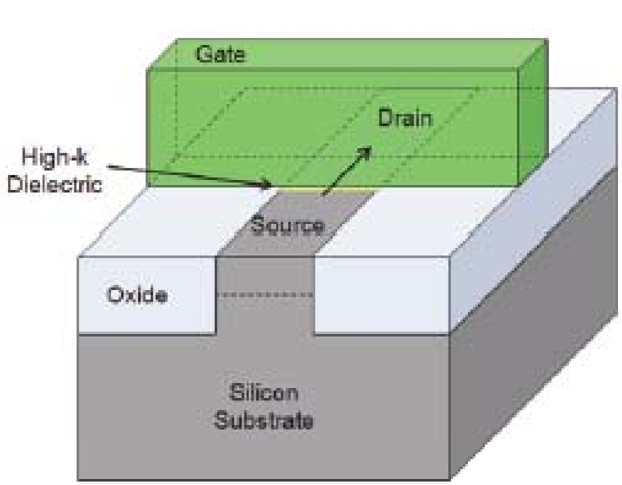
More than **100 of MCUs** in the Home



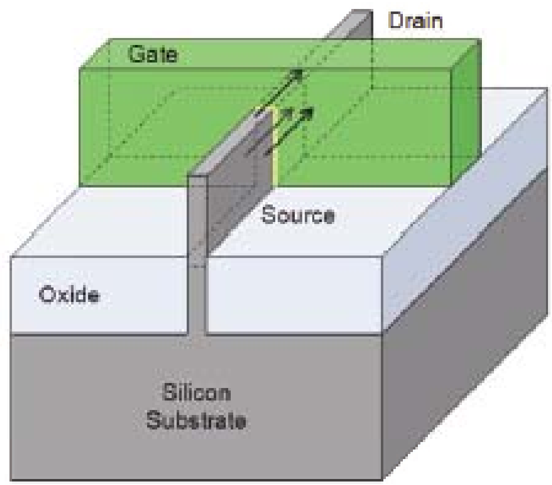
50 to 100 of MCUs in the Car



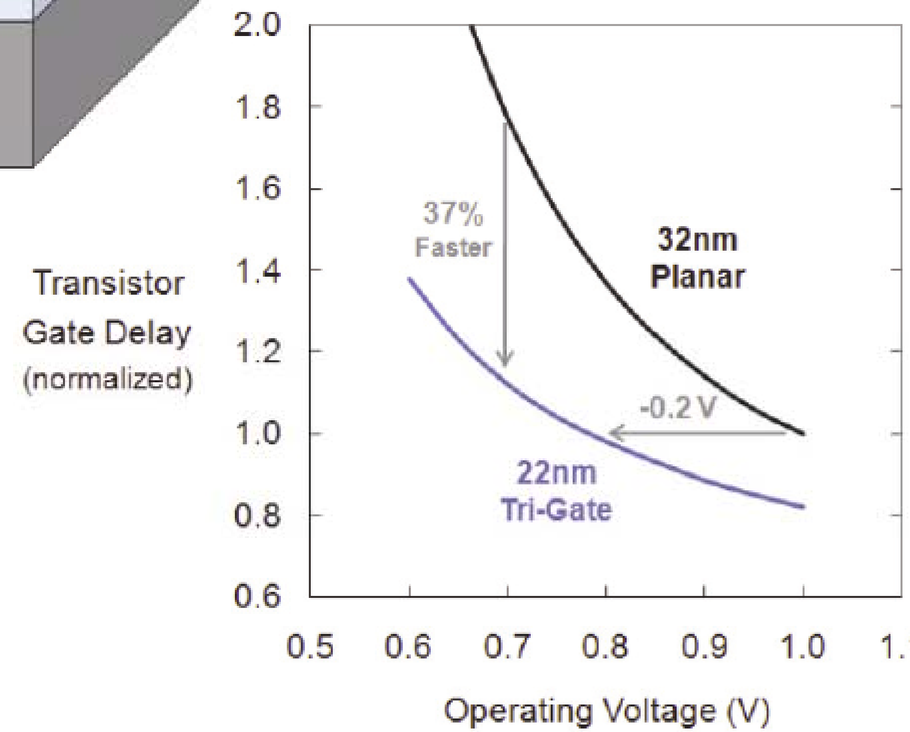
1.4 David Perlmutter of Intel



32nm Planar FET

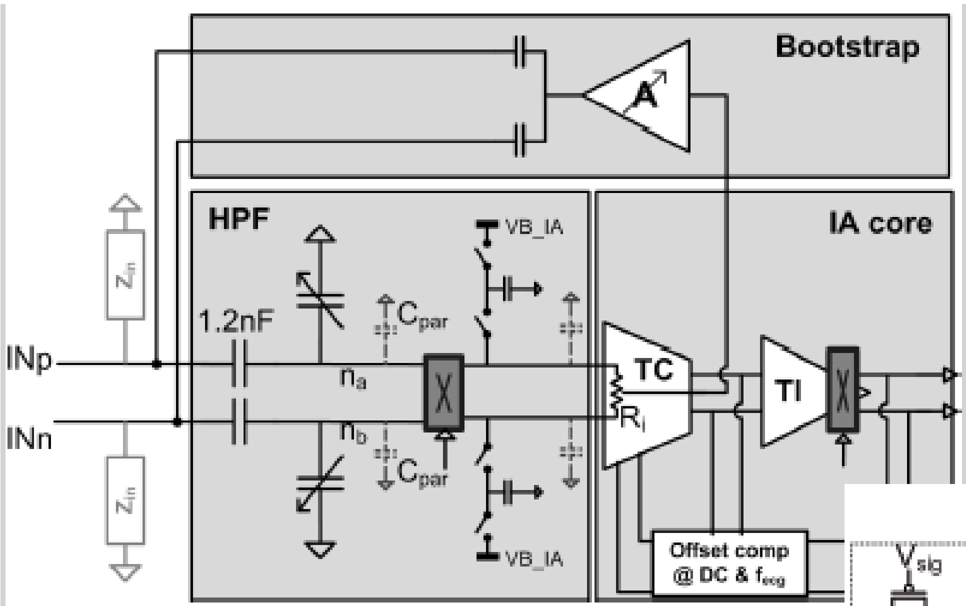


22nm Tri-Gate FET



6.5 160uA Biopotential Acquisition ASIC

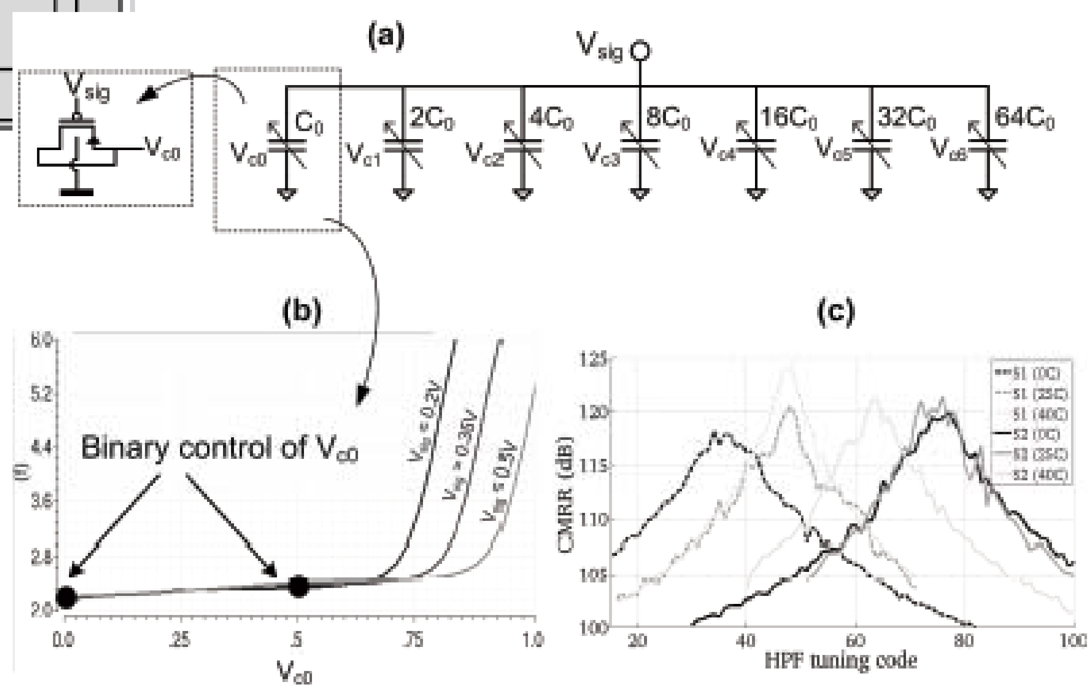
Nick Helleputte IMEC



Integrated 1.2nF AC coupling caps with digital cap trim for 120dB CMRR

4.5GΩ switched cap resistor for HPF

Positive feedback "bootstrap" loop used to compensate for parasitic impedances, increases input to >1GΩ

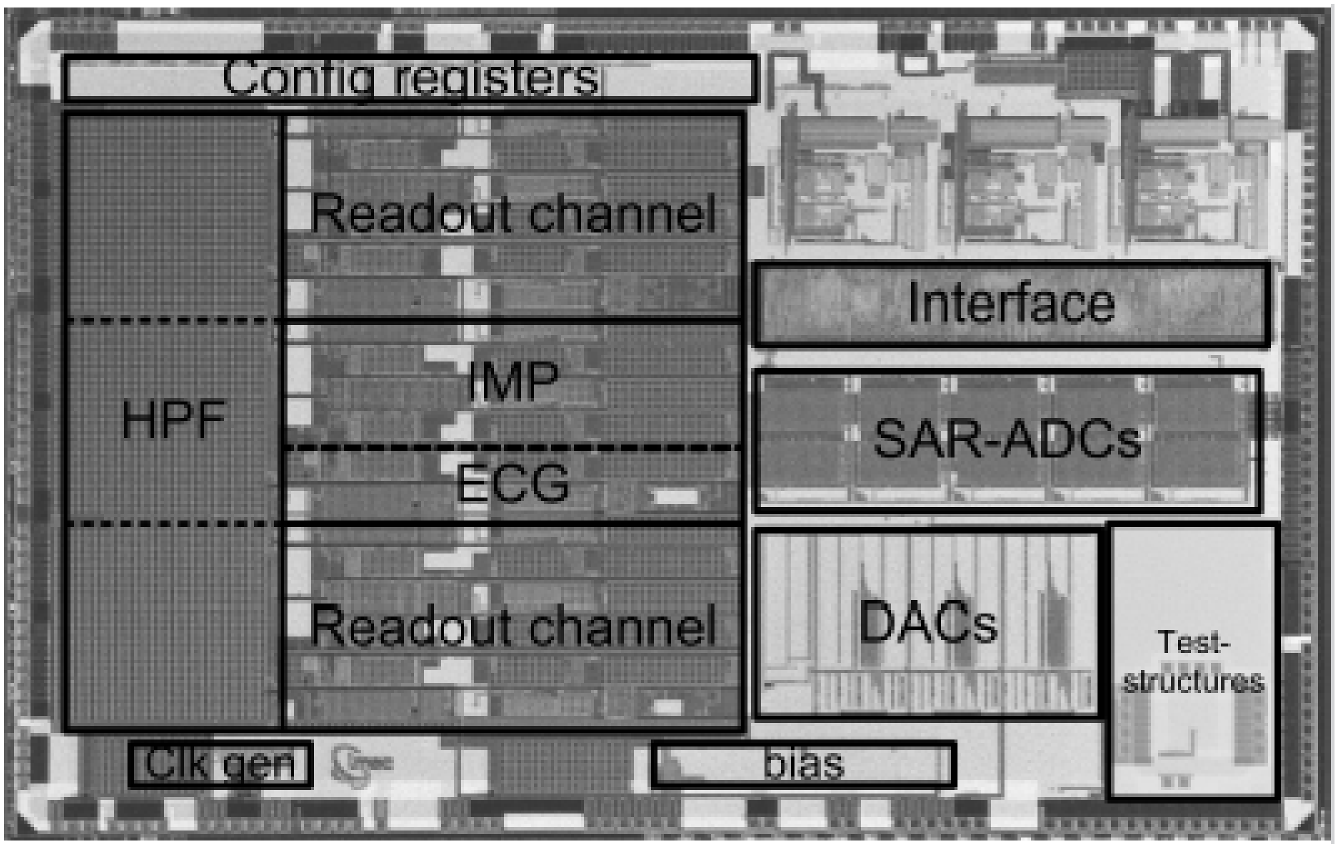


Sub-VTH bias control on FET caps allow 0.2fF trim step size

Similar idea used in some modern DXO designs

6.5 Continued

- Total of 6 1.2nF HPF caps consume 5.1mm^2
- 0.18μ process with 2fF/μm^2 MIM caps



Evening Sessions

- Paper presentations from 8:30am – 5:30pm
- Evening sessions run 8pm-10:30pm
- Very long days, but evening sessions not to be missed!
- “Technologies that could change the World”
- “Little Known Features of Well Known Creatures”
- Unfortunately no slides published from these sessions

Presenters in ES3
Technologies that could change the World

- Aaron Partridge – MEMs oscillators
- Kofi Makinwa – Thermal Diffusivity Sensors
- Michael Perrot – VCO based Quantizers
- Yannis Tsividis – Continuous Time DSPs
- Georges Gielen – Analog Synthesis

Aaron Partridge of SiTime Silicon Oscillators

- Compelling case made for replacing majority of XTALs
- Short lead time for any frequency at 1ppm accuracy
- 10X better failure rate an XTALs
- Vibration spur 25dB lower than XTAL
- EMI Interference 3-40X lower than XTAL
- Lower COGs than complete XTAL oscillator solutions
- Phase noise <0.7pS
- 0.5ppm accuracy over -40C to 90C
- Units shipped doubled every year for 5 yrs, 50M in 2011
- ~10B total XTAL unit market

SiTime Discussion Continued

- Surprisingly complex PLL and temperature correction circuitry needed
- LOTS of work for a “4-pin part that produces a square wave”
- “Engineers make small contributions that are multiplied countless times”
- One recurring theme from this ISSCC… extraordinary complexity when applied to the right applications can open new market opportunities

Kofi Makinwa
Thermal Diffusivity Temperature Sensors

- BJT Temp sensor +/-0.15C accuracy with 1 trim
  - Doesn't scale well at low voltages
  - Sensitive to doping variation and package stress
- Heat diffusion is a mechanical process
  - Phonons rather than electrons
- Exploit strengths of CMOS
  - Lithography space control is excellent, Si Diffusivity well defined, timing accuracy is good
- Accuracy of Diff. Sensor scales with process
  - In 0.18u get 0.2°C accuracy without trim!
  - Should compete with BJT sensor at 45 or 32nm node
- Paper 11.5 extends prior work by getting rid of accurate frequency reference-- compares diffusivity of Si to SiO_2

Michael Perrot - VCO Quantization

- Mismatch and offset insensitive compared to conventional quantizers
- Noise shaping of mismatch errors due to barrel shift in ring oscillator output phases
- Scales well with process
- Non-linear voltage to frequency conversion is biggest hurdle
- Many techniques have been used to improve this limitation

Yannis Tsividis - Continuous Time DSP

- Uniform sampling is overkill in some applications
- Level crossing sampling can be more efficient
- No quantization noise floor, only harmonics
- No aliasing (no Nyquist frequency)
- Dynamic power scales with signal activity
- Output reacts immediately to signal (no sample delay)
- [reference paper at conf.]

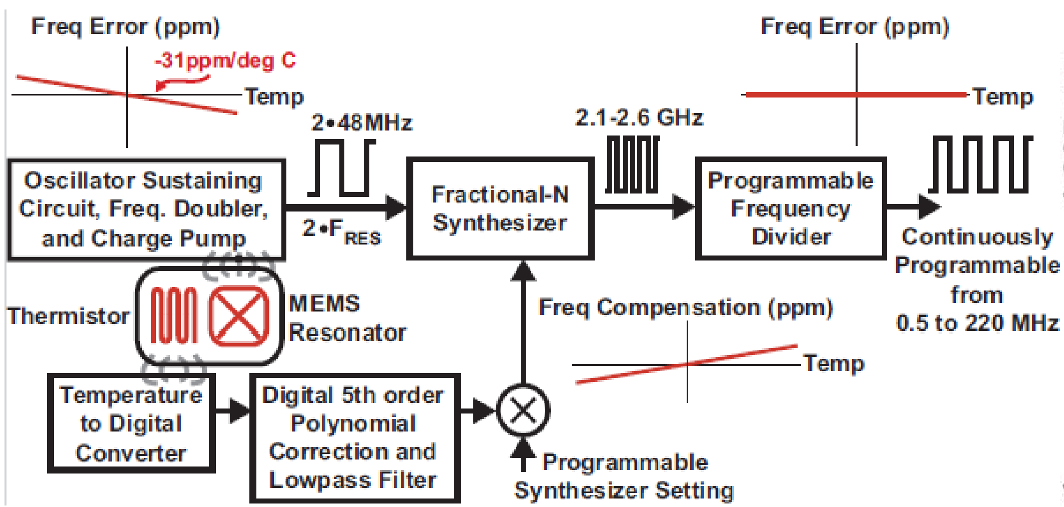
11.6 Temperature-to-Digital Converter for MEMS Oscillator with 0.5ppm stability

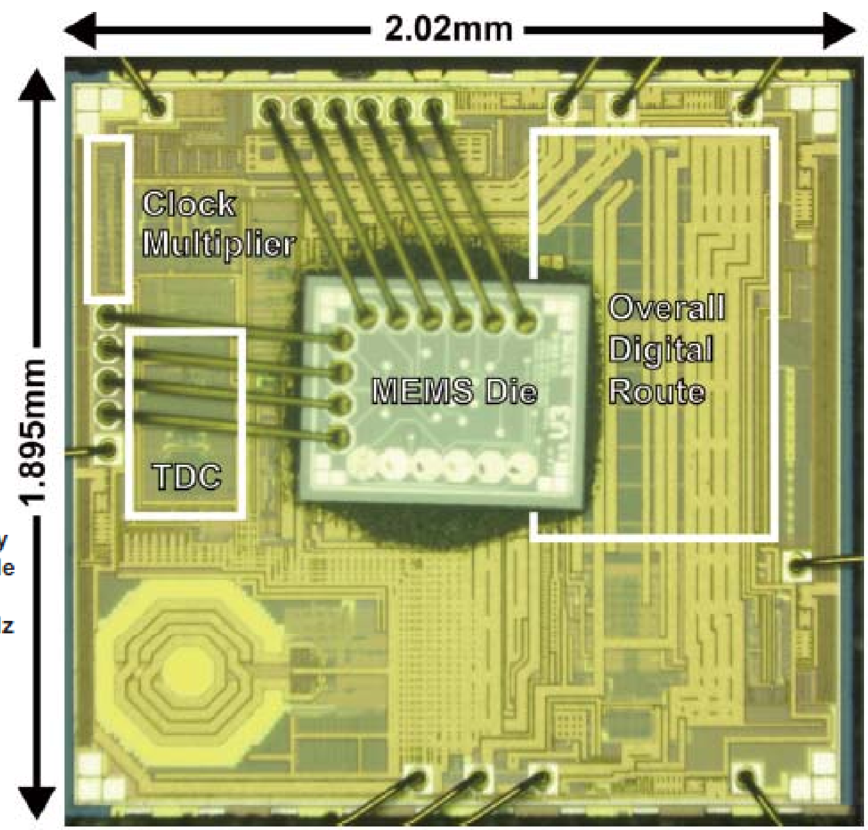
M. Perrot   Masdar UAE, SiTime

- Without compensation MEMs osc error is -31ppm/°C
- Current state-of-art compensated MEMs osc has 10ppm stability from -40C to 85C
- This work improves this to 0.5ppm (20X)
- Thermistor based detector is ~10X more sensitive than a diode based detector (1.6mV/°C)
- Noise lower than 0.00016Kelvin in 5Hz BW (also 20X improvement from best known)

11.6 Cont. MEMs oscillator circuit

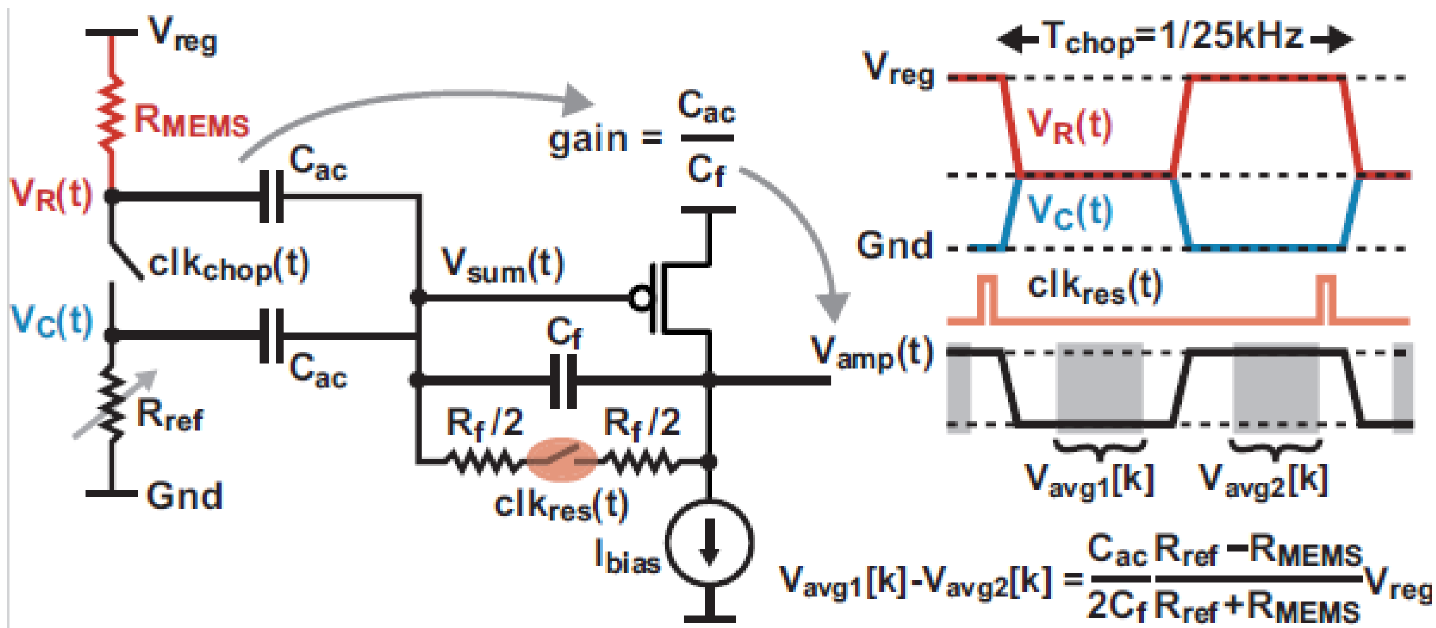
- 5th order polynominal correction with 5-10 temperature trims





11.6 Cont. TDC Front End

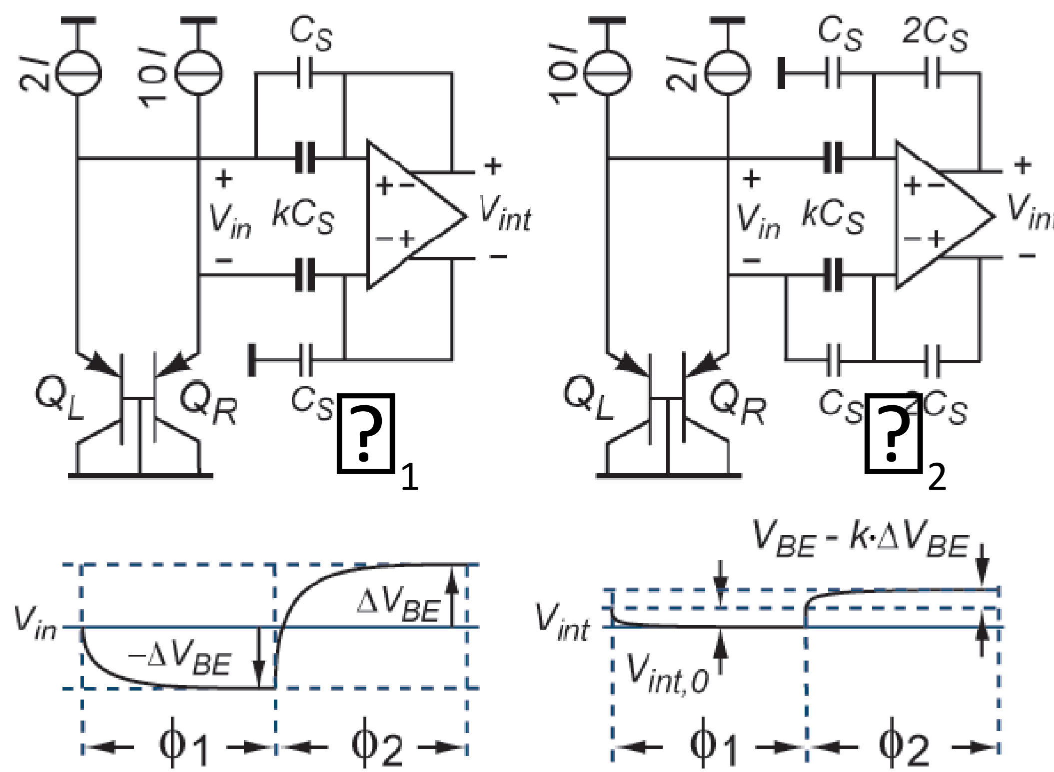
- FB loop adjusts R_{ref} to match R_{MEMS} thermistor
- Uses interesting chopping and correlated double sampling method to reject amp 1/f noise and offset
- Uses switched biasing to disconnect Rf devices during measurement to remove their noise
- R_{ref} implemented with switched capacitor



11.7 Temperature Sensor with Voltage Calibrated Inaccuracy of +/-0.15C

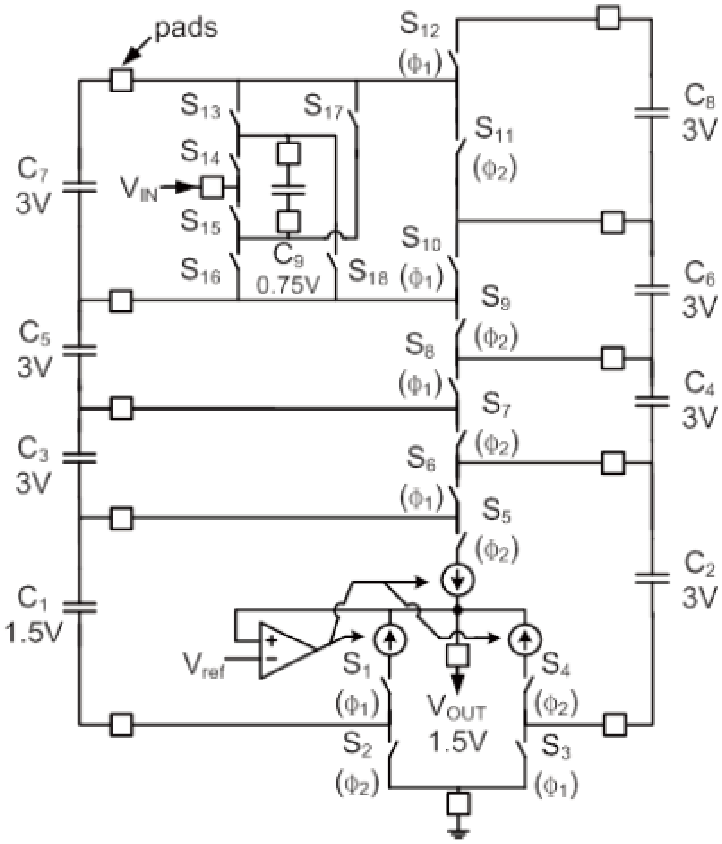
K. Souri Delft

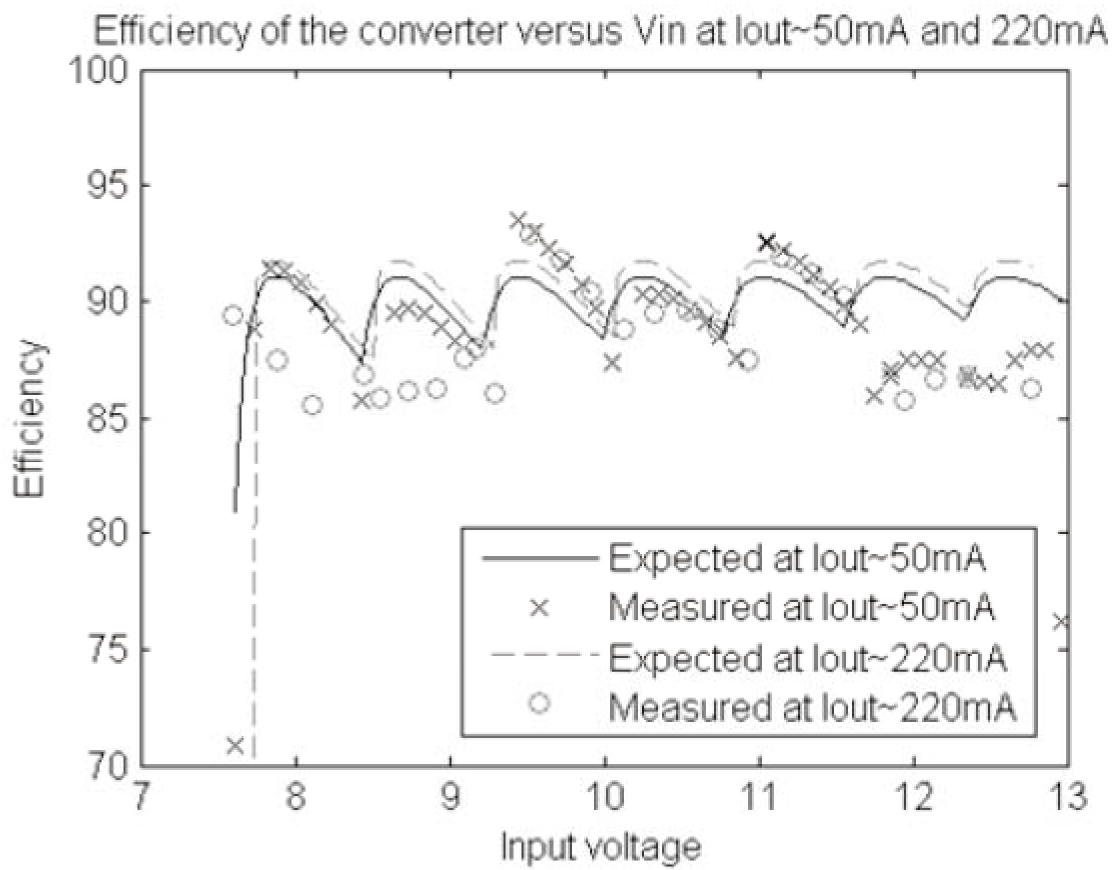
- Difficult to get better than 0.3C accuracy w/o multiple temperature trims which are slow and expensive
- Voltage calibration is MUCH faster and cheaper
- VBE and ΔVBE sampled simultaneously
- 2 step conversion
  - Fast SAR
  - Fine SigmaDelta



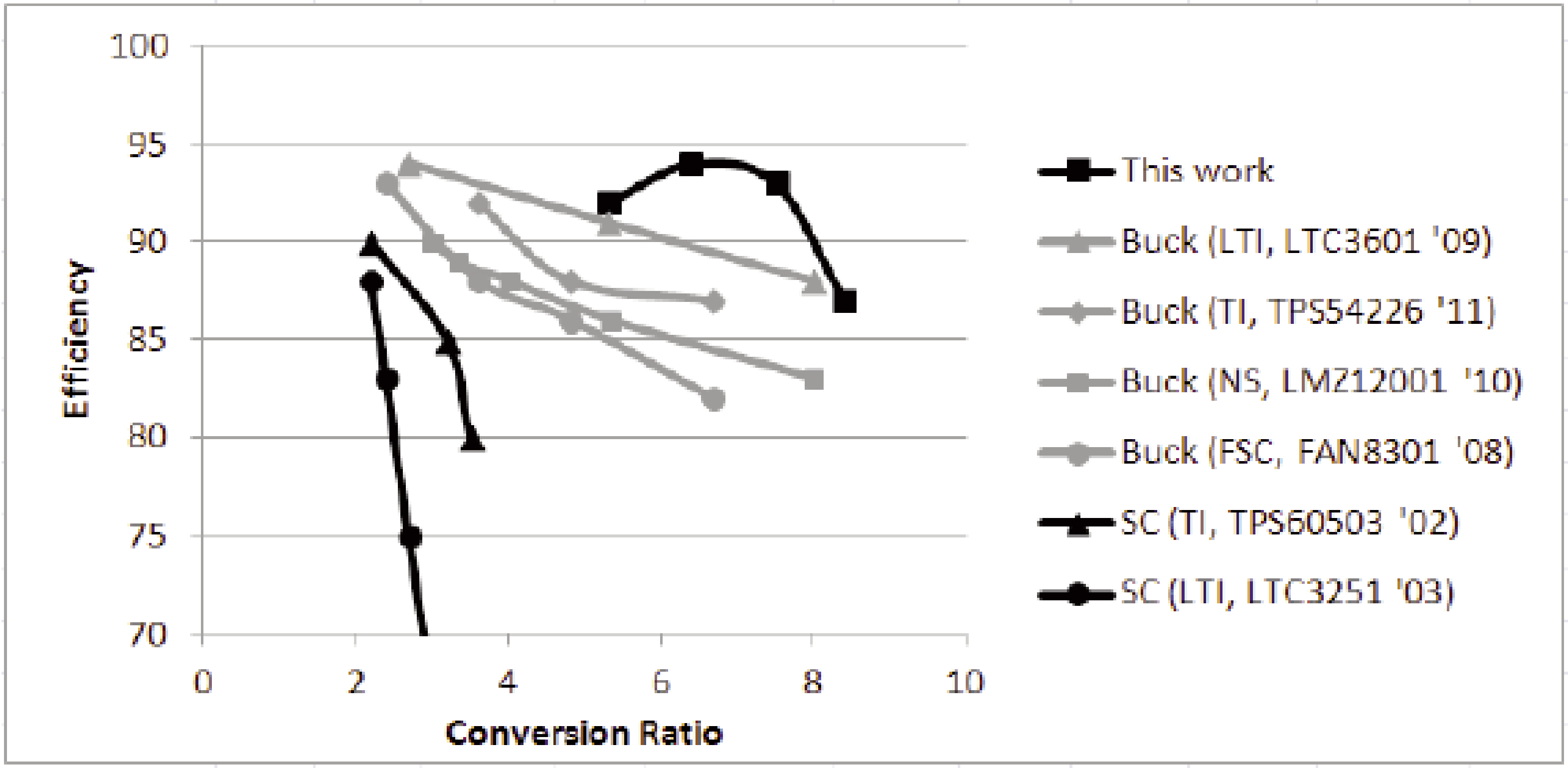
16.5 92% Efficiency Wide Input Range Switched C Converter Vincent Ng Berkley

- Great efficiency over wide voltage range
- Won’t work as well at lower input voltages





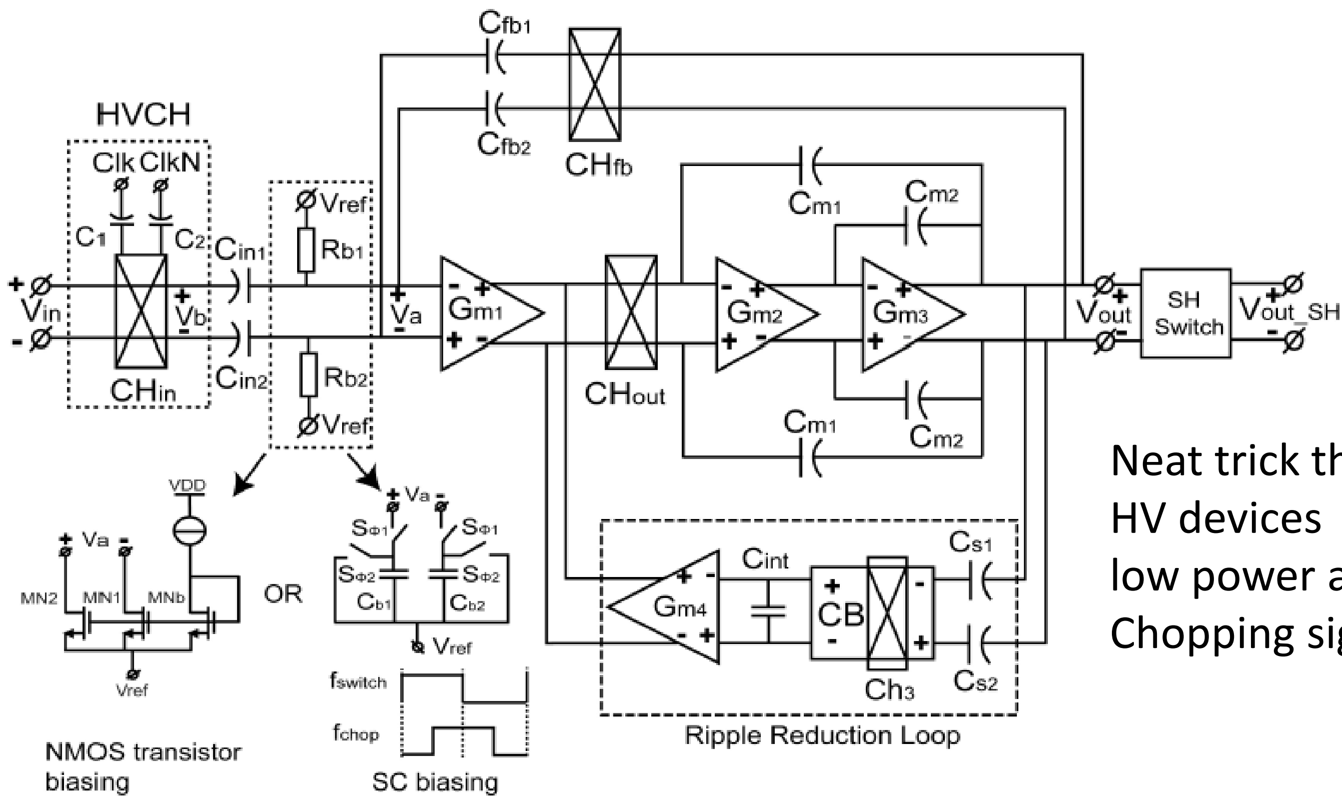
16.5 Continued



	V_{IN}	V_{OUT}	$I_{OUT,pk}$	Eff_{pk}	>80% eff	$tran_{pp}$	C_{IN}	C_{OUT}	Others	PCB	Cost
This work	11V	1.5V	1A	92%	5mA-1A	30mV	12μF	110μF	10μFx8	20mm²	$1
SC TI '02	5V	1.5V	0.25A	85%	2-200mA	50mV	2.2μF	10μF	1μFx2	3.6mm²	$0.10
SC LTI '03	5V	1.5V	0.5A	60%	-	50mV	1μF	10μF	1μFx2	2.7 mm²	$0.10
buck NS '10	12V	1.5V	1A	83%	0.35A-1A	40mV	10μF	100μF	10μH	57 mm²	$1
buck LTI '09	12V	1.8V	1.5A	88%	20mA-	100mV	22μF	22μF	2.2μH	27 mm²	$1.20
buck FSC '08	12V	1.8V	2A	82%	0.4A-1.3A	500mV	10μF	22μF	15μH	57 mm²	$1.70
buck TI '11	12V	1.8V	2A	87%	40mA-2A	30mV	20μF	44μF	2.2μH	30 mm²	$1.50

21.9 Cap Coupled Chopper Amp with +/-30V Common-Mode Range & 160dB CMRR
Q. Fan Delft

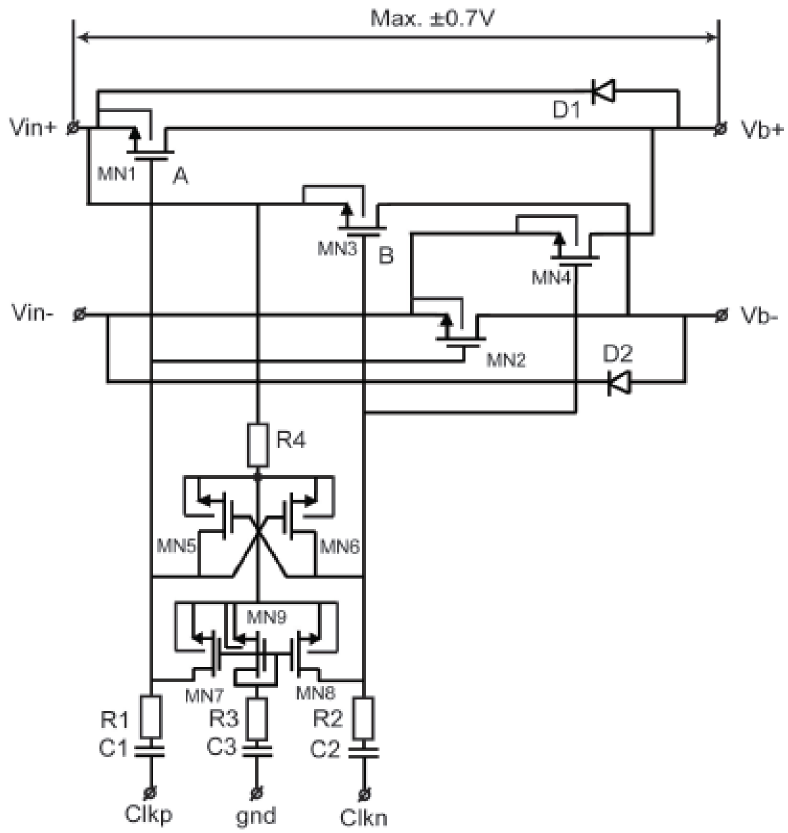
- Cap coupling at input allows huge CM range
- High-side current sense amp measures DC current, so chopping used on HV side

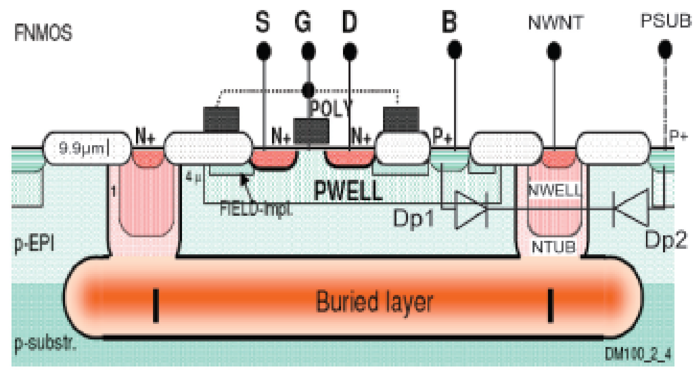


Neat trick that HV choppers use NO HV devices or HV supply current for low power and area
Chopping signals are cap coupled too

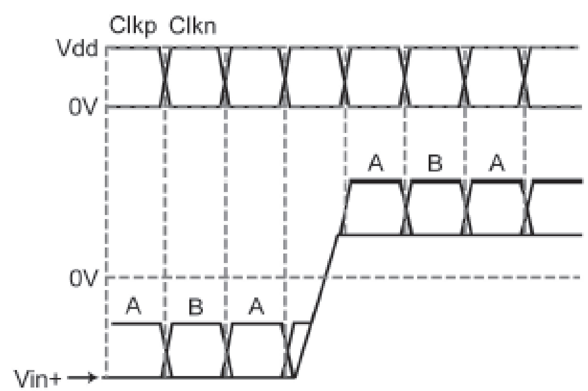
21.9 Continued

- High CM voltage choppers using LV devices
- Cross coupled latch sets chopper common mode





(b)



27.1 14b 3/6GHz Current-Steering DAC in 0.18μ G. Engel Analog Devices

- Quad current-steering switches ensure matched glitches (reducing code-dependent switching activity) without throwing away signal current like RTZ
- NFET current sources on neg supply to avoid level shifting steering logic
- Interesting options for upsampling or mixing the DAC output
- Includes 2 1.5GHz 14b LVDS ports

Power	600mW	@5GHz
LTE signal ACLR	66dBc	@2.9GHz Fout
DOCSIS ACLR 150carriers	~52dBc	(upper 2nd channel)
SFDR	>60dBc	<500MHz
	>52dBc	To Nyquist
IMD	>70dBc	<500MHz
	>65dBc	To Nyquist
Full Scale Current	20mA	33mA MAX
DAC Core Area	2mm x 2mm	
Die Area	5mm x 5.7mm	

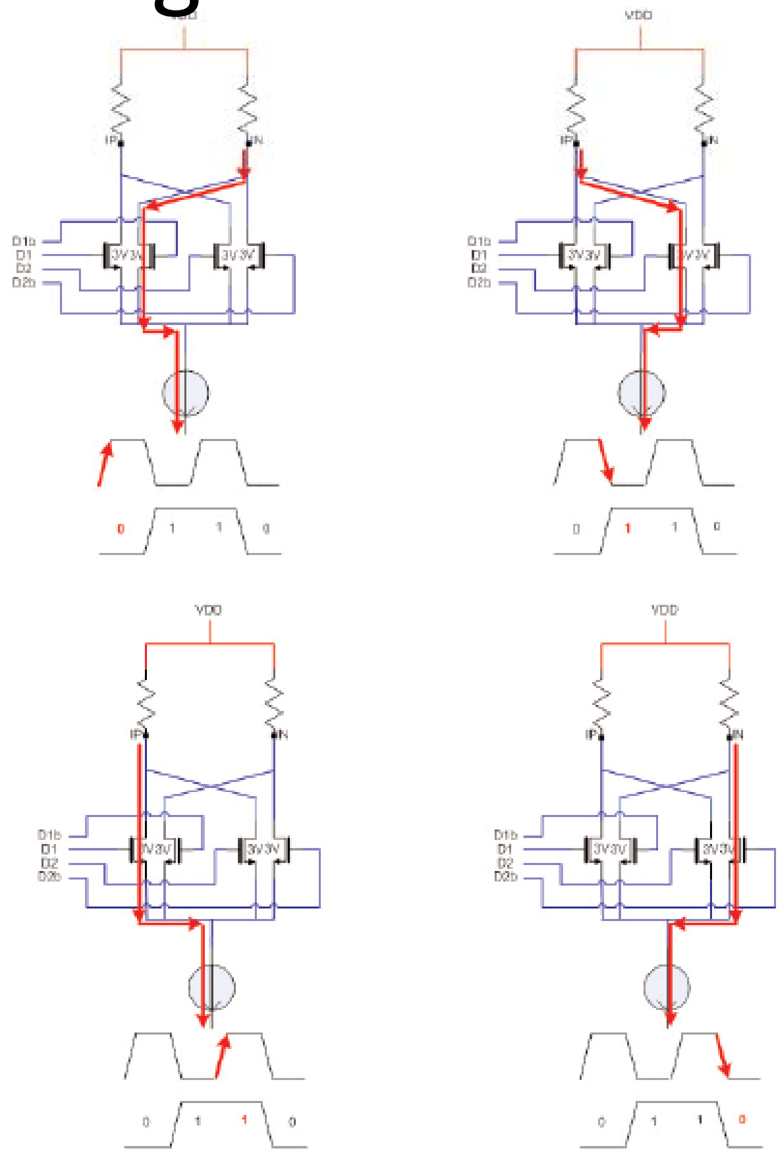
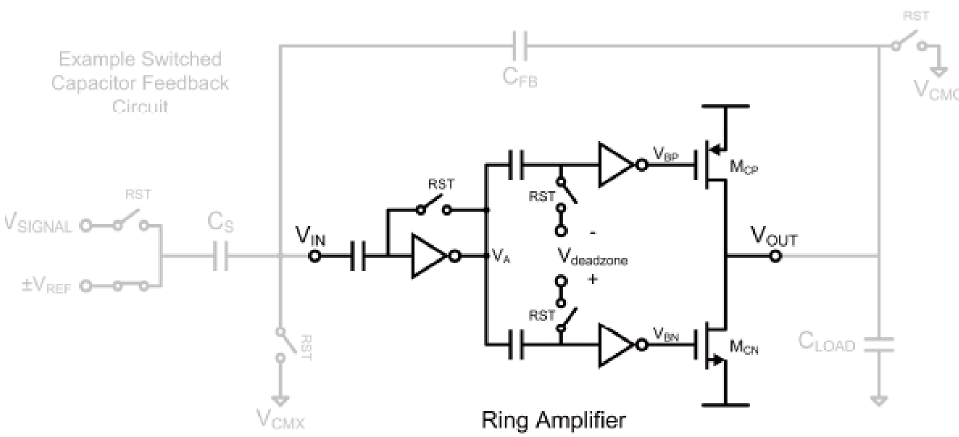


Figure 27.1.2: Double Data Rate (DDR) quad-switch function.

27.2 Ring Amplifiers for Switched-Capacitor Circuits B. Hershberg Oregon State

- Part of Dr. Moon's group-- evolution of the zero-crossing-based switched cap designs in last few ISSCCs
- Like a 3 inverter ring oscillator with a dead zone



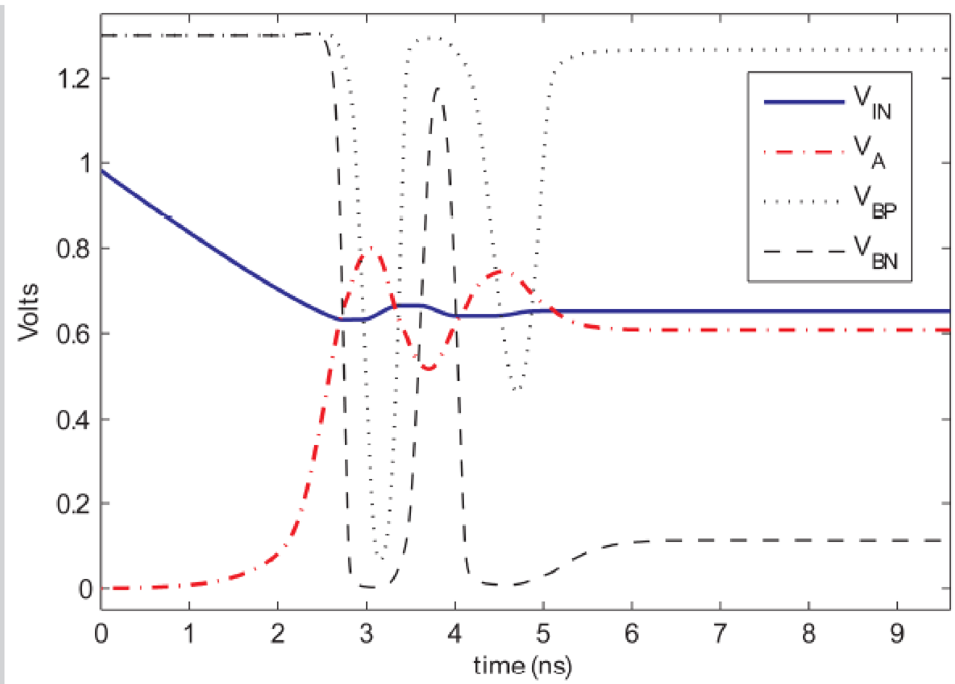
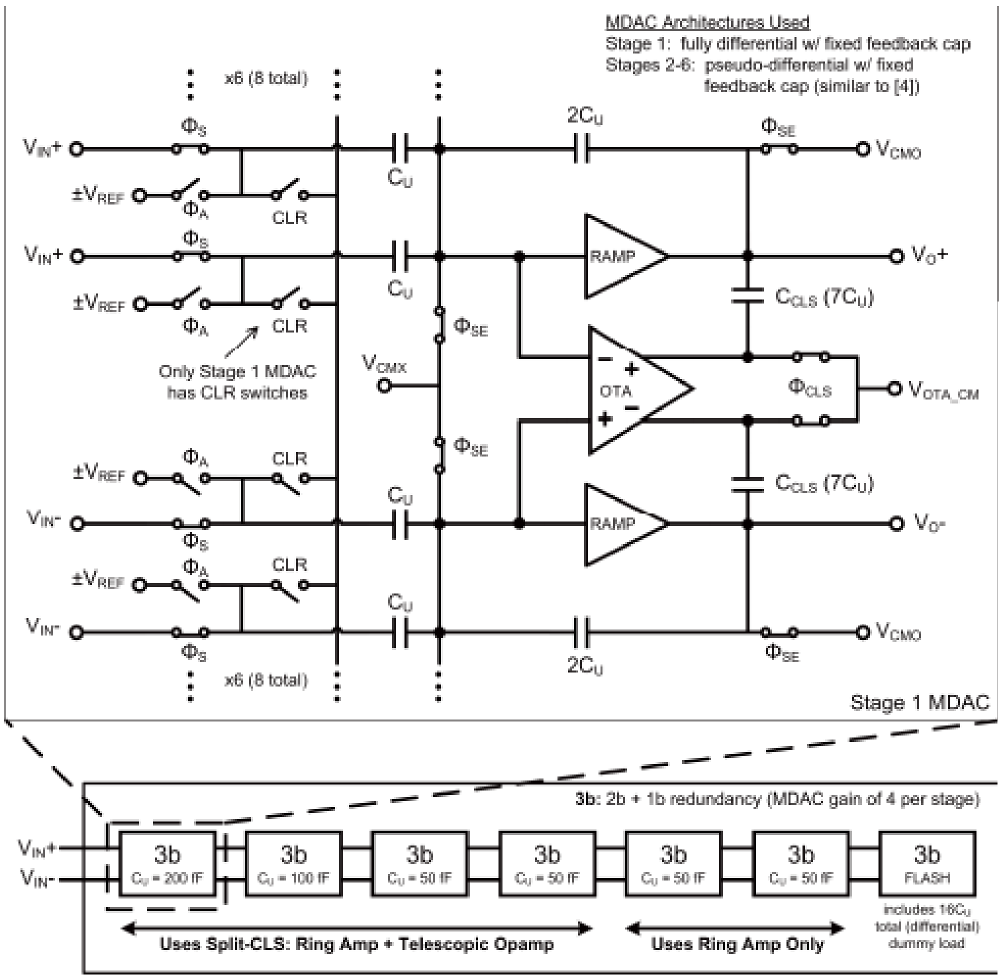


Figure 27.2.2: Settling behavior of Fig. 1 for a typical dead-zone size and charging

27.2 Continued

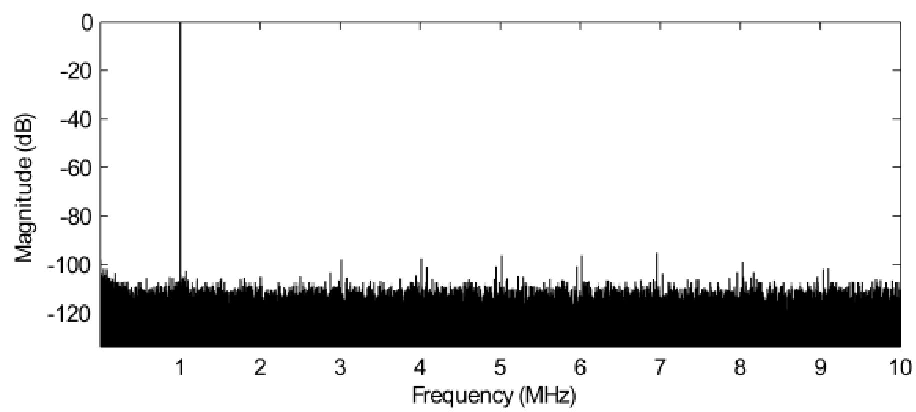
- Pipeline ADC with very good FOM built with Ring Amps as coarse charging device in first phase of split correlated level shifting amp scheme from Moon's group in 2010



27.2.3: Split-CLS pipeline ADC structure and first stage MDAC.

Performance Summary

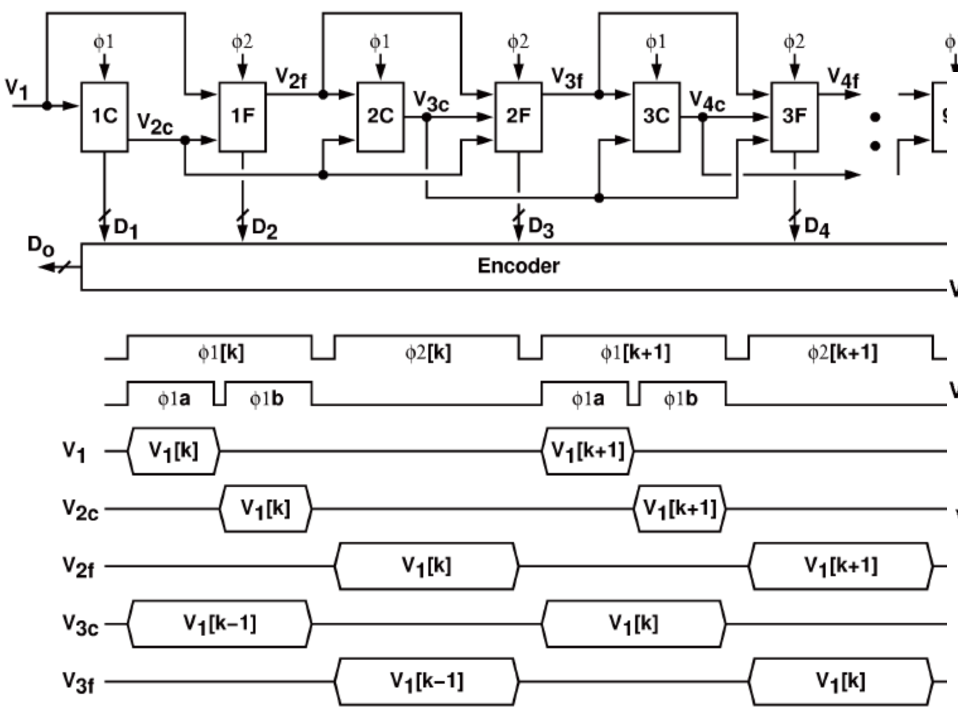
Resolution	15 bits	Input Range	2.5 V pk-pk diff.
Analog Supply	1.3 V	SNDR	76.8 dB
Sampling rate	20 Msps	SNR	77.2 dB
ERBW	10 MHz	SFDR	95.4 dB
Technology	0.18µm 1P4M CMOS	ENOB	12.5 bits
Active Area	1.98mm^2 (3.05mm x 0.65mm)	Total Power	5.1 mW
		FoM	45 fJ/c-step

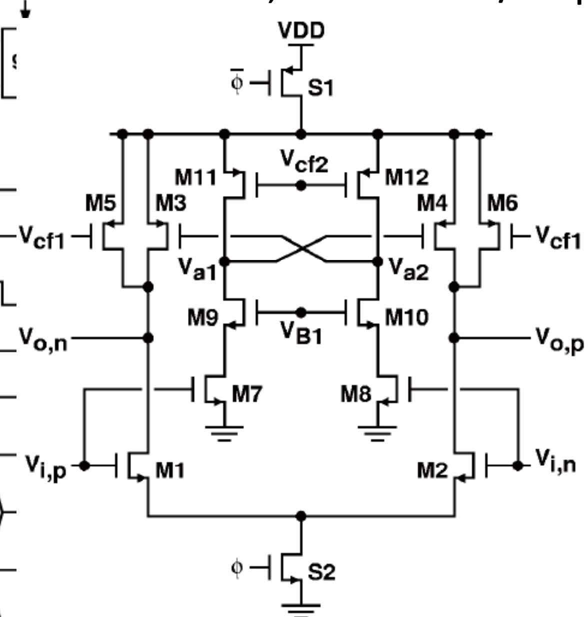


27.3 Dual-Path Pipelined ADC
Y. Chai National Chiao Tung U

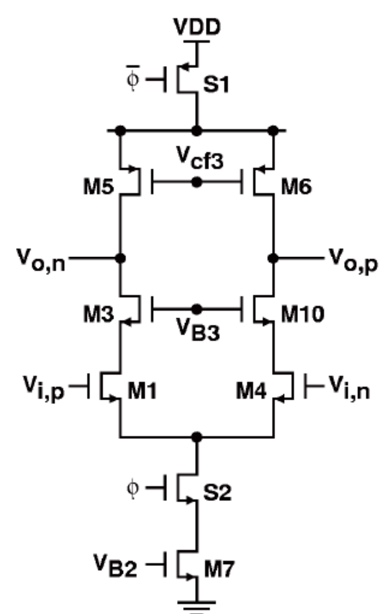
- Coarse amp has large swing output with low gain & speed
- Second fine amp stage settles accurately w/ small swing
- Amps are optimized separately for low power
- Effective DC gain is product of two stages

Fs=200MHz, SNDR=57dB, 5.37mW,
65nm, FOM=48fJ/step





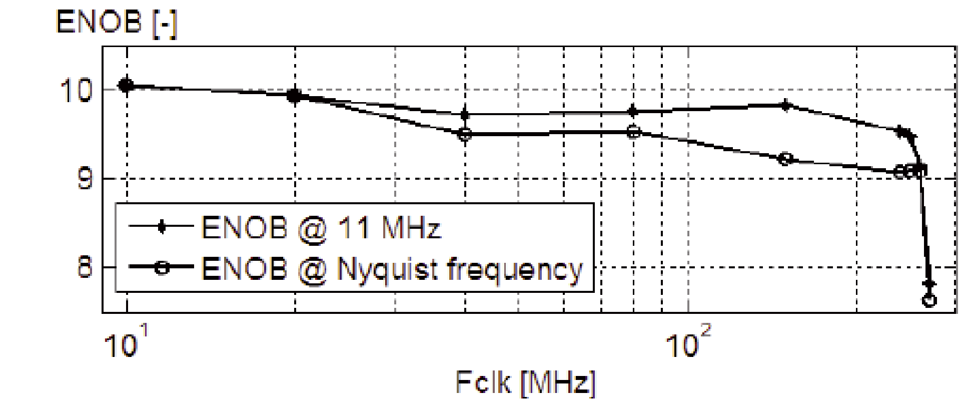
Coarse–Stage Opamp

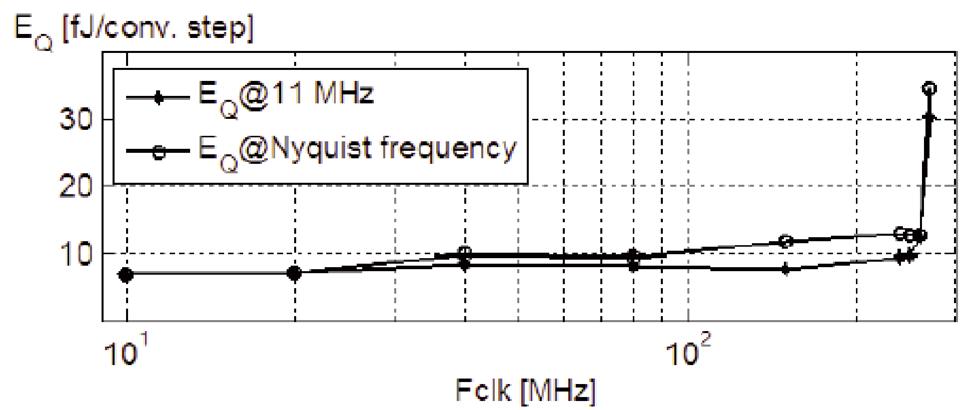


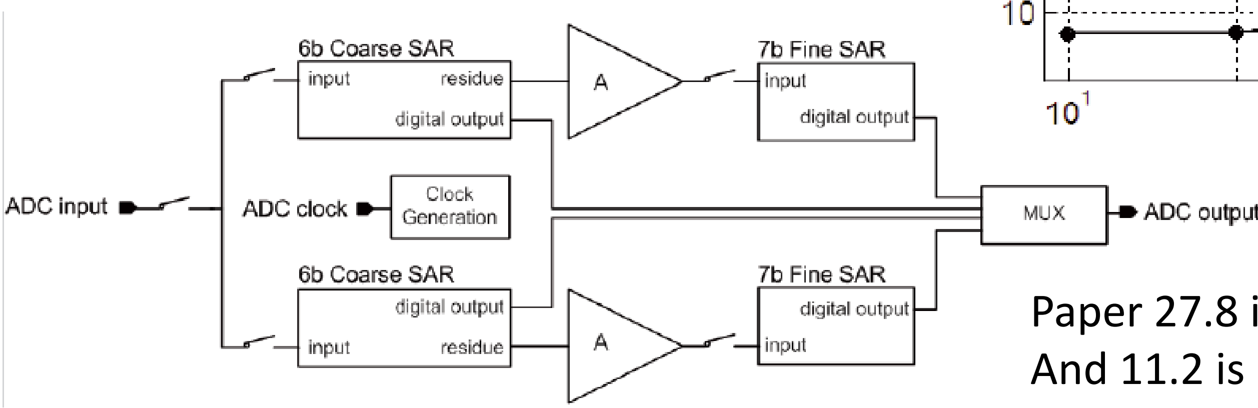
Fine–Stage Opamp

27.5 1.7mW 11b 250MSPS Fully Dynamic Pipelined SAR ADC in 40nm
B. Verbruggen IMEC

- 6bit coarse SAR and 7bit fine SAR
- With only dynamic power, energy per conv. step FOM is flat across large sample rate range



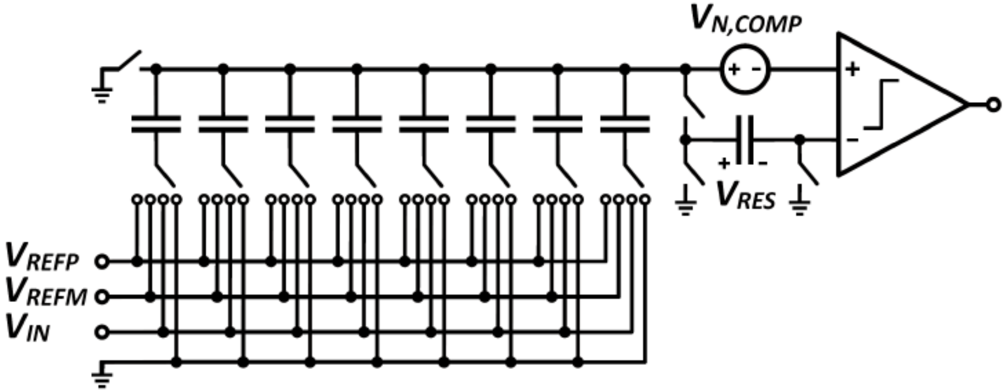


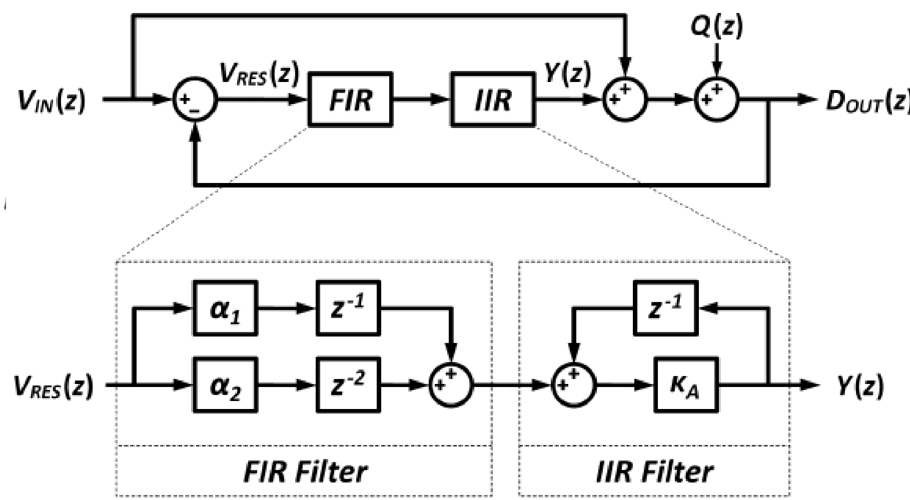


Paper 27.8 is another 2-step SAR
And 11.2 is a multi-step sigmadelta

27.6 90MSPS 11MHz BW Noise Shaped SAR ADC J. Fredenburg U. Michigan

- Add one extra cycle to SAR and leave residue on sample cap to include with next sample
- Add additional loop filter to increase noise shaping





$$D_{OUT}(z) = -V_{IN}(z) + \frac{1}{1+z^{-1}}\left[Q(z) + V_{N,COMP}(z)\right]$$

$$D_{OUT}(z) = V_{IN}(z) + \frac{1-\kappa_A z^{-1}}{1+\kappa_A(\alpha_1-1)z^{-1} + \kappa_A\alpha_2 z^{-2}}\,Q(z)$$

27.6 Continued

- Interesting concept, performance is good, but not stellar
- SNDR performance not really better than ideal 8b ADC with 4X OSR & no shaping
- Uses asynchronous timing
- DAC is 8b, OSR = 4
- FOM=35.8fJ/conv
- 65nm

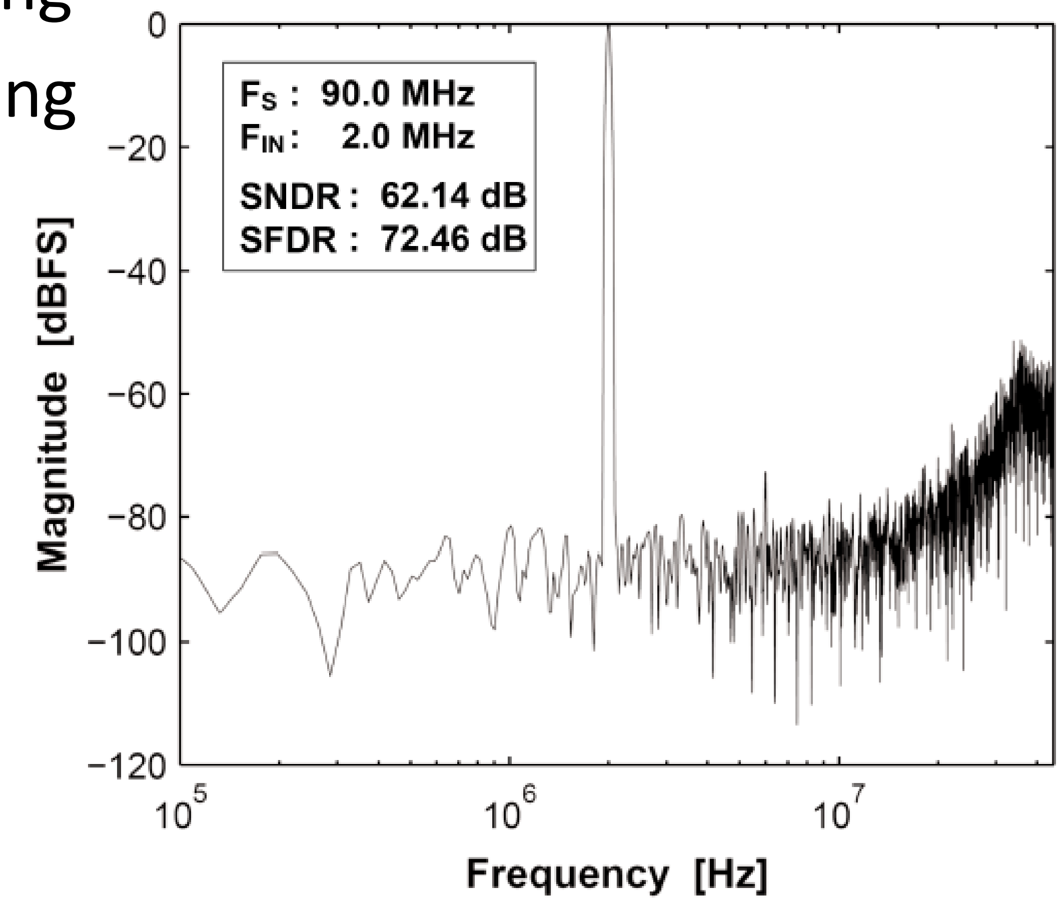


Figure 27.6.5: Output spectrum from a 4096-point FFT.

27.7 Current-integrating SAR ADC
B. Kalki IMEC

- Similar technique as is used in some LNA and discrete time mixer front ends
- Variable gain Gm_{in} and sample charge instead of voltage
- Uses non-linear FET caps since dealing with Q not V
- Passive amplification of ~4x by changing bias of FET caps

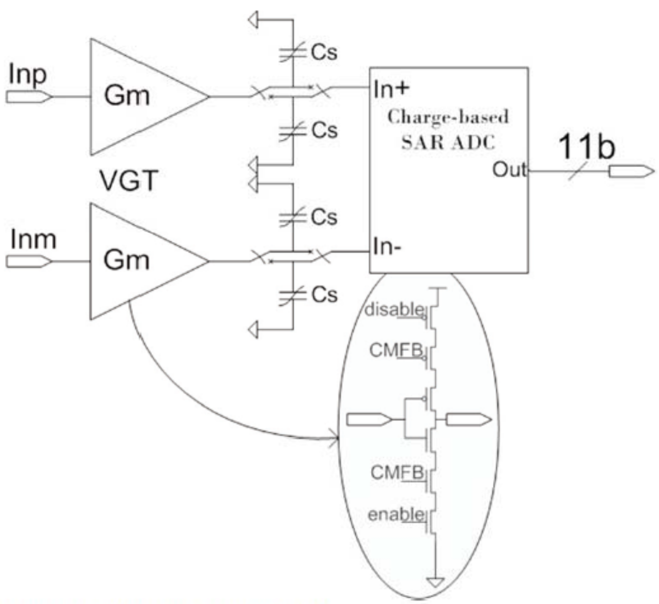
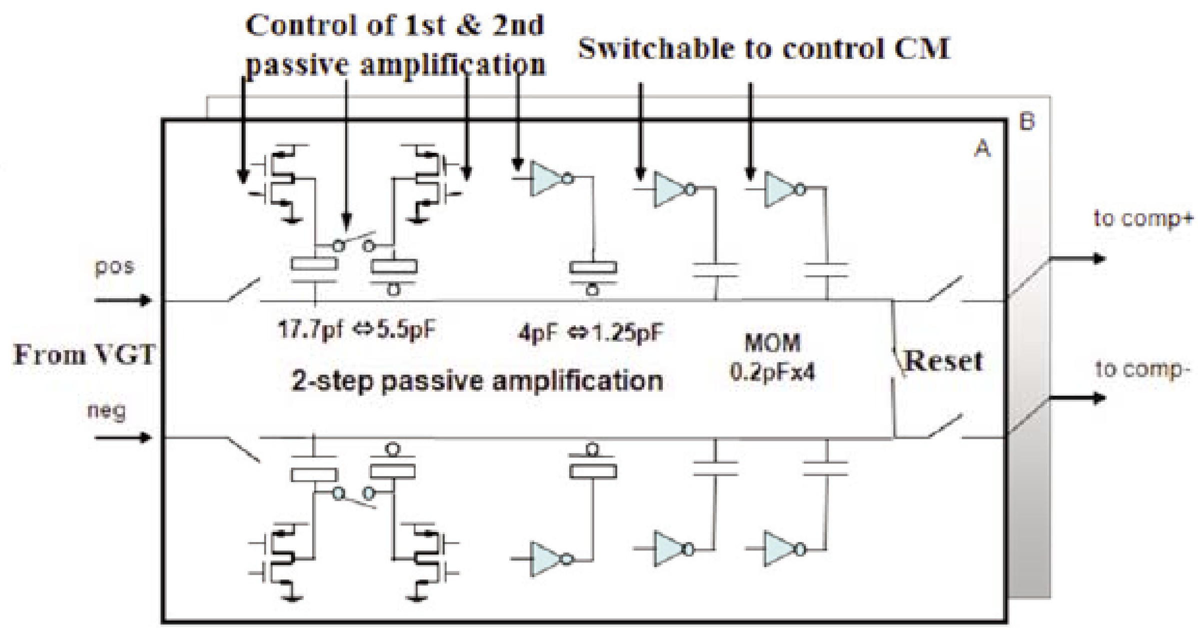
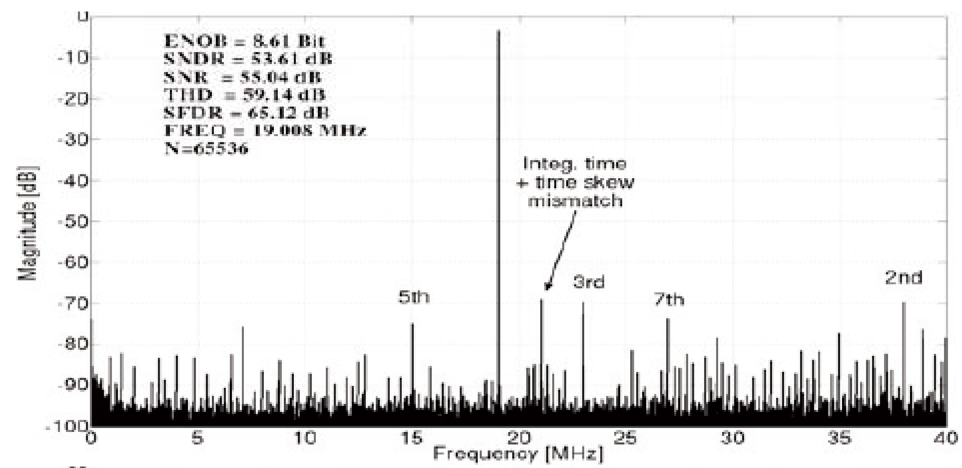


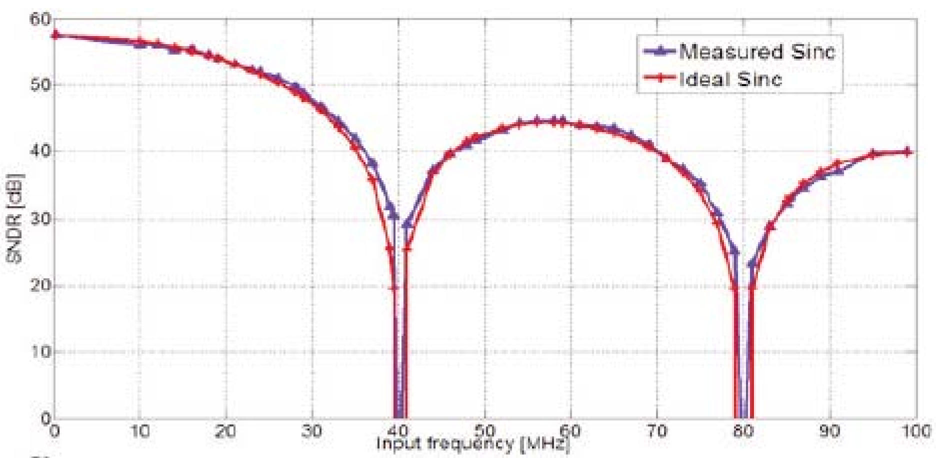
Figure 27.7.1: Architecture of the VGA/ADC.

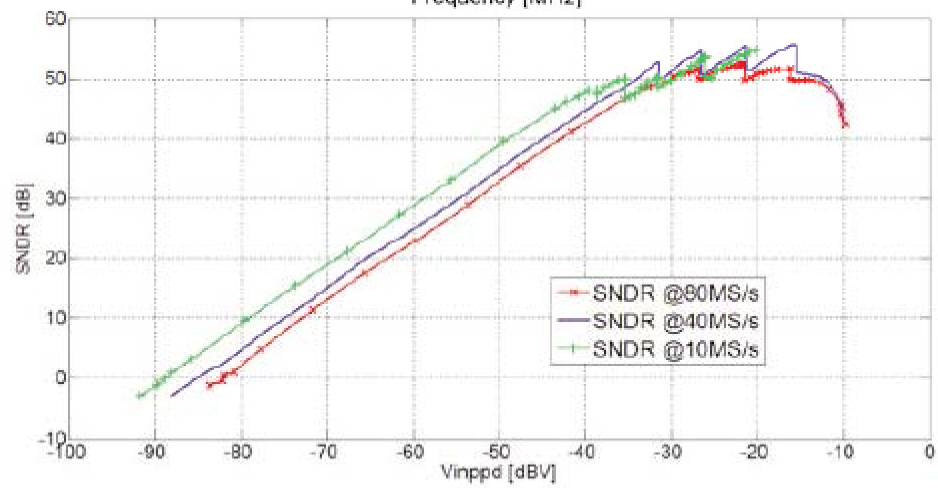


27.7 Continued

- Free input sync filter with input GmC integration







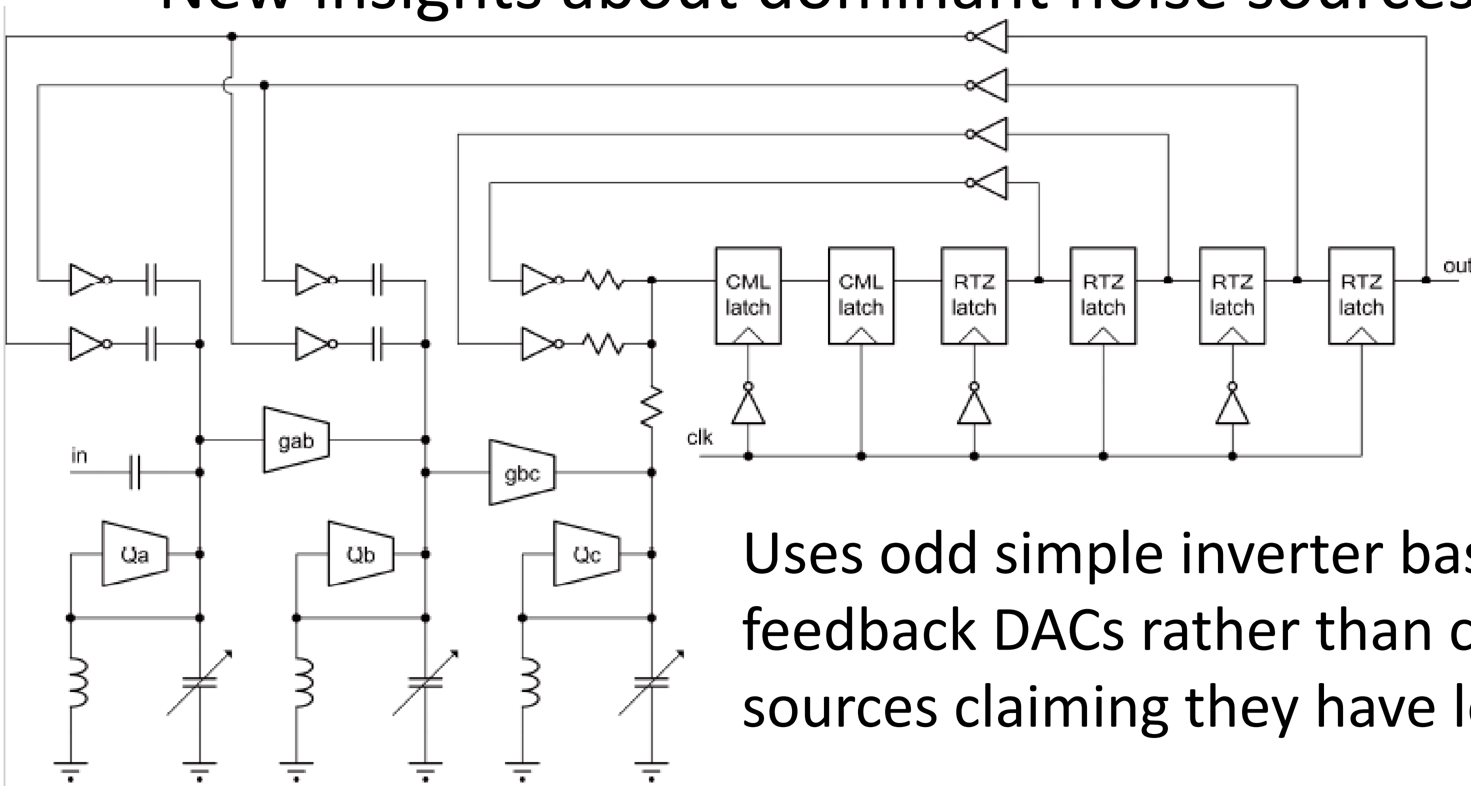
ISSCC Themes / Trends

- Quantization in time used extensively because it scales well in advanced processes
- Ring Oscillators used for everything (scale nicely)
- Not one DT Sigma-Delta presented, indicating perhaps that this has matured and is less favorable in advanced processes
- However, resolution is limited in CT ADCs, nothing above 14 bit resolution this year
- Two-stage (coarse/fine) conversions used for better power vs performance
- Noise shaping everywhere… it's not just for SigmaDelta ADCs anymore
- Extensive complexity opening new market opportunities (0.0001°C accurate temp sensor)

CT ADC Stuff (time allowing)

8.1 LC Bandpass ΔΣ with 70dB SNDR over 20MHz BW J. Harrison Broadcom

- Bandpass ΔΣ ADCs have historically shown ~10X lower FOM than lowpass ADCs
- This paper and next achieve very nice FOMs
- New insights about dominant noise sources

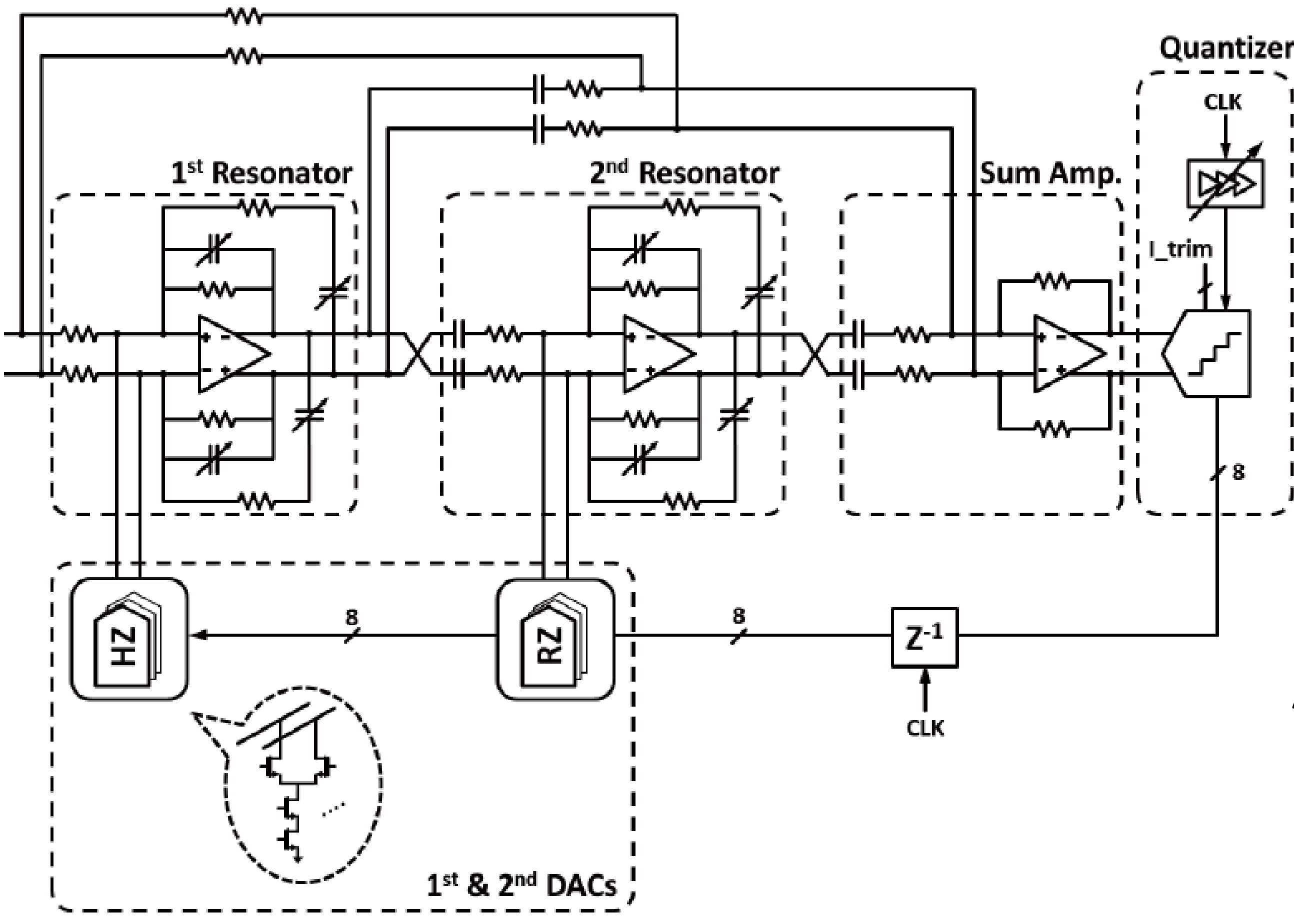


40nm
0.4mm^2
P=20mW
FOM=
0.19pJ/step

Uses odd simple inverter based feedback DACs rather than current sources claiming they have lower noise?

8.2 12mW CT BP ΔΣ with 58dB SNDR and 24MHz BW H. Chae U. Michigan

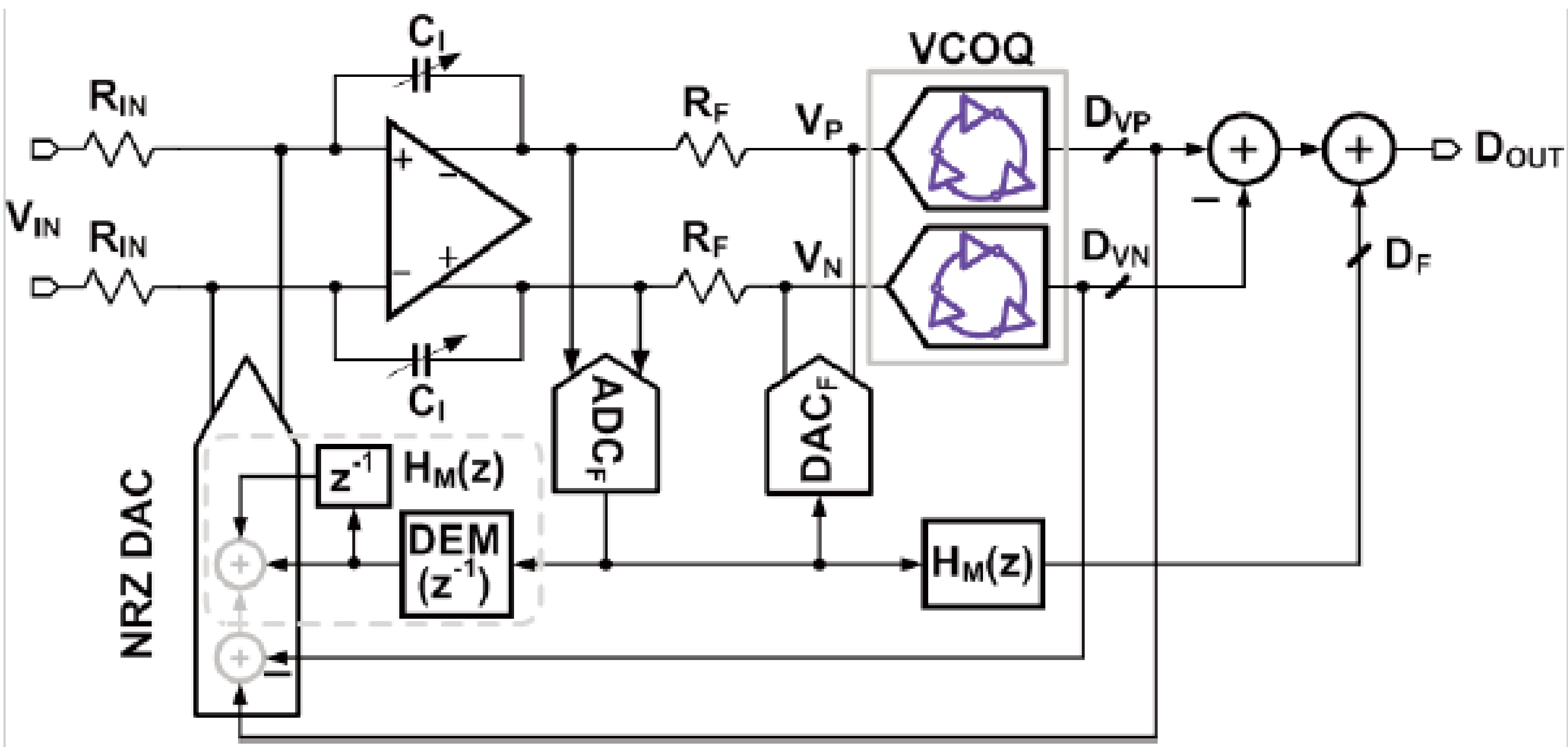
- High Q resonators with single amp
- Half power of Biquad resonators with same noise



65nm
Area=0.2mm^2
P=12mW
FOM= 0.385pJ/step

8.4 16mW 78dB SNDR 10MHz BW CT ΔΣ using Residue Cancelling VCO quantizer K. Reddy Oregon State

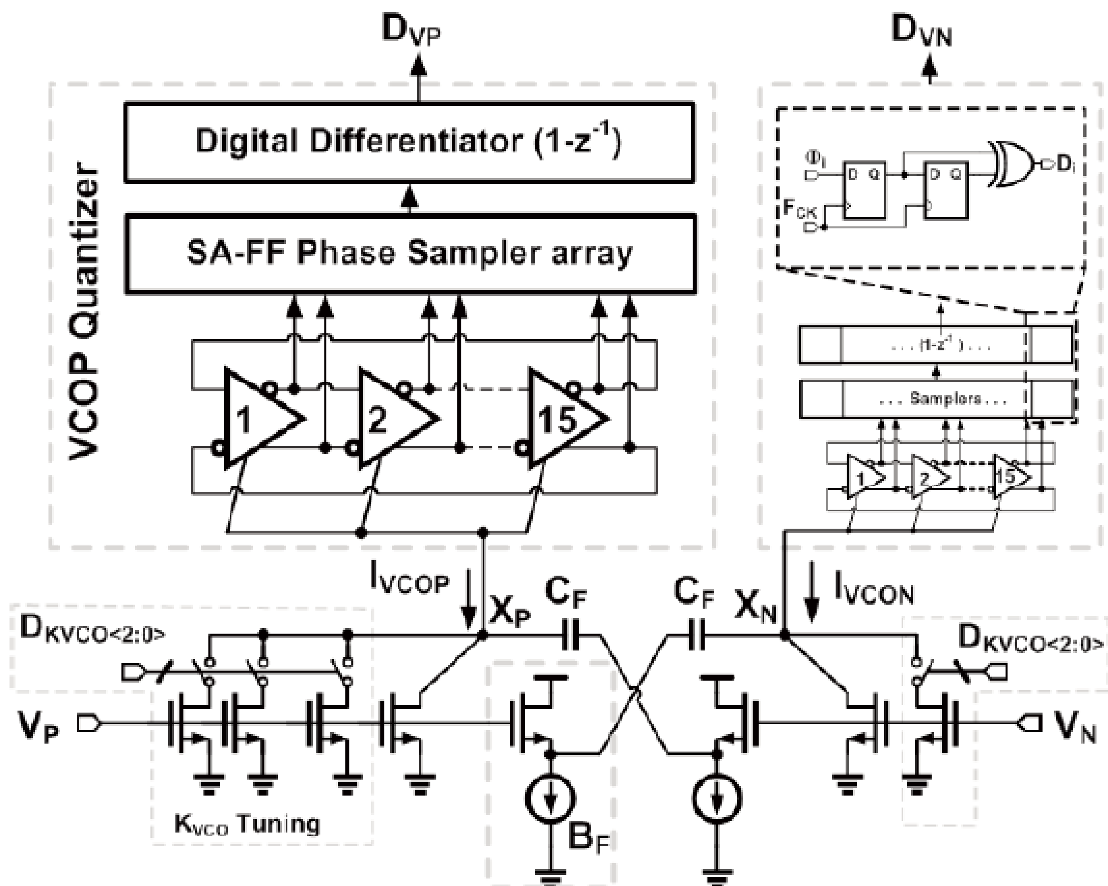
- VCO quantizer processes residue of the ADC_F flash ADC
- This improves VCO linearity from ~40dB to 78dB



8.4 Continued

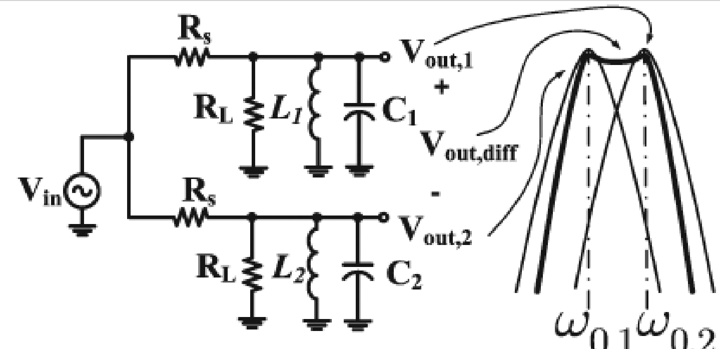
- VCO VtoF bandwidth normally limited by pole at Xp
- Bandwidth substantially extended using C_F and B_F feedforward branch to charge C_{VCO}
- D_{KVCO} control bits tune the VCO gain

90nm process
$0.36mm^2$



21.1 0.3-to-1.2GHz Tunable 4th-Order Switched g_mC Filter M. Darvishi U. Twente

- 4^{th} order filter created by subtracting 2 2^{nd} order filters
- Poly phase clocks used for center frequency shift



$$\frac{V_{out,i}}{V_{in}} = \frac{R_L}{R_L+R_s}\times\frac{\left(\frac{\omega_{0,i}}{Q_i}\right)\times s}{s^2+\frac{\omega_{0,i}}{Q_i}s+\omega_{0,i}^{2}}, i=1,2$$

$$\frac{V_{out,diff}}{V_{in}} = \frac{R_L}{R_L+R_s}\times\frac{\omega_{0,2}\omega_{0,1}\left(\frac{\omega_{0,2}}{Q_1}-\frac{\omega_{0,1}}{Q_2}\right)\times s}{\left(s^2+\frac{\omega_{0,1}}{Q_1}s+\omega_{0,1}^{2}\right)\left(s^2+\frac{\omega_{0,2}}{Q_2}s+\omega_{0,2}^{2}\right)}$$

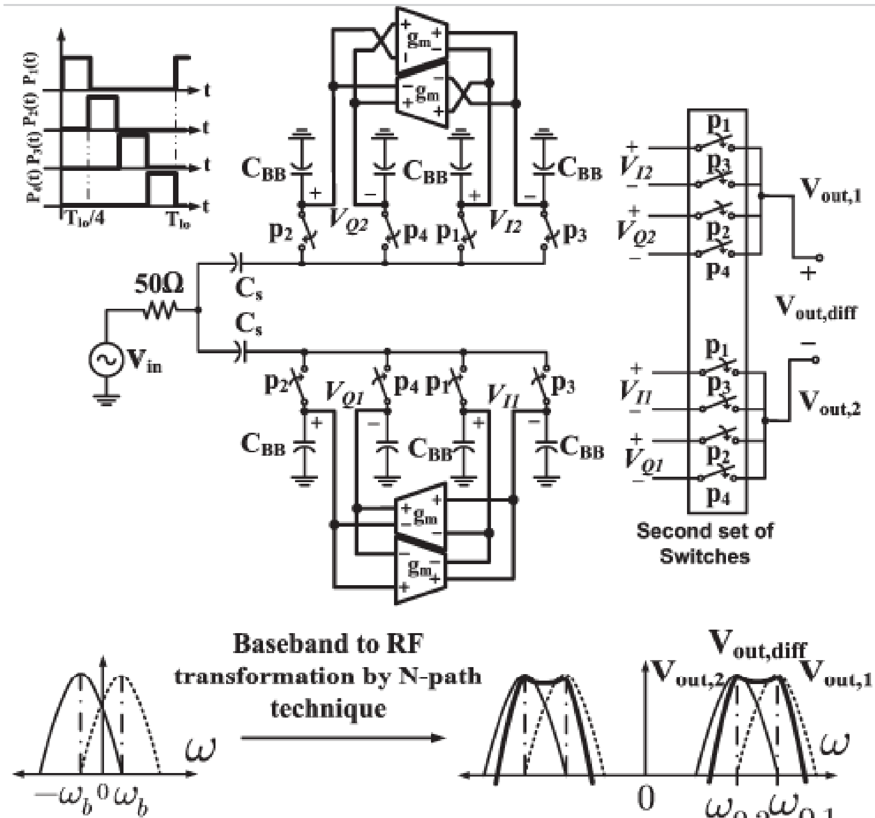


Figure 21.1.1: Subtracting the output voltage of two 2nd-order BPFs with slightly different center frequency to create a 4th-order BPF.

21.1 Continued

Filter rejection limited not by switch impedance, but by switch mismatch

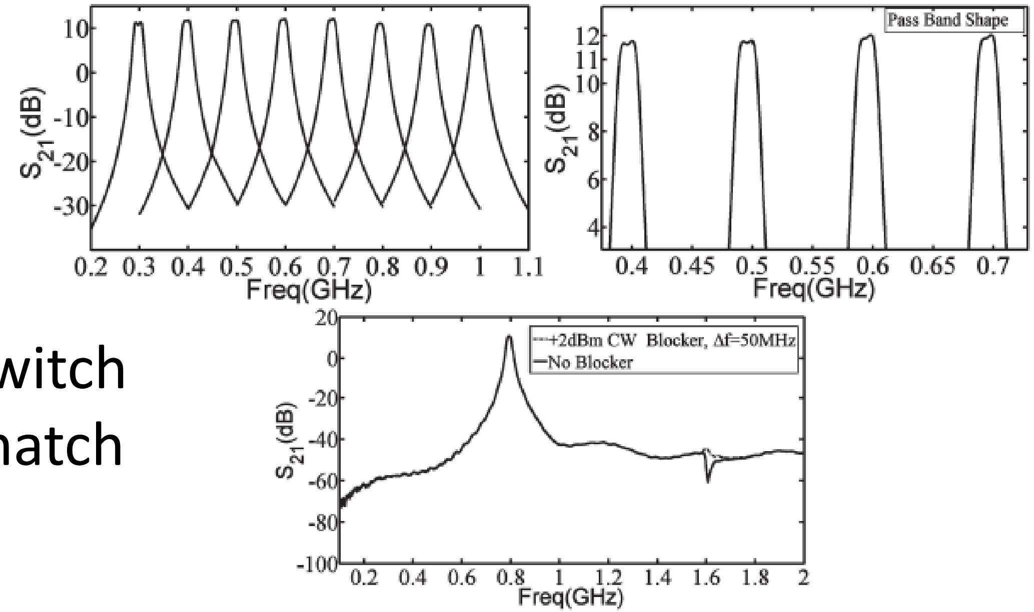


Figure 21.1.5: Measured tuneability of the filter and the filter characteristics w/wo +2dBm CW blocker at Δf=+50MHz from the center frequency.

	[4]	[5]	[6]	[3]	[2]	[1]	[This work]
Type	Receiver	Receiver	Filter	Filter	Filter	Filter	Filter
Technology[g]	65nm	65nm	65nm	65nm	250nm	SiGe: BiCMOS250nm BAW piezoelectric	65nm
Center Frequency(GHz)	2.14	0.05-2.4	0.1-1	0.08	2.14	2.14 (±0.15%)	0.3-1.2
Order of filter	6	2	2	4	6	4	4
BW(MHz)	4	20	35	10	60	60	21
Gain (dB)	+55[k]	+70[k]	-1	+2	0	-9	+3.5[h]
Ultimate Rejection (dB)	48[d]	13[i]	16[c]	32	?	28	55
P_{1dB}(in-band)(dBm)	?	?	2	?	-13.4	?	-4.4
IIP_3(in-band)(dBm)	-8.5	-67	+19	-2	-4.9	+35	+9
IIP_3(out-of-band)(dBm)	?	+25	?	?	?	?	+29[L]
NF(dB)	2.8[e]	5.5	5.5	21.5	19	9[f]	9.5[a]
Active Area(mm^2)	0.76	2.5	0.07	0.25	3.51	6.65	0.127
Max. Ripple(dB)	N.A	N.A	N.A	0.1	0.7	1.5	0.5
P_{diss}(mW)	34.2	60	18	13.2	17.5	7	17.6[b]

21.2 4th Order Filter using Ring-Oscillator-Based Integrators B. Drost Oregon State

- Replacing OTA based integrators with RO's integrators for better scaling with process

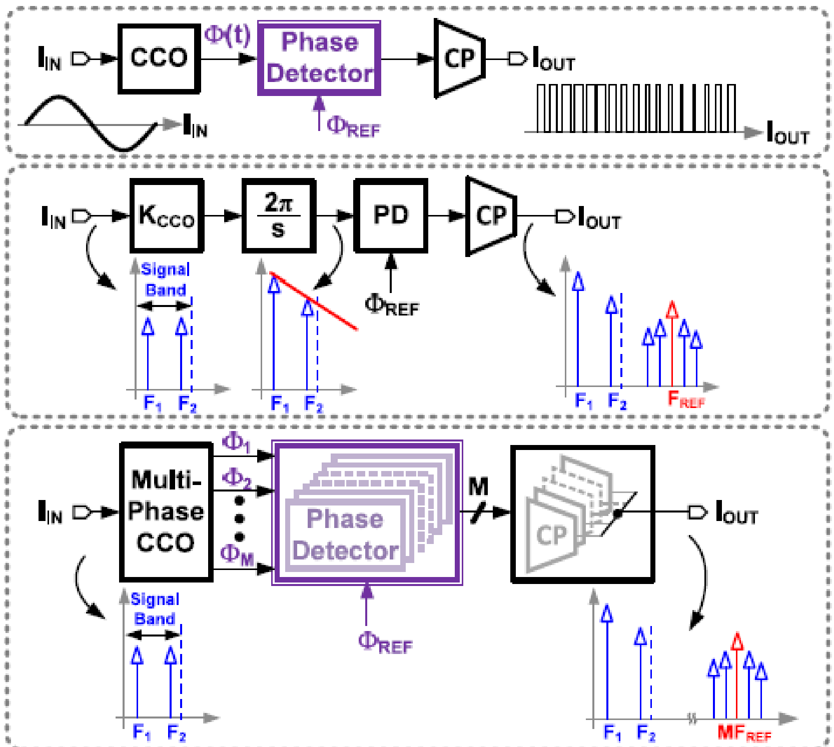


Figure 21.2.1: Conceptual diagram of the proposed ring-oscillator-based integrator (top); small-signal block diagram (middle); and multi-phase ring-oscillator-based integrator (bottom).

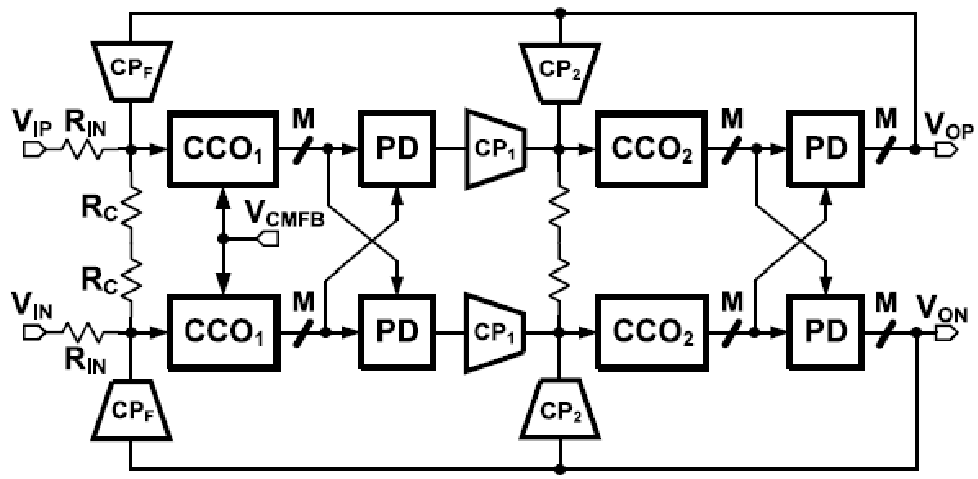


Figure 21.2.2: Block diagram of the first biquad used in the 4th-order Butterworth filter.

21.2 Continued

- RO integrators embedded in a feedback loop that keeps their input to near-zero to reduce effect of current-to-frequency non-linearity

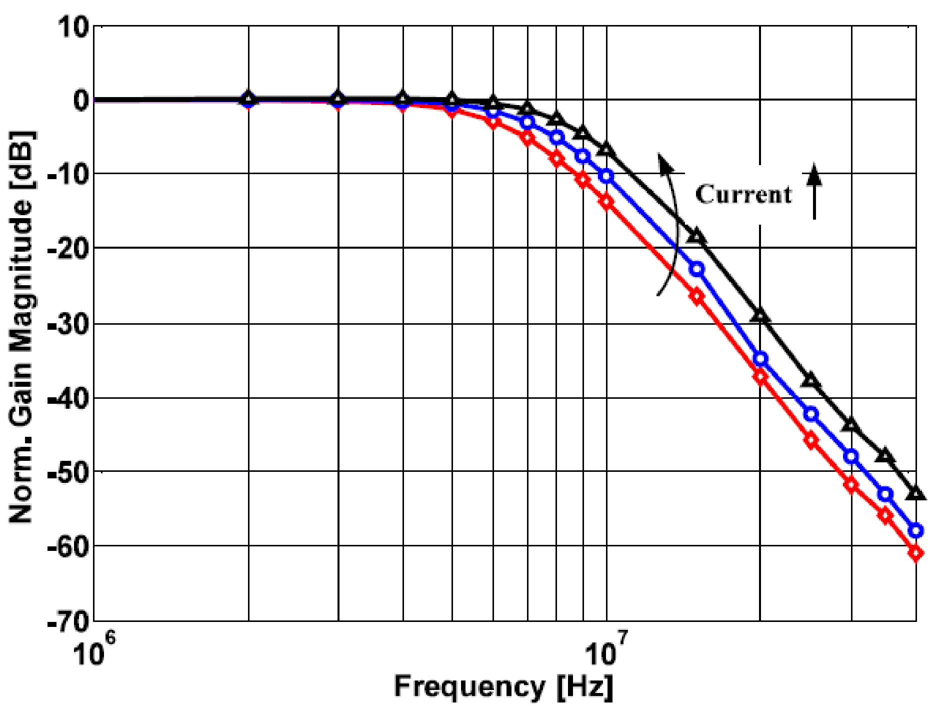


Figure 21.2.4: Measured filter response for two different charge-pump bias currents.

	This Work		JSSC 09 [4]	ISSCC 05 [1]
V_{DD} [V]	0.55	0.9	0.55	0.5
Technology	90nm	90nm	130nm	180nm
V_{TH} [V]	0.3	0.3	0.3	0.4
Power [mW]	2.9	19.1	3.5	1.1
Filter order	4	4	4	4
f_{-3dB} [MHz]	7	30	11.3	0.135
Noise [μV_{rms}]	62.4*	146.3**	110	74
DR [dB]	61	65.5	60	56.6
THD [dB]	60	65.2	40	40
Area [mm^2]	0.29	0.29	0.43	1

*input referred; integrated from 100kHz to 7MHz

**input referred; integrated from 100kHz to 20MHz

Figure 21.2.6: Filter performance summary and comparison with the state-of-the-art.