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ISSCC 2011 RF Highlights

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Outline

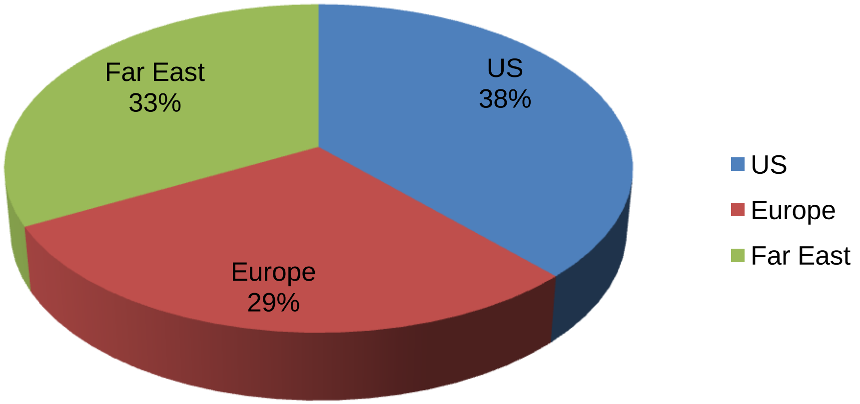
- **Overall and RF Paper Statistics**

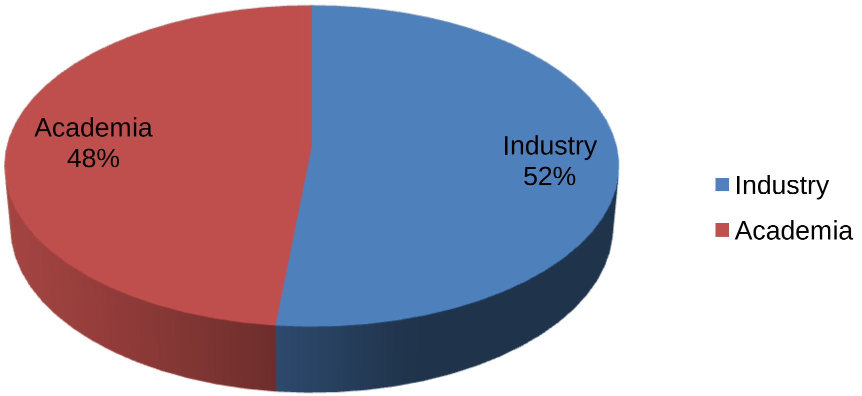
- **Trends in Wireless architectures**
  - SAW-less WBCDMA transceivers
  - Technology Scalable RF front-ends

- **RF Building Blocks**
  - Push-pull LNA’s
  - Phase shifters
  - Harmonic reject mixers
  - Noise cancelling LNA’s

Overall papers statistics

- 669 submission with 211 accepted (32% acceptance rate)
- 28 paper sessions

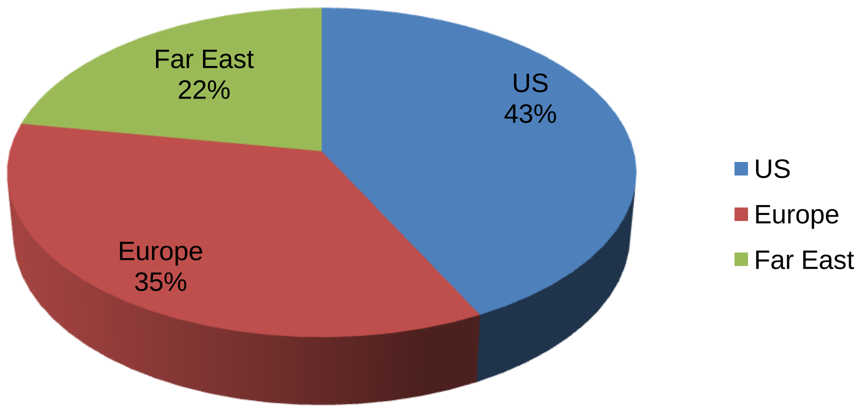


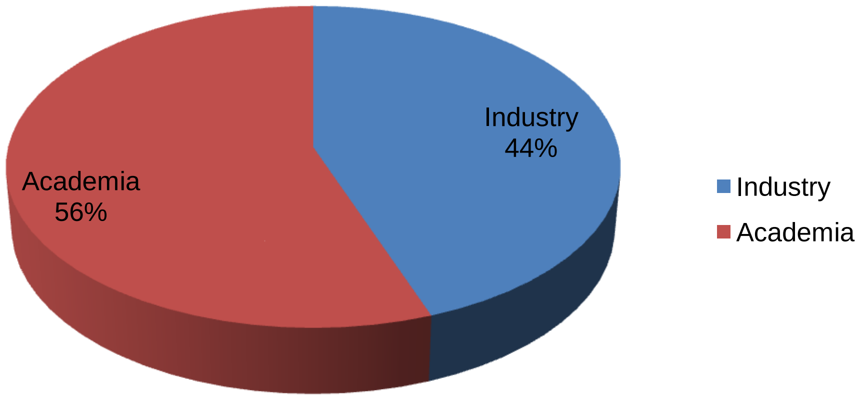


RF papers statistics

➢ RF session titles:

- RF techniques
- PLLs
- Wireless & mm-Wave Connectivity
- mm-Wave Design Techniques
- Cellular
- Transmitter blocks
- Low power wireless





Trends in Wireless architectures

- RF topics were fairly diversified.

- Two trends, however, stood out.

1. **SAW-less WBCDMA transceivers**
   - TX side solutions (Polar transmitters, 25% duty cycle passive mixing)
   - RX side solutions (High IIP2 RX path)

2. **Technology scalable RF circuits**
   - Wide-band Inductor-less designs
   - High-IF architectures with no SAW filter

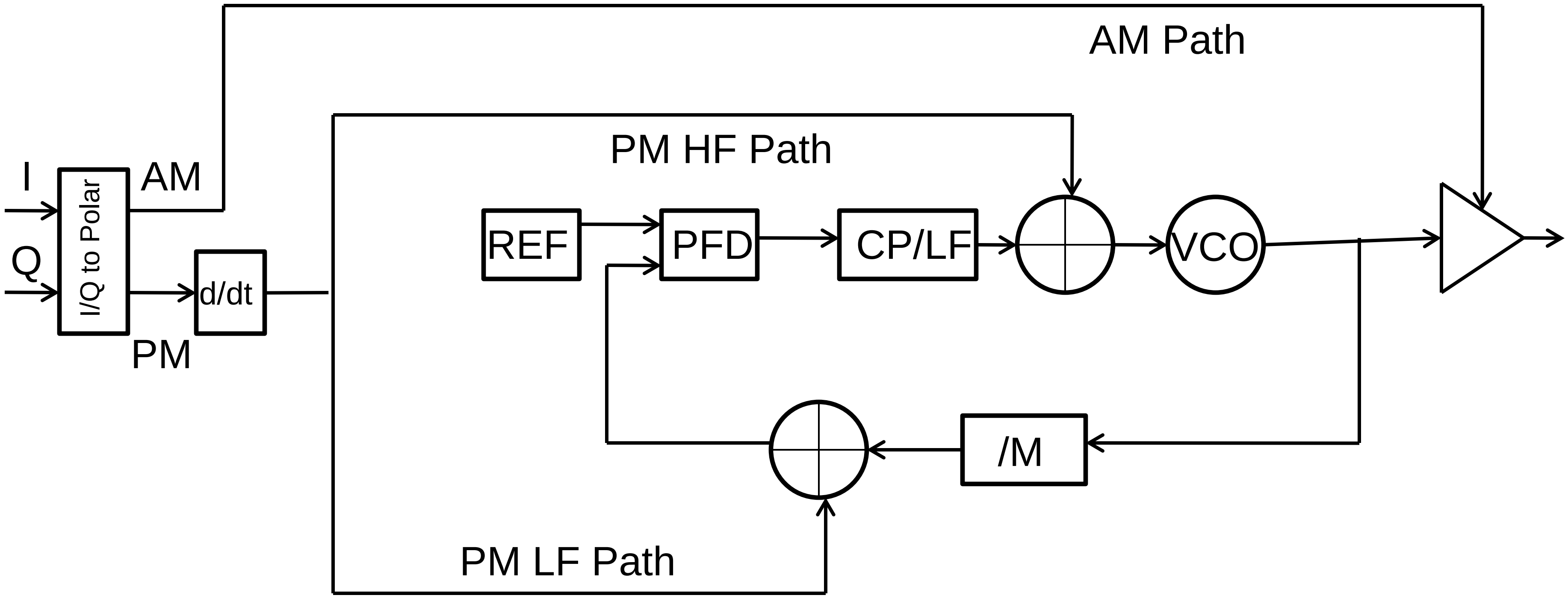
WBCDMA Issues

- **Simultaneous operation of TX and RX.**
- **The out-of-band TX noise can become in-band at RX.**
- **Large TX blockers also affect the RX through its nonlinearity.**
- **Duplexers are used to facilitate this.**
- **The TX/RX isolation, however, was not sufficient and further filtering was needed (Hence the extra SAW filters).**
- **The TX out-of-band noise can be overcome by using polar modulators**
  - Several papers were devoted to how to implement a practical polar modulator
- **A high dynamic RX chain would handle large TX blockers**
  - High IIP2 and IIP3 LNA and mixer architectures were proposed.

Polar modulators

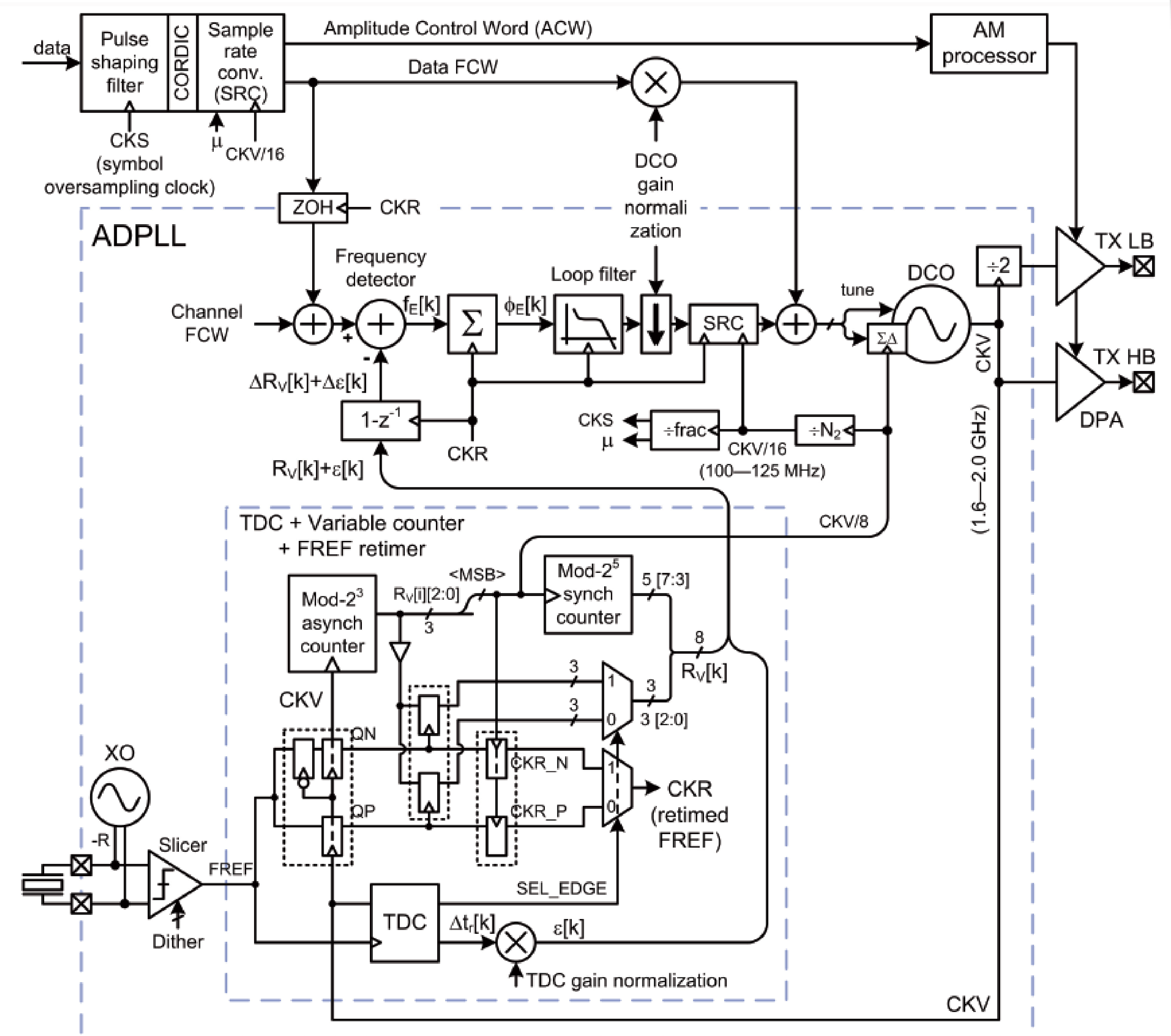
- The Cartesian (I/Q) up-conversion, while simple, has extra noisy components (such as DACs, image filters and mixers)
- Also needs a low efficiency PA.
- Alternatively, one can convert I/Q to ρ (AM) and θ (PM).
- The AM path can be applied to the PA gain and/or supply hence improving the power efficiency.
- The PM can be done by modulating a VCO phase via a PLL.
- This approach is inherently less noisy. However, …
- The delay between the two paths is crucial
  - Less than 1ns in WBCDMA
- The PM BW (8MHz) is wider than that of AM (3.84MHz) and is much wider the RF synthesizer BW (200 to 300kHz).
- Two point injection is usually used to solve this issue.

Two point injection



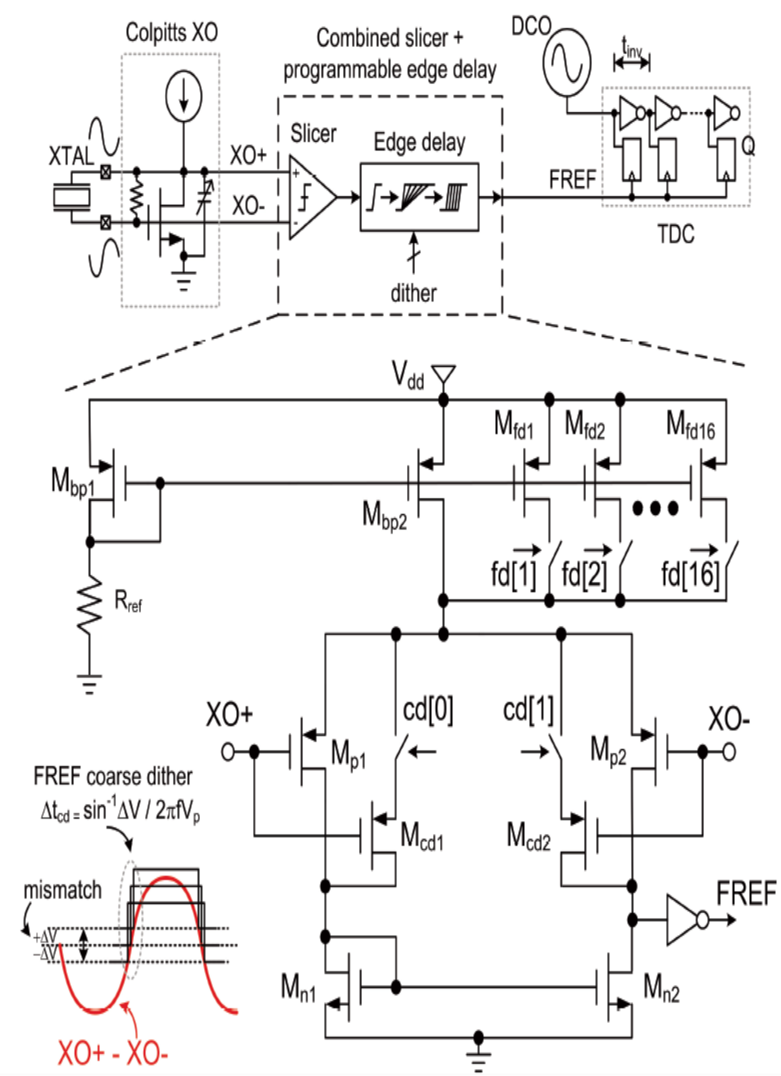
- Any injection at the VCO is HPF.
- Any injection at the PFD is LPF.
- Combined they can be ALL-pass filtered.
- VCO gain and linearity is a challenge.

3.1: Spur-Free All-Digital PLL



3.1: Spur-Free All-Digital PLL (cont.)

- **Digital implementation handles the AM/PM delay problem.**
- **PLL blocks are implemented digitally, except VCO and PFD**
  - ADC role is via Time-to-Digital Converters (TDC)
  - DAC role is played by switched cap varactor in the VCO
- **Dithering is required to break periodic quantization noise**
  - But it will increase phase noise
  - Use out-of-band tonal dither
- **VCO gain calibration is still required.**



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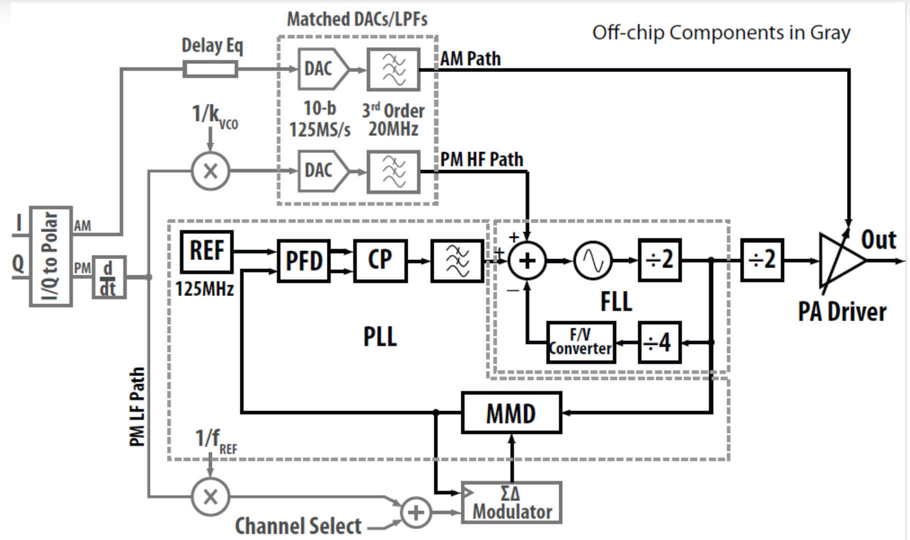
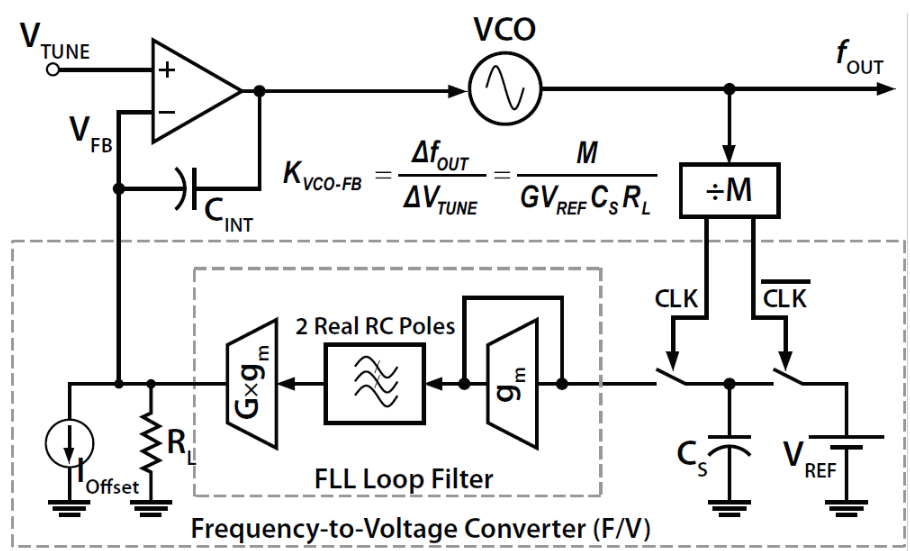
21.8 Wide-band polar transmitter

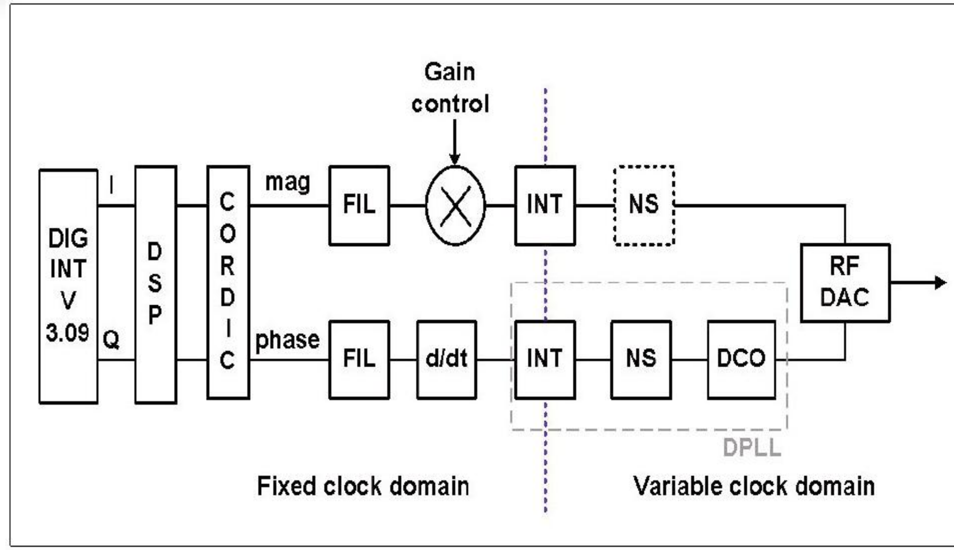
- Focuses on VCO gain and linearity issue
- Applied a feedback around the VCO to control its gain.
- The loop consists of:
  - V/F -> VCO
  - F/V -> Based on switched cap
- Switched capacitor is essentially a resistor which is a function of switching frequency.
- RC calibration can bring the VCO gain to within +-1%
- This is excluding Vref accuracy which needs a one-time factory calibration.
- The AM/PM delay matching is still a concern.

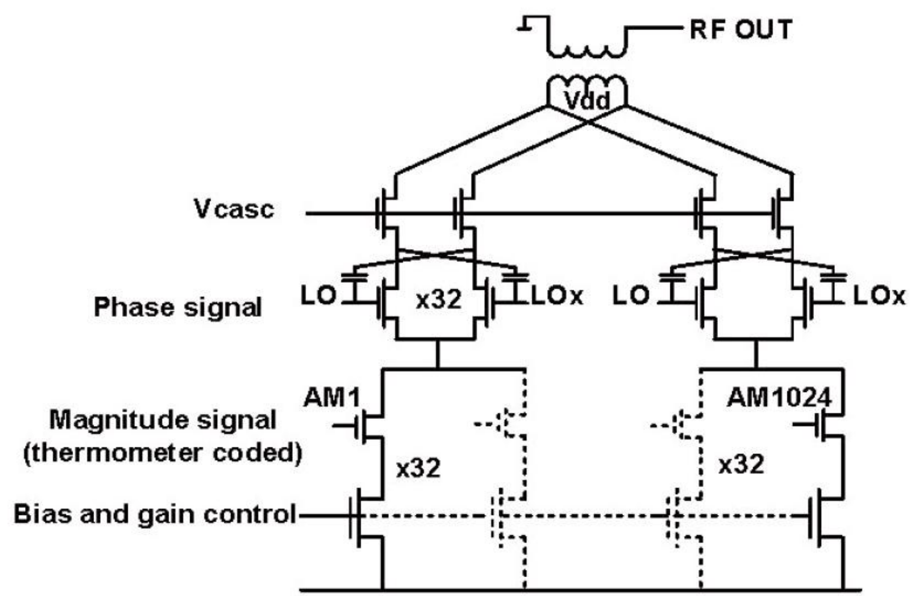




21.7 Polar transmitter employing RFDAC

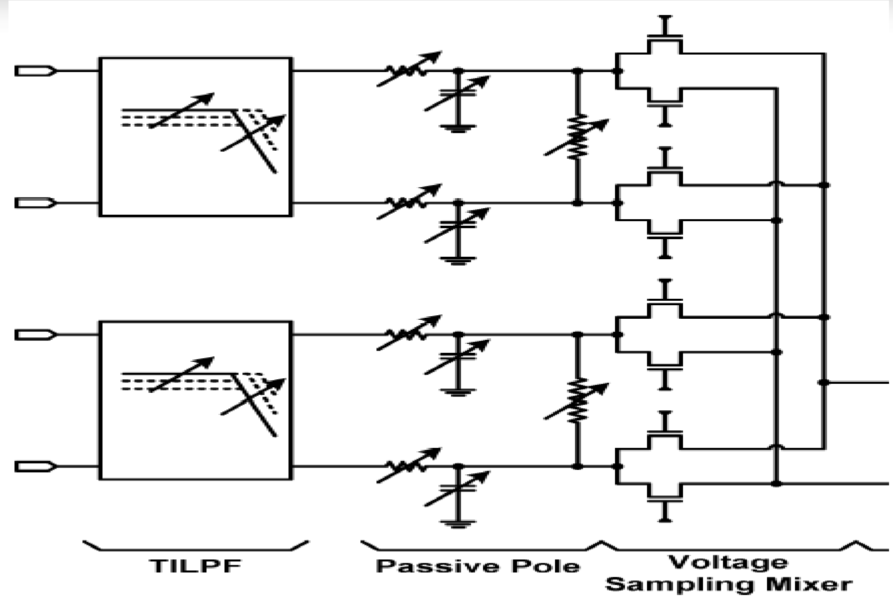
- **All digital approach to solve the AM/PM problem.**
  - All digital PLL with two point injection
- **A High DR mixing DAC is used to merge the AM and PM paths.**
  - 10 thermometer, 4 binary
  - Oversampled to GHz range
  - 17-bit resolution in 3.84MHz (CDMA)
  - 19-bit resolution in 200kHz (EDGE)
- **LO leakage is managed by:**
  - Single ended tail currents
  - Cross coupled caps.
  - Shutting off LO signal to the unused portion of the mixer when the gain is lowered.
- **Interesting, but:**
  - Higher power
  - Low efficiency PA.

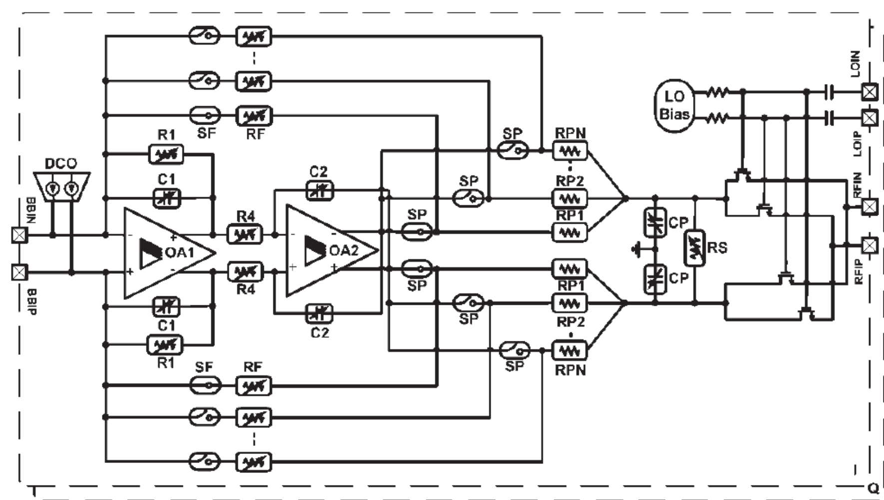




21.6: Multiband LTE in 40nm CMOS

- **Passive mixers with 25% duty cycles are used.**
  - Seamlessly performs the adding function by utilizing non-overlapping LO's
  - Reduces the number of V→I and I→V converters, hence enhancing out-of-band noise and linearity.
- **The switching along with the load capacitor synthesizes a load resistance.**
  - Affects the mixer gain
  - Compensate via variable resistor
  - Also allows variable BW.
- **Variable resistor are nonlinear**
  - Put the switch in the feedback path.



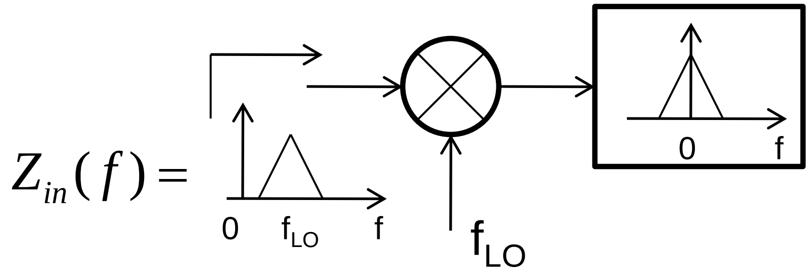


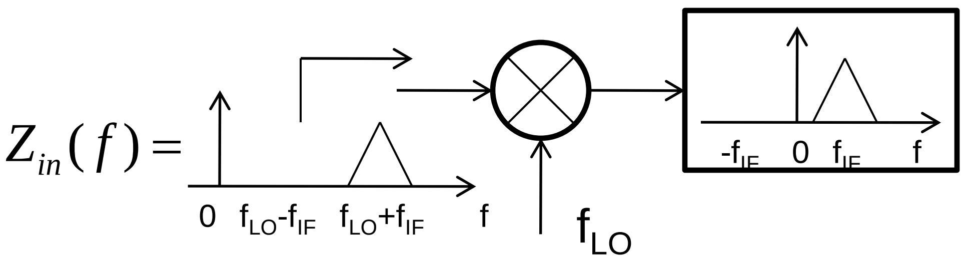
Technology Scalable RF front-end

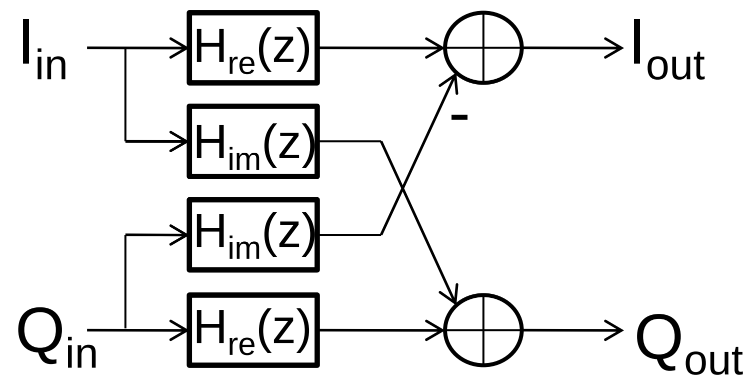
- **Finer line geometries allow digital circuit scaling.**
- **The conventional analog/RF circuits, however, do not.**
- **Two main reasons**
  - Matching requirements
  - Inductors
- **Low-IF and Zero-IF architectures eliminate the SAW filters but need high IIP2, low 1/f noise and small DC offsets**
  - All function of circuit area and hence non-scalable.
  - One paper proposed going back to high IF architectures which is insensitive to IIP2, 1/f noise and DC offset and therefore scalable.
  - A new method was proposed for highly selective filtering in lieu of SAW filters.
- **Narrow-band LNA’s require on-chip inductances.**
  - Use wide-band LNA’s (no inductor) with sufficient dynamic range instead.

3.5 Process scalable high-Q filters

- **Zero-IF and Low-IF Architectures**
  - Large RC time constants for BB
  - 1/f noise sensitive
  - IIP2 sensitive
  - DC offset sensitive
- **These are all non-scalable**
- **Use High-IF architecture**
  - Back to the past, but scalable
  - Small RC for BB
  - No 1/f noise, IIP2 or DC offset issues
  - Channel selection and Image rejection is an issue (SAW?)
- **Need a BPF for channel selection and image rejection**
  - Channel selection: Use real_in/real_out Z for BPF centered at F_{sw}.
  - Image Rejection: Use Complex_in/Complex_out Z

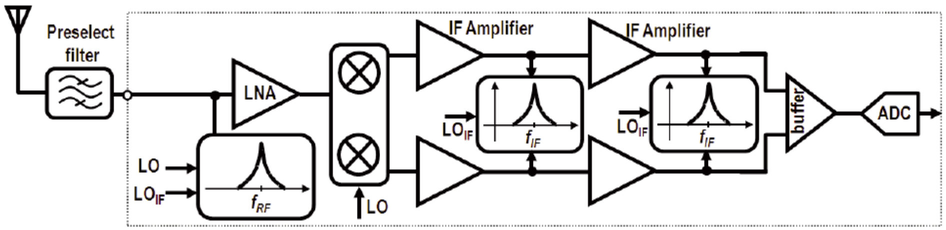


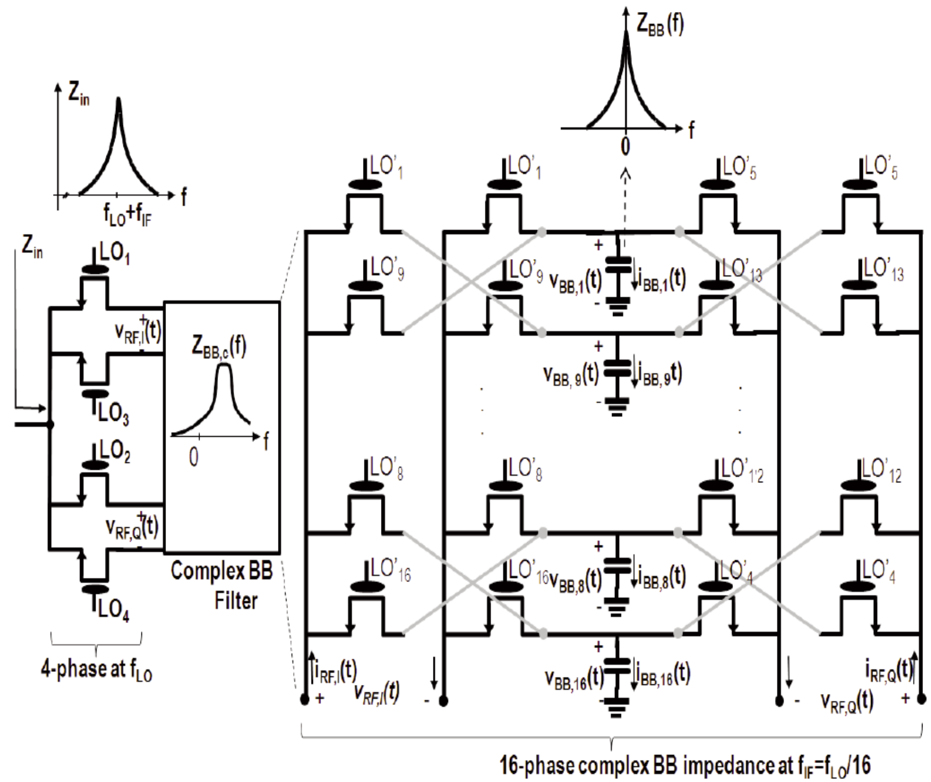




3.5: Process scalable high-Q filters (cont.)

- **A complex loaded switched BPF at LNA input**
  - Protects the LNA from blockers and image.
  - 10dB image rejection.
  - The complex load is based on a 16-phase (16-path) switched capacitor.
  - $16*F_{if}$ is chosen to push the folding frequencies to $15*F_{if}$ and $17*F_{if}$
- **Use cascaded complex loaded switched BPF at BB for more IR.**
- **Issues:**
  - Some preselect filtering is still required to attenuate folding frequencies.
  - Also, blockers at LO harmonics needs rejection.
  - LO feed though to antenna.
  - No Phase noise relaxation.
  - Only 50dB image rejection.





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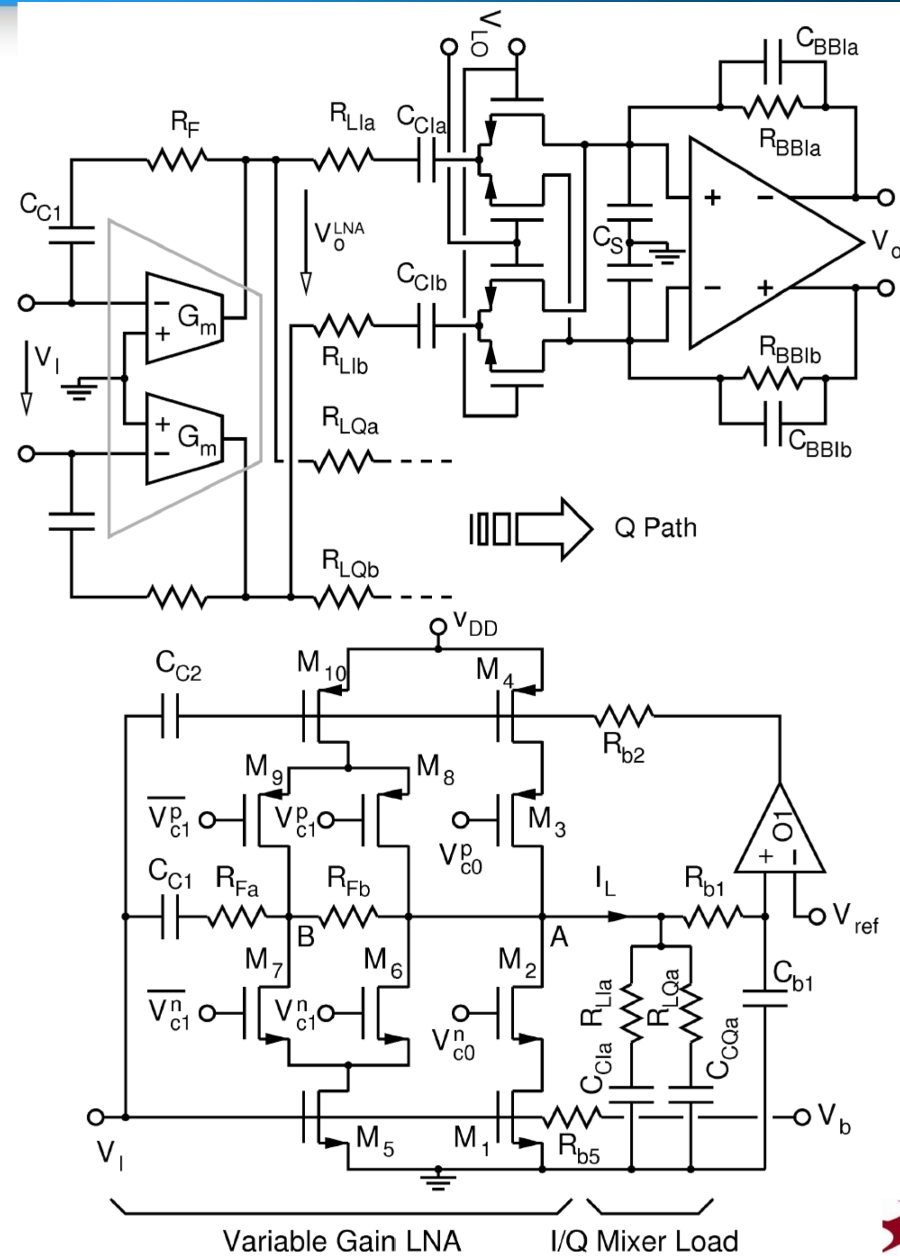
21.4 Inductorless WBCDMA/EDGE in 65nm

- **Multi-band RX need multiple LNA's**
  - No tunable pre-select filters
- **Each NB LNA has inductors**
  - Too many inductors
  - Not scalable
- **Use WB shunt feedback**
  - To change the gain turn portion of the FB resistor into load.
  - To keep the Z_{in} change the Gm.
- **Current-mode mixer**
  - DC to RF virtual ground
  - RI acting as degeneration for SW's making them linear.
  - AC coupling help 1/f noise and IIP2
- **Highly linear LNA and mixer**
  - No need for inter-stage SAW
  - LO coupling to RF minimized since there are no inductive coupling



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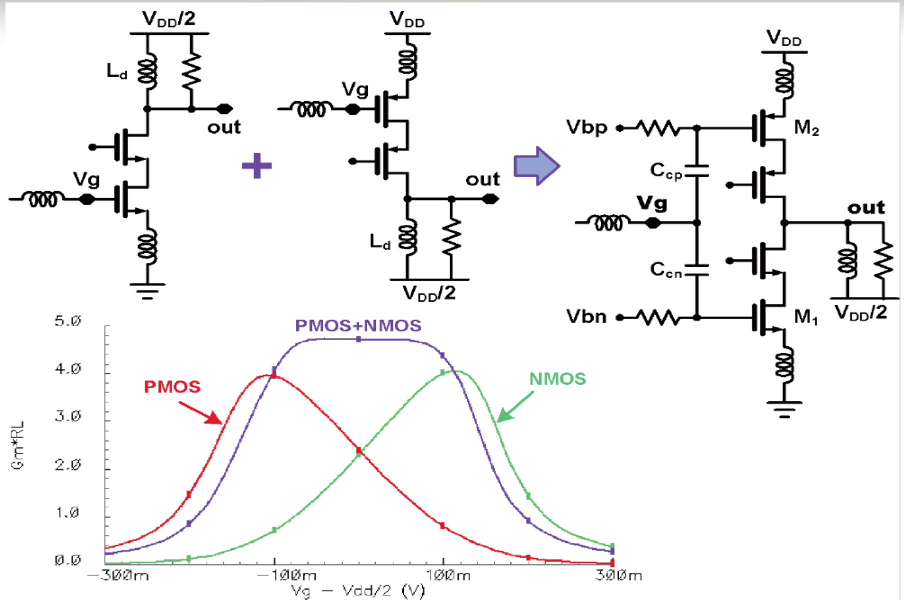
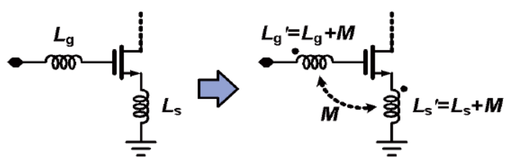
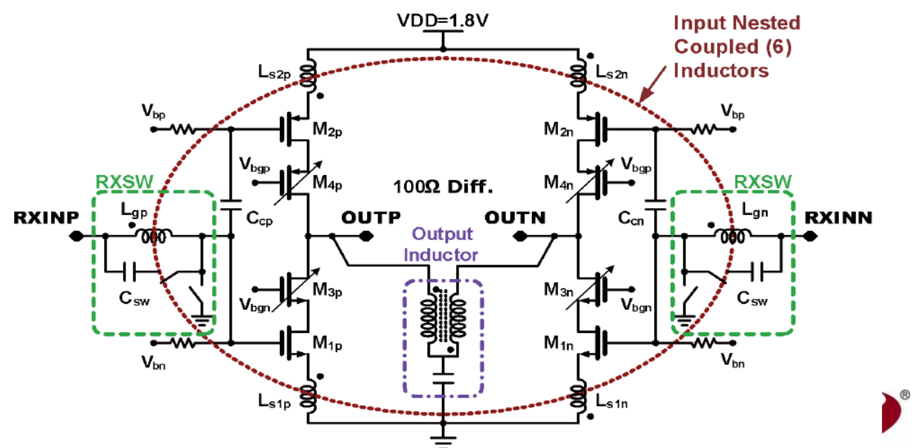
3.3: Push Pull LNA in 32nm

- **Use both PMOS and NMOS Gm's**
  - Intel's 32nm High-K metal gate process has similar strength PMOS and NMOS
  - Similar value for Lp and Ln.
- **Stacked output to ensure reliability**
- **But twice an many inductors are used compared to the single-ended case.**
  - The gate inductors are used by the transmitter as well.
  - Since the current in the four inductors are either in-phase or out-of-phase, they can be closely coupled.
  - This will increase the effective inductance.
  - It also allows them to be laid out on top of one another.







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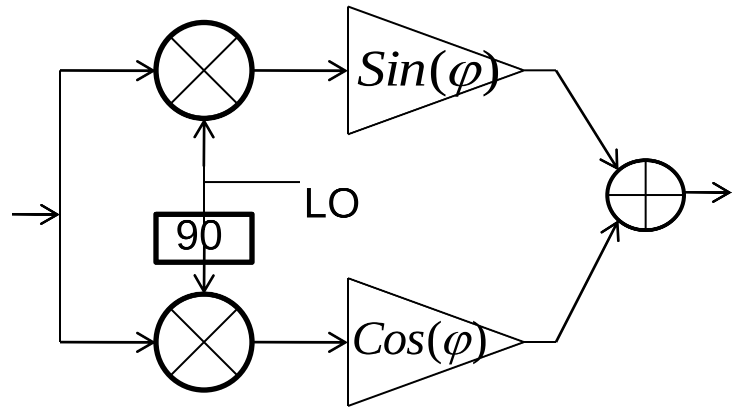
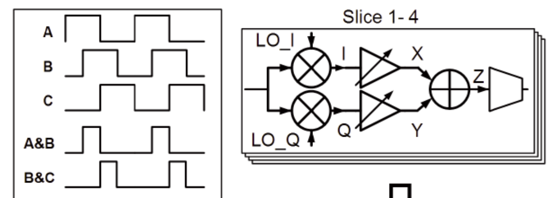
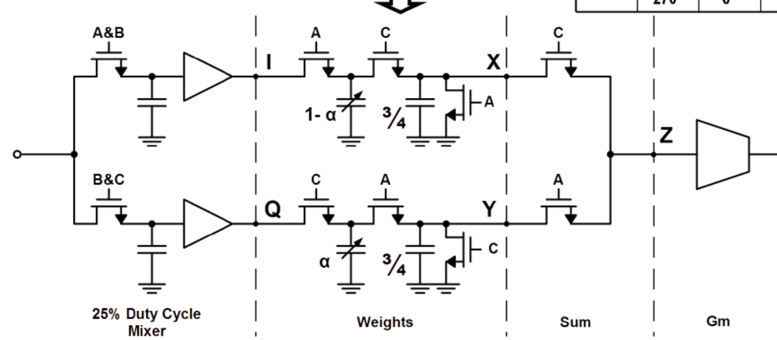
3.7: Phase shifter in 65nm

- **Multiple antenna Phased arrays**
  - Increase SNR
  - Spatial interferer rejection
- **Vector rotation**
  - Quadrature down conversion
  - Sine and Cosine gains
- **Sine and Cosine gains**
  - Non-uniform Sine step vs. phase step
  - Gain need high resolution
- **Approximate Sine and Cosine**
  - Use a fractional ratio
  - Uniform phase step -> almost uniform alpha step (cap steps)
  - Switch capacitor compatible
  - The final summation is done via charge sharing as well.





Slice	A	B	C
1	LO 0°	LO 90°	LO 180°
2	LO 90°	LO 180°	LO 270°
3	LO 180°	LO 270°	LO 0°
4	LO 270°	LO 0°	LO 90°



$$Y = Q \cdot \frac{\alpha}{\alpha + 3/4}$$

$$X = I \cdot \frac{1 - \alpha}{1 - \alpha + 3/4}$$

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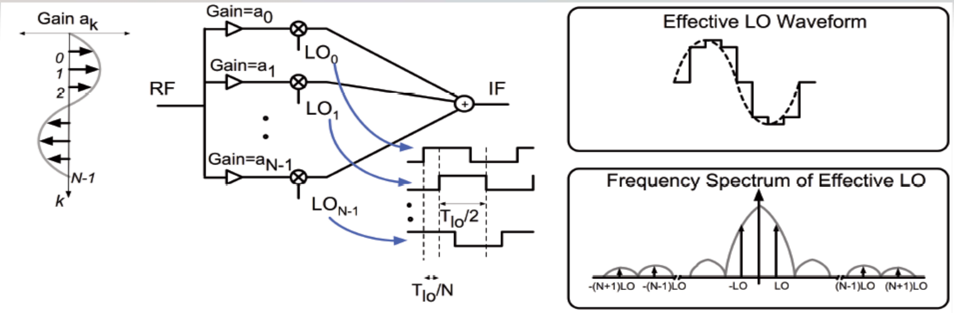
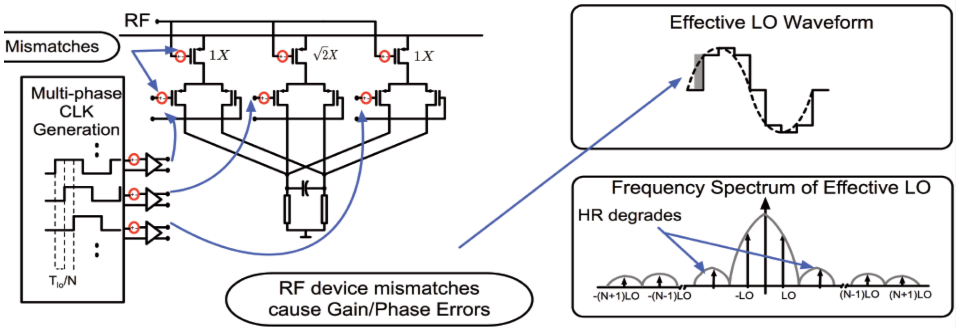
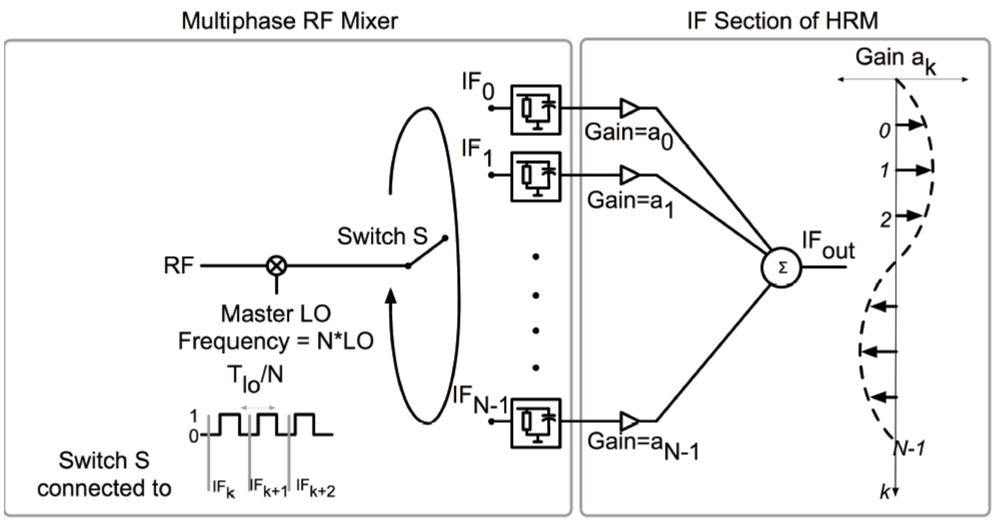
3.8: Harmonic rejection mixer (HRM)

- **LO waveform is rectangular**
  - Rich in higher harmonics
- **Conventional HRM**
  - Uses RF weighting
  - Needs RF matching (hard to do)
- ***Any imperfect matching causes HR deterioration***
- **What if the weighting is done in IF**
  - Lower frequency
  - Easier to match
- **Furthermore two layers of switches are used**
  - By commutating the second switch after the first one is done:
    - Second layer switch mismatch irrelevant
    - Robust 1/f noise and IIP2
    - Improved image rejection

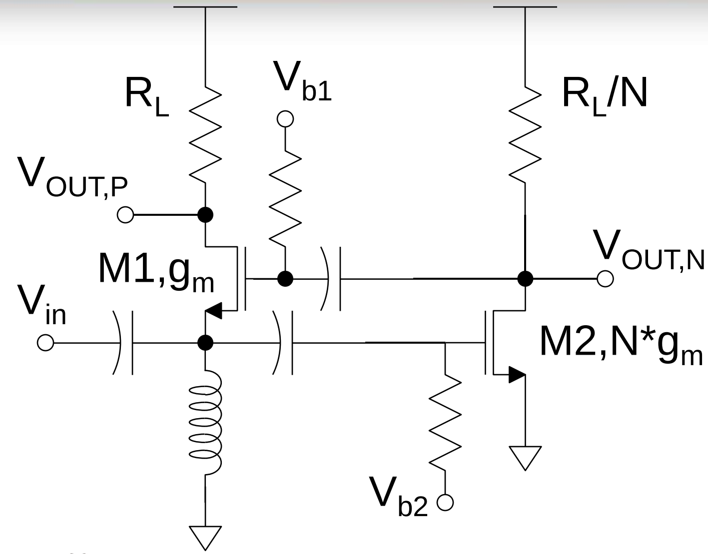


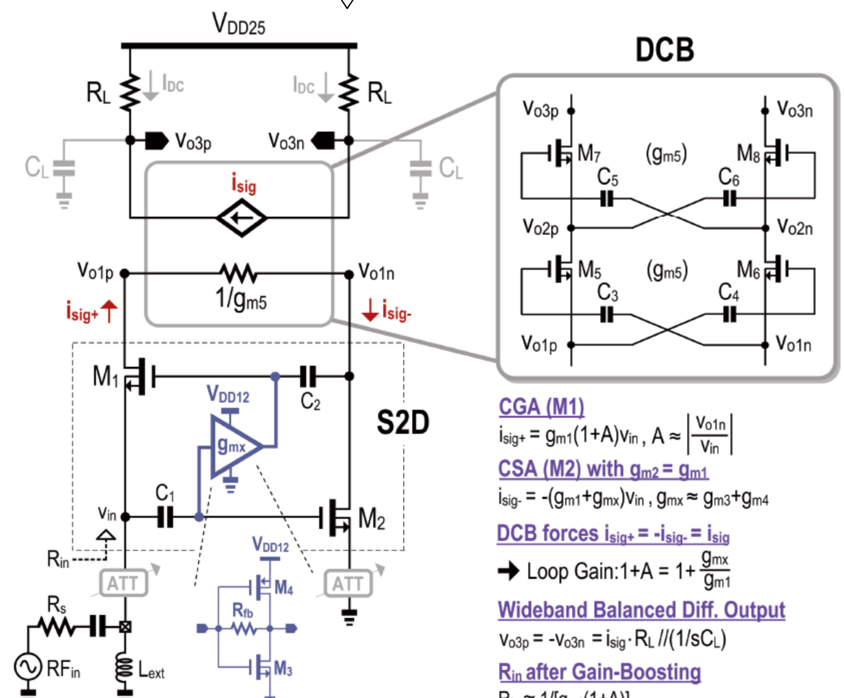




9.7: Noise cancelling LNA

- **TV application**
  - Wide-band input matching
- **Conventional noise cancelling LNA**
  - Loop gain around M1 reduces its input impedance and noise.
  - M2's gm is higher to reduce NF.
- **But the output is not balanced.**
  - Higher IIP2
  - Output buffers
- **Use similar M1 and M2**
  - Use auxiliary G_{mx} for gain boosting around M1.
  - Also biases the two gates.
- **Use current balancer to enforce isig+ = -iseg-**
  - $R_{in,CM} >> R_{in,DM}$
  - Rds will reduce the impact
  - Use cascade stages.





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