Central Texas Section IEEE SSCS ISSCC 2011 Memory Overview

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Memory Strategies International

<www.memorystrategies.com>

ISSCC 2011

Session 11 NAND Flash

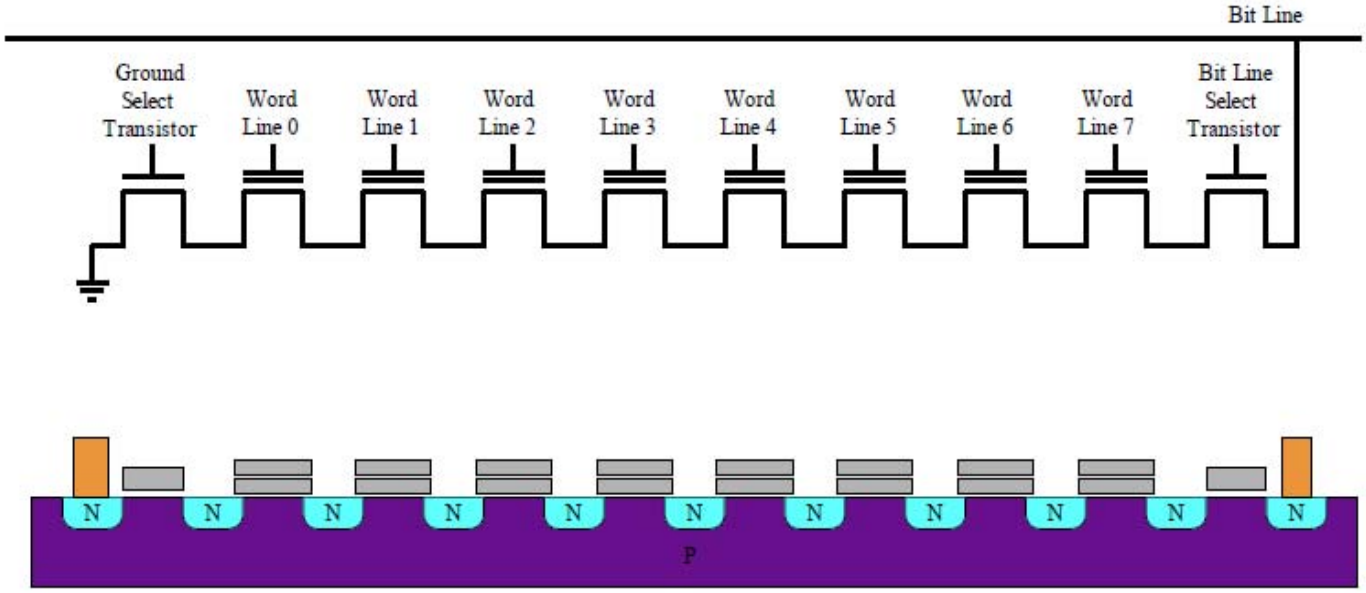
Emerging Non-Volatile Flash

Session 14 SRAM

Session 28 DRAM and High Speed I/O

Memory Strategies International

Basic NAND Flash Circuit and Cross-Section



NAND: A high on all the WL, takes the BL low

READ: To read, WL(Unselected) > Vt(PGM), WL(Selected)> Vt(erase).
BL Low if selected bit not programmed

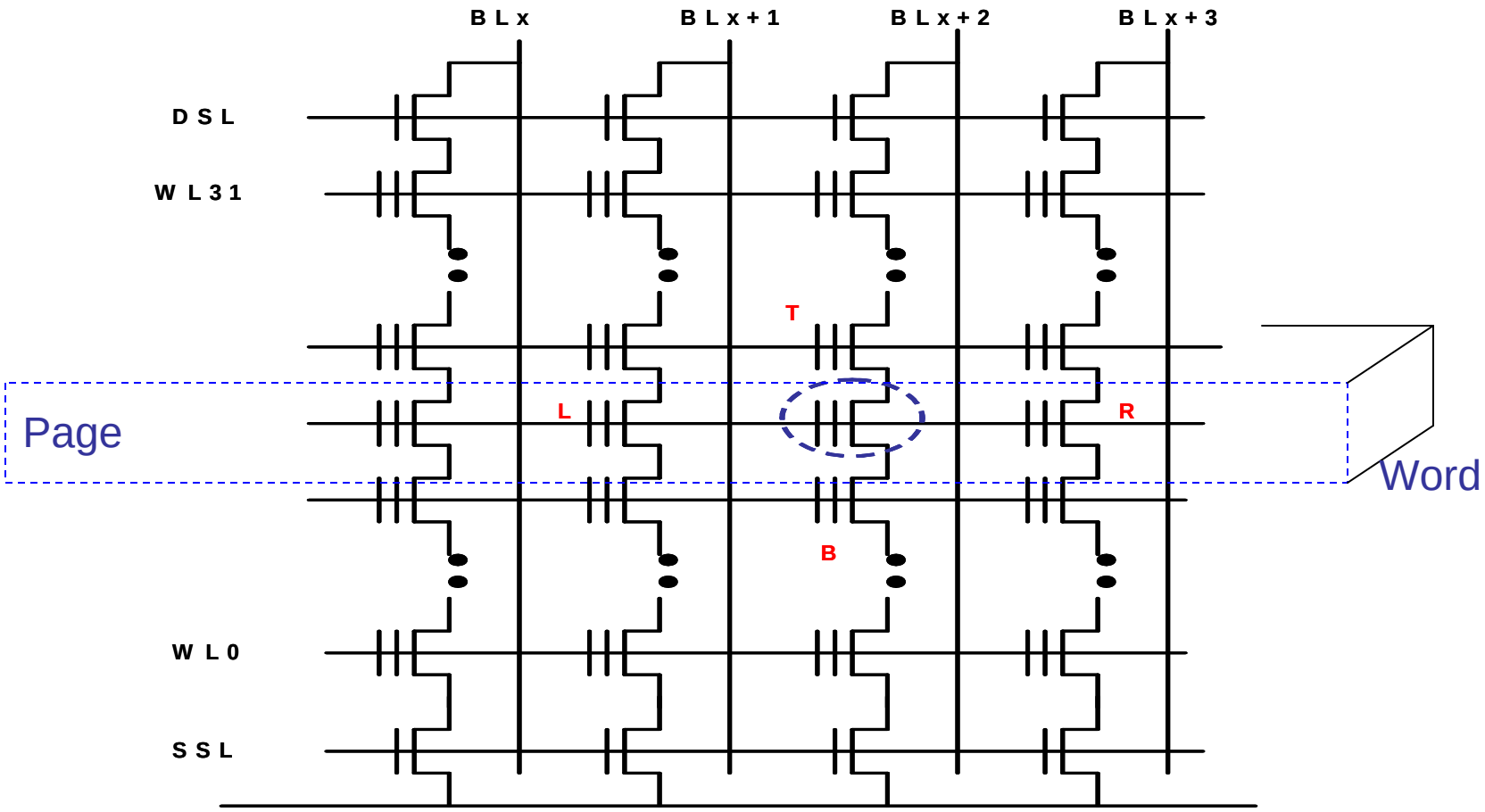
Program: Word Erase: Block Erase

Wikipedia, NAND Flash

ISSCC Session 11, NAND Flash

Illustration of a NAND Flash Array

Page X Word = Block



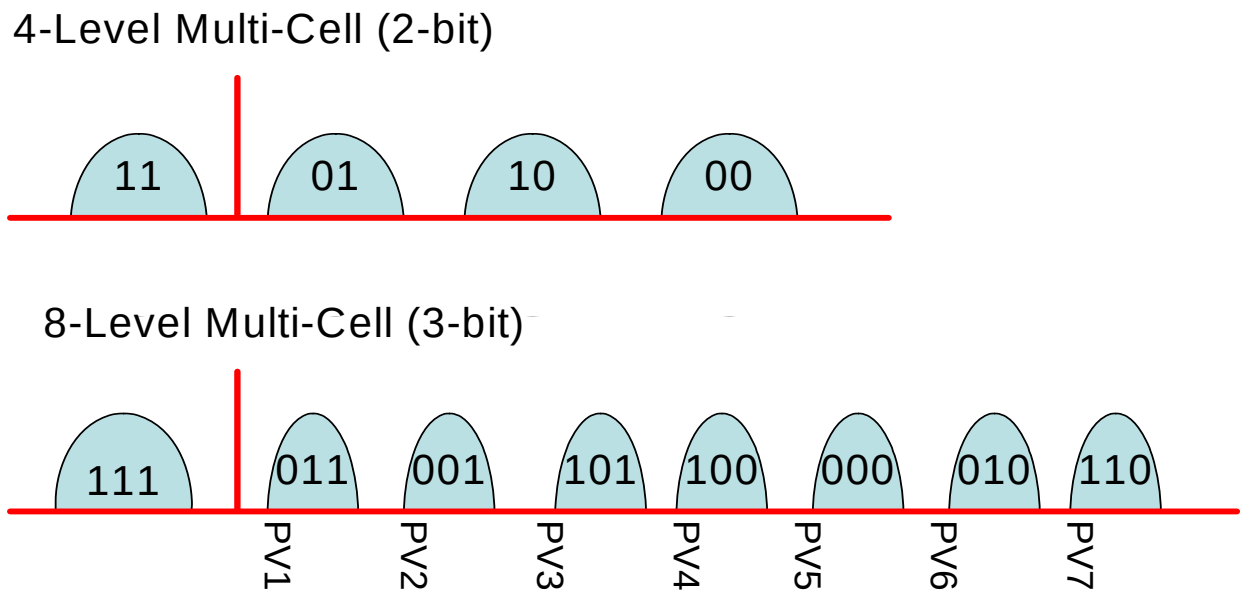
MSI Flash Report, Feb. 2010,

NAND Flash Issues

Improve Programming Speed

Improve Data Rate for Read

Threshold Voltage large enough for multi-level cell.



MSI Flash Report, Feb. 2010,

Session 11 NAND Flash

1. NAND Flash with Wider Vth Margin Window (Hynix)

32 Gb MLC(2) 26 nm NAND Flash, chip size 181.5 mm2.
Applied a negative voltage to the wordline and used a new bit line compensation method to get larger Vth margin window to program. This improved MLC reliability and performance. (11.3)

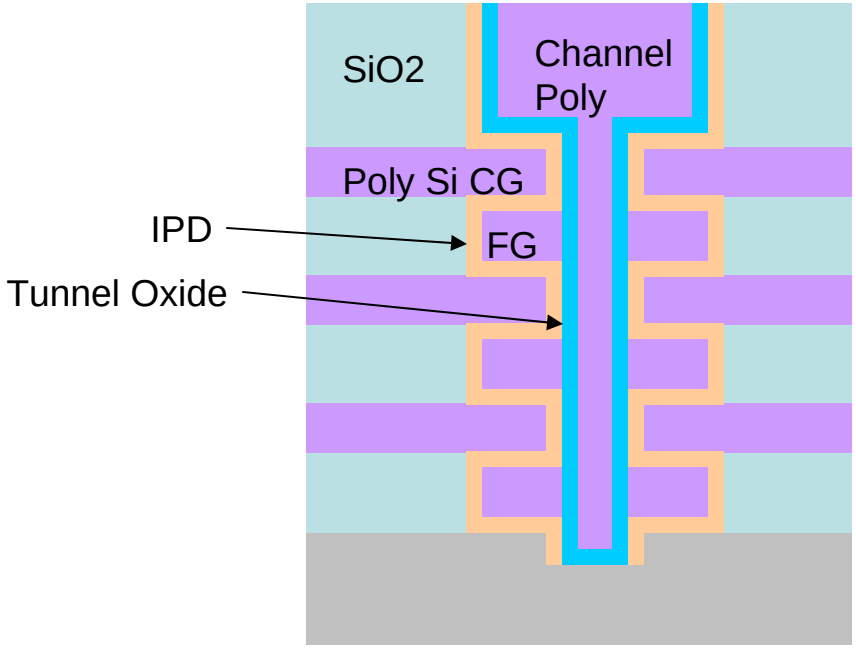
2. NAND Flash Faster Programming (Toshiba/Sandisk)

64 Gb MLC(2) 24 nm NAND with 151 mm2 chip size. 14 MB/s program and 266 MB/s data transfer. A bitline precharging algorithm during programming improves throughput by 5% and reduces current by 6%. (11.1)

3. NAND with High Throughput DDR Interface (Samsung)

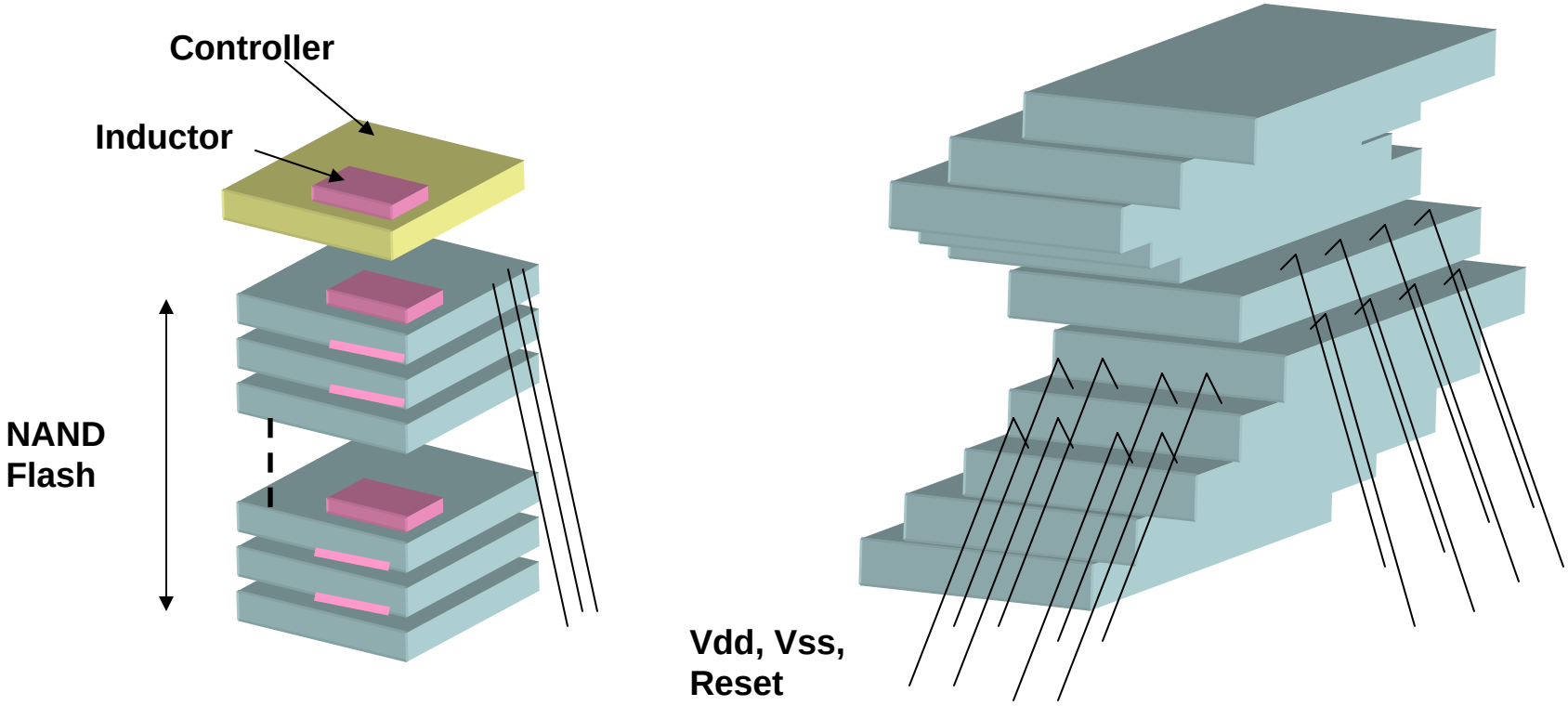
64 Gb TLC(3) 27nm NAND Flash with 200 Mb/s DDR interface for data transfer to page buffer. Used 2-step verify ISPP and fail page copy-back program function to enhance performance. (11.8)

3D NAND Flash
Vertical Pipe FG NAND Flash



Hynix, IEDM, Dec. 2010

3D NAND Flash
Stacked Inductive Coupling Interface



Y. Sugimori, et al, "A 2Gb/s 15pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking", (Keio U., U. of Tokyo), IEEE ISSCC, February 2009.

M. Saito, N. Miur, T. Kuroda, "A 2Gb.s 1.8pJ/b/chip Inductive-Coupling Through Chip Bus for 128-Die NAND-Flash Memory Stacking", (Keio U.), IEEE ISSCC, Feb. 2010.

Stacked Inductive Coupling Interface for NAND Flash

Bandwidth = 2.7 Gb/s/mm2

Energy/chip = 0.9 pJ/b/chip

BW increased by 10x, Energy reduced by half.

A relayed transmission method used one coil to reduce number of coils in the data link. Coupled resonation is uses for clock and data recovery resulting in elimination of a source synchronous clock link.

As a result, the total number of coils needed for a channel is reduced from 6 to 1. Better data rate, layout area and energy consumption.

N. Miura, Keio U., ISSCC, Feb. 2011

Stacked Inductor NAND Flash

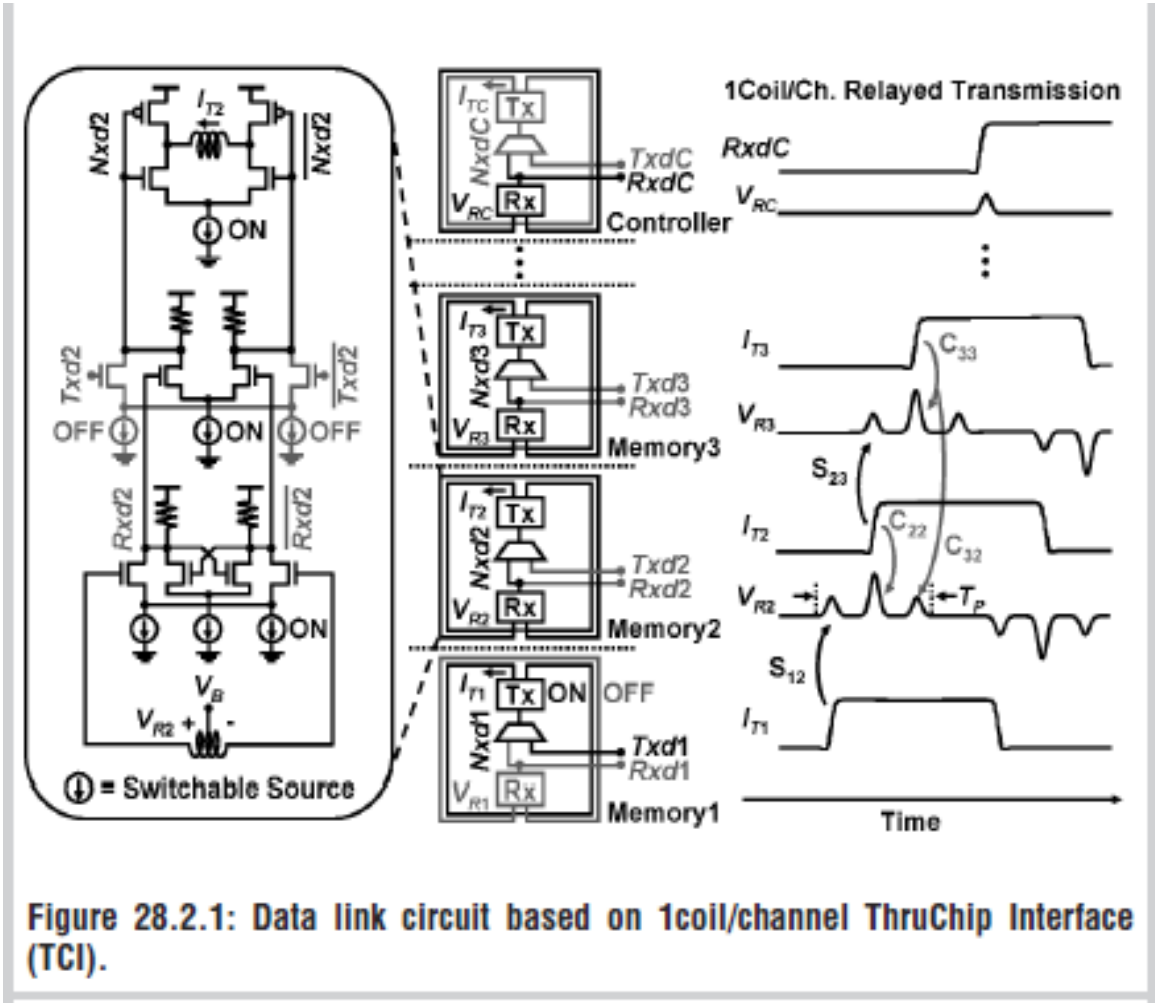


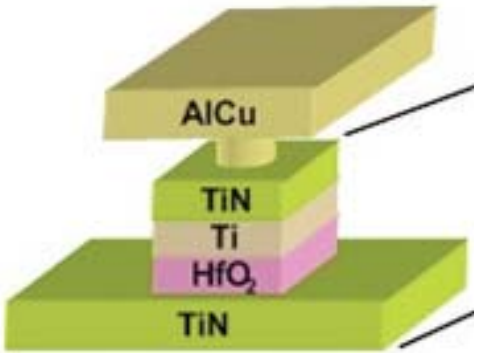
Figure 28.2.1: Data link circuit based on 1coil/channel ThruChip Interface (TCI).

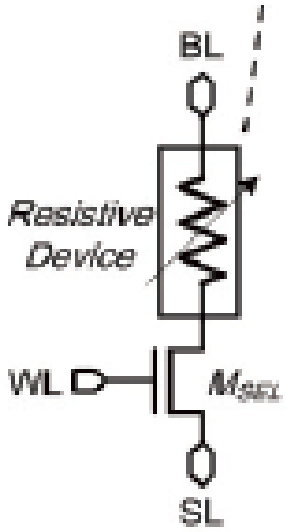
N. Miura, Keio U., ISSCC, Feb. 2011

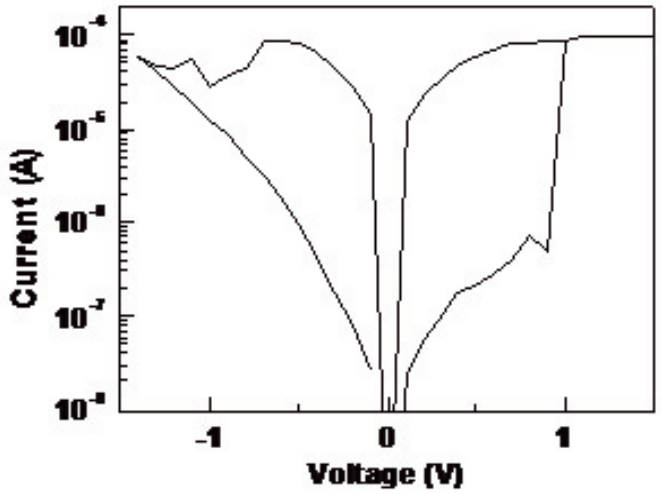
Session 11 - Emerging Non-Volatile Memory

RRAM: Fast RRAM (11.2)

4 Mb SLC RRAM 1T1R Cell with NMOS selector and HfO2 type Bipolar Resistive Memory element. 7.2 ns read-write Random Access time. 2-bit/cell with 160 nm Write-Verify. R-ratio = 100. RRAM advantages: fast write, large R ratio, small write power consumption.







SS Sheu, ITRI, NTHU, ISSCC, Feb. 2011

Session 11 - Emerging Non-Volatile Memory

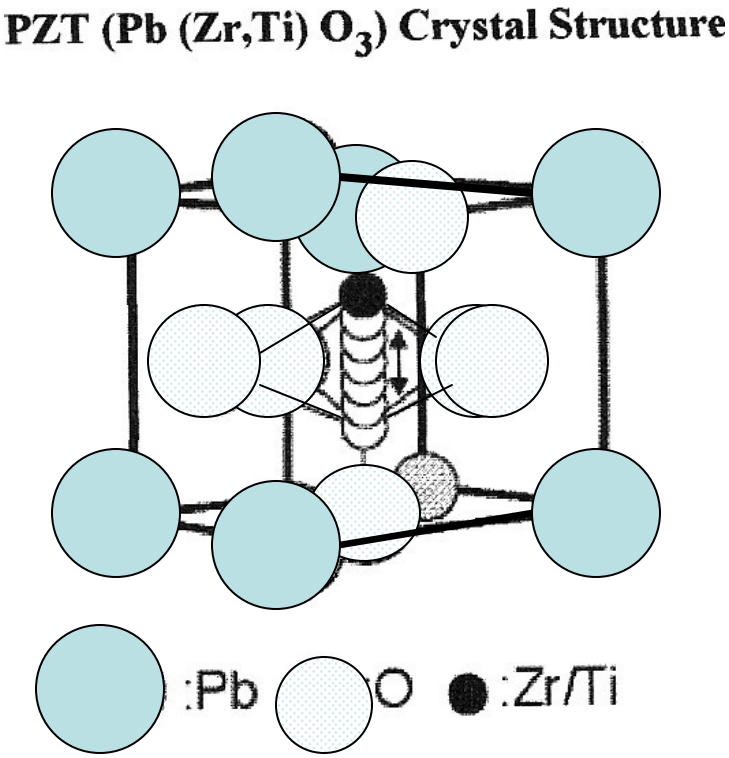
RRAM: (11.2 – Fast RRAM)

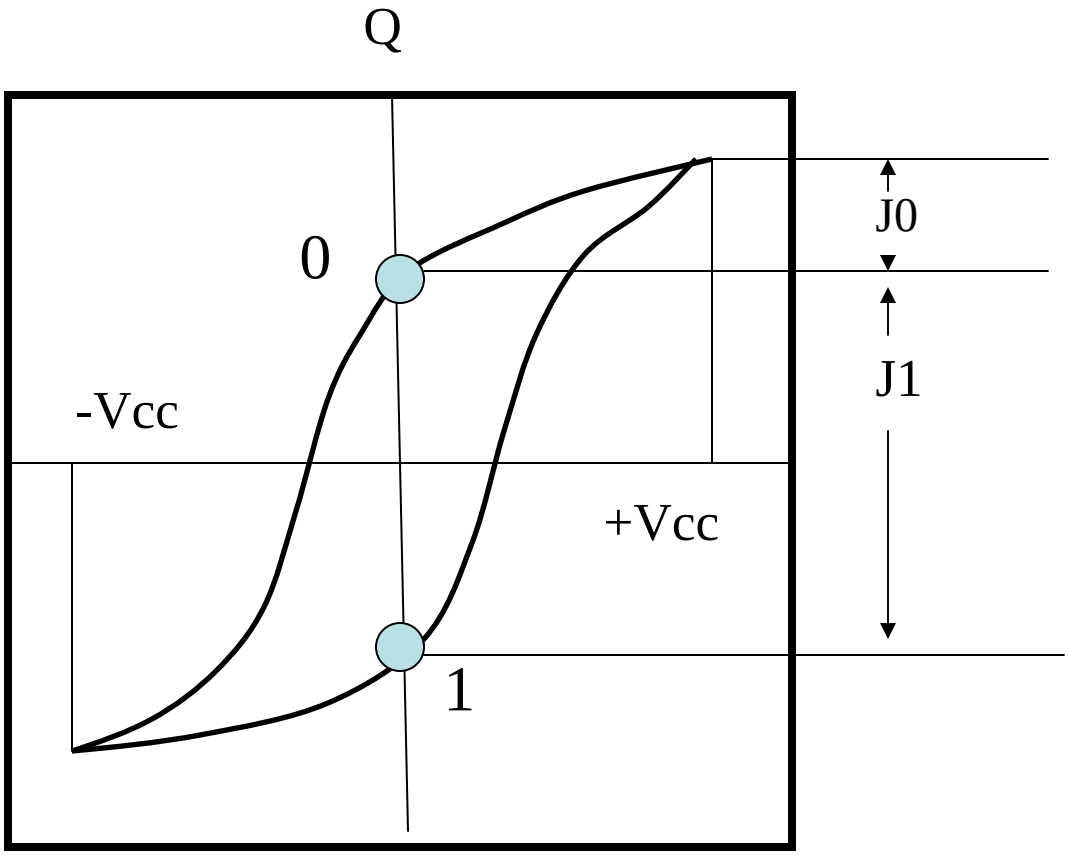
1. RRAMs have inter and intra-die resistance variations which effect RRAM reference cells. A parallel-series reference cell scheme narrows the Iref distribution against R-variation.
2. RRAMs require low read BL bias voltage to prevent read disturbance. This paper has resistance variation insensitive read method using a temperature aware dynamic bitline bias circuit.
3. MLC operations achieved using different WL voltages.

SS Sheu, ITRI, NTHU, ISSCC, Feb. 2011

Ferroelectric Memory

Stores Data in Distortion of Crystal Structure





A Low Voltage, Low Current, Non-Volatile SRAM

Memory Strategies International

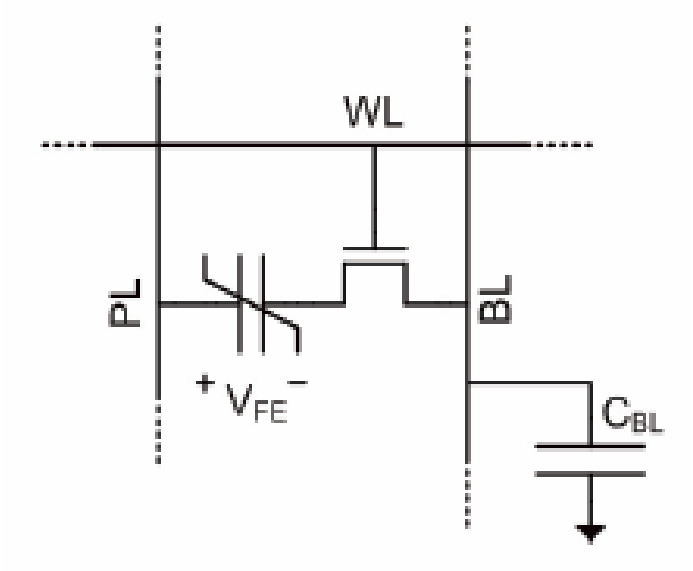
Session 11 - Emerging Non-Volatile Memory

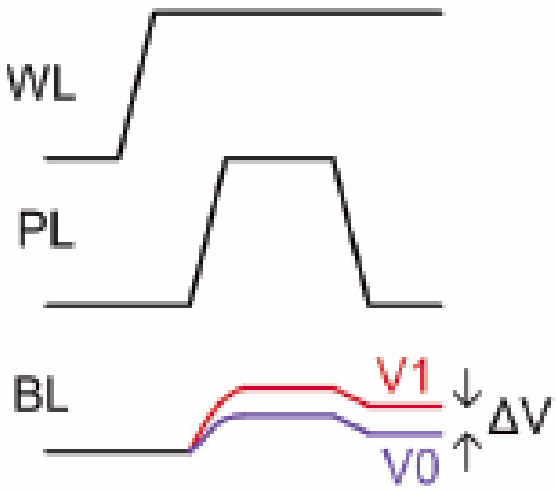
FeRAM with Low Voltage Operation (11.6)

1Mb 130 nm Low Voltage FeRAM with 1024 1T1C cells/BL

Target application: low power implantable medical devices

Issue: Scaling to 1V and below.

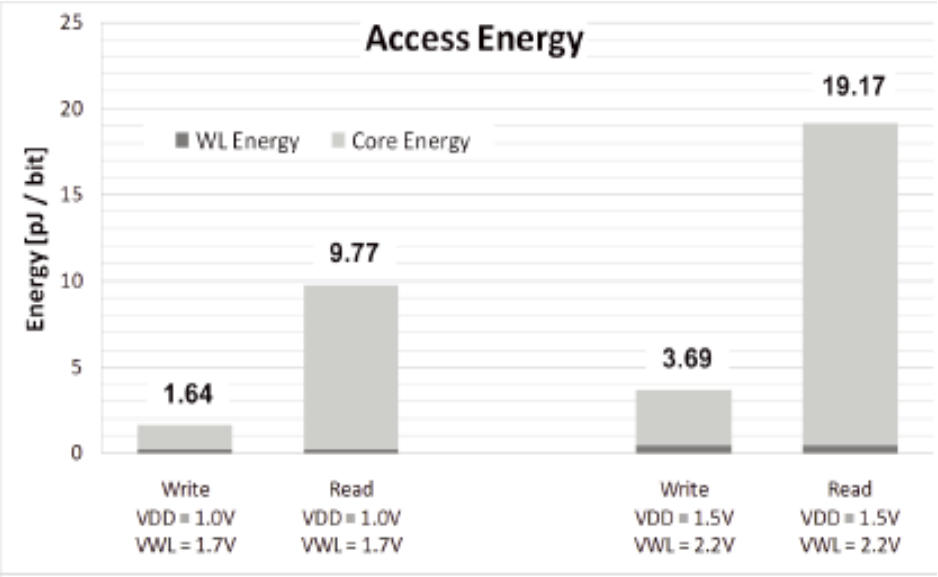


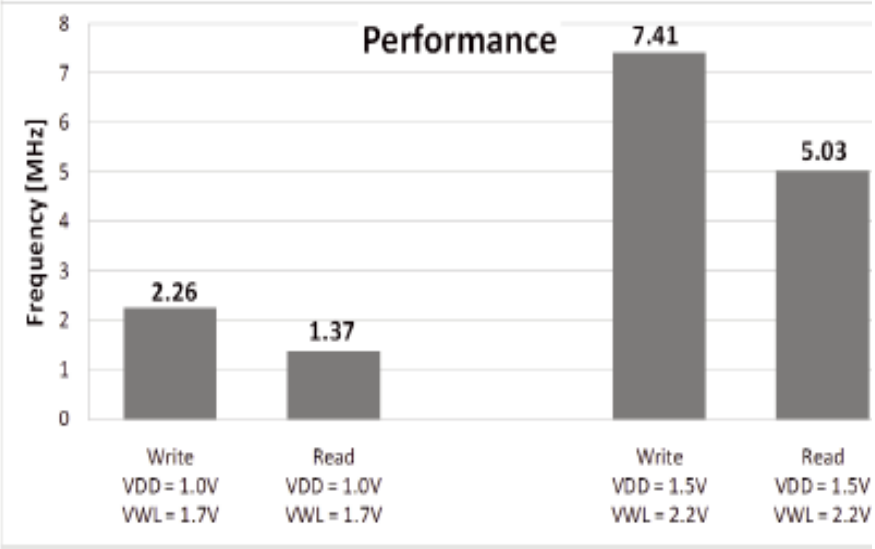


M. Qazi, et al, TI, MIT, ISSCC, Feb. 2011

Session 11 - Emerging Non-Volatile Memory

FeRAM runs at 1V by Expanding the Operating Margin





M. Qazi, et al, TI, ISSCC, Feb. 2011

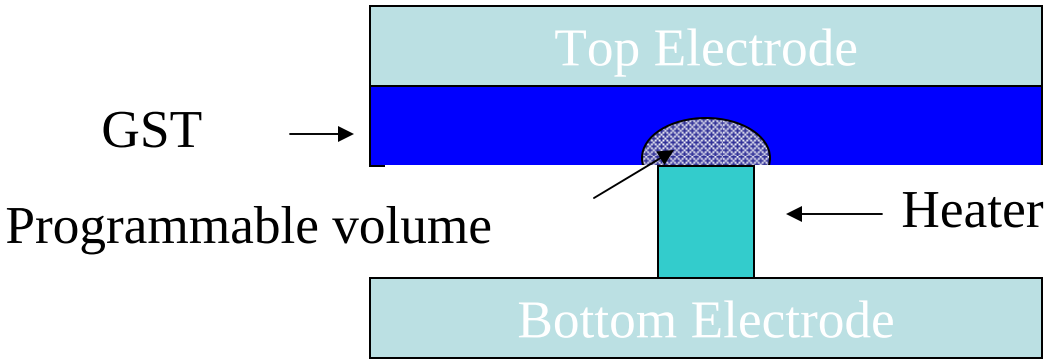
Session 11 - Emerging Non-Volatile Memory

Low Voltage FeRAM Features

High-Density 1T1C Design	
Organization	128k words of 8 bits
Technology	130nm LP CMOS
Array Efficiency	66.4%
Full Macro-level Density	0.936 Mb/mm^2
Operating Voltage (CORE / WL)	1.5V / 2.2V to 1.0V / 1.7V
Read Cycle Time	200ns to 730ns
Read Power	772uW to 107uW
Idle Power	251nW to 95nW
Standby Power	0W

M. Qazi, et al, TI, ISSCC, Feb. 2011

PC-RAM Cell
Schematic Cross-Section

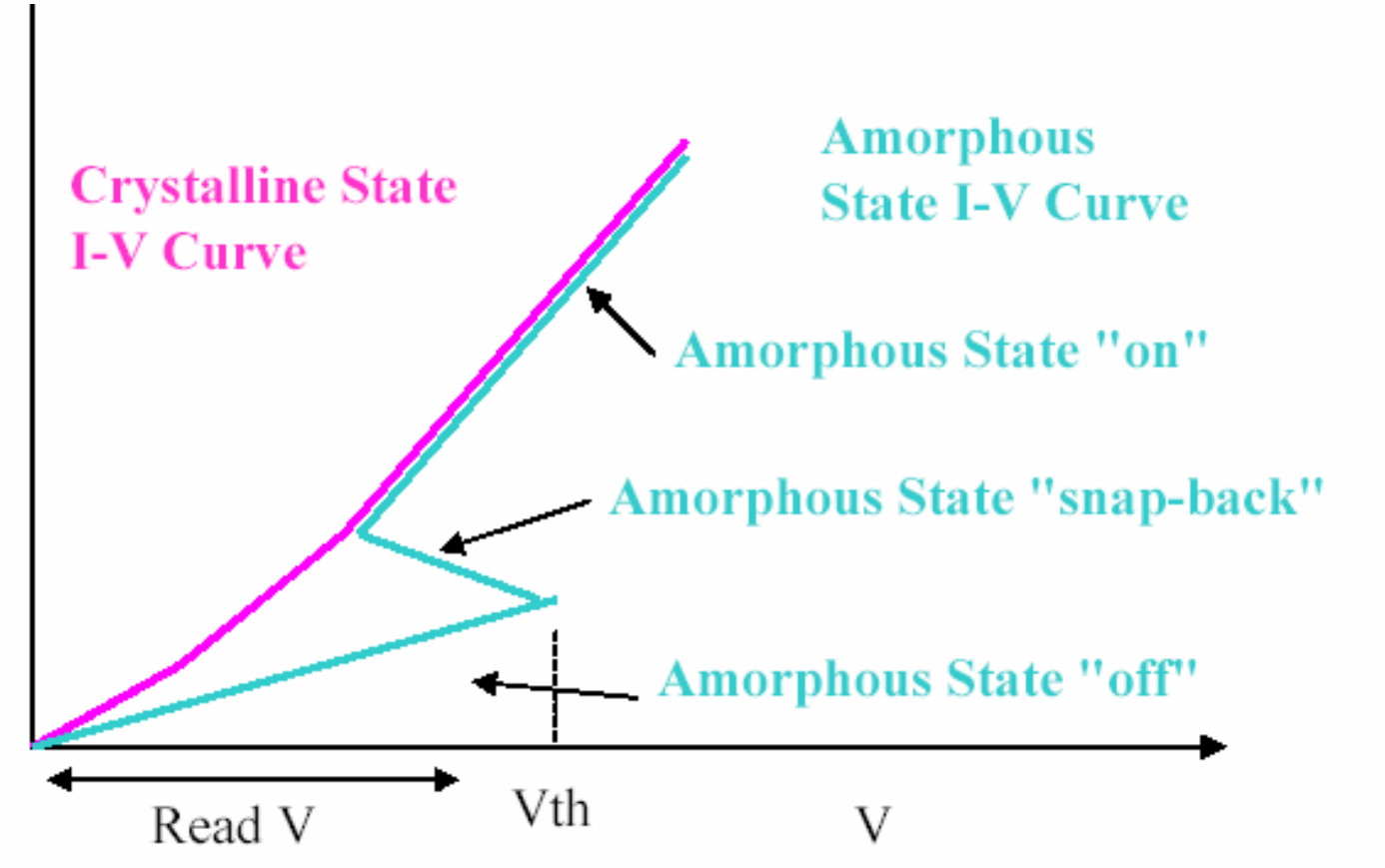


Data storage is by a thermally induced phase change between amorphous and polycrystalline states in a thin film chalcogenide alloy.

High Write current due to heating requirement

Ovonyx, Intel, ISSCC, 2002

Phase Change RAM Operation
(IV Characteristics)



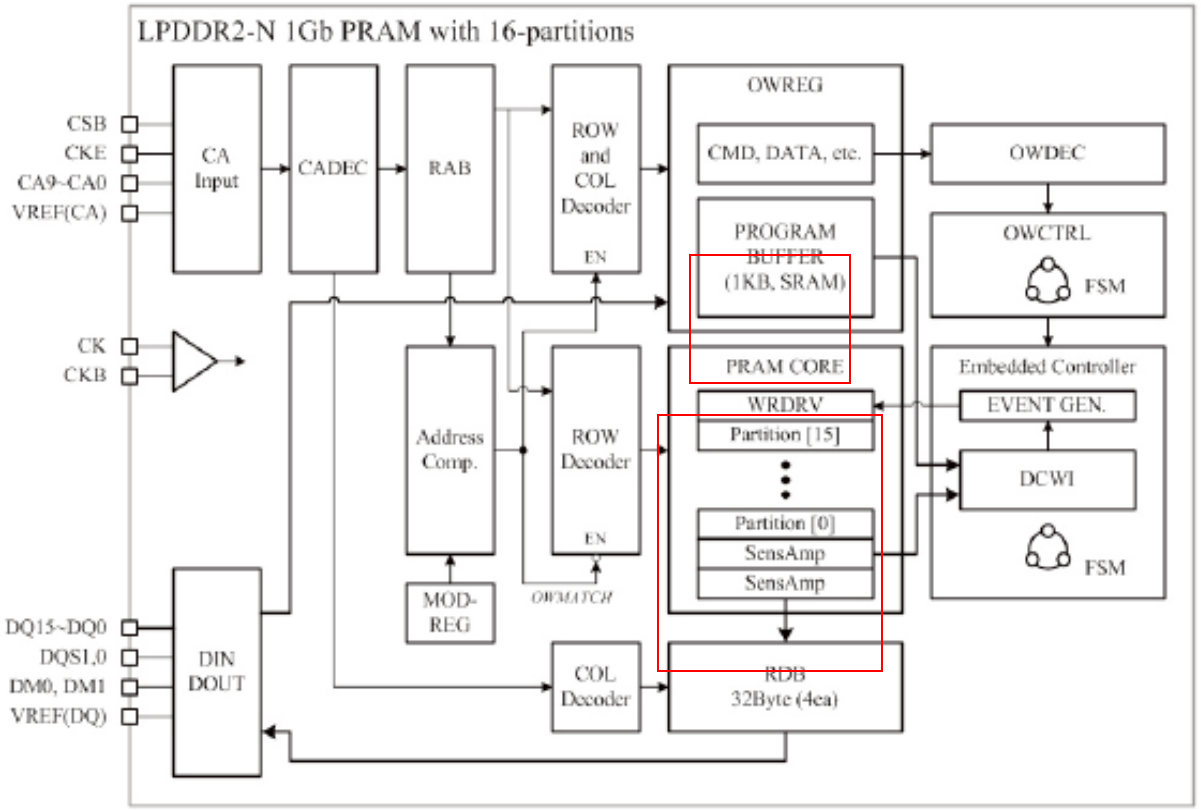
Macronix, 9/13/03

Session 28 – Fast Interface Memory:

PRAM with Fast Write (28.7)

58 nm 1.8V 1Gb PC-RAM with 6.4 MB/s DDR2-N Interface.
High performance, low power mobile replacement of flash

Plus SRAM 1KB 800 Mb/s program buffer controls program operation to handle the bandwidth difference.



H. Chung,et al, Samsung, ISSCC, Feb. 2011

Non-Volatile Memory Overview

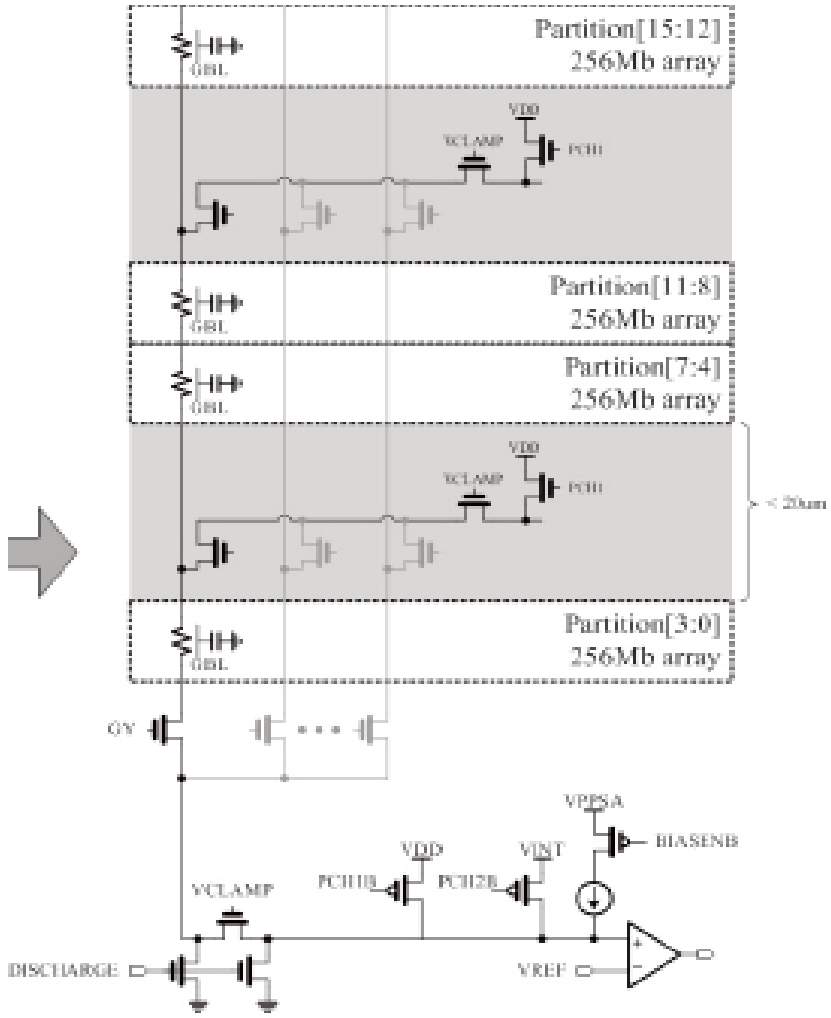
PRAM with Fast Write(29.7)

Mid-array precharge

is used for faster read.

The PRAM cell uses

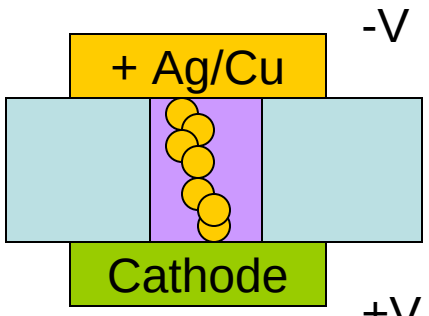
a diode switch.



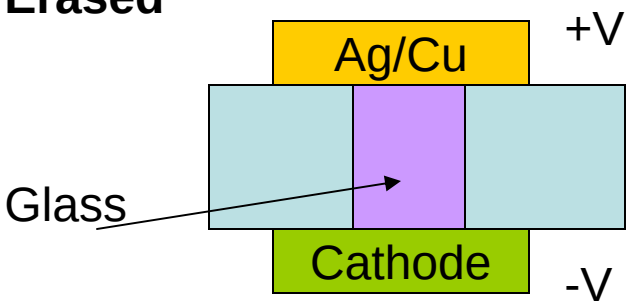
H. Chung,et al, Samsung, ISSCC, Feb. 2011

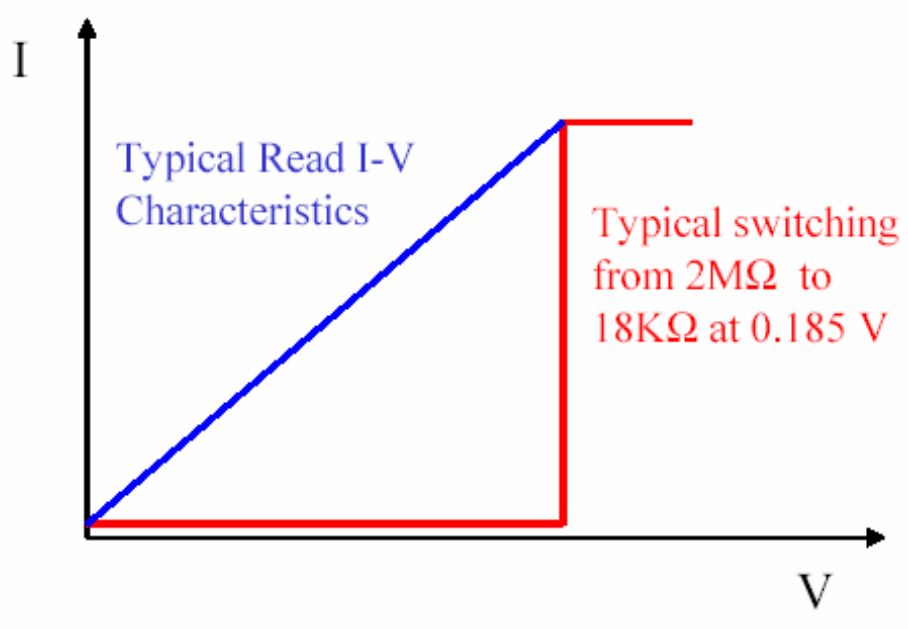
Conductive Bridge / PMC RAM

Programmed



Erased



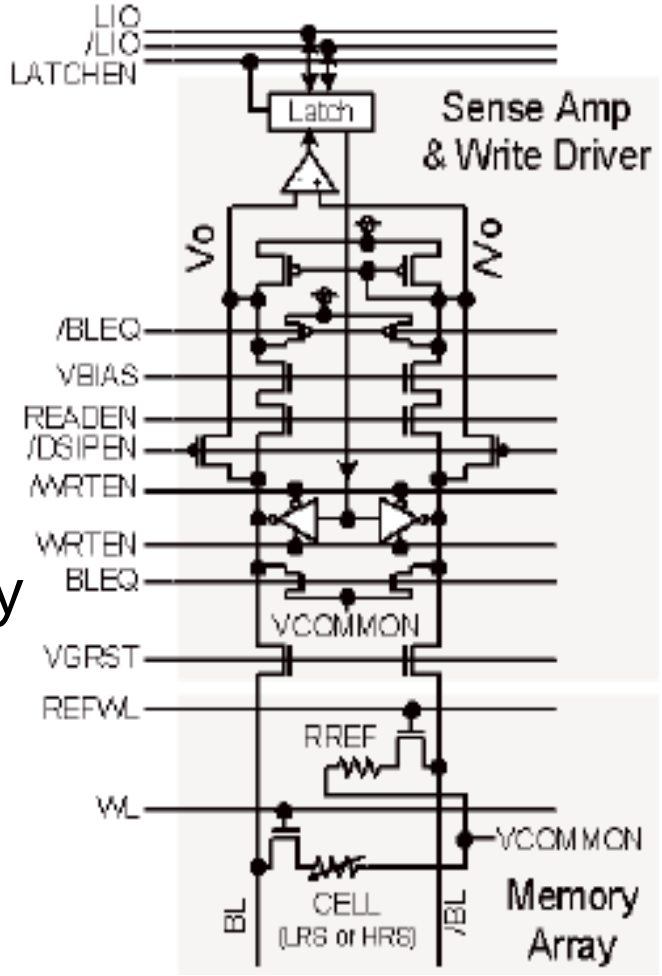


Resistance Switch Memory – Fits in a Via
Switched by Reversing Current (few uA)
Low Write Threshold Voltage
Copper or Silver Electrolyte

Axon Technology

Session 11 - Emerging Non-Volatile Memory: Conductive Bridge RAM (11.7) 4Mb in 180 nm CMOS

Programming operation uses direct sensing for 2.3 GB/s read, 216 MB/s Program, Folded BL cell array



Capacity	4 Mb
Tile	256Kb
Process	180nm CMOS
Chip size	6.8x5.26mm 35.8 mm^2
Cell architecture	1T-1R
Cell size	2.24 μm^2
Power Supply	3.3 V,1.8 V
Memory / IF clock	125MHz
Read Size, Throughput	128Byte 2.3GB/s
Program Size, Throughput	16Byte 216MB/s

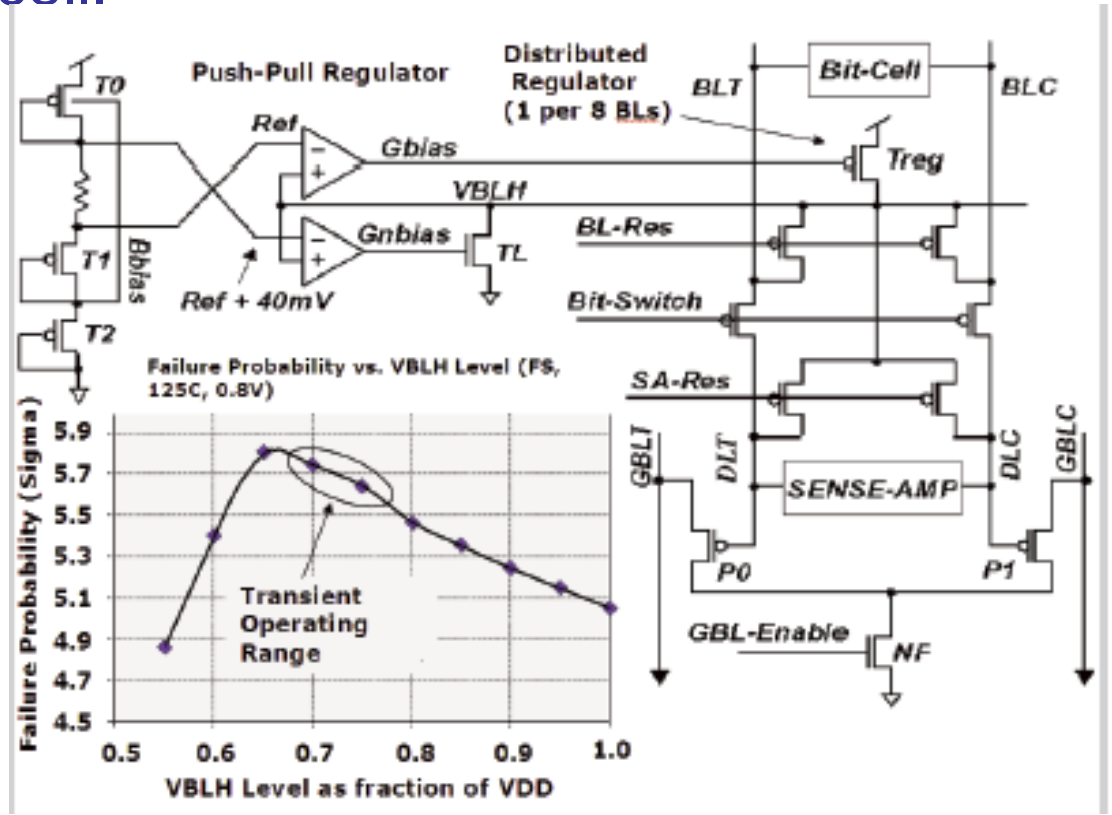
W. Oksuka, Sony, ISSCC, Feb. 2011

Session 14: High Performance eSRAM

64 Mb SRAM with Peripheral Assist Circuits (14.2)

IBM describes a peripheral circuit assist to enable 0.7 V operation for a 32 nm high-k metal gate SOI CMOS SRAM with a 0.154 um2 bit cell.

This BL regulation system does not degrade write margin. BL are precharged to a reduced level (VBLH).



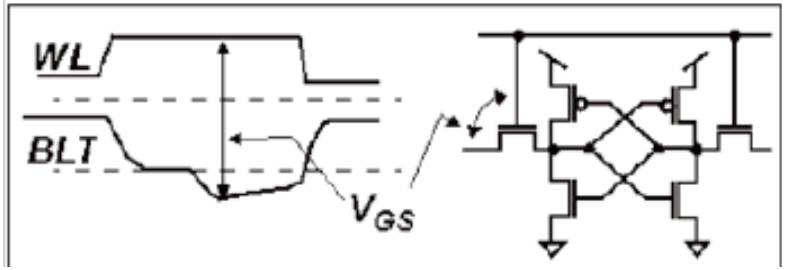
H. Pilo, IBM, ISSCC, Feb. 2011

Session 14: High Performance eSRAM

64 Mb SRAM with Peripheral Assist Circuits (14.2)

An improved write margin is achieved using a negative bitline technique with a higher boost voltage. A bit-cell-tracking delay monitor circuit improves process related performance and yield.

Write Driver with Boost Control



The read stability margin is enhanced by using a regulation scheme to reduce the bitline precharge voltage level. This limits the charge injection into the cell.

H. Pilo, IBM, ISSCC, Feb. 2011

Session 14: High Performance eSRAM

64Mb 32 nm SOI- SRAM for L3 Cache (AMD/IBM)(14.3)

8-MB Level 3 cache in 32 nm SOI CMOS that operates above 2.4 GHz at 1.1 V.

Area efficiency is improved by using a column select aliasing technique in which column select wires are shared between odd and even pairs for reads and writes.

Leakage power is minimized by doing supply gating and using floating bitlines.

The redundancy scheme uses centralized redundancy blocks instead of storing the redundant data in the macro.

D. Weiss, AMD, ISSCC, 2011

Session 28: DRAM with High Speed I/O

7 Gb/s/pin GDDR5 Graphics DRAM (28-6)

Overview of GDDR5:
GDDR5 uses parallel single ended signalling to restrict pincount and be backward compatible.

This leads to poor signal & power integrity at >5Gb/s/p. Channel crosstalk is becoming a major barrier to further speed improvement. Solution of shielding the line or widening the spacing has been used but increases cost.

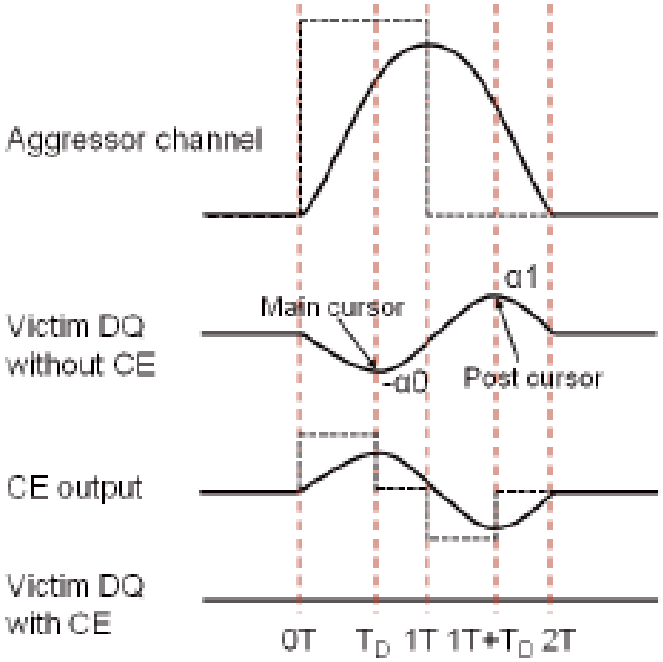
S.J. Bae, Samsung, ISSCC, Feb. 2011

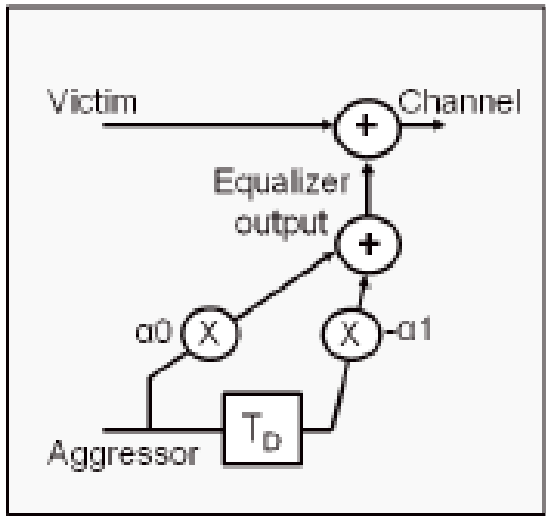
Session 28: DRAM with High Speed I/O

7 Gb/s/pin SDDR5 Graphics DRAM (28-6)

1.5 V, 2 Gb, 40 nm, for graphics cards and game consoles.

Chip uses a cross-talk equalizing filter for the transmitter which has: a programmable signal ordering capability,
data rate of 7 Gb/s/pin with 10% jitter reduction.





2-tap crosstalk equalizing filter

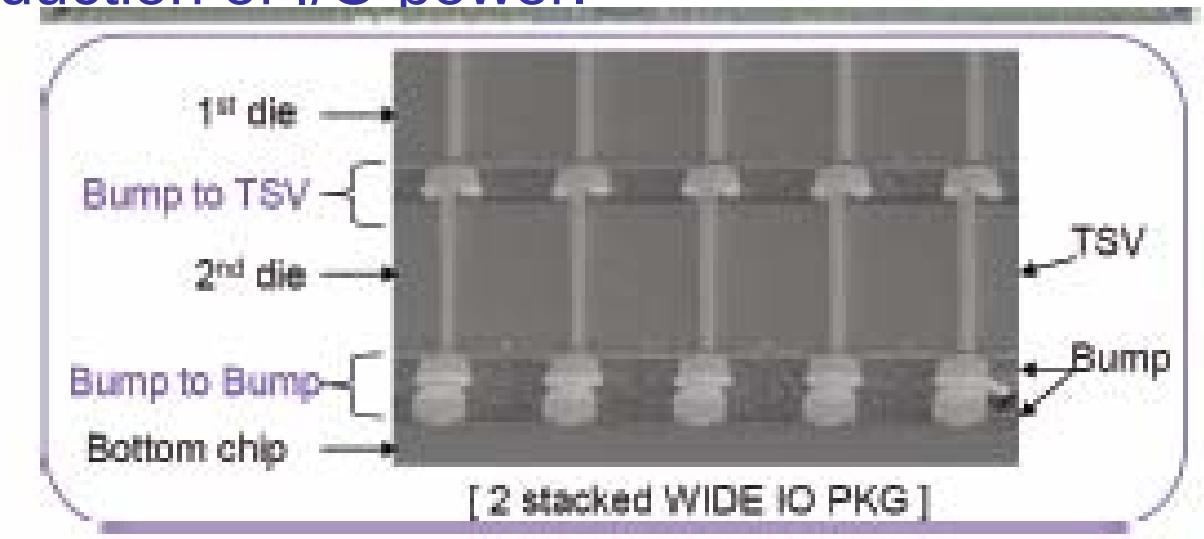
S.J. Bae, Samsung, ISSCC, Feb. 2011

Session 28: 3D DRAM with High Speed I/O

Stacked TSV 2 Gb 1.2V Mobile SDR SDRAM(28.5)

Stack:2 Gb 4x128 I/O = 512 DQ, 12.8 GB/s Data BW,
Chip: 1 Gb, 4 channels, 512 DQ pins, 12.8 GB/s DBW
Stacked using 7.5um via diameter TSV.

Compared with Conventional LP DDR2:
4 x higher data bandwidth, same standby power,
90% reduction of I/O power.



J.S.Kim, et al, Samsung, ISSCC, Feb. 2011