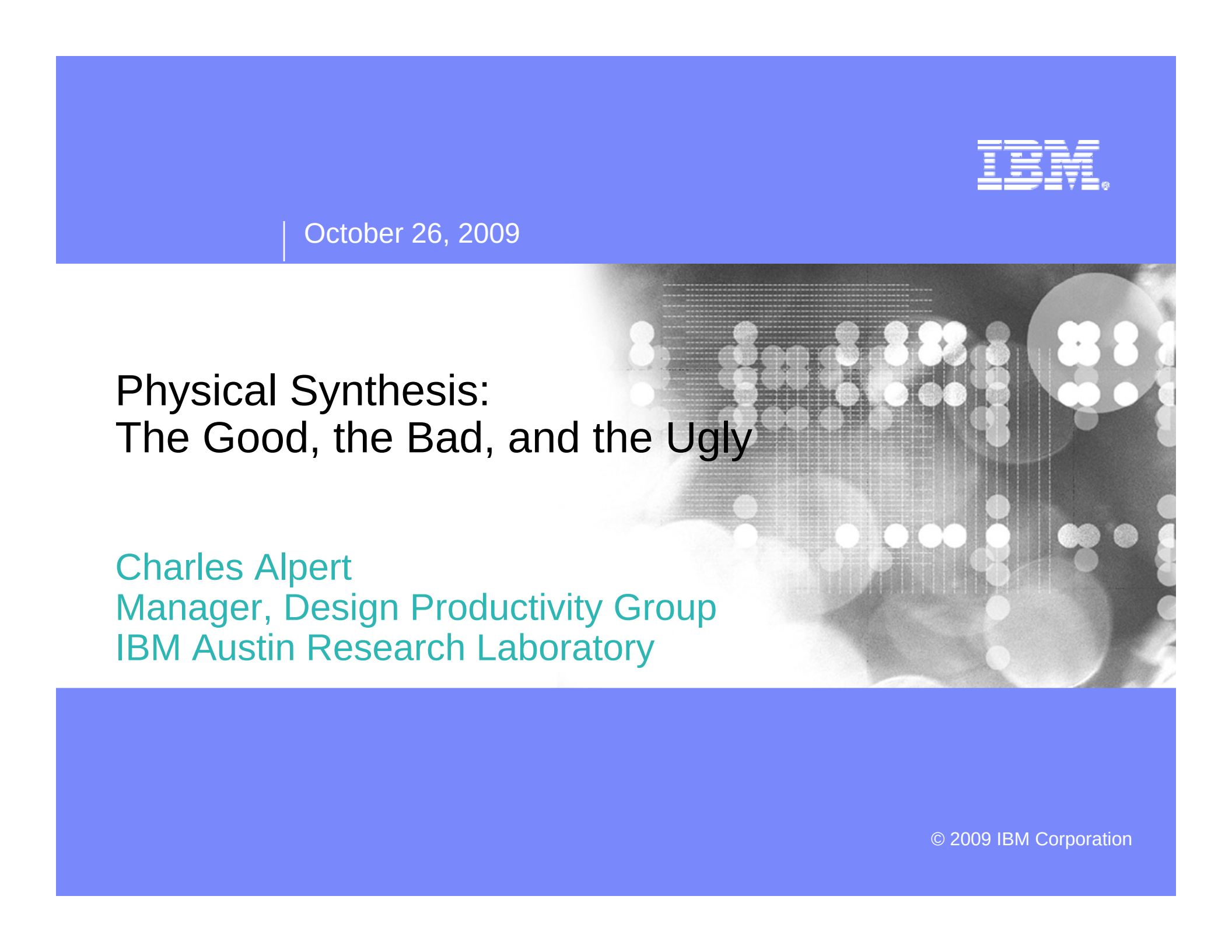
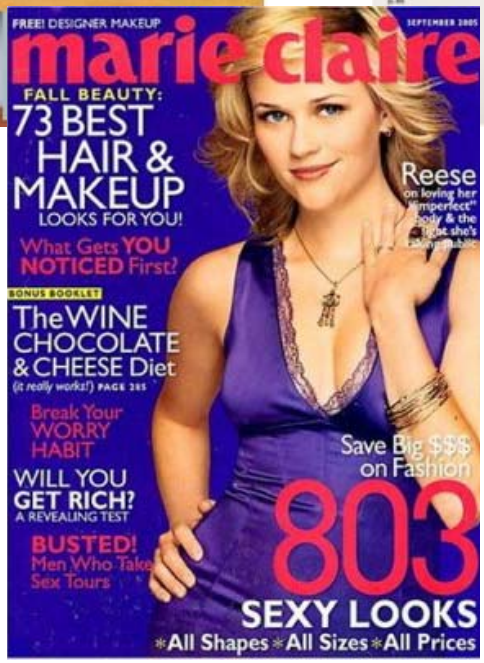


October 26, 2009

Physical Synthesis: The Good, the Bad, and the Ugly

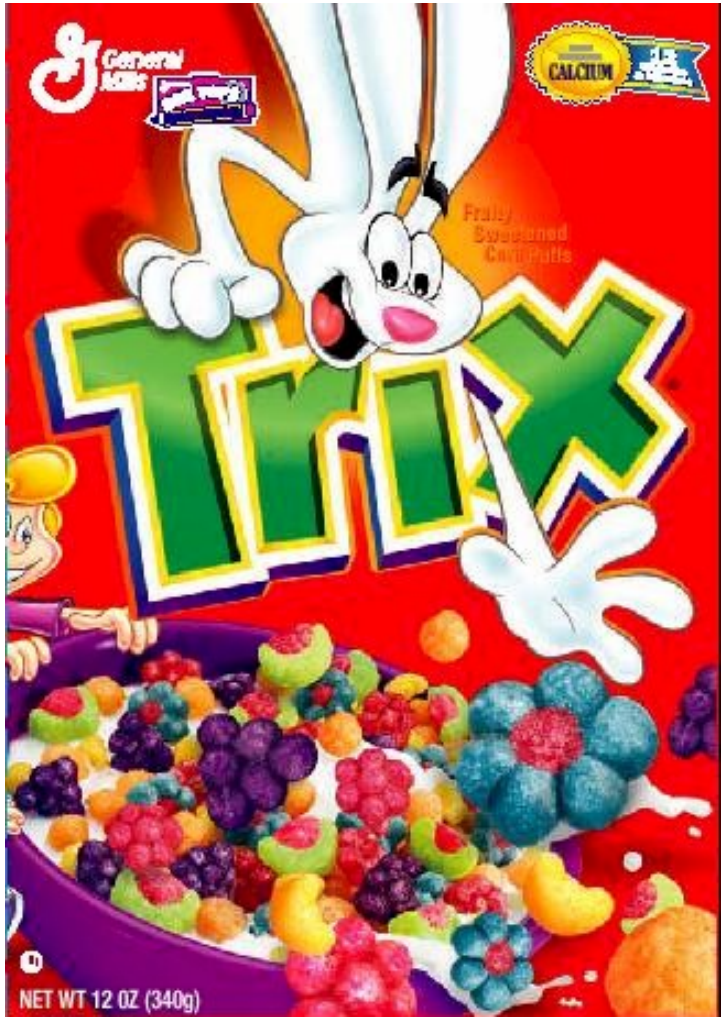
Charles Alpert
Manager, Design Productivity Group
IBM Austin Research Laboratory

The Nuisance Factor

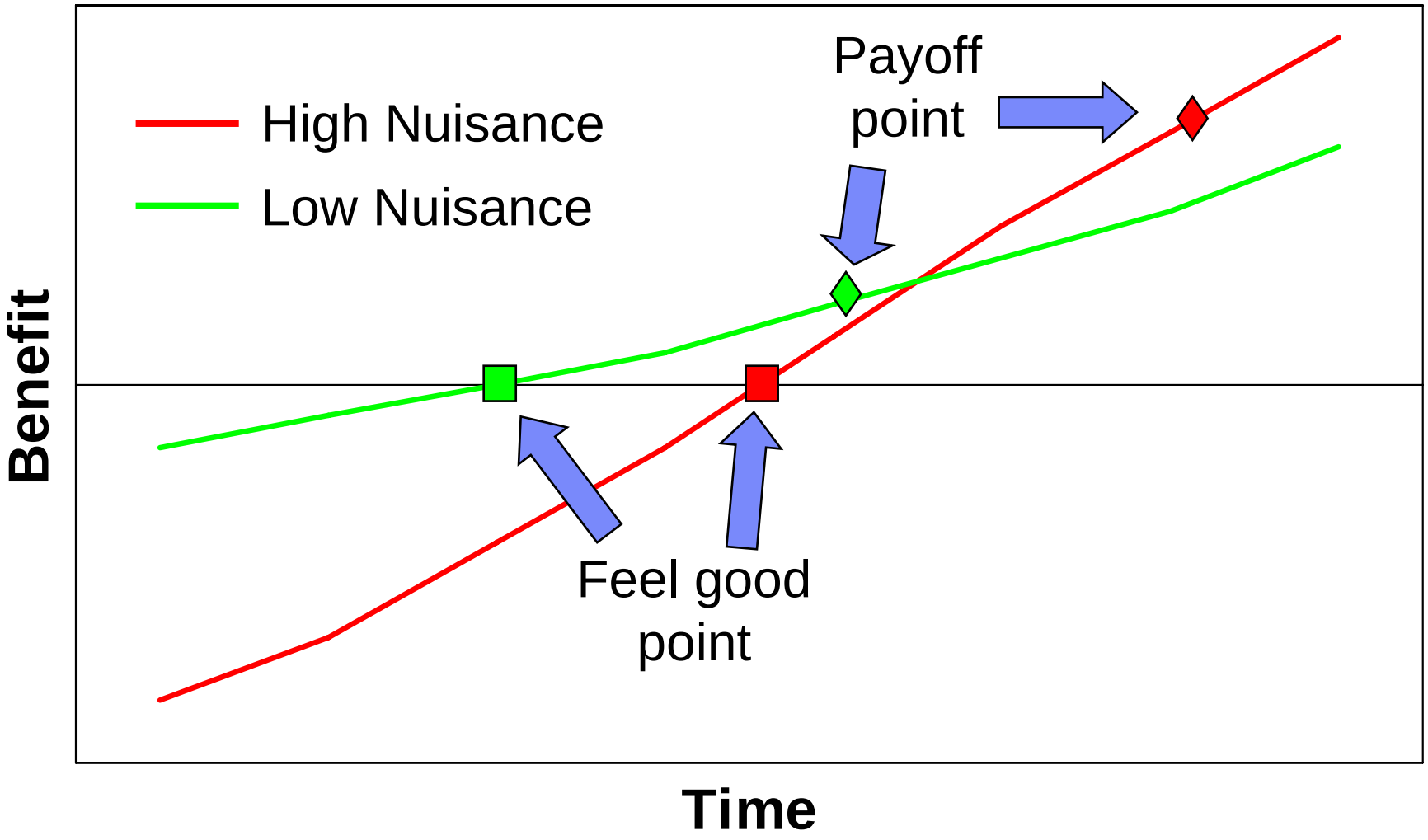


Decisions with High Nuisance Factors

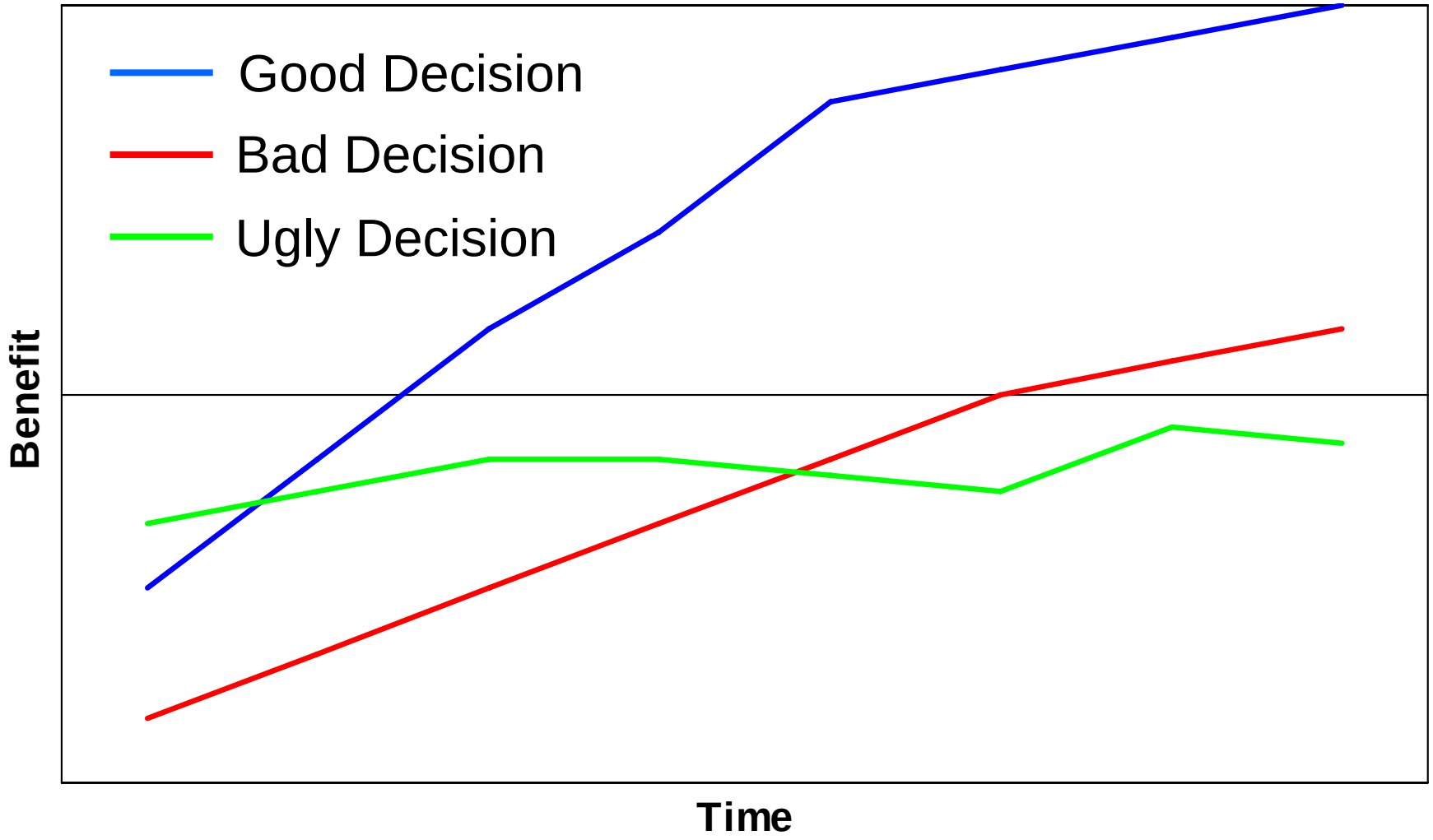
Low Nuisance Factors



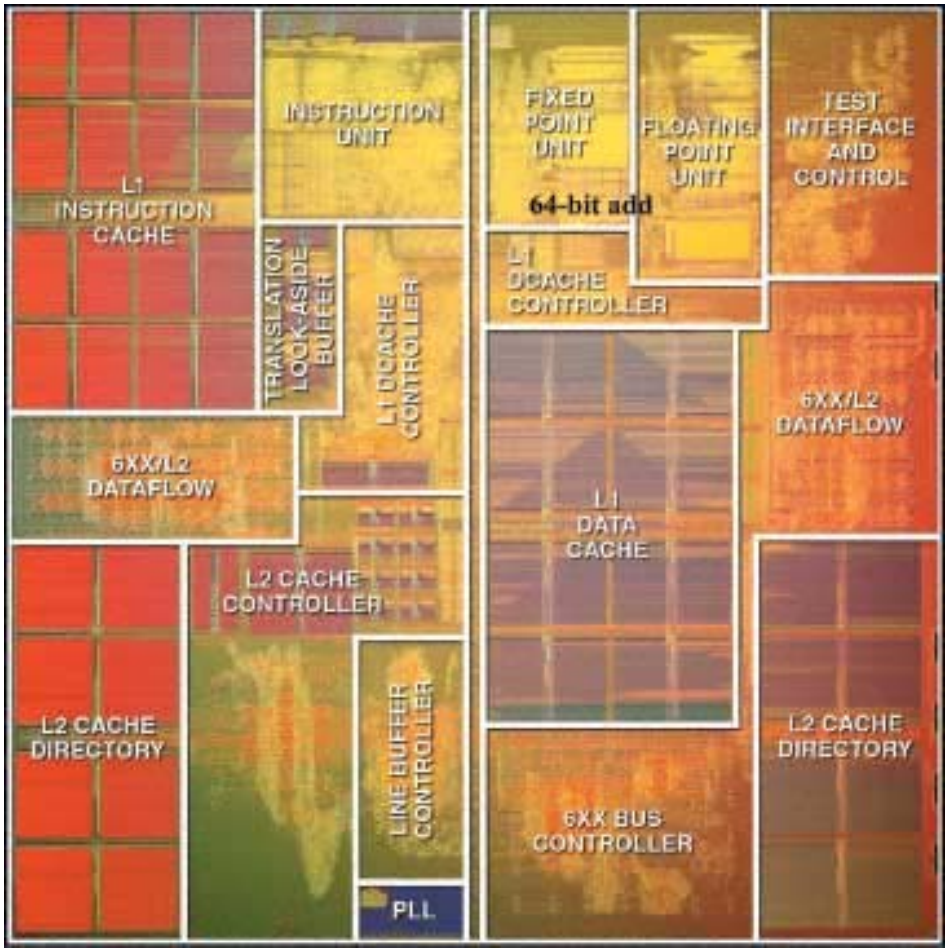
The Nuisance Curve of Decision Making

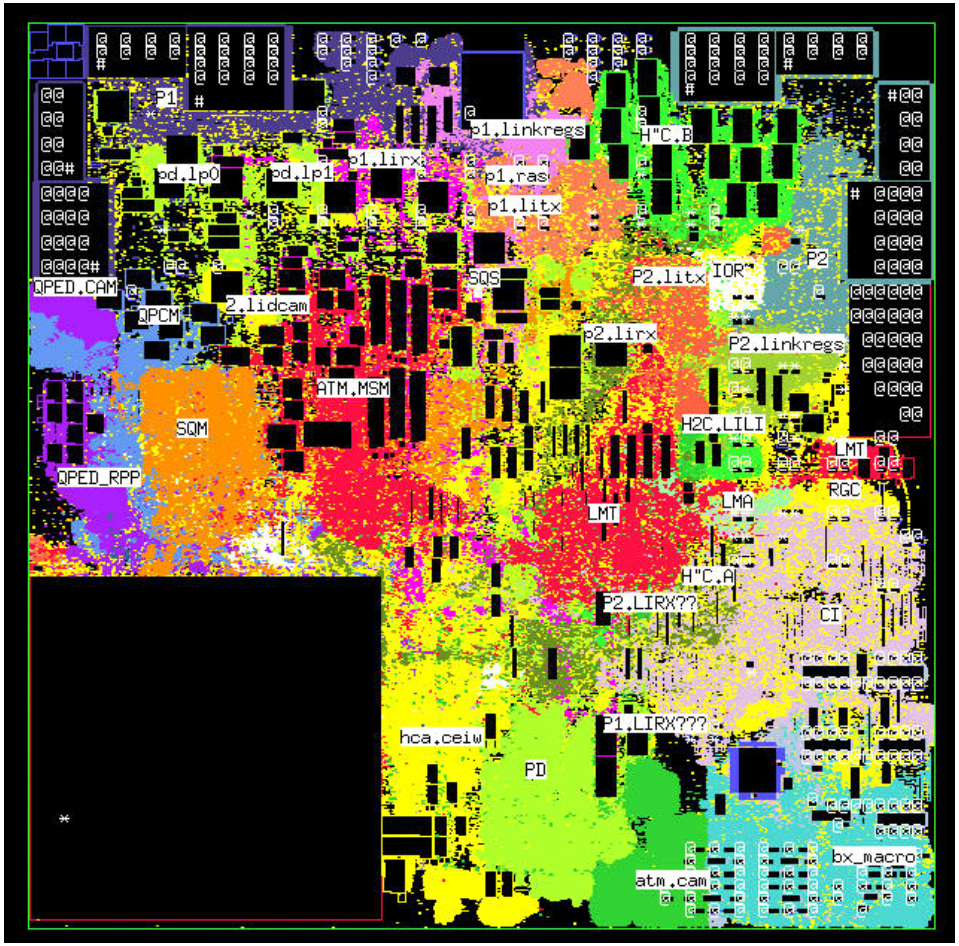


What about these Nuisance Curves?

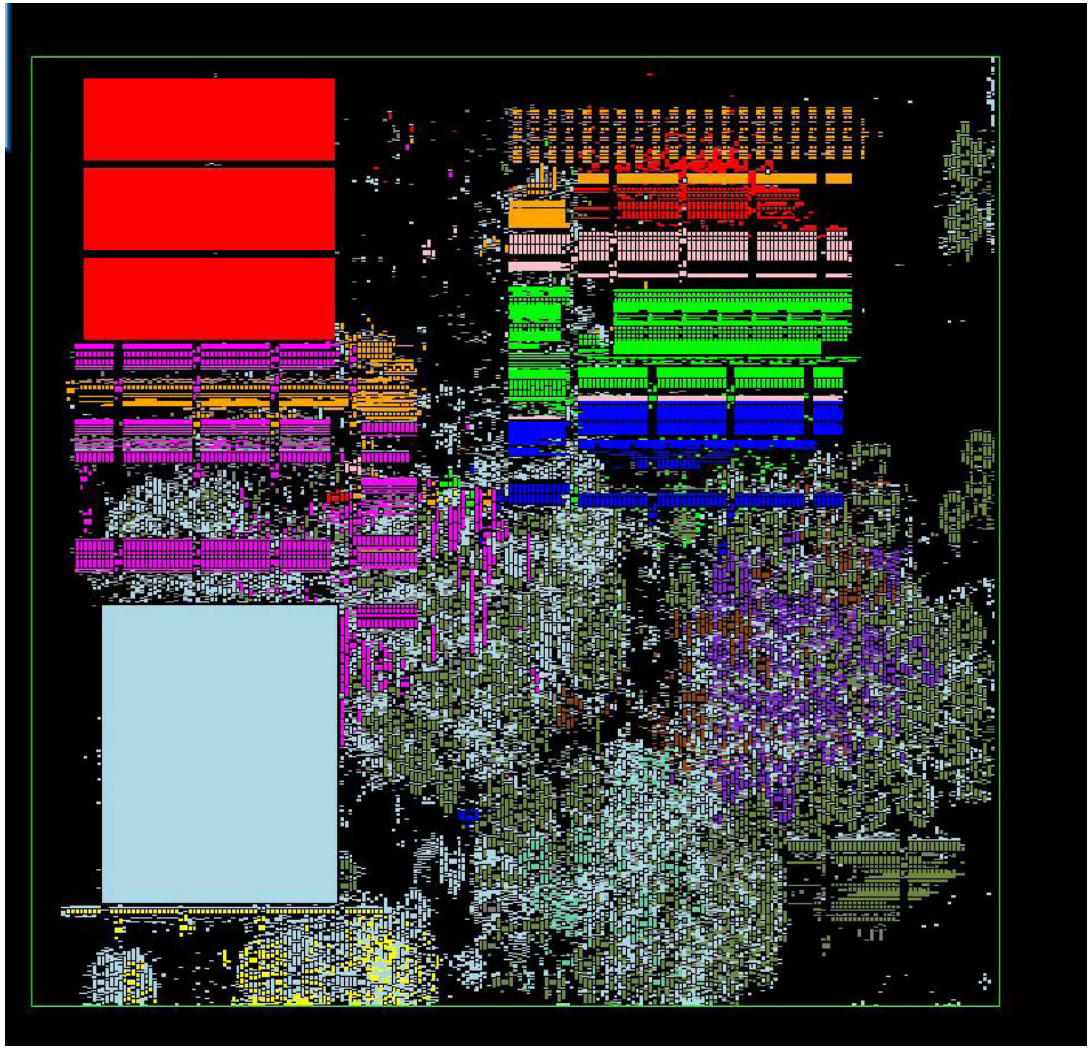


Why Do We Still Do Custom Design?

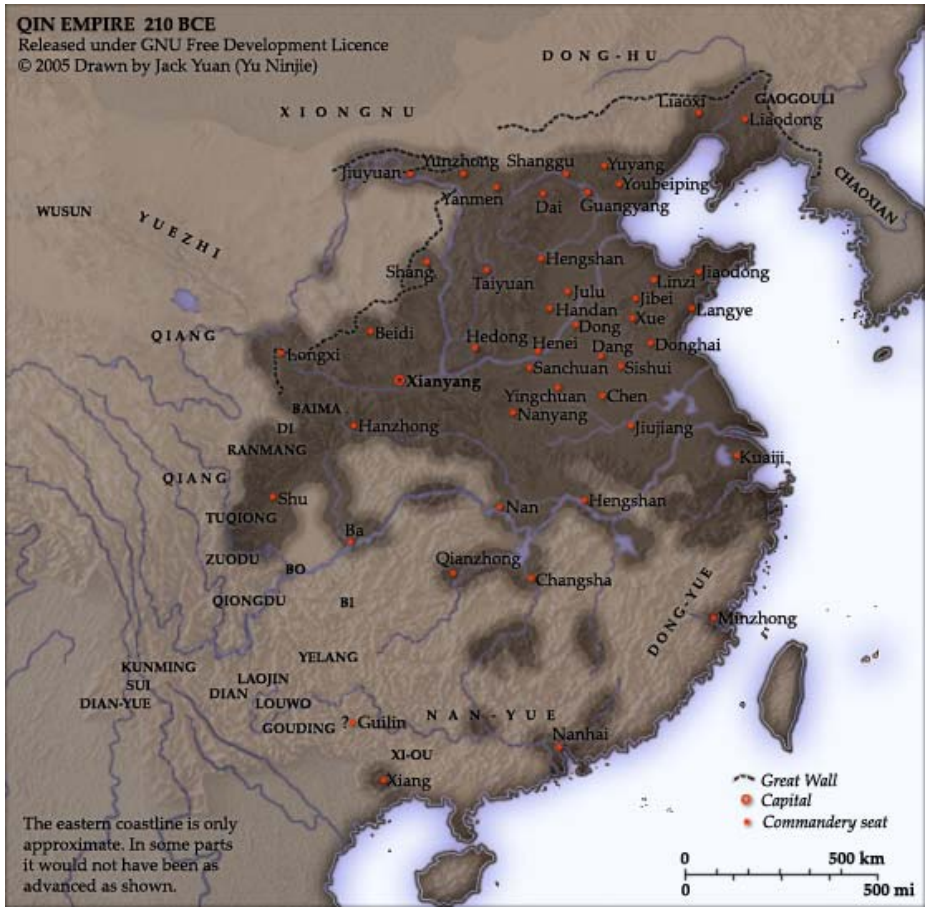




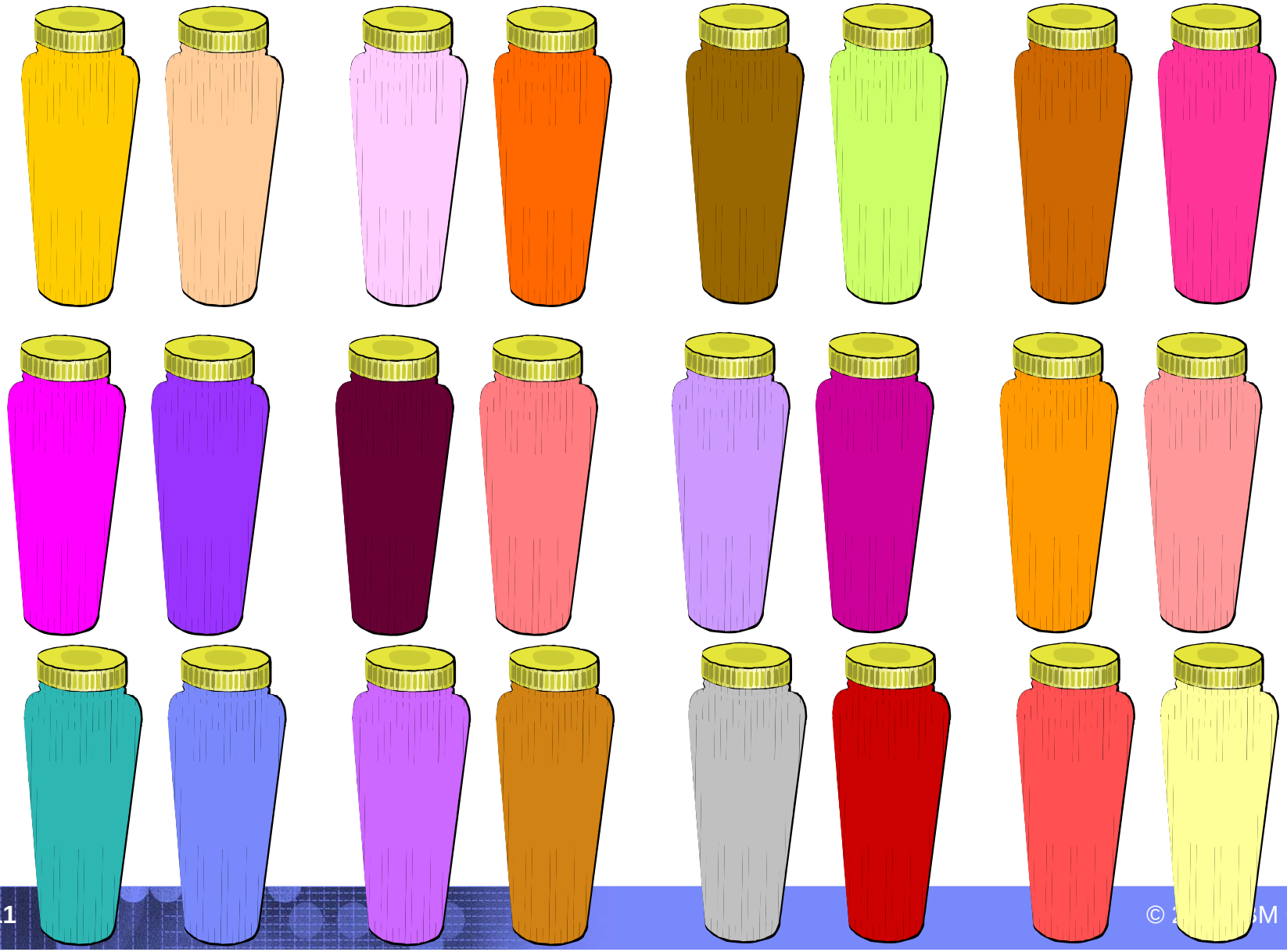
Perhaps a Compromise . . .



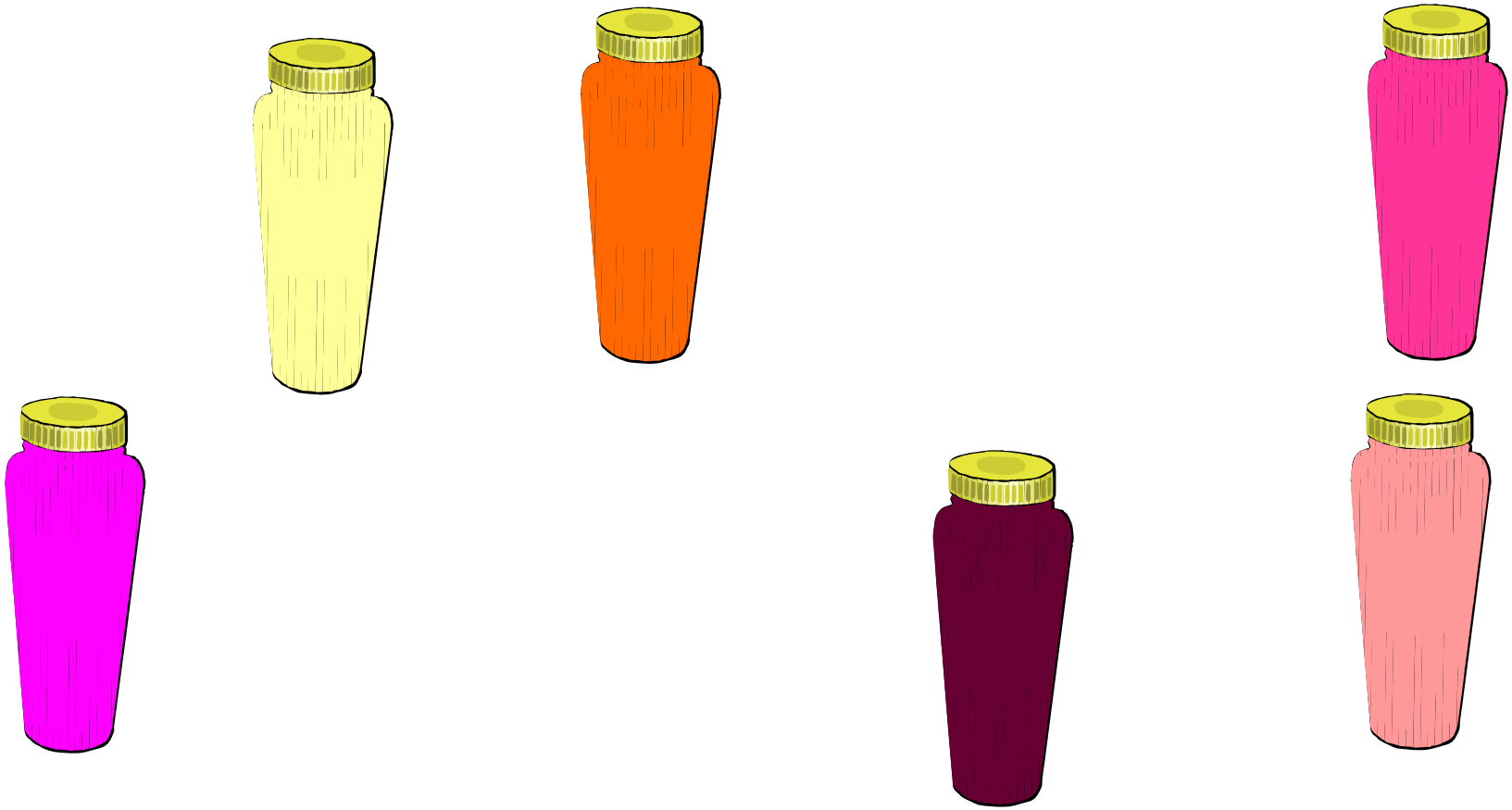
The Story of Xiang Yu



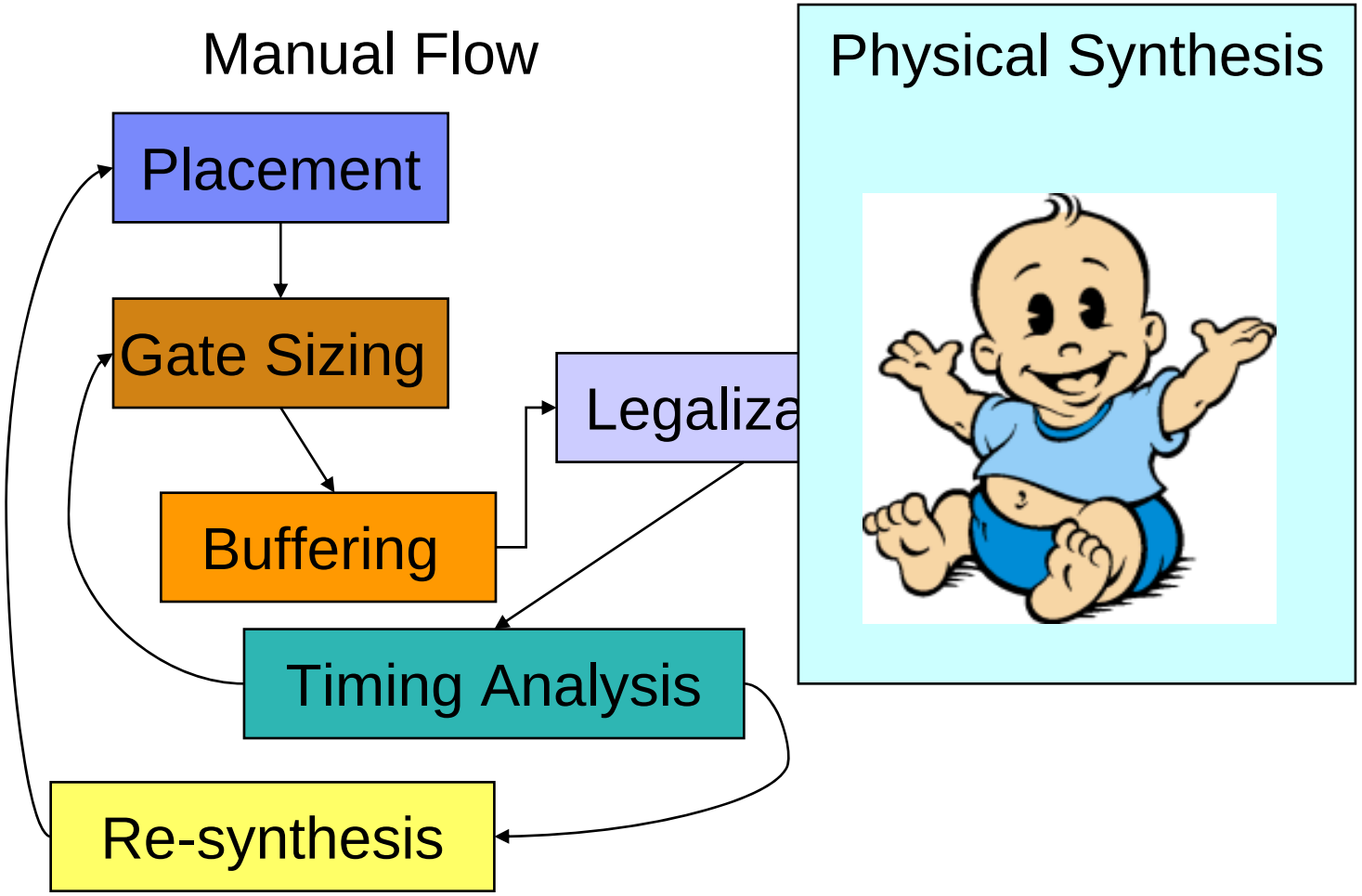
Too Many Choices Leads to Indecisiveness



Too Many Choices Leads to Indecisiveness

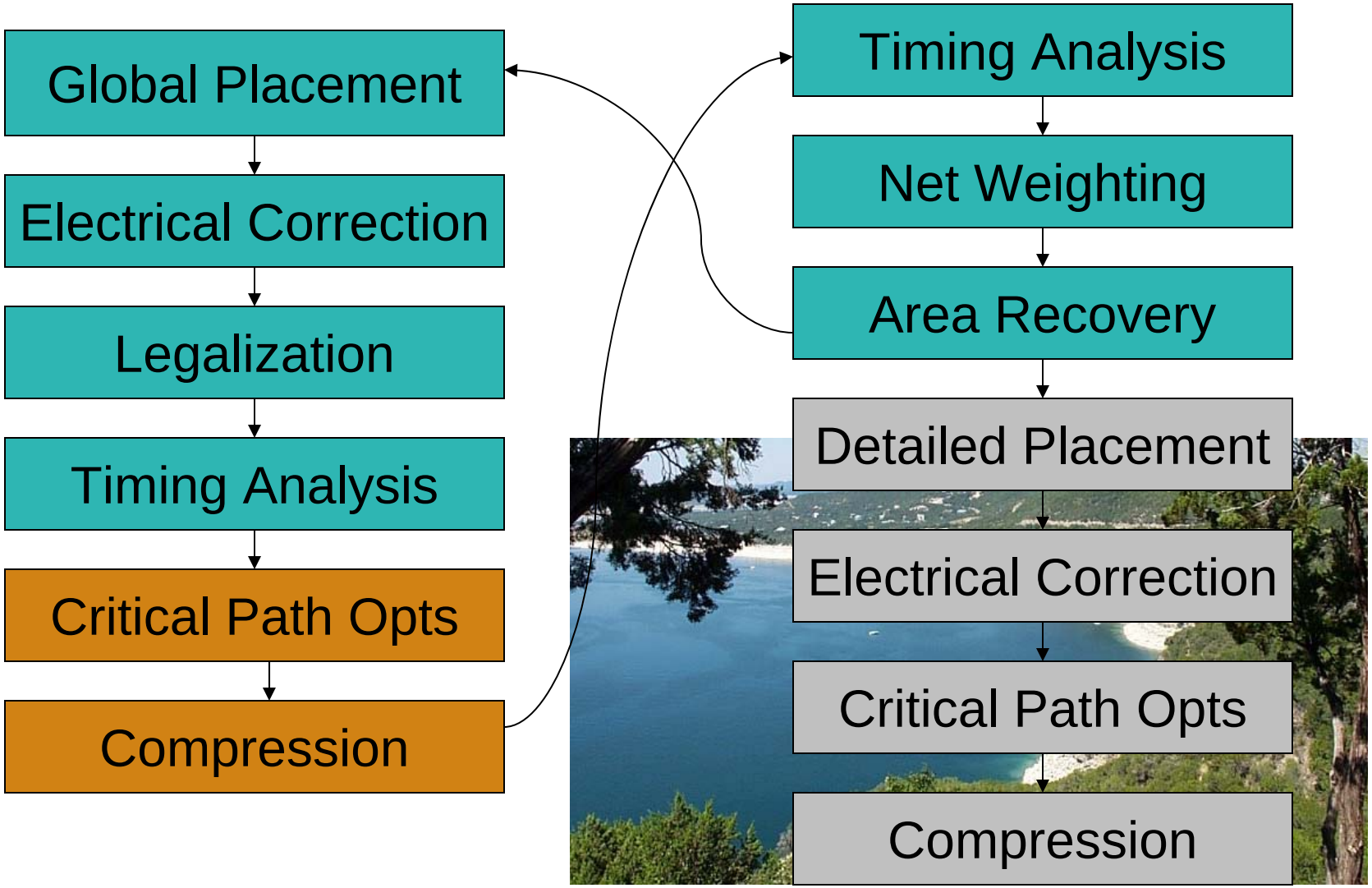


The Birth of Physical Synthesis

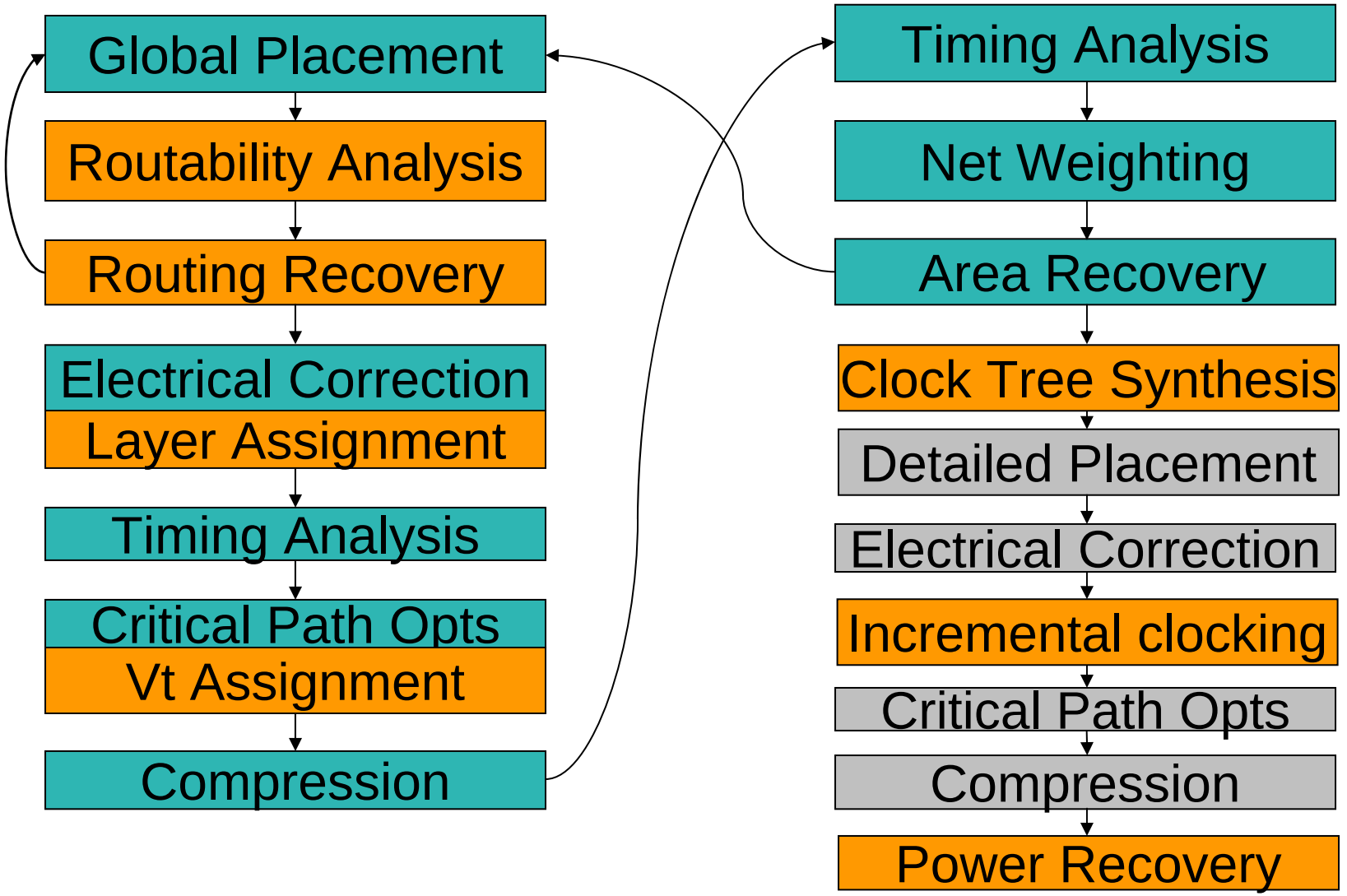


Constructive Versus Polishing

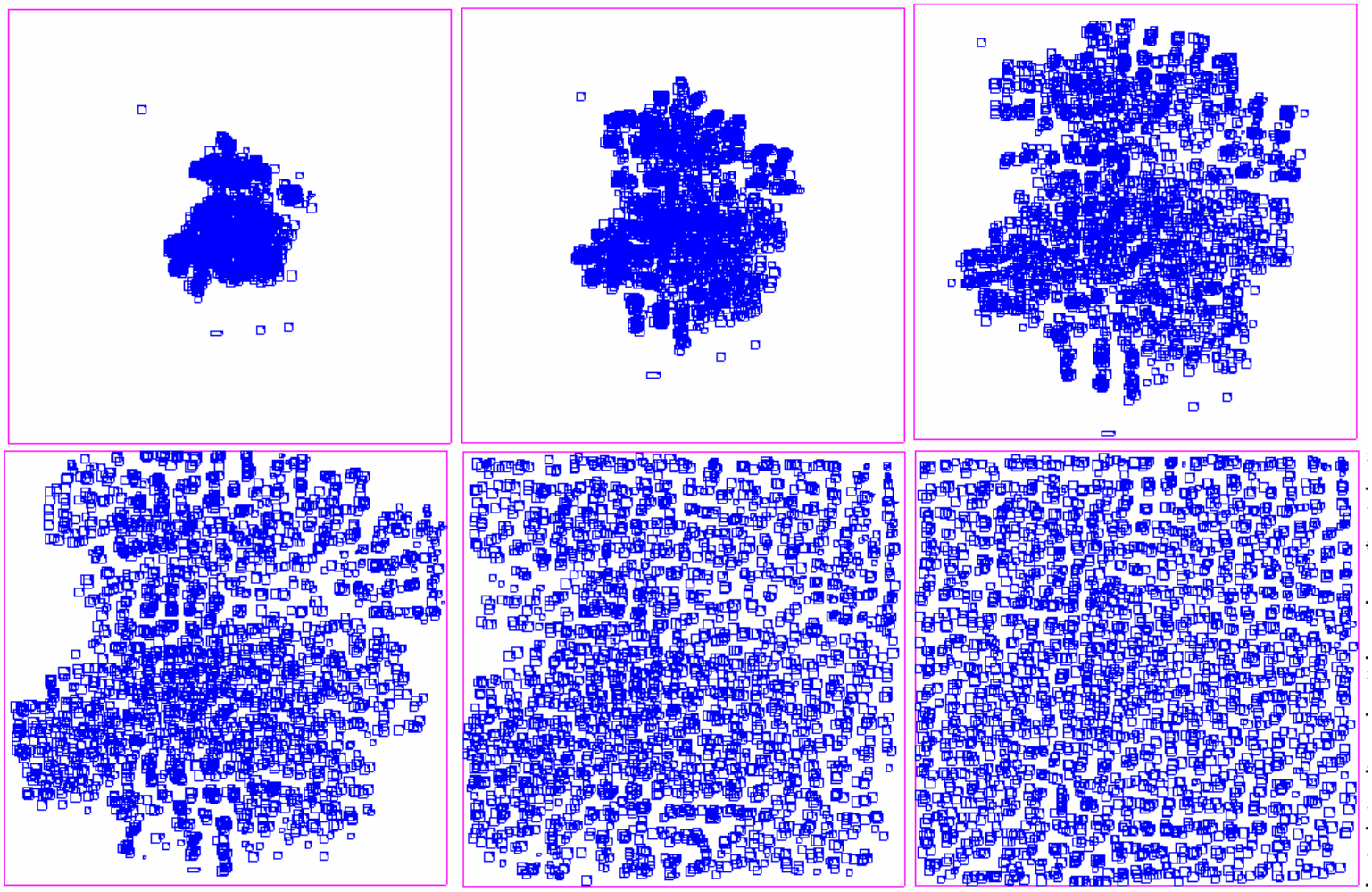
Example Physical Synthesis Flow

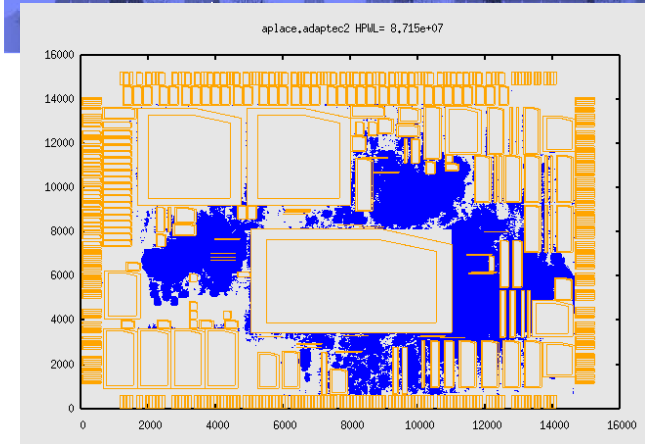


More Mature Physical Synthesis Flow



Good: Global Placement

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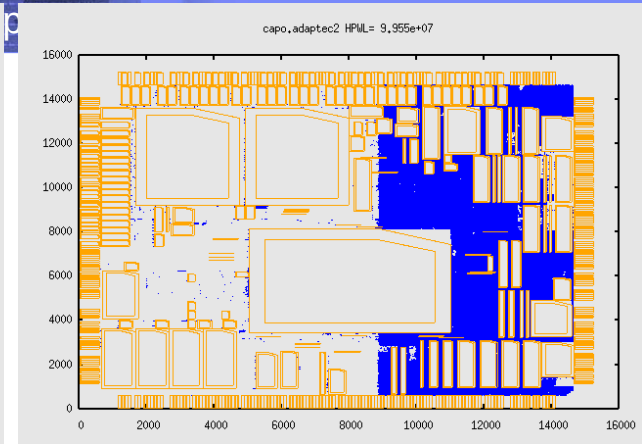
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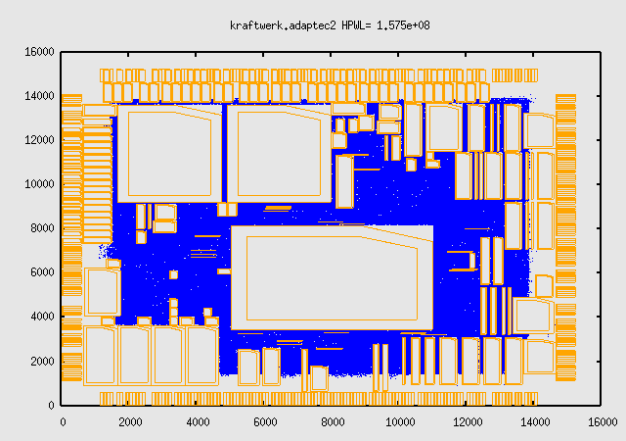
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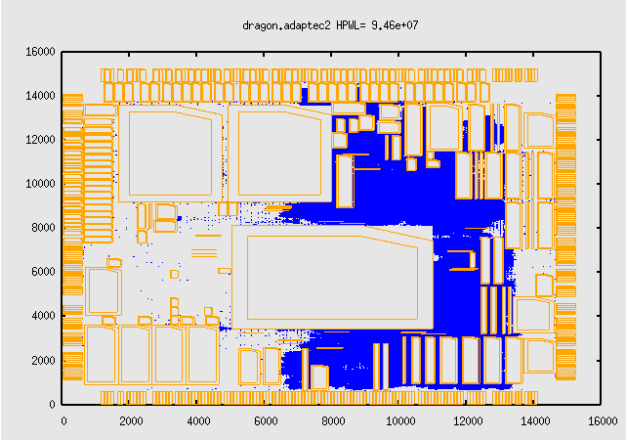
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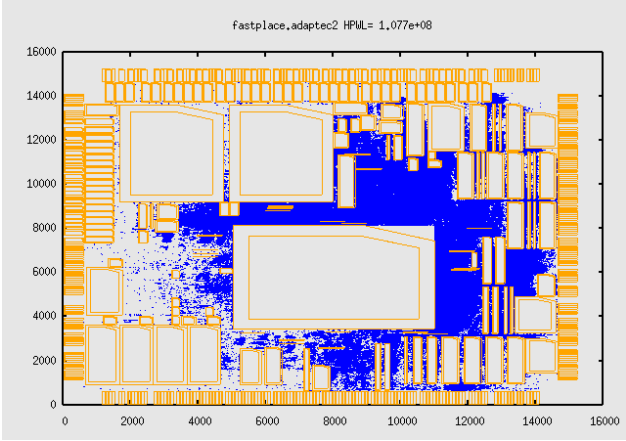
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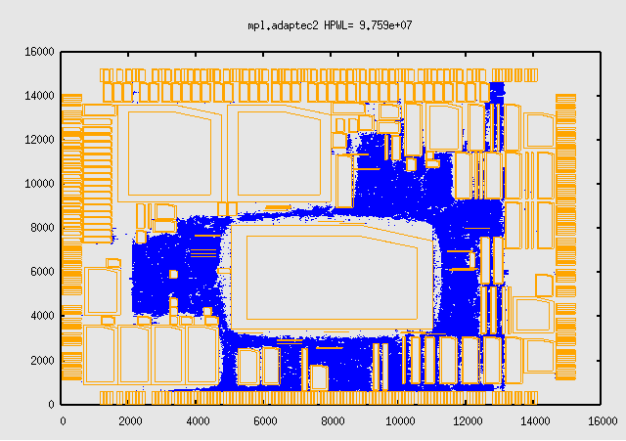
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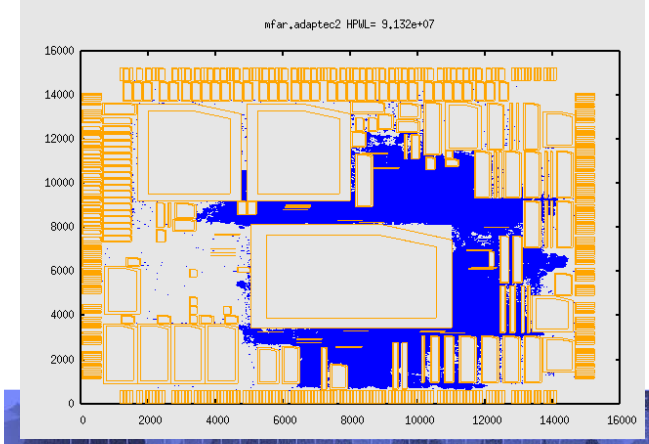
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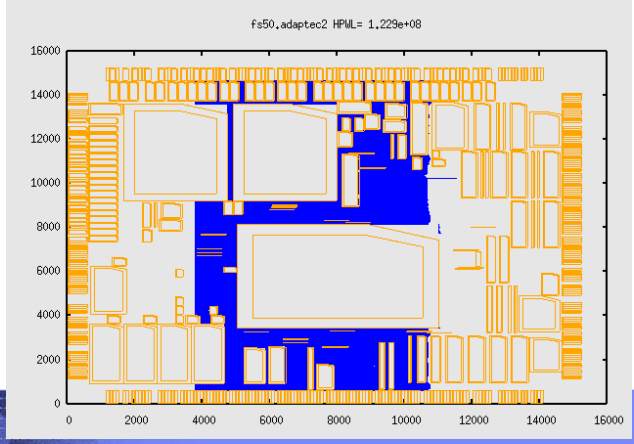
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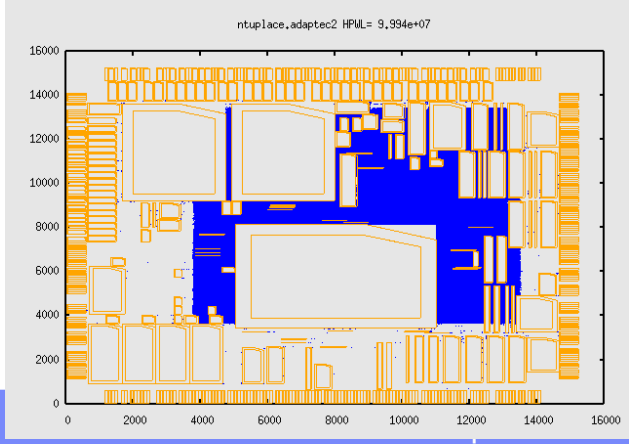
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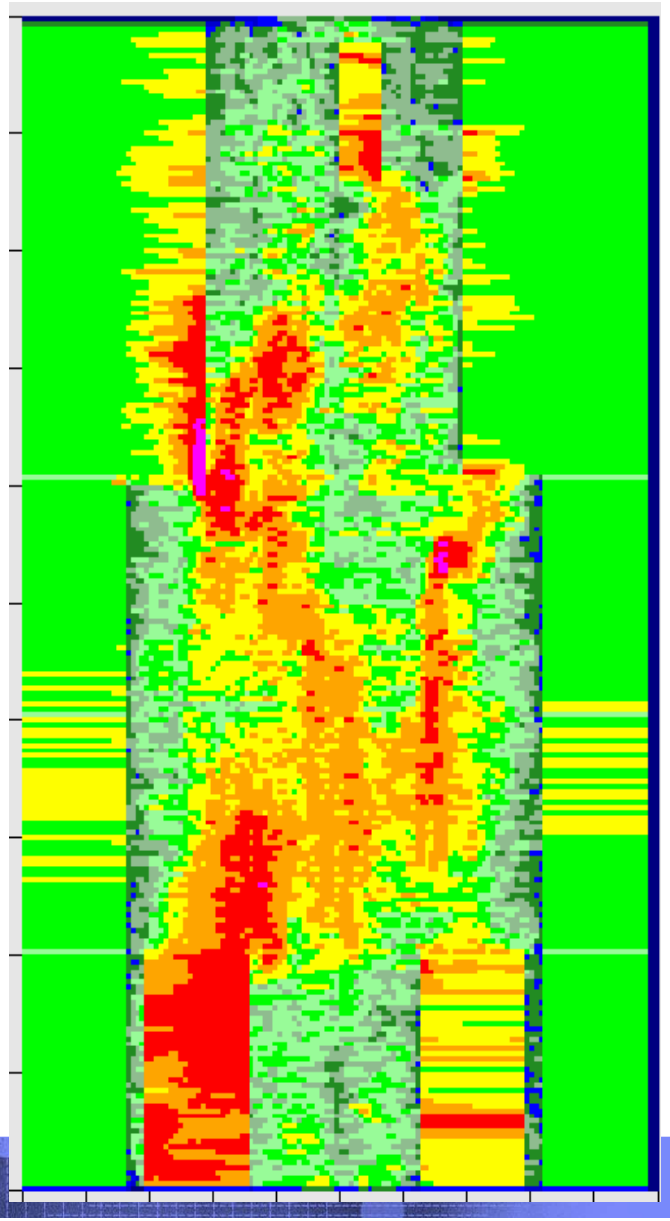
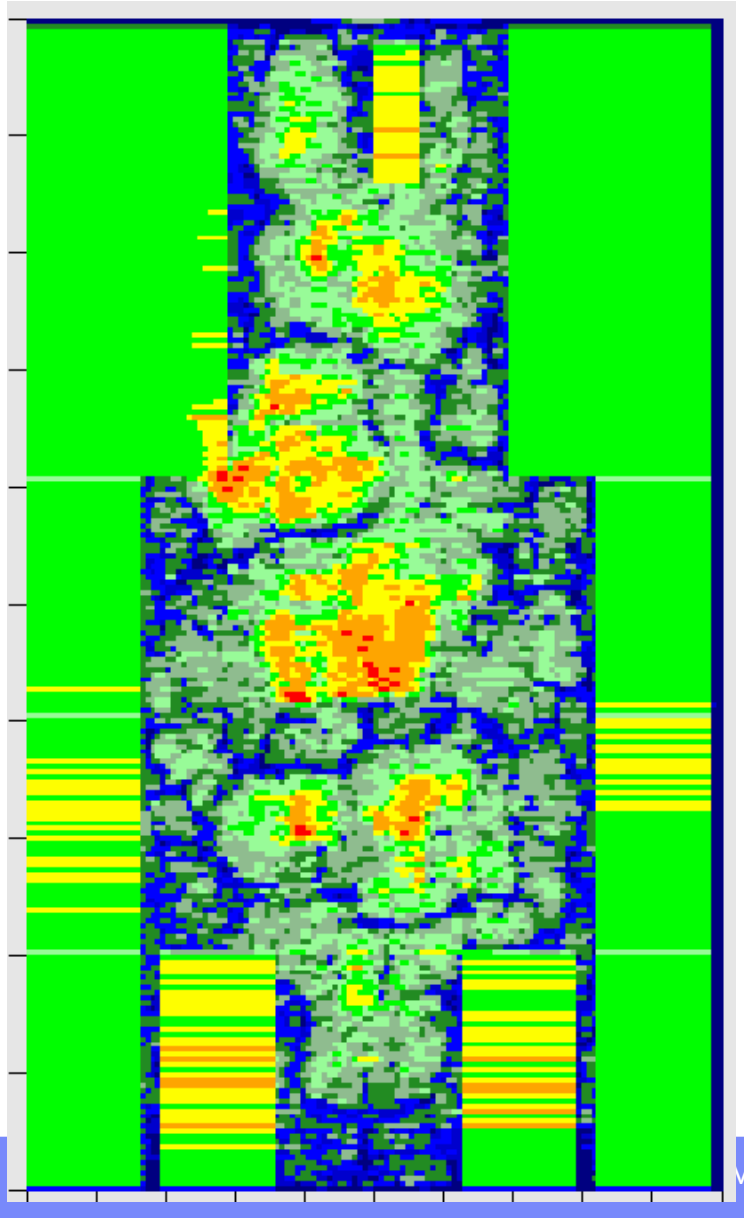
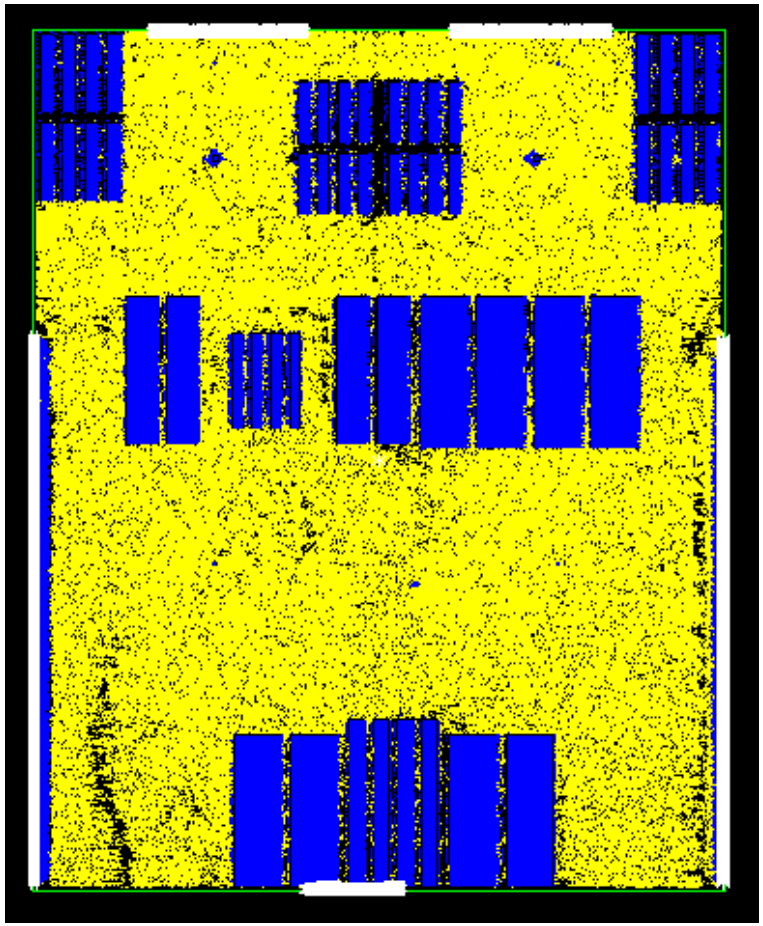
Potentially Big Congestion Reduction

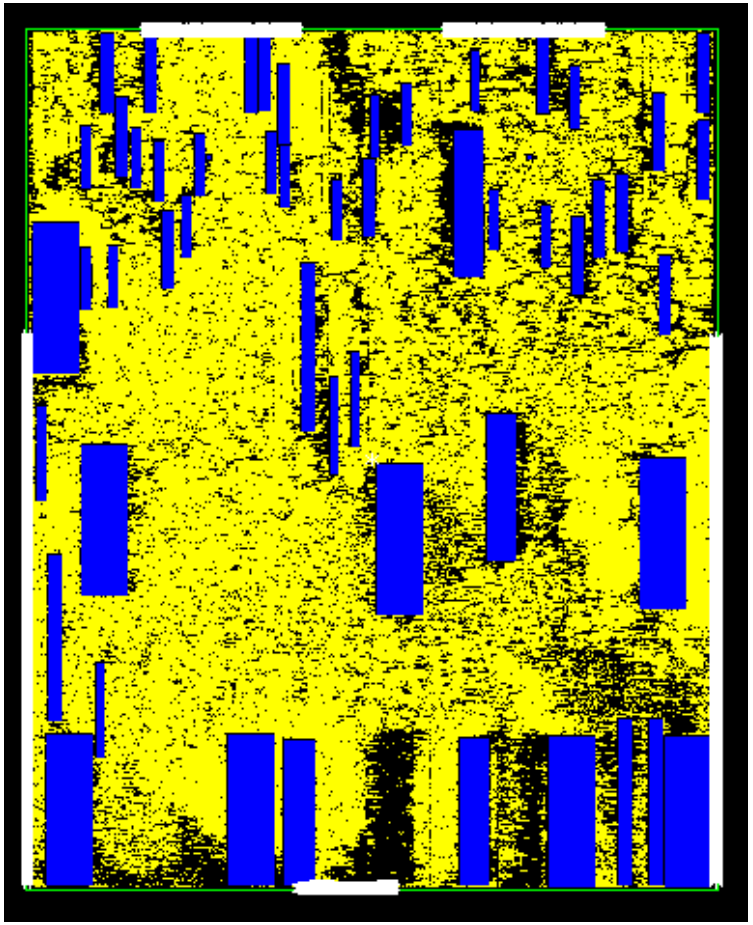




Big Block Placement: Good, Bad, Ugly?

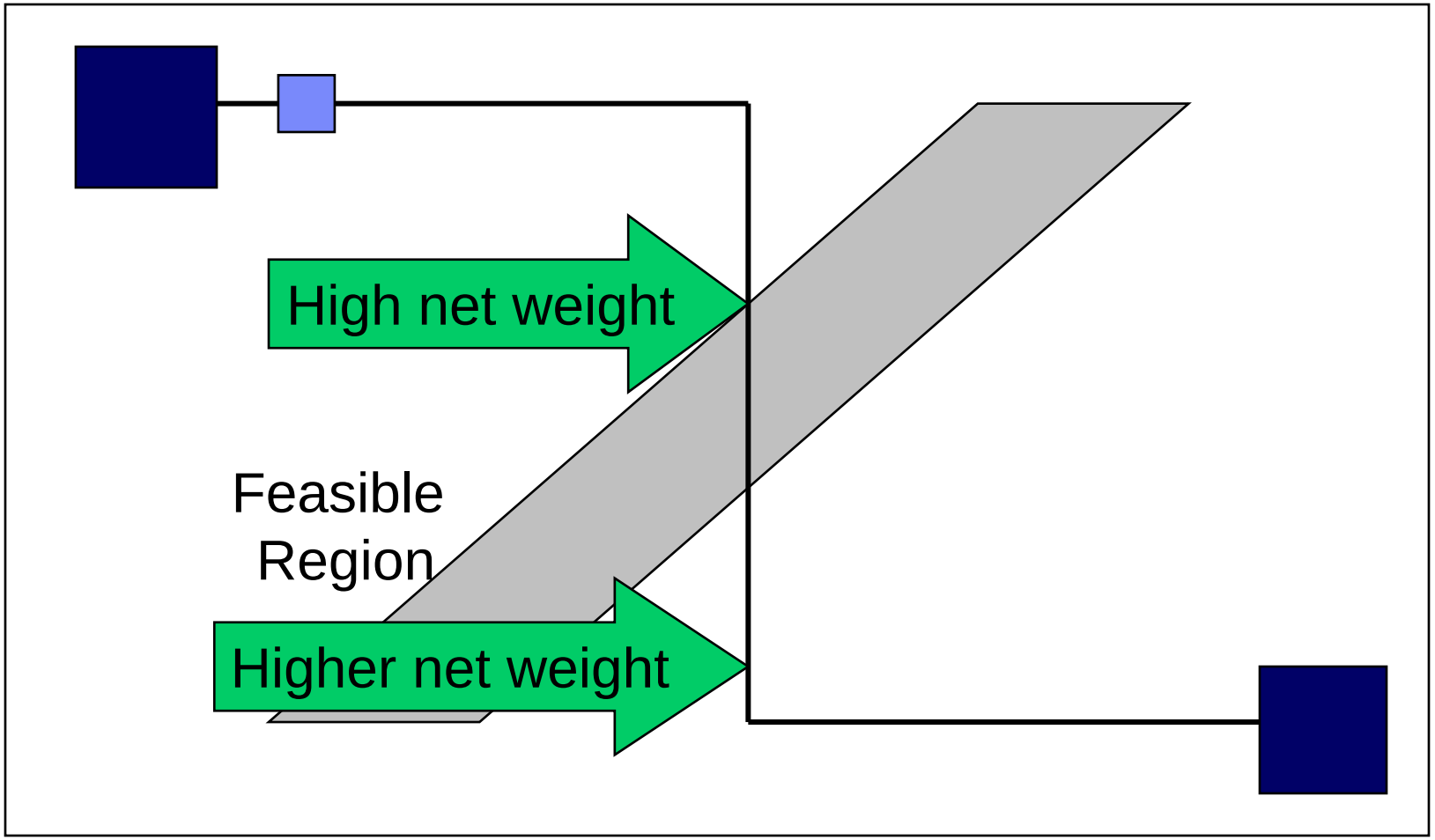


Hand Placed Blocks

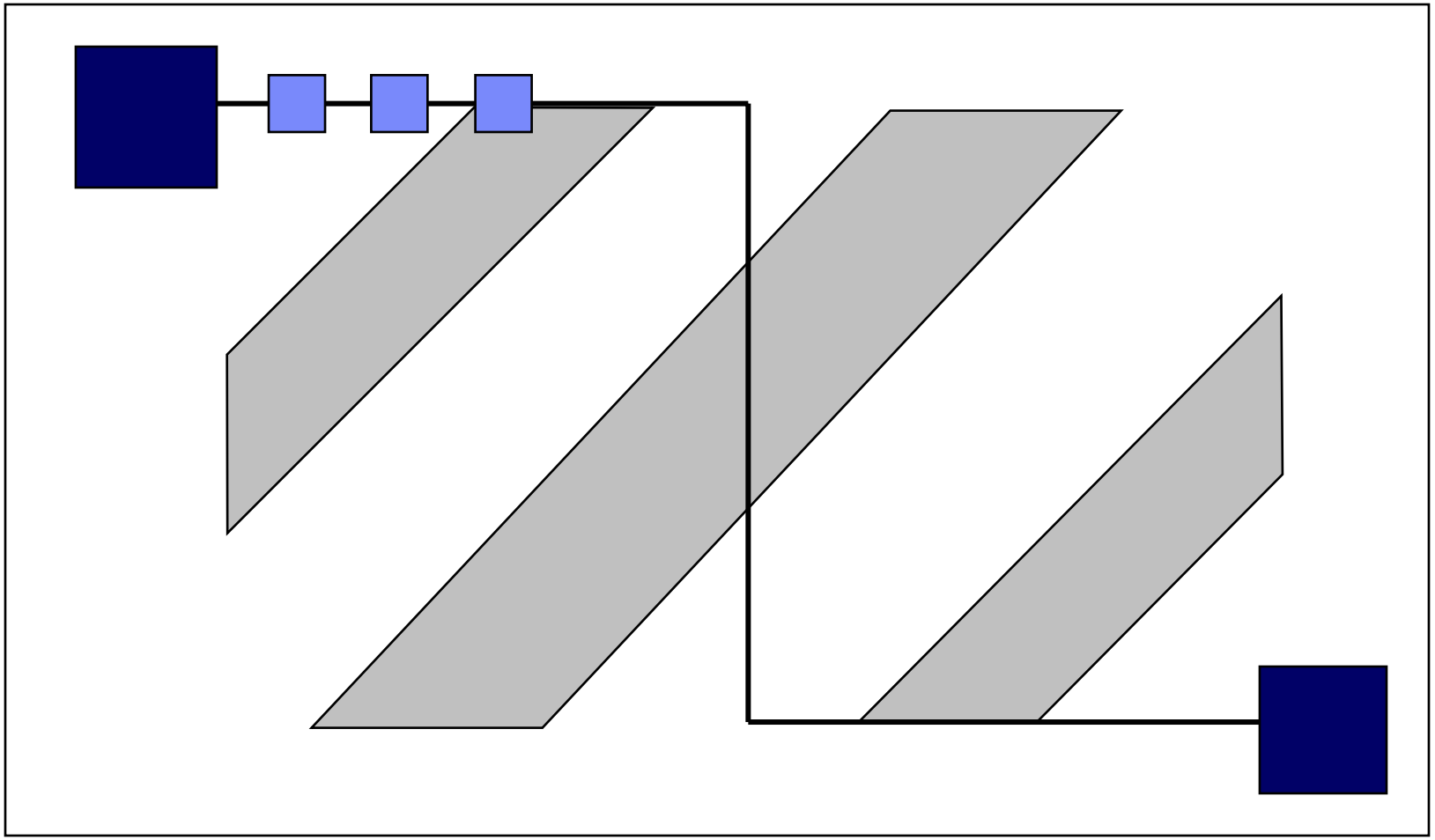


Automatic Block Placement

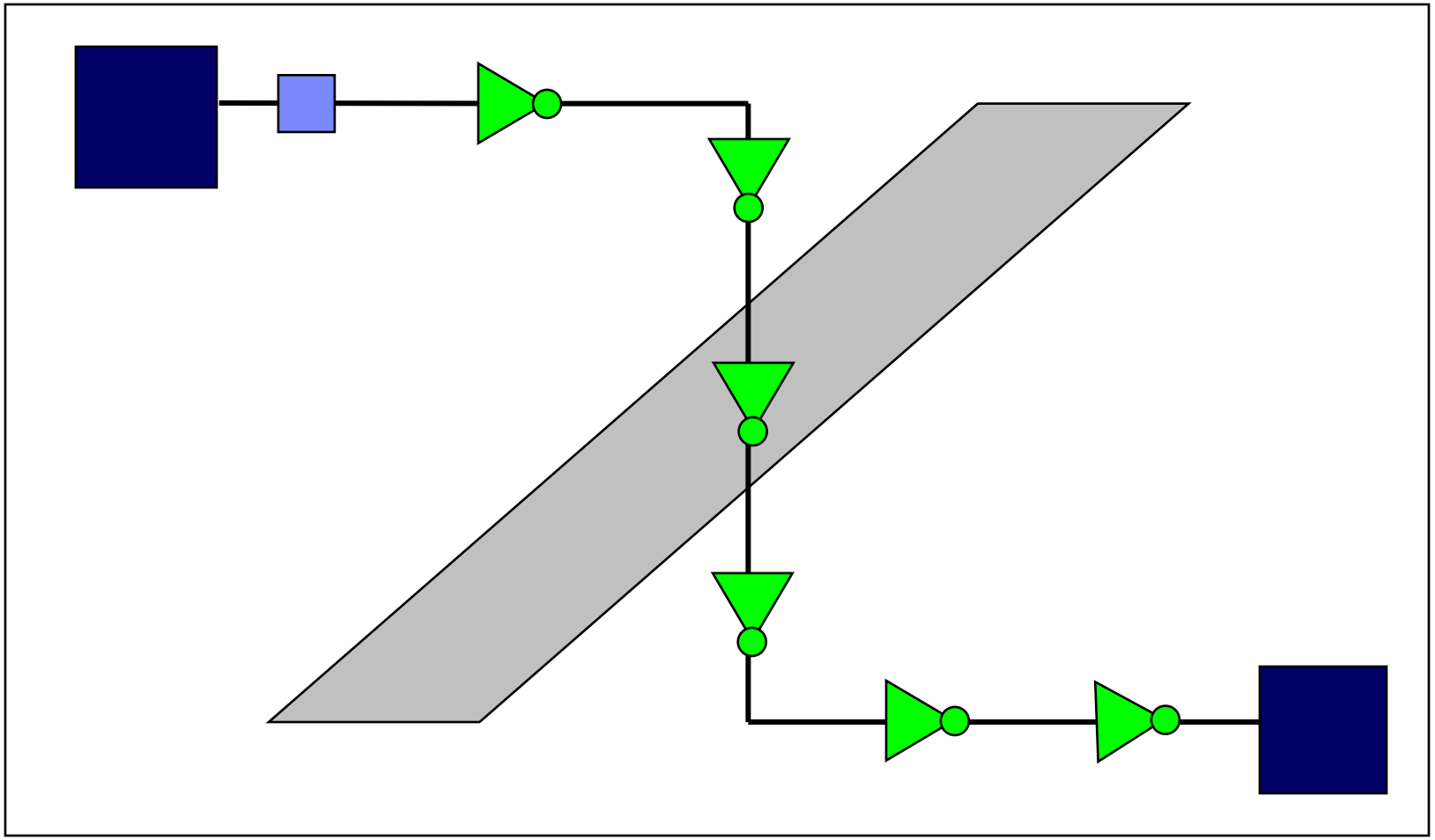
Pipeline Paths: Bad



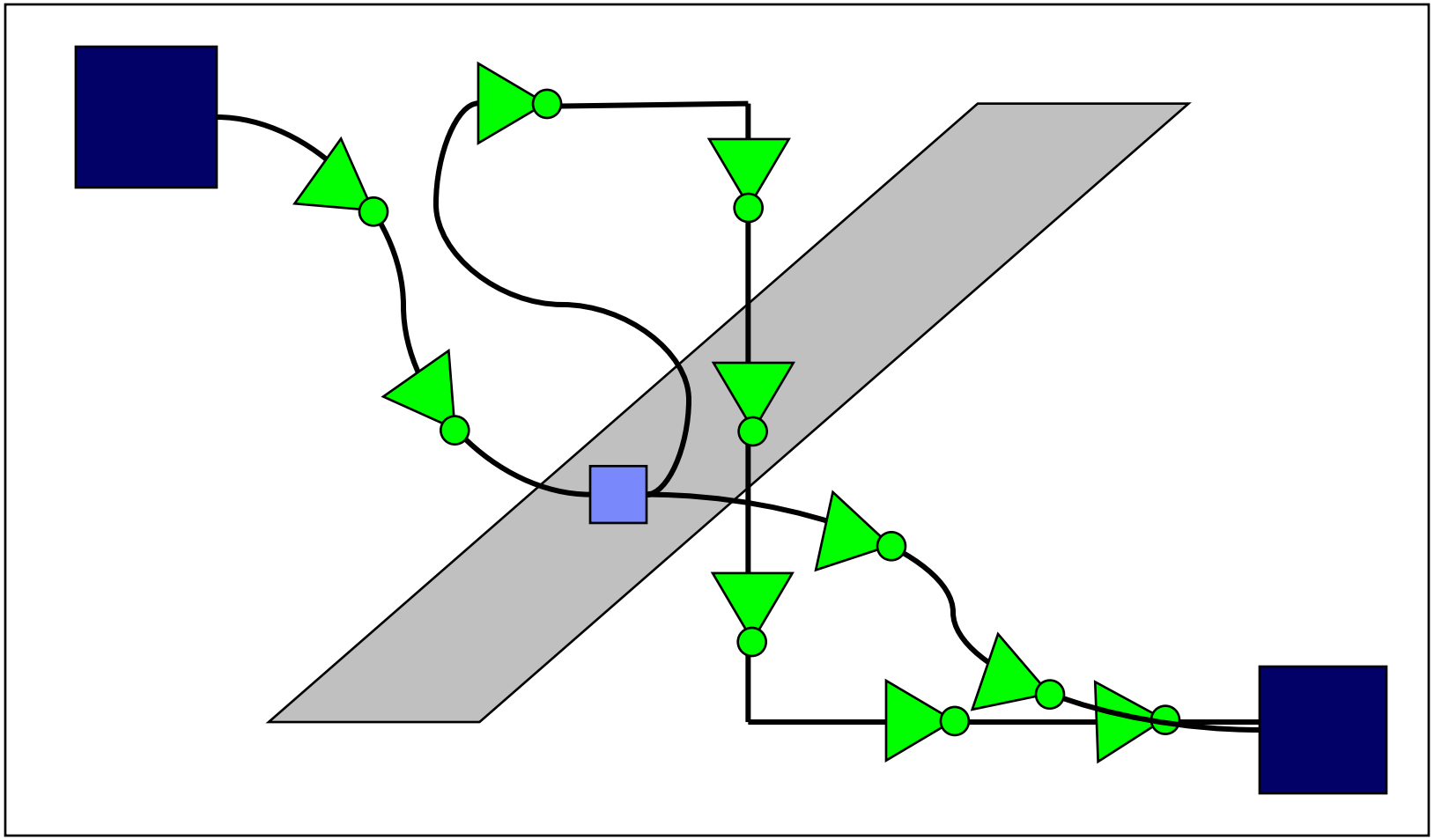
Example Four Cycle Path



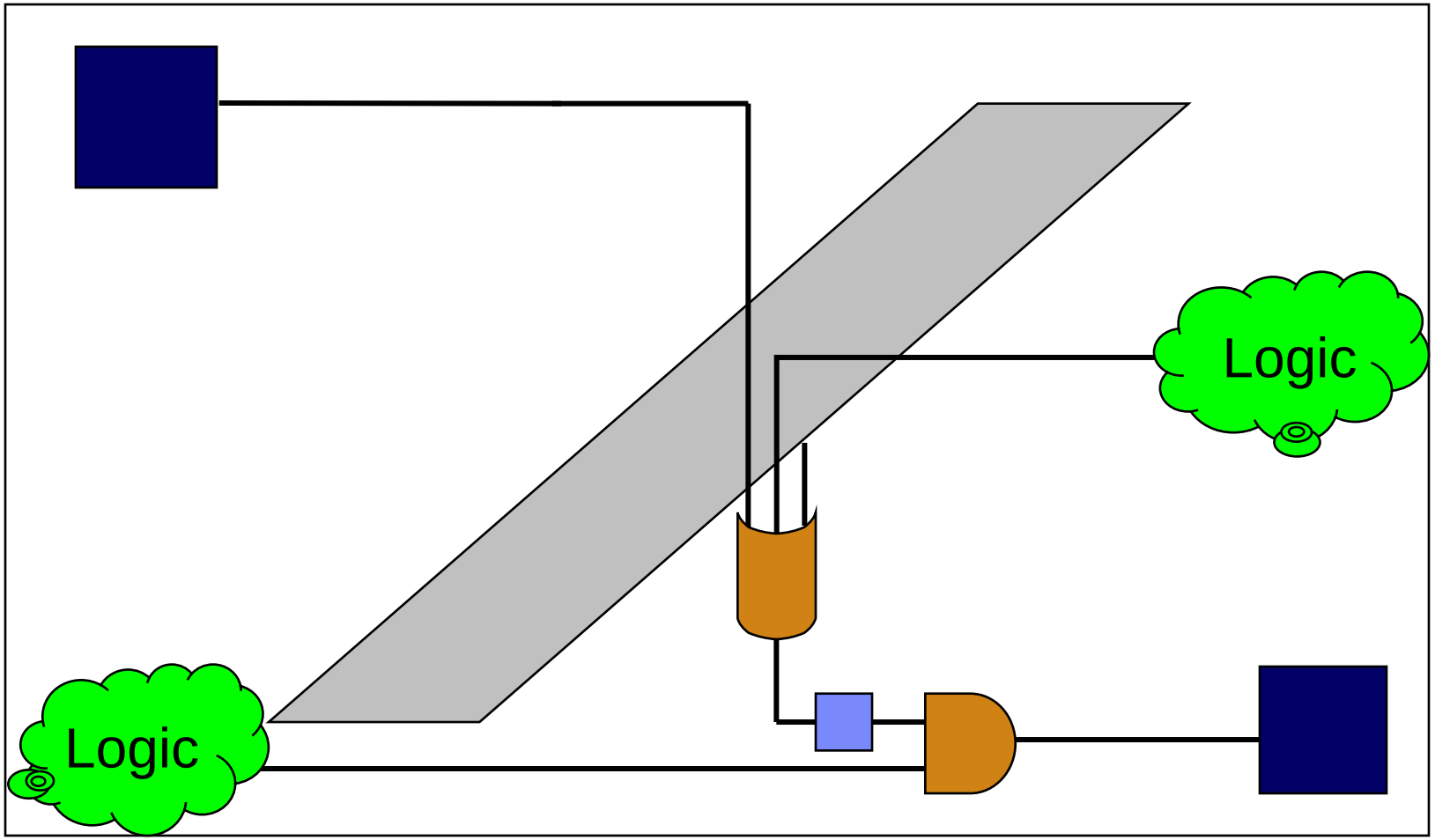
What about Buffering?



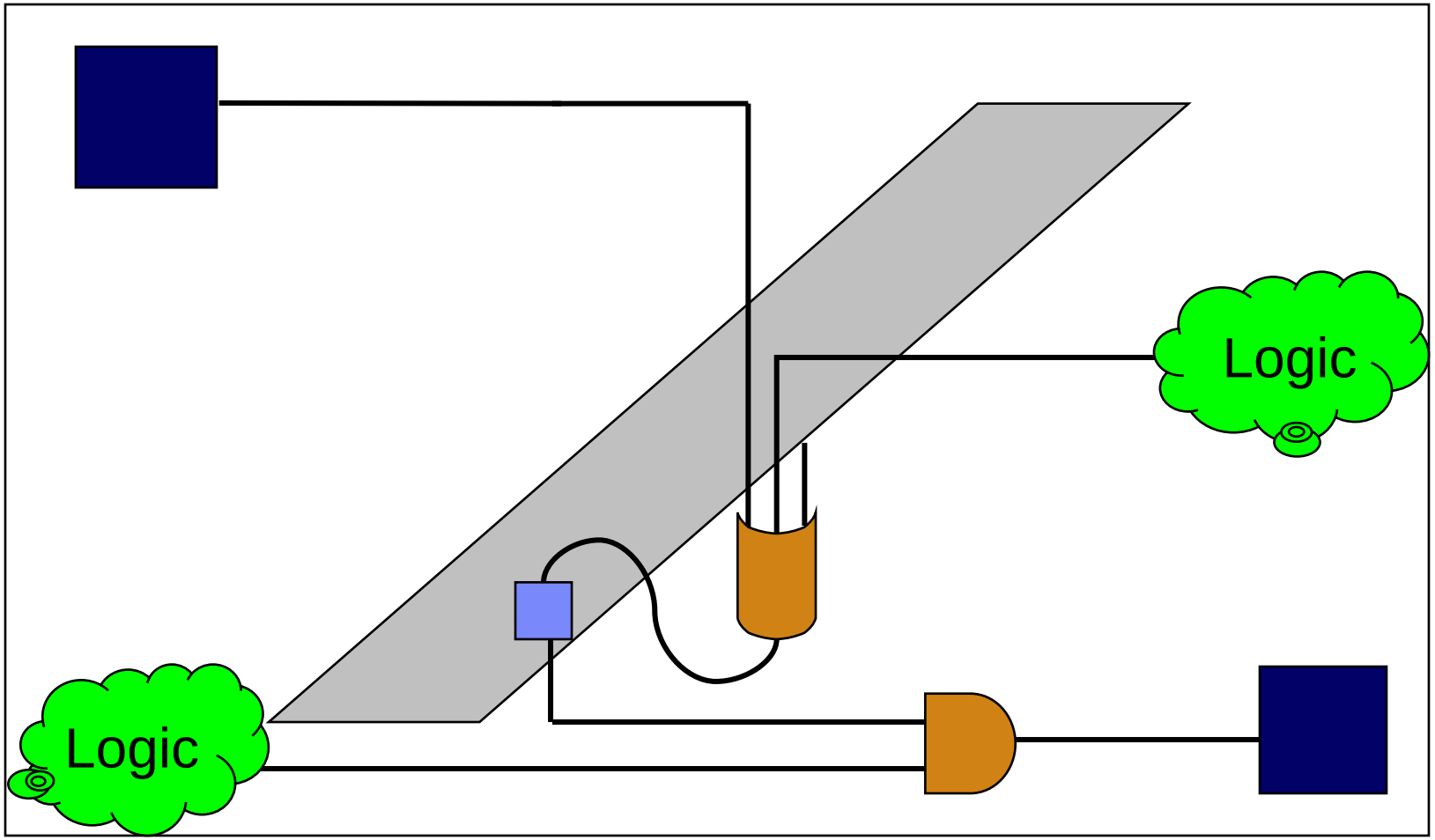
What about Buffering?



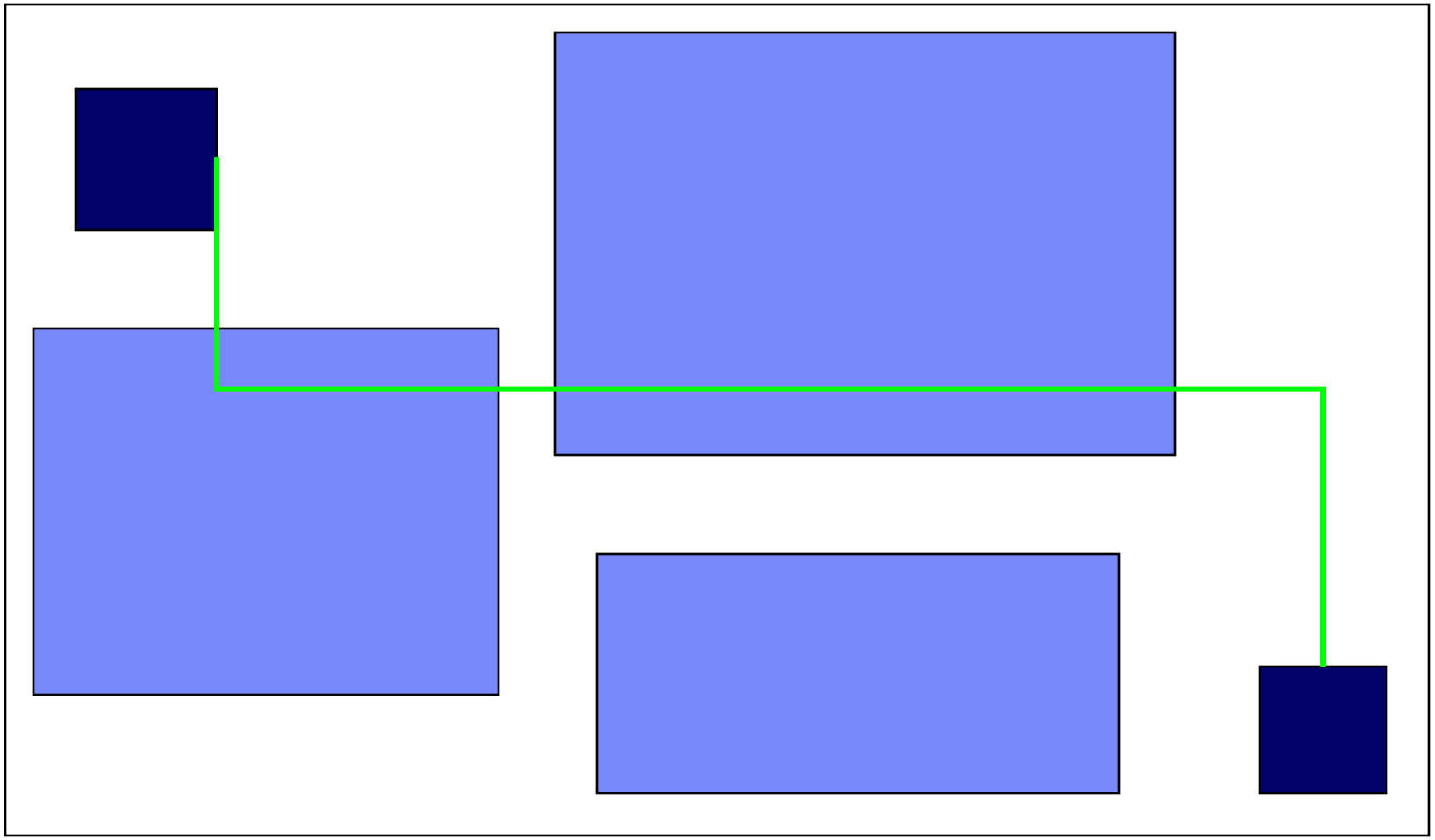
Interference From Other Logic



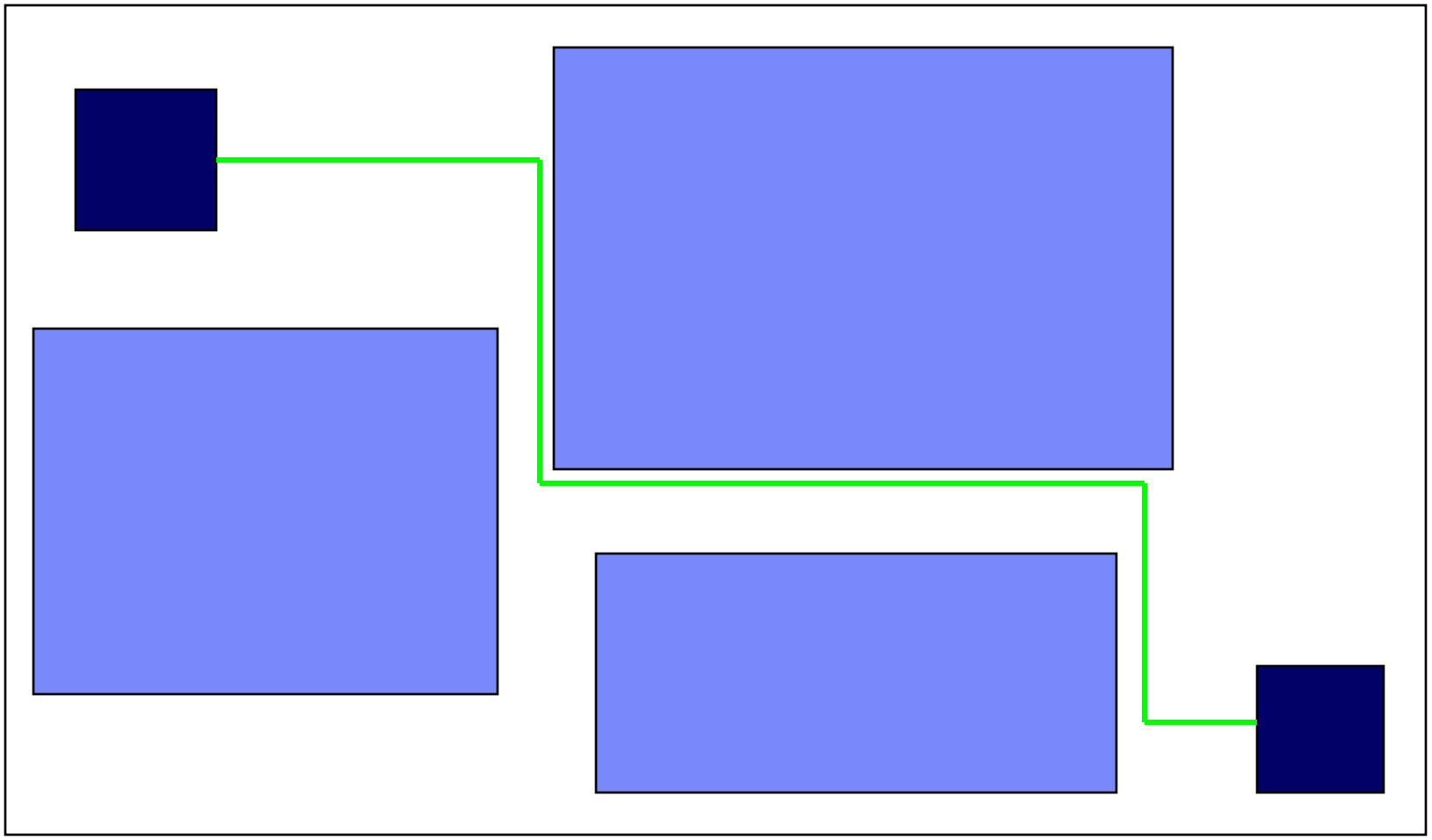
Interference From Other Logic



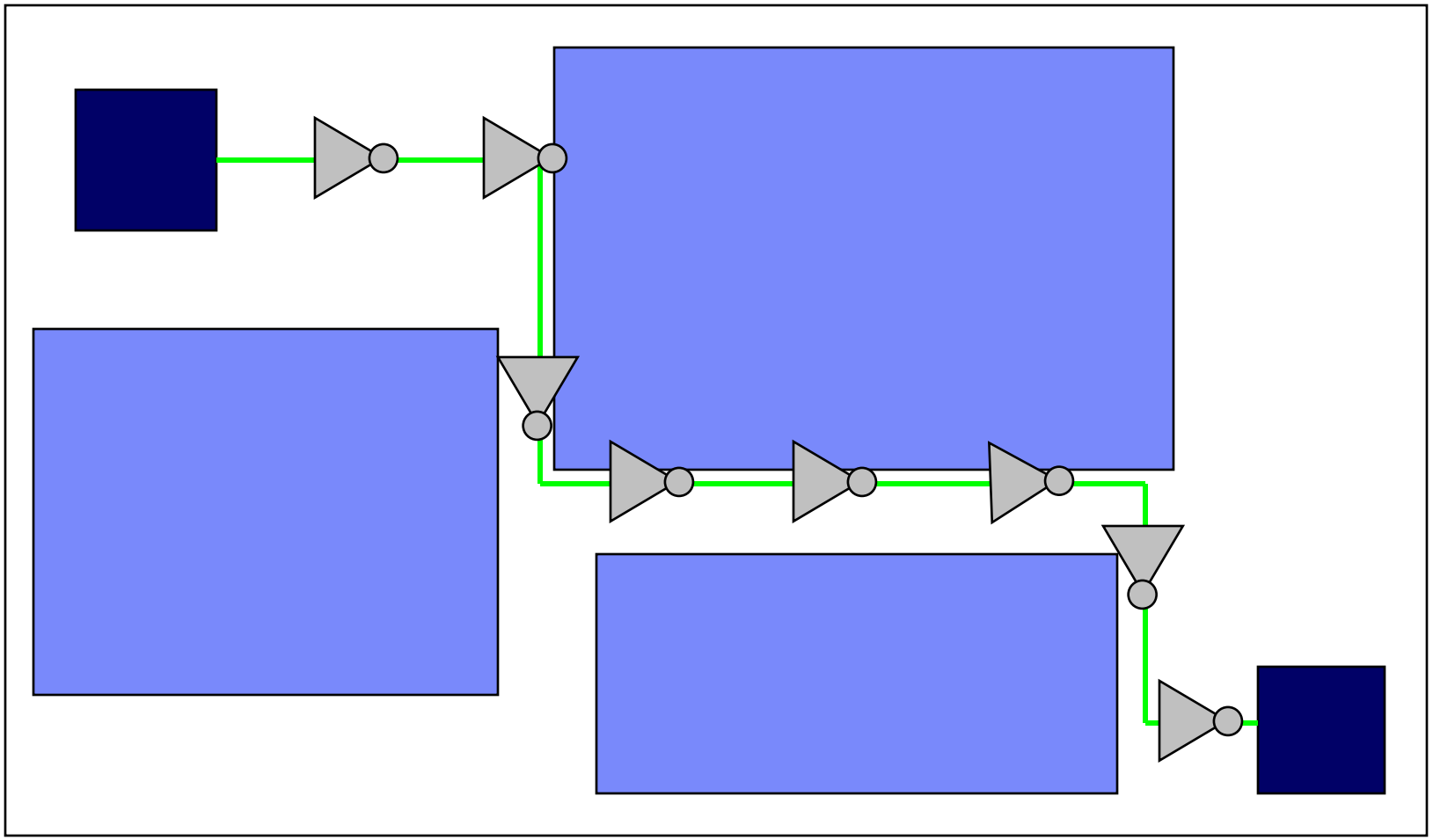
Buffer Aware Routing: Ugly



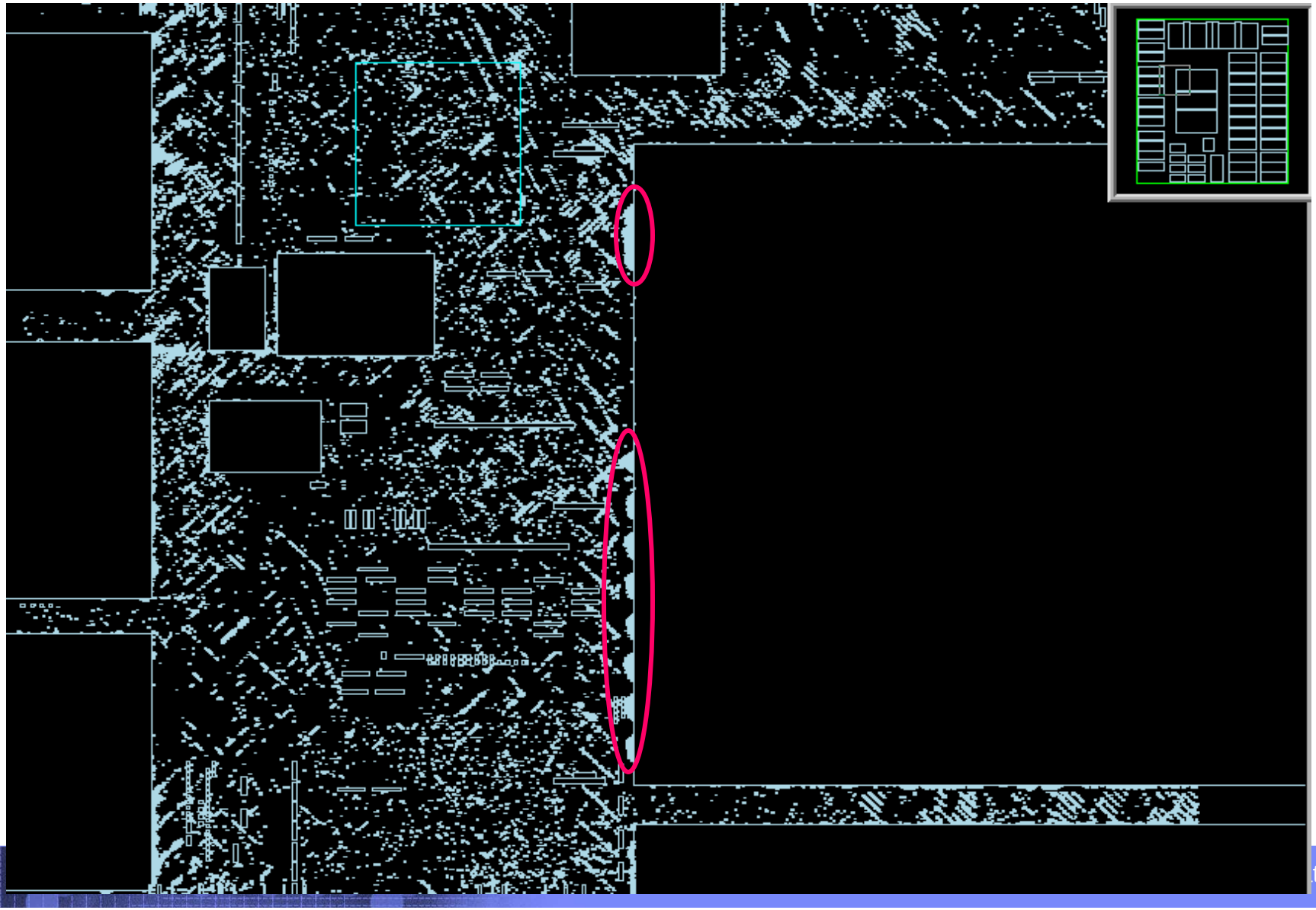
Blockage Avoidance Routing



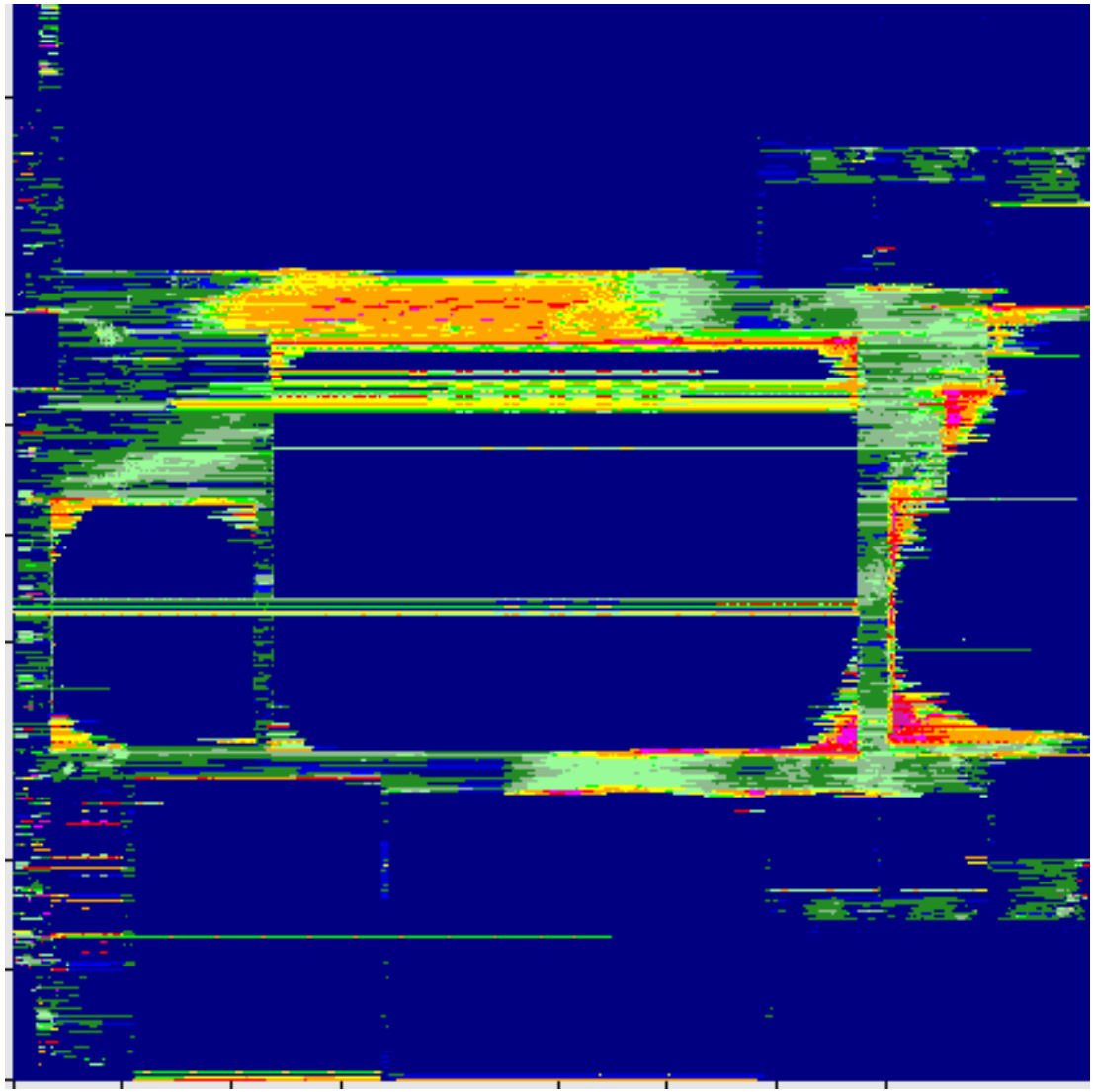
Buffering Restricts Global Routing



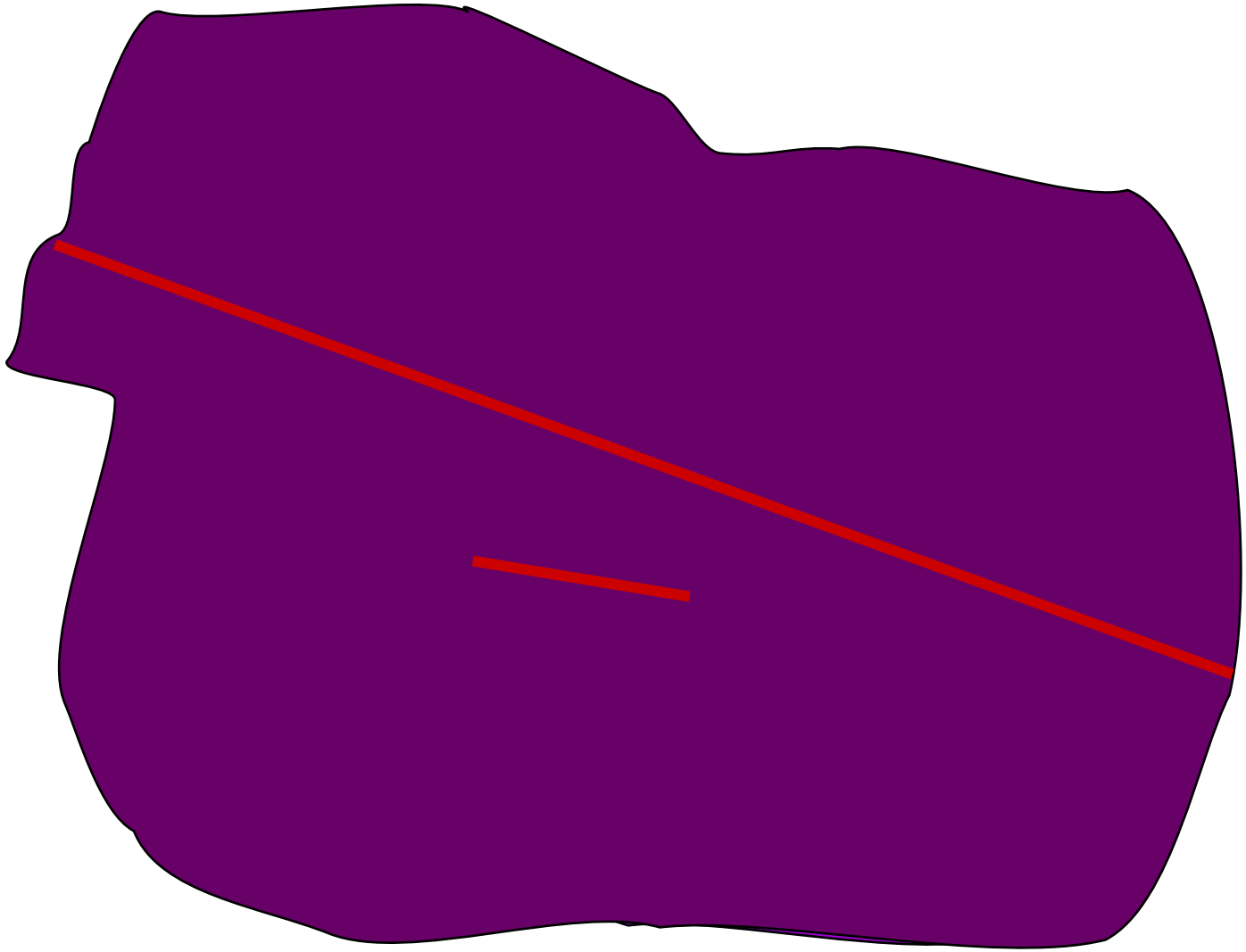
Buffer Pileups



The Corona Effect

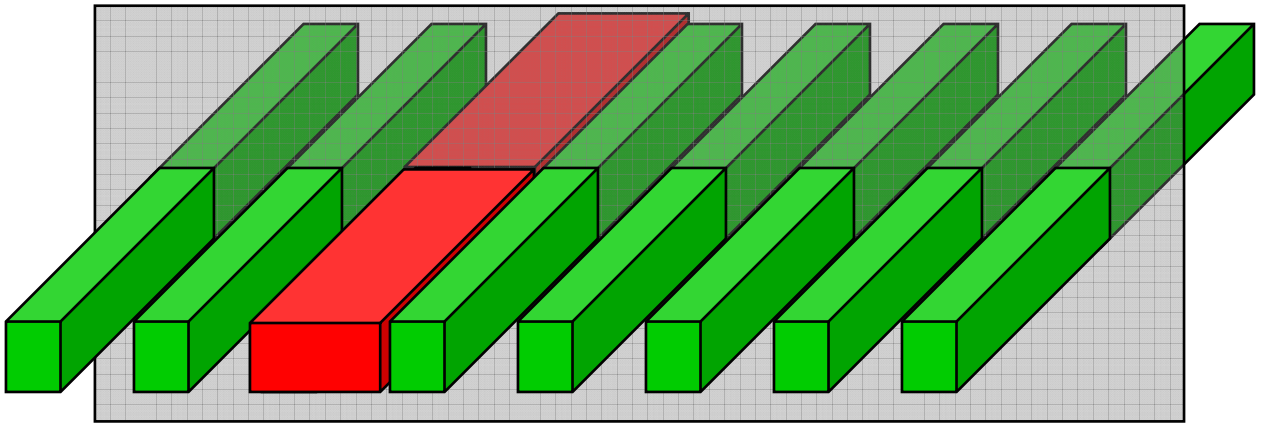


Getting Across Town



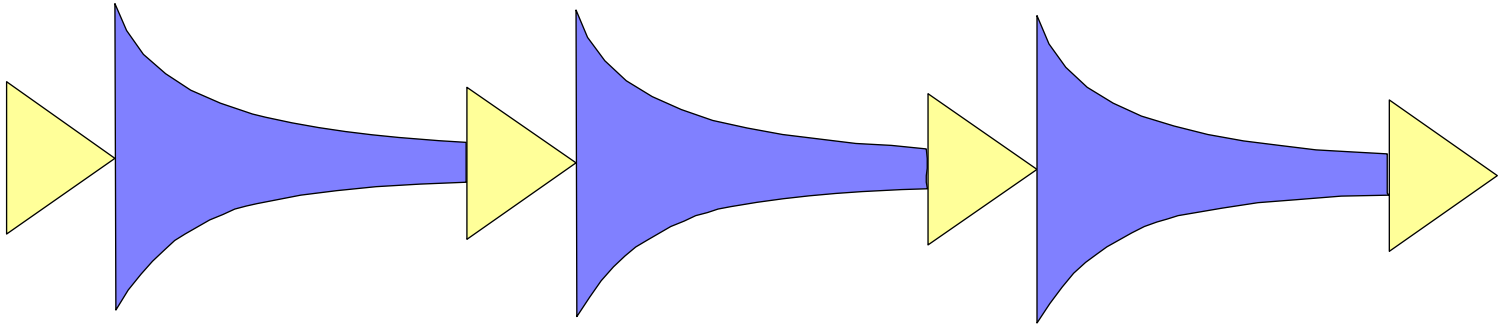
Fat Metal Wires Are Freeway Overpasses

1990s Uniform Wire Sizing in Optimization

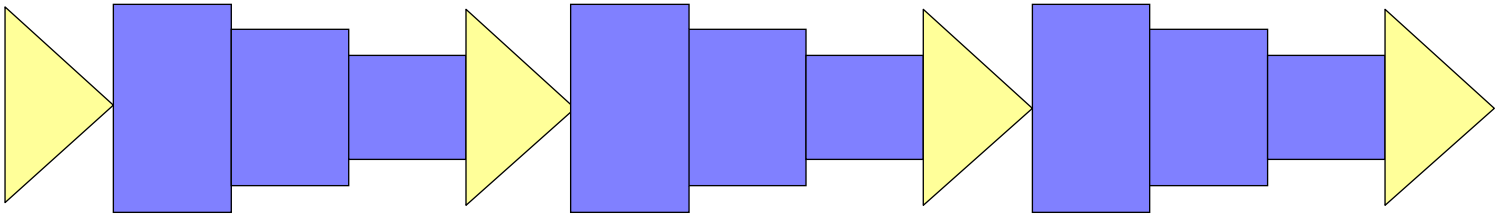


The Academics: Wire Synthesis in the 1990s

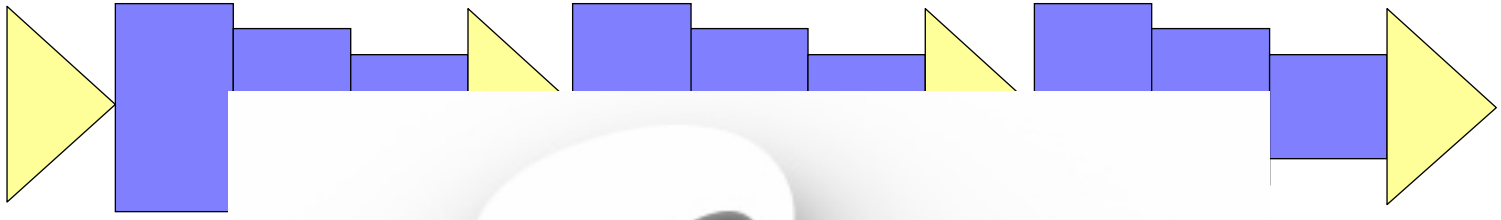
Optimal Wire Shape



Simultaneous Buffering and Wire Tapering



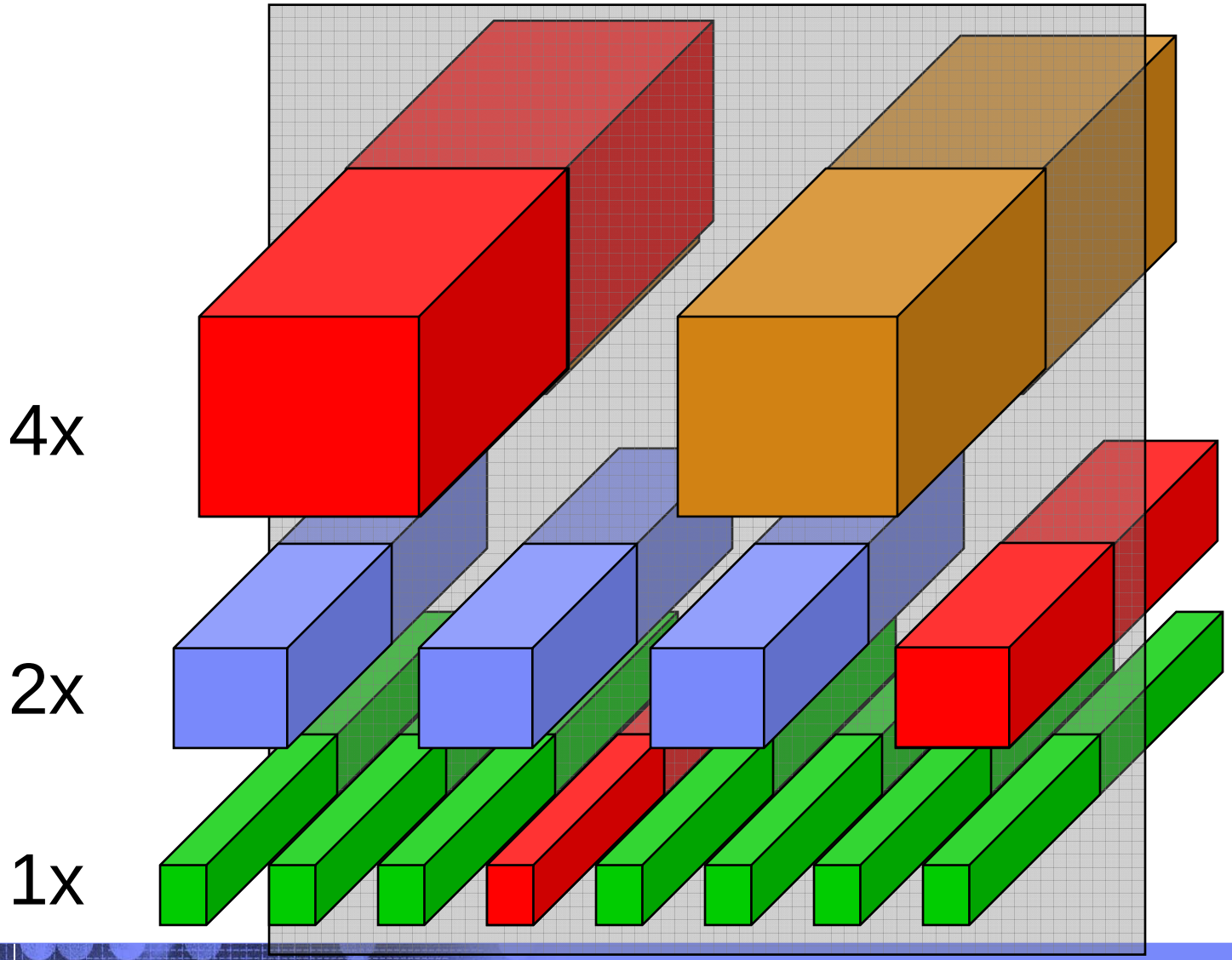
Was Wire Tapering Worthwhile?



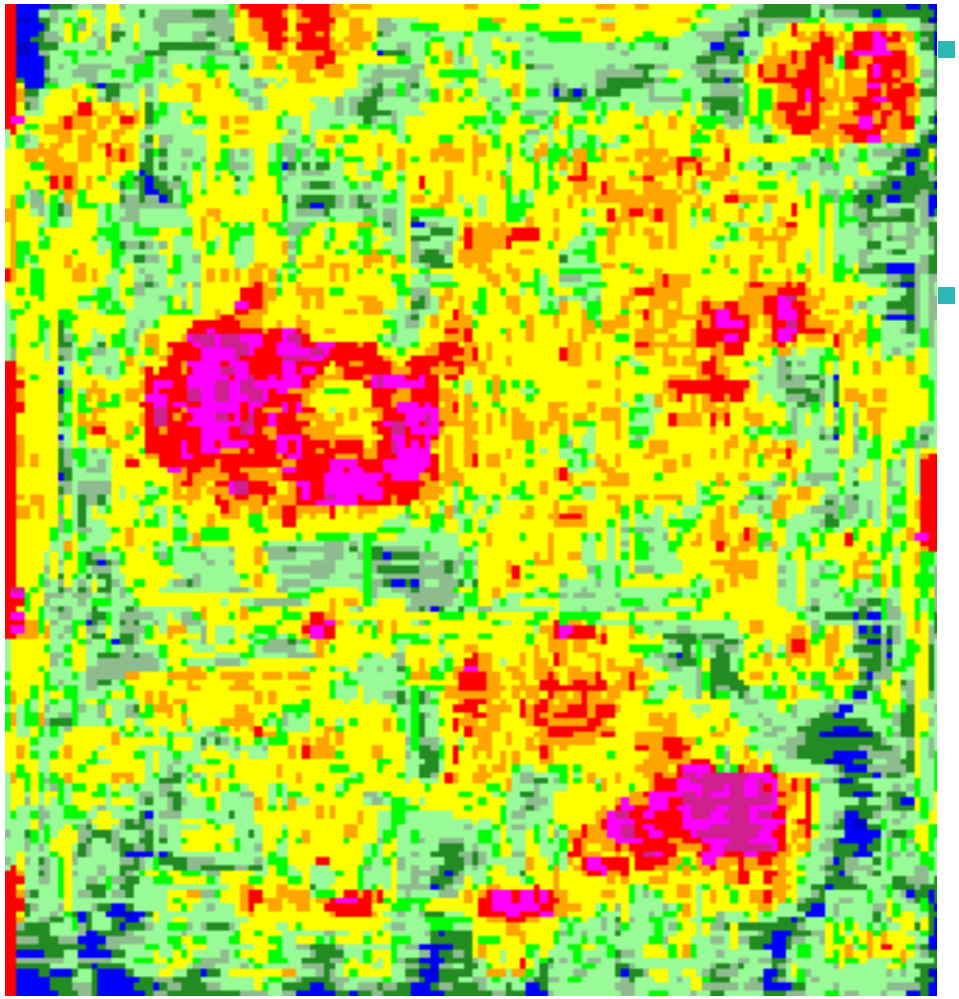
- Route well if at all
- Even

- With to tapering
- Theoretical formula: 3.5% difference in optimal cases

Performing Layer Assignment

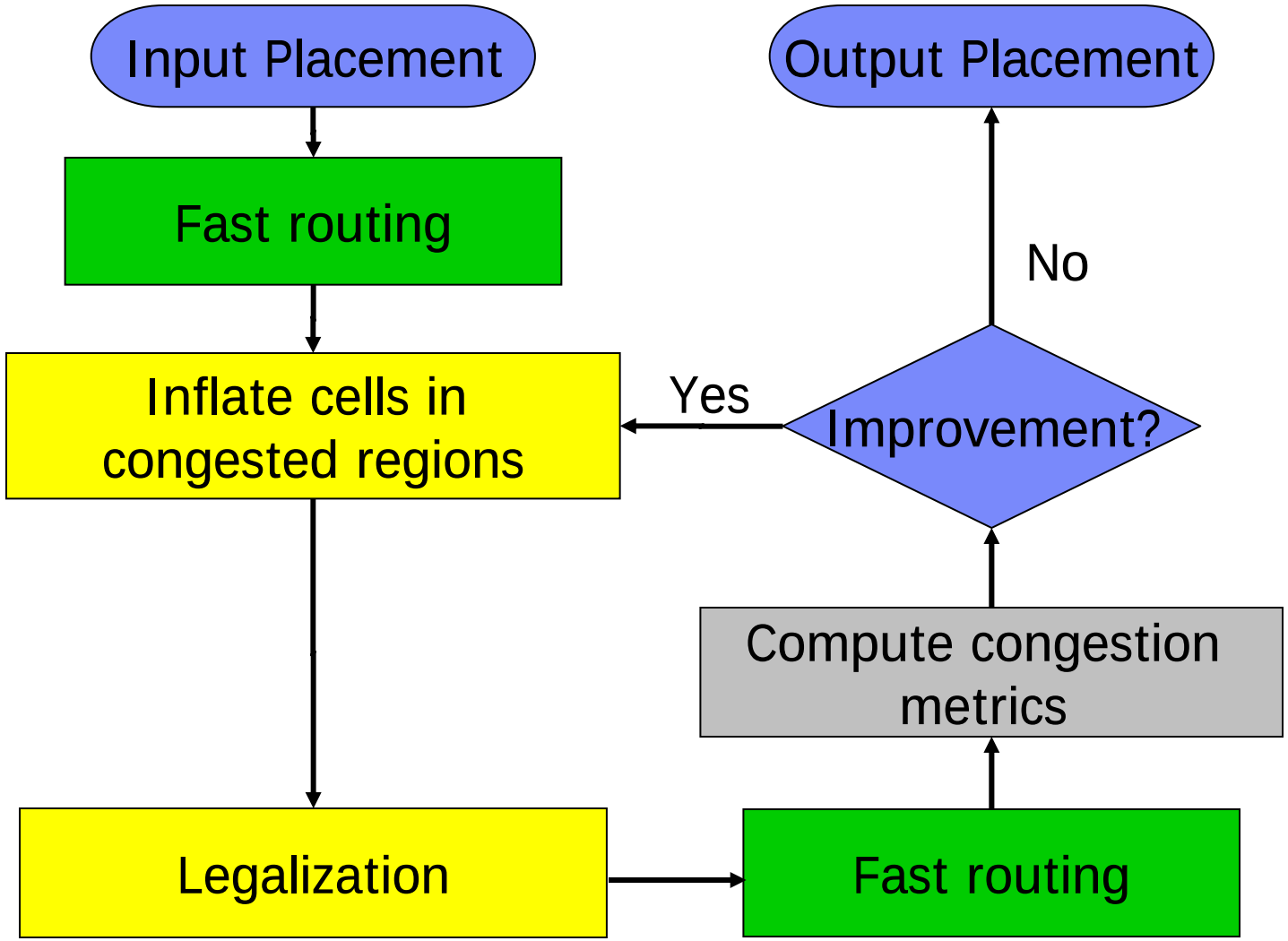


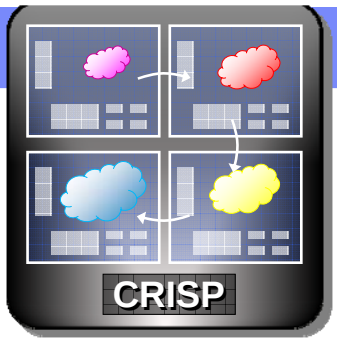
Global Routing Congestion



- **Global placement tries to achieve routability by minimizing wirelength**
- **Hotspots are inevitable**
  - Could make design unroutable
  - Detours hurt timing closure
  - Scenics → electrical violations
  - Must directly model congestion

Overly Simplified Congestion Reduction Flow

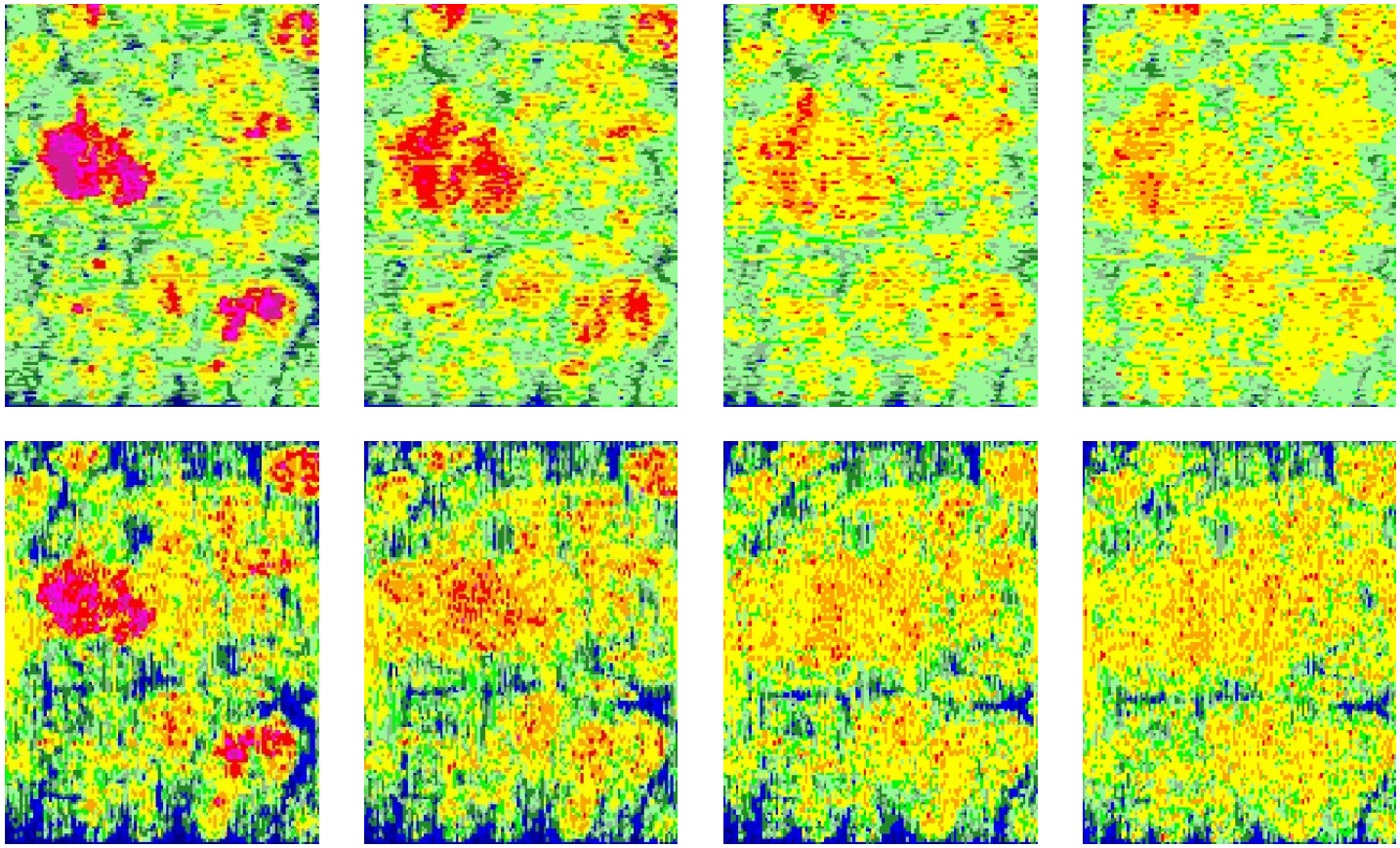




CRISP: Congestion Reduction by Iterated Spreading during Placement

Horizontal Congestion

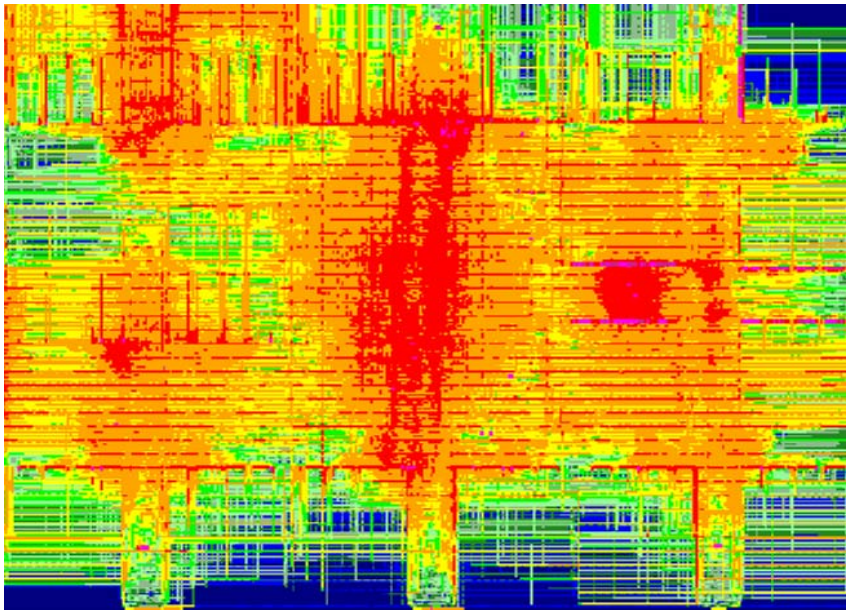
Vertical Congestion

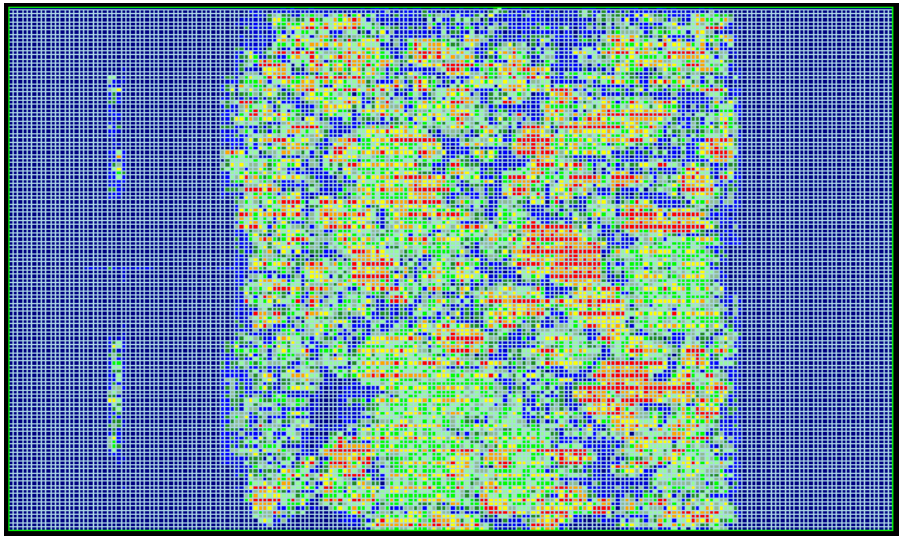


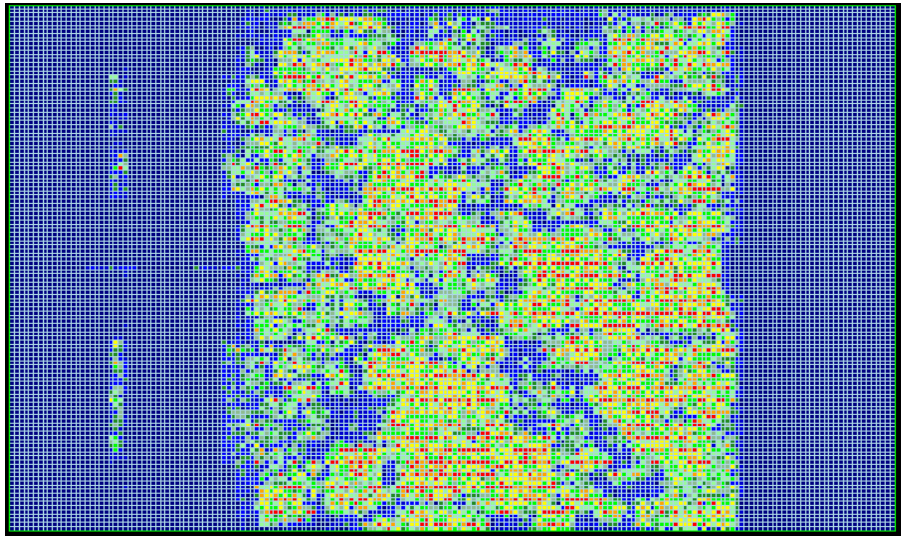
Initial Placement | Iteration 5 | Iteration 10 | Iteration 15

Problems with CRISP

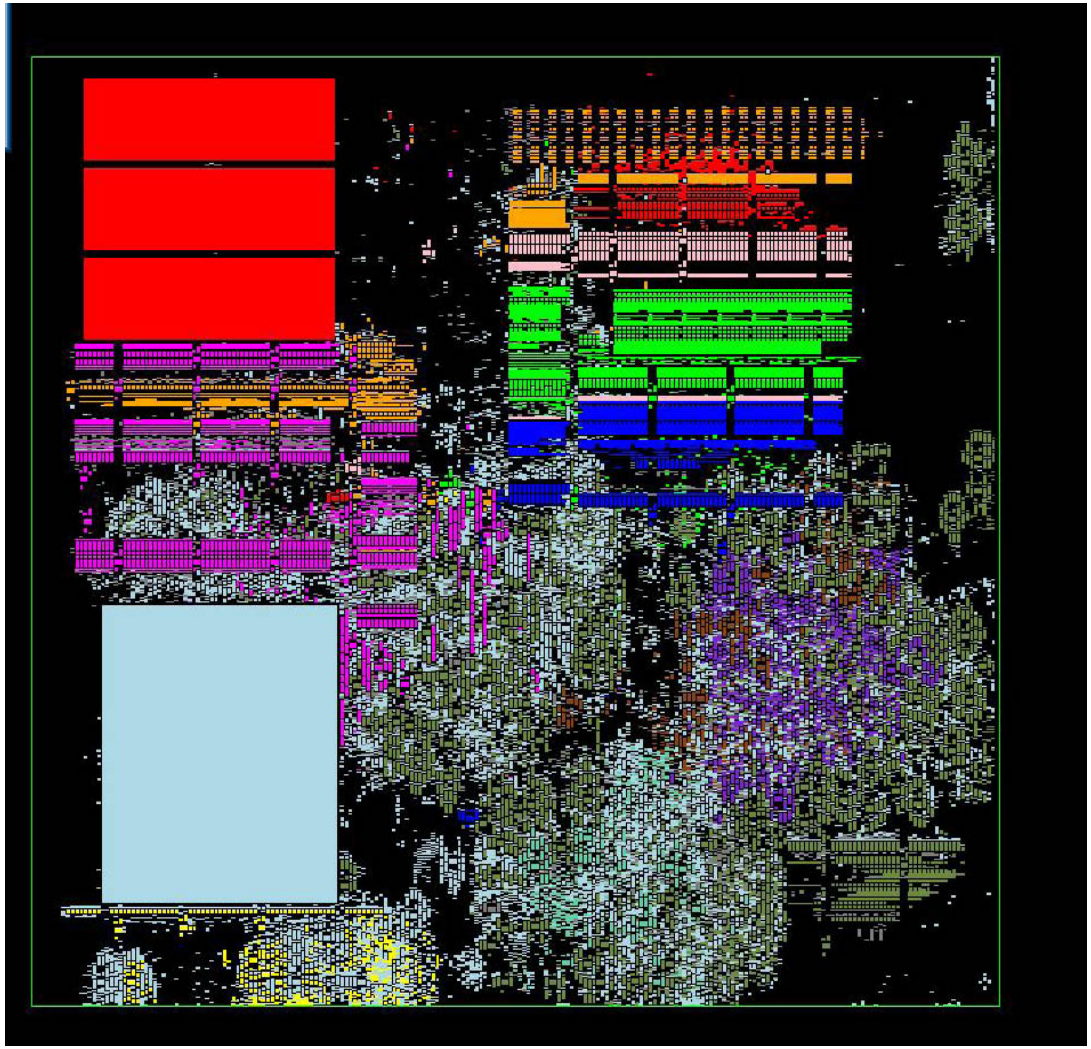
- **Alleys in blockages**
- **Can’t solve over congestion**
- **No capturing of local issues**







Why Do We Still Do Custom Design?



The Power of Our Friends

Grass Roots Change

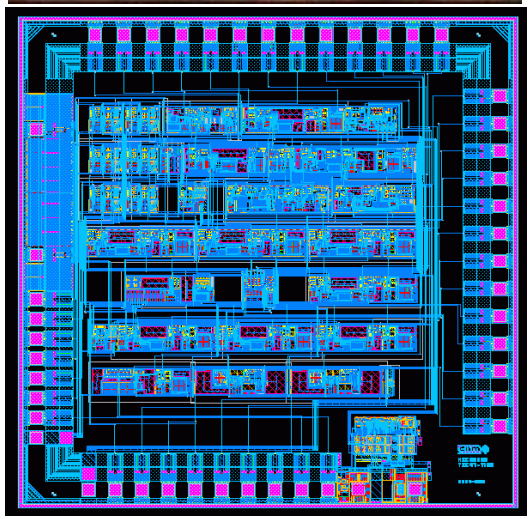
Grass Roots Change

Grass Roots Change

Grass Roots Change

You see, in this world there's two kinds of people, my friend: Those with loaded guns and those who dig. You dig.

- *Blondie*



You see, in this world there's two kinds of people, my friend: Those in charge of the design tools and methodology and those who design. You design.