Advanced Device Modeling in Nanoscale and Wireless Era

Yuhua Cheng

Siliconlinx, Inc.

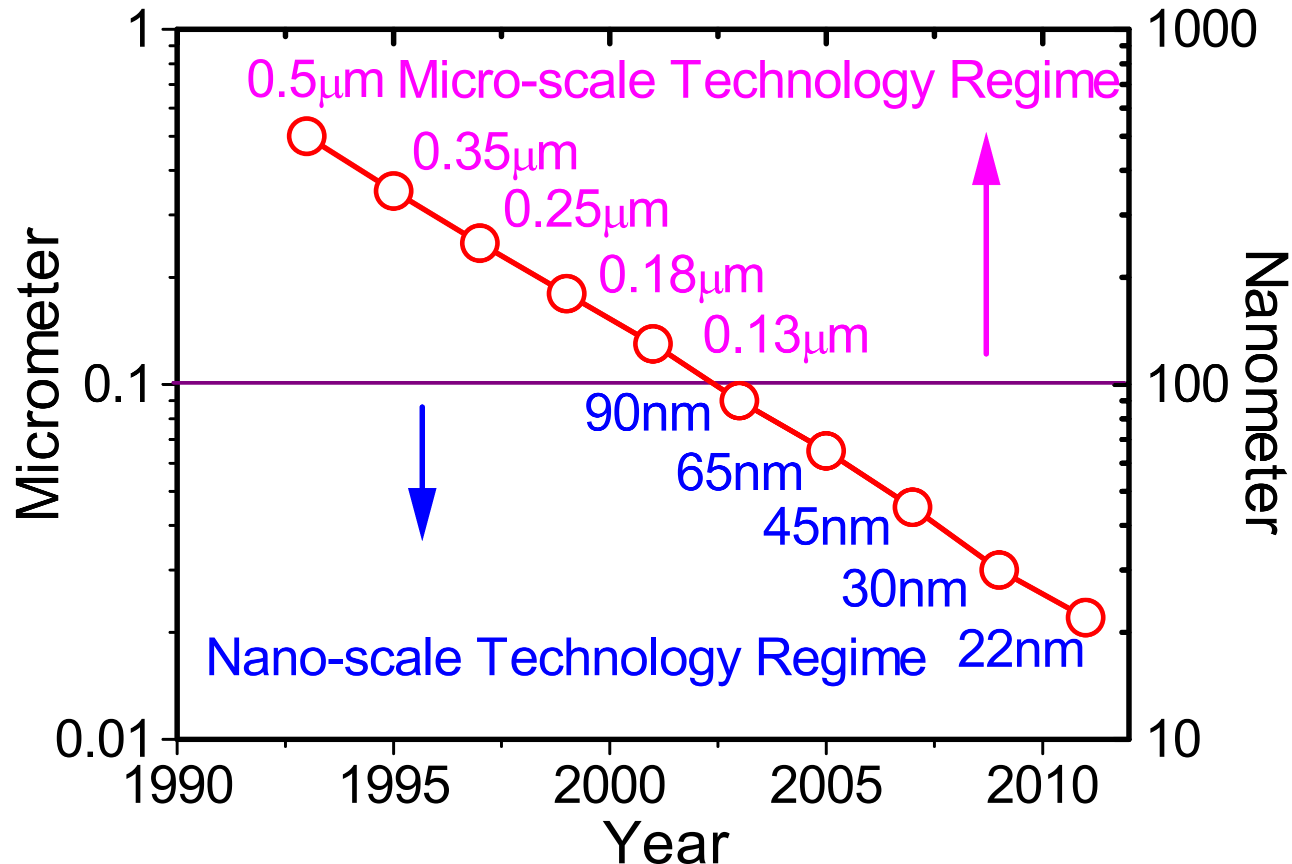
Bridging the gap between IC designers and foundries

Outline

- CMOS Technology Trends
- Nano-scale Device Modeling
- Device Modeling for RF IC Design
- Summary

SILICONLINX
Bridging the gap between IC designers and foundries

CMOS Technology Trends -- Nanoscale



- CMOS has entered into nano-scale era.
- Silicon CMOS is still the mainstream IC technology in the next 7-10 years before other nano devices play roles.

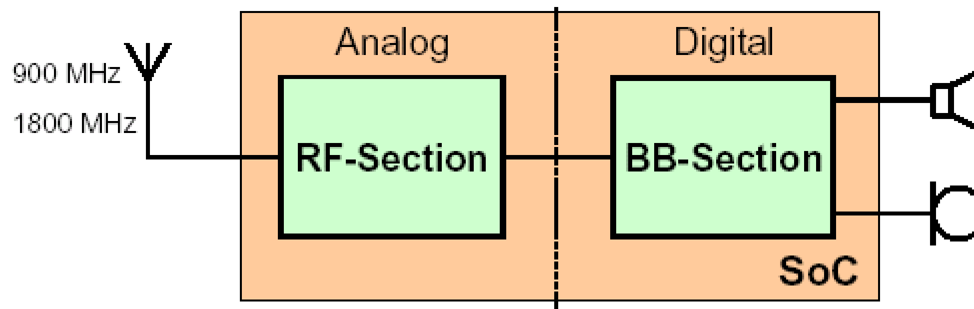
Yuhua. Cheng

SILICONLINX

Bridging the gap between IC designers and foundries

CMOS Technology Trends -- RF CMOS

- Recent speed improvements and better noise behavior of CMOS transistors have made it feasible to implement RF circuits for wireless products, such as cell phones, Global Positioning System, and Bluetooth.
- CMOS is one of the best suitable technologies to ingrate RF circuits with analog and base-band digital circuits.
- Tremendous research effort is dedicated to RF CMOS, driven by System-on-Chip (SoC), using inexpensive single chip transceivers, including both the base-band and the RF sections.



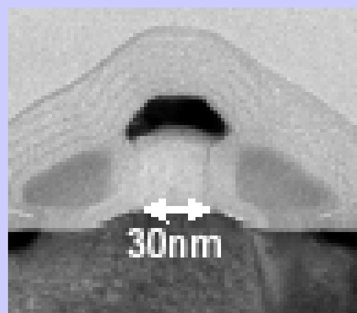
CMOS:
High integration density
High yield
Low power consumption
Low cost

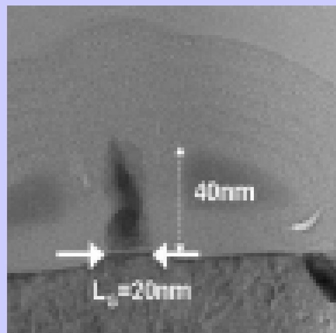
Yuhua. Cheng

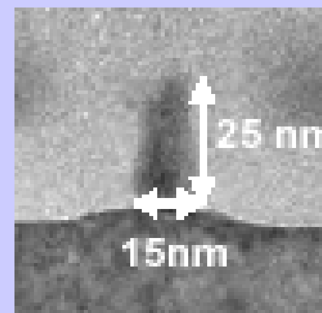
SILICONLINX
Bridging the gap between IC designers and foundries

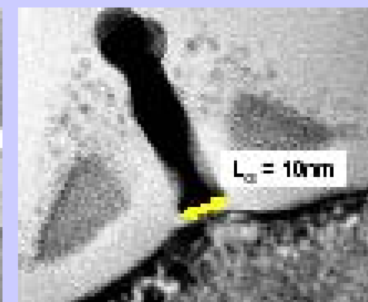
New Material & Novel Structures

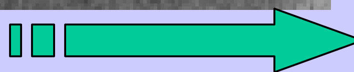
90nm Node | 65nm Node | 45nm Node | 32nm Node | 22nm Node

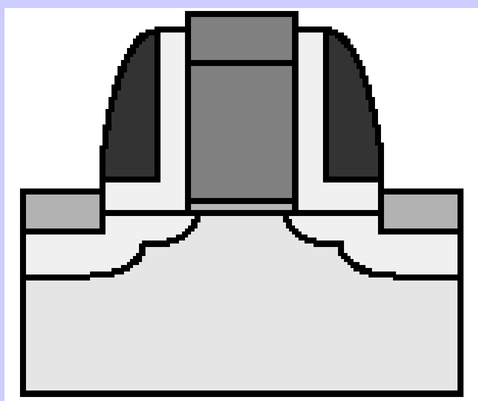


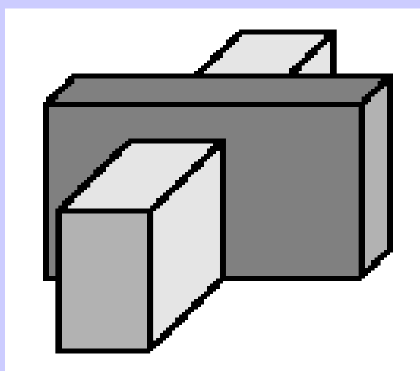


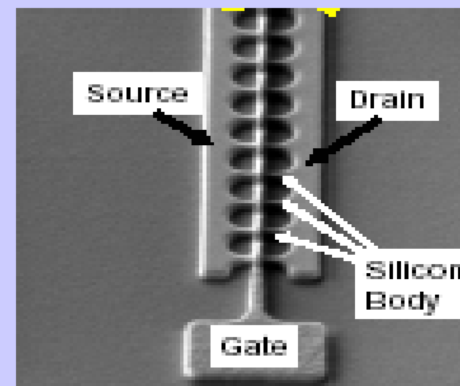




Low-K/Strained Channel  **High-K/Metal-Gate**



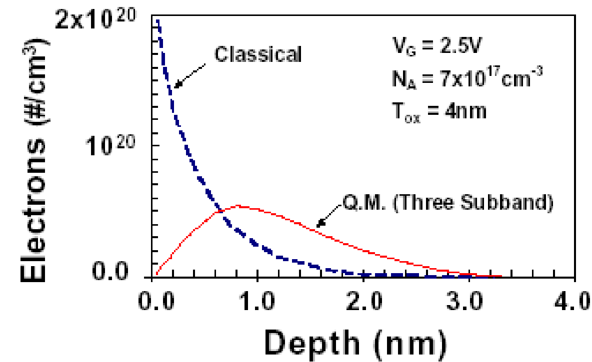


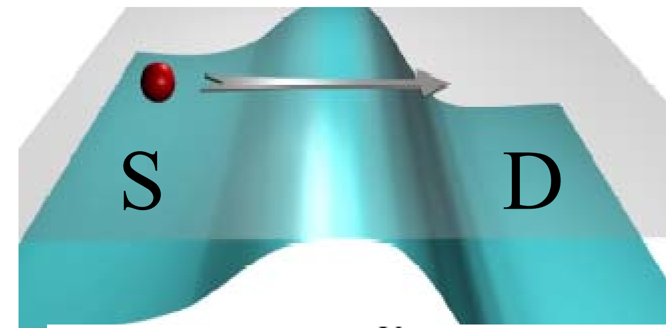


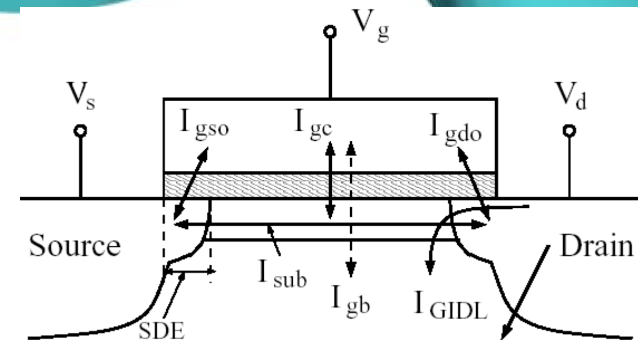
Planar MOSFET **3D Devices**

Device Physics in Nano-scale MOSFETs

- Quantum-mechanical Effects
  - Carrier distribution.
  - Impact of the thickness of inversion charge layer.
  - Both charge density and potential.
- Ballistic transportation
  - Velocity saturation at the source.
  - Electrons emitted from the source with sufficient energy to overcome the barrier in the channel reach the drain conserving energy and transversal momentum.
  - Carrier scattering at the source.
- Tunneling of Carriers
  - Through very thin gate oxide.
  - From source to drain, and from drain to the body of the MOSFET.
  - Quantum tunneling (intra-band and inter-band).







Yuhua. Cheng

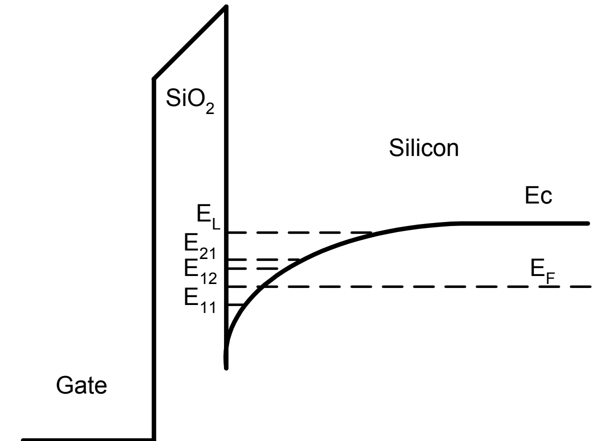
SILICONLINX
Bridging the gap between IC designers and foundries

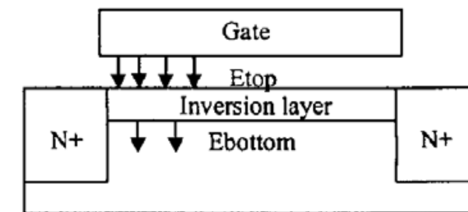
Modeling of Quantization Effects

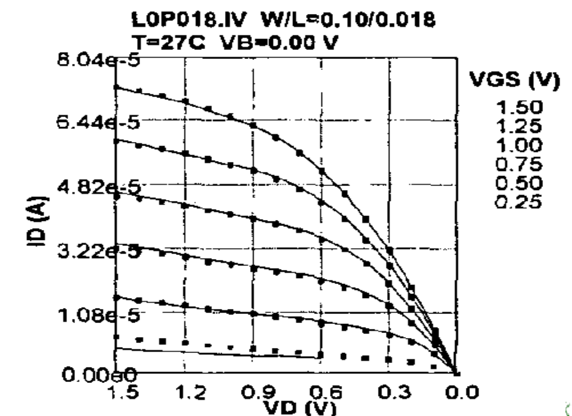
- Carriers are confined in the direction perpendicular to the surface and discrete energy levels need be treated quantum mechanically (2-D).

$$E_j = \left[\frac{3 \cdot h \cdot q \cdot E_s}{4\sqrt{2 \cdot m_x}} \left(j + \frac{3}{4} \right) \right]^{2/3}$$

- An efficient approach to model the quantum effect.
  - The Schrodinger equation was solved at the boundary conditions of Etop and Ebottom.
  - Models based on this approach could describe the behaviour of devices with L of 18nm.

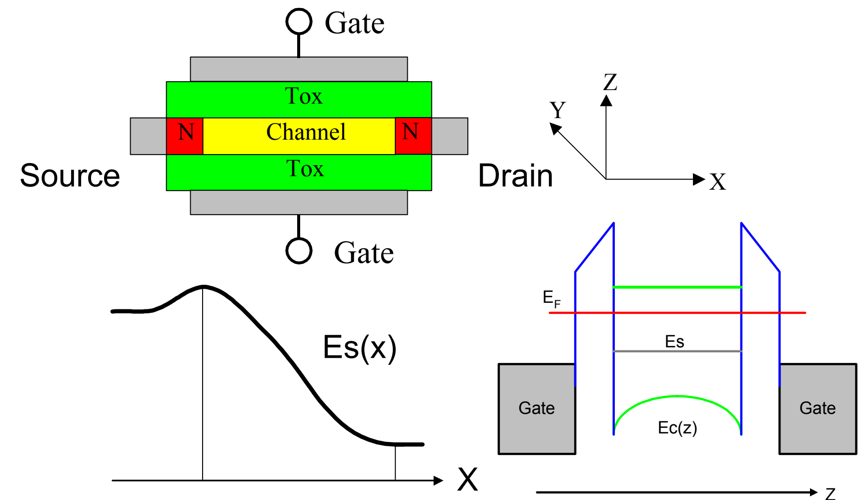






Modeling of the 2-D Effects

- A 2-D modelling approach considering vertical current distribution and lateral carrier transport due to the two-dimensional (2D) sub-band splitting and the lifting of the six-fold degeneracy of silicon conduction band is required.
- A quasi-2D approach to introduce quantum effects in vertical direction and use semi-classical method along the channel has been used in compact modeling.



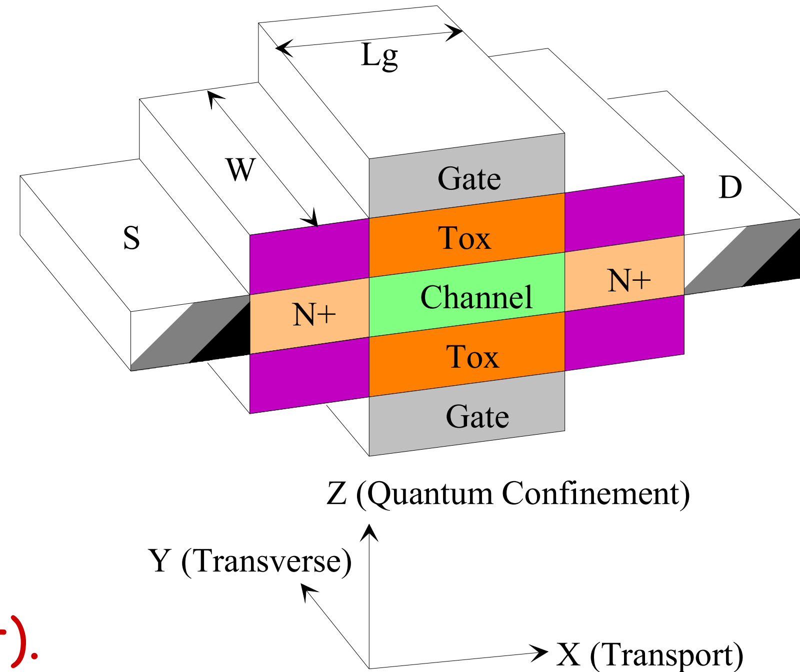
- Potential
- Charge
- Mobility
- Velocity

Yuhua. Cheng

SILICON LINX
Bridging the gap between IC designers and foundries

Modeling of the 3-D Effects

- Modern MOSFETs show 3-D effects
  - Confinement along z-direction (quantization effects).
  - Transport along x-direction (traditional short channel effects).
  - Transverse along y-direction (traditional narrow width effect).
- Semi-3D approaches based on tolerable assumptions and approximations are possible solutions in developing compact models for nano-scale devices.



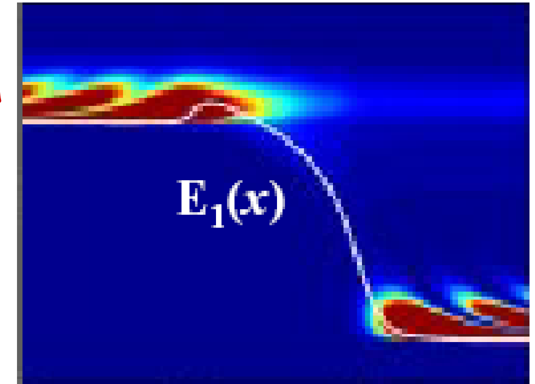
$$\psi(x,y,z) = \phi(x,z)\frac{f(y)}{\sqrt{W}}$$

Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

Modeling of Ballistic Transport

- Ballistic Transport (BT)
  - Ballistic electrons injected from the source with energy greater than the barrier height transmit freely from source to drain while those below the barrier are reflected to the source.

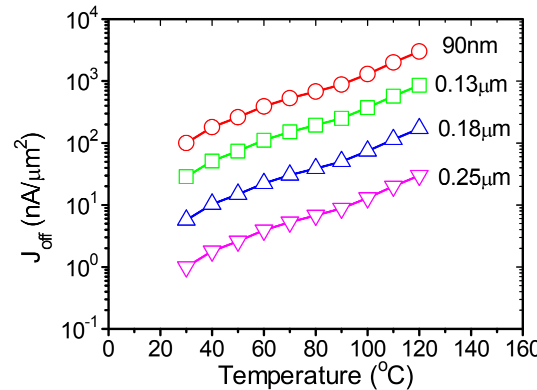


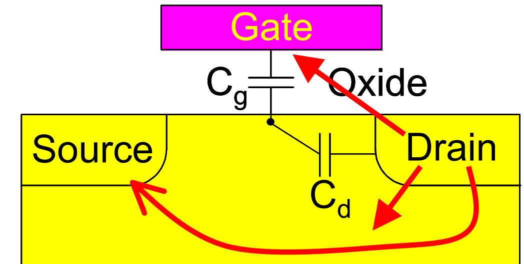
- Understanding of physics on BT
  - Fundamental device physics.
  - Ballistic distribution.
  - Solution of the ballistic BTE (Boltzmann transport equation).
- Modeling Issues
  - Models based on drift-diffusion underestimates Idsat.
  - Models based on ET (Energy Transport) approach overestimates Idsat.
  - Incorrect description of channel velocity overshoot.
- Modeling Efforts
  - New compact model based on solutions of current and energy equations.
  - Predicting ballistic peaks and imposing thermal injection limit.

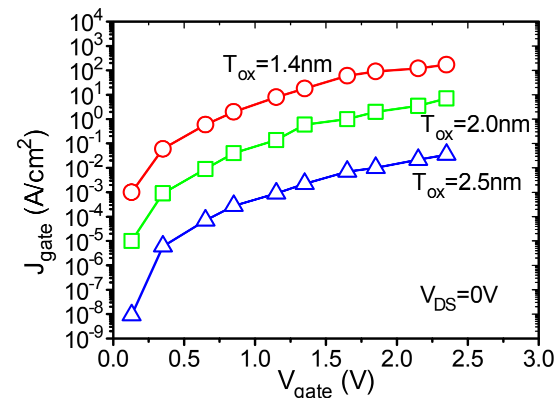
SILICONLINX
Bridging the gap between IC designers and foundries

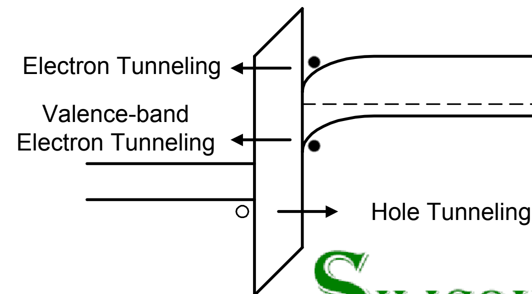
Modeling of Leakages

- Leakage increases significantly as technology advances.
- Accurate modeling of various leakages in nanoscale devices is challenging.
- In today's MOSFETs, gate leakage current increases by orders for the decrease of Tox.
- Modeling of gate tunneling at channel quantization condition.









SiliconLinX
Bridging the gap between IC designers and foundries

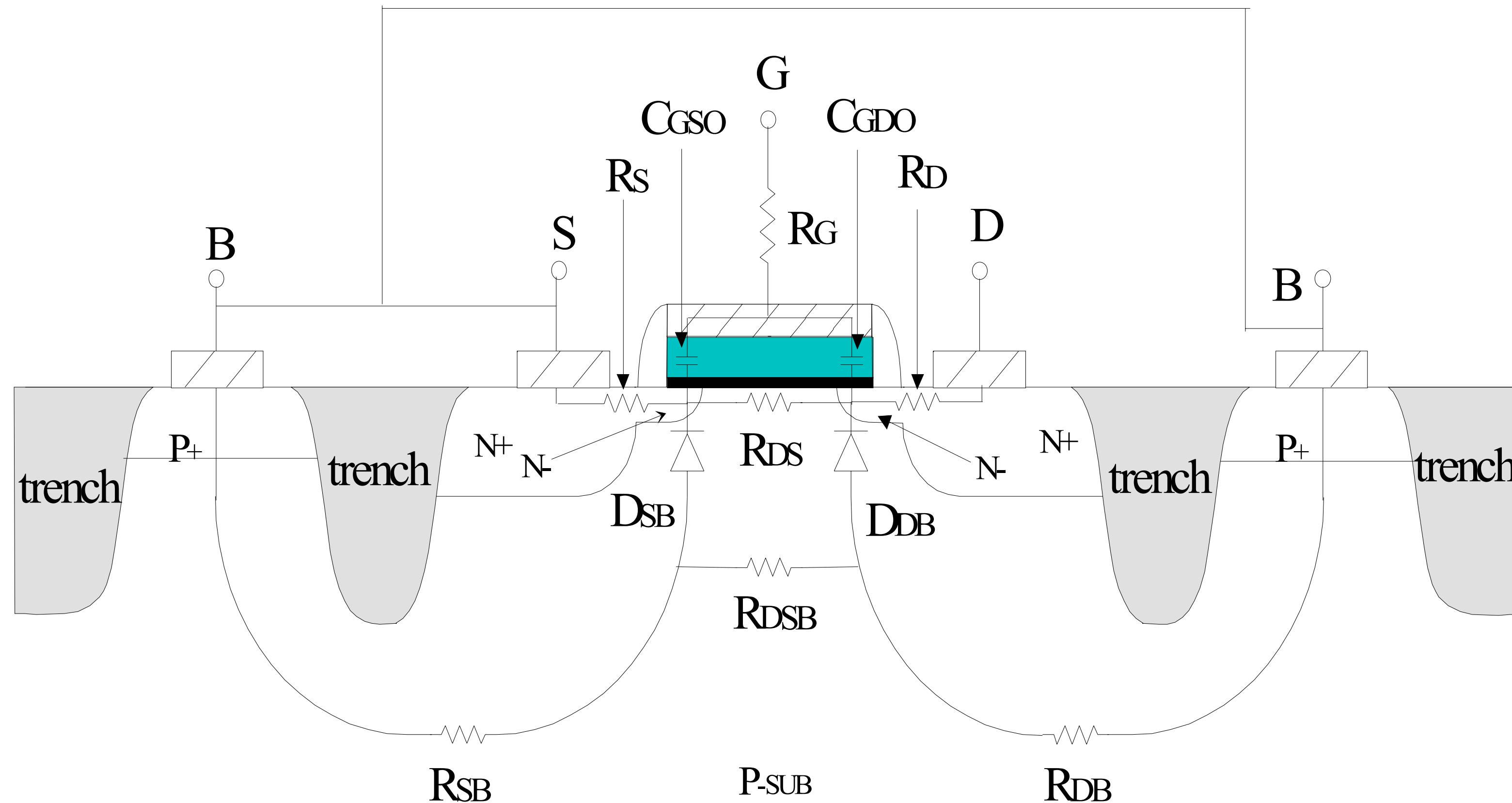
Modeling for RF Applications

- Modeling of MOSFET
- Modeling of passive devices (R, C, inductor,varactors)
- Modeling of special devices (LDMOS and PNP BJTs)
- Interconnect modeling
- Substrate modeling
- Statistical modeling

RF Modeling Challenges

- Modeling of all the physical effects in nano-scale transistors including those discussed previously.
- Modeling of flicker noise, and matching behavior etc for analog/RF applications.
- Core model with good continuity, accuracy and scalability over wide biases, temperatures and geometries.
- Scalable parasitic capacitance and resistance models.
- Non-Quasi Static (NQS) effects.
- Predict accurately the bias, frequency and temperature dependence of small signal AC, noise and non-linear and distortion behavior of the device at HF operation.

RF Modeling Challenges – Parasitics

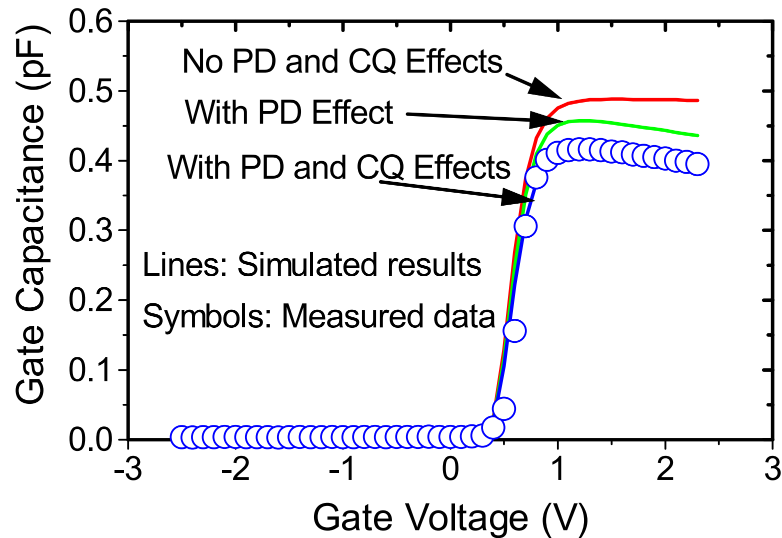


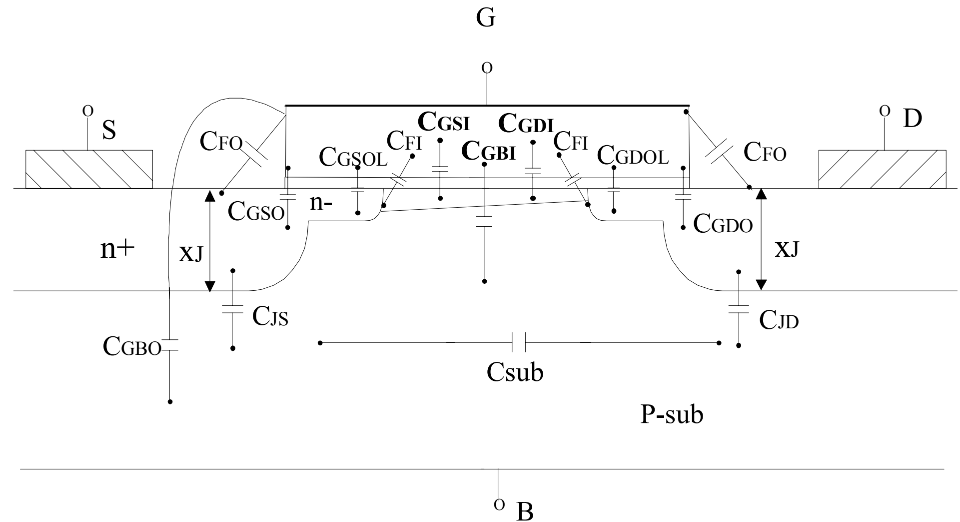
- In addition to the intrinsic core, many parasitic components exist.
- These parasitics play critical role at HF and need to be modeled.

Yuhua. Cheng

SILICON LINX
Bridging the gap between IC designers and foundries

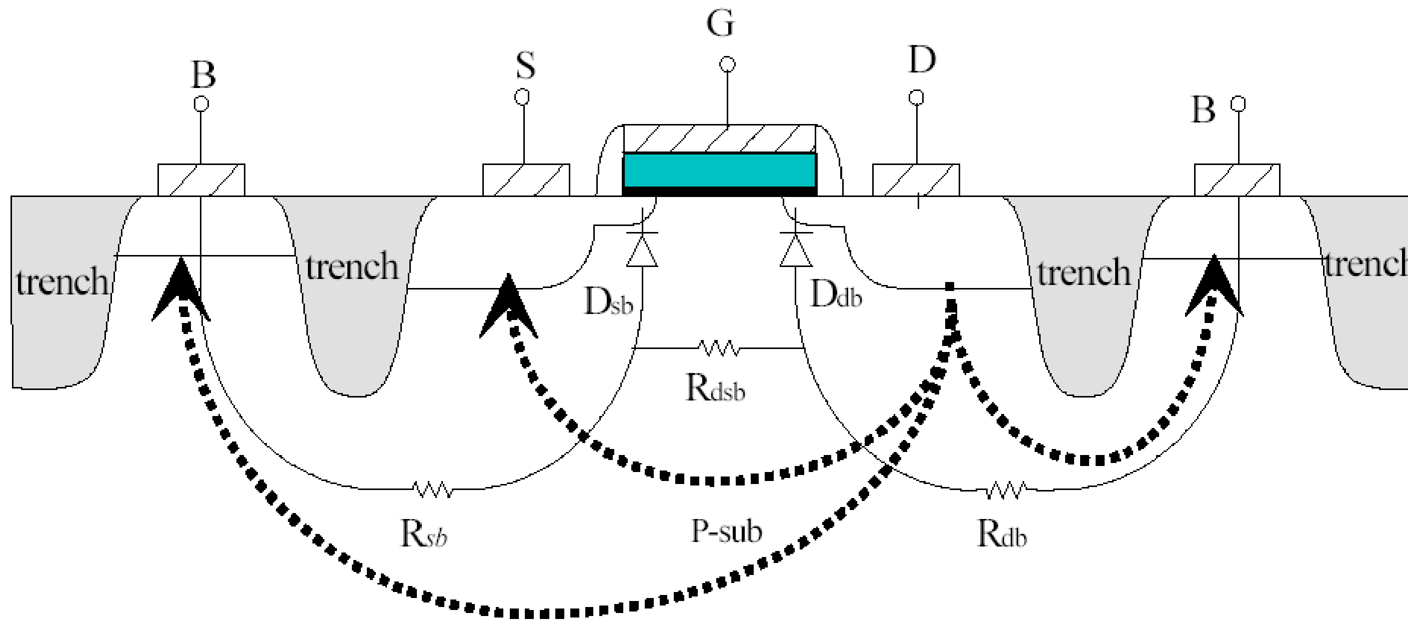
Modeling of Capacitance Characteristics



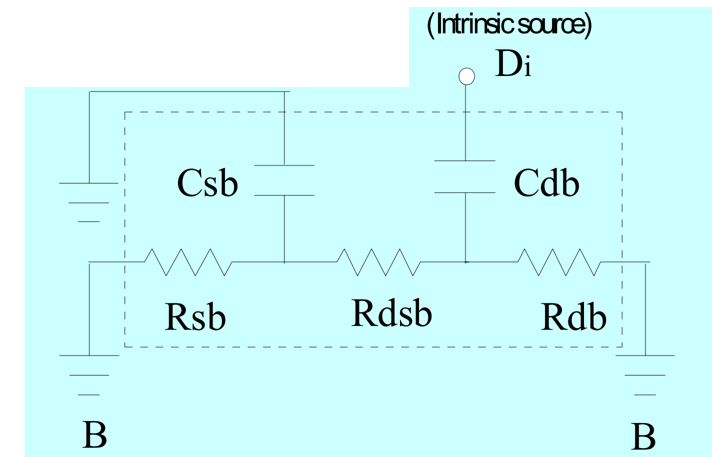


- Gate Capacitance is not constant in strong inversion.
- Bias dependence is caused by Poly-depletion effect.
- Both poly-depletion (PD) and channel quantization (CQ) effects will reduce Cgg.
- Extrinsic capacitance becomes critical, especially in 0.13 and below technologies.
- Csub can be ignored when f<10GHz.

Modeling of Substrate Coupling



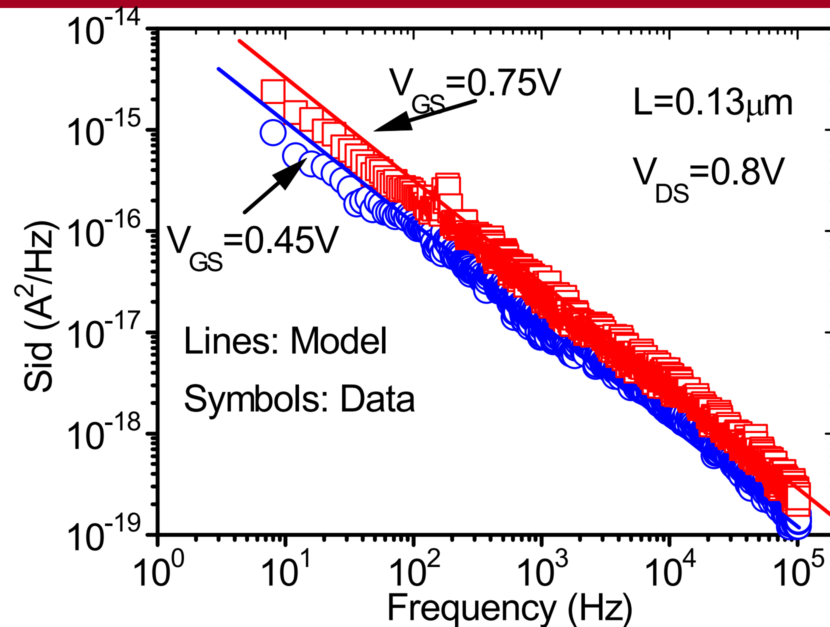
- At HF, signal is coupled to substrate through junction capacitance.
- This effect impact mainly the output impedance.
- Rsub should be scalable in terms of channel width, length and fingers.

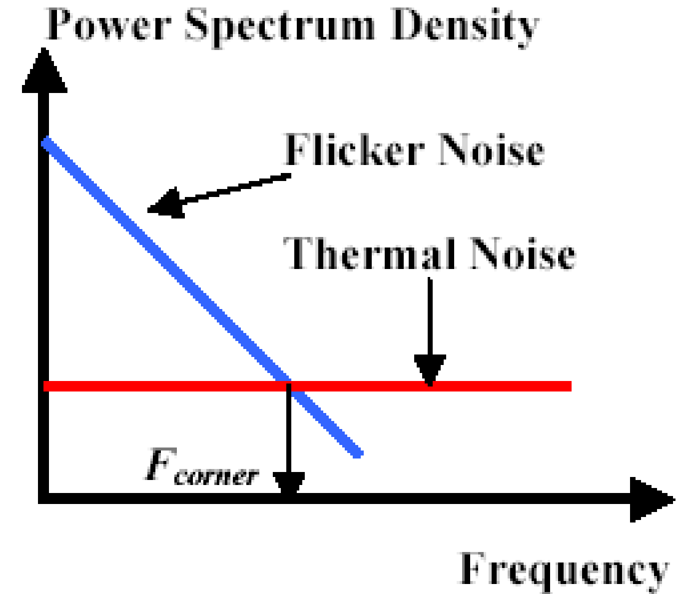


Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

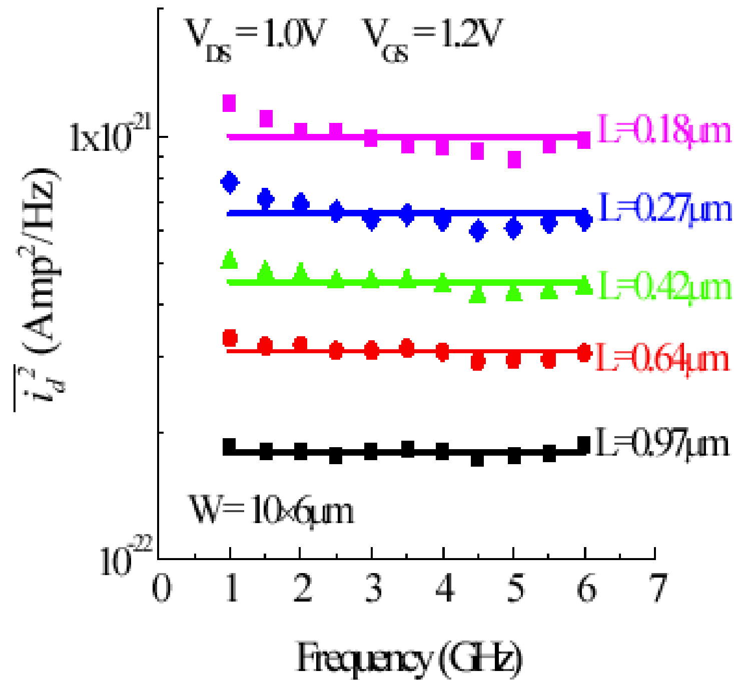
Modeling of Flicker noise

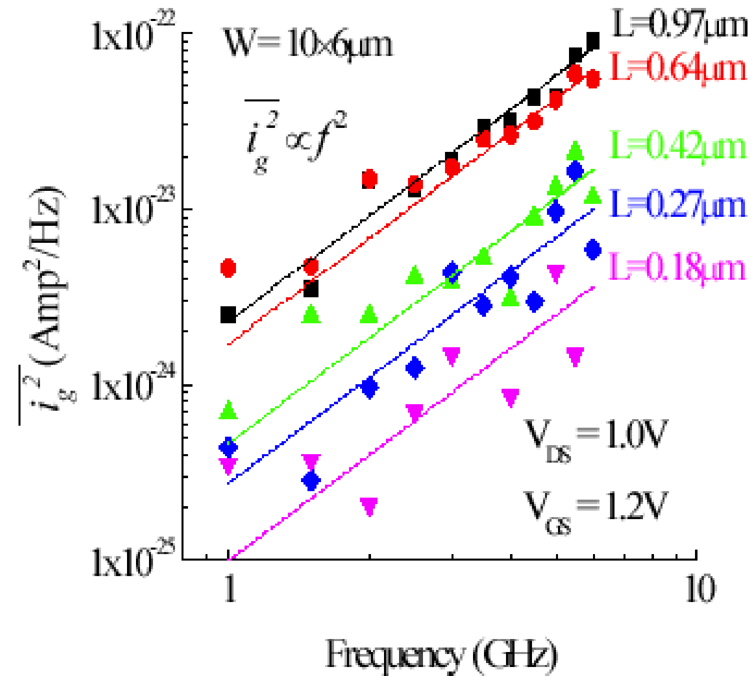




- It was reported that the channel quantization would impact the flicker noise behavior.
- Modeling of flicker noise in nano-scale devices becomes more challenging.
- Accurate prediction of corner frequency, Fcorner, is critical for circuit design.

Modeling of HF Noise



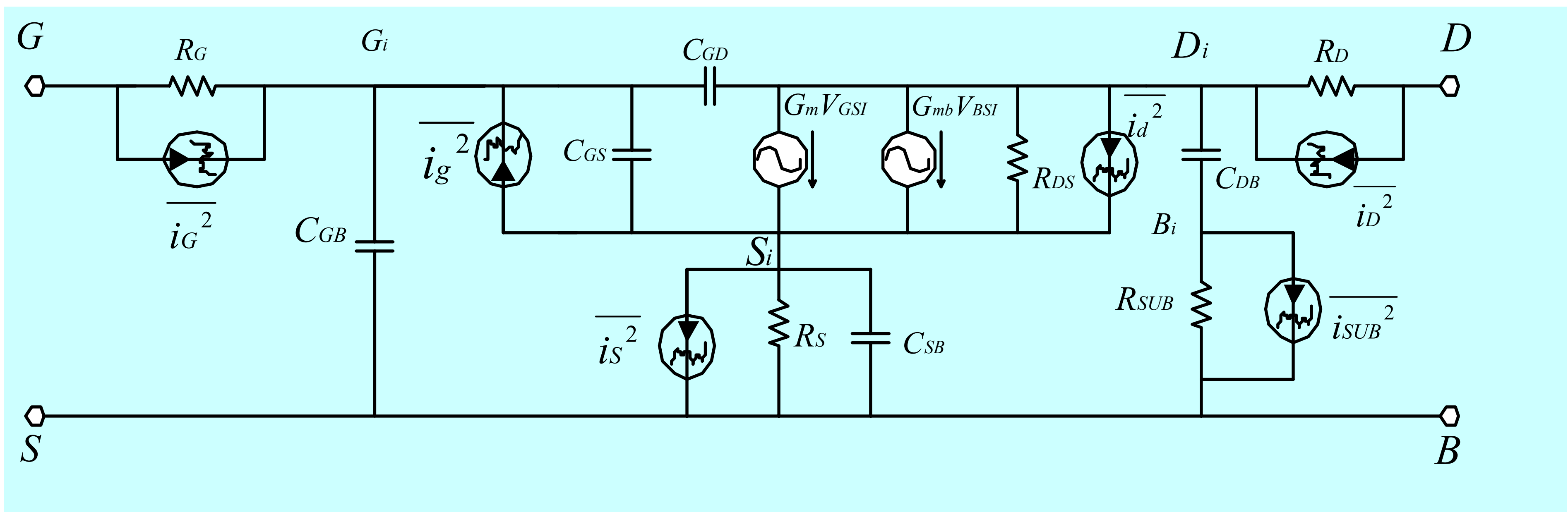


- Channel noise is frequency independent and induced gate noise is frequency dependent.
- Induced gate noise is not negligible in devices with long L or devices with short L but at very high frequency.

Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

Modeling Challenges - Noise Sources

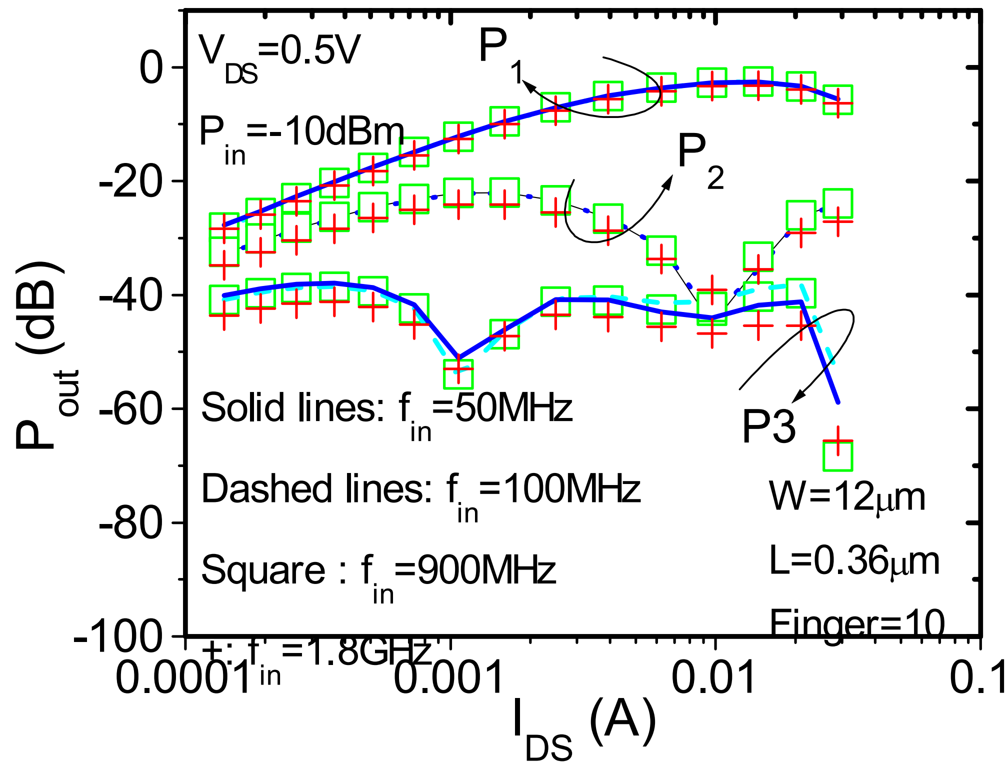


- Understanding of noise sources is important.
- Modeling of channel thermal noise and induced gate noise is the most challenging job.

Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

HF Device Behavior: High "Low Frequency Limit"

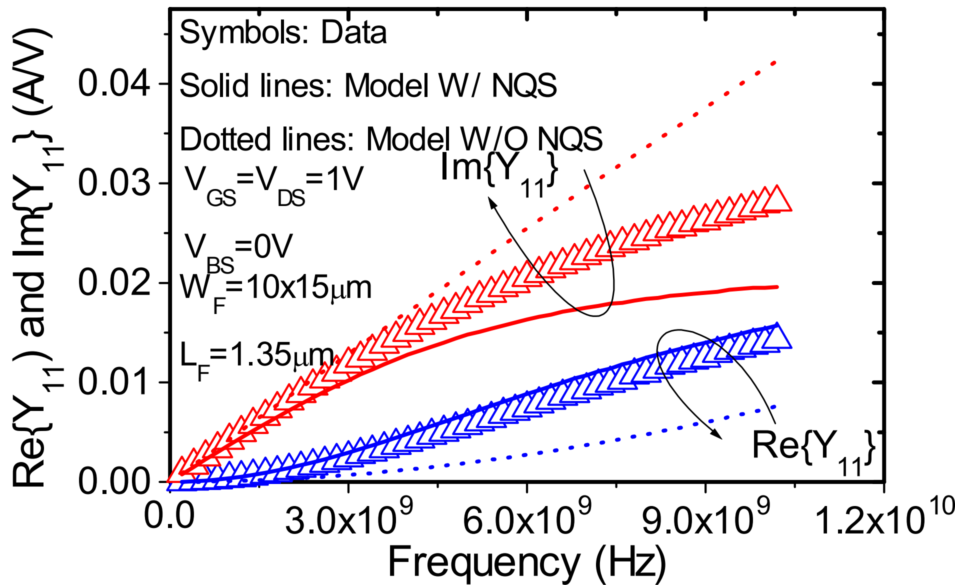


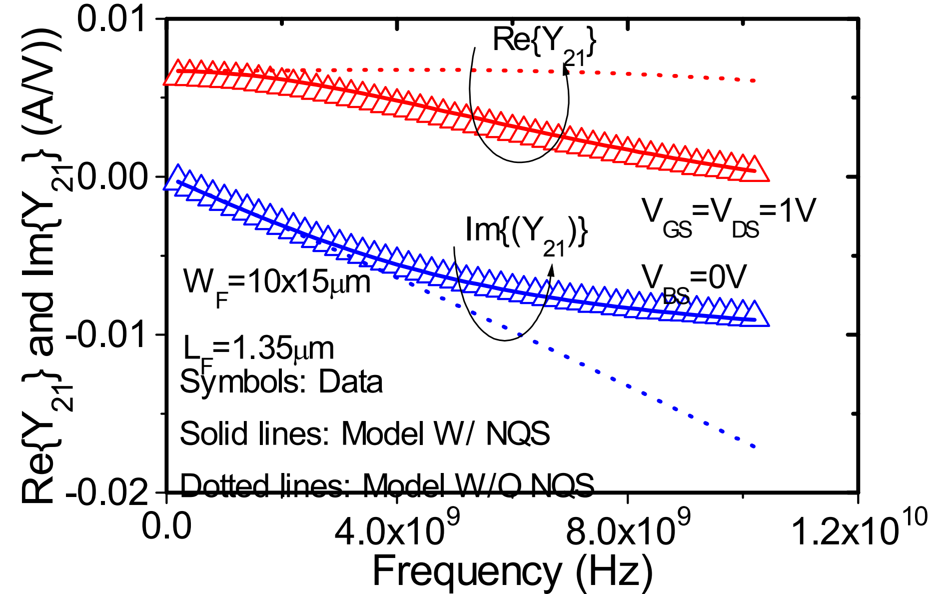
- MOSFET has much higher "low frequency limit" (LFL).
- HF distortion characteristics (<f_{LFL}) can be described by its low-frequency behavior.

Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

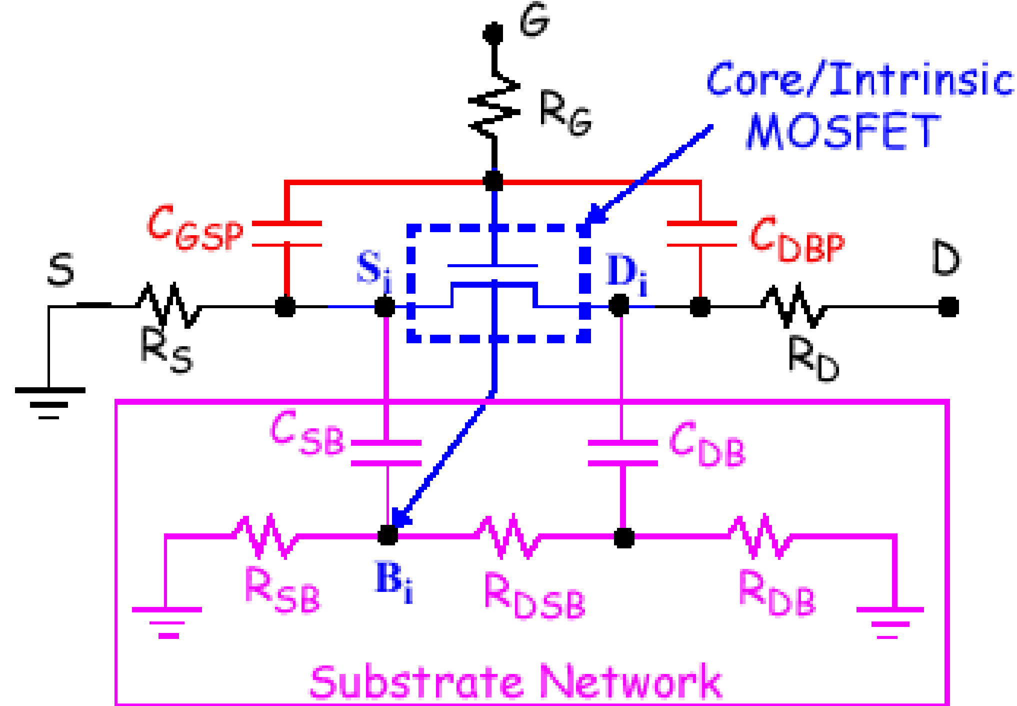
Modeling Challenges - NQS Effects





- NQS will significantly impact Y_{11} and Y_{21} behavior.
- Many approaches are proposed to model this effect:
  - Multi-segment approach.
  - Relaxation time.
  - Rg/Ri equivalent circuit approach.
- Efficient built-in NQS effect in intrinsic core model is preferred.

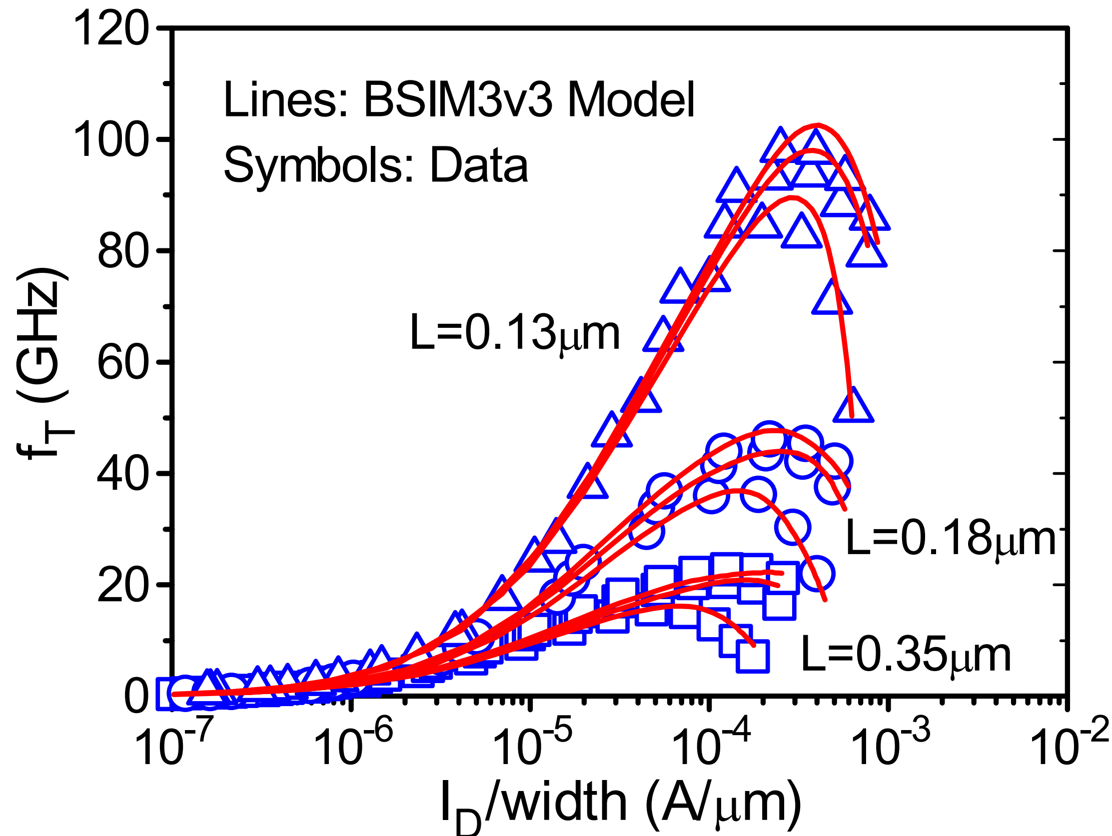
Subcircuit Model



- Important device physics are modeled in the core.
- All parasitic components should be scalable and extractable from measured data.

SILICONLINX
Bridging the gap between IC designers and foundries

f_T: Measured vs. Fitted

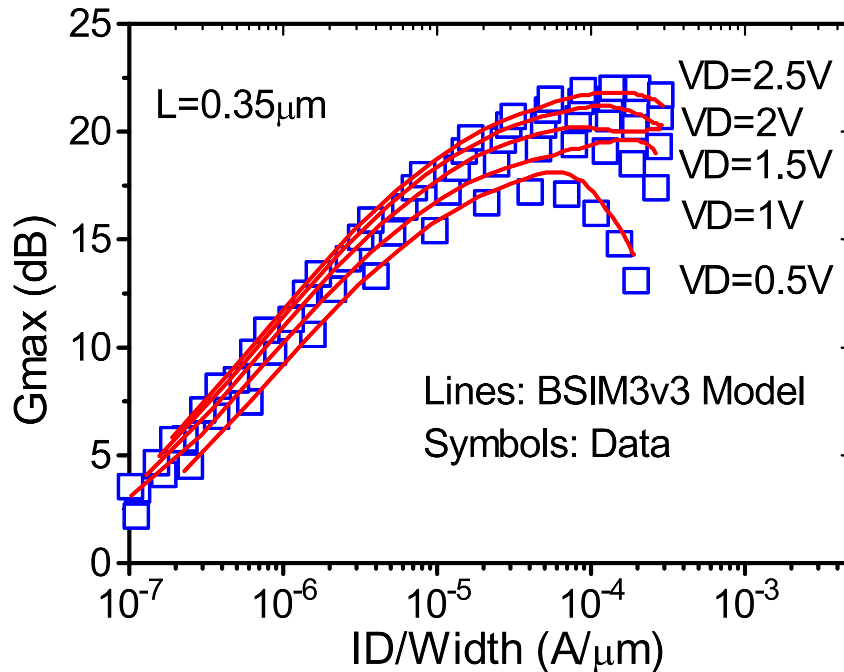


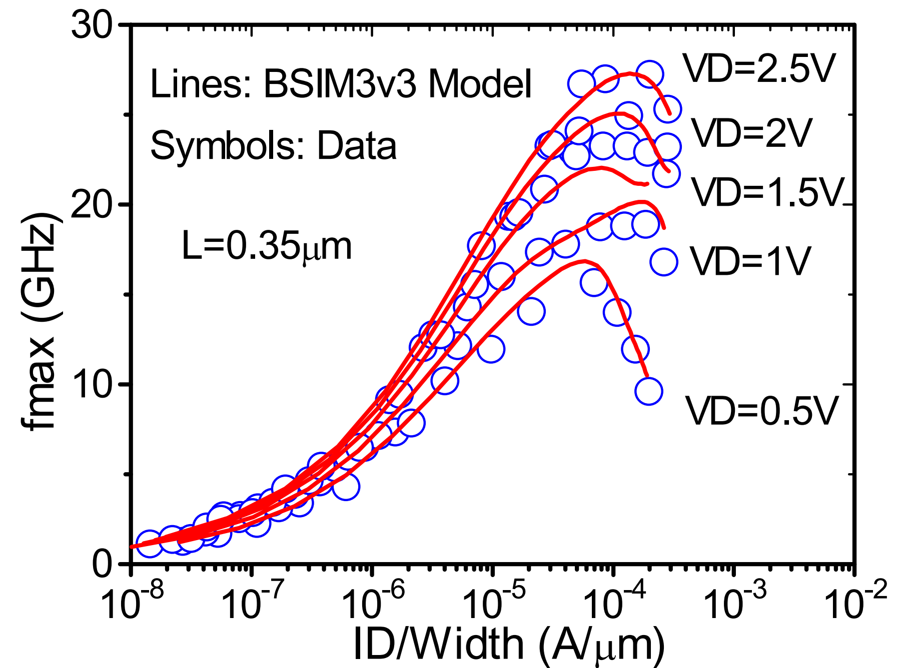
- A standard device parameter for model validation.
- However, only f_T is not enough to describe HF behavior of MOSFETs, especially at technology nodes such as 0.13um and below.

Yuhua. Cheng

SILICONLINX
Bridging the gap between IC designers and foundries

G_{max} and f_{max}: Measured vs. Fitted





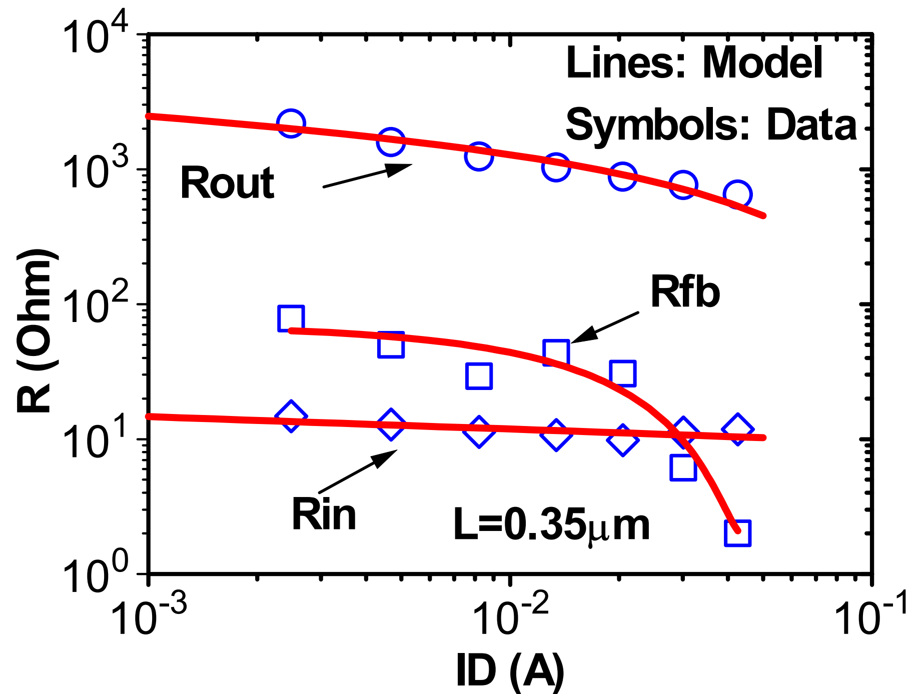
- f_{max} contains the impacts from parasitics such as gate and substrate resistance and is a better FoM than f_T

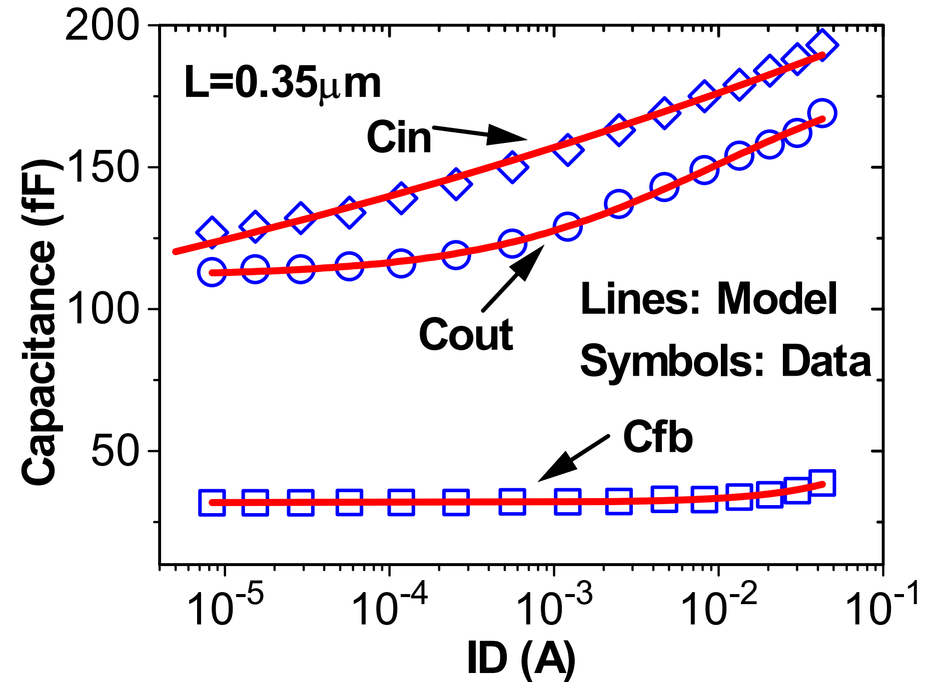
Yuhua. Cheng

SILICONLINX

Bridging the gap between IC designers and foundries

C-parameters: Measured vs. Fitted

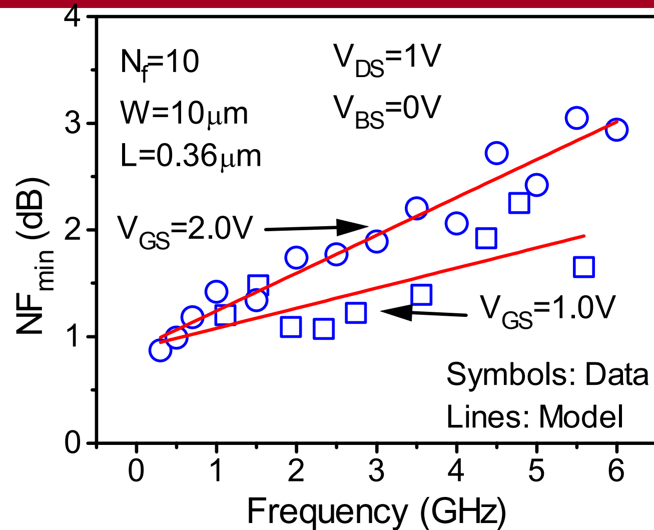


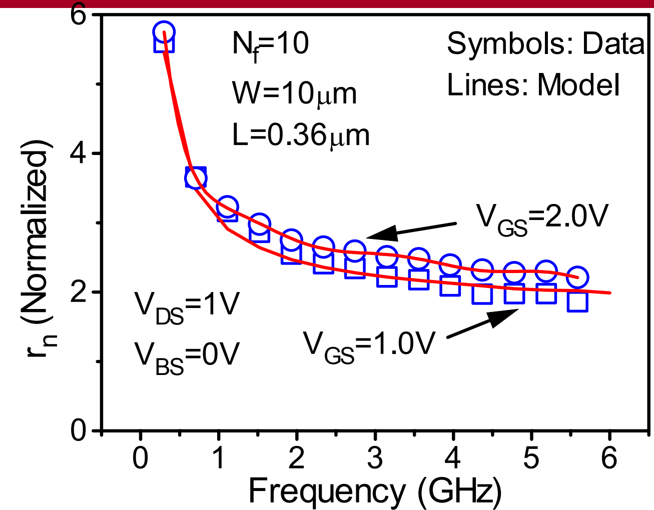


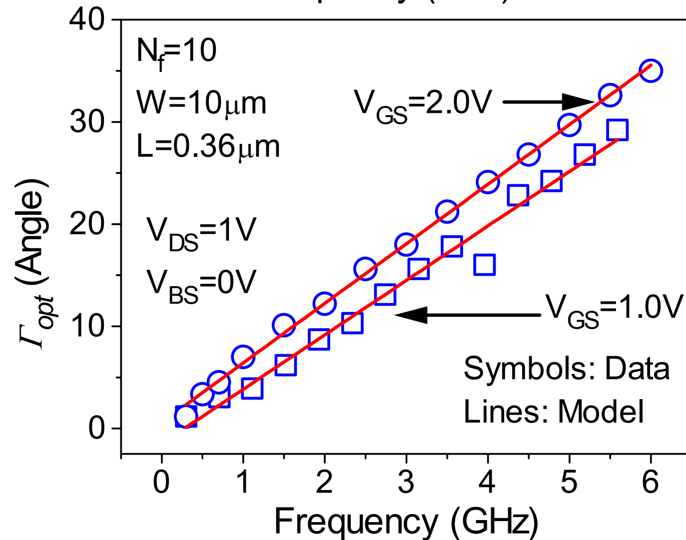
- C-parameters are more sensitive to the bias dependence of gate resistance and capacitance.
- Useful FoMs for model validation.

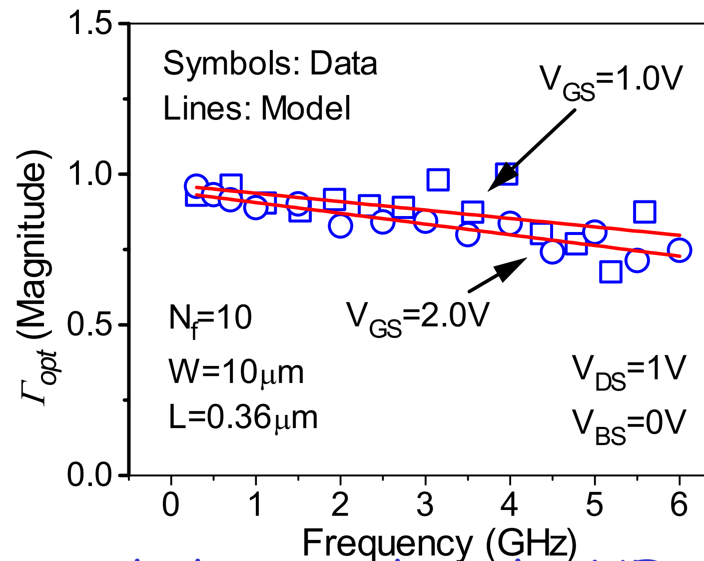
SILICONLINX
Bridging the gap between IC designers and foundries

HF Noise Parameters: Measured vs. Fitted







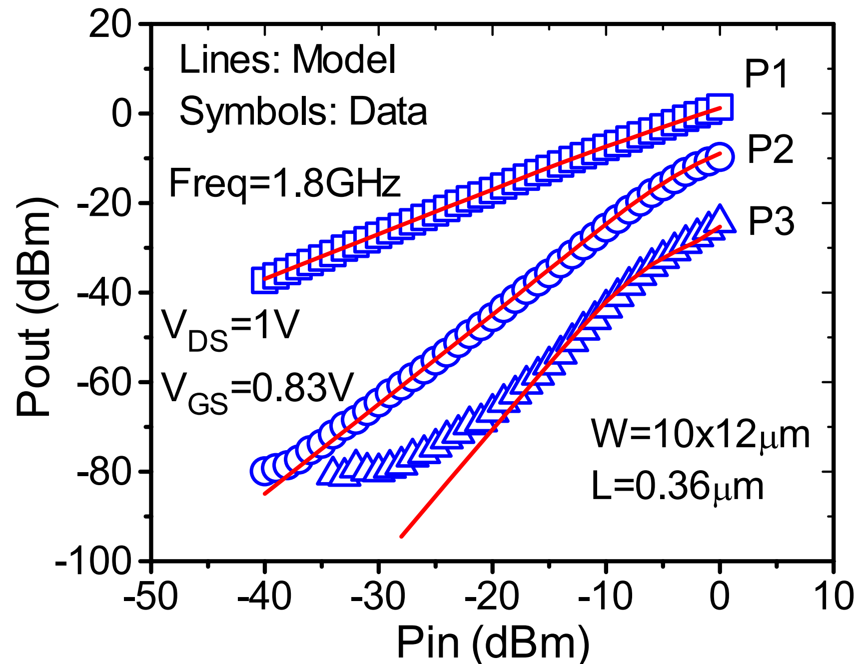


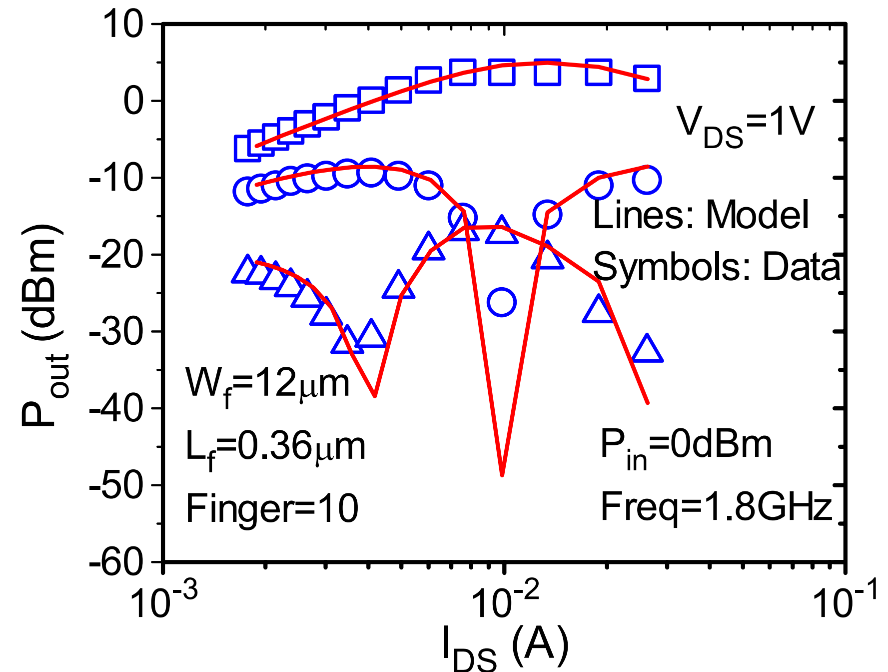
- Careful parameter extraction is needed to predict the HF noise parameters.

Yuhua. Cheng

SiliconLinX
Bridging the gap between IC designers and foundries

Large Signal Behavior: Measured vs. Fitted





- Below certain (the "LFL") frequency, the distortion behavior of MOSFETs is primarily determined by transconductance and capacitances.
- With careful parameter extraction at DC and HF small signal, a model can well predict the large signal distortion behavior.

Yuhua. Cheng

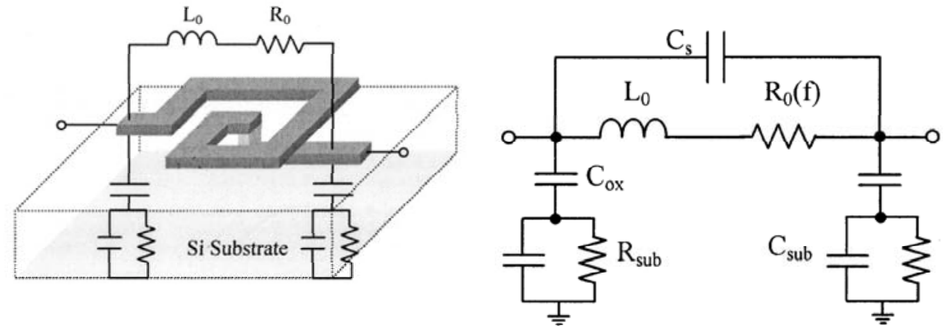
SILICONLINX
Bridging the gap between IC designers and foundries

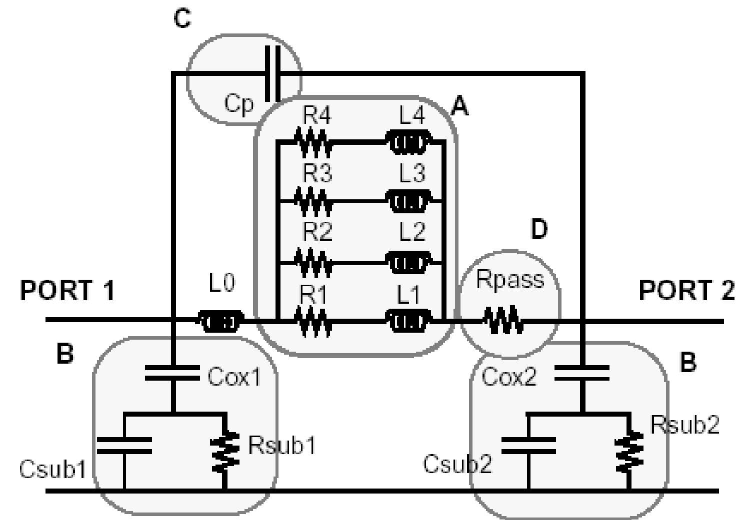
Statistical Modeling

- Process variation (even within a wafer) in today's advanced technologies becomes more significant.
- Need physical statistical models to predict process variation and local mismatch to optimize analog/RF circuits with high yield.
- Correlations between statistical modeling with considerations of both frontend and backend process variations and yield modeling/prediction should be developed.
- The model should include most important physical effects and the correlations based on independent process variables.

Example of Passive Device Modeling

- Inductor modeling is the m challenging effort for pass modeling.
- Lumped compact model is widely used in circuit simulation.
- Strong frequency dependenc of R and L components cause by skin and proximity effect should be modeled.
- An enhanced model with a resistor ladder to represent the distribution of current density and incorporate RF conduction loss.





SILICONLINX
Bridging the gap between IC designers and foundries

Summary

- While all the requirements for continuity, scalability, accuracy and computation efficiency need to be met for device models for circuit simulation, the new physical effects in nano-scale devices make compact model development very challenging.
- RF Modeling efforts such as HF noise and large signal distortion modeling, passive device modeling are also needed for RF circuit design.
- Advanced device modeling is critical and helpful to RF SOC design in nano-scale technologies.

Thank you for your attention

SiliconLinx
Bridging the gap between IC designers and foundries