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CMOS Scaling Limits and Nanoelectronic Devices

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Contents

- *Nanoelectronics, evolutionary "nano" and challenges*
- Metal gate/high K dielectrics and improvement of carrier mobility
- Integration density improvement, paradigm changes?
- Power consumption as the challenge
- "Wires and Tubes" as revolutionary "nano"
- What's beyond in revolutionary "nano"?
- What could possibly make the revolutionary "nano" real?
- Summary

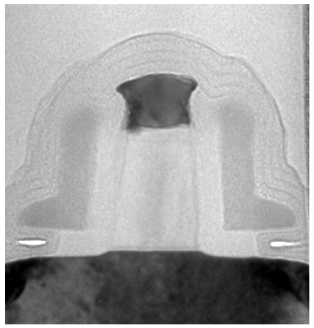
“Nano” electronic devices

- Evolutionary Nano
  scaled CMOS
  SOI
  GeMOS
  Strained CMOS
  FinFET

- Revolutionary Nano
  CNT
  Nanowires
  Molecular electronics
  Spintronics

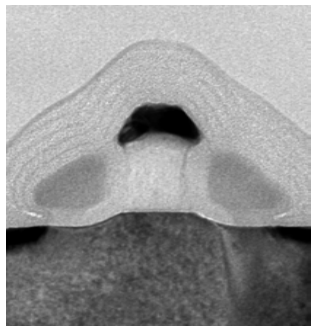
Evolutionary Silicon CMOS

90 nm node
2003



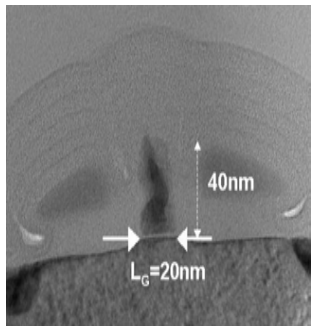
50 nm length
(IEDM 2002)

65 nm node
2005



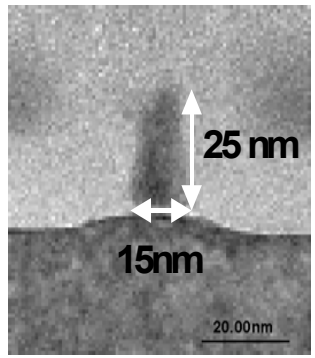
30 nm prototype
(IEDM 2000)

45 nm node
2007



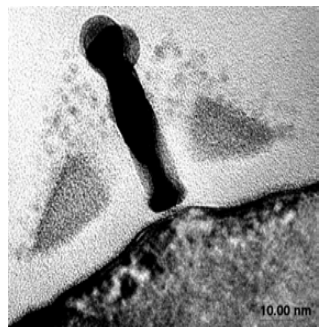
20 nm prototype
(VLSI 2001)

32 nm node
2009



15 nm prototype
(IEDM 2001)

22 nm node
2011



10 nm prototype
(DRC 2003)

Planar Si CMOS will scale down to ~10 nm L_{GATE}

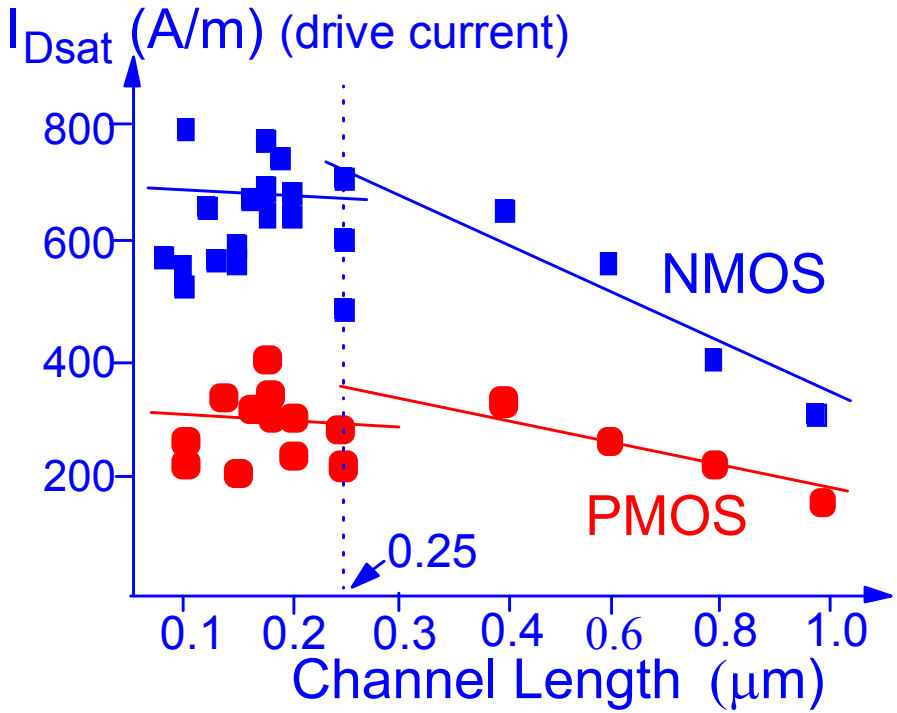
Will performance and leakage be what we need?

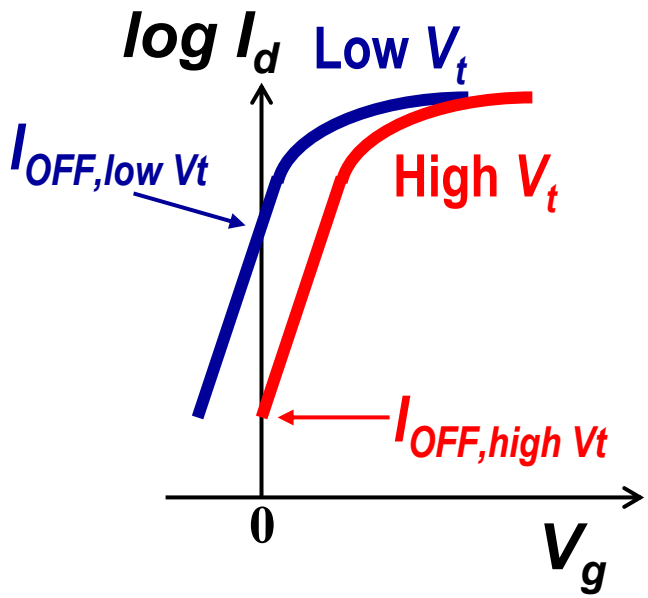
Mark Bohr

What conditions made sequential growth of IC manufacturing?

- Planar technology for precise control of positions in two dimensional plane, enabling the Moore's Law
- Ion implantation for vertical control of impurity profiles
- Film deposition and etching enabling vertical scaling
- CD control within 10% of minimum geometry
- Clean technology resulting in defect density control for over 85% yield for 10^9devices on chip.
- Every new technology node enabled 30-50% cost reduction per bit or gate over previous node
- Highly controlled environment for credible statistical data acquisitions

Saturation of I_{dsat}

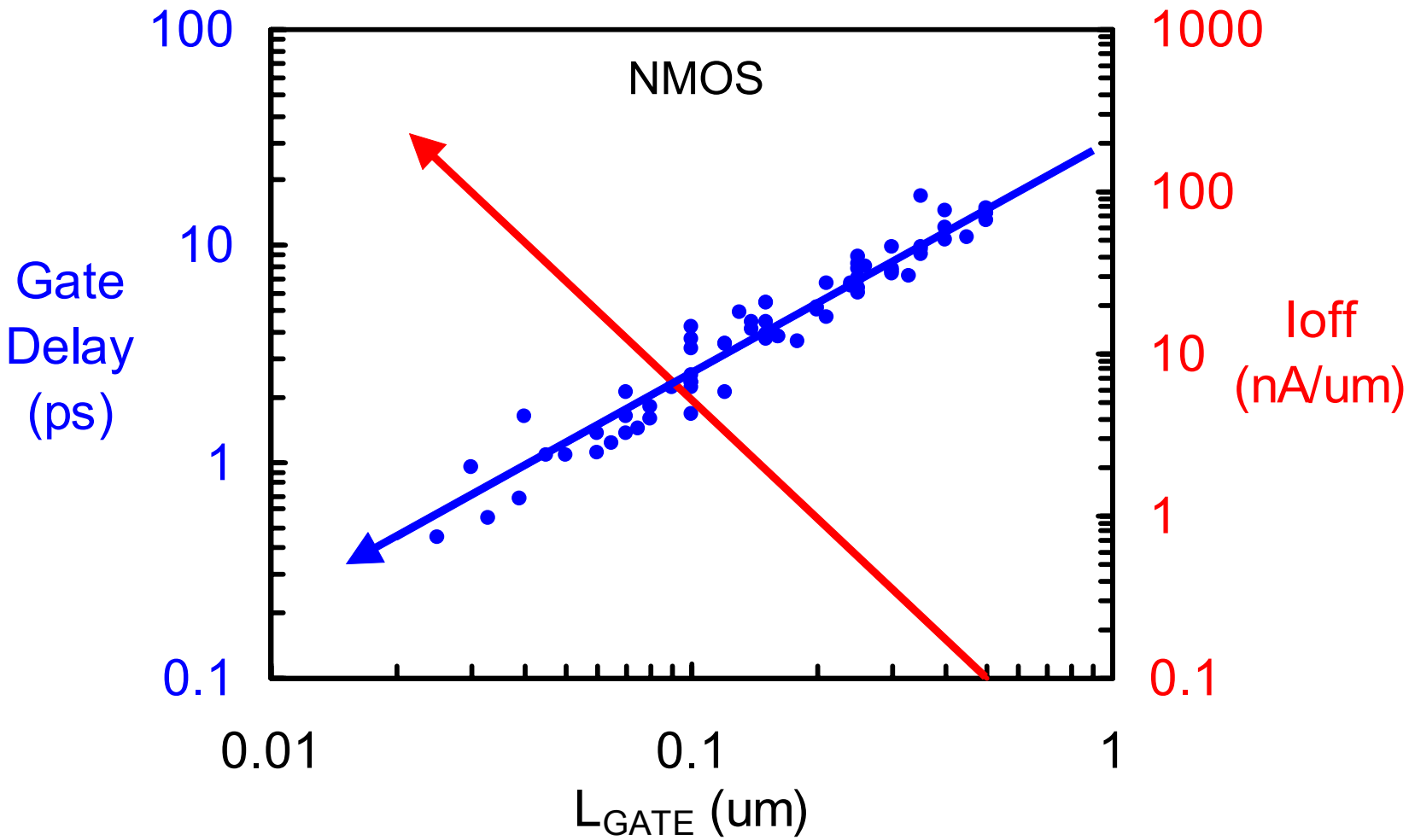




- I_{Dsat} data from IBM, TI, Intel, AMD, Motorola and Lucent for constant I_{OFF}
- Low V_t is desirable for high ON current: $I_{dsat} \propto (V_{dd} - V_t)^{\eta}$
- High V_t desirable for low OFF current:

Changhoon Choi, PhD Thesis in Dutton Group, Stanford Univ., 2002

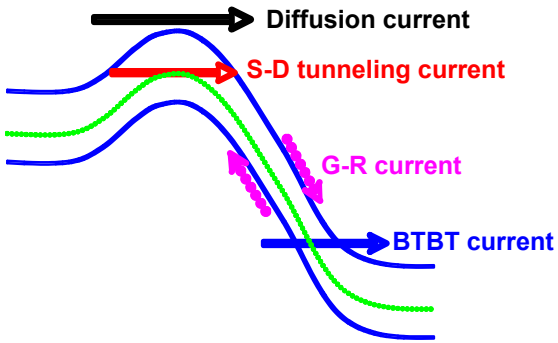
Transistor CV/I Delay and Leakage Trends



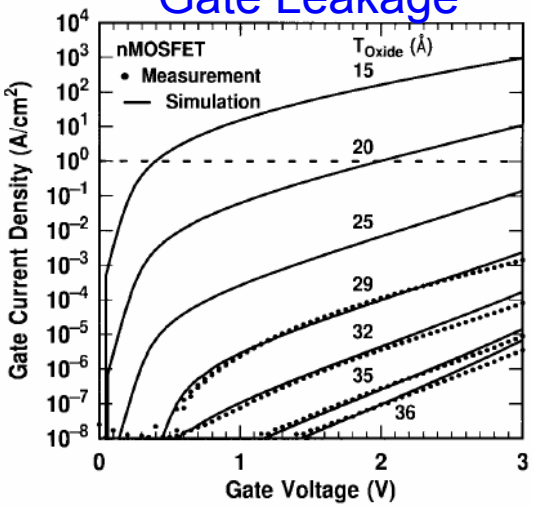
Continued gate delay reduction, but at the expense of leakage current

MOSFET Scaling Limit: Leakage

S/D Leakage

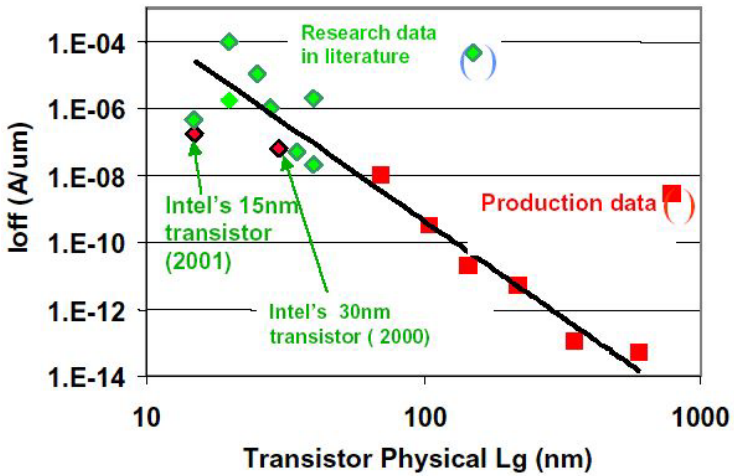


Gate Leakage

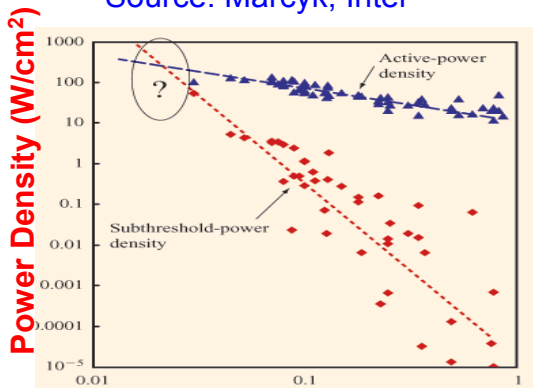


Lo et al.,IEEE EDL, May 1997.

Leakage Trend

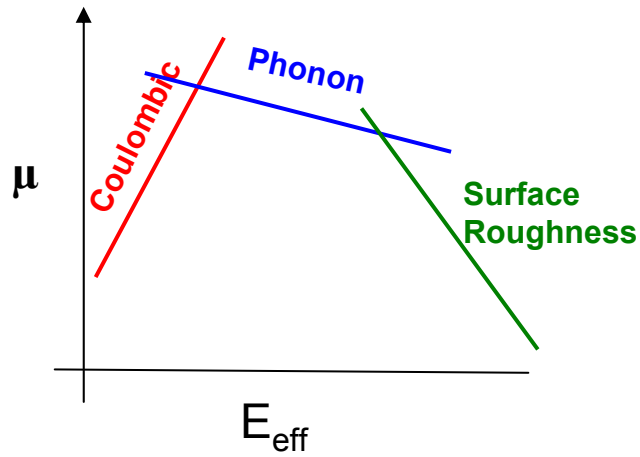


Source: Marcyk, Intel



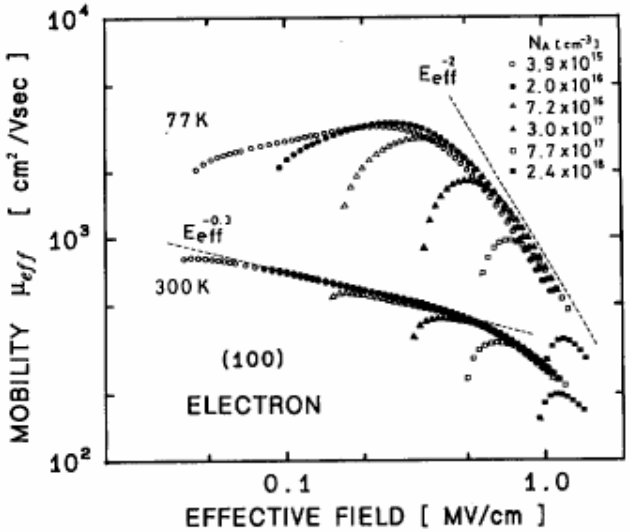
- **Ability to control I_{off} will limit gate-length scaling**
  - **Thermionic emission over barrier**
  - **QM tunneling through barrier**
  - **Band-to-band tunneling from body to drain**
- **To suppress D/S leakage, need to use:**
  - **Higher body doping to reduce DIBL**
    - **⇒ lower mobility, higher junction capacitance, increased junction leakage**
  - **Thinner gate dielectric to improve gate control ⇒ higher gate leakage**
  - **Ultra-shallow S/D junctions to reduce DIBL ⇒ higher R_{series}**

Effects of Scaling Bulk MOSFET on Mobility



$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}$$

$$E_{eff} = \frac{q}{\varepsilon_{Si}}(N_{dep} + \eta \cdot N_{Channel})$$



S. Takagi *et al.*, *IEEE TED*, **41** (1994) 2357.

N_{dep}= depletion charge density
$N_{Channel}$ = charge induced in the channel

- **Increases in substrate doping ⇒ N_{dep} ⇑**
- **Gate oxide thickness decrease ⇒ $N_{Channel}$ ⇑**
- **E_{eff} increases with scaling ⇒ μ ⇓**
- **Reduced gate oxide thickness increases remote charge scattering ⇒ μ ⇓**
- **High k dielectrics have higher coulombic scattering due to surface states and soft phonon scattering ⇒ μ ⇓**

Key questions to evolutionary "nano"

- How far can "scaled CMOS" go?
- Would the rate of increase in Idsat hold?
- What can possibly allow us to break "the curse of universal mobility"?
- Is there any trick to maintain s-factor for low Ioff?

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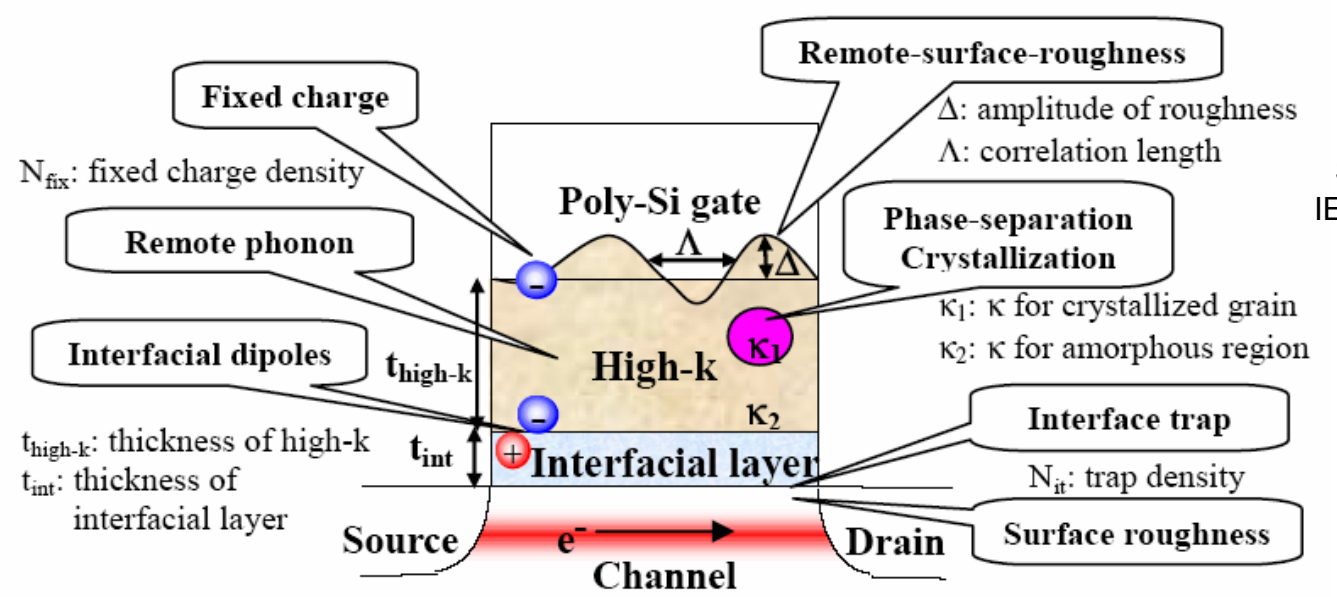
Issues With High k Dielectrics



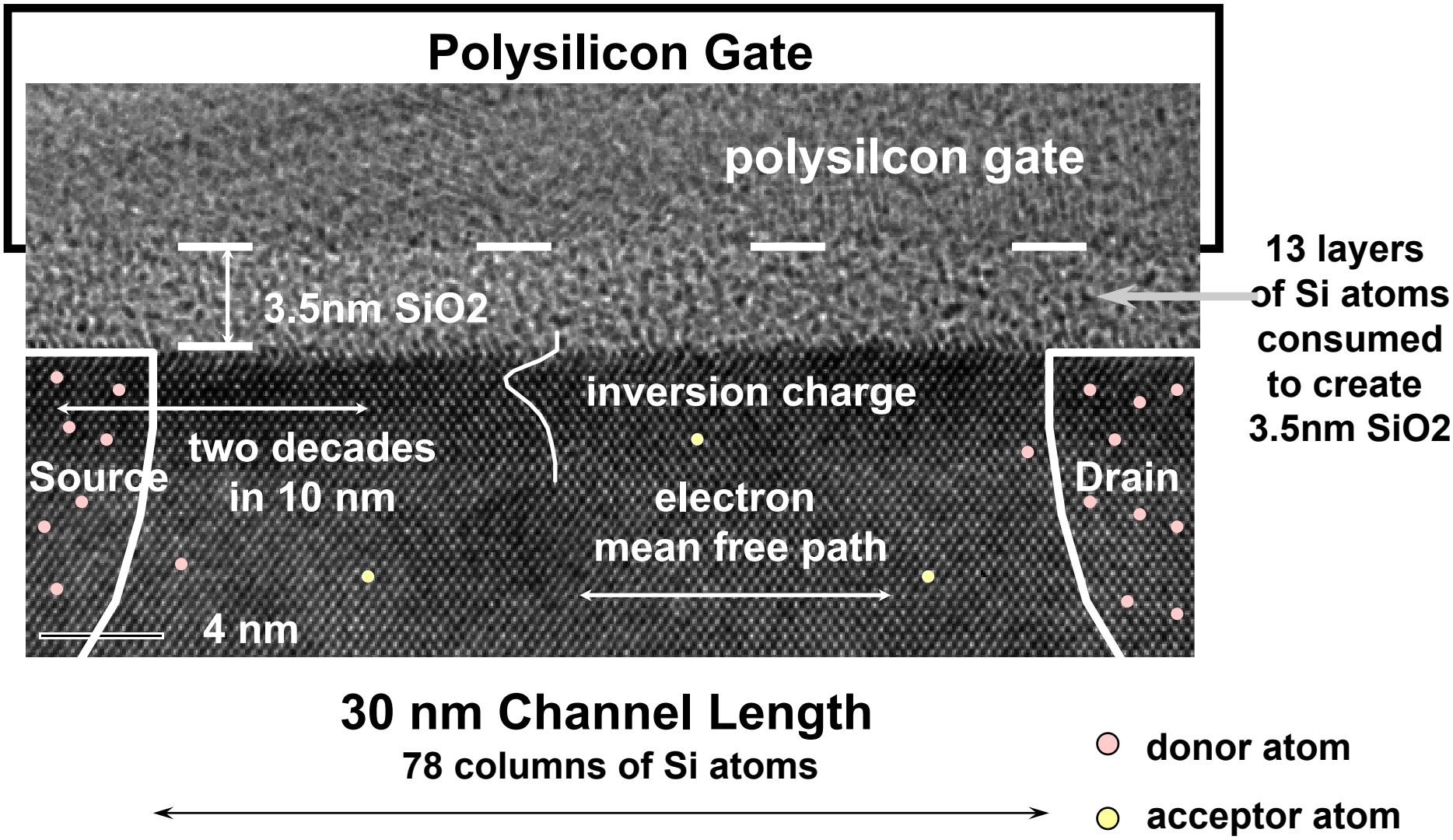
S. Saito, et al., IEEE IEDM 2003.

- **Bulk and interface traps and charges ⇒ mobility, reliability**
- **Contamination of Si by metal atoms**
- **Compatibility with gate electrode ⇒ metal gate**
- **High temperature stability**
- **Minimum EOT achievable**
- **Technology integration**

Extensive research is needed to understand these mechanisms and how to minimize their impact on device performance

High Resolution TEM showing 0.03 μm Channel Length

Richard Chapman

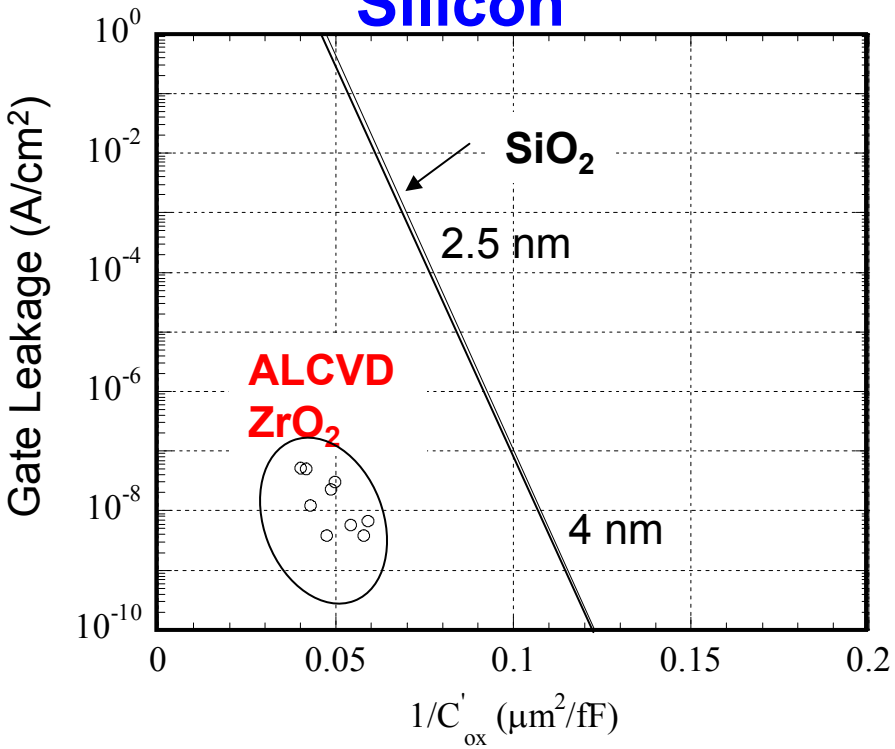


Metal gate and high K

- Avoid poly depletion/remote charge scattering and reduce ionized impurity scattering in channel: *metal gate*
- Reduce gate tunneling: *high K*
- Suppress soft phonon scattering caused by softer metal-oxygen bond: *metal gate & high K*
- Need “workfunction engineering”: *metal gate*

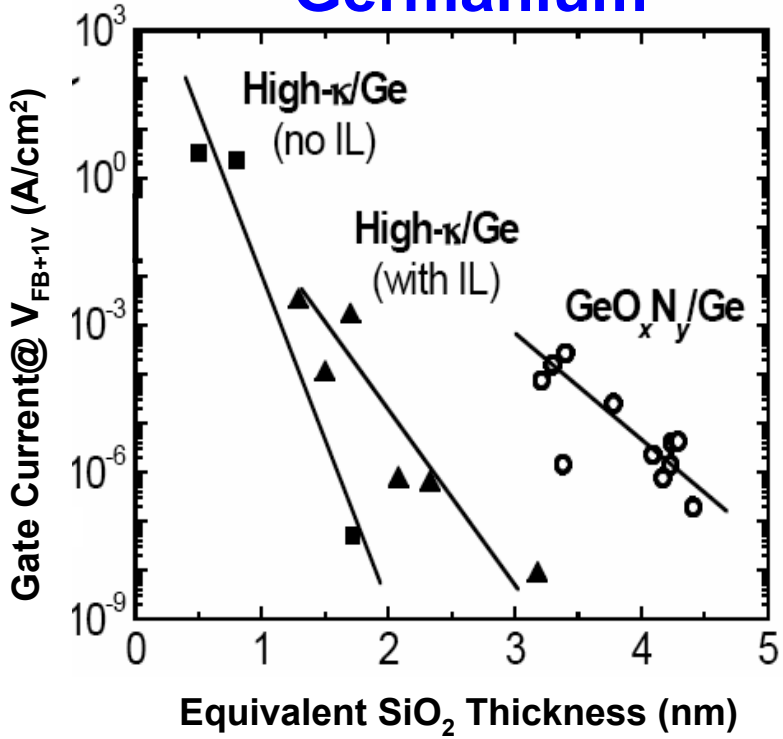
Capacitance and Leakage for High-k Gate Dielectric Films Grown Using ALCVD

Silicon

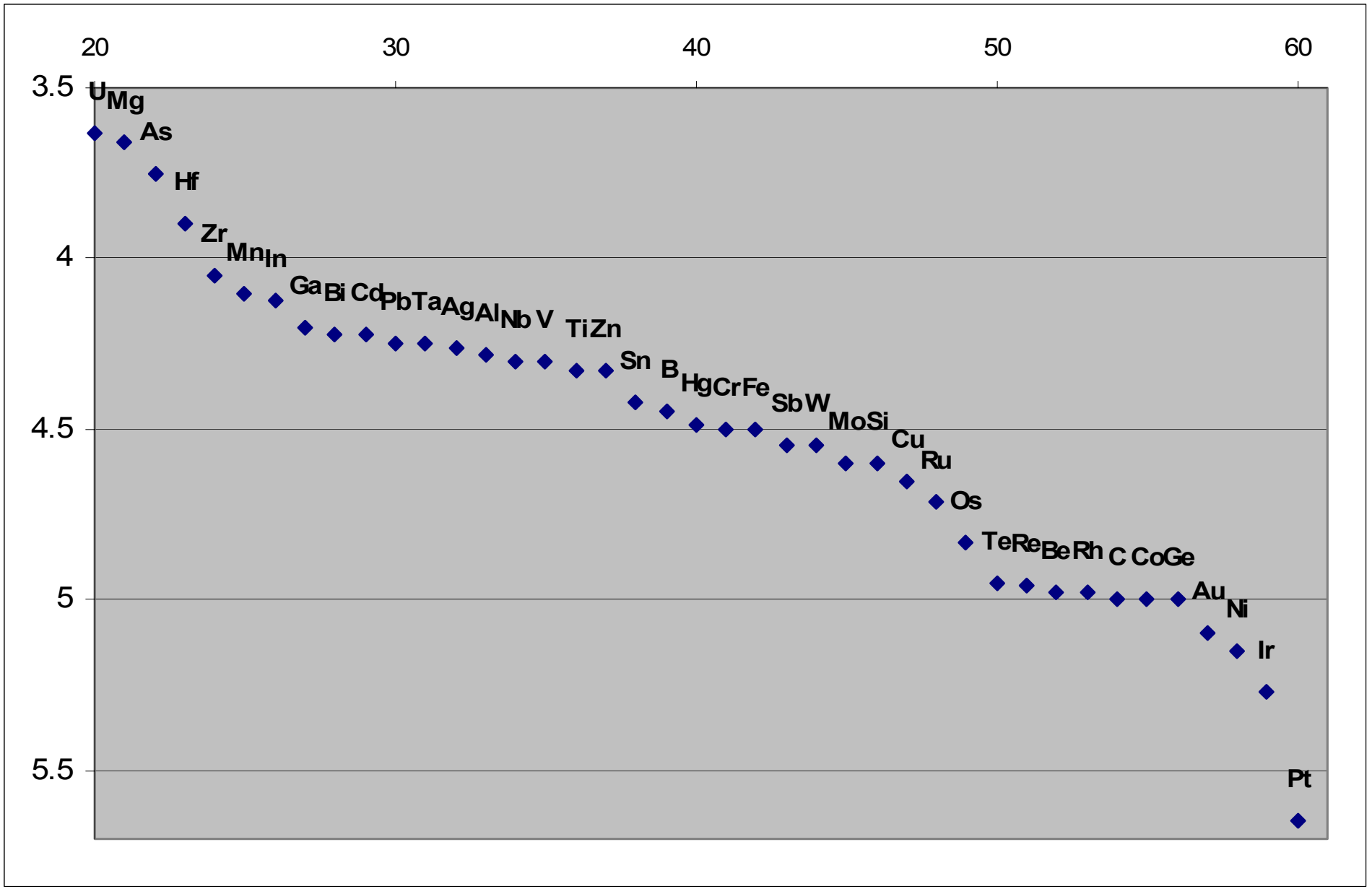


Perkins, Saraswat and McIntyre,
Stanford Univ. 2002

Germanium



Chui, Kim, Saraswat and McIntyre,
Stanford Univ. 2004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Ru
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Te
Re
Be
Rh
C
Co
Ge
Au
Ni
Ir
Pt

Approaches for Workfunction Tuning (INMP)

Gate structure	Examples	Adjustable workfunction	Issues
Dual metal* 	Ti/Mo; Ti/Ni	None	Etch damage
Alloy** 	Ta/Ru	~ 0.8 eV	Non-uniform degree of alloying, toxicity
Implanted metal* 	TiNx, Mo	~ 0.4 eV	Dielectric damage
silicide*** 	NiSi; TiSi	~ 1 eV	Dopant penetration
Bilayer 	Al/Ni; Ti/Pt; Al/TaN	~ 1 eV	Thermal stability

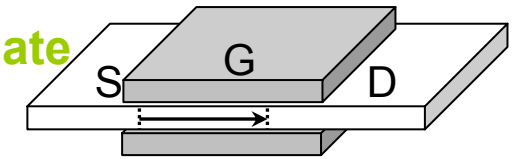
*King, UC Berkeley

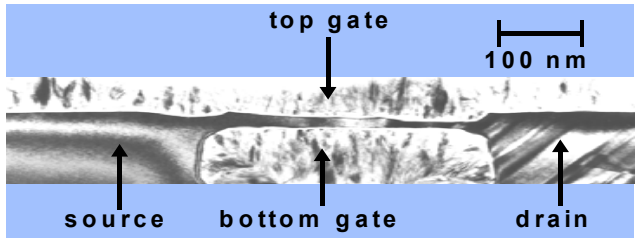
**Misra, NC state University

***Patrick, UC Berkeley

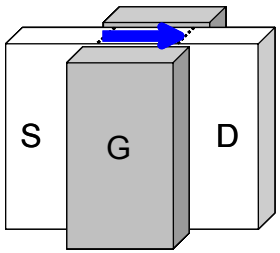
Electrostatic: Double-Gate Transistor Structures

Double Gate SOI





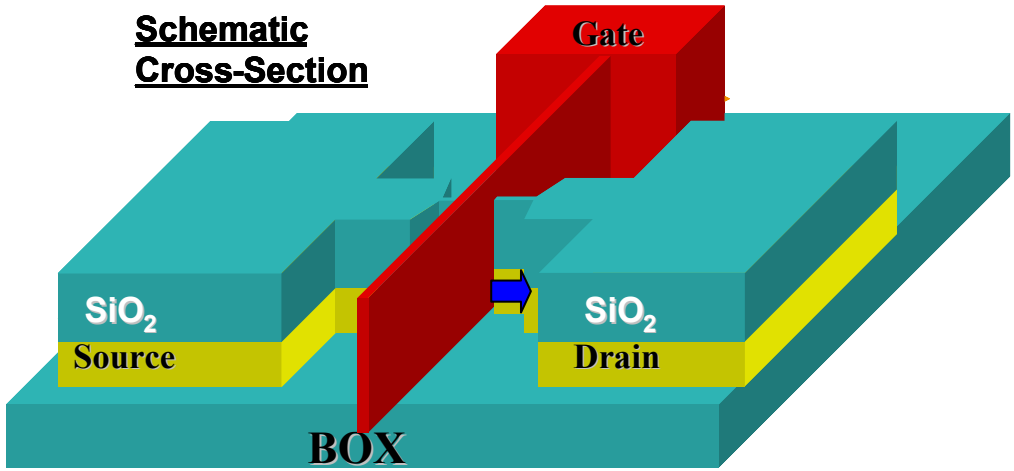
IBM '97



FinFET

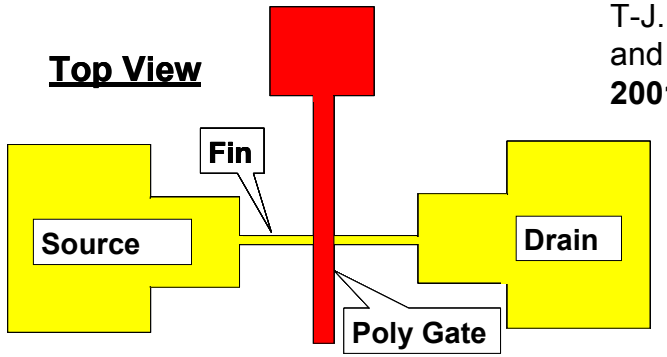
Simplified view of FinFET (one type of double-gate MOSFET)

Schematic Cross-Section



Key advantage: relatively conventional processing, largely compatible with current techniques

Top View

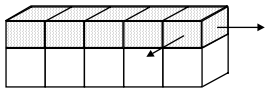


T-J. King and C. Hu, UC/Berkeley and Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

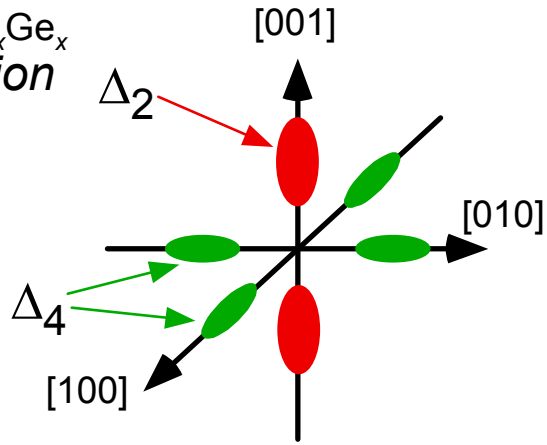
Transport: Effects of Biaxial Tensile Strain on Si Energy Bands

Hoytt, 2002

Strained Si grown on Relaxed $Si_{1-x}Ge_x$



biaxial tension

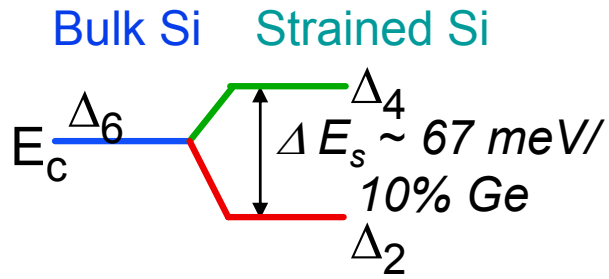


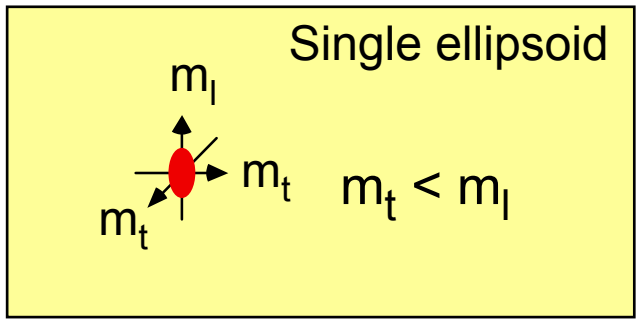
Conduction Band

Additional splitting:➔
Band repopulation

- reduced intervalley scattering
- smaller in-plane effective transport mass

$$\mu = q\frac{\tau}{m_c^*}$$

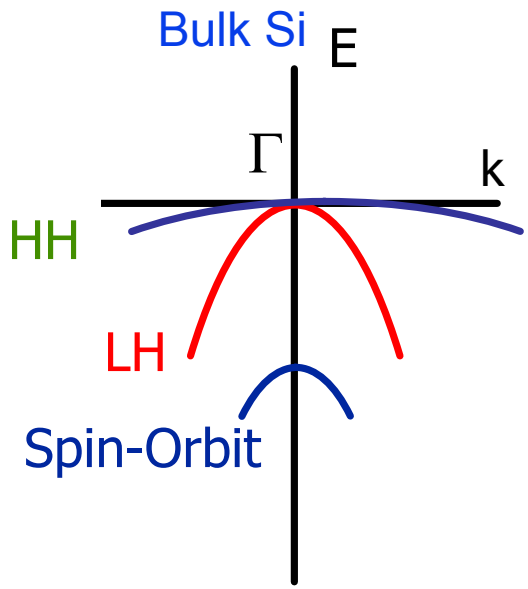


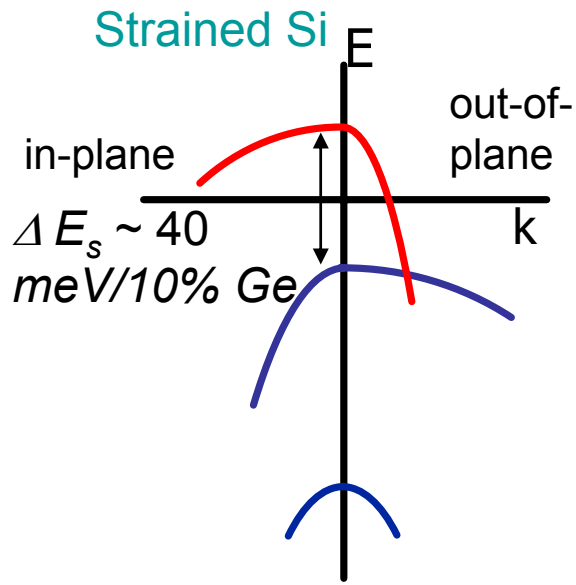


Valley Band

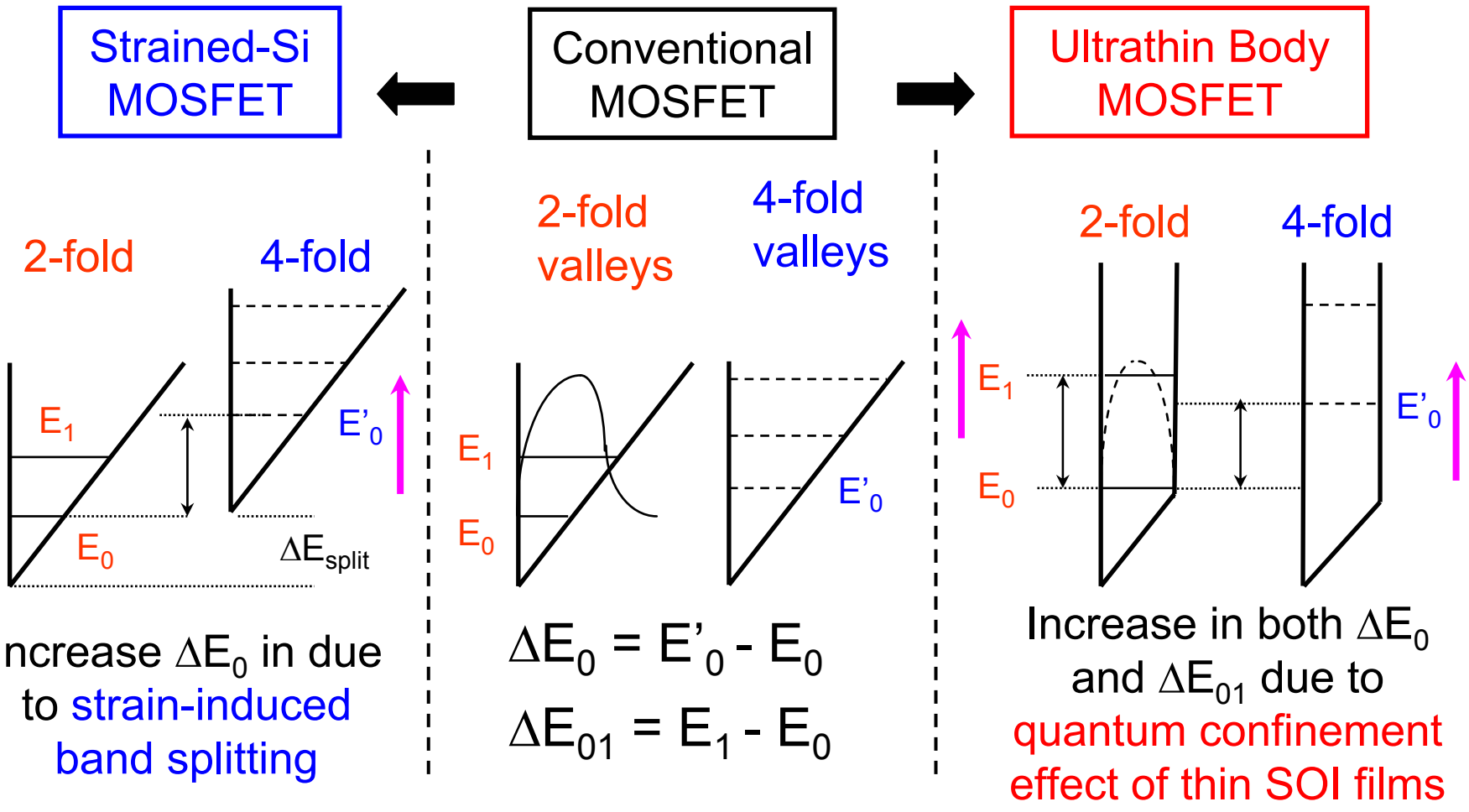
HH/LH degeneracy lifted at Γ

- reduced interband scattering
- smaller in-plane transport mass due to band deformation





Sub-band Structure Engineering



S. Takagi, May 2003 at Stanford

What about carrier transport in ultra short channel MOSFET

"Electrons will not reach saturation velocity before reaching the drain."

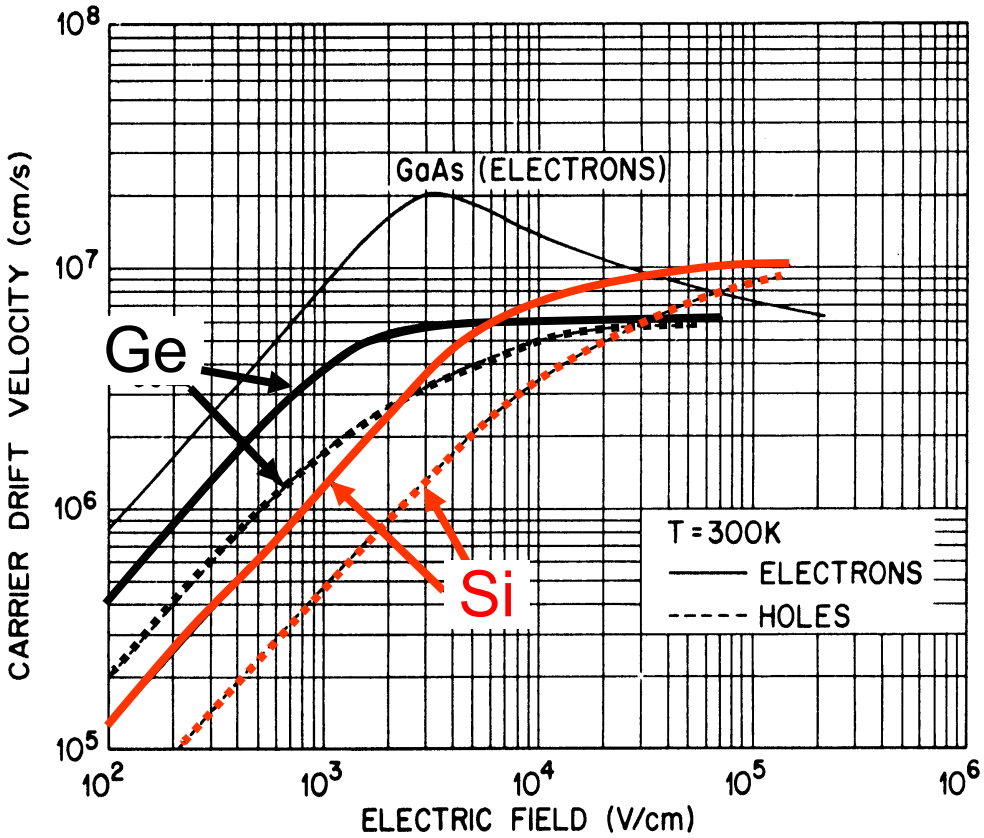
Change in transport mechanism

As the channel length becomes in the range of ballistic transport:

- Initial velocity is more important than the saturation velocity: “low field mobility” plays major role
- Carrier scattering mechanisms by surface roughness, remote charges, surface phonons still remain important
- Charge injection efficiency from the source: another key for the performance

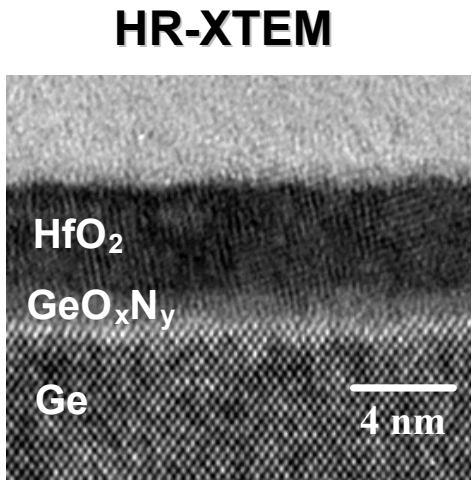
Why Germanium MOS Transistors?

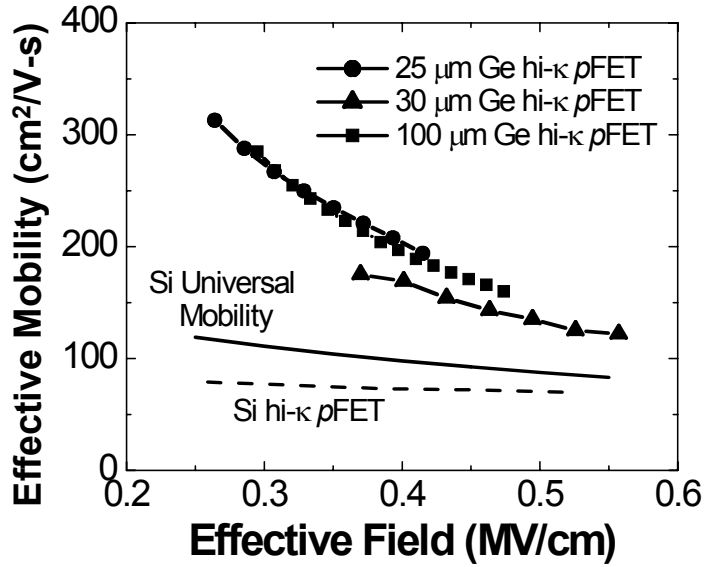
- More symmetric and higher carrier mobilities (low-field)
  - ⇒ More efficient source injection
  - ⇒ ↓ CMOS gate delay
- Smaller energy bandgap
  - ⇒ Survives V_{DD} scaling
  - ⇒ ↓ R with ↓ barrier height
- Lower temperature processing
  - ⇒3-D compatible
- Use high-k dielectrics to passivate Ge



S. Sze, *Phys. of Semicond. Devs.*

High Mobility Ge FETs with High-k (INMP)





Key Results

- Passivation of Ge with GeO_xN_y, ZrO_2 and HfO_2
- n and p dopant incorporation
- 1st demo of Ge MOSFETs with metal gate and hi-κ
- *p*-MOSFET with 3× mobility vs. Hi-k Si
- *n*-MOSFET demonstrated but mobility low

Chui, et. al., IEDM 2002 & IEDM 2003

Side benefit of germanium when it is applied to VLSI for high performance

“ It is a narrow band gap semiconductor”

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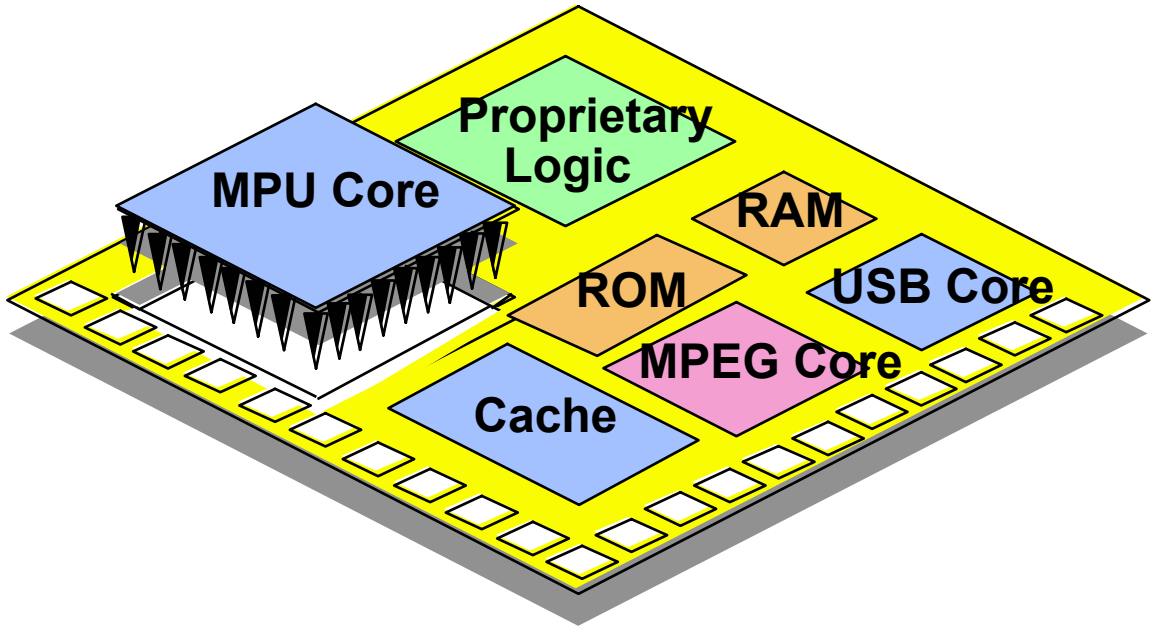
Integration of Heterogeneous Functionality

- SOC, driven by digital/analog/RF/power
- SIP, driven by cost
- 3D integration, the future?

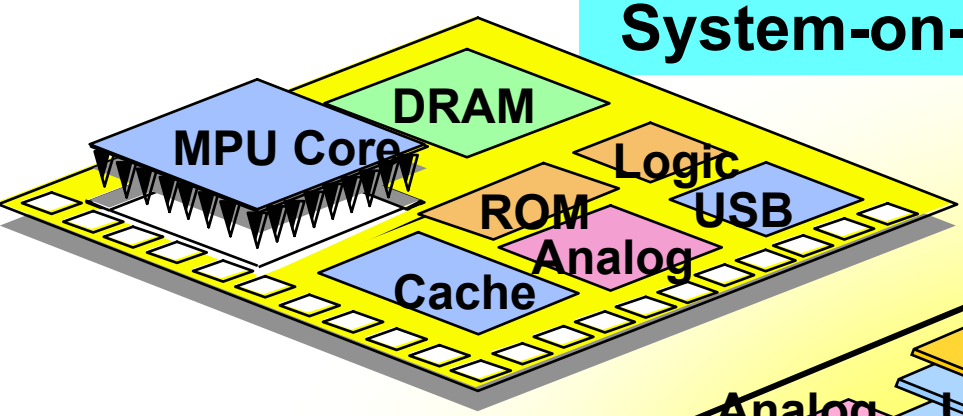
System-on-a-Chip (SoC)



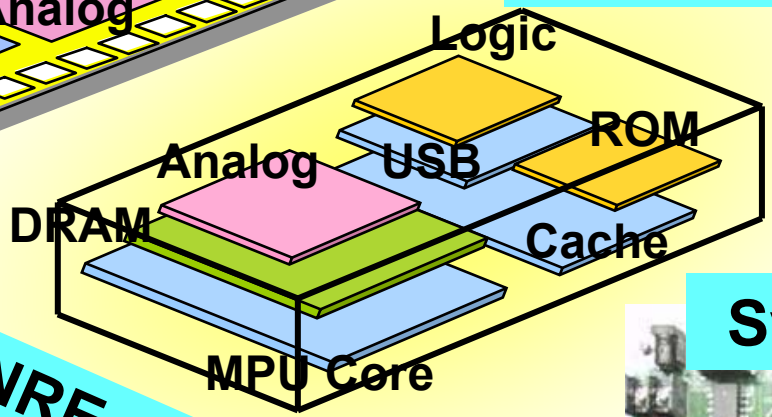
IP ; CPU, DSP, memories, analog, I/O, logic..
HW/FW/SW

System-in-a-Package (SiP) comes into market

System-on-a-Chip (SoC)



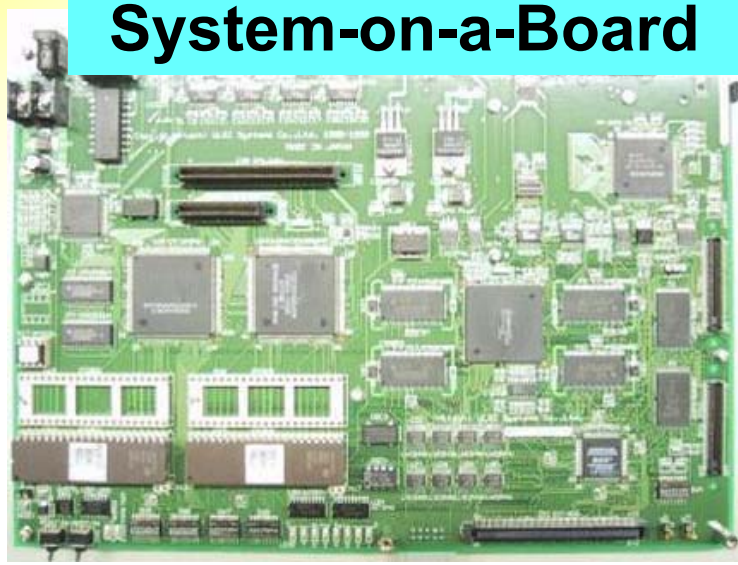
System-in-a-Package (SiP)



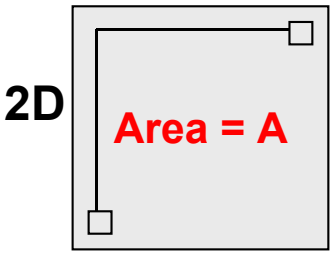
Lower NRE, QTAT

Higher performance

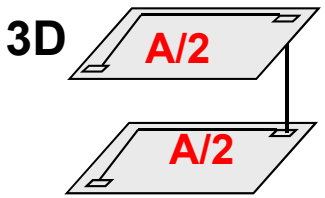
System-on-a-Board



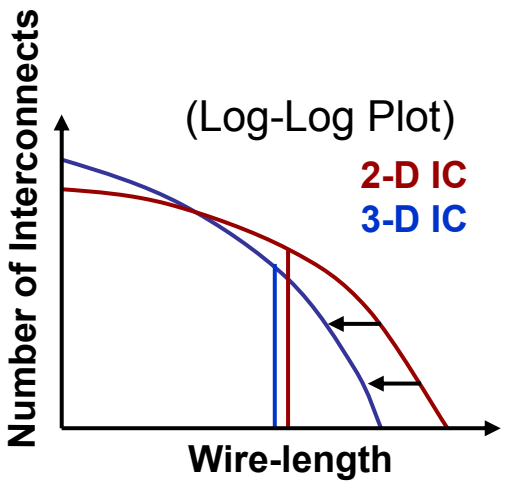
3-D integration

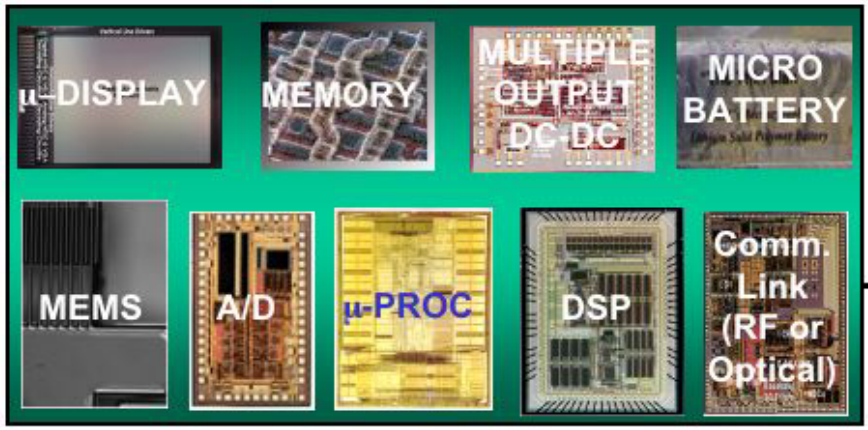


Very Long Wire

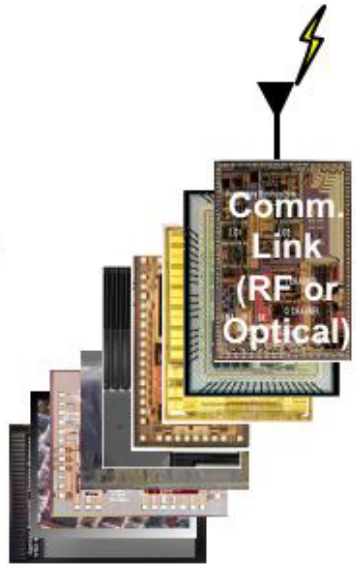


Shorter Wire





2-D System

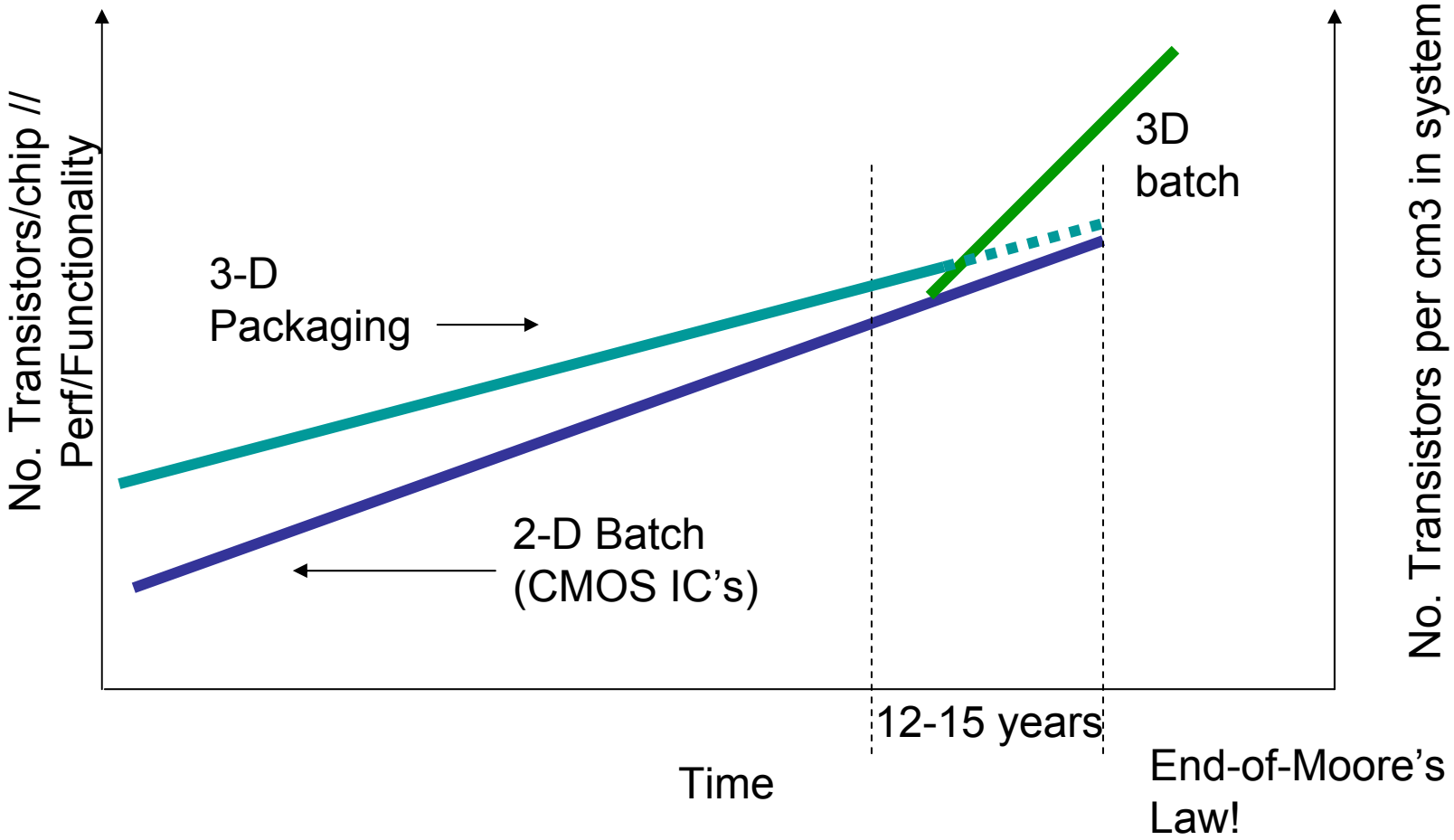


3-D System

- **Integration of heterogeneous technologies possible, e.g., memory & logic, optical I/O**
- **Reduce chip footprint**
- **Replace long horizontal wires by short vertical wires**
- **Interconnect length ⇓ and therefore R, L, C ⇓**
  - **Power reduction**
  - **Delay reduction**

Slide courtesy of K.C. Saraswat

Motivation: Integration Density



The Best Integrators of Electronic Devices Will Own the Heart of Every System – We have <15 Years to Figure it out

Source: D. Radack, DARPA

Contents

- Nanoelectronics, evolutionary “nano” and challenges
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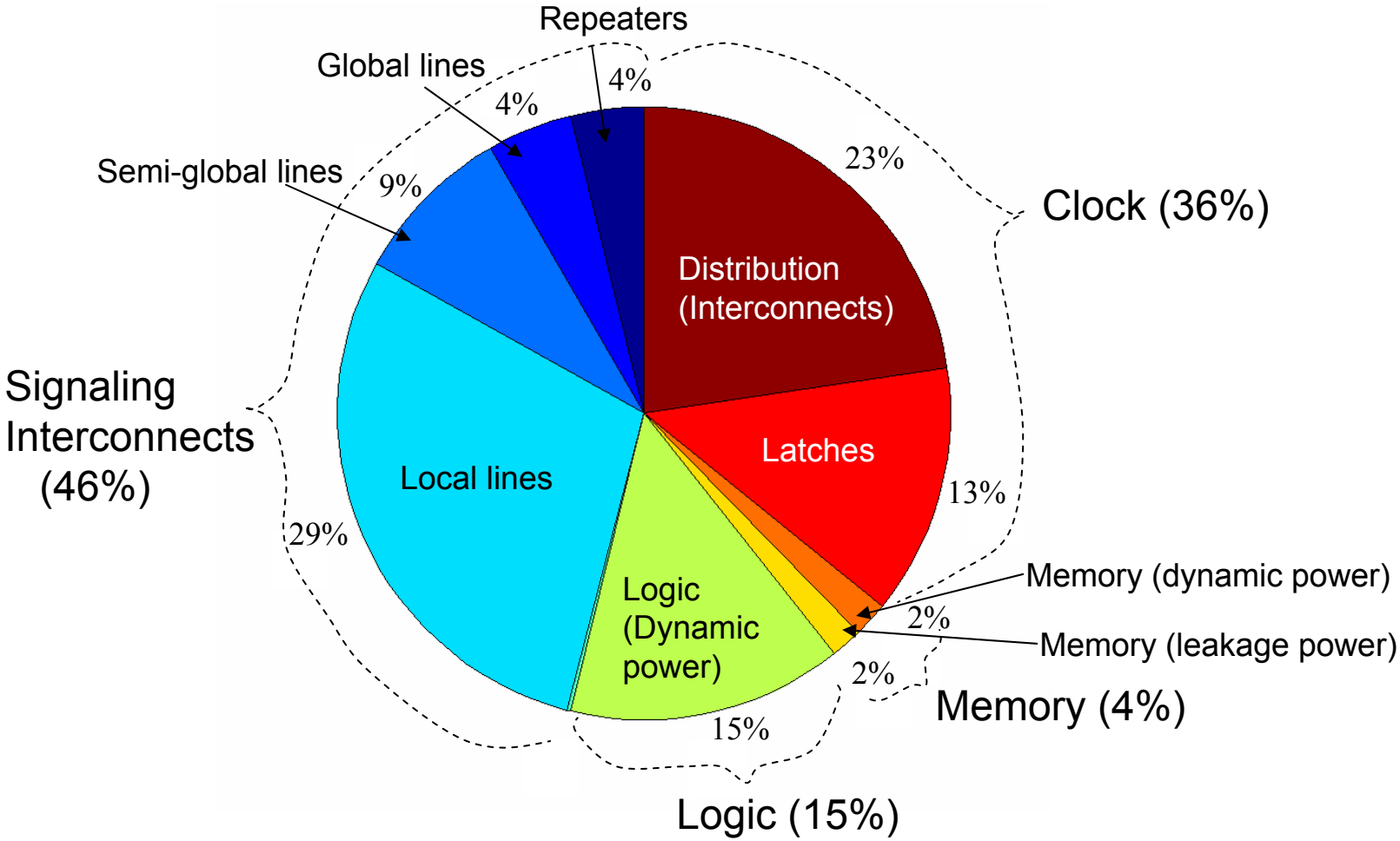
Silicon Based CMOS as "Dominant design" in microelectronics due to lowest power consumption

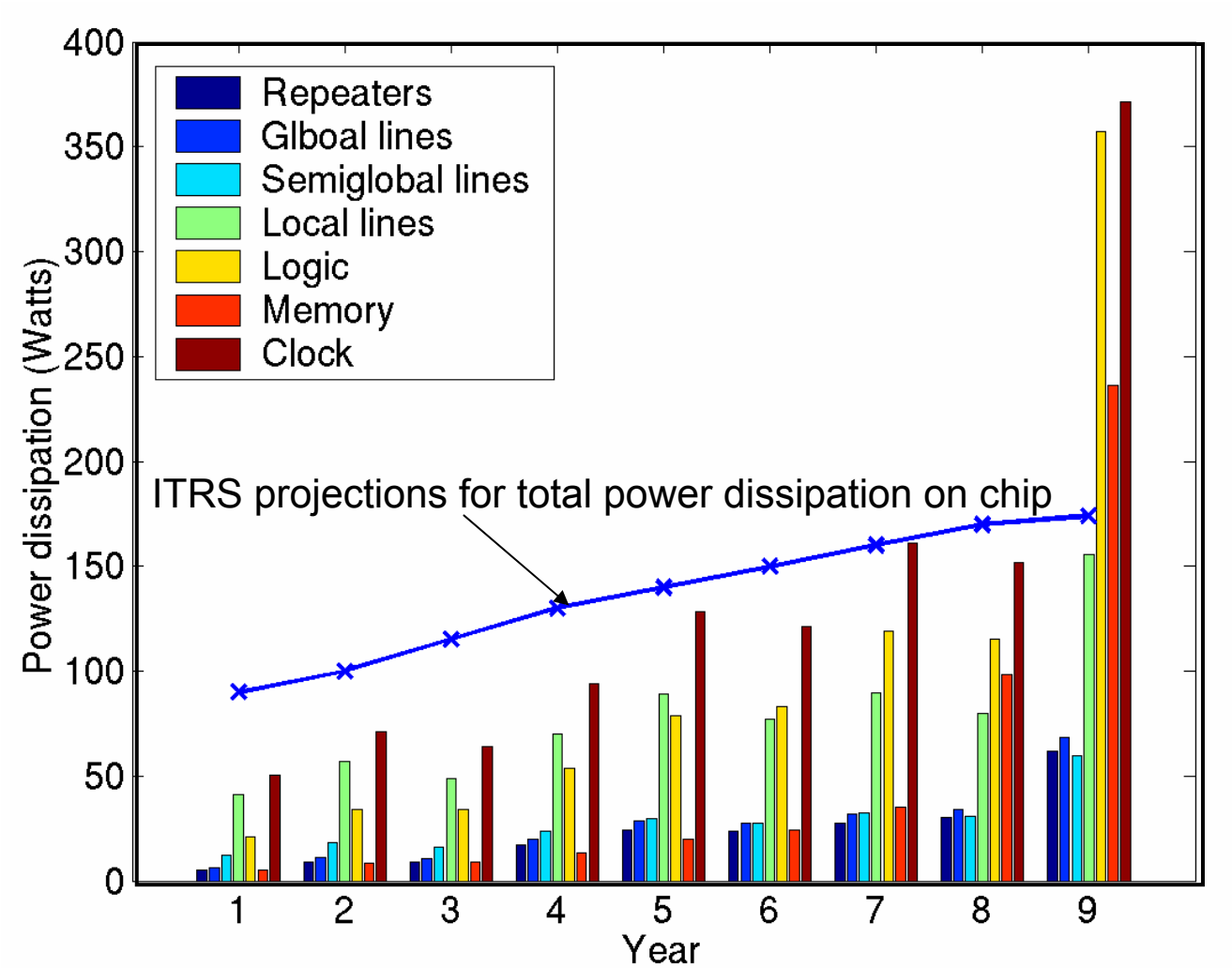
However, both active and passive power consumptions becoming the most challenging issues in nanoelectronics era

Power breakdown at the 180nm node



Chandra, Kapur and Saraswat, IEEE IITC, June 2002

Result: scaling of power components

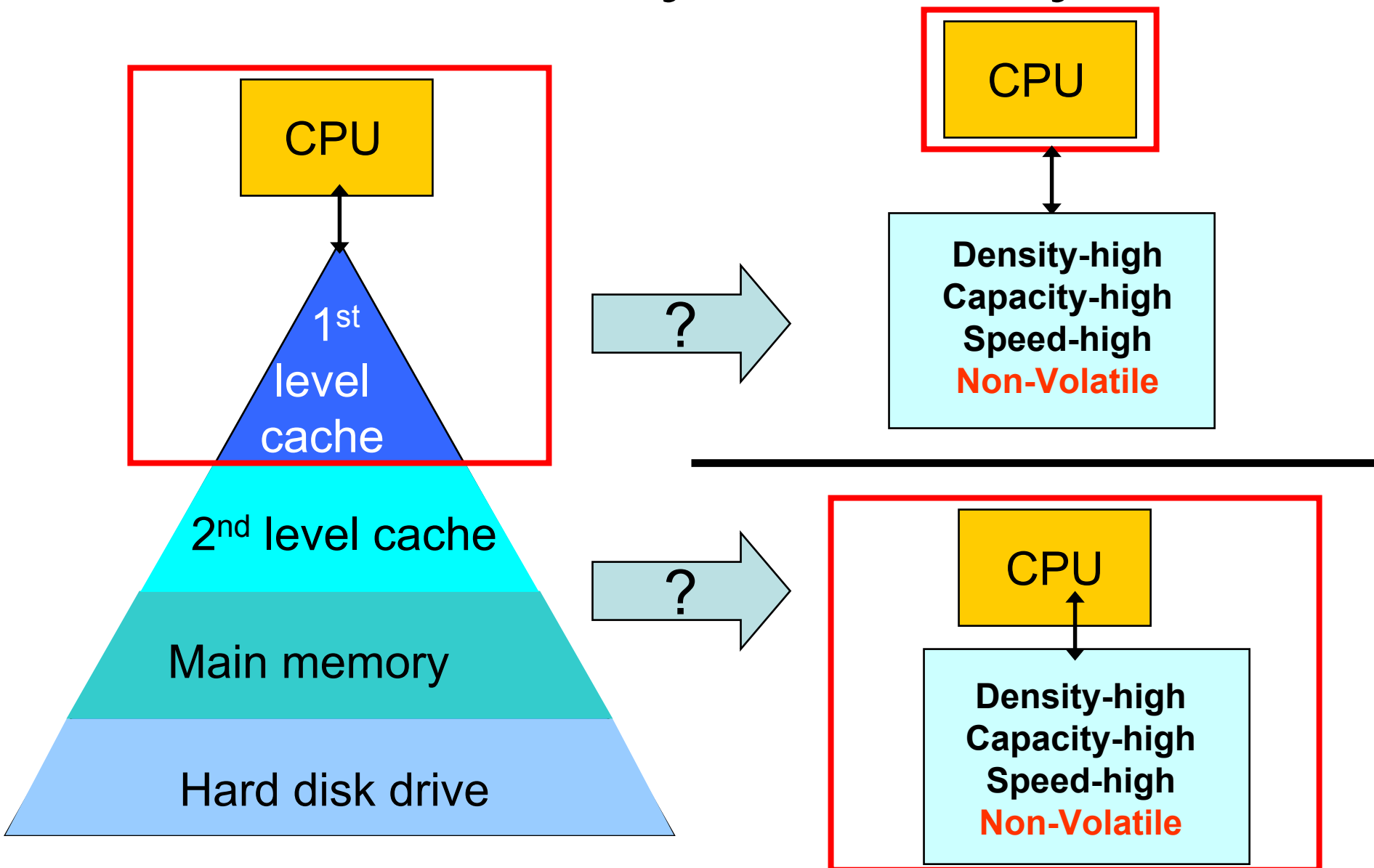


Chandra, Kapur and Saraswat, IEEE IITC, June 2002

Power Consumption and Embedded memory

- As we see continuous increase in embedded memory capacity, power consumed by memory has become significant issue
- Stand-by power for SRAM is destined to increase with MOS Ioff increase
- Soft error immunity also decrease
- Non-volatile memory will be an important part of possible solutions
- Mushrooming of new non-volatility ideas with ***nanoelectronics era*** coming

New Memory Hierarchy ?

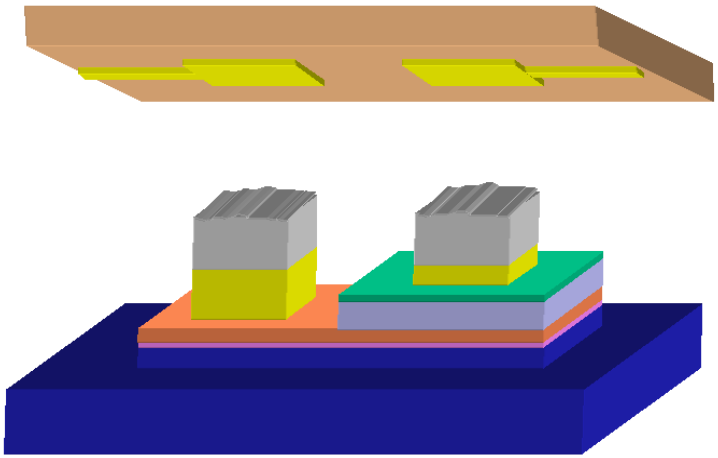


Comparison

	Flash	CBRAM	FeRAM	MRAM	ORAM	PCRAM
Maturity	High Volume Product	Single Cells	Niche Products	Product Samples	Single Cells	Product Demonstrators
Density	4Gb	-	32Mb	16Mb	-	64Mb
Cell Size [um^2]	0.025	-	0.6	1.4	-	0.5
Embeddability	Yes	Yes	Yes	Yes	Yes	Yes
Nonvolatile	Yes	Yes	Yes	Yes	Yes	Yes
Random Read Access	80ns/10µs	<200ns	50ns	30ns	<200ns	50ns
Random Write Access	~10µs (erase 100ms)	<200ns	75ns	30ns	<100ns	50ns
Destructive READ	No	No	Yes	No	No	No
Write Endurance	10^6	$>10^5$	$>10^{12}$	10^{15}	10^5	$>10^{12}$
Write Voltage	Vdd+~10V	Vdd	Vdd	Vdd	Vdd+~2V	Vdd
Companies (Criteria: IEDM, ISSCC, VLSI publication during last 3 years)	Actrans System, eMemory Tech., Fujitsu, HaloLSI, Infineon, Intel, Macronix, Motorola, Powerchip, Renesas / Hitachi, Samsung, Sandisk, Sony, SST, ST, Toshiba		Agilent, Fujitsu, Hynix, Infineon Matsushita, Oki Ramtron Samsung Sanyo Toshiba TI	IBM Infineon Motorola NEC Renesas Samsung Sony	Infineon	Hitachi Intel Macronix Ovonyx Samsung ST

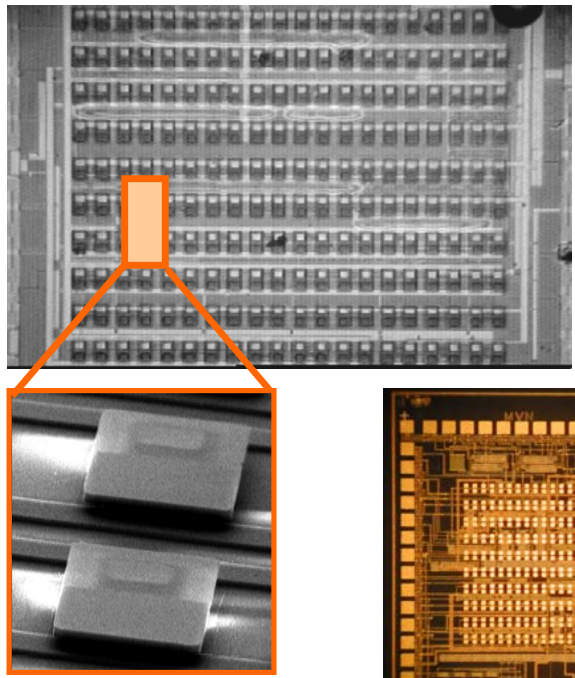
Hybrid integration of optoelectronic devices to CMOS

Silicon CMOS chip with gold bonding pads



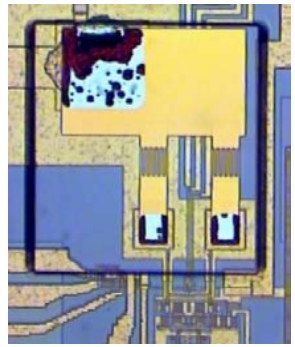
GaAs optoelectronic chip with indium flip-chip bumps

III-V Device arrays on CMOS

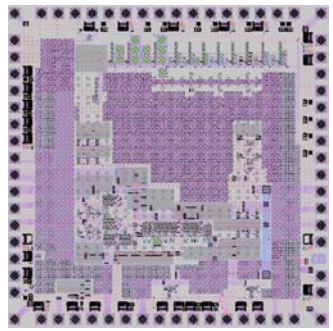


WDM interconnect chip (with light beams)

Low capacitance MSM photodetectors on CMOS



SOI chip (optical clocking)



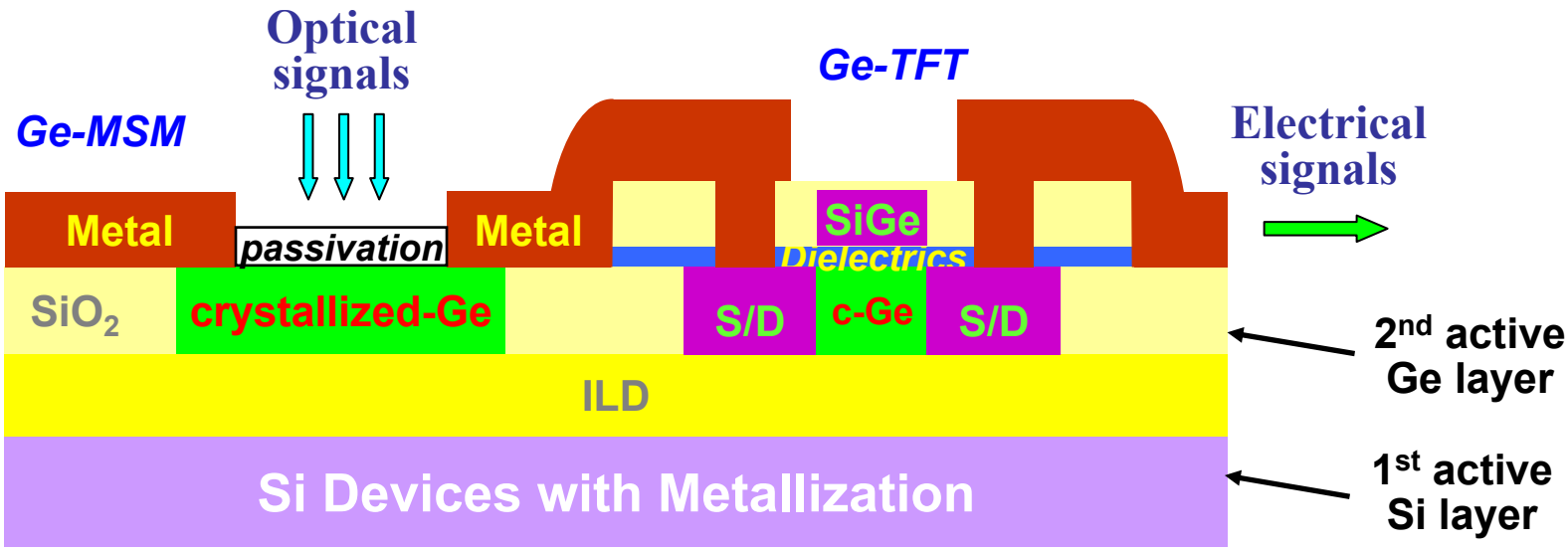
optical latency test chip

D. Millar, Stanford Univ.

Monolithically Integrated Receiver

Ge Transistor + Ge Photodetector:

- Employ recrystallization techniques on α-Ge films at low temp
  ⇒ Improve film crystallinity to ↓ I_{dark} and ↓ carrier scattering
- Integration of optical receiver in the upper active (Ge) layer
  ⇒ On-chip optical clock distribution in 3D-ICs



Already enough for "evolutionary nano", but what about "revolutionary nano"???

Contents

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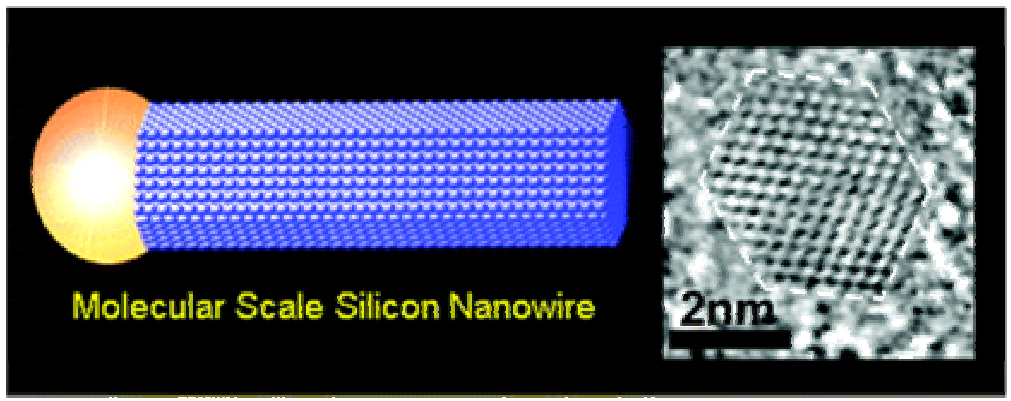
Revolutionary "nano"

- Still charge controlled device?
- Better electrostatics?
- Better transport properties?
- Control of every parameters which has been "pre-requisite" of evolutionary "nano"

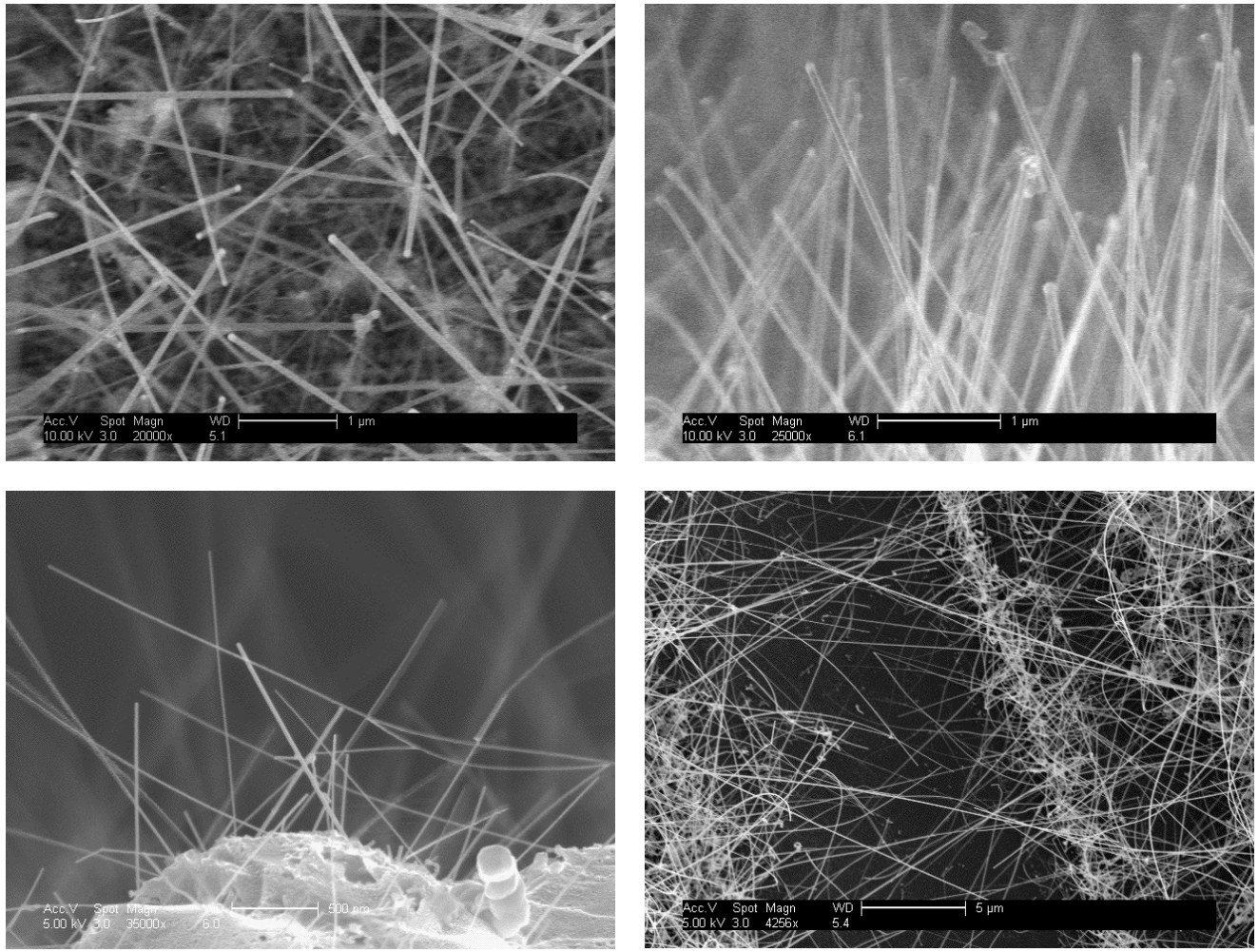
Why Nanowires ?

- **Lithography independent (self-assembled)**
- **Low thermal budget process**
- **High mobility charge transport**
- **Building block for modern nanoscale devices and structures**
- **Potential for exploring scaling in dimensionality**



Yue Wu et. al., NANO LETTERS 2004, Vol. 4, No. 3, pp. 433-436

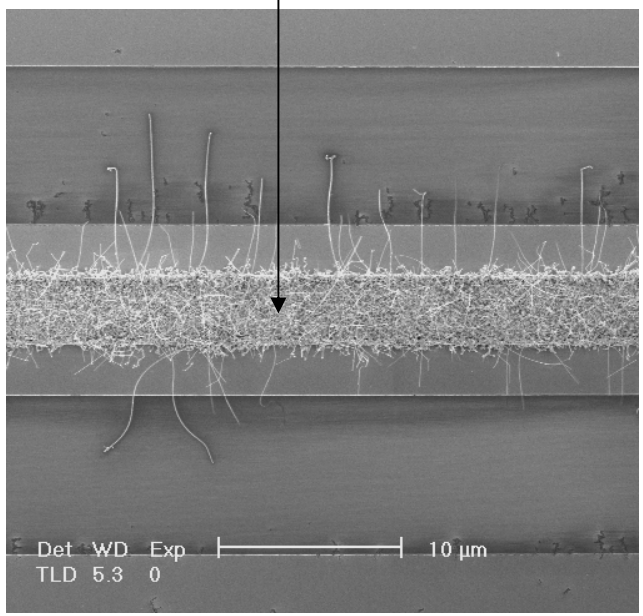
Germanium Nanowire Growth Results

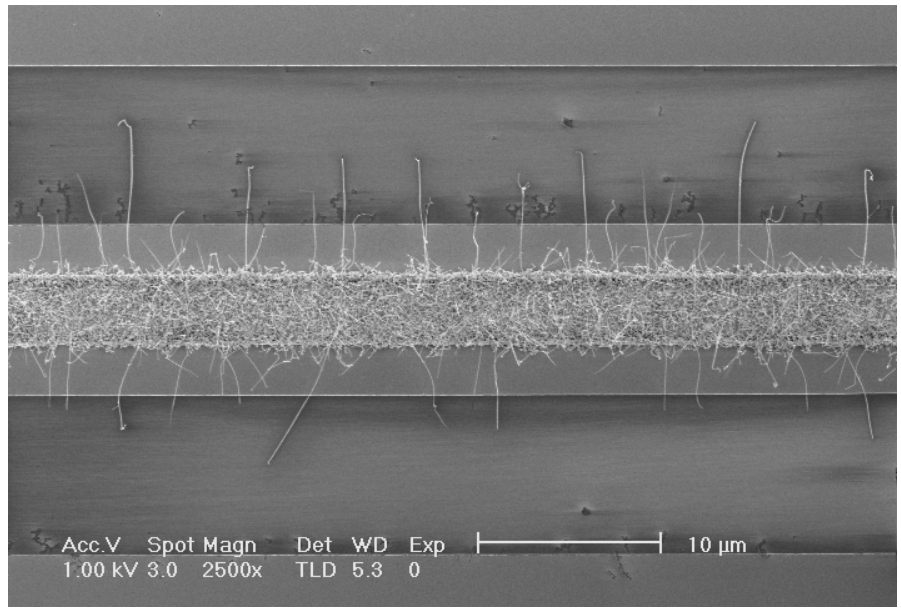


20 - 60 nm silicon and germanium nanowires

Alignment: In situ growth in electric field

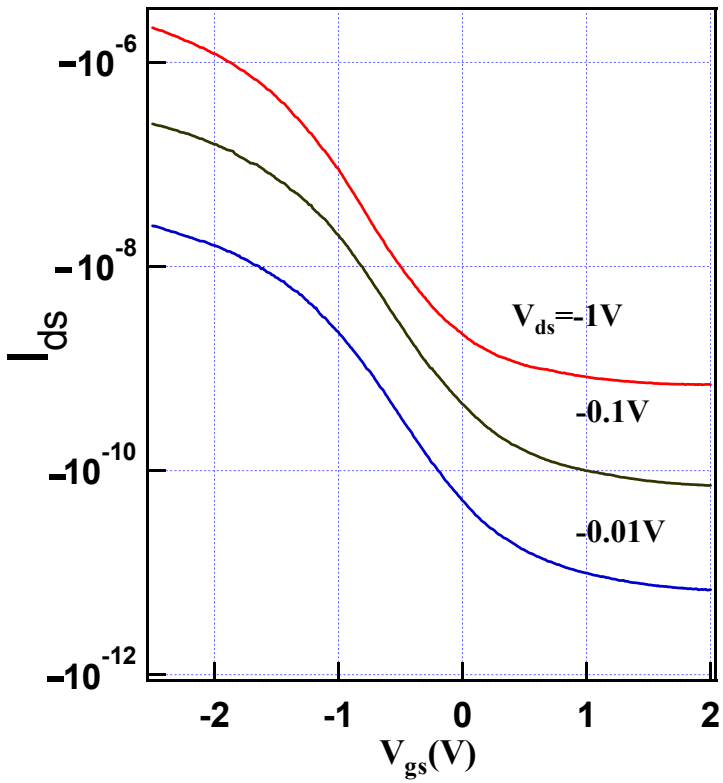
Patterned catalyst strip

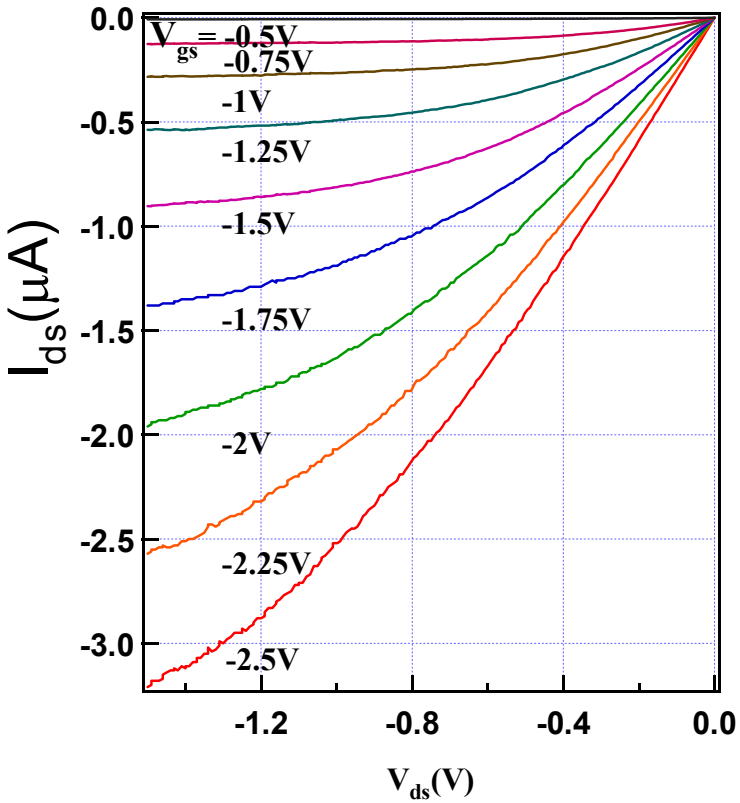




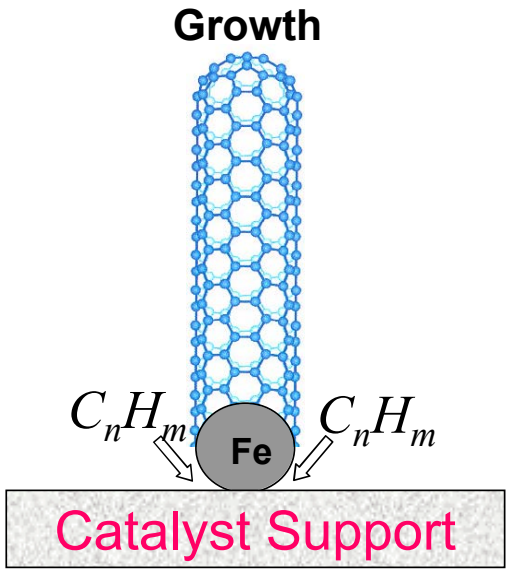
E-field 1V/µm

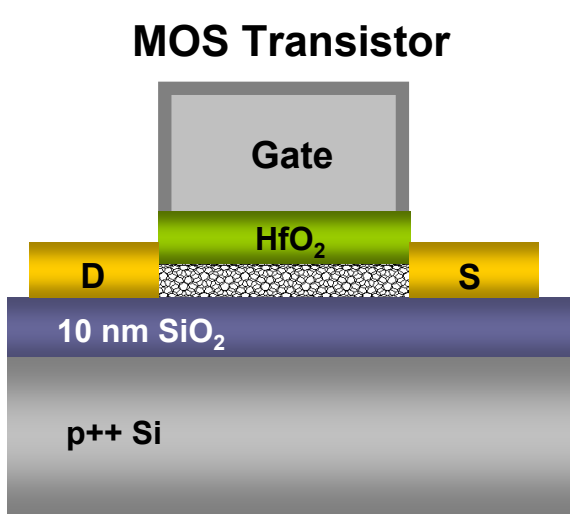
GeNW FETs with HfO_2 as gate dielectrics

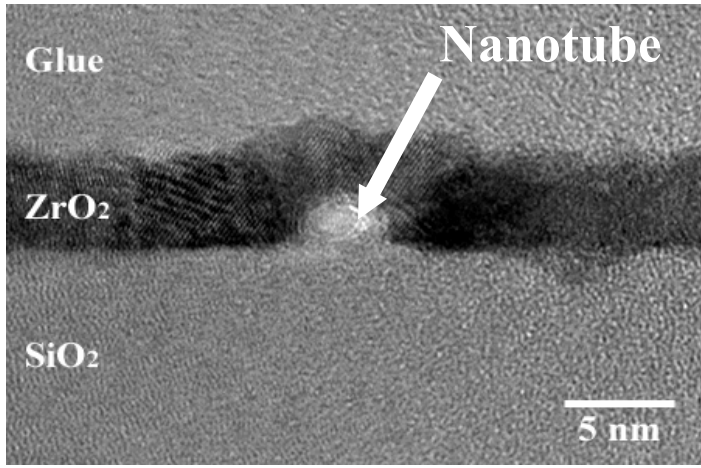




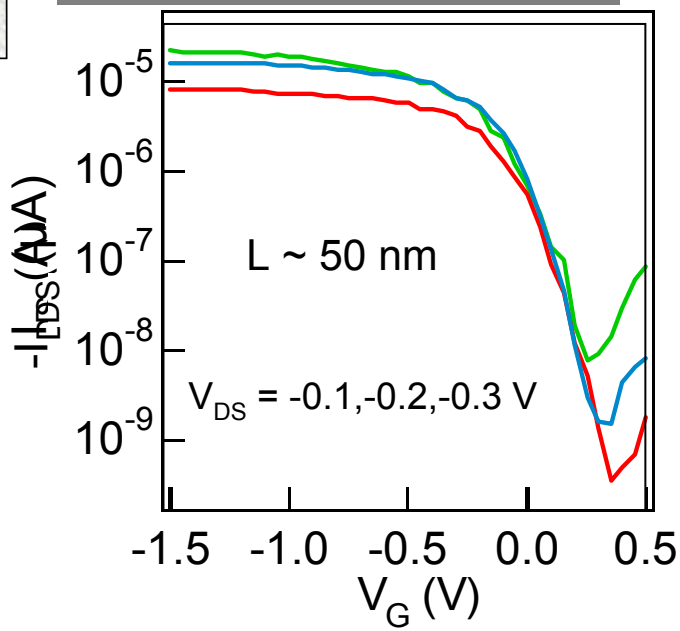
Ballistic Nanotube Transistors

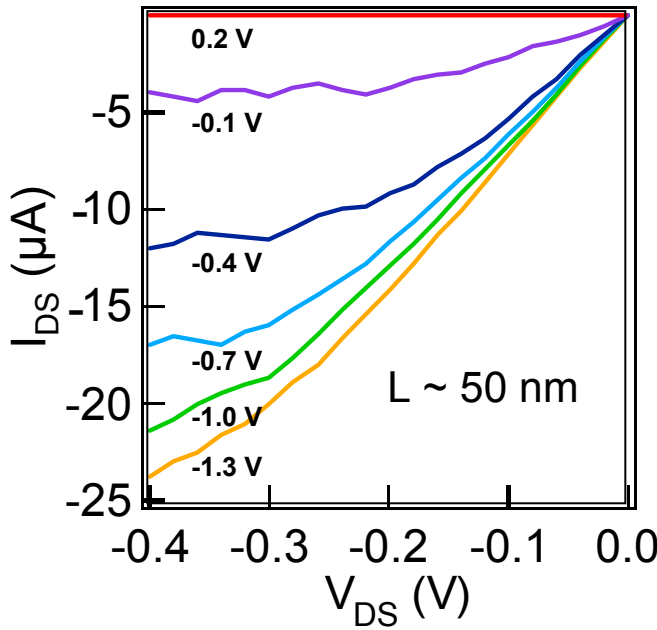






Dai (Stanford)
McIntyre (Stanford)
Gordon (Harvard)
Lundstrom (Purdue)



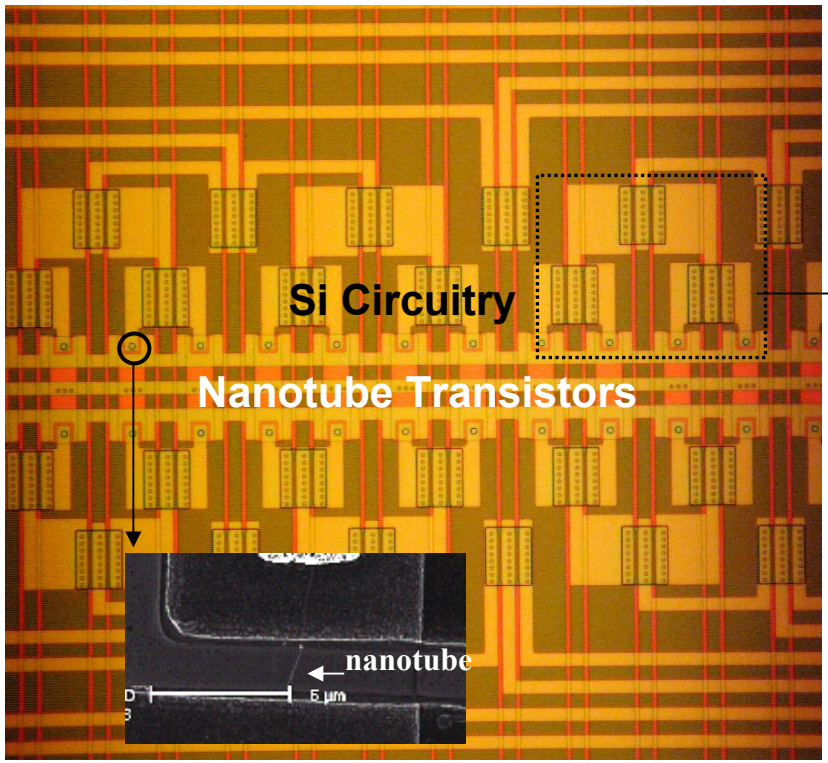


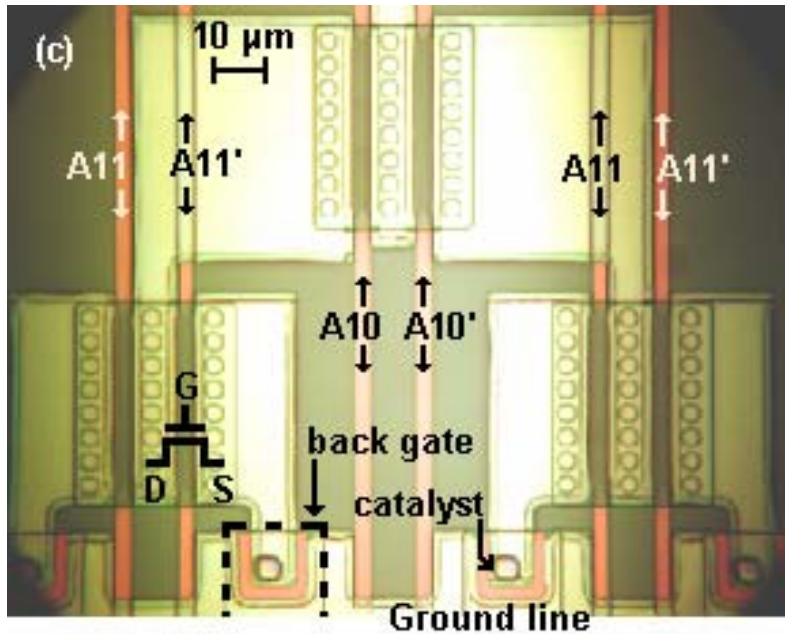
Key Challenge: Low thermal budget controlled growth

Integration of Nanotubes with Si MOS Technology?

Nanotube/Si CMOS hybrid devices: a possible approach to future electronics?

Integrated Carbon Nanotube Devices with MOS Circuits





Berkeley-Stanford

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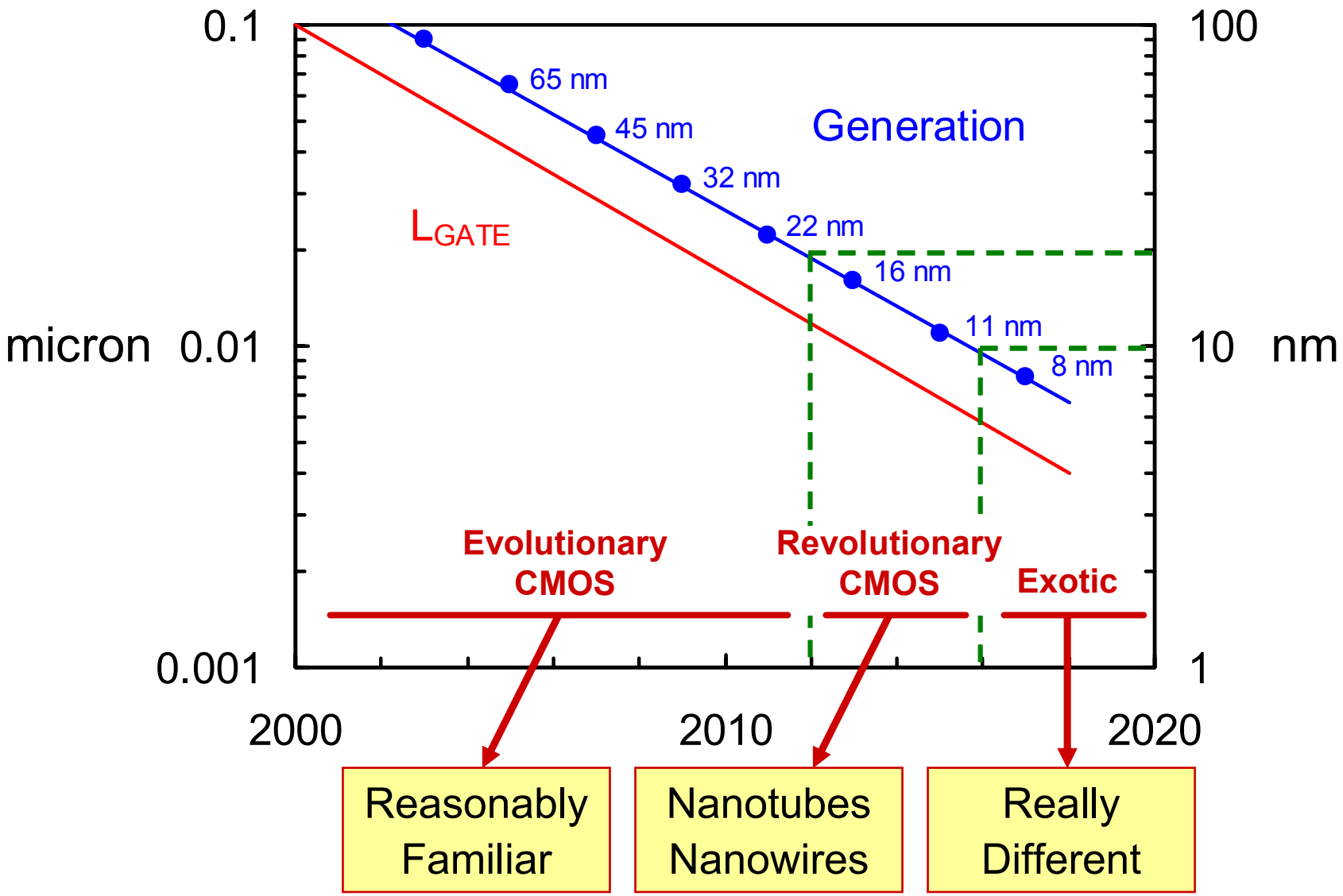
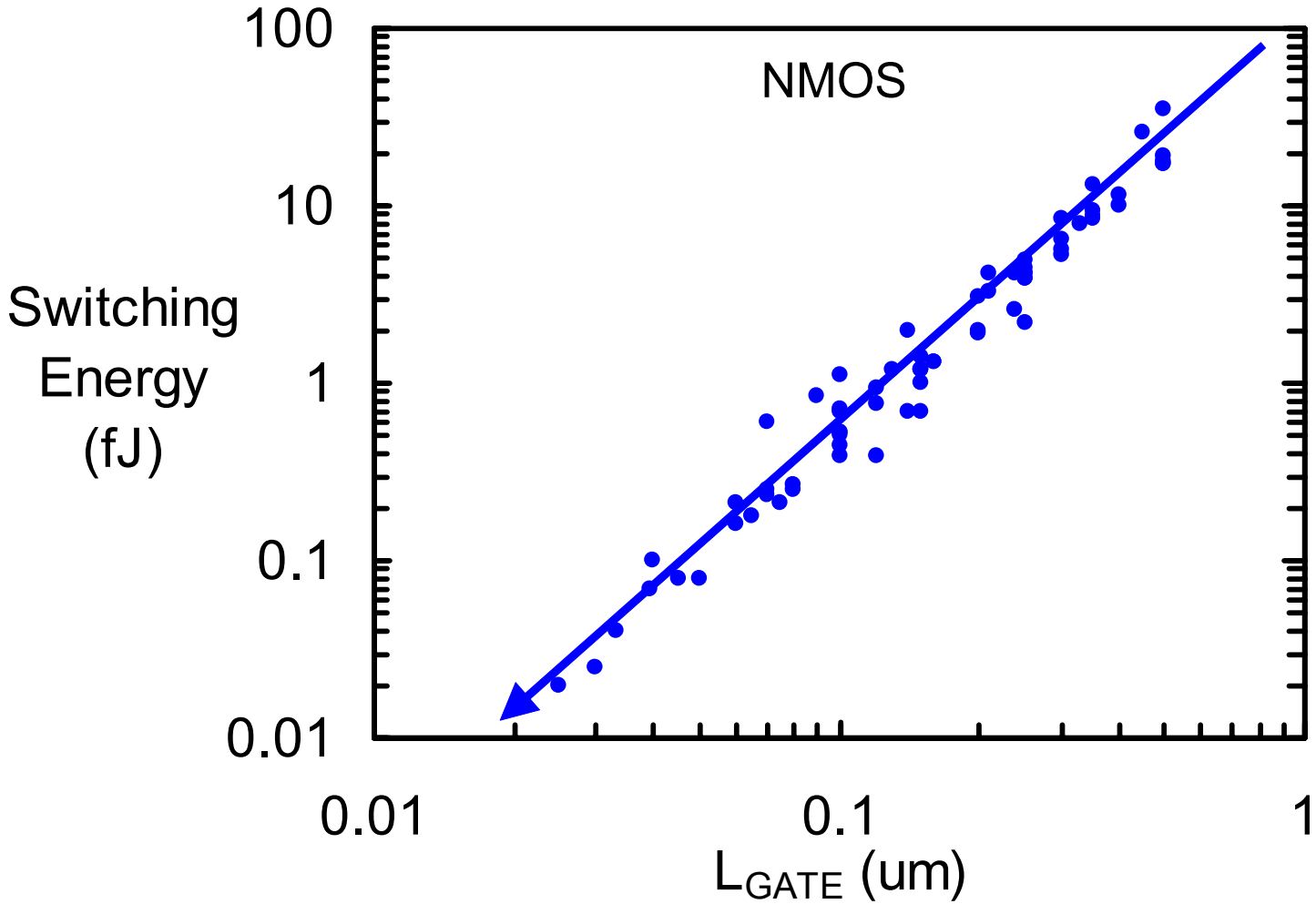
Nanotechnology Eras



Mark Bohr, Intel

Transistor CV^2 Switching Energy Trend



Significant switching energy reduction due to feature size and supply voltage scaling

What's beyond charge control devices??

- Spintronics?

  Spin-lattice relaxation time too short?

  Room temperature operations?
- Molecular devices?

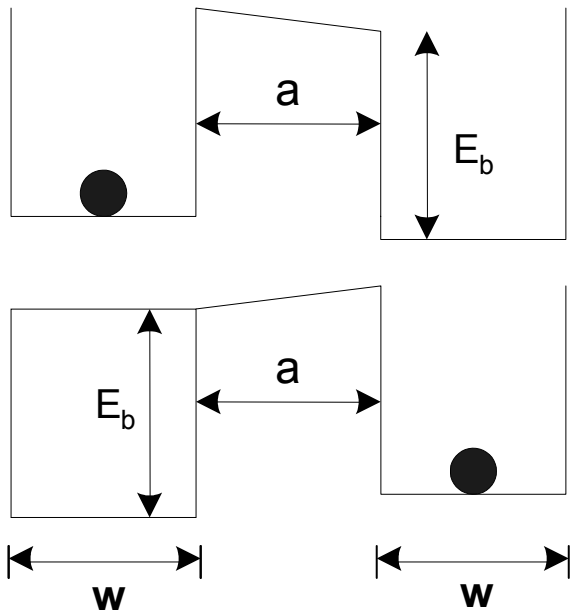
  Any gain?

  Molecule-electrode contact?
- A variety of "non-volatile memory"

Spin Based Switch

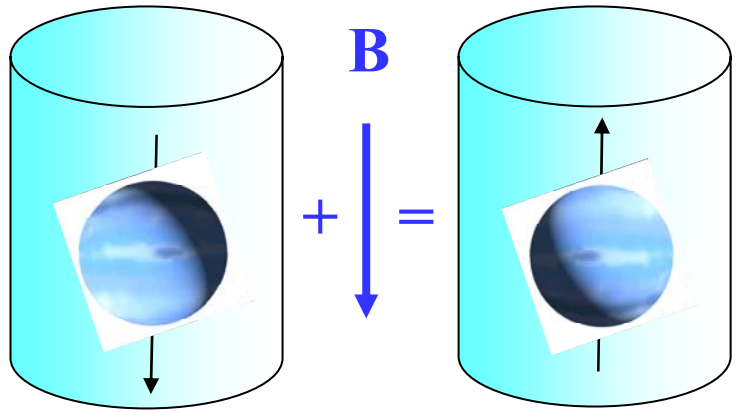
Charge

ΔE_b(e-) ~1.7x10^{-2} eV



Spin

ΔE(spin) ~8.6x10^{-8} eV



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Challenges Facing a Pervasive Replacement of "Ultimate Scaled CMOS"

- **Operable at room temperature**
- **Cost of less than 0.5 micro-cents per logic gate**
- **Greater than $4x10^8$ logic gates per cm^2**
- **Greater than 10^{10} "minimum-size switches" per cm^2 (e.g., SRAM transistors)**
- **Cost of less than 50 nano-cents per bit of memory**
- **Greater than 30 Gbits of memory per cm^2**
- **Intrinsic switching speed greater than 5 THz**
- **Power consumption of less than 6 μW per MOP/sec**
- **Reliability of greater than 10^5 hours (~ 10 years) operating lifetime**
- **SER of less than a few thousand FITs per Mbit in terrestrial environment**
- **Capable of "mass production" (e.g., > 1 million units /day)**
- **Ability to integrate logic, analog, RF, memory (high-speed, high-density, nonvolatile, etc.)**

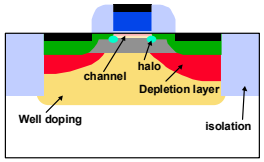
Revolutionary "nano" in evolutionary "nano" space?

- Current drive capability: Except for CNT, wires are fundamentally same as scaled CMOS
- Density: Unless vertically standing, neither CNT nor wire adds much density improvement
- New semiconducting materials or band engineering provides further current gain
- Non-volatile memories can deal with chip power consumption if endurance/imprint issues solved
- 3D integration of "revolutionary nano" on top of "evolutionary nano" could assure continuation of Moore's law, i.e. density increase with reduced cost/gate or bit

Technology Progression

Nanotechnology

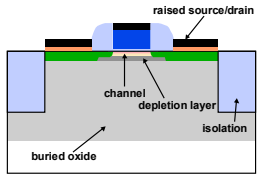
Bulk CMOS



Cu interconnect

Low-*k* ILD

FD SOI CMOS

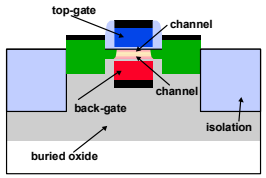


Metal gate

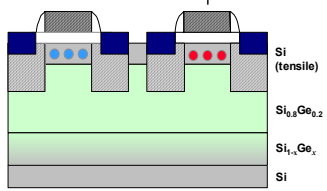
High *k* gate dielectric

Ge on Si hetroepitaxy

Double-Gate CMOS

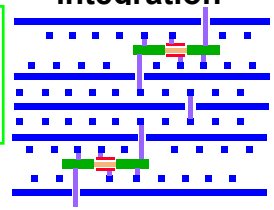


Strained Si
Ge channel

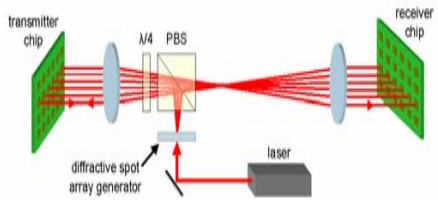


Wafer bonding
Crystallization
Nanowires

3D, heterogeneous integration



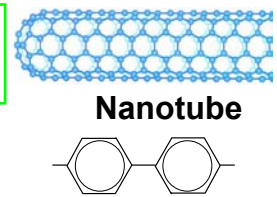
Optical interconnect



Detectors, lasers, modulators, waveguides

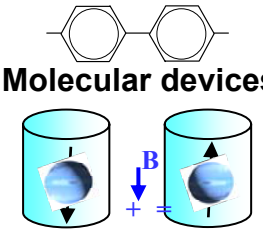
Interconnects and contacts for nanodevices

Self-assembly



Nanotube

Molecular devices



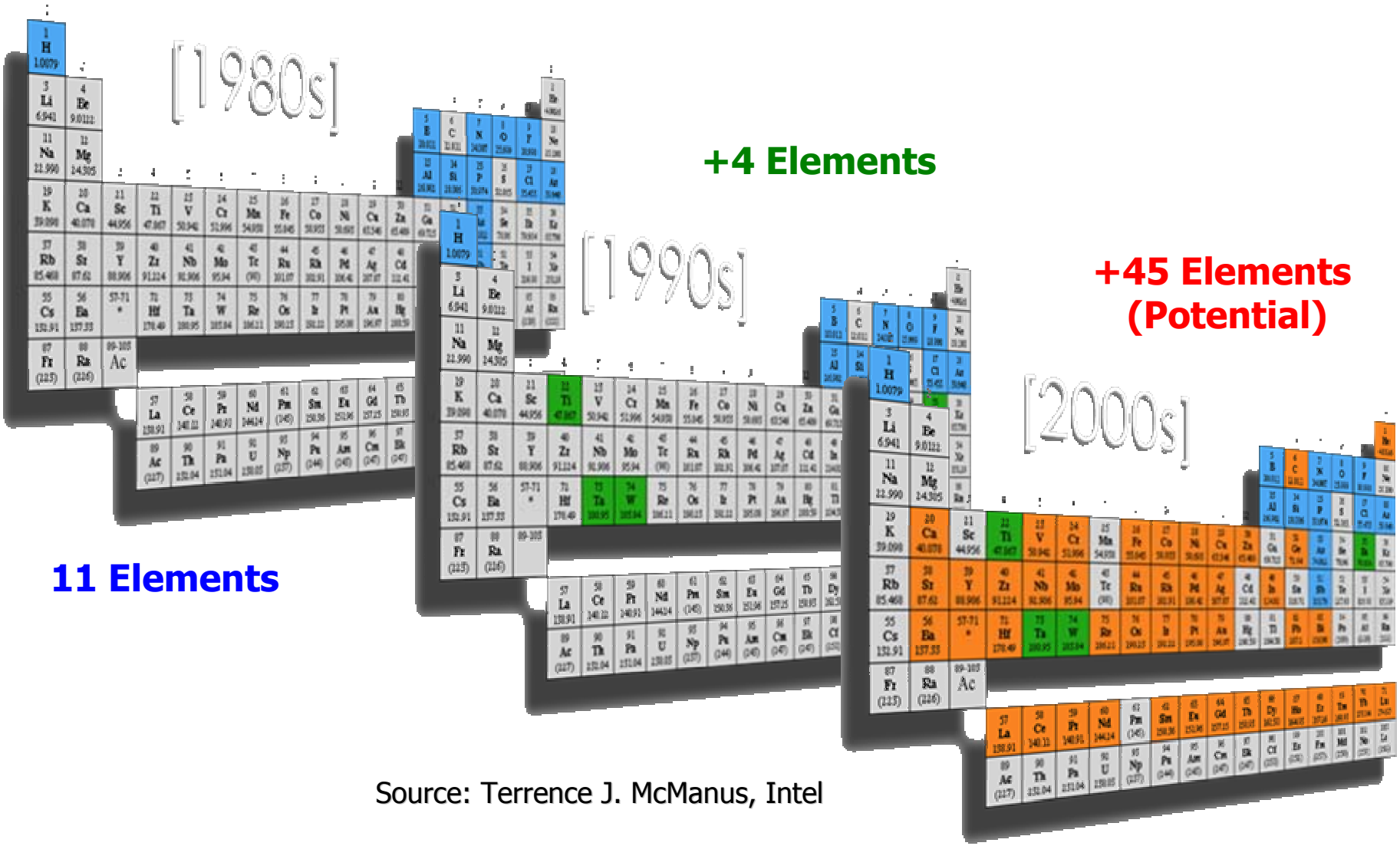
Spin devices

100 nm

2 nm

Feature Size

Moore's Law Increasingly Relies on Introduction of New Materials



Source: Terrence J. McManus, Intel

Summary

- **Changes from microelectronics to nanoelectronics is beyond the geometry shrink, but a combination of evolutionary and revolutionary progress of science and technology**
- **Nanotechnology requires broad spectrum of expertise and cross disciplinary interactions for people and organization involved from industry and academia**
- **System on chip integration not only 2D but likely to be 3D with active layer stacking beyond wafer/die bonding, accompanied by manufacturing/testability challenges, providing new challenge to interconnect**
- **Revolutionary “nano” has still a long way to go before any practical applications in integrated electronics where strong focus from engineering are needed**