CMOS RF Integrated Systems--
Trends and Challenges

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Outline

- **RF Active and Passive Devices v/s Scaling Roadmap**
- **Monolithic Inductors v/s Monolithic Transformers**
- **Single-Ended v/s Fully-Differential RF Circuits**
- **Compact Modeling / Simulated Annealing Optimization**
- **CMOS RF Circuit Examples: LNA, DA, PA, etc.**

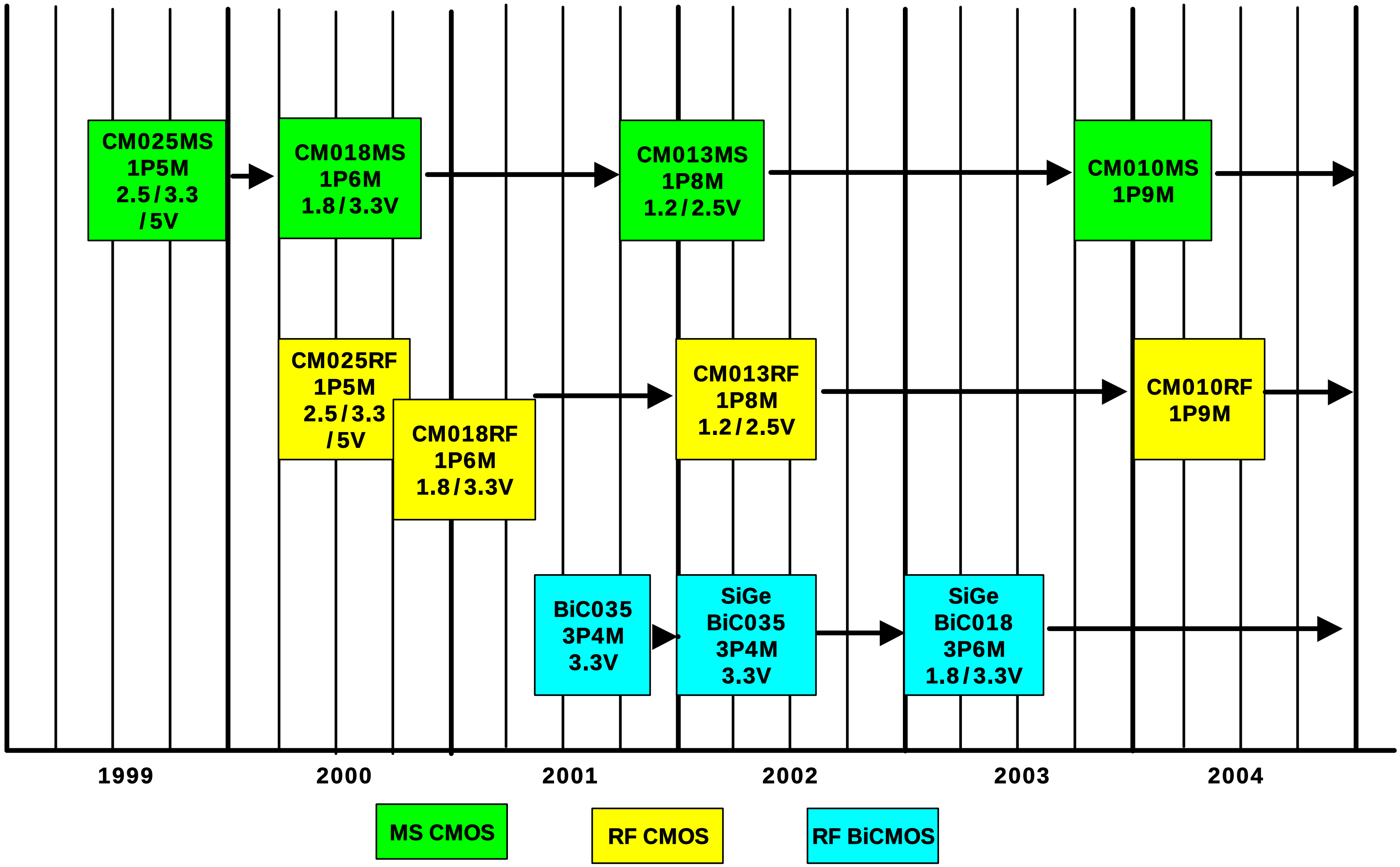
SIA National Technology Roadmap

Gate Length (nm)	180	140	120	100	70	50	35
Year First Product Shipment	1997	1999	2001	2003	2006	2009	2012
MPU FETs/cm**2	8M	14M	16M	24M	40M	64M	100M
ASIC CHIP SIZE (mm**2)	480	800	850	900	1000	1100	1300
ASIC PACKAGE PINS/BALLS	1100	1500	1800	2200	3000	4100	5500
ASIC CLOCK FREQ. (MHZ)	300	500	600	700	900	1200	1500
MAX. WIRING LEVELS	6	6 or 7	7	7	7 or 8	8 or 9	9
MIN. LOGIC VDD (V)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
POWER (HAND HELD) (W)	1.2	1.4	1.7	2	2.4	2.8	3.2
POWER (HEAT SINK) (W)	70	90	110	130	160	170	175

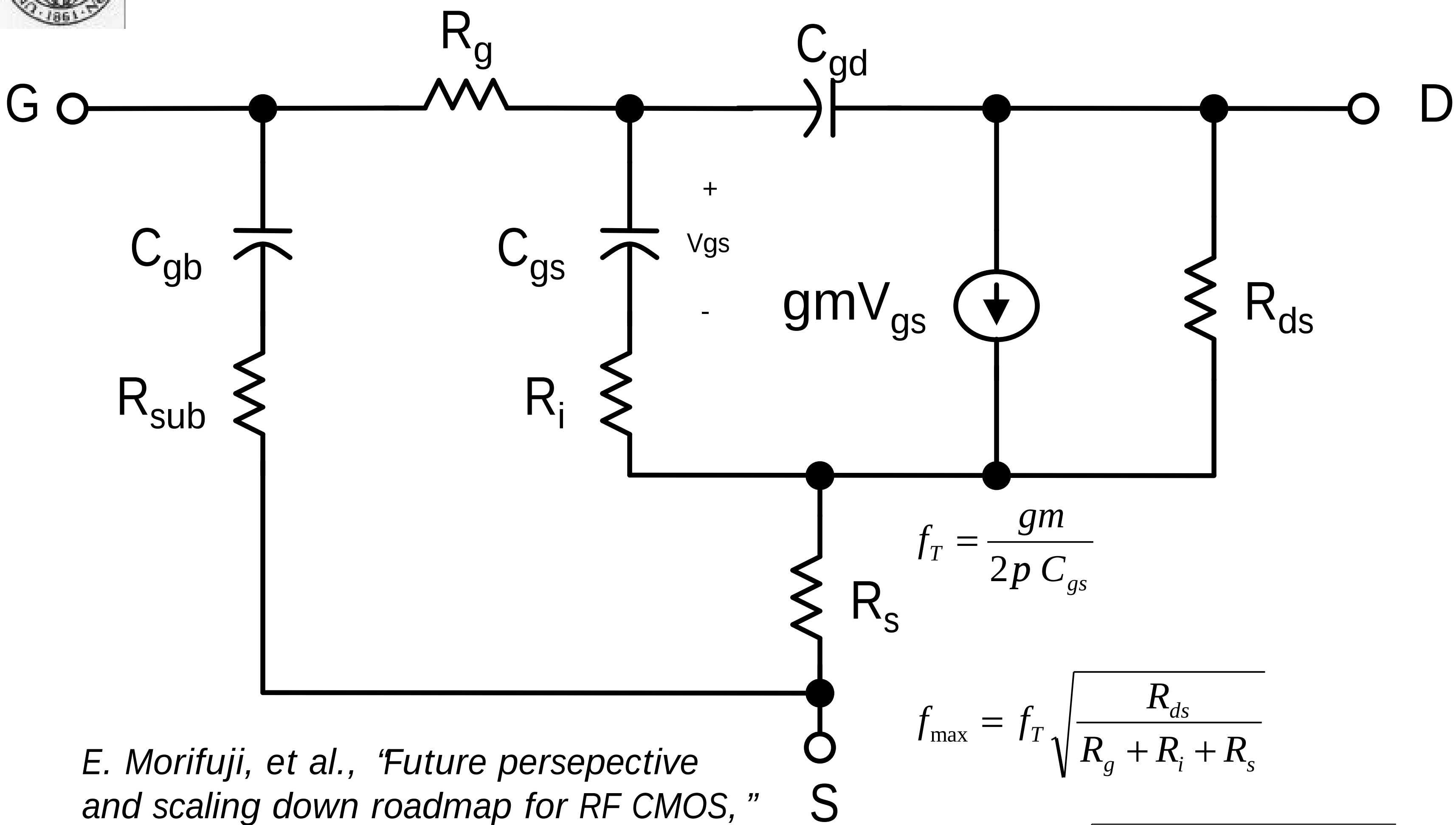
Key Issues: Cascodes Problematic at Low Voltages

More metal layers for inductors/transformers

TSMC Mixed-Signal/RF Technology Roadmap



Small-signal model



$$f_T = \frac{gm}{2p\, C_{gs}}$$

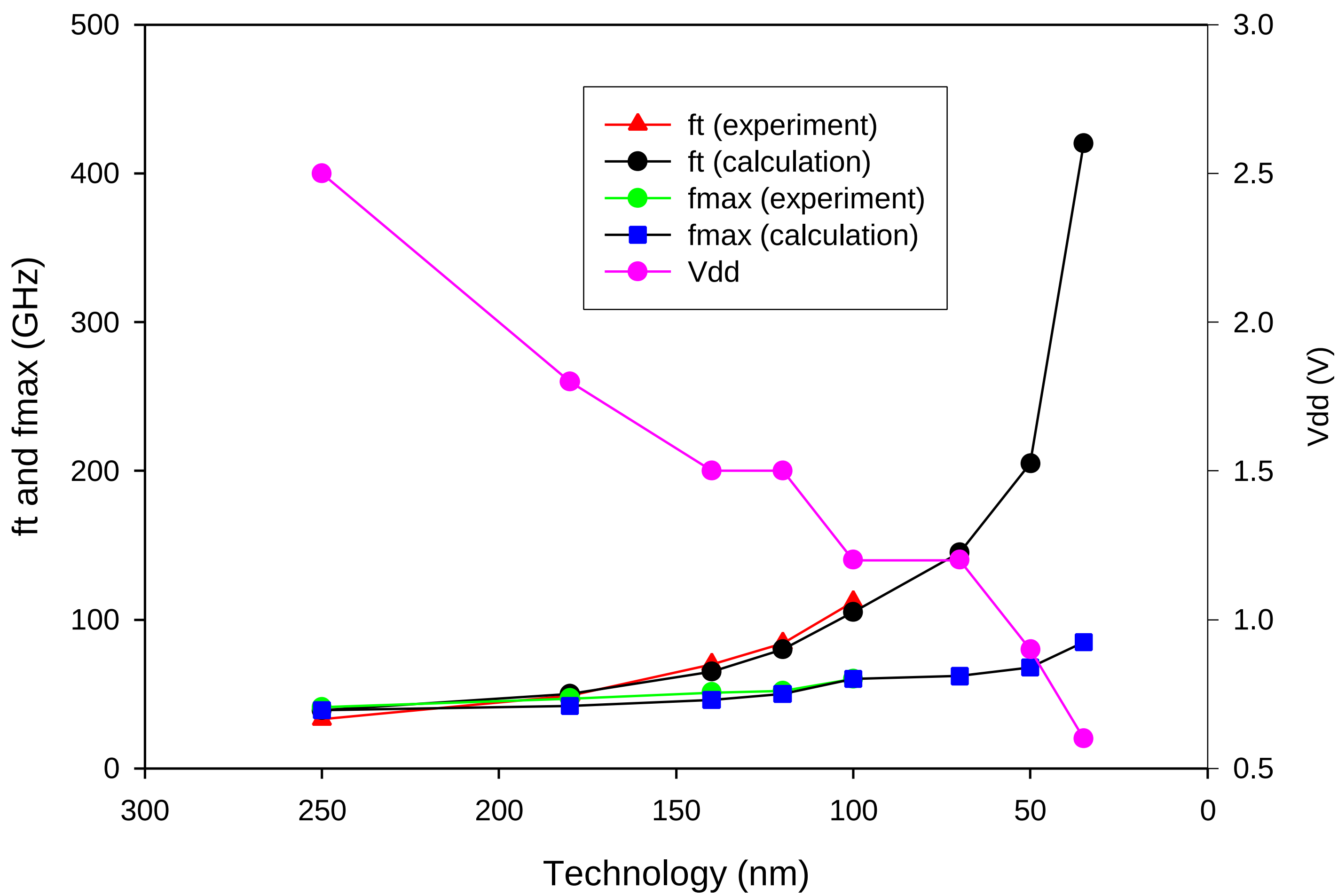
$$f_{\max} = f_T \sqrt{\frac{R_{ds}}{R_g + R_i + R_s}}$$

$$NF_{\min} = 1 + 2\sqrt{(R_g + R_s + P / g_m) C_{gs}{}^2 w^2 R_i}$$

$Note : P \approx 1.5$

E. Morifuji, et al., ‘Future persepective and scaling down roadmap for RF CMOS,” Symposium on VLSI Circuits, pp. 165-166, 1999.

Ft, Fmax and Vdd vs Technology

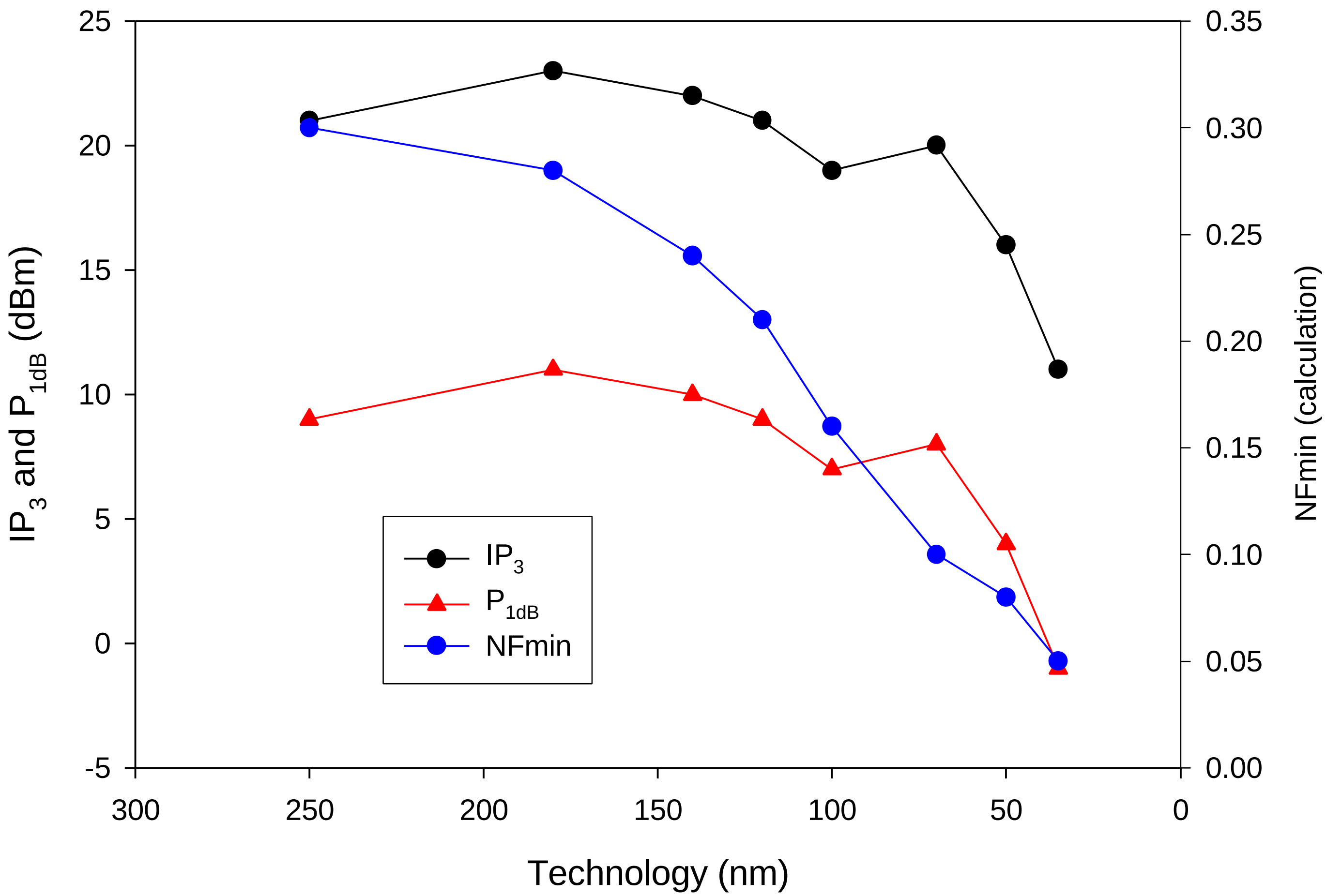


Roadmap of Linearity (IP_3 at gm=40mS) and P_{1dB}

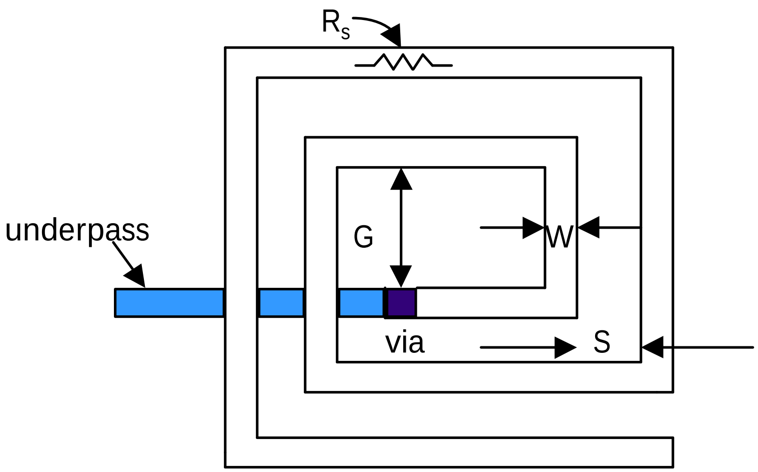
Year		1995	1997	1999	2001	2003	2005	2007	2009
Gate Length (nm)		250	180	140	120	100	70	50	35
Wg=200µm constant	IP_3(dBm)	16	21	19	17	9	1	---	---
	Id(mA)	7.0	6.7	4.4	3.9	2.6	1.2	---	---
Wg:scaled With Lg	Wg(µm)	200	150	110	100	80	60	50	35
	IP_3(dBm)	16	17	15	16	17	11	9	6
	Id(mA)	7.0	8.8	7.0	6.5	5.5	3.0	2.9	3.6
Wg:optimized scaling	Wg(µm)	280	240	170	140	110	80	70	60
	IP_3(dBm)	21	23	22	21	19	20	16	11
	P_{1dB}(dBm)	9	11	10	9	7	8	4	-1
	Id(mA)	4.7	6.7	4.9	4.1	3.6	2.2	2.0	1.9

IP3 = 10log(gm/gm_3) + 12.2dBm; 12.2dBm is a fudge factor

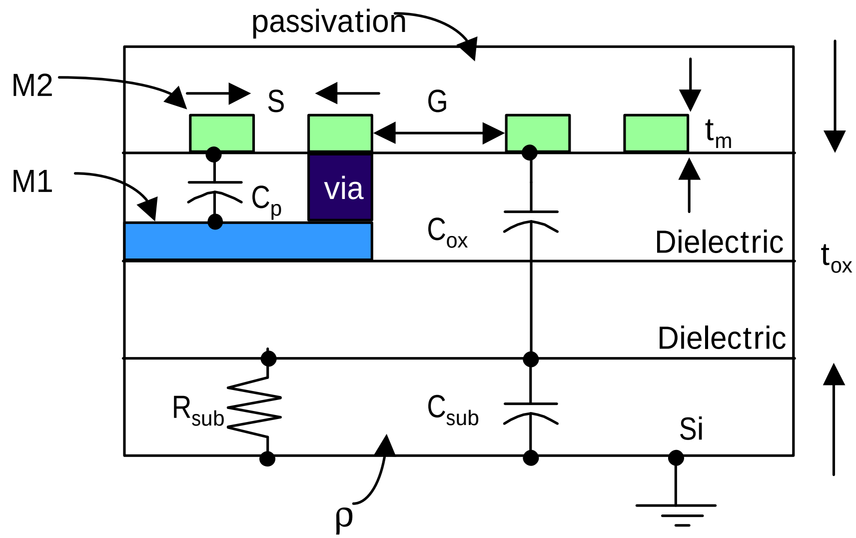
IP_3 , P_{1dB} and NFmin vs Technology



Silicon Spiral Inductor



Top View



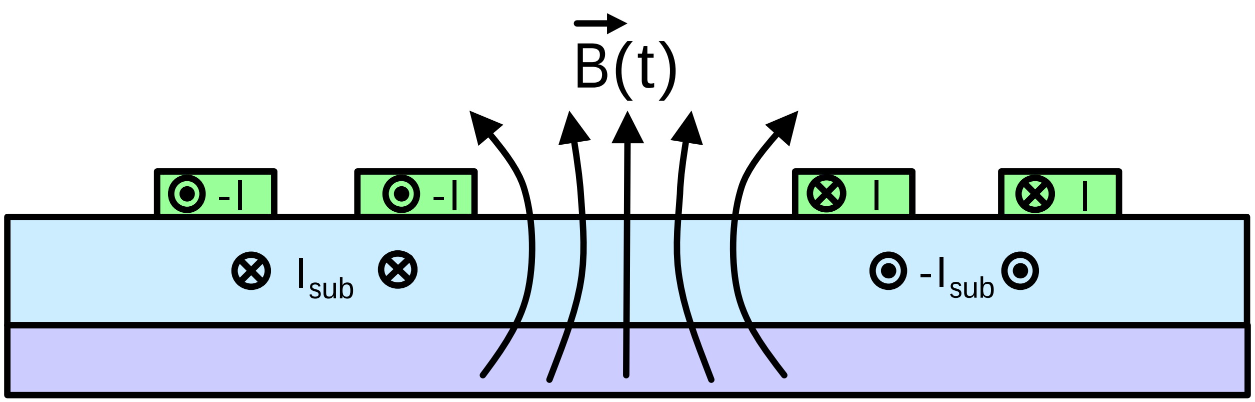
Cross Section

R_s – Series resistance
W – Width
S – Spacing
G – Inner core gap

C_{ox} – Oxide capacitance
R_{sub} – Substrate resistance
C_{sub} – Substrate capacitance
t_m – Metal thickness
t_{ox} – Oxide thickness

Substrate Loss due to Magnetic Coupling

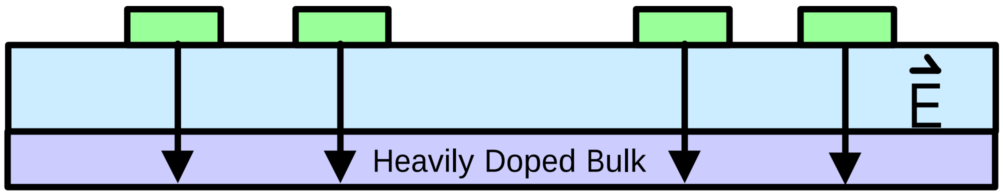
- Lenz's law – "An induced electromotive force generates a current that induces a counter magnetic field that opposes the magnetic field generating the current." $V = -N\ (\Delta\phi / \Delta t)$



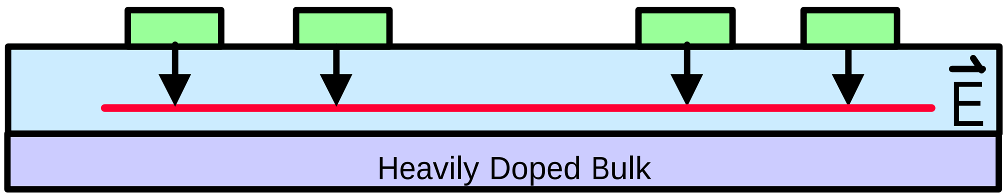
- I_{sub} reduced by high resistivity substrate

Resistive Loss in Epi due to E-Field Penetration

- Reduced by high resistivity



- Reduced by Pattern Ground Shield [1]



  - **Tradeoff: Lower self-resonant frequency f_{SR}**
- **Thicker oxide**
- **Low-k dielectric**

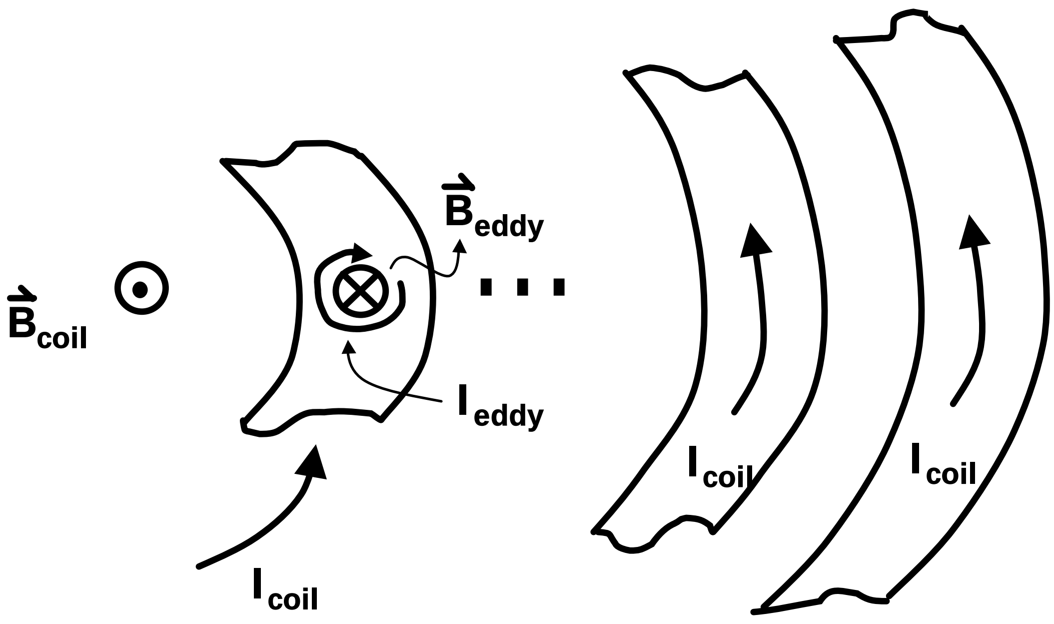
[1] C. Yue, et al, "On-chip Spiral Inductors with Patterned Ground Shields for Si-based RF IC's," JSSC, May 98, pp. 743 - 752

Conductor Loss

- Series R_s – reduce by strapping 2 or more metal lines; use Cu
- Skin effect – $$d=\sqrt{\frac{2}{m\cdot s\cdot w}}$$
- δ - skin depth, μ - permeability, σ - resistivity
  - Avoid using wide metal lines

Eddy Currents in Planar Inductor

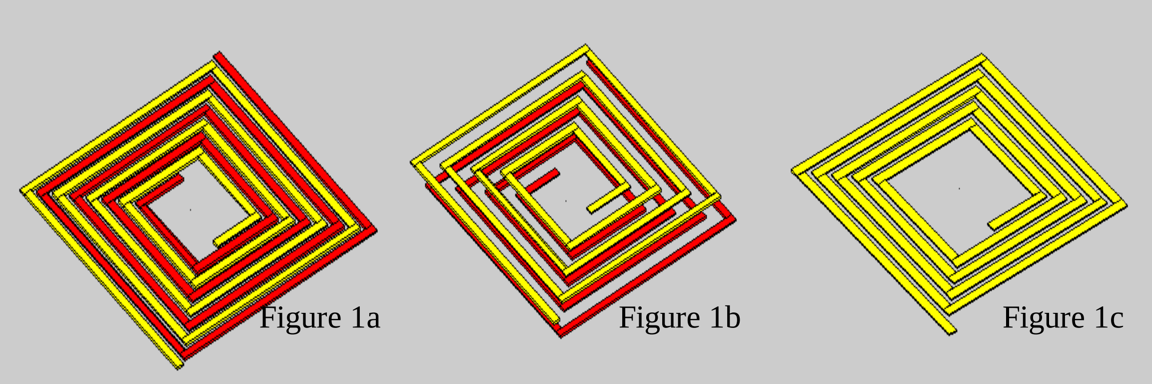
- Generation of eddy currents in the planar inductor decreases the inductance
  - **Use large inner core gap – G (120mm)**



Impact of Technology Advancement on Inductors

- More metal layers for strapping $\rightarrow$ less series resistance, R_s
- Copper metal $\rightarrow$ lower series resistance
- Low-k dielectric $\rightarrow$ improves substrate loss

Coupled Inductors/Transformers



A=planar transformer; B=stacked transformer;C=planar inductor

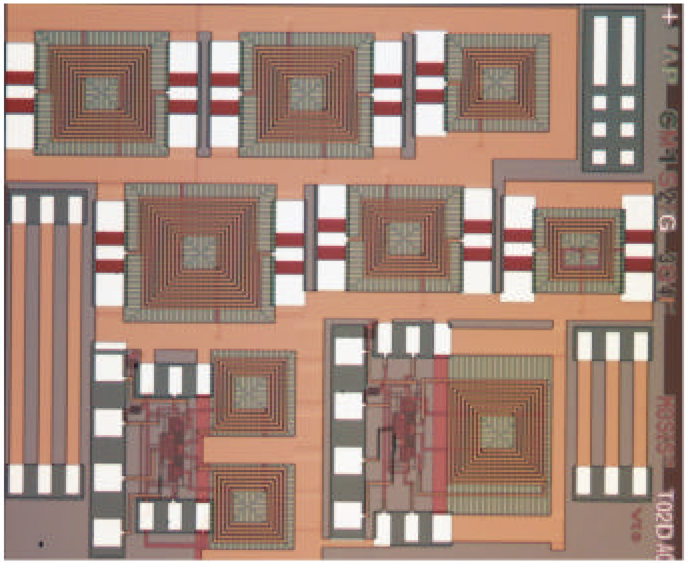


Table 1

	Structure	Number of turns	Metallization
Transformer a	Planar (Fig. 1a)	3	Metal 5
Transformer b	Planar (Fig. 1a)	4	Metal 5
Transformer c	Planar (Fig. 1a)	5	Metal 5
Transformer d	Planar (Fig. 1a)	4	Metal 5 shorted to Metal 4
Transformer e	Non-planar (Fig 1b)	4	Metal 5 spiral on Metal 4 spiral
Inductor	(Fig 1c)	5	Metal 5

0.25 mm CMOS transformer test chip

Lumped-Element Transformer Models

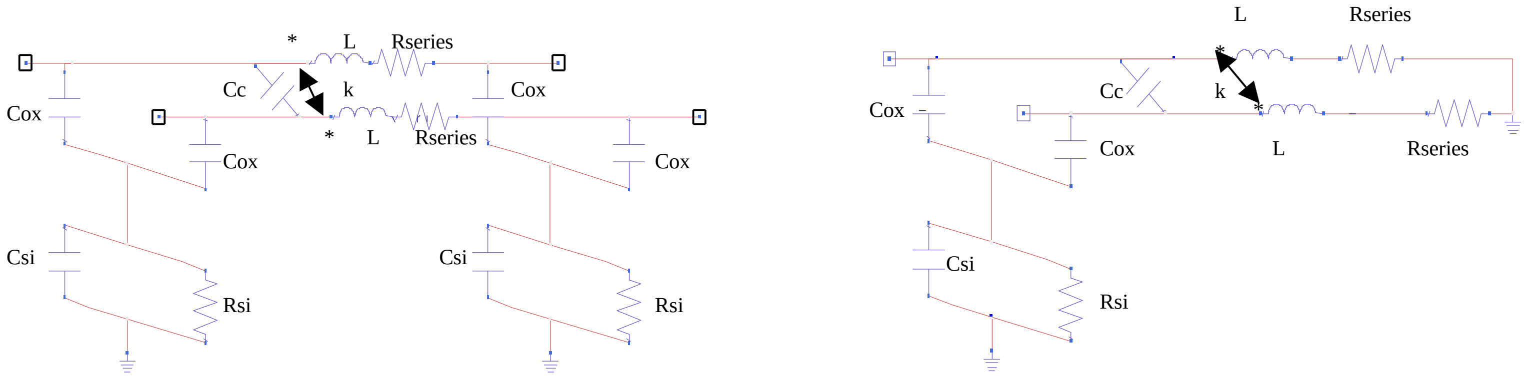


Table 2

	L(nH)	k	R (Ohms)	Cox (pF)	Cc (pF)	Csi (pF)	Rsi(Ohms)
Trans a	3.3	0.71	9.0+2.0f	0.10	0.005	0.7	8
Trans b	5.2	0.75	11+3.5f	0.18	0.01	0.0005	2
Trans c	7.9	0.79	16+5.2f	0.29	0.06	0.005	4
Trans d	5.5	0.78	8.1+3.6f	0.19	0.02	0.001	3
Trans e upper/lower	3.1 / 3.4	0.92	9.5+1.0f / 18+1.0f	0.06 / 0.21	0.10	0.001	1
Inductor	6.9		12+5.0f	0.086	0.09	0.4	6

FastHenry (MIT) used to estimate inductance; L is assumed freq. Independent above. It actually varied by about 10% from 1GHz to 4GHz so including a freq. Dependent inductance would increase model accuracy.

S11, S22 Measurements; Symmetrical Transformers

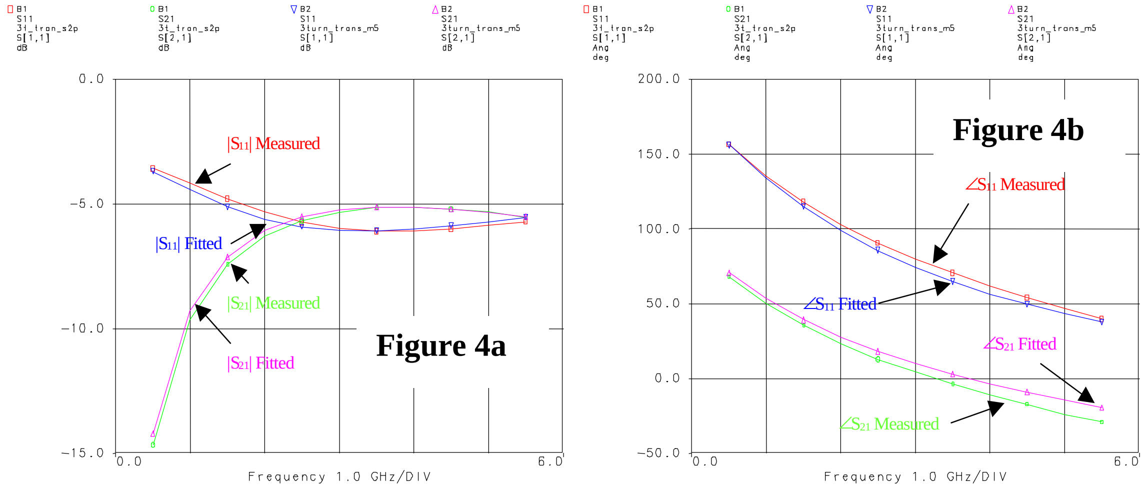


Figure 4) Measured and modeled (fitted) s-parameters for the 3-turn transformer in metal 5 (transformer a).
a) S11 and S21 magnitude, and b) S11 and S21 angle.

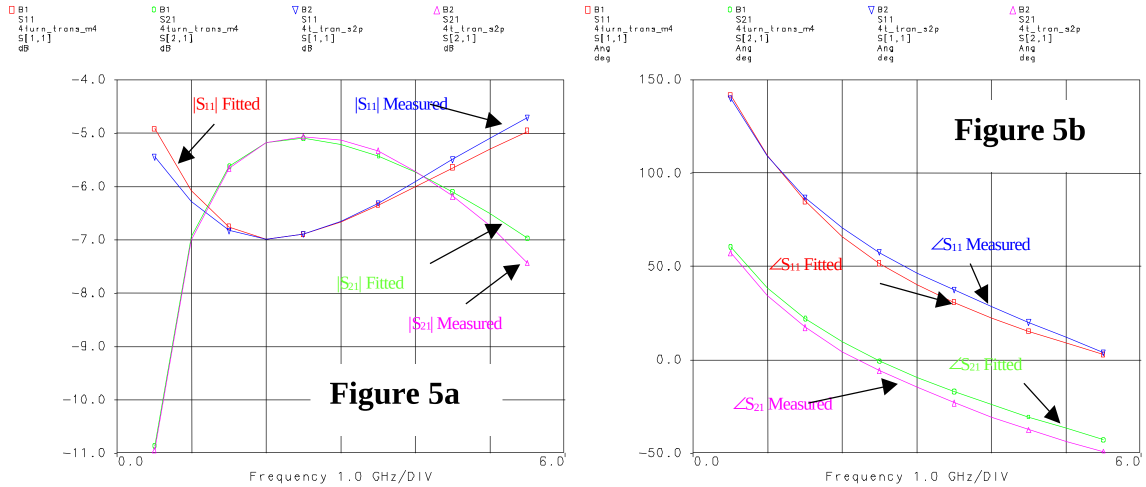


Figure 5) Measured and modeled (fitted) s-parameters for the 4-turn transformer in metal 5 (transformer b).
a) S11 and S21 magnitude, and b) S11 and S21 angle.

S-Measurements; Non-symmetrical Transformers

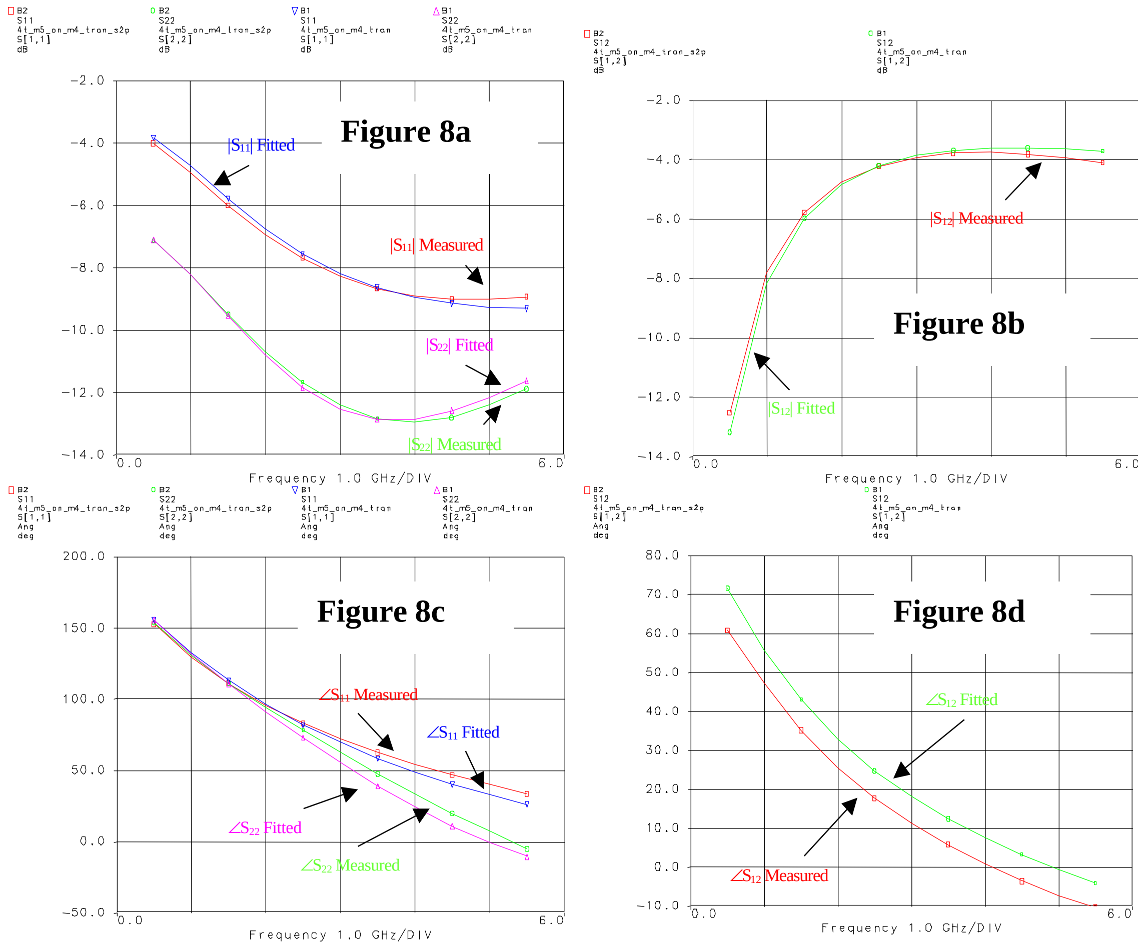


Figure 8) Measured and modeled (fitted) s-parameters for the 4-turn transformer with primary in metal 5 and secondary in metal 4(transformer e). a) S11 and S22 magnitude, b) S12 magnitude (identical to S21), c) S11 and S22 angle, d) S12 angle (identical to S21).

Transformer/Inductor Q-Factor/Resonant Freq

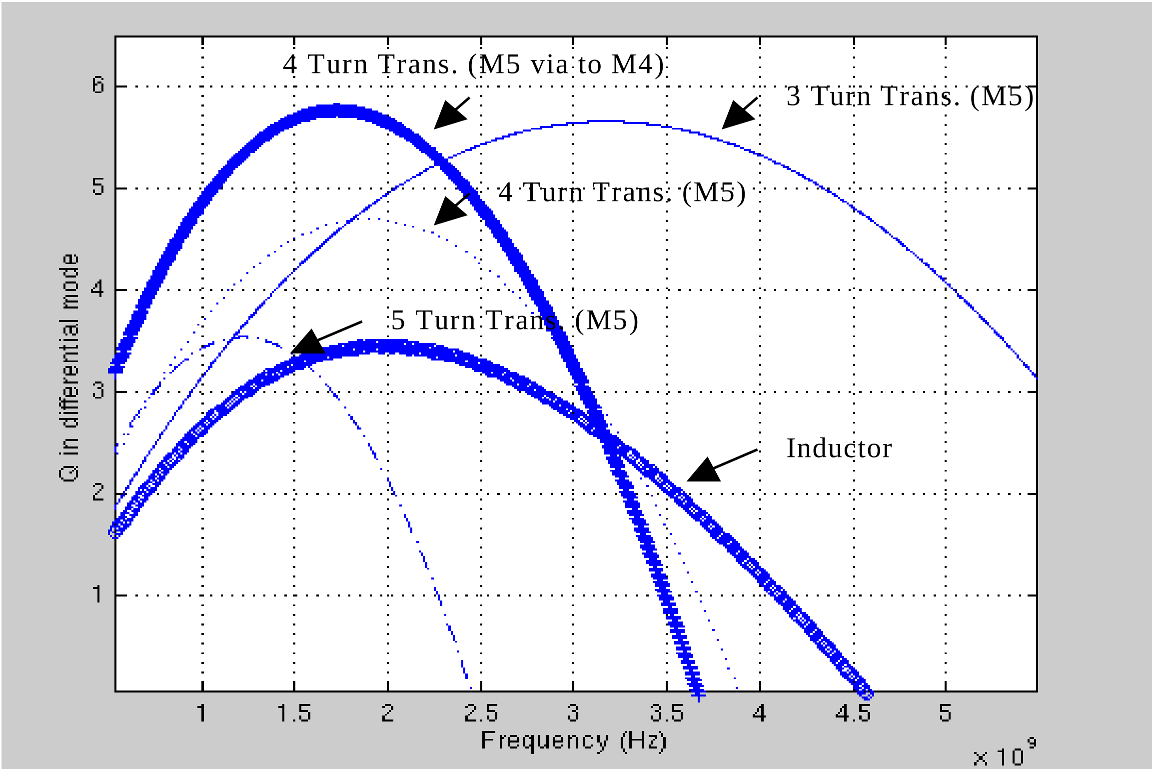
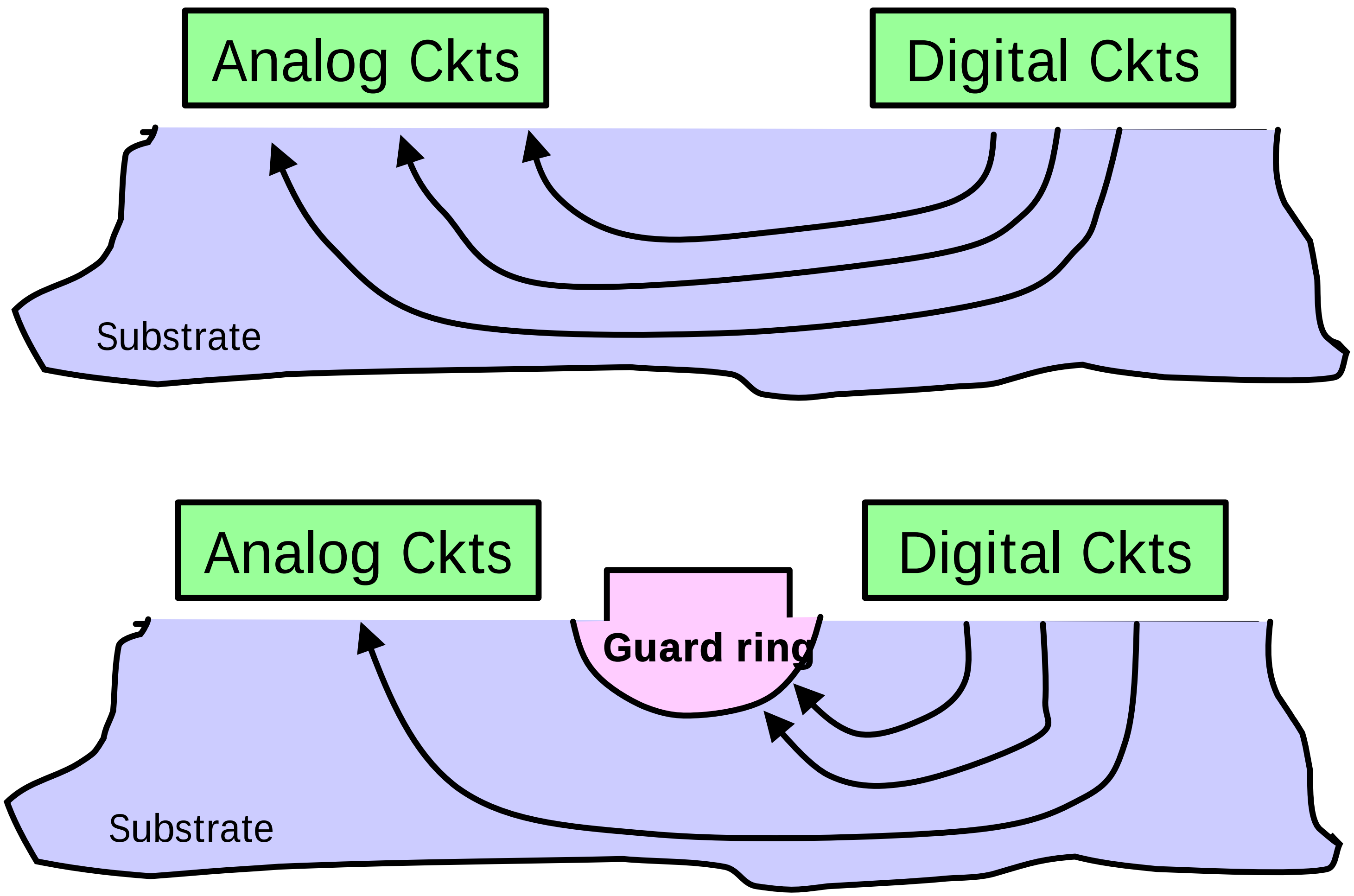


Table 3

	L (nH)	Q	SRF (GHz)
Trans a differential mode	5.6	5.6 peak @3.2GHz	6.7
Trans b differential mode	9.1	4.8 peak @2.0GHz	3.9
Trans c differential mode	14	3.6 peak ? @1.3GHz	2.5
Trans d differential mode	9.8	5.9 peak @1.7GHz	3.7
Inductor	6.9	3.5 peak @2.0GHz	6.5

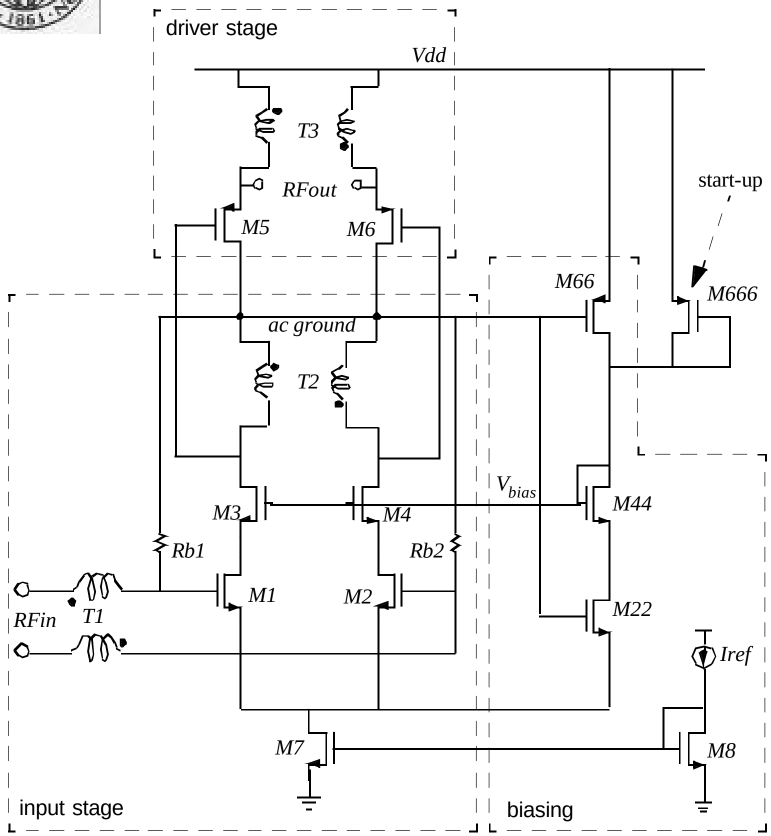
Substrate Noise Effects

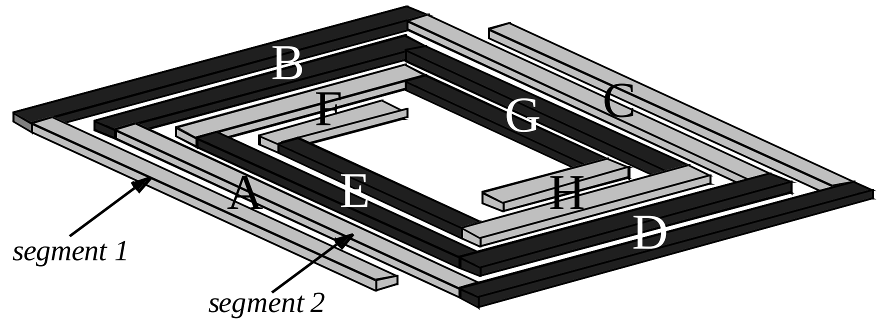


Isolation of Substrate Noise in Differential Circuits

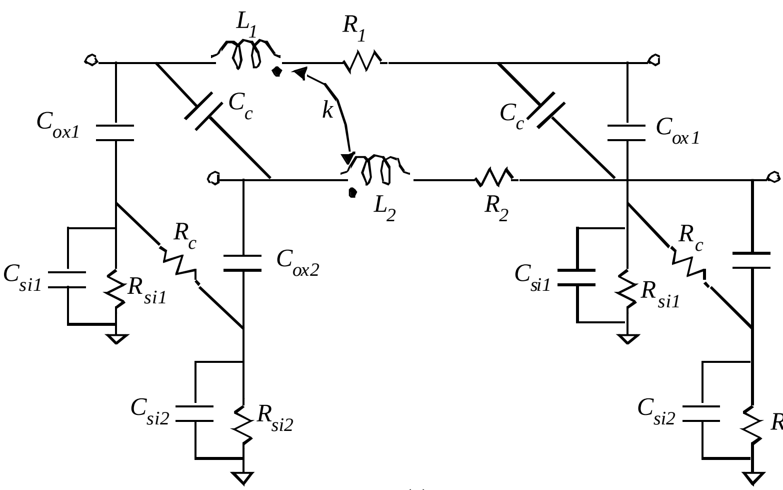
- Excellent substrate noise isolation was found in differential circuits
  - All noise signals coupled to the substrate appear as common mode signals on the differential outputs

900 MHz CMOS Low-Noise Amplifier





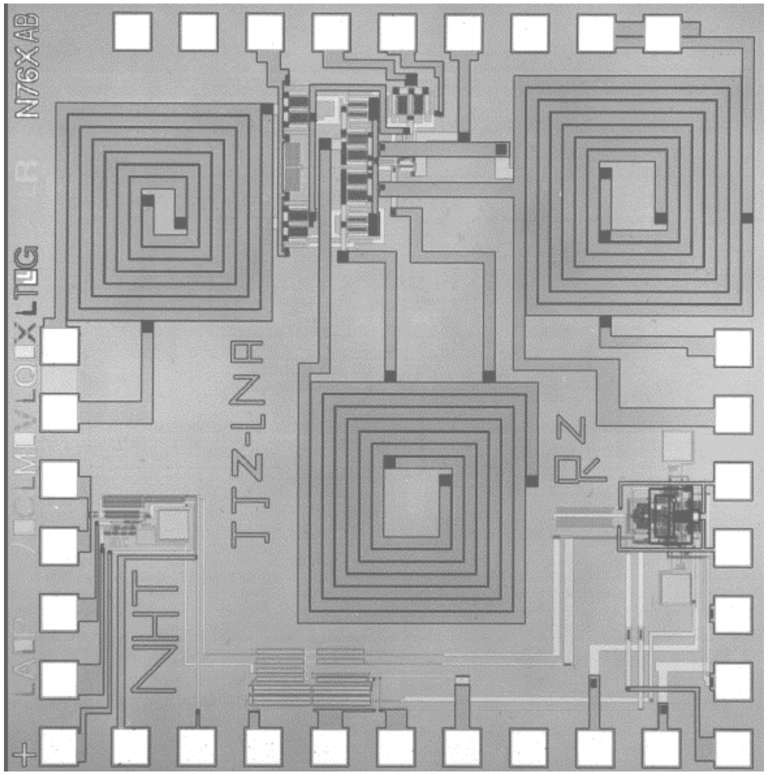
(b)



(c)

- First fully-differential CMOS LNA and first CMOS RF circuit to employ monolithic transformers

900 MHz CMOS Low-Noise Amplifier (cont.)



• J.J. Zhou and D.J. Allstot, "A fully-integrated CMOS 900 MHz LNA using monolithic transformers," *ISSCC Digest of Technical Papers*, pp. 132-133, Feb. 1998.

• J.J. Zhou and D.J. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE J. Solid-State Circuits*, pp. 2020-2027, Dec. 1998.

• Supply Voltage = 3 V

• Power Dissipation = 18 mW

• Noise Figure = 4.1 dB

• S21 = 12.3 dB; S12 = -33.0 dB

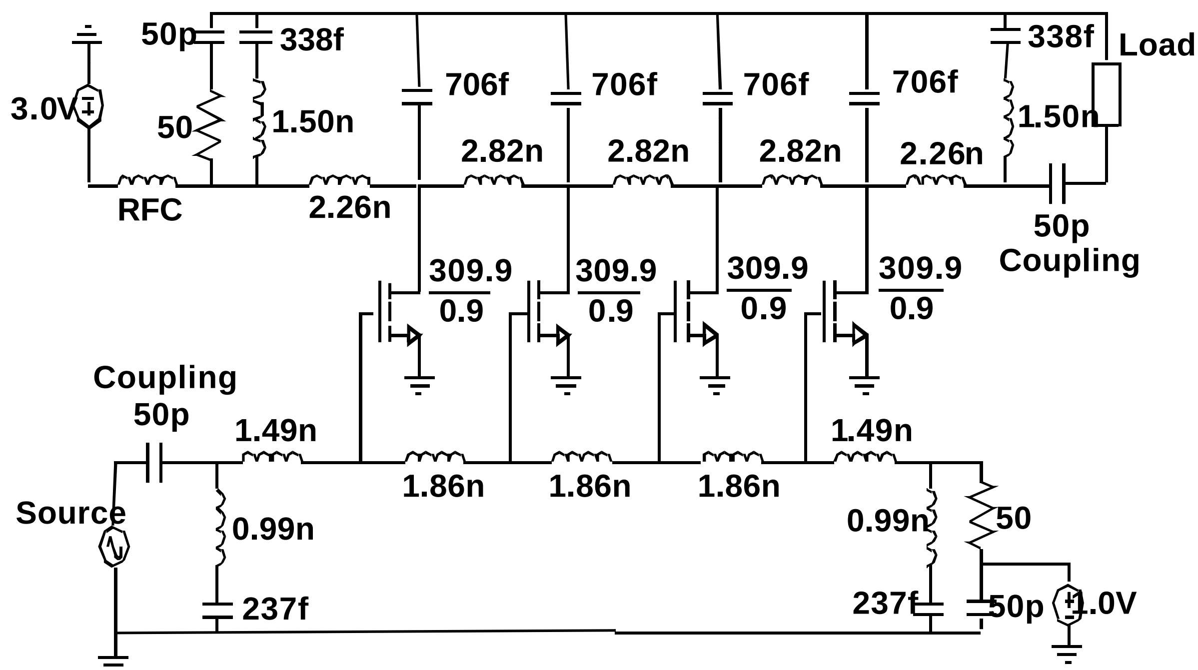
• 1 dB Compression (input) = -16dBm

• Technology: 3-metal 0.6um CMOS

• Key Trend: Fully-Differential RF Circuits to Reject Switching Noise

0.5-5.5 GHz 5 dB CMOS Distributed Amplifier

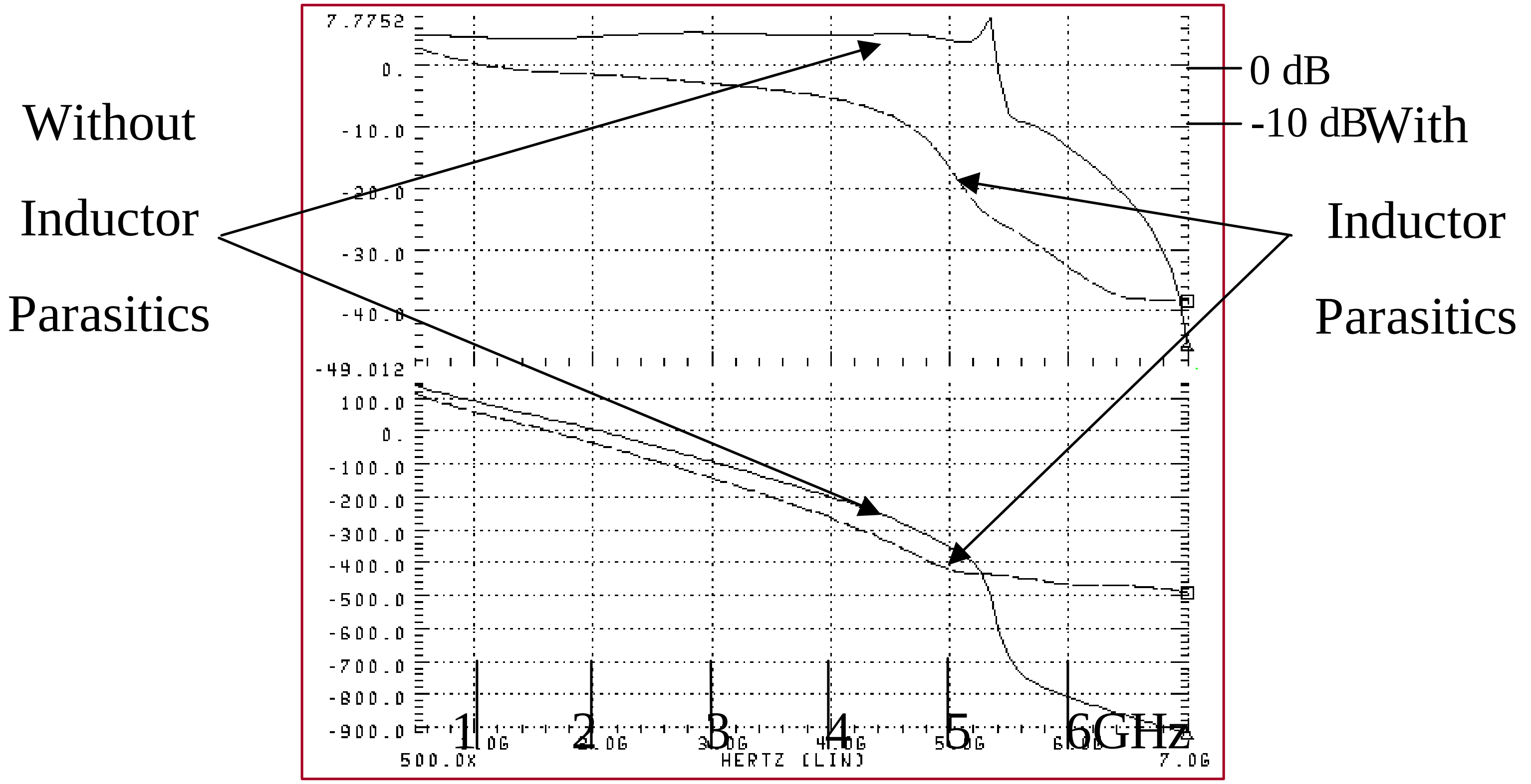
Initial Analytic Design



Another key trend: Parametric modeling and aggressive optimization

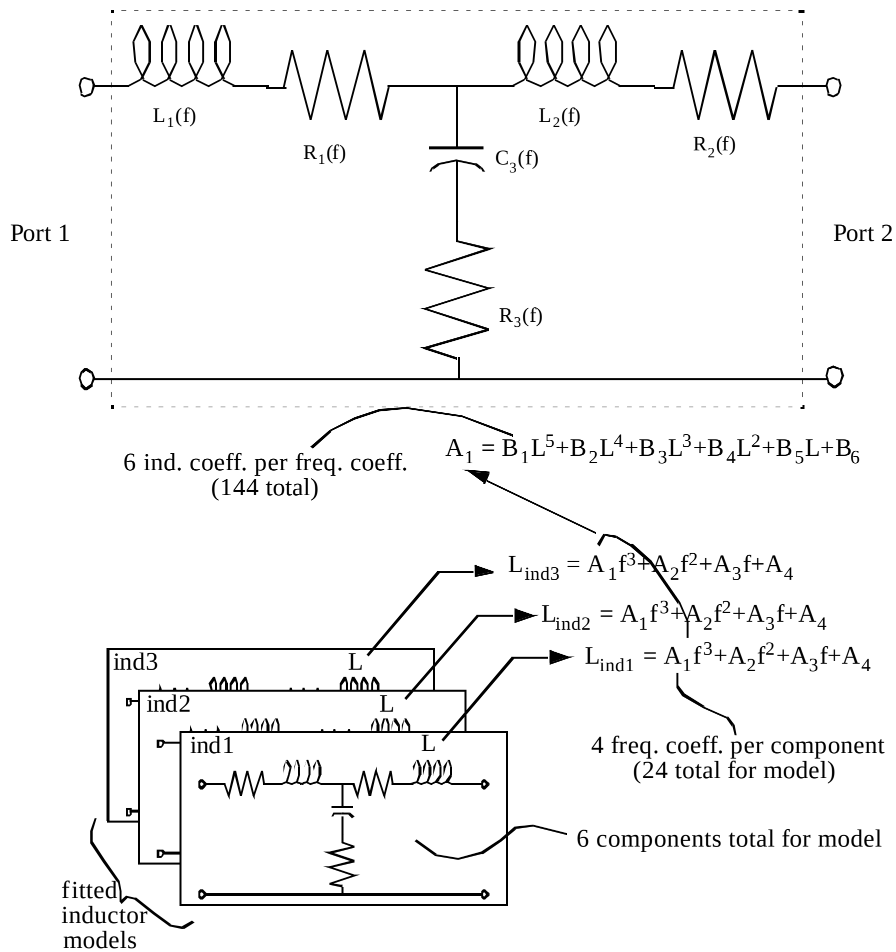
0.5-5.5 GHz 5 dB CMOS Distributed Amplifier (cont.)

Initial Design--Simulation Results with and w/o Inductor Parasitics



Poor Response. Smith Chart? Parasitic-Aware Design!

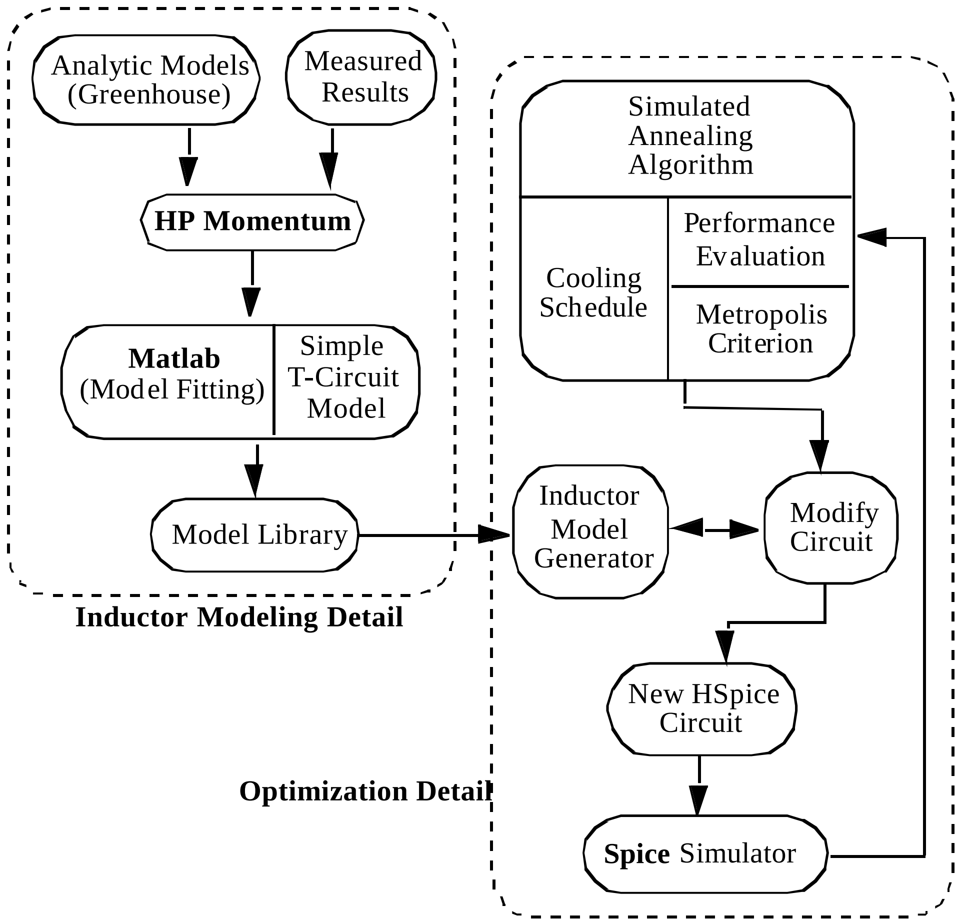
Parametric Inductor Modeling: Analytic/Experimental



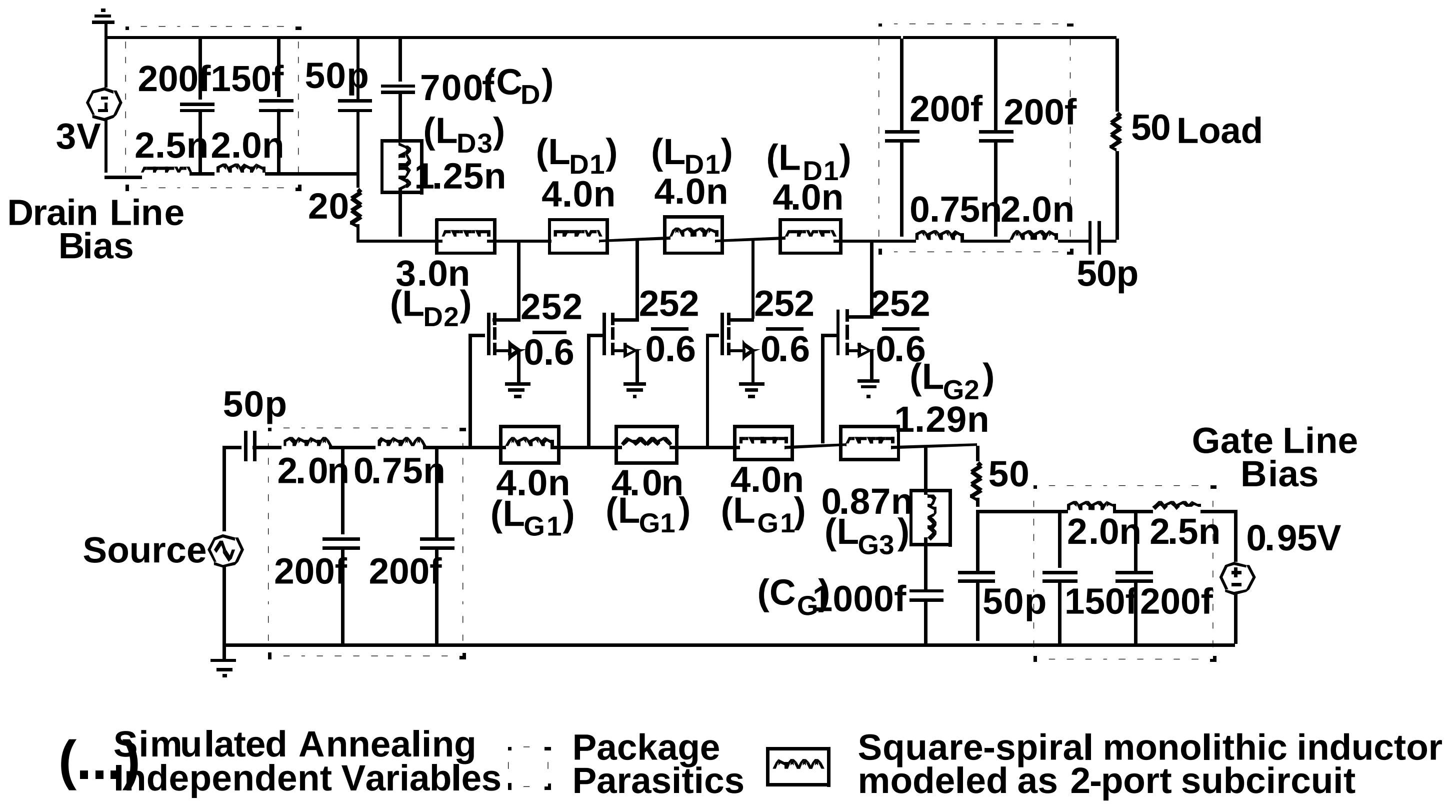
3 Measured Inductors: (Min, Mid, Max) Fit Measured S Params to *MOMENTUM*. Use *MOMENTUM* for Interpolation

Simulated Annealing Optimization Loop

Key Result for RF Design



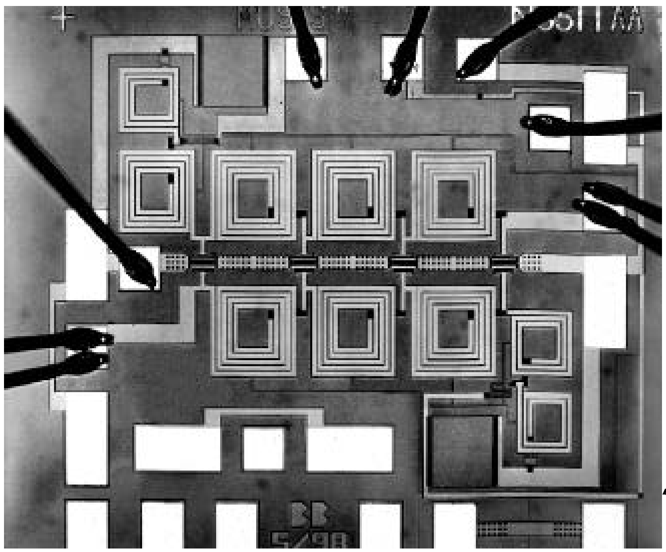
0.5-5.5 GHz CMOS Distributed Amplifier

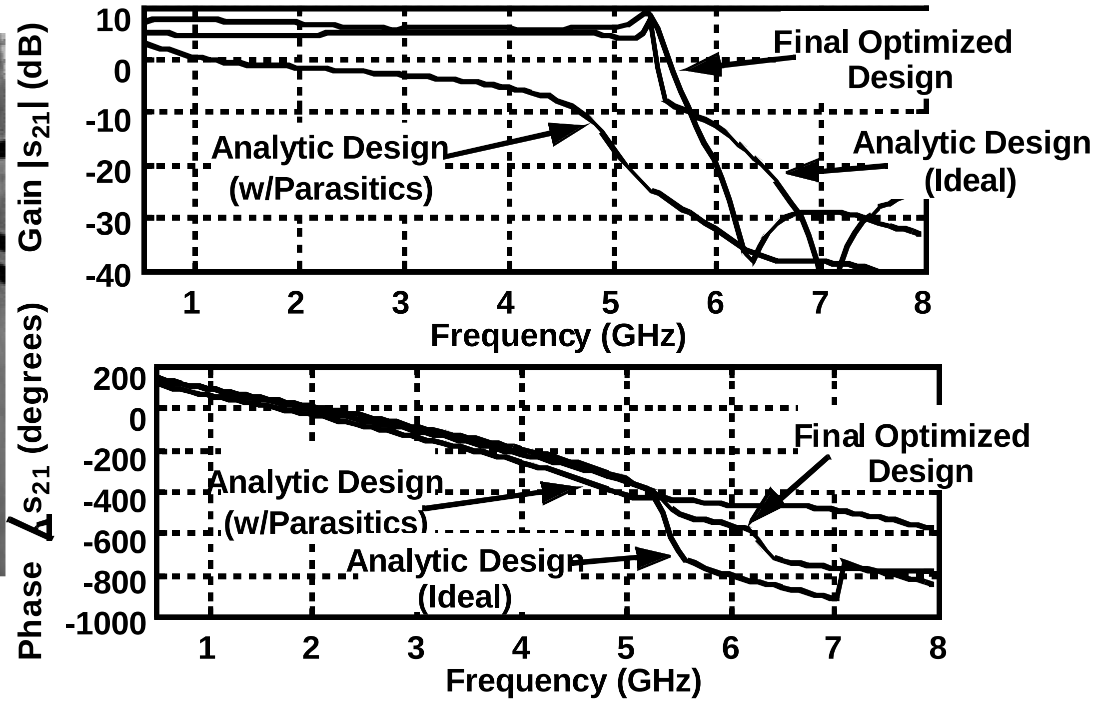


• First fully-monolithic 0.6 μm CMOS DA and first to be synthesized using simulated-annealing custom CAD tool.

0.5-5.5 GHz CMOS Distributed Amplifier (cont.)

Test Results from Single-Ended Dist. Amplifier



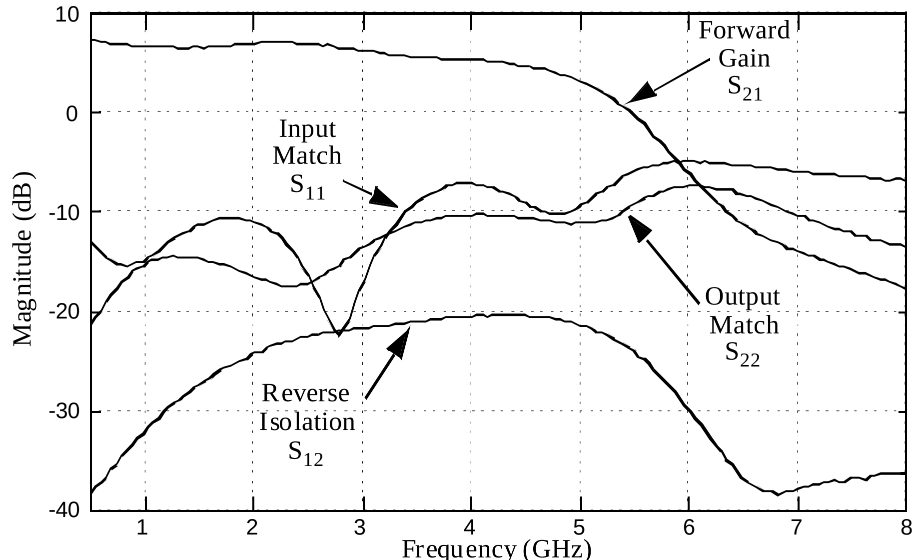


0.79mmxmm; 0.6um CMOS

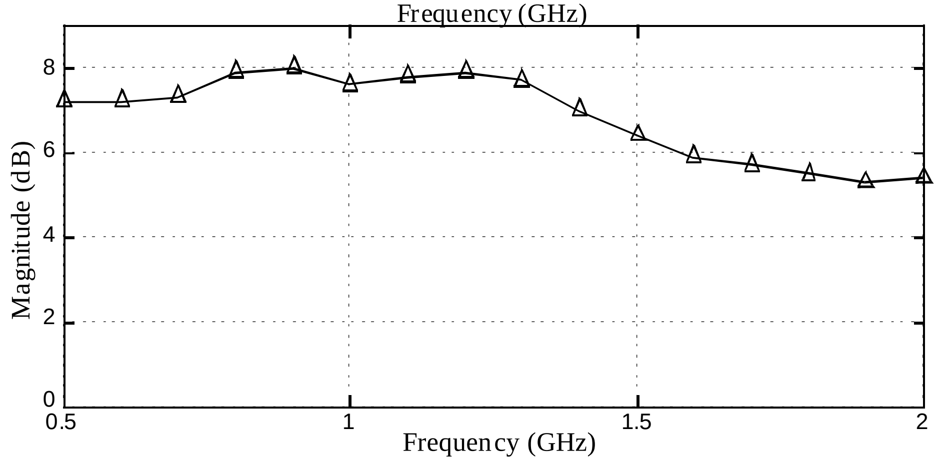
- B. Ballweber, R. Gupta, and D.J. Allstot, "Fully-integrated CMOS RF amplifiers," *ISSCC Digest of Technical Papers*, pp. 72,73,448, Feb. 1999.

- B. Ballweber, R. Gupta, and D.J. Allstot, "A fully-integrated 0.5-5.5 GHz CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, pp. 231-239, Feb. 2000.

0.5-5.5 GHz CMOS Distributed Amplifier (cont.)



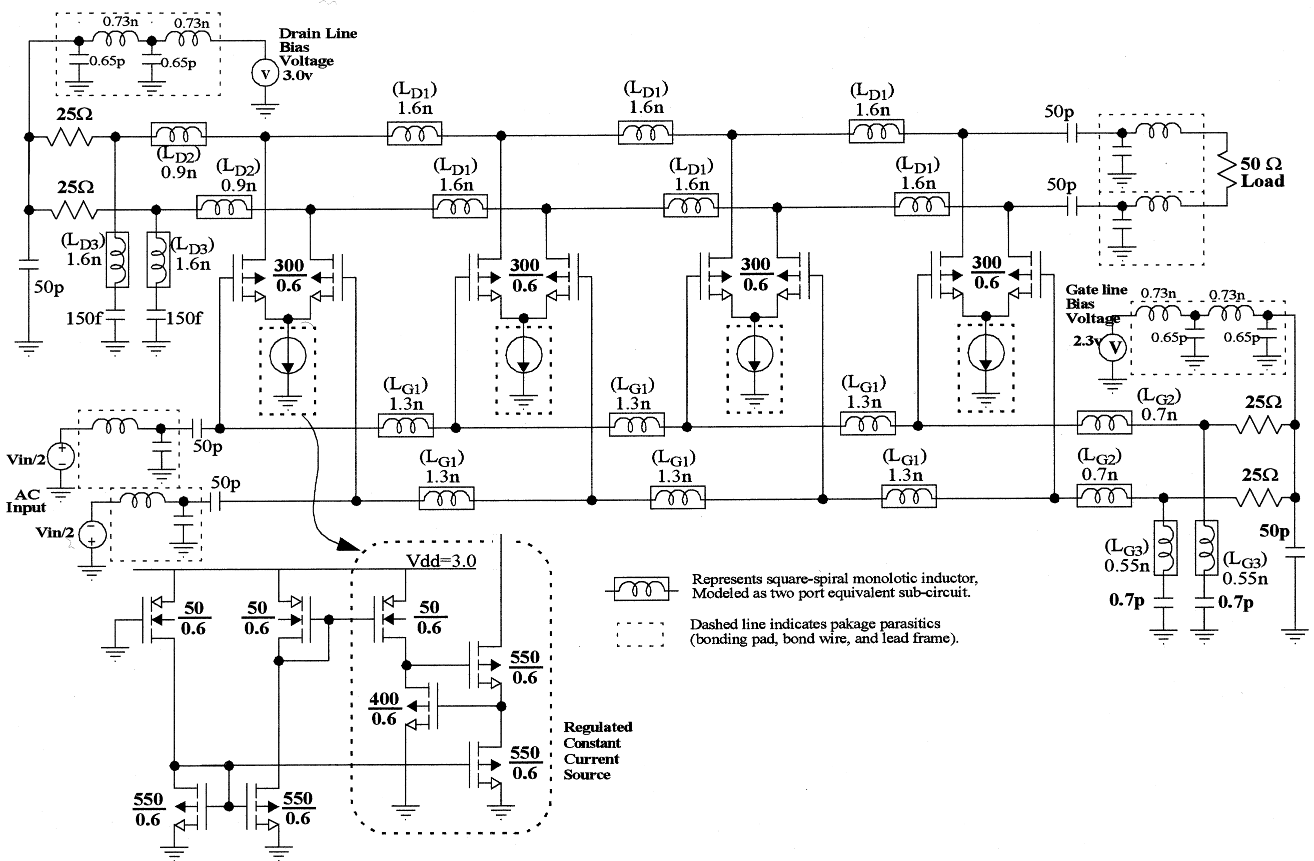
Measured s-parameter values



Measured NF (1.8GHz)

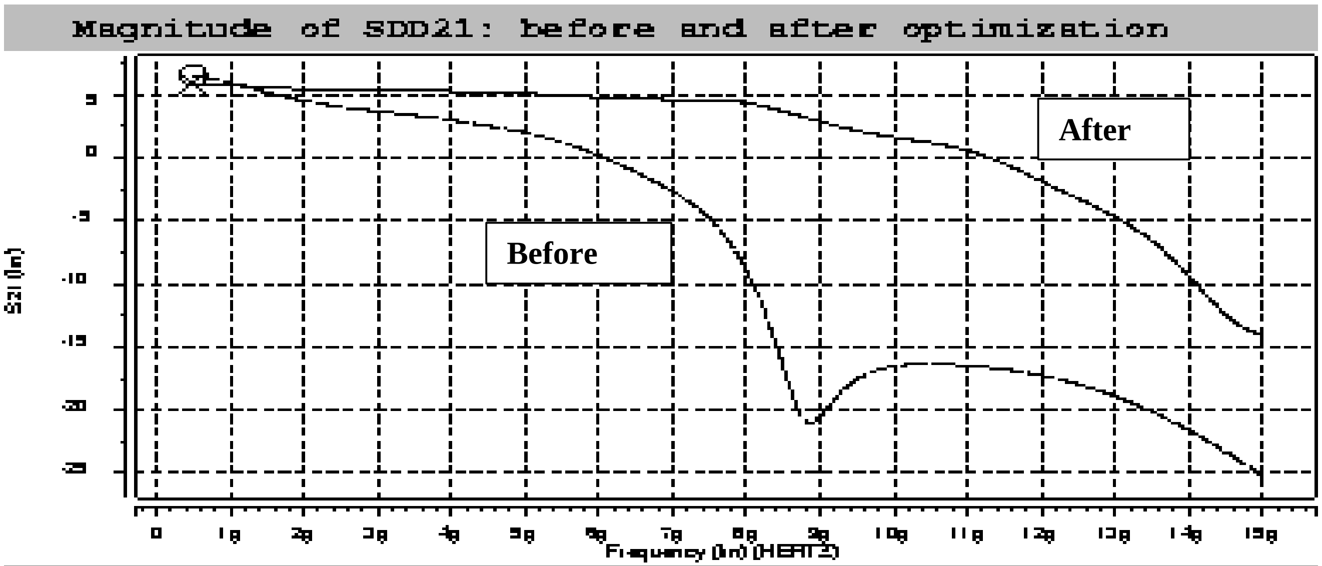
Power Dissipation = 83mW

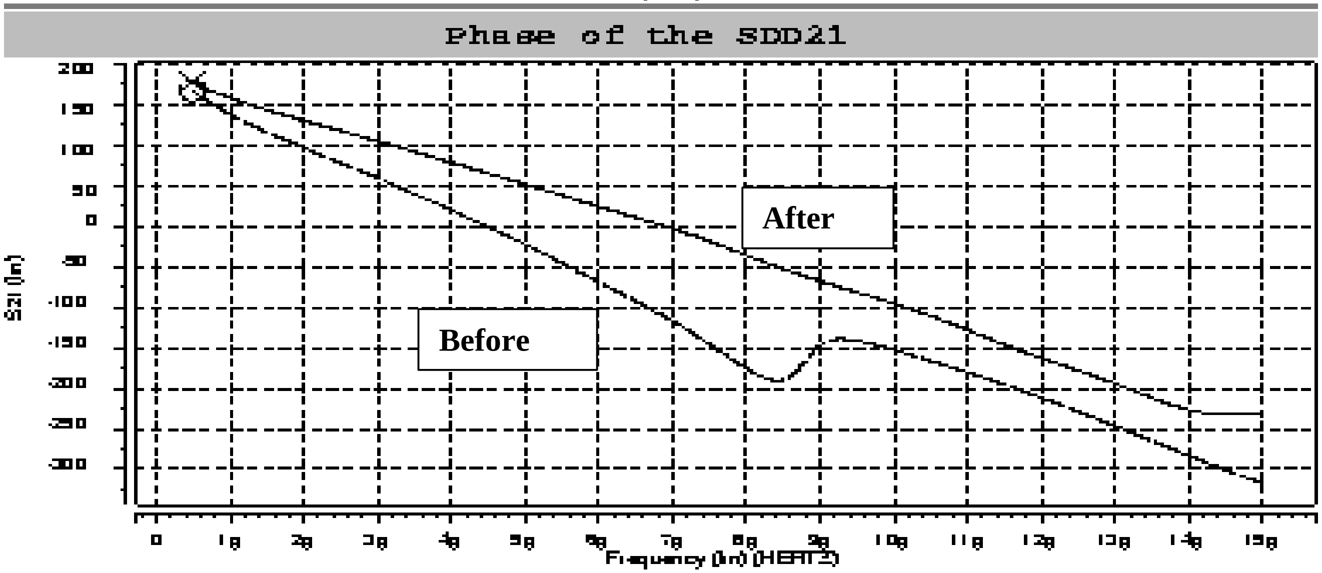
0.5-8.5 GHz CMOS Fully-Differential Dist. Amplifier



• First fully-monolithic fully-differential 0.6 μm CMOS DA. Key Idea: Wideband due to elimination of inductor source degeneration. Also achieves digital switching noise rejection.

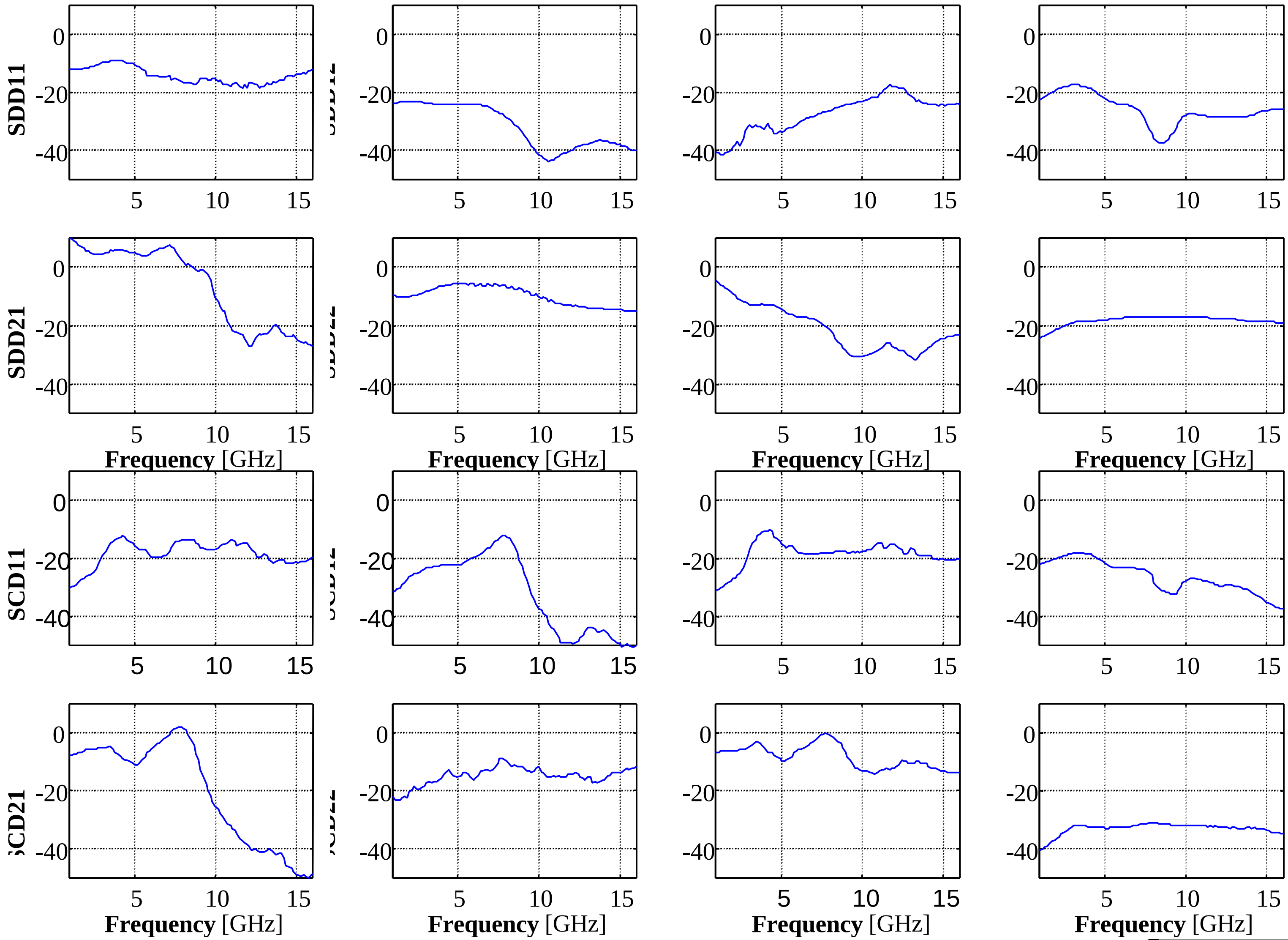
Simulations--Simulated Annealing Optimization





0.5-8.5 GHz CMOS Fully-Differential Dist. Amplifier

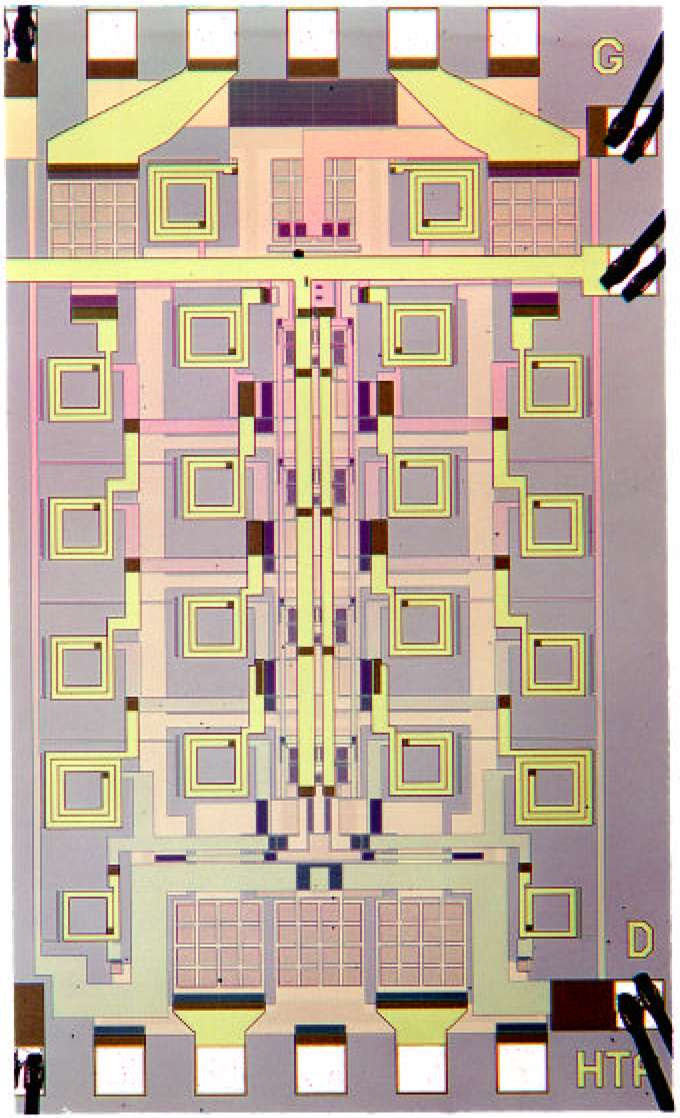
Measured mixed-mode S-parameters in [dB] of fully-differential distributed amplifier



Comparative Results--Single-ended v/s Differential

	Fully-Differential Distributed Amplifier	Single-ended Distributed Amplifier [9]
Differential Gain, S_{DD21}	5 ± 1.5dB (1.5 - 7.5GHz)	6.1 ± 1.3dB (0.5 – 4GHz)
Unity Gain Bandwidth	8.5GHz	5.5GHz (Probed) 4GHz (Pakaged)
Noise Figure	8.7 – 13dB (1 – 2GHz)	5.4 – 8.2dB (1 – 2GHz)
Isolation, S_{DD12}	-22dB	-20dB
Power dissipation	216mW (V_{DD}=3.0V)	103.8mW (V_{DD}=3.0V)
Chip Size	1.3mm x 2.2mm	1.4mm x 0.8mm
Technology	0.6µm standard CMOS	0.6µm standard CMOS

0.5-8.5 GHz CMOS Fully-Diff. Dist. Amp. (cont.)

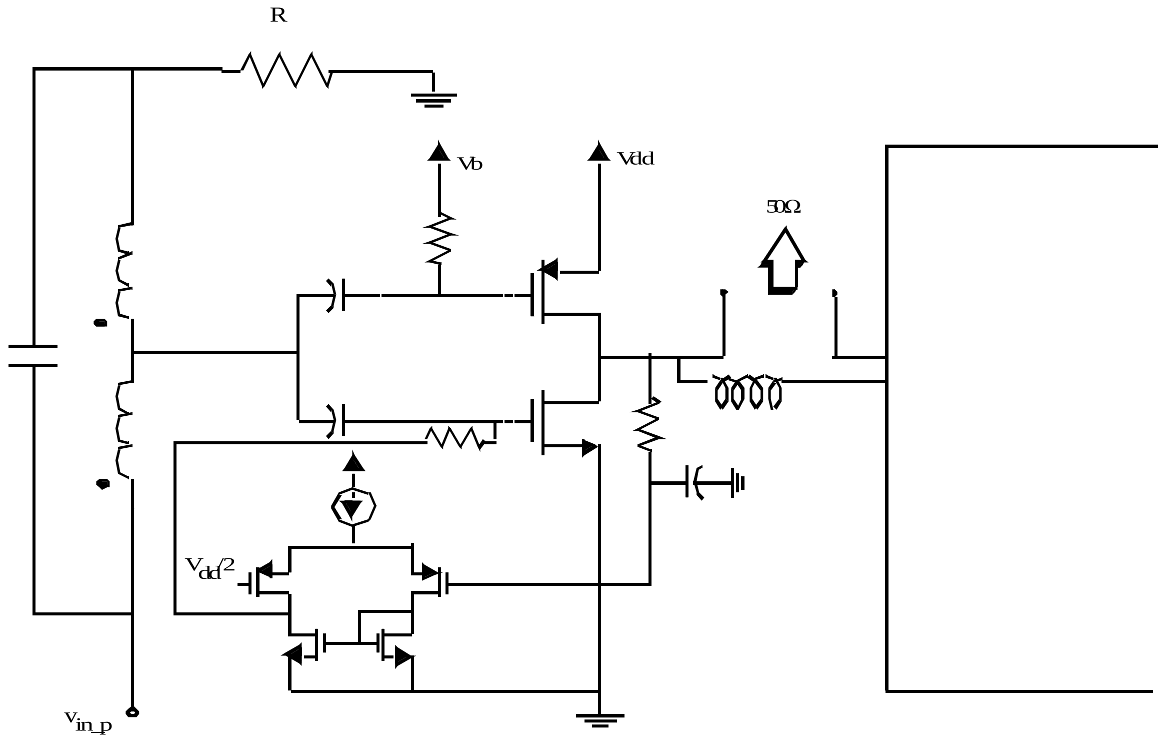


• H.-T. Ahn and D.J. Allstot, "A 0.5-8.5 GHz fully-differential CMOS distributed amplifier," *IEEE J. Solid-State Circuits*, 2001. (To appear)

Note: Hee-Tae Ahn is currently with National Semiconductor, Inc.

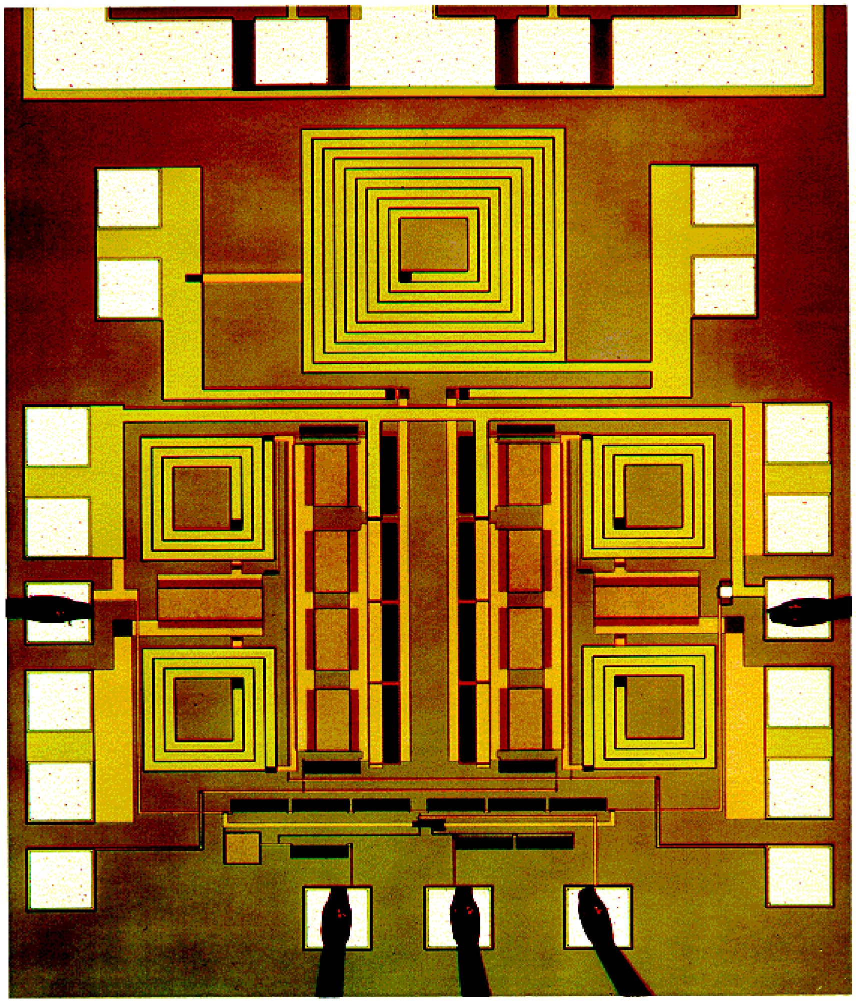
Key Points: Fully-Differential Topologies for rejection of digital switching noise and elimination of some inductive feedback effects. Simulated annealing optimization for robust design accuracy.

900 MHz CMOS Class-C Power Amp Output Stage



• First fully-monolithic fully-balanced 0.6 μm CMOS PA. Achieved 55% drain efficiency due to inductor modeling/CAD optimization (basically simulated-annealing *load-pull* method).

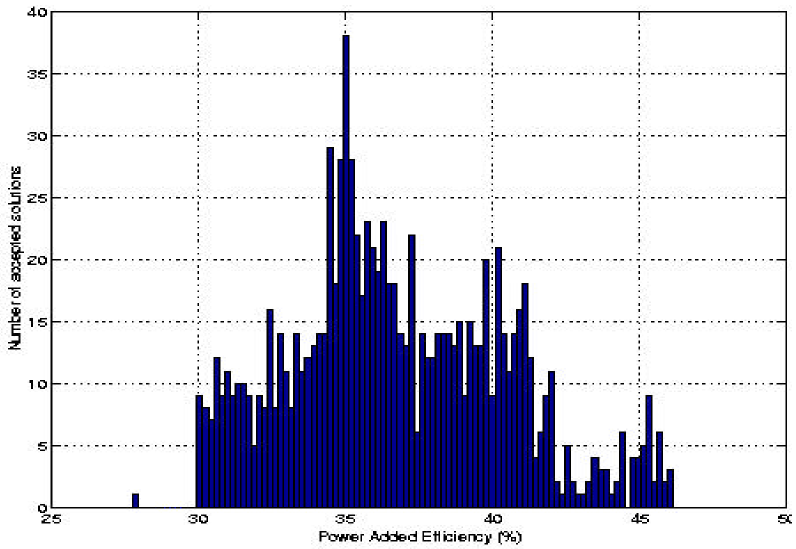
900 MHz 100 mW CMOS Class-C Power Amp (cont.)

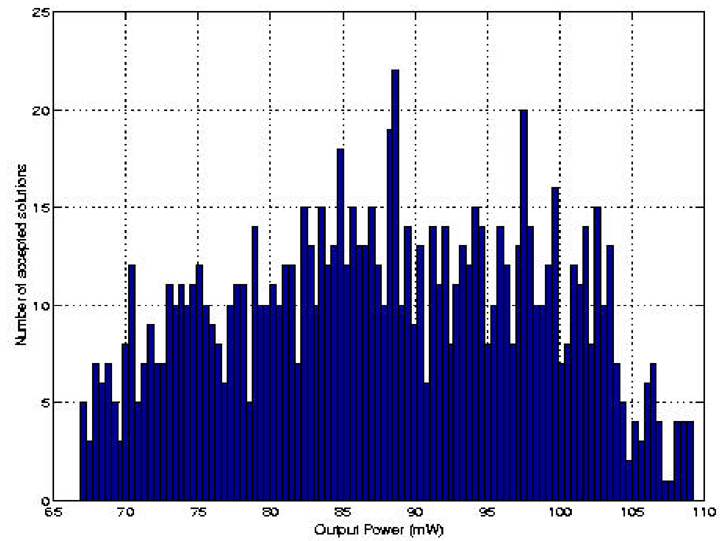


- R. Gupta and D.J. Allstot, "Fully-Monolithic CMOS RF Power Amplifiers: Recent Advances," *IEEE Communications Magazine*, vol. 37, pp. 94-98, April 1999.
- R. Gupta, B. Ballweber, and D.J. Allstot, "Design and optimization of CMOS RF power amplifiers," *IEEE J. Solid-State Circuits*, Jan. 2001.
- S21 = 6.0 dB
- S11 = -6.15 dB
- S12 = -25.6 dB
- PAE = 30 %

Simulated Annealing Statistical Design Space

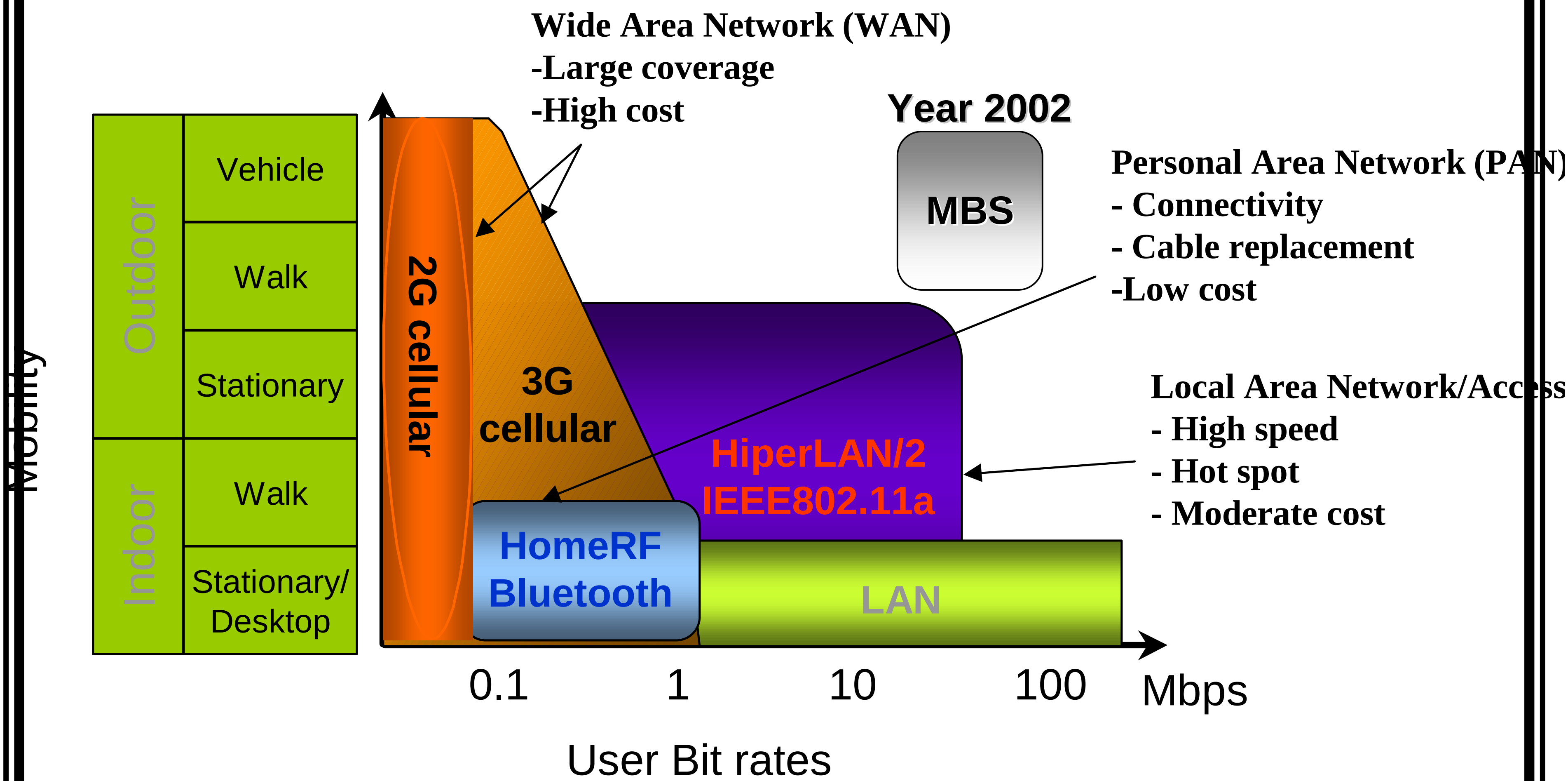
Simulated Annealing does not guarantee an optimimum solution; Acceptable solutions are statistical in nature.





Simulated Annealing is computationally intensive: 40,000 simulations for PA Output Stage; 4 days on Sun Ultra-10

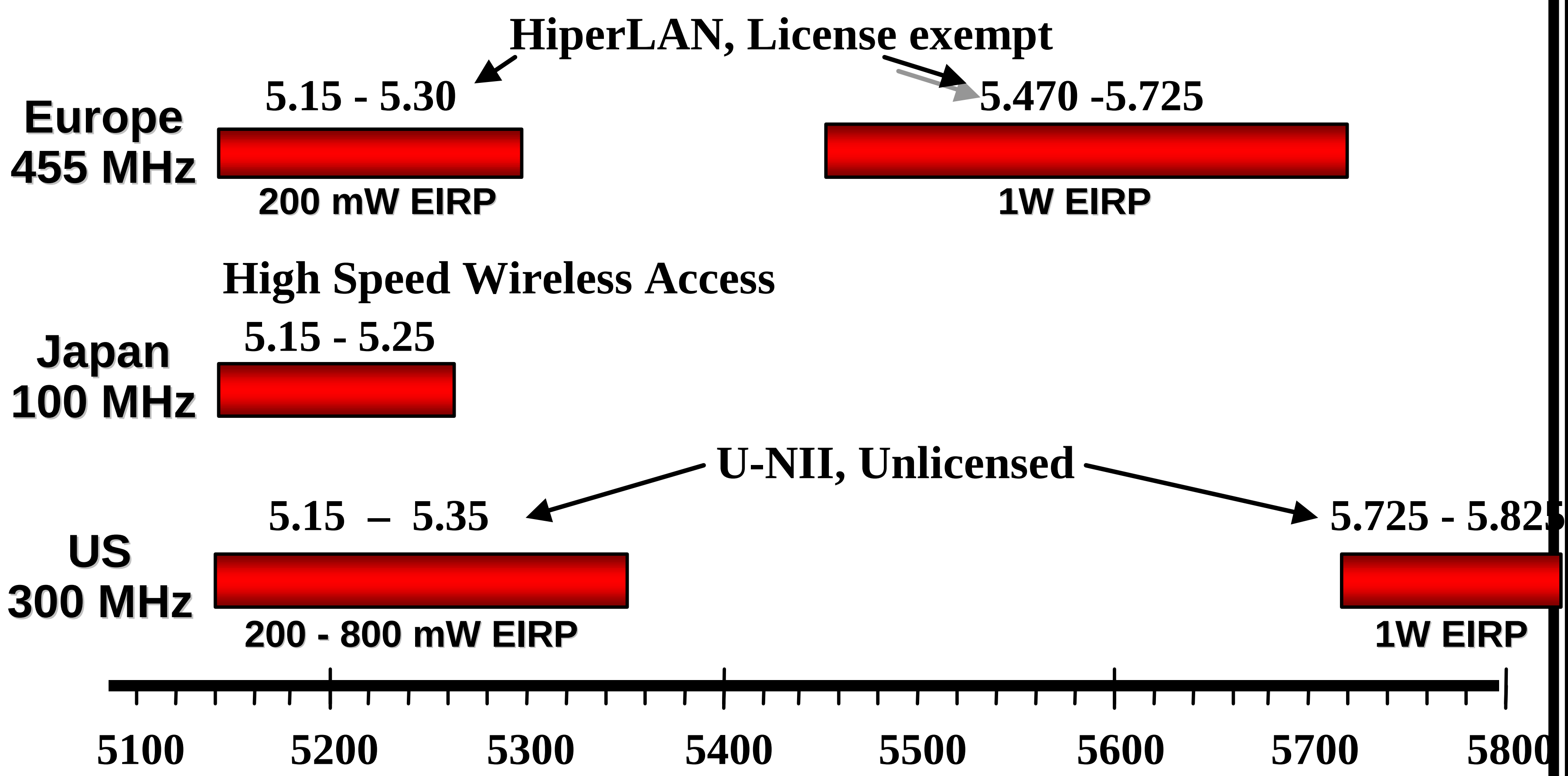
Past, present and future



HIPERLAN family

HIPERLAN TYPE 1 Wireless LAN	HIPERLAN TYPE 2 Wireless ATM Indoor access	HIPERLAN TYPE 3 Wireless ATM Remote access	HIPERLAN TYPE 4 Wireless ATM Interconnect
MAC	DLC	DLC	DLC
PHY (5 GHz) 20 + Mbps	PHY (5 GHz) 20 + Mbps	PHY (5 GHz) 20 + Mbps	PHY (17 GHz) 150 + Mbps

Spectrum allocation @ 5 GHz



Conclusions

- Fast improvement in RF Devices v/s scaling trends
- Slow improvement in Passive devices v/s scaling trends
- Implementation of Fully-Differential RF circuits ... A la mixed-signal circuits in recent years
- Modeling/Optimization key to robust RF designs
- CMOS RF Wireless LAN at 5GHz (Atheros, Radiata, etc.) Products are here!
- Seamless Multi-Standard CMOS Radios (Bluetooth, 802.11, etc. -- Mobilian Corporation -- neat products coming!