Electron Devices Society

UCF

Reliability of Advanced CMOS Devices and Circuits

Presented by:

The IEEE Orlando Section EDS Chapter and the IEEE UCF Student Branch

Speaker

Jim Stathis received the bachelor's in physics from Washington University in St. Louis (1980), and the Ph.D. in physics from the Massachusetts Institute of Technology (1986), joining the IBM Research Division the same year. At IBM the focus of his work has been the electrical properties of point defects in SiO2, including basic studies of defect structure using magnetic resonance and electrical measurement techniques, and the role of defects in wearout and breakdown. He is the author or coauthor of more than 100 research papers and over 60 invited talks. From November 2005 to February 2007 he served as Technical Assistant to the Vice President for Science and Technology, IBM Research Division. In February 2007 he became manager of High-k/Metal-Gate Characterization and Reliability, IBM Research. Jim has served on technical program committees for SISC, INFOS, IRPS, ESREF, IPFA, MIEL and other conferences, served as Chair of the dielectrics sub-committee for the 2003 IRPS in Dallas, and is on the IRPS management committee. He was the Technical Program Chair for IRPS 2009 and is Vice-General Chair for IRPS 2010. He has presented tutorials on CMOS reliability at IRPS, ESREF, MRS, and IPFA and is an Associate Editor of the journal Microelectronics Reliability. He is a Senior Member of IEEE and a Fellow of the American Physical Society.

Time and Location

Friday, December 4th, 11am

ENG2-203 (Near the Atrium)

Abstract

As MOSFET devices have scaled to nanometer dimensions, dielectric reliability has remained as a central focus of fundamental research and reliability engineering studies. The recent introduction and rapid maturation of complex hafnium-based gate insulators with metal gates has further intensified the study of the two dominant gate oxide failure mechanisms -- dielectric breakdown and the so-called bias/temperature instability. Ultimately, the importance of these mechanisms depends on the degree to which they impact integrated circuit functionality and performance over the lifetime of a product. In this talk we will discuss new physical understanding of dielectric wearout mechanisms and statistics, and describe how these concepts may be used to estimate circuit failure rates under use conditions.

Refreshments will be provided

For More Information Contact:

Slavica Malobabic smalobabic@ieee.org Vinit Todi vtodi@mail.ucf.edu