IBM Systems and Technology Group - SRDC

Beyond Scaling

– Teaching the Old Dog some New Tricks!

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What I'd like to discuss with you today:

The Limits of Classical Scaling
Strain engineering, Hi k .

On-chip memory
SRAM & DRAM

Autonomic Chips

Power Supply
decoupling

Laser vs electonic Fuses
BIST and BISR
Self monitoring and self
repairing chips

What
about 3D

The Humble
capacitor

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There is only one reason to scale:

Performance,
Power

Miniaturization

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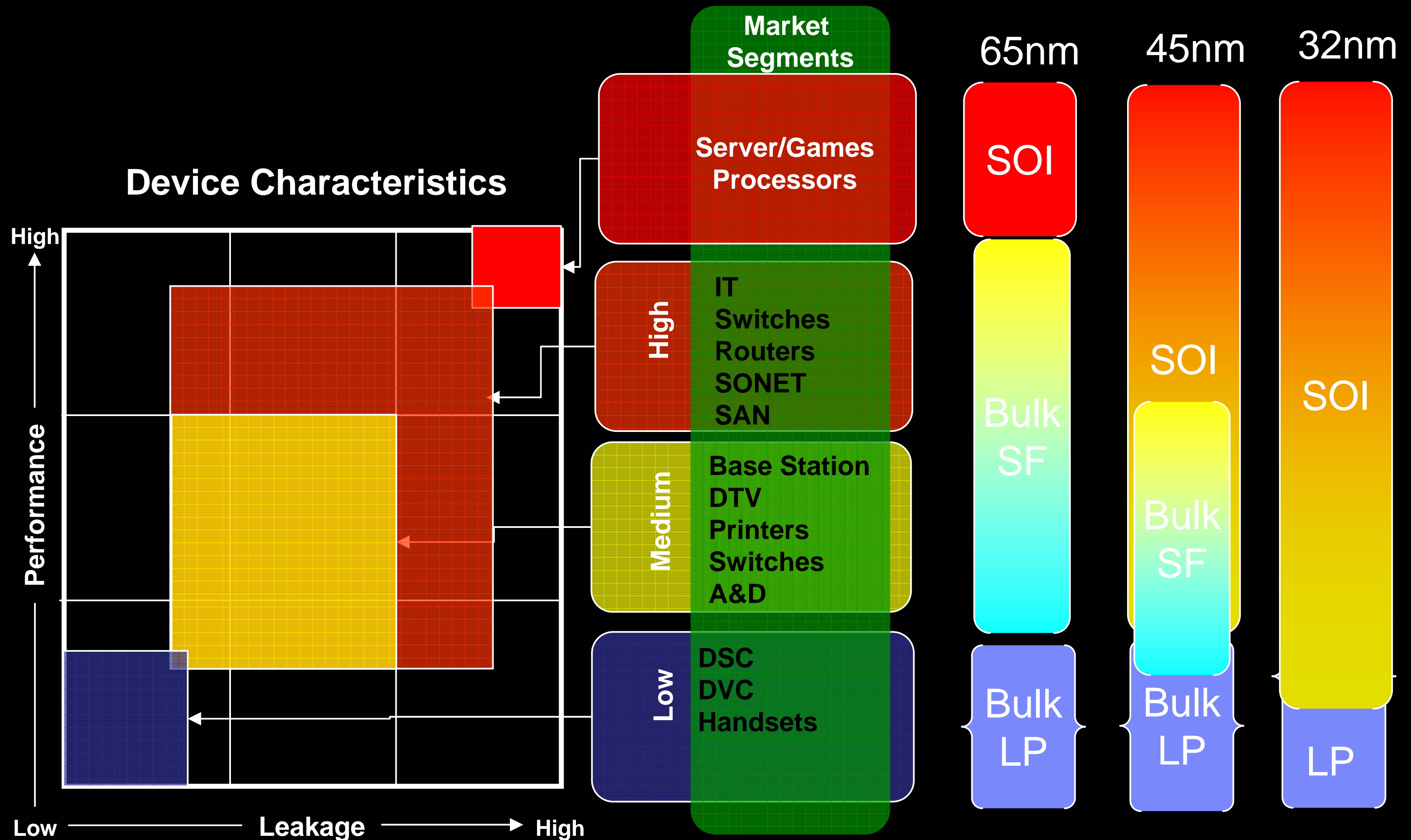
What are these functions ?



Customers need the flexibility to mix high performance and low leakage devices on the same die to optimize power and performance

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Where Are We Going with Scaling?

- Historically constant field scaling came to a grinding halt at 90nm
- Stress engineering saved the day
- At 32nm HiK is a game changer
- It is designed to allow us to mix higher performance and low leakage on the same die at reasonable cost
- At 22nm further innovations are called for

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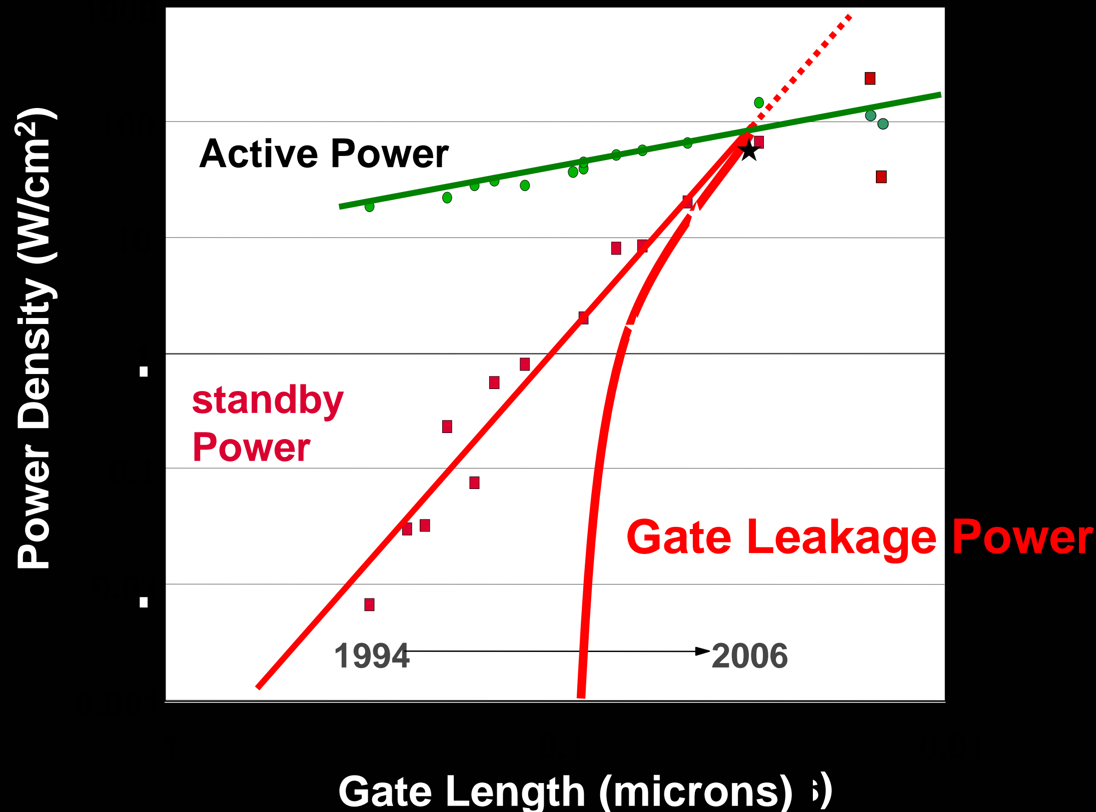
Power Density Keeps Growing !



- Non-scaling causing power density to increase
- **Gate leakage power growing exponentially !!**

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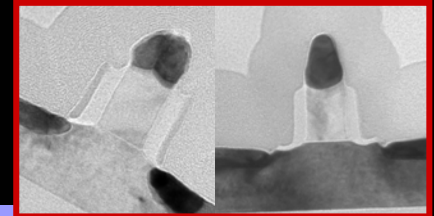
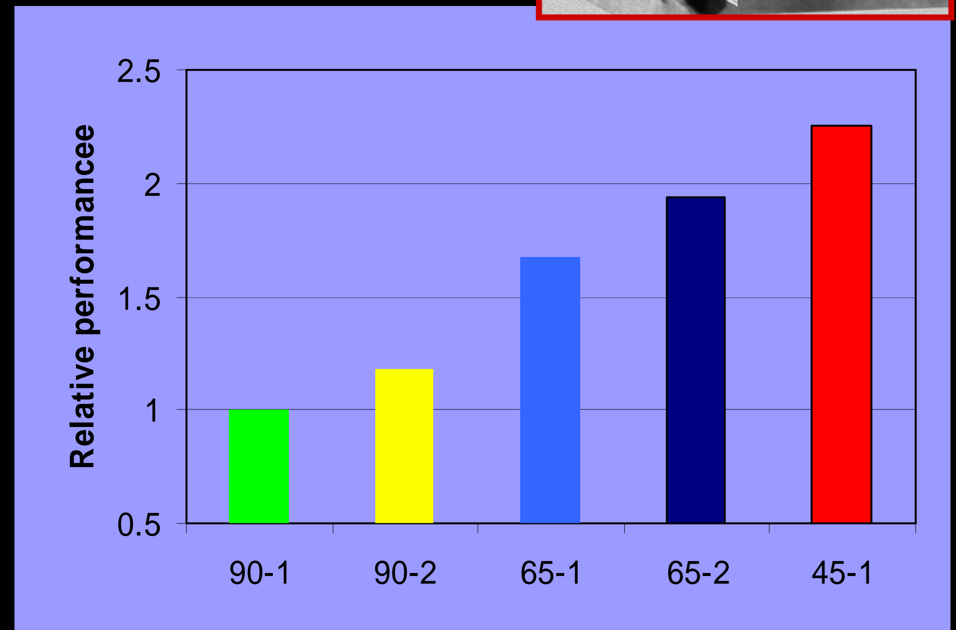
Strained Silicon: Achieving Relentless Performance Improvement



- **Dual Stress Liner (DSL)**
- **Stress Memorization Technique (SMT)**
- **Embedded SiGe (eSiGe)**
- **Stress Proximity Technique (SPT)**



Basic Strain	DSL	DSL SMT	DSL SMT eSiGe	DSL SMT eSiGe SPT

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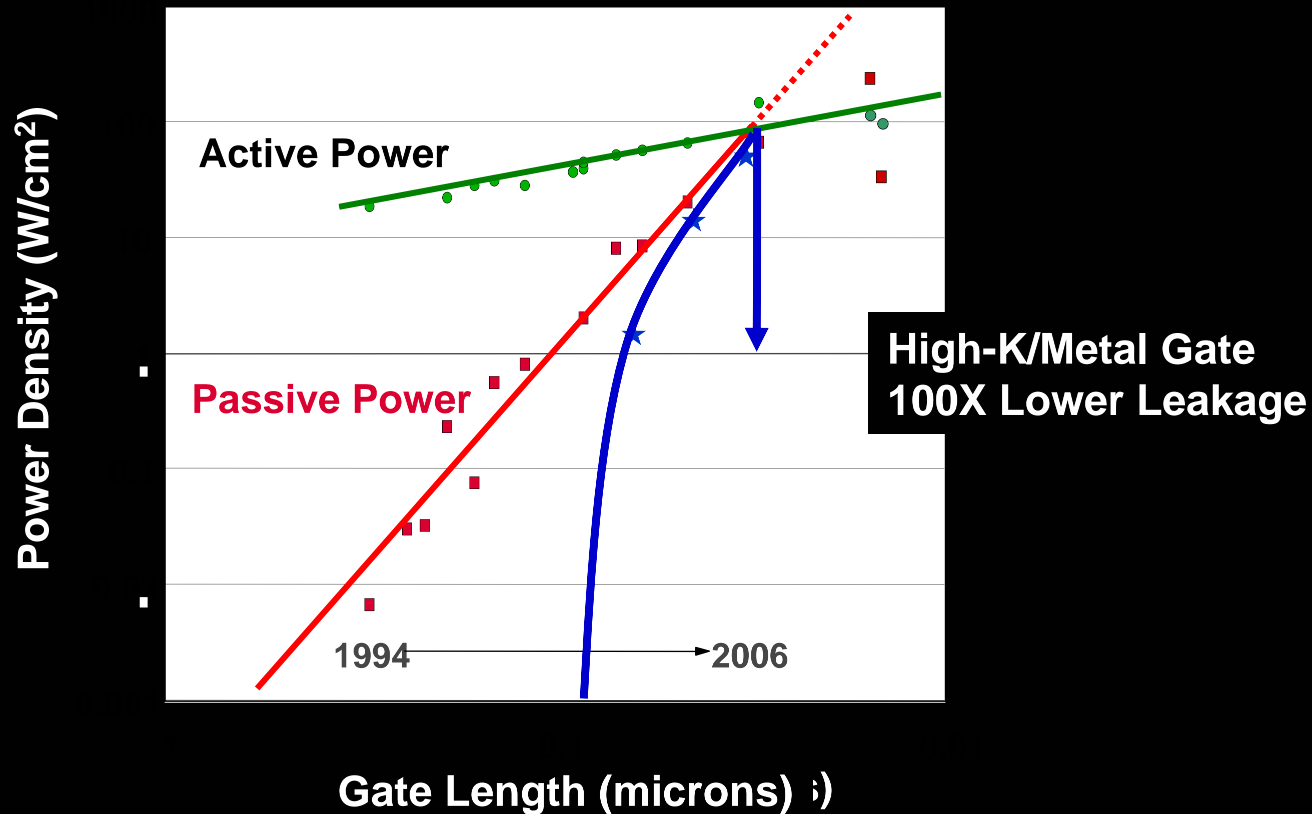
High-K/Metal Gate Enables Power Reduction



- High-K/Metal Gate reduces gate leakage power by 100X

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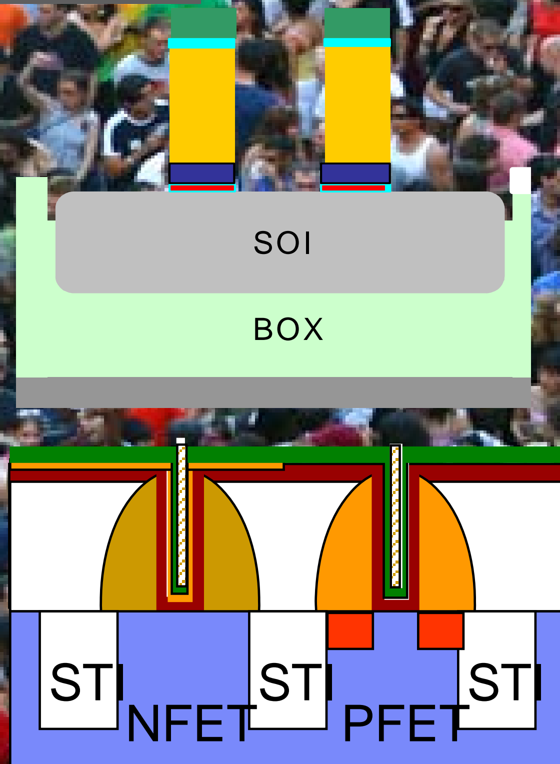
Where are Hi K materials when you need them ?

- **Material Issues**
  - Compatible gate materials
    - Band edge vs Near Bandedge
  - Performance vs Power Tradeoffs
  - Temperature Stability
  - Integration Schemes
  - Scaling channel length



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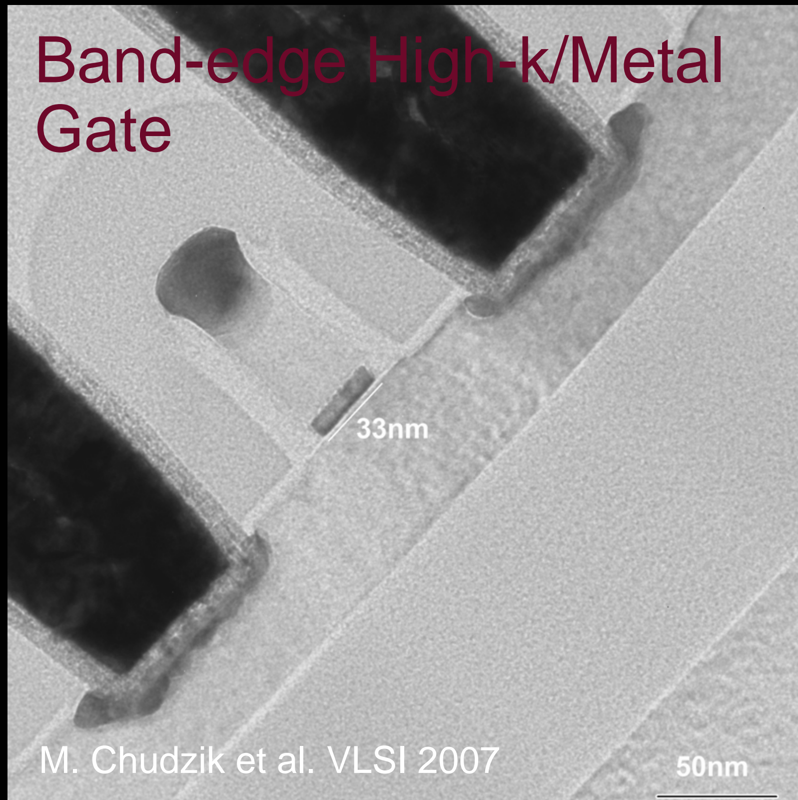
Scaling to 32 nm and beyond



- **TEM cross-sectional images of band-edge NFET HKMG stacks after full build showing a physical gate length of <40nm**

- Hi K allows us to return to scaling as we knew it
- Lower leakage devices will be possible by adjusting threshold
- But there are better ways of adjusting threshold
- So we will be able to offer both high performance as well as low leakage devices with a single gate dielectric without suffering from gate leakage limitations

But you must be able to scale the channel length !!

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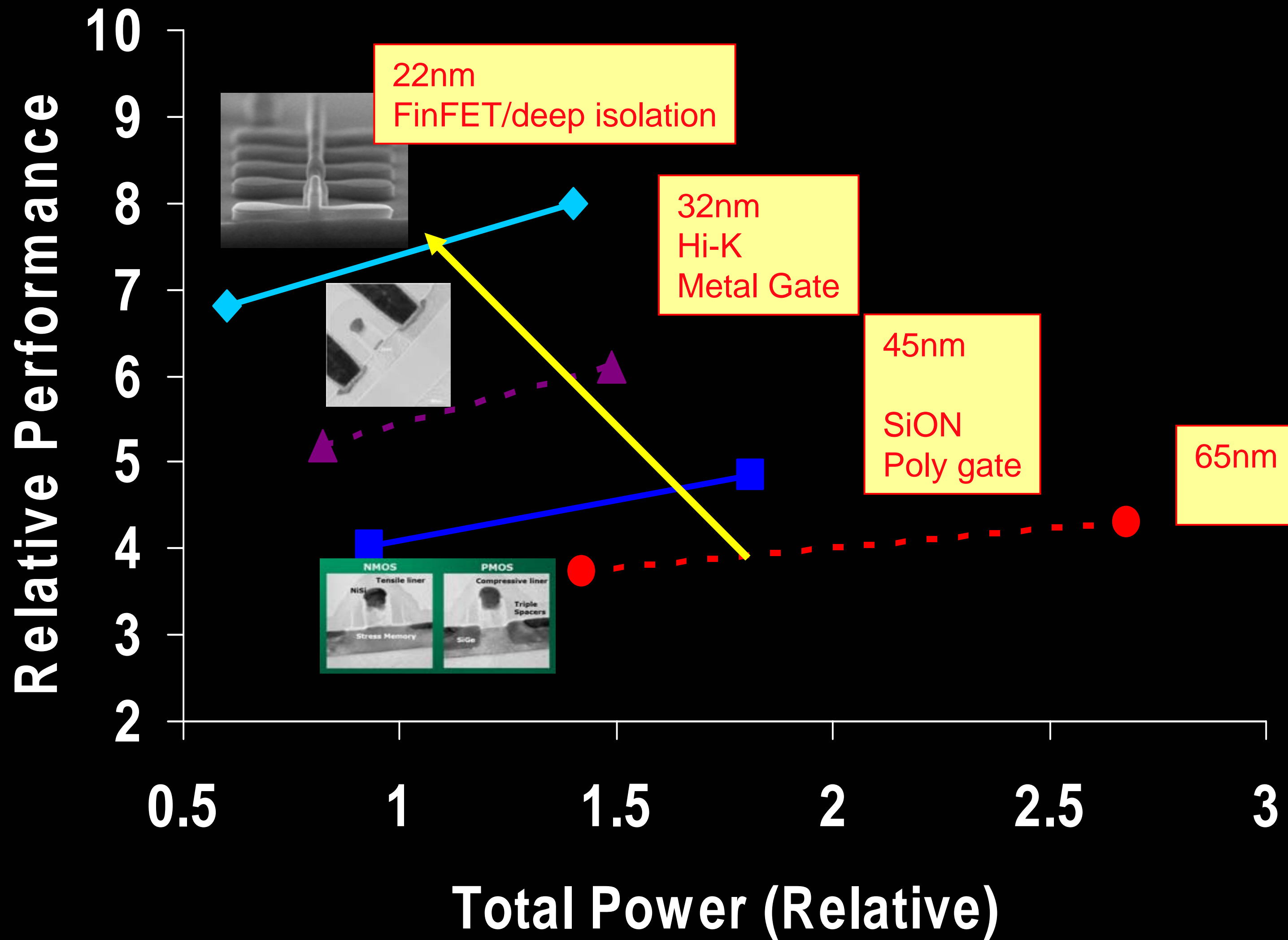

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Key Issues Facing our Industry

- Scaling for performance is getting more difficult and very expensive
- Chip Power – both standby and active are getting to be un-manageable
- Manufacturing cost is becoming huge while more and more parts are being commoditized
- Technology development is getting very expensive

Net: Value needs to come from system concepts applied to ICs

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So how did you like the ride ?

455 HP! This car moves!!!

But the gas tank is too small !! And my Kids don't fit in the back seat !!

Performance Auto

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Going beyond Scaling and New Materials

- Scaling, strain engineering, and improved materials will continue to improve performance , though at diminishing rates and certainly with diminishing returns
- A combination of voltage supply reduction, power budget constraints and design IP migration suggest that the days of dramatic raw performance gains are over
- Performance must come from elsewhere

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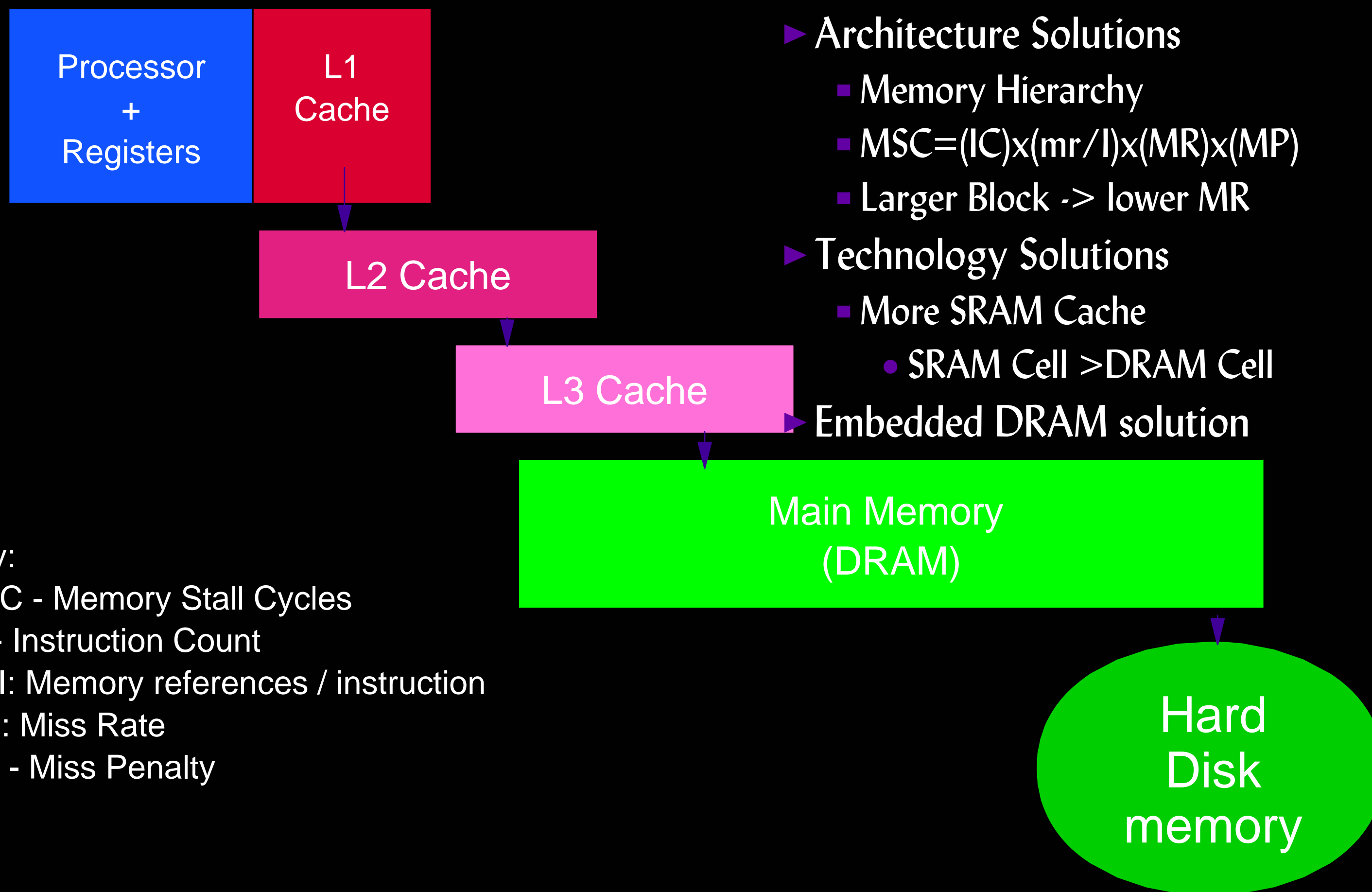
Memory Hierarchy in a Modern Processor



- Architecture Solutions
  - Memory Hierarchy
  - MSC=(IC)x(mr/I)x(MR)x(MP)
  - Larger Block -> lower MR
- Technology Solutions
  - More SRAM Cache
    - SRAM Cell >DRAM Cell
- Embedded DRAM solution

Key:
MSC - Memory Stall Cycles
IC - Instruction Count
mr/I: Memory references / instruction
MR: Miss Rate
MP - Miss Penalty

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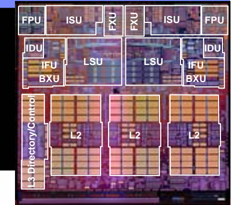
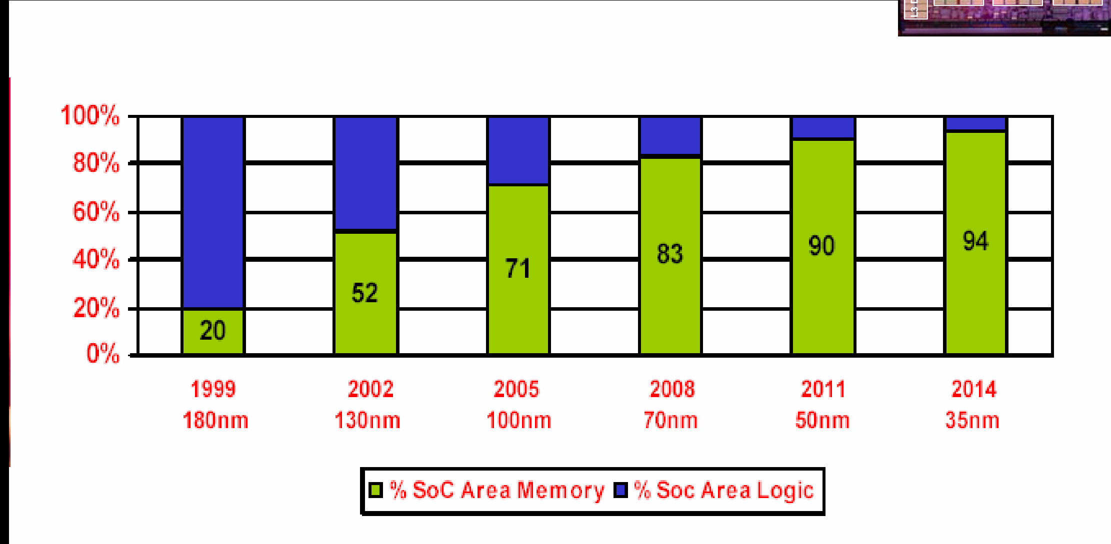
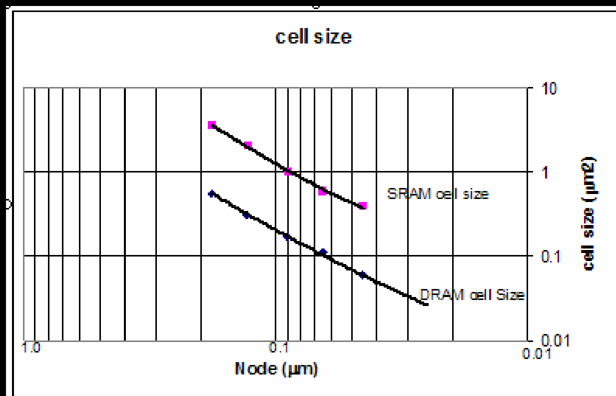


At the system level, you never have enough memory!

How do you integrate large amounts of dense memory on chip ?

DRAM cells are 6X smaller than SRAM cells
about 3.5X as dense / Mb
And about half as fast





Integrate DRAMs on a logic chip additionally they

- Save power
- Have 10^4 lower SER
- and are more stable

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SIA ITRS

The SRAM conundrum

- SRAMs are not aging with dignity
- Vmin stability due to
  - Dopant fluctuation
  - Gate oxide leakage
- Solutions
  - Slow down scaling of both area and voltage
  - Multiple cells with unique devices and layouts
- Power
- Soft Error Rate continues to rise

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Integrating DRAM and Logic

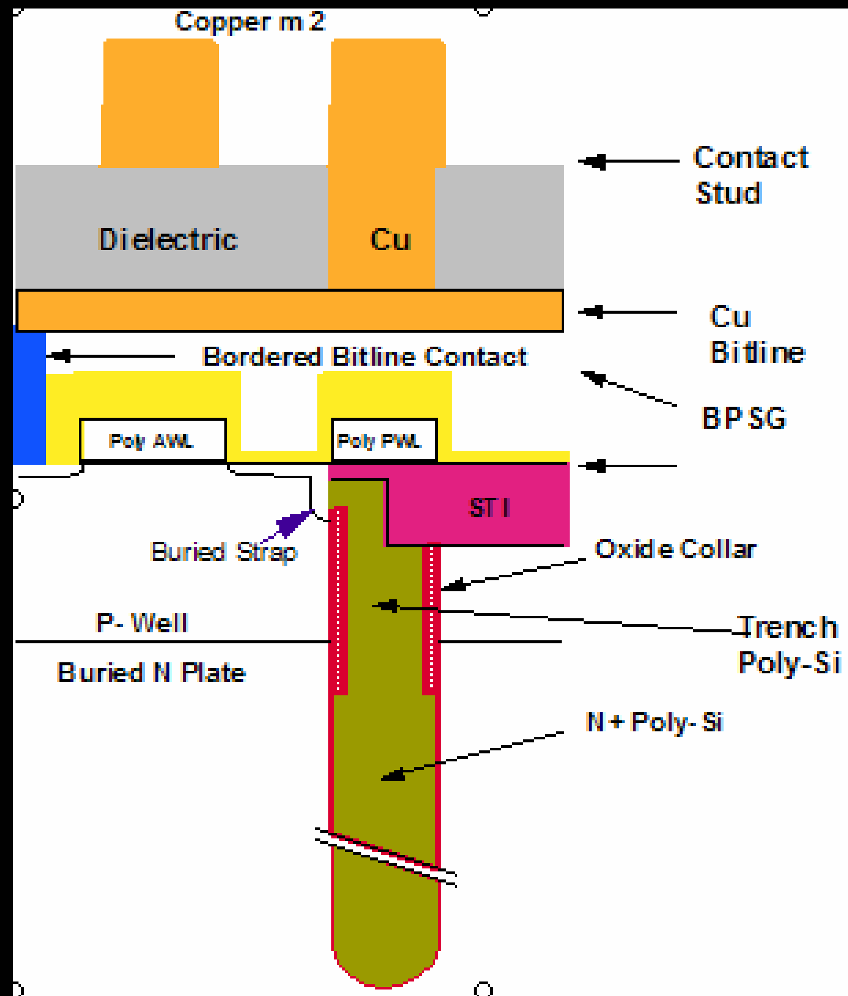
- **Integrate with Logic without impacting logic Performance, Reliability or Yields**

•The Deep Trench process is intrinsically logic friendly

•Capacitor fabricated first

•No perturbation of the remaining logic flow

- Significant Process & Test know-how in DRAMs using deep trench technology



Over five generations, embedded DRAM has adapted to logic technology resulting In simpler processes and significantly higher cell performance

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Blue Gene – world's fastest supercomputer in 0.13μ bulk CMOS

- Two Power PC 440 processors
- Associated local SRAM caches
- Two Floating Point units
- Five network controllers
- memory control system
- 4 MB of on chip Dynamic Memory(L3)

System
(64 cabinets, 64x32x32)

Cabinet
(32 Node boards, 8x8x16)

Node Board
(32 chips, 4x4x2)
16 Compute Cards

Compute Card
(2 chips, 2x1x1)

Chip
(2 processors)

180/360 TF/s
16 TB DDR

2.9/5.7 TF/s
256 GB DDR

90/180 GF/s
8 GB DDR

5.6/11.2 GF/s
0.5 GB DDR

2.8/5.6 GF/s
4 MB

Tree
FPU1
PU0
L2
PU1
Torus
FPU0
Eth
JTAG
Perf
L3

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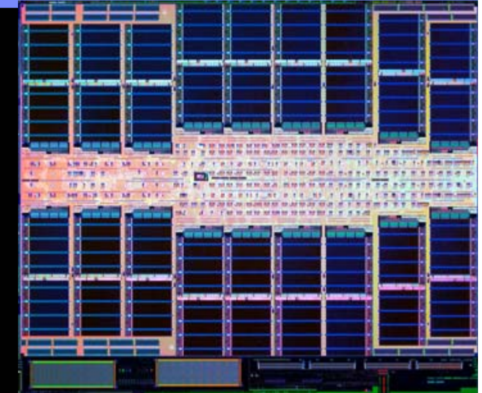
Power 5 – L3 cache

- 430 Million Transistors... Largest ASIC Chip Ever Produced
- 344Mb of L3 Memory per Die
- 4x to 6x larger than SRAMs used by competitors
- Enables a 50% improvement in System Performance



"We consider IBM's reworking of the Level 3 cache design to be one of the top design wins in Power5."

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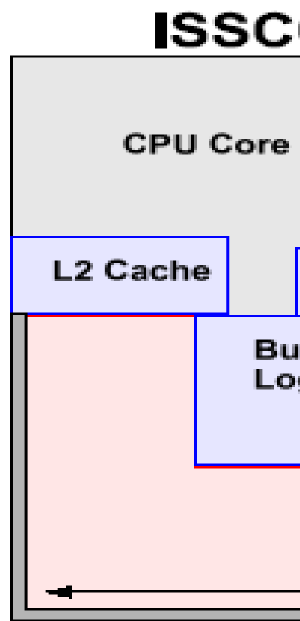
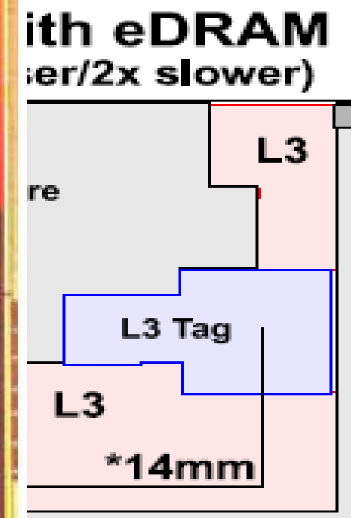
Case Study: *hypothetical* processor chip w/ eDRAM

SRAM

ISSC



ith eDRAM
er/2x slower)



barray

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Scaling: Introduction of DRAM is equivalent to scaling (memory) *additional* two generations

DRAM introduction allows for a 0.28X scaling of memory block size at the time of introduction in addition to the assumed 0.7 scaling i.e. total scaling of 0.17

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Scaling: Introduction of DRAM is equivalent to scaling (memory) *additional* two generations

DRAM introduction allows for a 0.28X scaling of memory block size at the time of introduction in addition to the assumed 0.6 scaling i.e. total scaling of 0.17

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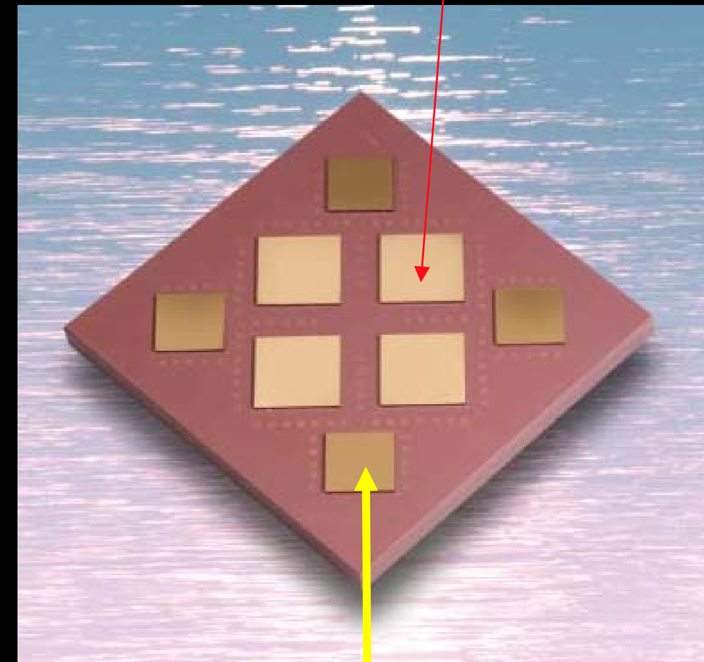
Going forward

Power 4,5, 6 MCM

- The next step is integration with the processor
- What are the challenges ?
  - Scaling and performance
- What is the approach



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Performance eDRAM

- **70% of performance is gated by logic performance**
  - **Address Decoding functions**
  - **Row system Logic**
  - **Sensing circuits**
- **30% of performance dictated by cell (writeback)**
- **Subarray architecture plays an overall role in optimizing performance-area-power tradeoff**
- **Logic based technologies comeout ahead on all fronts**

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Technology Innovation – Development of SOI DRAM cell

- **Technology:**

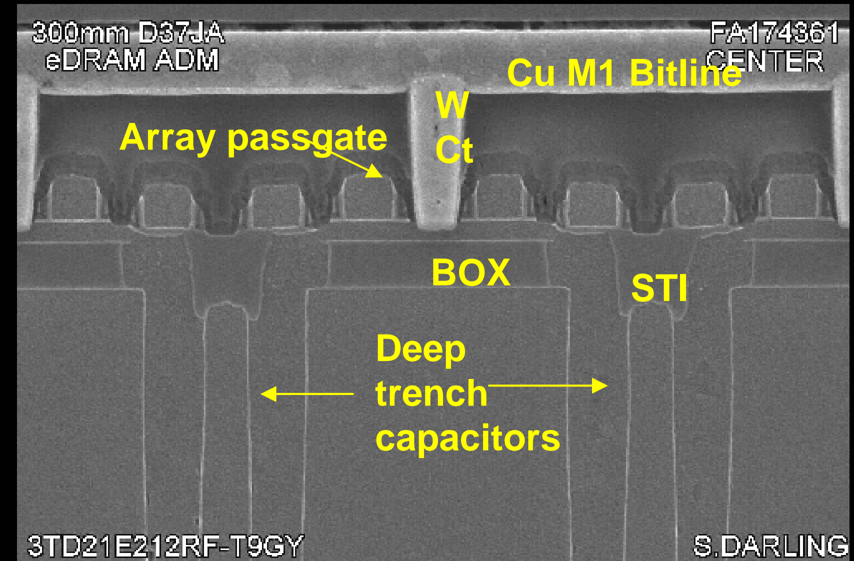
  Use the Buried oxide to simplify the process & reduce parasitics – half the cost of bulk eDRAM

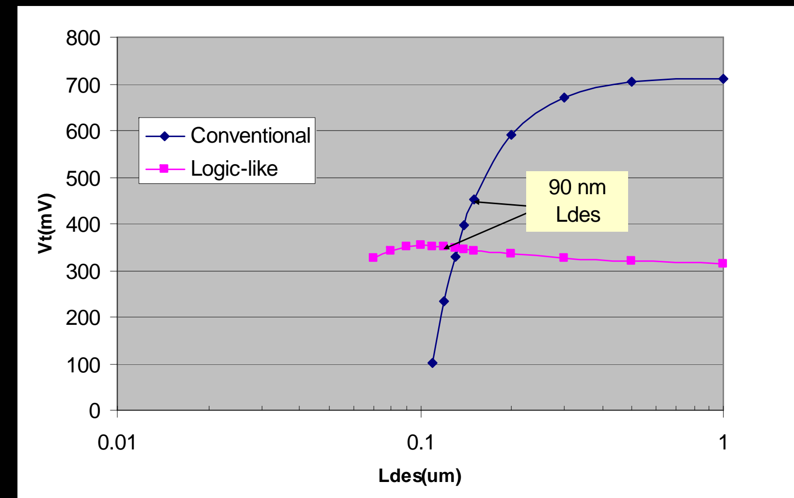
  Scale the pass transistor for higher performance

- **Design**

  Address retention through concurrent refresh

  Ultra short bitlines with direct sense architecture





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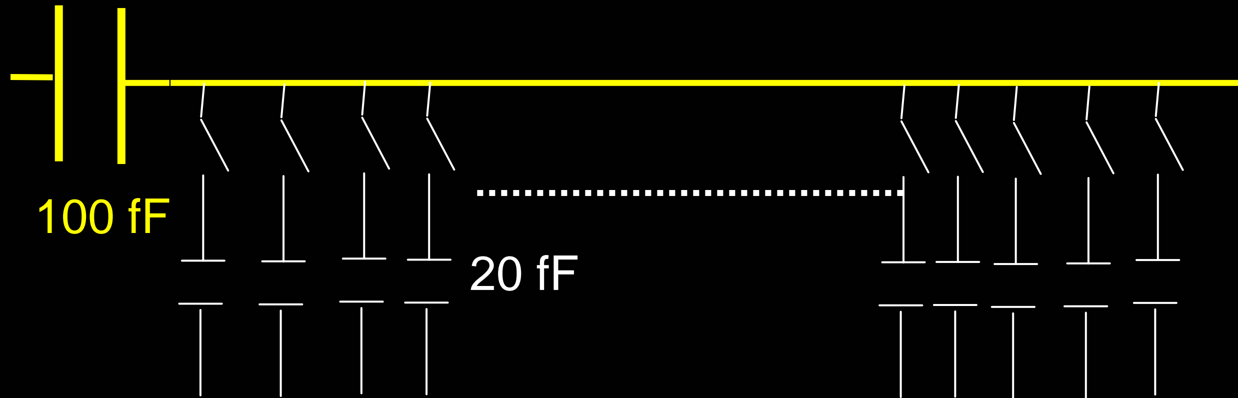
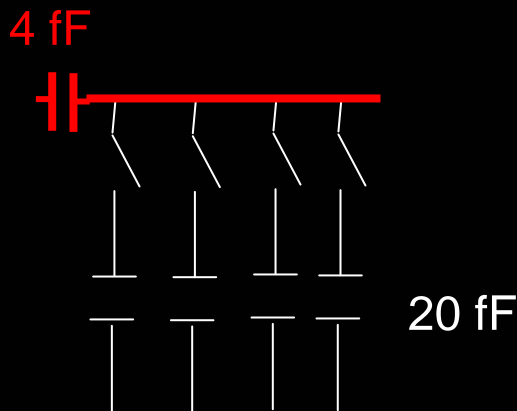
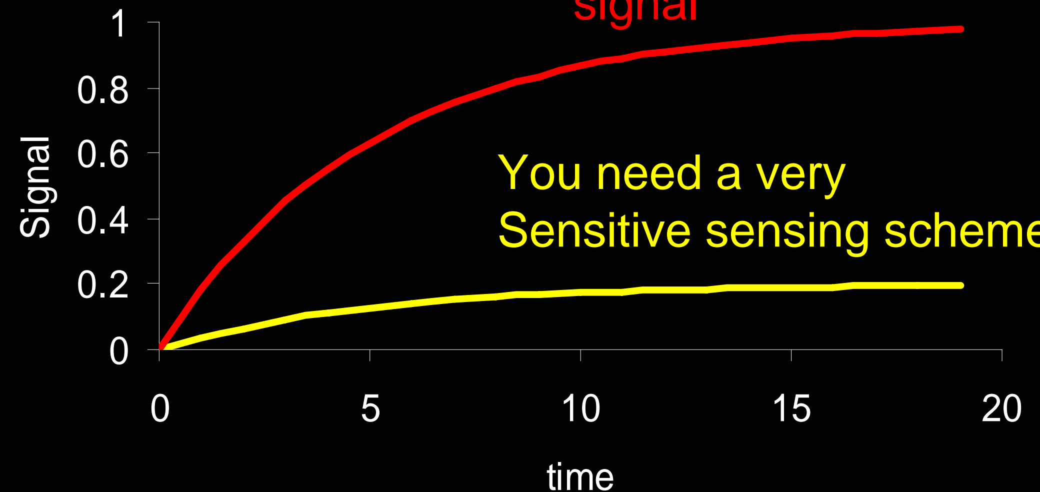
Ultrashort bitlines & μSense Advantage



Conventional – small signal, long time

μSense – large signal short time





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Collar Process Elimination

Bulk

M1 Bitline
CA
WL
N P N
P-WELL
N-Band
DT
Vertical Parasitic Device
Thick Oxide Collar to shutoff parasitic

SOI

M1 Bitline
CA
WL
N P N
Buried Oxide (BOX)
N-Band
DT
No Vertical Parasitic Device
No Collar Required

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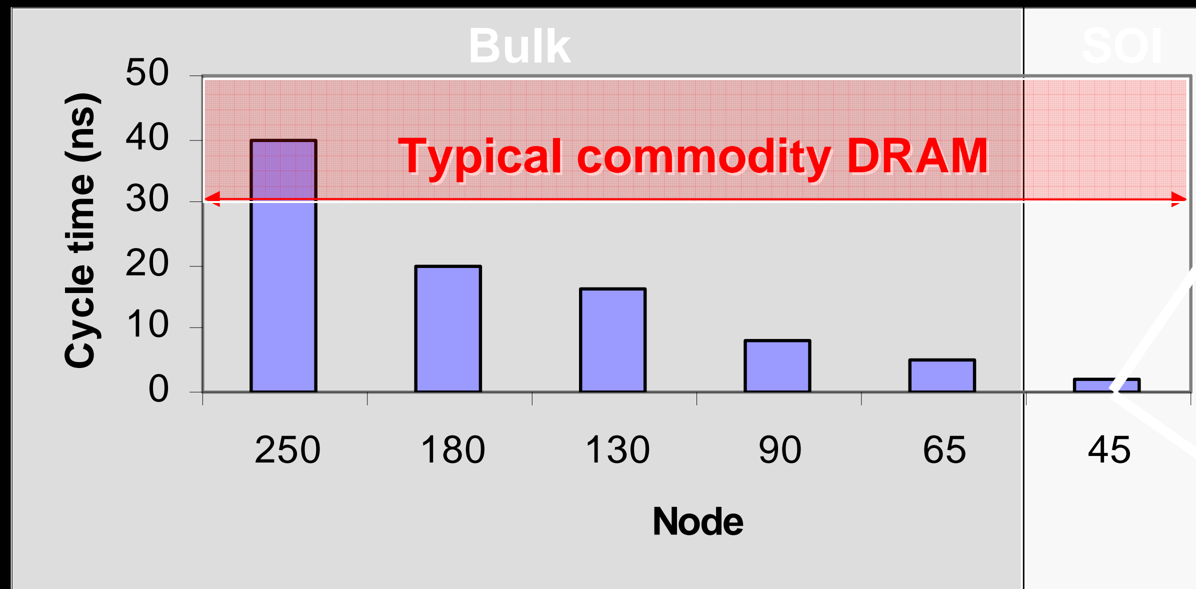
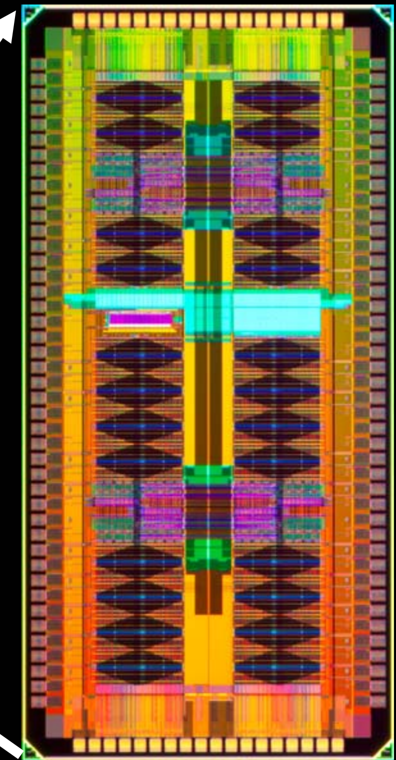
SOI eDRAM





Advantages:

- **SRAM like performance @ DRAM density, power and Soft Error Rate**
- **Full Logic compatibility**
- **~3.5X reduction in memory area (3 additional mask levels)**

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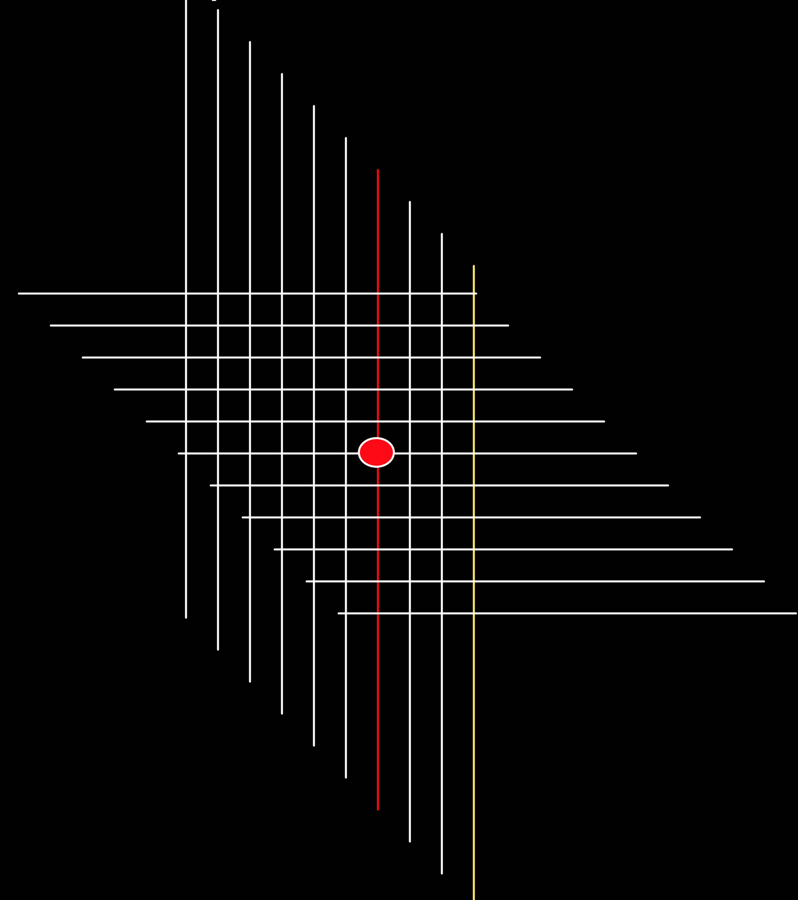
L3 caches in servers

Yielding Large Memory Chips Requires redundancy

L3 cache used in P5
344 Mb, 430M transistors
Largest ASIC made at IBM

Note: a chip this size can have as many as 32K fuses



Redundancy invoked using fuses

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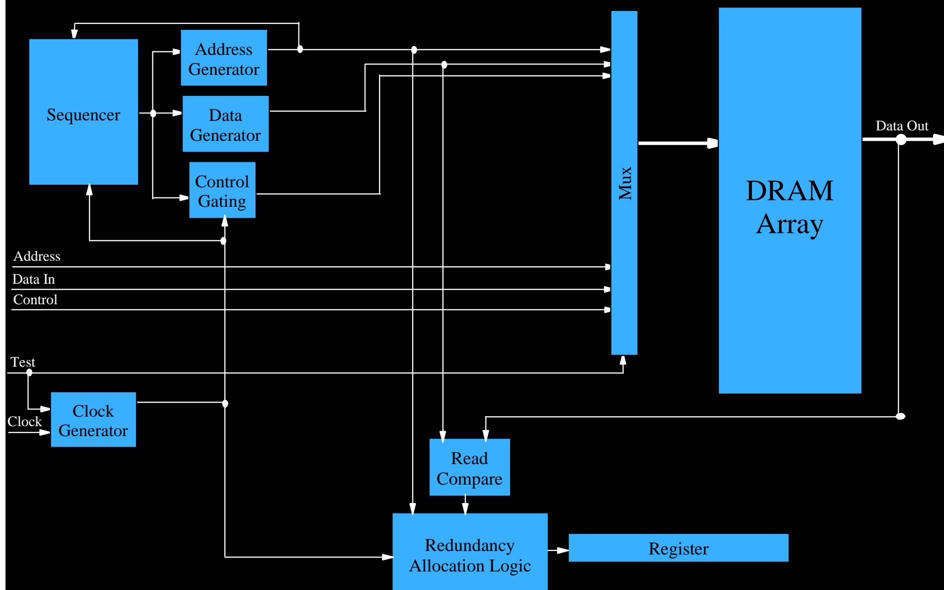
Built-in Self Test and repair

Key Enablers: BIST & Redundancy

- Test at High speed
- Very large bandwidth but very few pin-outs
- Solution : Since you have access to a high speed logic technology why not build the tester on-chip
- Next step : repair faulty chips!



- On chip test engine
- Hard & Soft Patterns
- Allocates Redundancy
- Tests redundant elements
- Generates Fuse String

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Laser Fuses

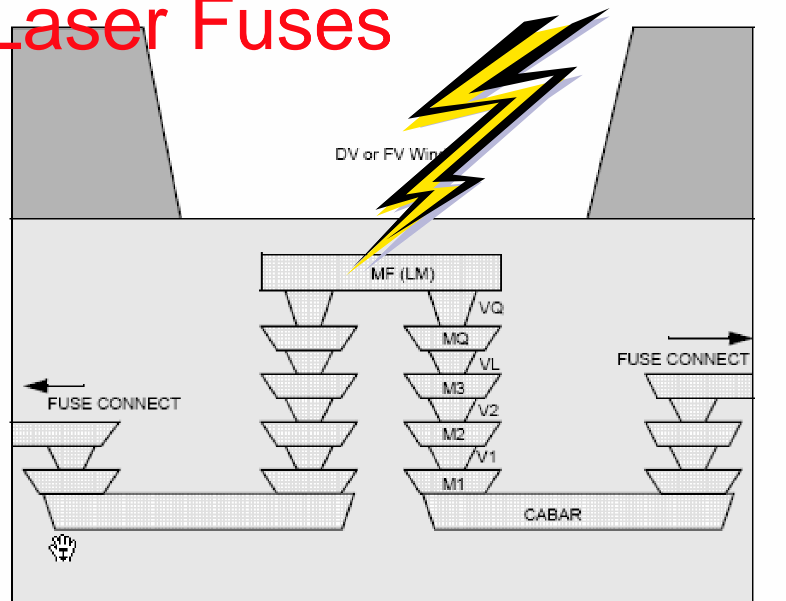

Figure 27: Fuse Cross-Section example - LM

- Test
- Determine repairs
- Move wafer to laser fuser
- Move repair data to laser fuse
- Blow laser fuses
- Take wafer back to tester
- Test again to verify
- Hope nothing break again ever!

- Do not scale & occupy too much space
- Block wiring and C4s
- Need to be exposed
- Can be blown only at wafer leve
- Need precise mechanical alignment
- Require a complex laser fuser
- Require multiple wafer handling and data manipulation

Net: Laser Fuses are a pain!!

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So, For ages DRAM yogis have pondered important questions:

What is the origin of the Universe ?

Why are we doing DRAMs ?

How do you eliminate laser fuses ?

An electronic fuse would answer these questions

You could use circuits on the chip to program them!

Maybe you could even make the chip autonomic !!

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What are *Autonomic Chips* ?

- Chips that can identify, test and repair themselves
  - In the Fab at wafer level, In the package, In the field multiple times
- Repairs are self-consistent and contained on chip without need to access the rest of the system
  - They need to be hard-coded on the die
- Chips that can maximize their yield within a predefined parametric space
- Chips that ensure only authorized access
- Chips that identify hazardous operating conditions
  - Temperature, excessive device drifts ……
- Chips that can track their history

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Achieving autonomic chips

- Need on-chip monitor to be aware of things going wrong

  Built-in-Self Test (BIST) engine (processor or dedicated)
- A self-repair methodology
  - **At the algorithmic level**

    Aware of previous repairs

    Aware of available repair opportunities

    Decides on irreparability and functional disablement
  - **A method to execute the same permanently on chip**

    A non-volatile memory element that is easy to implement (e.g.. Fuse)

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But seriously

Do you want this on your chip ?

Fine Print: Explosion here has been somewhat exaggerated

Poly Si Fuse Programmed by rupture

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The eFUSE Philosophy

Technology Independent

Fuse must work even if die is marginal

Programming time should be short

Should be programmable on chip

Use design levels and Booleans to create Fuse link

Understand the physics of the blow mechanism

Design innovative circuits to program and sense the fuses

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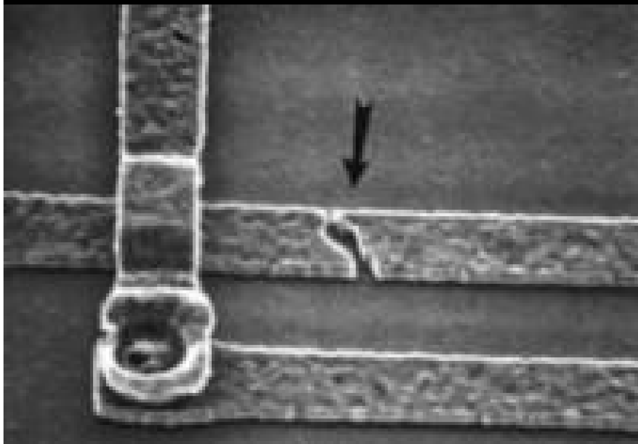
The Kinder Gentler Fuse

We need to induce an electrical open without needing material to disappear.



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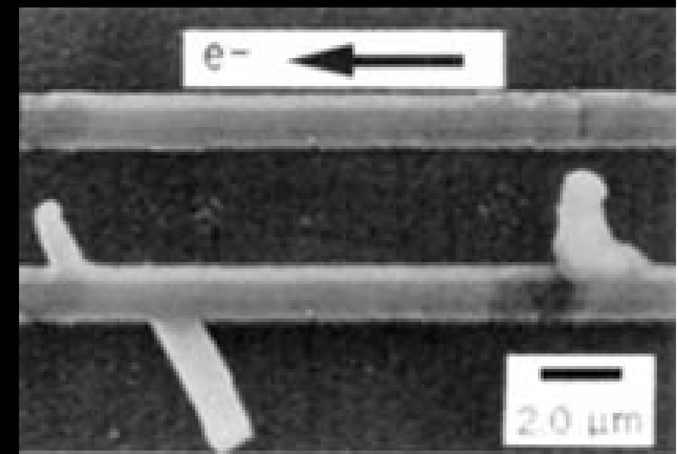

Can we employ electromigration of metal lines ?

Modern interconnects are electromigration resistant

Need to control the electromigration and complete in a reasonable time e.g. 200 μs – Cu line not an option

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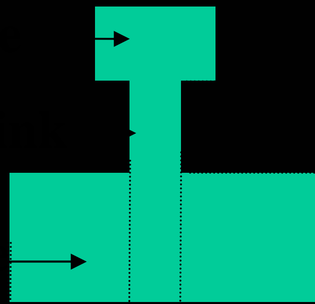
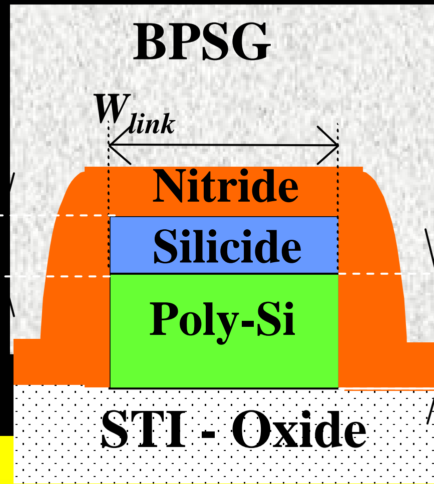
eFUSE - physical layout





$W_{cathode}$

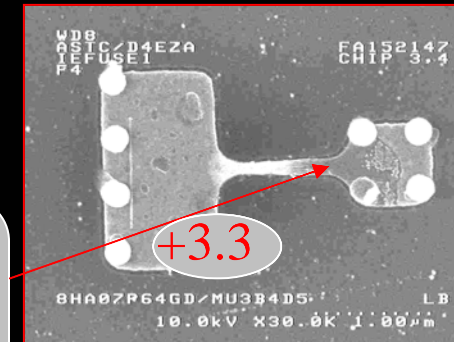
Key Features

- Geometry
- Thermal environment
- Current Characteristics

Mechanism:

- Current driven through silicide
- Temperature rises & gradient set up
- Silicide electromigrates but current is sustained as the Poly Si is hot intrinsic and conductive
- Electromigration of silicide is forced to completion
- Current turned off, everything cools and link is high resistance

Silicide removal always occurs at cathode



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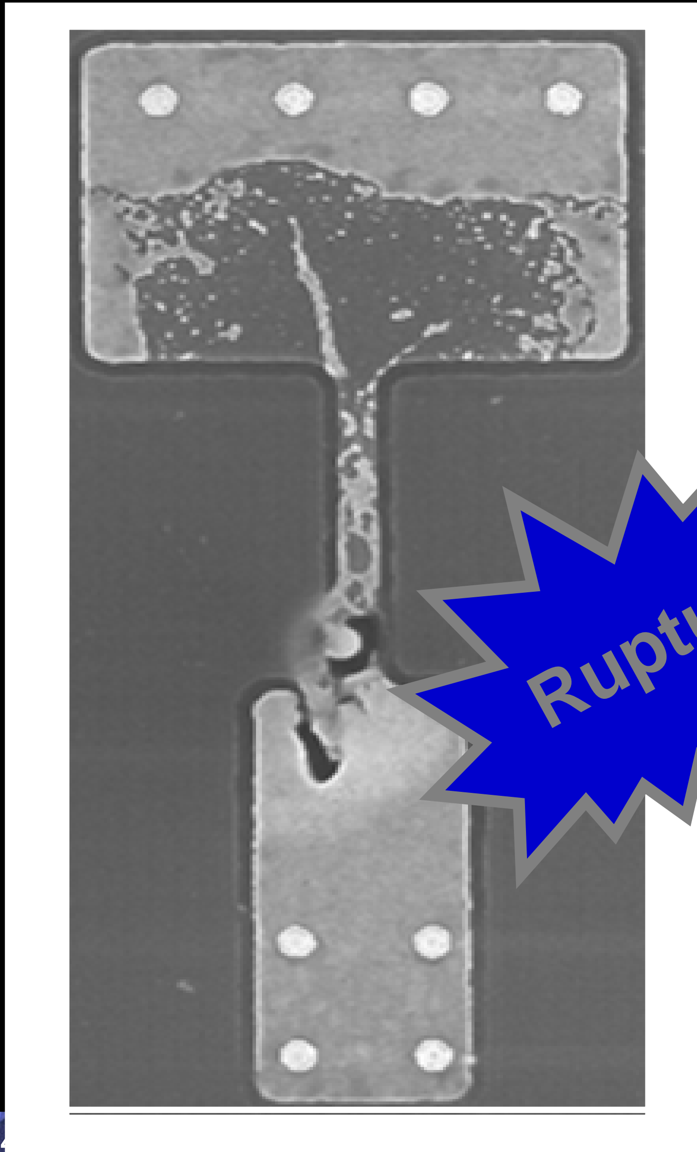
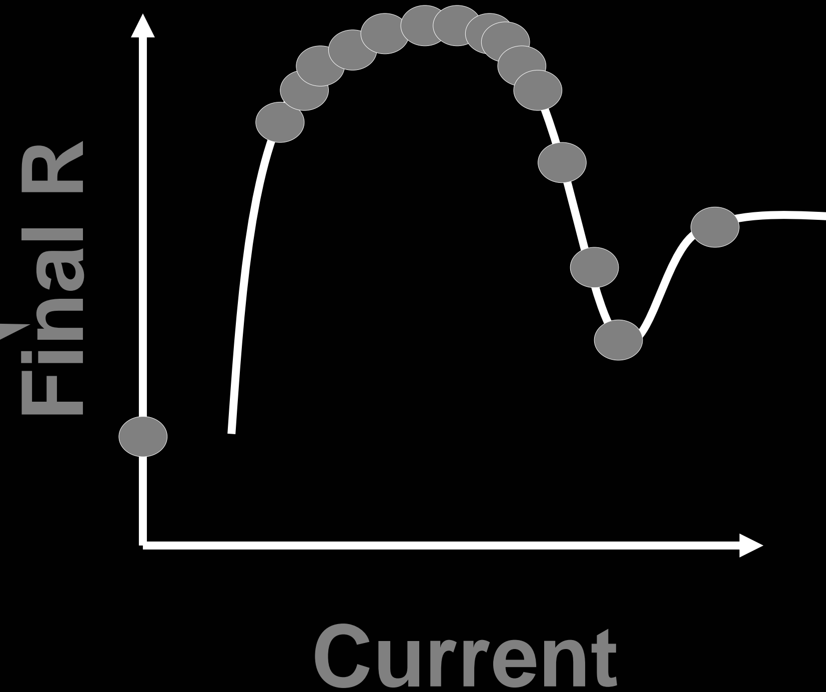
eFUSE Programming



Intact Fuse



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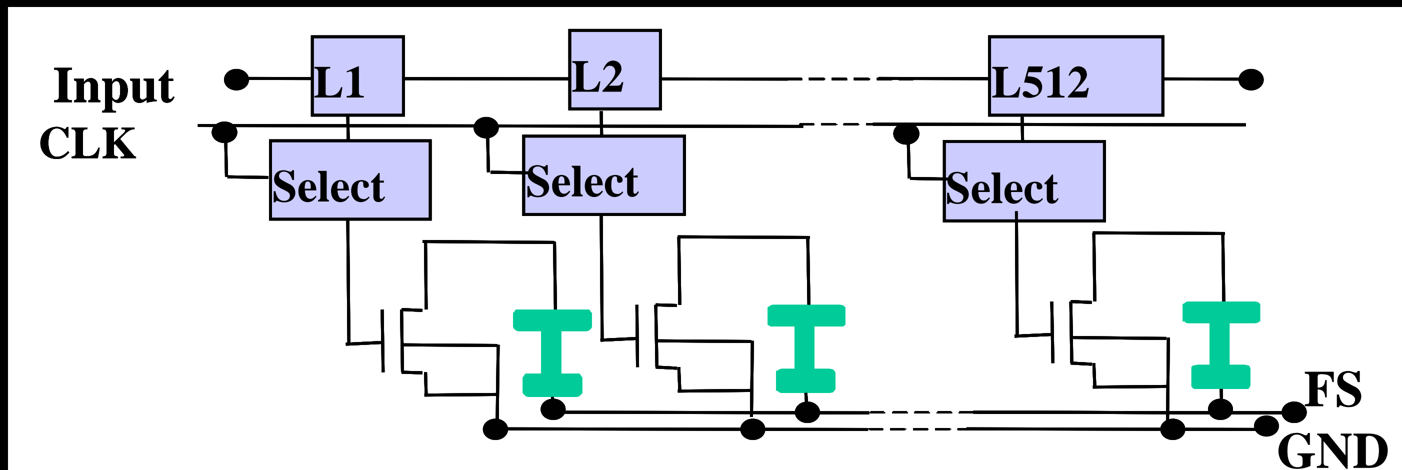
Circuit details



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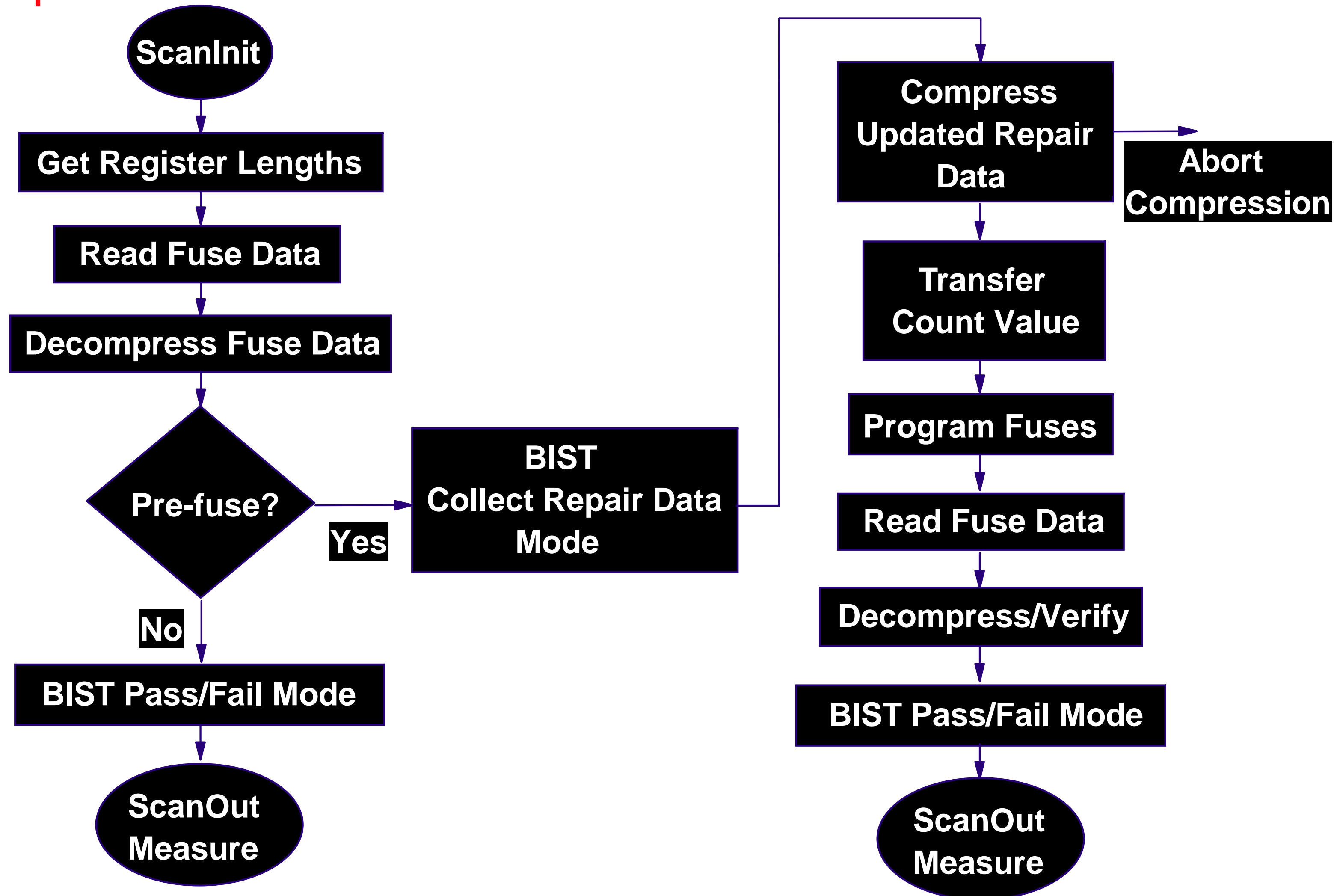
Self-Test and Repair Flow – one touch test, repair & verify as implemented in Cu08



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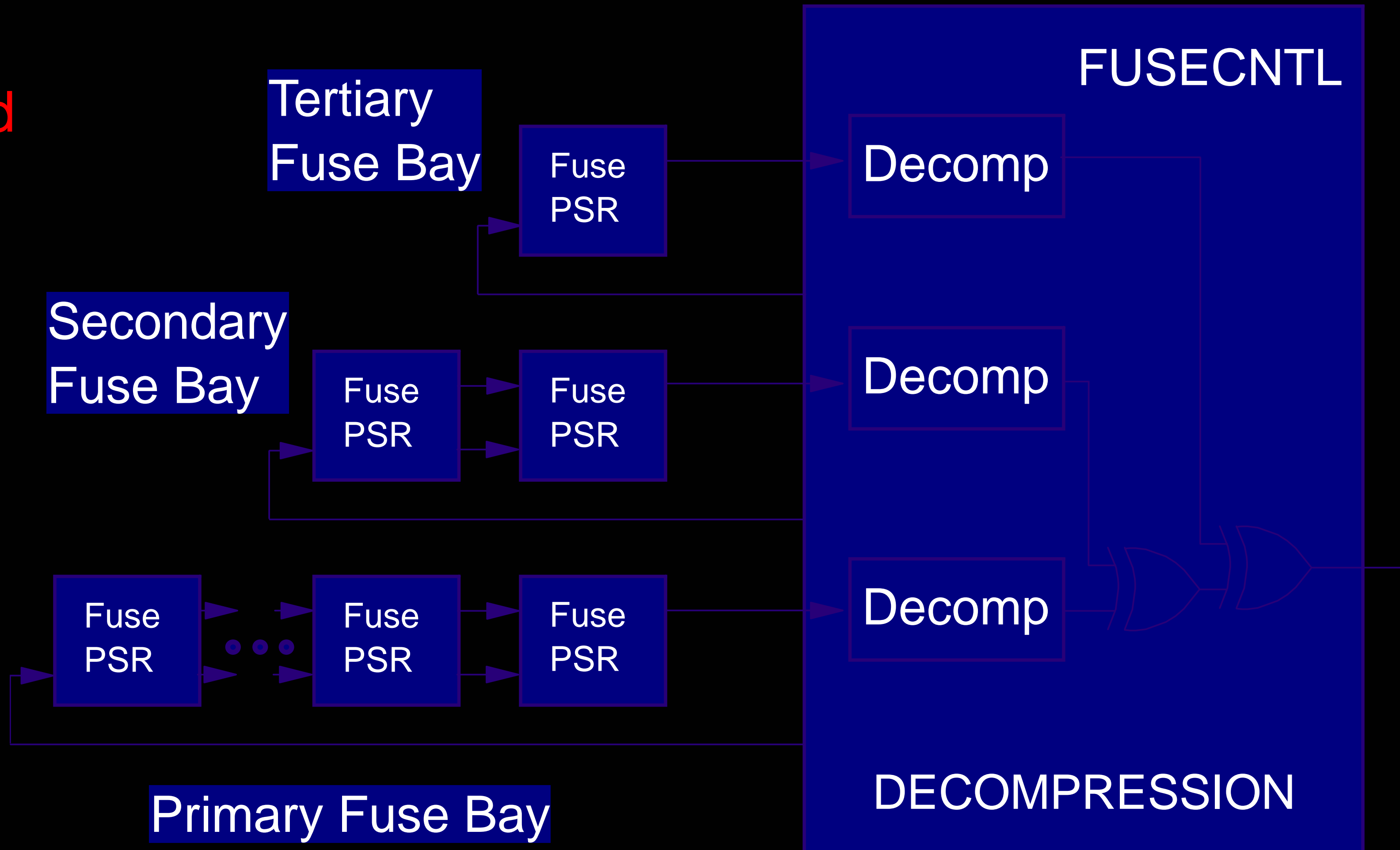
Hierarchical Repair - Combining Three Repair Steps as implemented in Cu08



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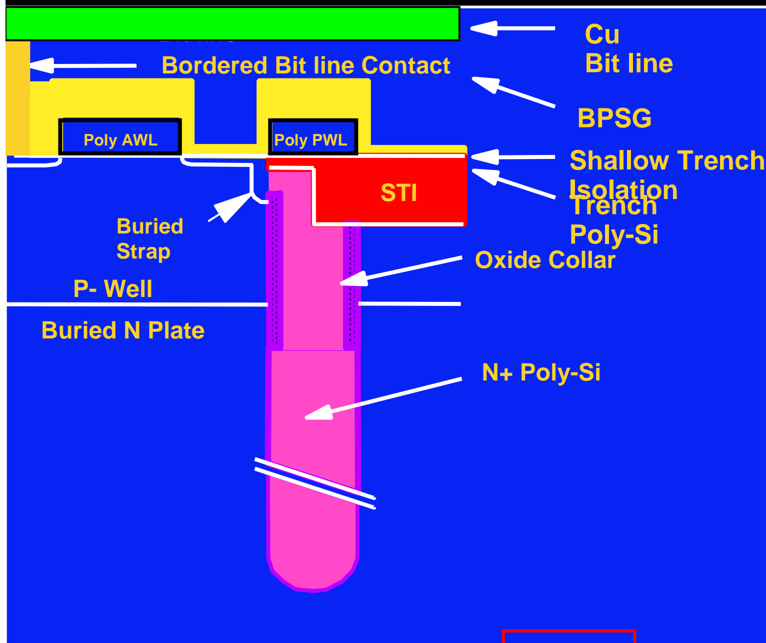
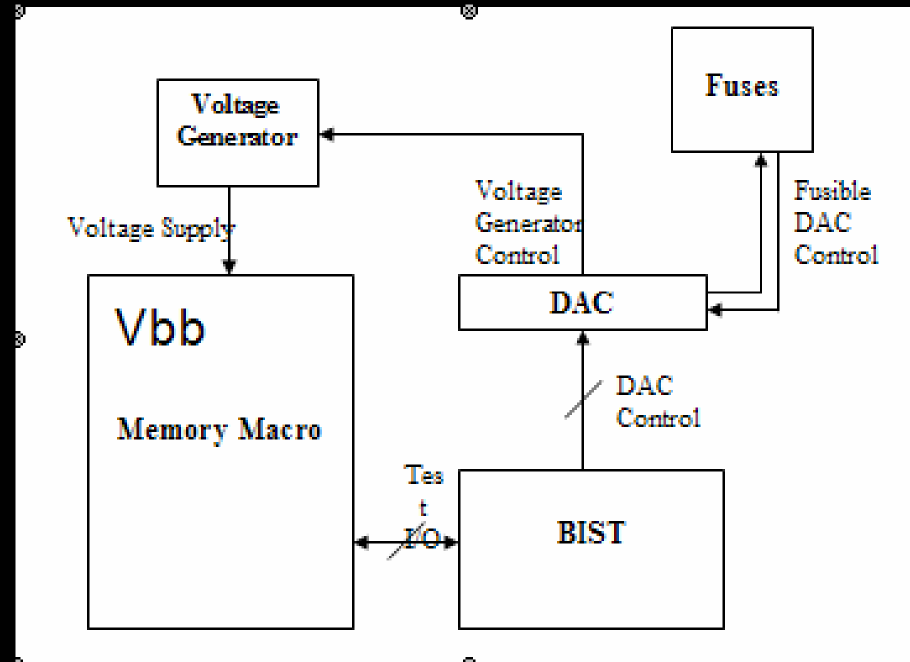
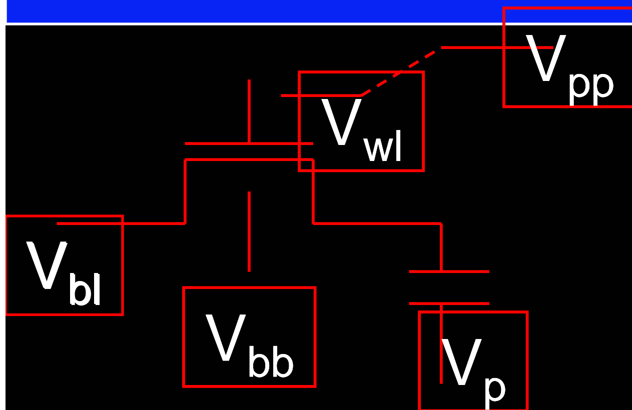
Die specific Yield optimization:
Voltage setting using eFUSE in embedded DRAM







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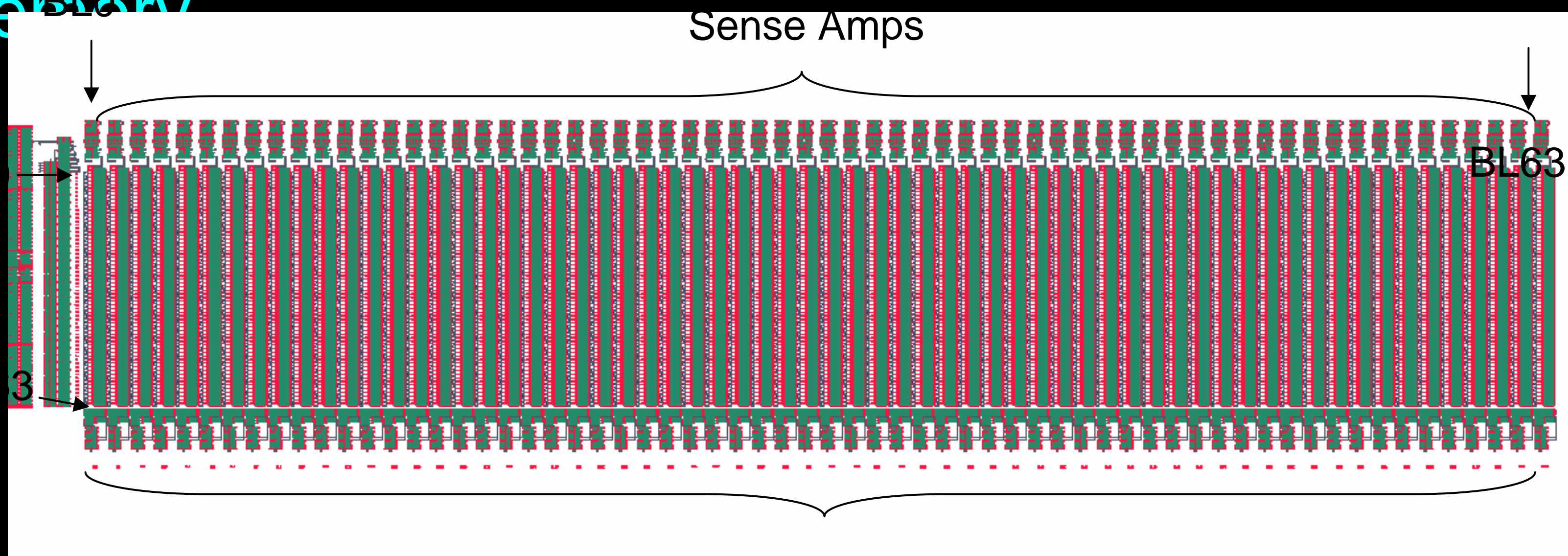
2 Dimensional OTP ROM – for on-chip nonvolatile memory

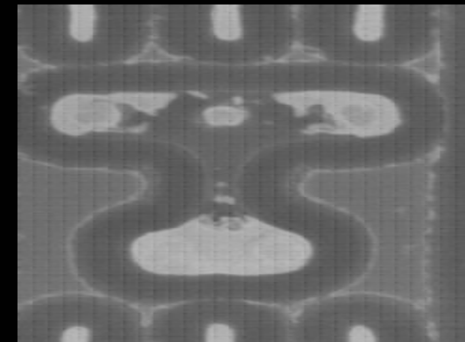


Based on our electromigration Fuse technology – - - - No added process Cost

Memory architecture allows for ~15X improvement in bit density (115 μm^2/bit to 7 μm^2/bit)

Compilable in 2Kb blocks

Centralized repair, code and autonomic functions



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What's next ?

- Optimizing chips for power and performance
- More autonomic functions
- Supply Chain management
- Chip identifiers for authentication
- RFID tags
- Logic compatible 2D OTP ROM

- Exploit other phenomena: Hot carrier, NBTI to self balance mismatched circuits

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Power supply decoupling

- Why is decoupling important ?
  The concept of voltage compression
- Decoupling today is mostly an afterthought but compression is a serious problem
- A judicious of decoupling can allow for upto 10% reduction in Vdd due to reduced compression

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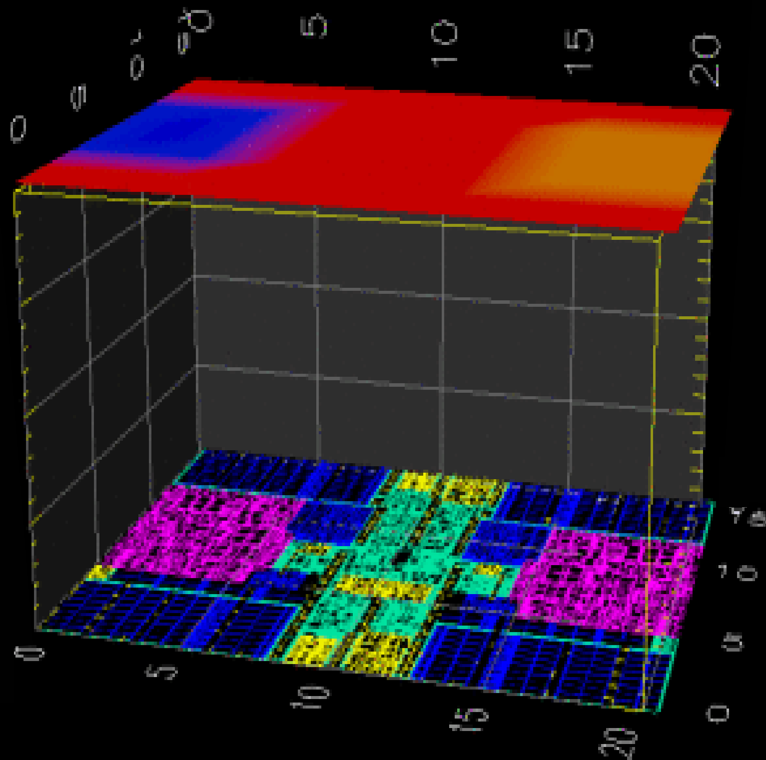
Noise Traveling Across Chip (Connected cores)



- Noise travels from active core to idle core
- ~4ns delay between cores
- Noise is attenuated at quiet core

James et al, ISSCC 2007

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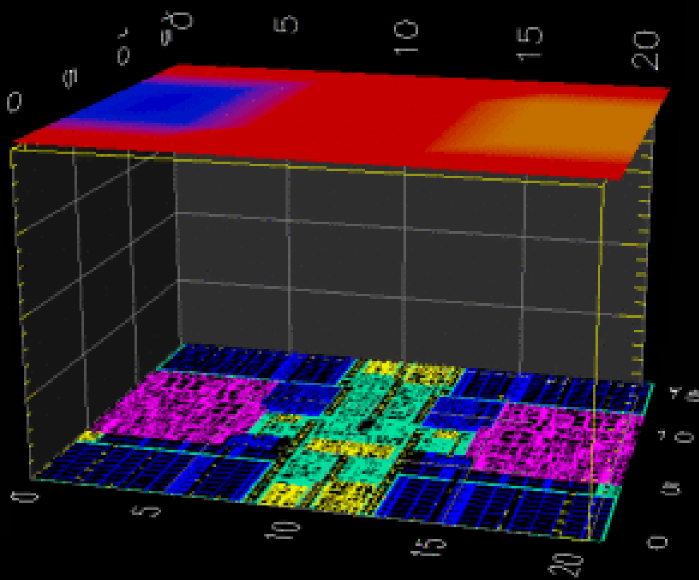
Noise Traveling Across Chip (Connected cores)



- Decoupling today is mostly an afterthought but Transient voltage droops due switching activity is a serious problem
- Planar Caps are large and leak tremendously
- So we cannot isolate this noise and must increase power supply to overcome
- Can be a serious issue in high performance multicore applications

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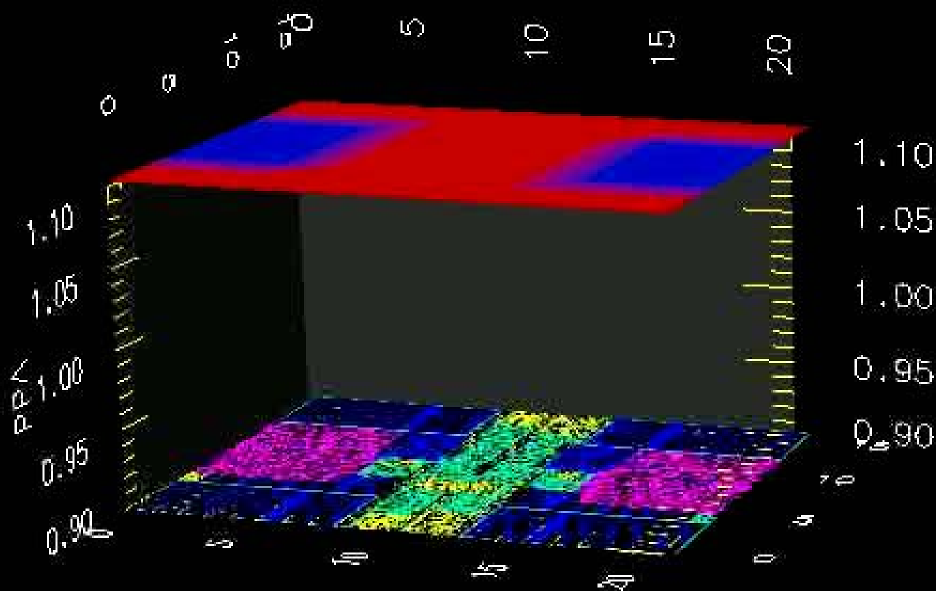
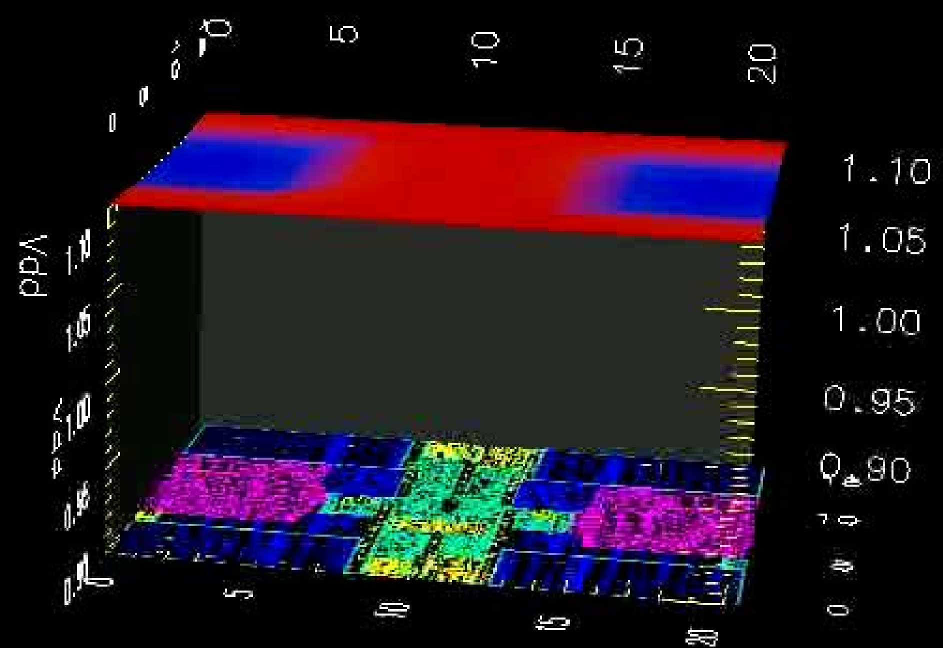
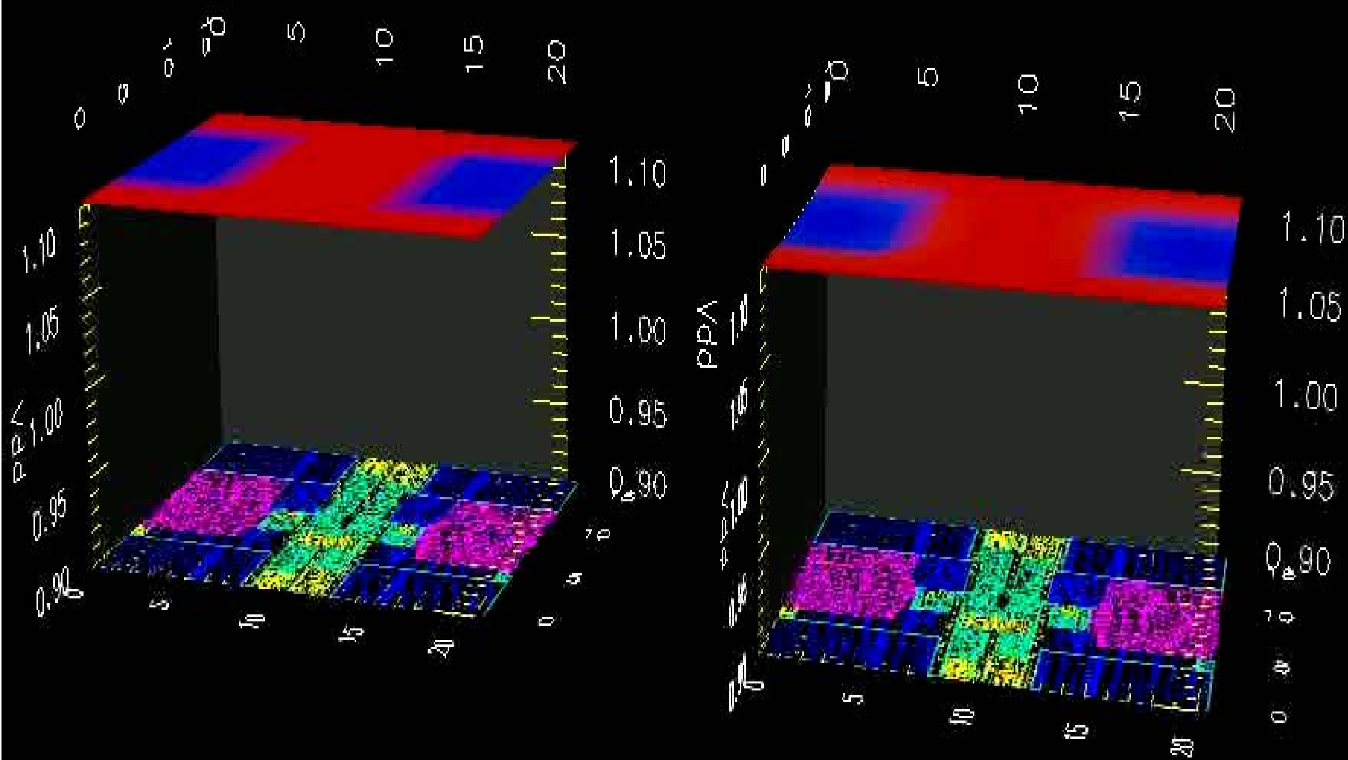
Trench based Decoupling

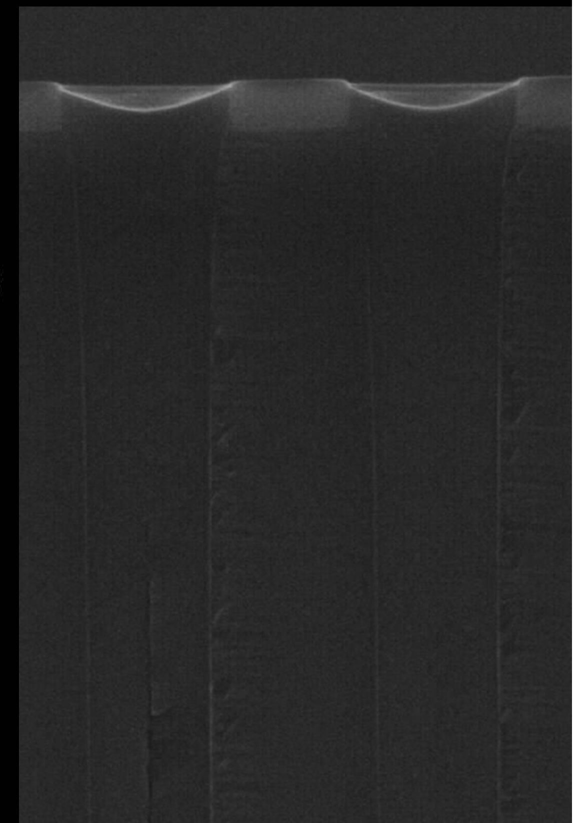
- Deep trench decoupling reduces this by over 100mV and enables a 10% reduction of power supply voltage at same performance
- Comes free with our embedded DRAM





Trench based Decoupling





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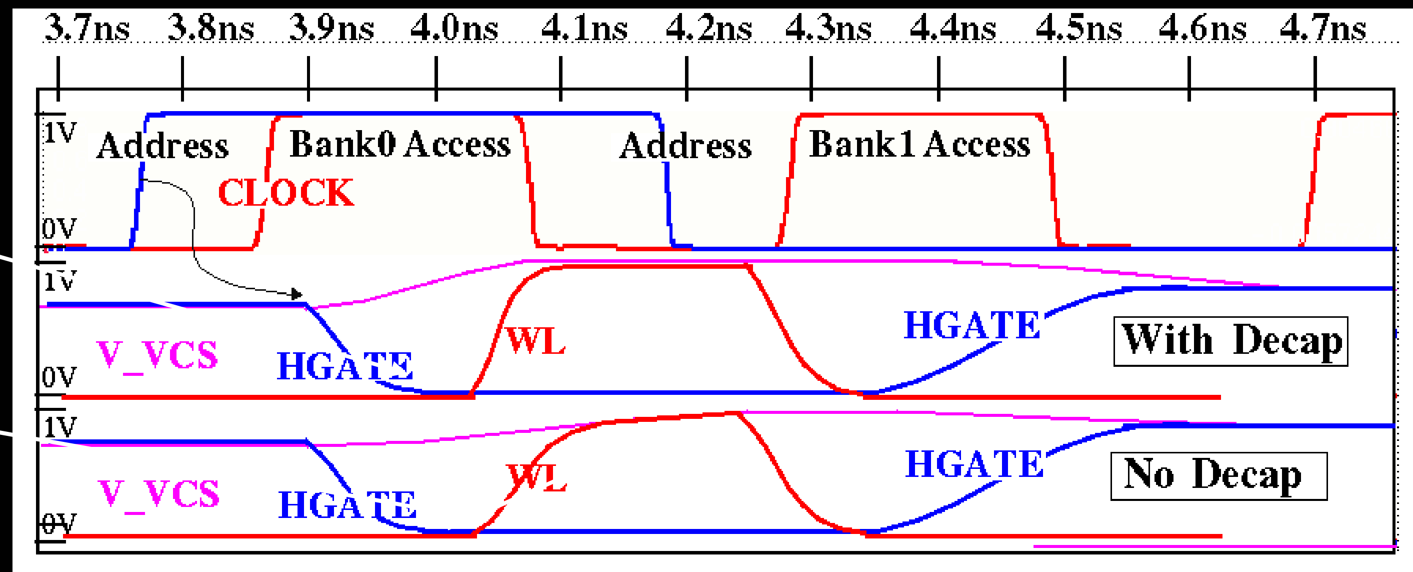
- **Current Solutions / Problems**
  - Header / Footer based power gating popular
  - Lower array supply to save on leakage (reduce V_{DS})
  - Problem occurs during Wake Up (access cycle)
  - Most schemes have wake up cycles for DI/DT
    - Power supply response time > 1ns
    - Need multiple wake cycles @ 3-4 GHz frequencies
  - **Area efficient local charge reservoir can help !**

Fast Charge up w/ decap

Slow RC without decap



Performance penalty

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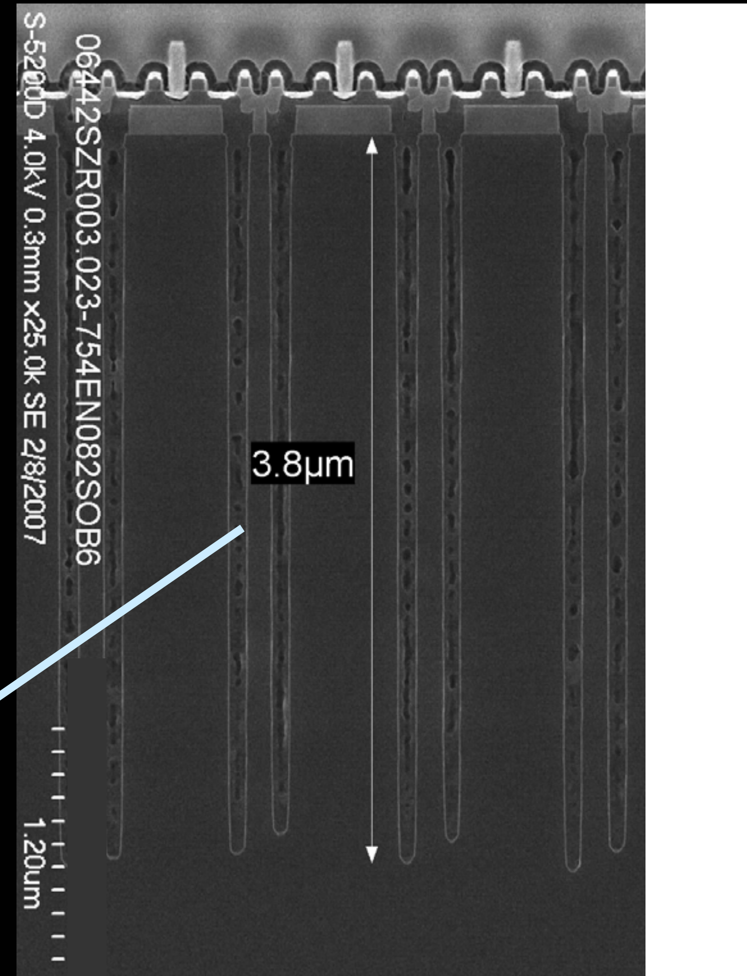
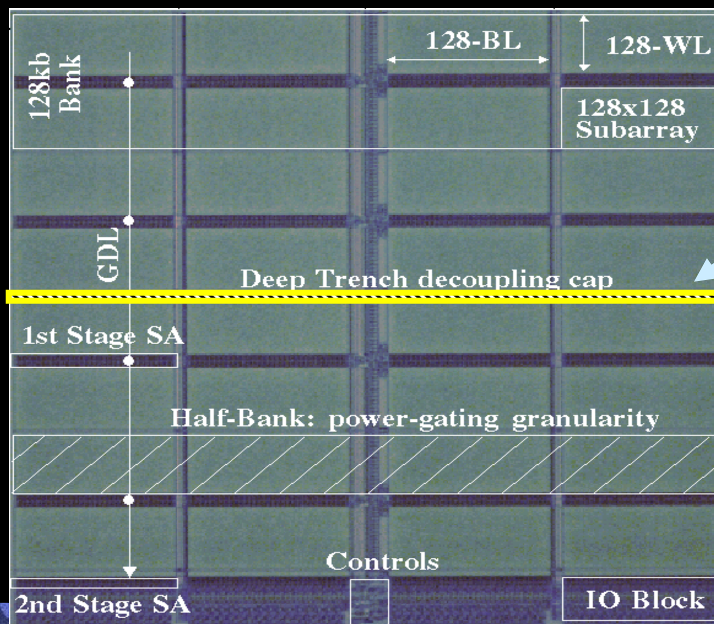
The DT Decoupling Cap 20X Advantage

- DT decoupling capacitance: 200fF/μm^2 vs. 11fF/μm^2 for thick-oxide depletion device
- Incorporated in 45nm ASIC Methodology
- Local array-supply charge reservoir to enable dynamic leakage reduction with NO wake-up cycles for > 2GHz operation



512Kb
ASIC
SRAM



< 2% area impact for 250pF of Embedded DT CAP

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Three Dimensional Integration – scaling in the third dimension

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Summary

- Scaling provides some density benefit
- Technology performance comes from technology features rather than scaling: eg Strain Engineering
- Hi K if can get us back to scaling for a short time
- Memory integration is a very big thing
- Chips will have more autonomic system level like functions enabled by technology features such as eFUSE
- Innovative decoupling can provide for upto a 10% performance improvement
- Three Dimensional Integration is the next huge thing

I would like to acknowledge the contributions of the 45nm , Hi K, embedded DRAM and eFUSE teams

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Yes……..
The Old Dog does learn new tricks

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